A Full Custom Front-End ASIC Prototype "CMAD" for COMPASS-RICH-1 Particle Detector System

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***Abstract*— An 8 channel, full-custom ASIC prototype, named "CMAD", designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN is presented.**

The task of the chip is amplifying the signals coming from fast multianode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

CMAD, developed using a 350nm commercial CMOS technology, occupies an area of $4.7x3.2mm^2$ and consumes $26mW/Ch$ power from a 3.3 V single source.

I. Introduction

COMPASS [1] is an experiment at the CERN SPS designed to study the structure and spectroscopy of hadrons with diverse types of high intensity beams. One of the key components of the experimental apparatus is a Ring Imaging CHerenkov (RICH) detector, used to perform particle identification.

In order to improve the reconstruction efficiency of the RICH, an upgrade is under development [2]. The experience gained with the first physics runs has shown that a trigger rate of 100 kHz and a single channel rate of 5 MHz should be sustained in order to reach optimal performance. These tight requirements can be achieved by detecting the photons produced in the sensitive volume by photomultiplier tubes equipped with fast read-out electronics. The granularity of the system demands the use of compact multianode photomultipliers (MPT). The increased event rate that the system has to cope with has motivated the development of a new front end (FE) ASIC.

CMAD, presented in this paper, will replace the MAD-4 [3] presently used in the read-out of the RICH-I. Produced in AMS 0.35 μm CMOS technology, the chip performs binary read-out of the MPT signals.

Section II gives an architectural overview, whereas section III deals with circuit design and finally section IV summarizes preliminary test results.

II. Architecture

Fig. 1 shows the architecture of a single channel. Each processing channel features a low-noise transimpedance amplifier followed by a shaper with 10 ns peaking time, a baseline holder (BLH), a comparator, a programmable oneshot to maintain the backward compatibility with the existing read-out system[4] and an LVDS driver.

The gain of the preamplifier can be adjusted from 0.4 mV/fC to 1.2 mV/fC in steps of 0.08 mV/fC. This allows to compensate at least partially for the channel-to-channel gain variation of the MPTs. Additionally, the threshold of each comparator can be adjusted on a channel by channel basis via a local 8-bit digital to analog converter (D/A). The gain of the front-end and the D/A codes are programmed using a digital control unit and the I2C standard.

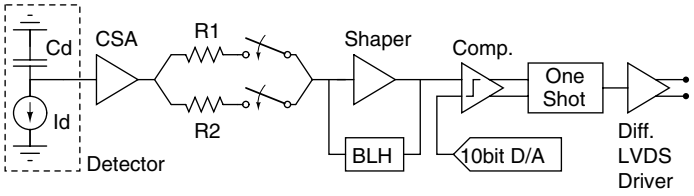


Fig. 1. Binary read-out architecture of a single channel.

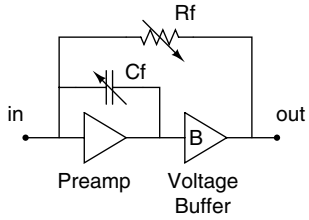


Fig. 2. Charge sensitive amplifier.

Charge Sensitive Amplifier (CSA) used as the first element of the chain is shown in Fig. 2. It consists of a basic amplifier with a capacitive feedback C_f, a voltage buffer B and a resistive feedback R_f as resetting device. Voltage buffer B is placed so to overcome the problem of open loop low frequency voltage gain drop due to the loading effect of R_f. The voltage buffer also allows for avoiding a direct coupling between C_f and possible input capacitances of the following stages.

The fast shaper shown in Fig. 3 is based on a class AB operational amplifier [5] around which two feedback networks are implemented. A fast path (shaper) performs high frequency filtering while a slow BLH feedback provides the AC coupling with the previous stage and guarantees baseline stabilization [6].

A fast unity gain buffer with limited slew rate is used in the baseline control loop. Fast signals at the output of the shaper are clipped before arriving at the transconductor stage. The baseline stabilization circuit (BLH) is designed to reduce the baseline shift to less than 3 mV for output pulses with a 3 V amplitude and 10 MHz rate.

As seen in Fig. 1, first stage (CSA) drives the second stage

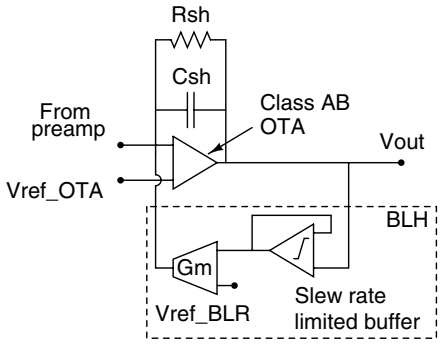


Fig. 3. Architecture of the shaper with BLH.

(shaper) with a current signal through an adjustable resistive connection. The design motivation is that this resistor allows for selecting the gain of the channel and properly current drive the second stage. This can be shown simply by inspecting the transfer functions of both the stages. Ignoring the voltage buffer B, the input integrator has a transfer function of the form

$$\frac{V_{out}}{I_{in}}(s) = \frac{A}{s(C_d + C_f) + sAC_f} \tag{1}$$

following a reasonable assumption of $A >> (C_d + C_f)/C_f$ yields

$$V_{out}(s) = \frac{1}{C_f}\frac{I_{in}(s)}{s} \tag{2}$$

and the inverse Laplace transform gives the approximate time domain output of CSA as

$$V_{out}(t) = \frac{Q(t)}{C_f} \tag{3}$$

confirming that the stage is an integrator. A similar simplification can be followed to achieve the transfer function of the shaper with BLH. The G_m block has a frequency dependent transfer function $f(s)$. Ignoring the slew rate limited amplifier and reverse transfer functions, the forward transfer functions of the second stage are

$$T_{low}(s) = \frac{1}{f(s)} \qquad and \qquad T_{high}(s) = T_{sh}(s) \tag{4}$$

where $T_{low}(s)$ and $T_{high}(s)$ are the transfer functions of the second stage at low and high frequencies and $T_{sh}(s)$ is the transfer function of the shaper without BLH feedback. $f(s)$ is low pass, so the first transfer function in Eq. 4 is a high pass filter. G_m stage has a narrow bandwidth such that the fast input signals can pass through the whole block without being affected. However, base line can move if the input rate increases. For that reason, a slew rate limited non-linear buffer is inserted before the G_m stage. This block dynamically clips the pulses to be processed by G_m block and reduces the area of large and fast signals significantly, preventing low frequency base line fluctuations. The transfer function of the whole circuit (CSA+Shaper) is achieved as

$$T(s) = \frac{T_{CSA}(s)T_{Shaper}(s)}{R_{1or2}} \tag{5}$$

confirming the design motivation of adjustable resistive drive between the first two stages as seen in Fig. 1.

The peaking time at the output of the shaper is 10 ns. The system has been designed to cope with a rate in excess of 5 MHz/Ch. The output pulses are stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels (Fig. 1).

III. Circuit Design

In the binary architecture given in Fig. 1, a global D/A can not be used since each of the read-out channels needs its own comparator that operates independently from the rest. This brings the necessity of a low power and small area D/A architecture, since it would be used for each read-out channel and thus more than once per chip.

Conceptually, the simplest D/As use a binary-weighted architecture, where n-binary weighted elements (current sources, resistors or capacitors) are combined to provide an analog output (n = D/A resolution). Digital encoding circuits are minimized, but the difference between the MSB and the LSB weights increase with increasing resolution, making accurate element matching difficult.

Among others like Kelvin divider or segmented architectures, the R-2R, or ladder, architecture relaxes component-matching requirements since only two component values are required in a 2:1 ratio. The R-2R architecture can be configured as a voltage- or current-mode D/A, together with different advantages and disadvantages.

A drawback of a current-mode R-2R architecture is the inversion introduced by the opamp which usually exists as an output current-to-voltage converter. Another disadvantage is the complicated stabilization of the opamp due to the fact that the D/A output impedance varies with digital input code. Current mode operation also results in higher glitch, since the switches connect directly to the output.

Advantage of voltage-mode R-2R configuration is that the output has constant impedance, thus simplifying amplifier stabilization. Glitch generated by switch capacitance is also minimized. The drawback of voltage-mode R-2R configuration is that the reference input impedance varies widely, so a low-impedance reference must be used. Also, the switches operate from ground to Vref, restricting the allowed range of the reference.

CMAD implementation employs Low Drop-Out regulators (LDOs) for setting the reference voltage and bias current of the D/A together with some other blocks. The technology used (0.35 μm) has relatively a high analog performance compared to recent low feature size technologies, so the amplifier compensation is easily achievable for the whole operation range. Relatively a high accuracy of matching is also feasible with proper layout.

Concerning the above discussion, transistor-only current-mode R-2R architecture is a suitable solution as it is composed of only transistors that are compact and that consume very low power. An important concern is also the output impedances driving the comparator, namely the outputs of the shaper and

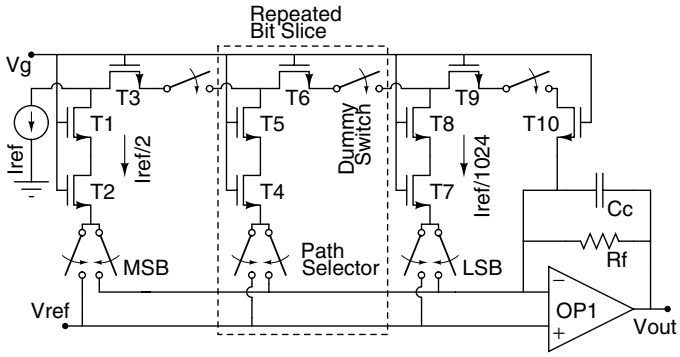


Fig. 4. 10b transistor-only R-2R architecture.

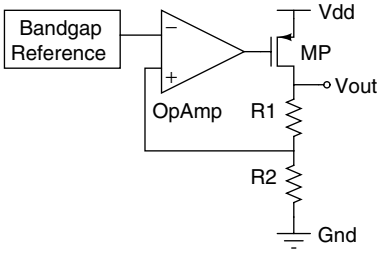


Fig. 5. LDO voltage reference.

the D/A. For proper functioning of the comparator input stage which is basically a differential pair, it is desired to equalize these impedances. The shaper has a low output impedance, thus requiring the same for the D/A.

Fig. 4 shows conceptually the architecture of the small area-low power 10-bit D/A used for setting the threshold of the comparator [7]. In such an architecture, transistors in the ladder do not necessarily emulate identical resistor values but instead, successful operation is based on linear current division principle [8]. The accuracy of the division technique used is based on the characteristic I-V curve matching of the two transistors but not on their linearity [9].

In operation, first two MSBs are set globally together with the base line and the effective resolution required by the channel is 8 bits. Additional pads are also provided for the flexibility of disabling the on-chip LDO reference to be able to apply external sources. The LSB, thus the resolution, of the D/A can be adjusted for different conditions, in this way.

Power consumption of the D/A in Fig. 4 is approximately 1.1 mW including the opamp. A current mirror implementation with the same functionality and power consumption would exhibit a much larger output impedance, affecting the comparator operation. CMOST-only R-2R core operates with 50 μA of current which is negligible compared to the one consumed by the opamp.

On-chip biasing is implemented via reference sources based on LDOs driven by band-gap voltage sources, as seen in Fig. 5. Linear voltage regulators use an active pass element (MP) to reduce the input voltage (Vdd) to the regulated output voltage (V_{OUT}). Linear voltage regulators force a fixed voltage level to appear at the output terminal [10].

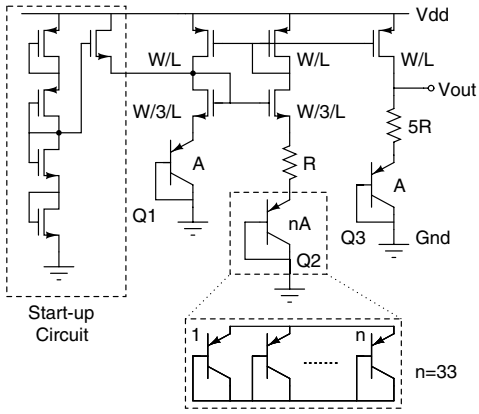


Fig. 6. Implemented opamp-less band-gap reference.

The LDOs implemented for CMAD are optimized for sub-circuit requirements and consume 0.9 mW from 3.3 V single source.

Fig. 6 shows the implementation of the opamp-less band-gap reference driving the LDOs. The reference voltage output is given as

$$V_{out} = V_{BE3} + 5V_T ln(n) \tag{6}$$

where V_{BE3} is the base-emitter potential difference of Q3, V_T is the thermal voltage and n (=33) is the area ratio between Q2 and Q1. Band-gap in Fig. 6 consumes 93 μW from 3.3 V single source.

IV. Test Results

Measurements showed good agreement with simulation results. Gain and the output pulse shape of the preamplifier is adjustable by controlling the values of capacitive and resistive components in the feedback path. These component values can be set either independently or in a correlated manner in order to preserve the shape of the output signal.

The gain of the preamplifier is a strong function of the resistor as seen in Fig. 7. In order to keep the signal with the optimum shape, the capacitor should be adjusted in such a way that the time constant remains the same. Capacitor value has only a slight effect on the preamplifier gain. It is utilized to adjust the time constant but not the gain itself. An increase in the binary code for resistor must be accompanied by an increased capacitor code. Reverse logic is used internally in the chip to preserve the direction of the digital code change maintaining the optimum signal shape.

Linearity of the preamplifier output is important for proper operation. Fig. 8 shows the measurement results. In the upper plot, circles represent the normalized preamplifier output values and the solid line is the linear fit. The nonlinearity is less than 2%, as seen in residual between data and linear fit given in the bottom plot of Fig. 8.

Designed to match the specific features imposed by fast multianode photomultipliers that guarantee full efficiency up to $5MHz/Ch$, the CMAD has to sustain the same event rate in order to overcome the limitation of MAD-4 at $1MHz$. Fig.

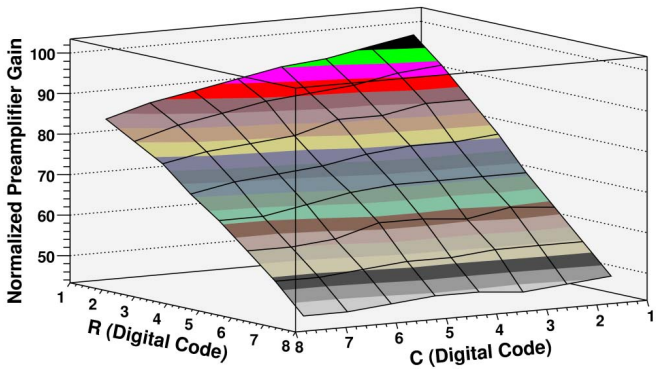


Fig. 7. Measurement results for adjustable gain of the preamplifier as a function of R and C binary D/A converter inputs.

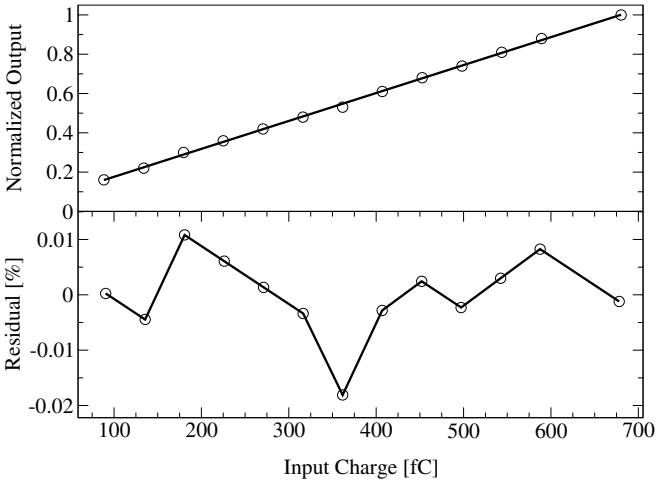


Fig. 8. Gain linearity of the preamplifier; measurement and linear fit (upper plot) and the difference between fit and measurement.

9 shows the efficiencies of CMAD and MAD-4 as a function of event rate, demonstrating that the new ASIC can effectively provide a higher rate, being fully efficient above $5 MHz/Ch$. The CMAD data in Fig. 9 were acquired both for the slew rate limiting buffer (SRLB), seen in Fig. 3, enabled (filled circles) and disabled (empty circles) cases.

V. Conclusion

An 8 channel, full-custom ASIC prototype, named CMAD, designed for the readout of the RICH-I detector system of the COMPASS experiment at CERN is presented.

In CMAD, threshold of each channel can be adjusted independent from the other channels. Thanks to low noise preamplifier, lower thresholds can be set individually to improve front-end performance. The new design provides a higher speed of more than 5 MHz/Ch with a lower power consumption of 26 mW. These features are specific to CMAD motivating the replacement of MAD-4 currently in use. Table I summarizes the specification details of CMAD and shows the layout.

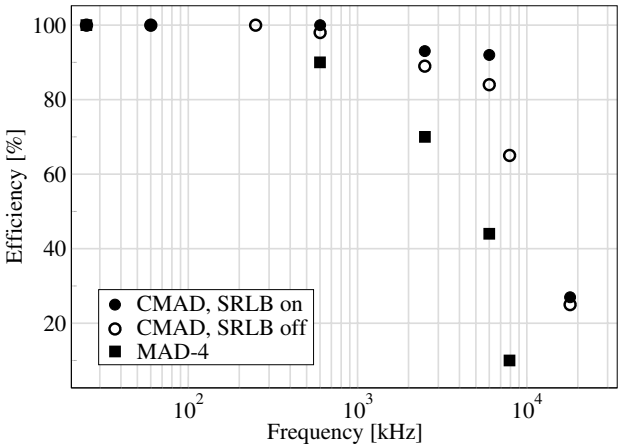
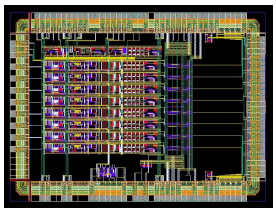


Fig. 9. Channel efficiency measurements both for CMAD and MAD-4 as a function of event rate.

TABLE I
CMAD Properties

Technology	0.35 μm
Number of Channels	$8/Chip$
Preamplifier Gain Range	0.4-1.2 mV/fC
Preamplifier Gain Resolution	0.08 mV/fC
Peaking Time	10 ns
Speed	>5 MHz/Ch
Chip Size	4.7x3.2 mm^2
Power (w/o LVDS Drivers)	26 mW
Layout	

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