

Laboratory and testbeam results for thin and epitaxial planar sensors for HL-LHC

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ABSTRACT: The High-Luminosity LHC (HL-LHC) upgrade of the CMS pixel detector will require the development of novel pixel sensors which can withstand the increase in instantaneous luminosity to $L = 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and collect $\sim 3000\text{fb}^{-1}$ of data. The innermost layer of the pixel detector will be exposed to doses of about $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$. Hence, new pixel sensors with improved radiation hardness need to be investigated. A variety of silicon materials (Float-zone, Magnetic Czochralski and Epitaxially grown silicon), with thicknesses from $50 \mu\text{m}$ to $320 \mu\text{m}$ in p- and n-type substrates have been fabricated using single-sided processing. The effect of reducing the sensor active thickness to improve radiation hardness by using various techniques (deep diffusion, wafer thinning, or growing epitaxial silicon on a handle wafer) have been studied. The results for electrical characterization, charge collection efficiency, and position resolution of various n-in-p pixel sensors with different substrates and different pixel geometries (different bias dot gaps and pixel implant sizes) will be presented.

KEYWORDS: CMS; Pixel; Phase 2 upgrade; HL-LHC; thin, planar sensors; silicon.

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1. Introduction

The current CMS pixel detector [1] was designed to operate up to a fluence of 6×10^{14} n_{eq}/cm². New radiation hard sensors are required for the High Luminosity upgrade of the LHC (HL-LHC), which is expected to reach an instantaneous luminosity of $L = 5 \times 10^{34}$ cm⁻²s⁻¹ and to collect $\sim 3000\text{fb}^{-1}$ of data [2]. The innermost layers of pixel detectors will be exposed to a dose of about 10^{16} n_{eq}/cm² during the operation of HL-LHC. This is ten times higher than the design fluence of the current detector.

A variety of pixel technologies (3D, diamond, HV-CMOS) are being proposed for the HL-LHC upgrade of CMS experiment. These technologies offer improved radiation hardness, but most of them are expensive and difficult to produce compared to planar sensors. In order to continue using planar sensors for HL-LHC upgrade of CMS, their radiation hardness needs to be improved.

The radiation hardness of planar silicon sensors can be improved by reducing the active thickness of the bulk (down to 120 μm , or perhaps even 50 μm), while still collecting good charge above the readout chip threshold. Detectors with thin active layers require lower bias voltages to achieve full depletion after irradiation. The reduction of active thickness also improves the electrical field

inside the sensor and shortens the charge collection length, which increases the charge collection significantly after heavy irradiation. Furthermore, charge multiplication effects have been reported in many epitaxial sensors [3], which can improve the amount of charge collected after heavy irradiation. The CMS Phase1 Upgrade readout chip has a threshold lower than 2,000 electrons and therefore, can be used to study the performance of thin silicon sensors.

In this paper, we report on the laboratory and testbeam measurements results for various thin n-on-p pixel sensors. The results for electrical characterization (I-V, C-V), laboratory measurements (noise and charge collection efficiency using a Sr^{90} source), and testbeam measurements (cell efficiency, charge collected and position resolution) will be presented.

1.1 CMS Tracker Campaign

In order to find a suitable silicon base material for the upcoming HL-LHC upgrade of the CMS Tracker, the CMS collaboration started a large campaign to investigate the properties of thin, single sided silicon sensors [4]. 164 wafers carrying several different designs have been produced by Hamamatsu Photonics K.K. (HPK) in Japan. Several wafers with the same mask design, but different silicon base material (Float Zone (FZ), Magnetic Czochralski (MCz) and Epitaxial (E) silicon), and wafer thickness (50 μm to 320 μm) were fabricated.

The sensors discussed in this paper are identified with a naming convention that includes silicon type (FDB: float-zone with deep diffusion, active thickness of 120 μm and physical thickness of 320 μm ; E: active thickness 50 μm and 100 μm on a handle wafer, total thickness of 320 μm), and doping type (N: n-type; P: p-type with p-stop; Y: p-type with p-spray). Sensors from a few other layout types (FZ320, MCz200) were also measured for comparison.

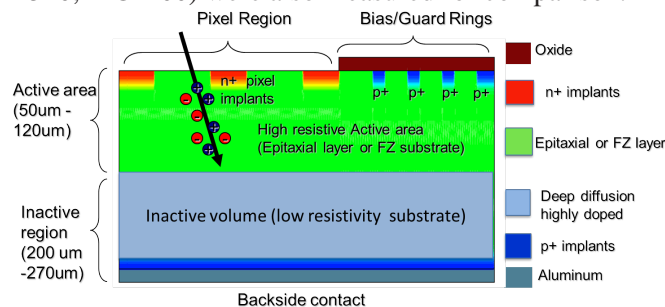


Figure 1. Schematic cross-section layout of thin, planar sensors using different active substrates.

1.1.1 Reduction of active thickness

Various techniques have been used in order to reduce the active sensor thickness, such as deep diffusion, wafer thinning, and epitaxial silicon. Figure 1 shows the generic cross-sectional layout of thin, planar sensors produced for this campaign.

For FDB sensors (FDB120), instead of thinning the bulk of FZ sensors by using a handle wafer, diffusion of dopants very deep into the sensor was performed. This highly doped backside region (resistivity: 0.5-2 Ωcm for FDB120) cannot be depleted, and thus does not contribute to active sensor volume (resistivity: 3-8 $k\Omega\text{cm}$). However, there is a soft transition between highly doped backside and active volume, as compared to the sharp transition obtained in wafer bonding process. This leads to interface effects and higher than expected charge collected by the sensor.

Another method to reduce active volume of the device is to use epitaxial technology. A thin layer (50-100 μm) of highly resistive, epitaxial silicon (resistivity of 0.5-2 $k\Omega\text{cm}$) is deposited by

CVD process on top of a handle wafer with very low resistivity (resistivity of $5E-4 \Omega cm$). Thus, the active area of sensors in the epitaxial process is limited by thickness of the epitaxial layer as shown in Figure 1. The epitaxial layer deposition process is slow and costly compared to FZ and MCz processes.

1.1.2 Single sided processing: n-on-p layouts

Instead of traditional "n-on-n" designs which have been used for the current CMS pixel detector, "n-on-p" designs were investigated for this campaign. n-on-p sensors do not suffer from type inversion, collects electrons which have higher mobility and reduced charge trapping compared to holes. Furthermore, n-on-p sensors can be fabricated with single sided processing which improves costs significantly by reducing the number of masks and processing steps required to almost half.

1.2 Sensor layouts

A total of 6 layouts were realized to study the effect of bias dot size (BPIX), and region between p-stops and pixel implants (FPIX) on the electrical and charge collection properties of pixel sensors. The pixel sensors were designed similar to the layout of current CMS Forward Pixel (FPIX) ([1], [5]) and Barrel Pixel (BPIX) ([6]) sensors, with pixels of $150 \mu m \times 100 \mu m$ pitch. For FPIX, two designs with a single open p-stop ring, and different gap sizes were fabricated: the gap size for FPIX-E (Figure 2 (a)) and FPIX-F (Figure 2 (b)) are $\sim 30 \mu m$ and $50 \mu m$ respectively. For BPIX, four layouts with different gap sizes between bias dot and pixel implants were fabricated: BPIX A-C (Figure 2 (c)): gap in the bias structure between $14 \mu m$ ($\sim 8\%$ of total pixel area) and $22 \mu m$ (16% of total pixel area) with interpixel gap of $36 \mu m$, BPIX-D (Figure 2 (d)): small bias structure, $10 \mu m$ gap ($\sim 5\%$ of total pixel area) and $22 \mu m$ interpixel gap. FPIX-F and BPIX-D are most similar in design to the current CMS pixel sensors.

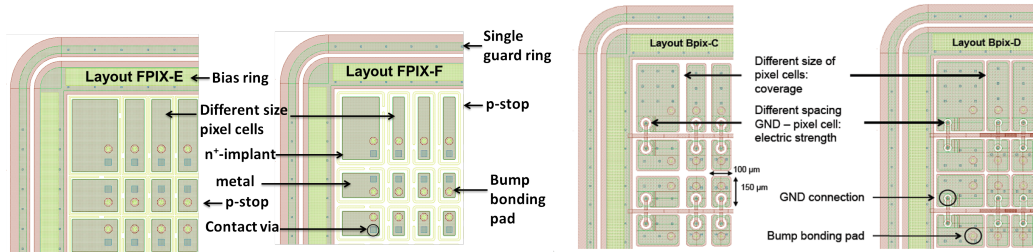


Figure 2. Detailed layout of different FPIX-E (a), FPIX-F (b), BPIX-C (c) and BPIX-D (d) sensors from HPK Tracker campaign.

2. Electrical characterization

2.1 IV and CV measurements

The pixel sensors were diced out from the wafers without any further processing (no under bump metallization or deposition of bumps) since the wafers contained several other structures (strips, test structures, etc.) which were used for Tracker campaign [4]. The electrical characterization (I-V and C-V measurements) of HPK pixel sensors was performed in the laboratory at room temperature. The leakage current, I_L , was again measured after bump bonding for quality control. Figure 3 (left) shows the measured I_L as a function of the bias voltage, V_{Bias} for E50P FPIX sensors (p-type bulk and p-stop isolation). FPIX-E sensors (dotted curves) with larger n^+ implants, and smaller gap between p-stops have smaller currents and earlier breakdowns (350V-380V) compared with

FPIX-F sensors (solid curves) which have higher leakage current, and higher breakdown voltages (450V-500V). This is expected due to the larger surface current and higher electric field at the edge of p-stops in pixel sensors with smaller implants. Similar trend in breakdown voltage is also observed for E100P and FDB120P FPIX sensors.

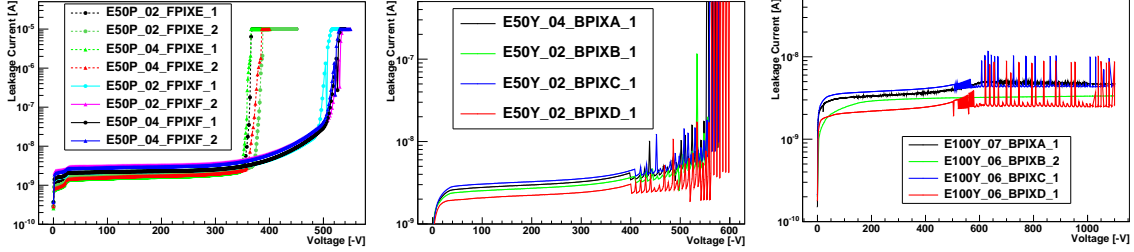


Figure 3. I-V measurements of E50P FPIX E-F (left), E50Y BPIX A-D (middle) and E100Y BPIX A-D sensors.

I-V curves for E50Y (p-type bulk and p-spray isolation) BPIX layouts are shown in Figure 3 (middle). All the different E50Y BPIX layouts have similar leakage currents, and show similar breakdown voltage (550V-600V). I_L for various E100Y BPIX sensors (Figure 3 (right)) shows a soft breakdown around 500V, but do not show hard breakdown until 1100V. I_L for FDB120Y BPIX layouts (Figure 4 (right)) also shows similar I-V behavior. TCAD simulations need to be performed to understand the cause of this soft breakdown behavior and noisy leakage in BPIX layouts.

In order to compare the effect of p-spray isolation on FPIX layouts, some E50Y, E100Y and FDB120Y FPIX sensors were also bump bonded and measured. Figure 4 (left) shows the I-V for E50Y and E100Y, and Figure 4 (right) shows the I-V for FDB120Y FPIX layouts. FPIX-F layouts with smaller implants and p-spray isolation (solid curves) tend to break down earlier (at ~ 380 V) compared to FPIX-E layouts (dotted curves) which have a very gradual breakdown around 450V. This trend is opposite to the FPIX layouts realized with p-stop isolation, as shown in Figure 3 (left). This effect is caused by stronger electric fields at the edge of implants in FPIX-F layouts with p-spray isolation.

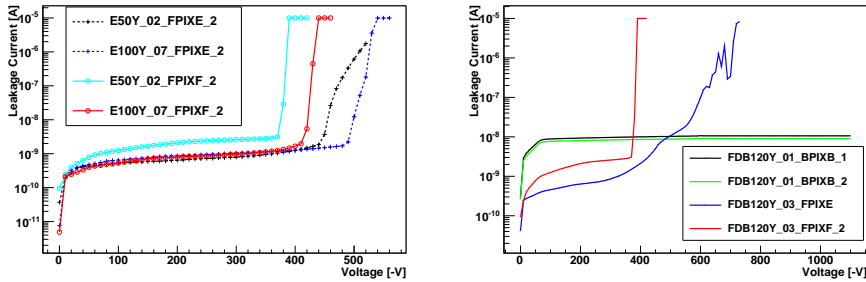


Figure 4. I-V measurements of E100Y, E50Y FPIX (left) and FDB120Y (right) p-spray FPIX/BPIX layouts.

C-V measurements were also done on bare dies to estimate the depletion voltage of different layouts and sensor thickness. All BPIX layouts in general have higher depletion capacitance compared to FPIX layouts. Figure 5 (left) shows the C-V curves for E50P FPIX and E50Y BPIX layouts. E50P FPIX devices deplete ~ 24 V, while E50Y BPIX layouts fully deplete ~ 38 V. E50 FPIX with p-stop (E50P) layouts have smaller full depletion capacitance (15pF) compared to E50Y BPIX layouts with p-spray (100pF), which suggests that E50Y BPIX sensors are expected to be

more noisy during operation. E100Y BPIX have similar depletion voltage ($\sim 35\text{V}$ - 40V for BPIX A-C and $\sim 25\text{V}$ for BPIX-D) as E50Y BPIX sensors, but have lower depletion capacitance. Figure 5 (right) shows the C-V curves for FDB120Y FPIX and BPIX layouts. Depletion voltage of FDB120Y (Figure 5 (right)) FPIX sensors is 10V , while BPIX sensors deplete in 55V - 60V range.

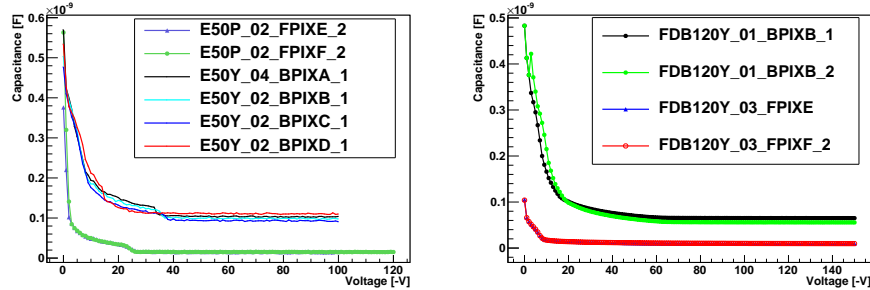


Figure 5. C-V measurements of E50P FPIX E-F and E50Y BPIX A-D sensors (left), and FDB120Y FPIX/BPIX sensors (right).

2.2 Bump bonding and Edge passivation

Most of the sensors were initially bump-bonded to the 2005 CMS PSI46v2 Read-out Chip (ROC) [7], which is the older, analog chip with higher threshold. In order to use lower threshold for studying thin sensors, a few pixel sensors were also bump bonded to the new CMS PSI V2B digital chip [8], which can survive higher levels of irradiation ($1.5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$).

The sensors were bump bonded at Princeton University's PRISM Micro Nano Fabrication facility. Photolithography was done on individually diced sensors which reduced the bump bonding yield significantly. Indium was used as the bump solder material. 100 nm of Ti-W was sputtered as UBM, then $4\text{-}6 \text{ }\mu\text{m}$ of Indium metal was deposited using a thermal evaporator. Measurements indicate that the final gap between sensor and ROC varied between $4\text{-}6 \text{ }\mu\text{m}$ on average.

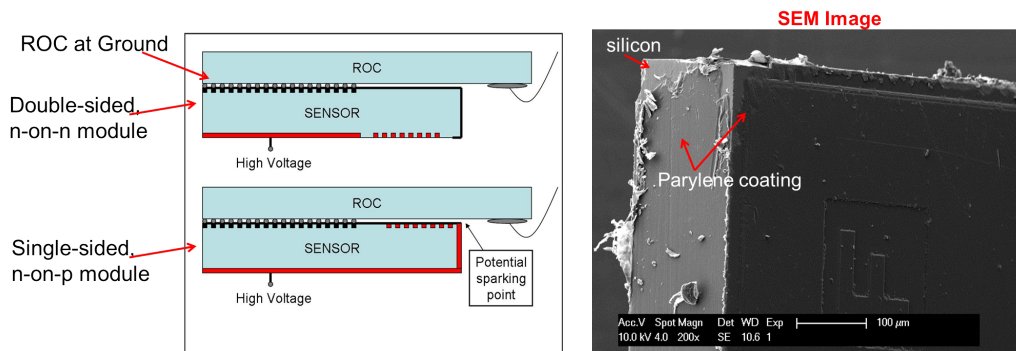


Figure 6. Double sided vs single sided modules (left) and SEM micrograph showing parylene coating over a FZ320Y FPIX sensor (right).

Due to the soft nature of indium bumps and absence of reflow after bump bonding, the gap between the sensor and ROC obtained was less ($<10 \text{ }\mu\text{m}$) than conventional Pb-Sn bumps ($\sim 20 \text{ }\mu\text{m}$). Since these sensors were fabricated using a single-sided process, there is a potential for arcing in the small air gap (dielectric strength of air is only $3\text{V}/\mu\text{m}$) between the edge of sensor (which is at sensor bias voltage) and ROC (which is at the ground potential). Figure 6 (left) shows the cross-section of an n-on-p module showing the potential arcing region. In order to avoid arcing, a dielectric

material (Parylene-N) was applied using a CVD process at Purdue’s Birck Nanotechnology Center. Parylene-N has very good dielectric strength ($280 \text{ V}/\mu\text{m}$), provides good passivation, and is highly conformal. SEM micrograph of the sensor after coating (Figure 6 (right)) shows that a uniform coating was deposited over the entire sensor surface, including the gap between sensor and ROC. We have also shown that Parylene-N does not affect the leakage current and capacitance of the sensors up to 1100V, even after irradiation up to a dose of $2\text{E}15 \text{ neq}/\text{cm}^2$.

2.3 Laboratory measurements

Sensors were tested with a $1\text{mCi } \text{Sr}^{90}$ radioactive source in the laboratory. The PSI analog and digital test-boards, and DAQ software were used as the DAQ system for lab measurements with analog ROC [7] and the new digital ROC [8].

2.3.1 Noise

The S-curve test was used to determine the pixel noise by sending internal calibration signals through the injection capacitor to the ROC preamplifier input, and measuring the response efficiency on a pixel-by-pixel basis. Figure 7 (left) shows that the measured noise for HPK sensors of different substrate thickness saturates to $120e^- - 140e^-$ after full depletion. In general, smaller pixel implants leads to lower inter-pixel capacitance, and thus lower noise values. BPIX layouts ($140e^-$) have slightly higher noise than FPIX layouts ($120e^-$) for same substrate type - all the noise results are in agreement with the C-V results obtained earlier.

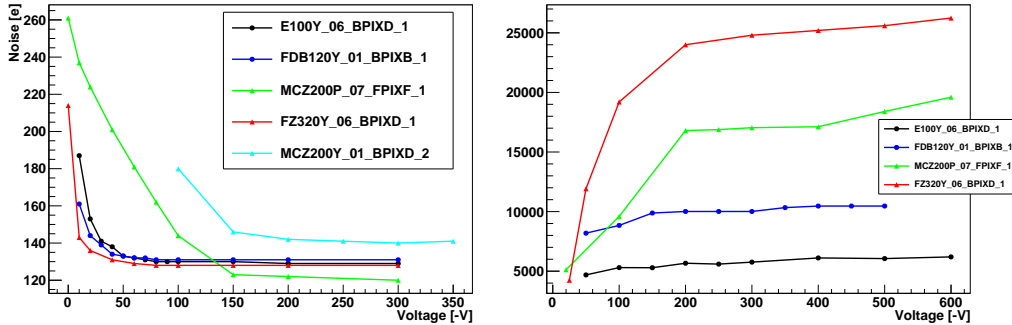


Figure 7. Noise (left) and charge collected (right) as a function of applied bias for different HPK sensors.

2.3.2 Charge collection using a source

Charge collection was measured in the laboratory with a Sr^{90} source for all sensors. The analog ROC was operated with a threshold of 3.9 ke^- , while the digital ROC was operated at a threshold of 2 ke^- . Although it is possible to reduce the threshold of the digital ROC even lower, it appears that operating at lower thresholds (1500 e^-) makes the chip noisy and causes multiple double columns to freeze randomly.

Figure 7 (right) shows the charge collected as a function of bias voltage for various HPK sensors. The amount of charge collected increases at larger values of V_{Bias} for MCZ200 and FZ320 devices, while charge collected for E100 and FDB120 sensors saturate very quickly. This is due to the lower depletion voltage of E100 (25V-40V) and FDB120 (55V-60V) sensors compared to MCZ sensors (80V-100V). Large number of size 2 clusters were observed since the sensors were placed at some distance above the Sr^{90} source.

There are small differences between measured charge and expected values of charge collected (assuming 80 electron-hole pairs generated per micron thickness in silicon at room temperature) for FDB120 and E100 sensors. The PSI ROC was optimized for reading out the charge from $\sim 300 \mu\text{m}$ sensors, and has a good linear pulse height (PH) curve in the high charge regions. But in low charge region, the ROC gain is non-linear which affects the measured charge.

3. Testbeam Measurements

Sensors were tested with 120 GeV/c protons at the Fermilab Meson Test Beam Facility. The Fermilab testbeam setup is described in detail in [9]. A telescope made of eight planes of planar CMS pixel detectors was used to reconstruct the tracks. The intrinsic track resolution of the telescope is about $7 \mu\text{m}$ in both the X and Y local coordinates.

3.1 Charge collection efficiency

Figure 8 shows the Landau distribution (left) of the charge collected for single pixel clusters of E100Y BPIX-B sensors bump bonded to analog chip (threshold of $3.9 ke^-$). The amount of charge collected depends on the position of the incident particle with respect to the pixel implant. Figure 8 (right) shows the detailed charge collected for a 4x4 pixel array. Even after punch-through, there is still charge loss in the bias dot, and the gap between bias dot and the implant region. Also, the metal grid providing the bias voltage to the sensor was left floating after bump bonding, so there is significant charge loss in the bias grid area. There is added loss due to charge sharing along both the pixel edge regions. Charge collected as a function of bias voltage was also measured and is similar to the values obtained with a radioactive source as given in Section 2.3.2.

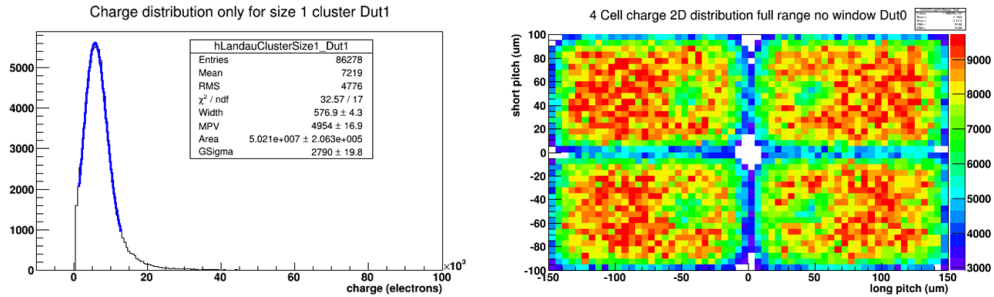


Figure 8. Landau distribution of charge collected in beam test (left) and charge collected for a 4x4 pixel array (right) for Epitaxial $100 \mu\text{m}$ BPIX-B layout sensor using analog chip at 300V.

3.2 Tracking Efficiency

The hit efficiency in a pixel cell was measured for both FPIX and BPIX sensors using events with single tracks. Figures 9 (left) and 10 (left) show the efficiency for a 4x4 array of pixels for E100Y BPIX-B and FDB120Y BPIX-B sensors respectively. The chip was operated at a threshold of $3.9 ke^-$ and the detector was orthogonal to the beam (angle of 0°). The measured average hit efficiency was 95.4% for E100Y BPIX-B and 96.8% for FDB120Y BPIX-B at 0° . The low hit efficiency is explained by the charge loss in the bias dot and metal grid, which are partially inactive volumes.

The loss in efficiency due to the bias dot is recovered by rotating the sensor. The pixel efficiency increases by rotating the Detector Under Test (DUT) on the short pitch with respect to the beam axis, reaching a value of 95.7% for E100Y BPIX-B at an angle of 25° (Figure 9 (right)), and 98.5% for FDB120Y BPIX-B at an angle of 20° (Figure 10 (right)). However, rotating the

DUT also increases charge sharing which reduces the amount of charge collected along the edges of pixel below chip threshold, and causes loss in efficiency along the pixel edges. Thus, there is no significant improvement in efficiency for E100Y BPIX-B sensor. However, due to the higher charge collected inside each pixel for FDB120Y BPIX-B sensor with same pixel layout, rotating the sensor to 20° improved the cell efficiency from 96.8% at 0° to 98.5% at 20° . Rotating beyond 20° did not improve efficiency further due to increased charge sharing.

Even after rotation, some loss in efficiency is still observed in the bias grid area for BPIX layouts. In order to ensure that the bias grid is properly grounded, the CMS pixel sensors contained 2 extra bumps to short the entire bias grid to the ground potential of ROC which was missing in HPK sensors (making the bias grid floating). This can be easily corrected by changing the mask for bump metal deposition.

Similar detailed studies were also done on different FPIX layouts, and very good charge and efficiency values were obtained, especially in the region between pixel implant and p-stop isolation. Due to space constraints in this paper, we omit the detailed results for FPIX sensors.

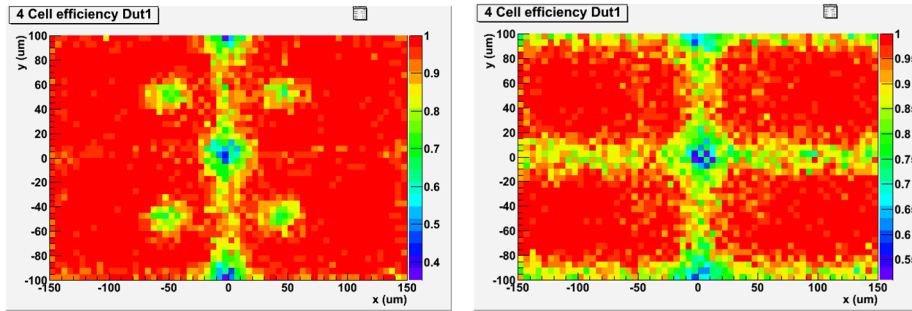


Figure 9. Hit efficiency of Epitaxial $100\ \mu\text{m}$ BPIX-B layout at 0 degree (left) and at 25 degrees (right) at 300V (depletion 40V) and $5\ ke^-$ average charge collected.

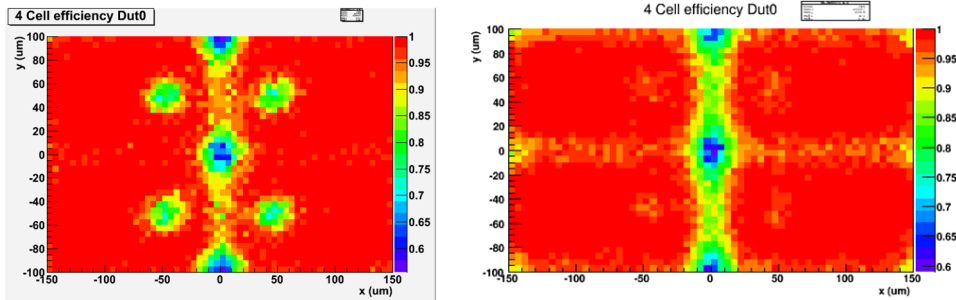


Figure 10. Hit efficiency of Deep diffusion FZ $120\ \mu\text{m}$ BPIX-B layout at 0 degree (left) and at 20 degrees (right) at bias of 300V (depletion 55V) and $9.5\ ke^-$ average charge collected.

3.3 Efficiency vs. Bias and Angle

Figure 11 shows the the hit efficiency as a function of the V_{bias} (left) and rotation angle (middle). E50Y BPIX-A and E100Y FPIX-F were bump bonded to digital chip (threshold of $2\ ke^-$), while E100Y BPIX-B and FDB120Y BPIX-B were bump bonded to the analog chip (threshold of $3.9\ ke^-$). Charge collected and hit efficiency typically increases as a function of V_{bias} , up to full depletion voltage after which both the charge collected, and pixel hit efficiency remained al-

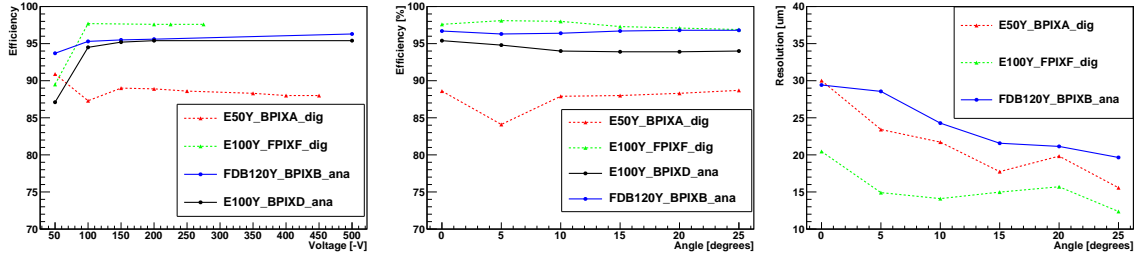


Figure 11. Hit Efficiency vs. Bias (left) and vs. angle (middle), and Resolution vs. angle (right) of different Epitaxial and Deep diffusion FZ sensors.

most constant. The only exception was E50Y BPIX-A whose efficiency reduces slightly with the increase in bias voltage. This result is unusual and is under investigation.

Figure 11 (middle) shows the hit efficiency as a function of rotation angle. As the sensor is rotated, the efficiency slightly improves for FDB120Y BPIXB sensor while the efficiency for both E100Y BPIXD and E100Y FPIXF slightly decreases. This has been explained above as a result of reduced charge collected after charge sharing, which causes a loss of efficiency along the inter-pixel regions. The efficiency for E50 in general, was significantly lower compared to E100 and FDB120, which is due to lower charge collected by E50 sensors.

Track residuals are calculated as the distance between the predicted and measured positions of a cluster. Figure 11 (right) shows the track residual as a function of rotation angle for different FPIX and BPIX sensors.

4. Conclusions and Outlook

This paper presents the pre-irradiation lab and testbeam measurement results of thin, planar sensor designs from different substrates. Using digital ROCs with lower thresholds improves the charge collection and tracking efficiency. In general, 120 μm sensors show good charge collection results, high tracking efficiency and good spatial resolution, while 50 μm and 100 μm designs suffer from reduced charge collected after rotation due to charge sharing, which reduces the hit efficiency in the inter-pixel regions.

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