Production and Test of a Readout Chip for the ALICE SDD Experiment

Samuele Antinori, Davide Falchieri, Alessandro Gabrielli, Enzo Gandolfi

INFN & Physics Department University of Bologna

Viale Berti Pichat 6/2 40127 Bologna Italy

Tel. +39-051-2095052 FAX +39-051-2095297 E-mail: gabrielli@bo.infn.it

Abstract

The paper summarizes the design, the fabrication and test of a chip for the silicon drift detector experiment, part of the A Large Ion Collider Experiment (ALICE) at CERN. The chip performs data reduction via bi-dimensional compression and packing for the readout chain of the experiment. The chip interfaces with front-end electronics and with the counting room. It is synchronized with a 40 MHz system master clock and configured via a serial signal. The work presents the tests that were performed to characterize the chip and it exploits the final yield of 89% over 700 fabricated chips. The whole tests were performed in laboratory and the chip was also tested in a test beam at CERN on November 2004.

PACS 07.05.Hd, 84.30.-r, 84.30.Qi, 85.40.-e

Keywords: SDD, ALICE, CARLOS, ASIC

I. Introduction

This paper describes the design, the construction the tests of a digital rad-tolerant chip, part of the A Large Ion Collider Experiment (ALICE [1], [2], [3]) Silicon Drift Detector (SDD) [4] which functions as a data compressor [5] and JTAG switch for Front-End Electronics (FEE) of the experiment. Named CARLOS, the chip was designed via radiation tolerant 0.25μm digital library derived from a commercial technology. In particular the chip is an Application Specific Integrated Circuit (ASIC) [6], [7] designed and developed in the context of the ALICE collaboration, both in the Physics Department of Bologna University and at CERN. However its general bidimensional compression algorithm could be applied to high-energy physics experiments where detectors provide long dataset streams that require off-line compression [8]. In the context of SDD experiment the length of this stream, i.e. the number of incoming data words that constitute the event, depends on the number of anodes in the detectors and the length of the data for each anode (i.e. the number of 8-bit samples per event per anode). Here, each detector is made up of two 256-anodes half-detectors. Event data are received by the bi-dimensional compressor in the form of a stream of 8-bit data, synchronous with a 40 MHz clock. The CARLOS chip can be configured to handle anode data lengths from 8 up to a maximum of 256 samples and writes 16-bit output words at 40 MHz. Thus the event data may consist of a stream of up to 256×256 8-bit data samples. Indeed, CARLOS contains a bi-dimensional compressor per channel that detects, encodes and pack output data. Thus, it may handle the two different streams originated from the two half-detectors that make up one SDD. The chip design passed through three prototypes to characterize its functions. Now the production has been fabricated and all the 700 chips have been tested in the final version.

II. CARLOS chip

CARLOS has been designed mostly by means of the VHDL language and implemented on a 0.25μm CMOS 3-metal rad-tolerant digital library. The chip implements 4 rad-tolerant full-custom 256-words RAMs [9] that have been designed separately and imported as black boxes in the whole chip. The library itself has been developed at CERN to be applied into the experiment electronics even though it is basically derived from a

standard 0.25μm CMOS commercial technology. CARLOS is composed of nearly 15k gates, 88 user pads out of the 100 total pads, it is clocked at 40 MHz, and the whole die area is 4×4 mm^2.

The radiation hardness of the chip is mainly obtained by means of dedicated transistor layout geometry: the enclosed gate transistors [10]. This particular technique guarantees the radiation hardness of the transistors under the total ionizing dose of the experiments that is expected to be some tens of krad. Figure 1 shows a picture of the final layout of CARLOS.

A. Bidimensional Compressor

Most of the 'pixels' in the bi-dimensional data matrices delivered to the CARLOS chip by the Front-End Electronics (FEE) cards contain digitized noise signal that should be rejected to achieve a significant compression of the dataset. However, in general hits are not confined to a single pixel but will cluster over adjacent pixels both in the coordinate defined by the anode array and in the drift-time coordinate. The cluster is defined by a five cross-like 8-bit pixel structure as shown in Fig. 2. The cluster is recognized essentially if at least one of the five pixels is above a predefined high-threshold and, at the same time, at least one other pixel of the cross is higher than a second predefined low-threshold (obviously lower than the high-threshold). When both conditions are met the central point of the cross is encoded and compressed and sent to the compressor's output. In particular, the compressor applies a Huffman-like [11] encoding and compression scheme to the selected data [8]. In more detail, the cluster finding technique is applied sequentially pixel-by-pixel across the matrix. If the cluster is isolated, separated from others, the encoded data value is transferred together with its position within the matrix. This case applies always at the beginning of a multiple cluster. Conversely, if the cluster is a continuation of a previously detected adjacent cluster, its position is already known since it is "the previous one + 1" and the encoded data are transferred without any position information. In case no cluster is detected no information is sent to the output. The two programmable threshold values can be adjusted so that the latter case is the most frequent, thereby resulting in a significant reduction of the transmitted data.

Fig. 2 illustrates a full-event matrix containing a single cluster and a multiple cluster. Each row of the matrix corresponds to the samples from a different anode. The five pixels of a potential single cluster are labeled EAST, CENTER, WEST, NORTH and SOUTH. Each CARLOS chip carries out the digital compression, whatever the dataset length. The chip only recognizes, from time to time, events made up of datasets formed by up to 256×256×8-bits that correspond to a silicon drift detector (256-samples times 256-anodes). The matrix can be made up of a smaller dataset depending on the number of samples that form each anode.

III. CARLOS TESTS

The CARLOS chips were randomly selected from the central lines of the silicon wafer during manufacture and were slightly stressed in frequency and voltage supply as summarized in Table I. About 700 chips were fabricated and fully tested. At higher clock frequencies compared to what is reported in the table, they begin to fail. At the required 40MHz clock frequency, the chips consume power at a level of 275mW. The table also summarizes average current consumption over the tested chips and relative current deviation of 0.5 mA. Voltage supply varies from 2.1 V to 2.7 V.

At first CARLOS was stimulated using the identical test vectors applied during post-layout simulation in the chip's design phase. Fig. 4 shows a picture of a portion of the board used to test the chips. A Zero Insertion Force (ZIF) has been used to plug-and-play the vectors. The pattern generator provided a 100 k-word test bench including the configuration and two 50-kword events. Then the datasets read by the logic analyzer were processed using a dedicated SW tool to reconstruct the original input dataset. In other words, this tool performs the reverse function of CARLOS. The tool then compares the actual input values with the reconstructed ones and lists errors in case of any mismatch. This software tool has helped to automate CARLOS tests and allowed us to reach conclusions about the data acquisition chain's overall functionality.

A brief summary of the to date tests on 700 chips is reported below:

- 623 chips work properly,
- 77 chips fail

As the dies were randomly selected from the wafers, it is reasonable to assume that most of the non-working components originated from bugged portions of the silicon. In fact, 4×4 mm^2 of silicon in a 0.25μm CMOS technology is not a huge area for digital chips and the expected yield would have been higher than what has been observed to date (623/700) 89%. In addition, with low production numbers and in multi project wafers the yield may vary significantly in respect of average technological values.

Besides the mentioned input patterns, other test benches were used to stimulate CARLOS including 48k-word events with random generated values, gaussian generated values and data originating from a test beam.

A. Tests on Bi-dimensional Compressor

As for the latter, the chip was tested as described above using the internal bi-dimensional compressor. Figs. 3a and 3b show two plots of the chip under test: an incoming dataset event and a reconstructed one respectively. The pictures show data samples of about 50k words deriving from 256 anodes (left-hand axis), each containing 200 timing samples (right-hand axis). Plots represent the same event before and after bi-dimensional compression. Each peak can be interpreted as the higher datum of a cluster. If adjacent anodes have corresponding peaks that satisfy the bi-dimensional algorithm, the cluster is confirmed; otherwise the peak is considered as a mere noise spike. Nevertheless the figures show that all peaks are properly reconstructed - both in position and in height - while background noise is present in the original event but significantly absent in the reconstructed one. This test was performed on several sets of data to ensure the bi-dimensional compressor did not reject any real clusters. The data were extracted in a physics experiment: this involved a 256×200×8-bit event corresponding to a silicon drift detector consisting of 256 anodes.

Temperature was not considered during the to date tests because the whole data acquisition chain will work under room conditions. Some temperature tests will be carried out in the near future on the whole chain to characterize chiefly the system from the mechanical point of view (cabling, connectors, bondings).

This test has been performed on several sets of data to be confident the bi-dimensional compressor does not reject any real cluster. The data have been extracted by a physics experiment; it has been used a 256×200×8-bit event that corresponds to a silicon drift detector made of 256 anodes each of which is time-scanned for 200 timing slots. In this case the lower and higher thresholds of the compressor were set to two given values.

If they were set to higher levels the Fig. 3b would show less clusters since the higher are the thresholds (even just one), the smaller is the number of clusters detected.

IV. CONCLUSION

The CARLOS chip was implemented using CERN library 0.25μm CMOS technology employing a radiation tolerant layout design. CARLOS is a prototype tailored to fit into ALICE SDD readout architecture. The final version of the chip was sent to the foundry in May 2004 and the 700 chips production has been tested.

The CARLOS chip will be inserted on an end-ladder card of the ALICE SDD experiment.

The work presents the tests that were performed to characterize the chip and exploit the final yield of 89% over 700 fabricated chips. The whole tests were performed in laboratory and the chip was also used in a test beam at CERN on November 2004.

References

[1] ALICE Collaboration, “The ALICE detector at LHC”, Nucl. Instr. Meth. A, 344, (1994), 27-38,

[2] F. Tosello, “The ALICE inner tracking system”, Nucl. Instr. Meth. A, 473, (2001), 210-218,

[3] ALICE Collaboration, “The inner tracking system of the Alice experiment”, Nucl. Instr. Meth. A, 530, (2004), 28-32,

[4] A. Rashevsky at al., “Characteristics of the ALICE Silicon Drift Detector”, Nucl. Instr. Meth. A, 461, (2001), 133-138,

[5] A. Calin et al., “Single event effects in static and dynamic registers in a 0.25μm CMOS technology”**,** IEEE Trans. Nucl. Sci., 46, (1999), 1434-1439,

[6] S. Antinori, et al., “A Rad-Hard 2D-Compressor ASIC for ALICE SDD Experiment”, Nucl. Instr. Meth. A, 524, (2004), 295-305,

[7] S. Antinori, et al., “Design, realization and test of a rad-hard 2D-compressor and packing chip for high energy physics experiments”, Nucl. Instr. Meth. A, 530, (2004), 92-97,

[8] A. Gabrielli et al., “Implementation of a bi-dimensional compressor for a high energy physics experiment”, IEEE Tran. Nucl. Sci., 51, (2004), 2491-2496,

[9] F. Faccio, et al. “SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 μm CMOS technology for applications in the LHC”, 5th Workshop on Electronics for LHC Exp., 11/20-24/1999, pp. 571-575, (http://nicewww.cern.ch/~lebwshop/LEB99_Book/Paperonly/faccio.pdf),

[10] G. Anelli, “Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technology for the LHC experiments”, PhD Thesis, (http://www.cern.ch/RD49/RD49Docs/anelli/g_Chapter4.pdf),

[11] A. Werbrouck et al., “Image compression for the silicon drift detectors in the ALICE experiment” Nucl. Instr. Meth. A, 471, (2001), 281-284

[12] A. Marchioro et al., “G-link and gigabit Ethernet compliant serializer for LHC data transmission”, Nuclear Science Symposium Conference Record, 2, (2000), 96-99, ISBN: 0-7803-6503-8,

Illustration Captions

Fig. 1: CARLOS layout

Fig. 2: Cluster across the matrix

Fig. 3a: Original 256 x 200 event before 2D compression

Fig. 3b: Reconstructed 256 x 200 event after 2D compression

Fig. 4: CARLOS Test Board

TABLE I - CARLOS TESTS (623 CHIPS)

Voltage (V)	Frequency (MHz)	I (mA)	σ (mA)
2.5	39	105.3	0.5
2.5	40	110.7	0.5
2.5	41	113.2	0.5
2.1	40	84.8	0.5
2.7	40	121.5	0.5

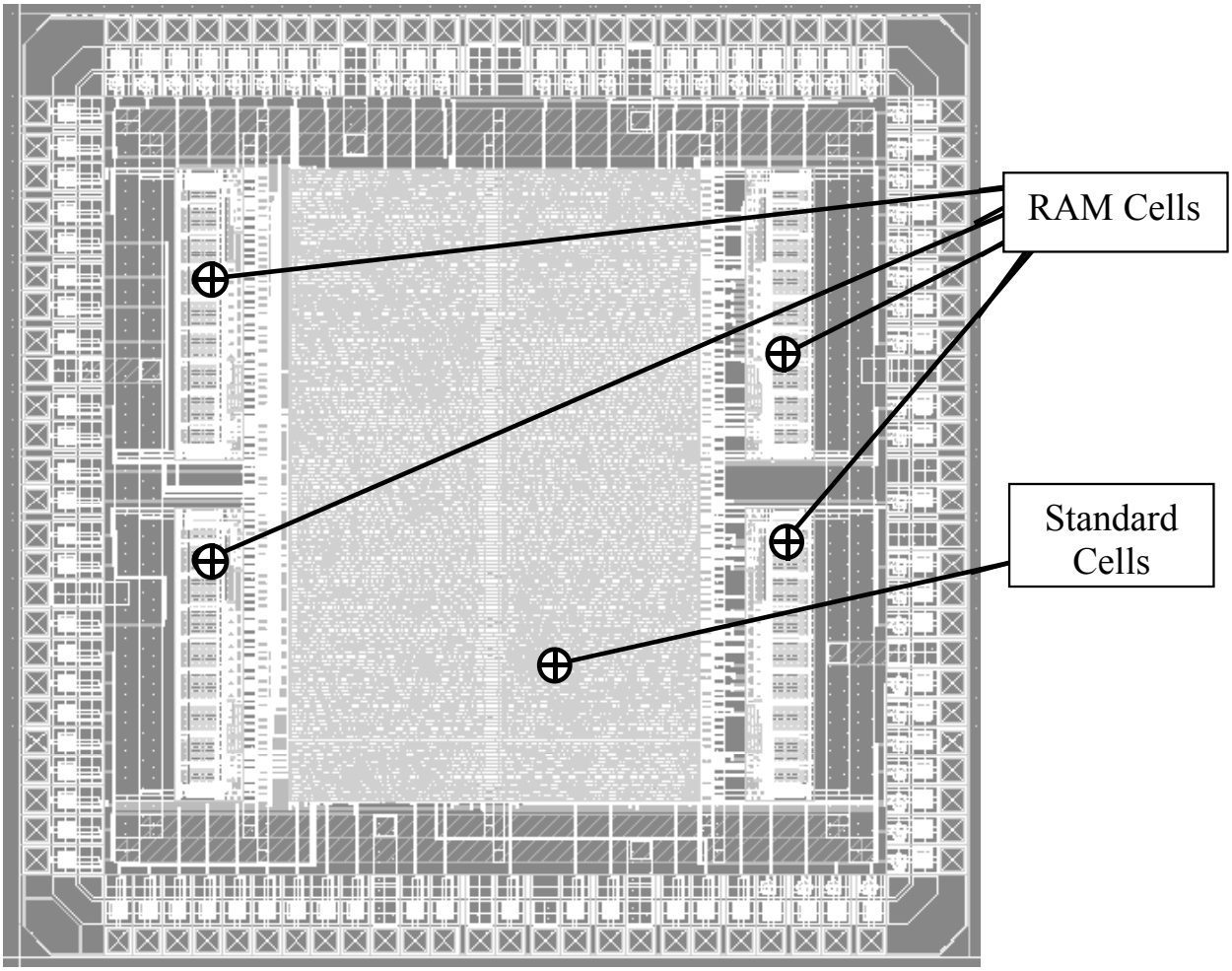

Fig. 1: CARLOS layout

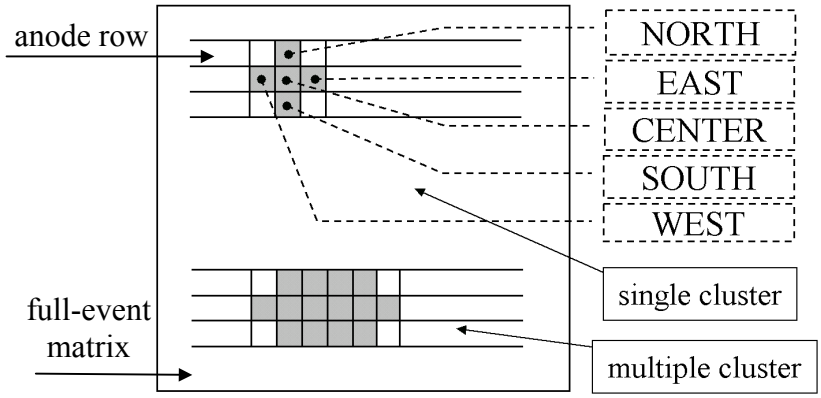

Fig. 2: Cluster across the matrix

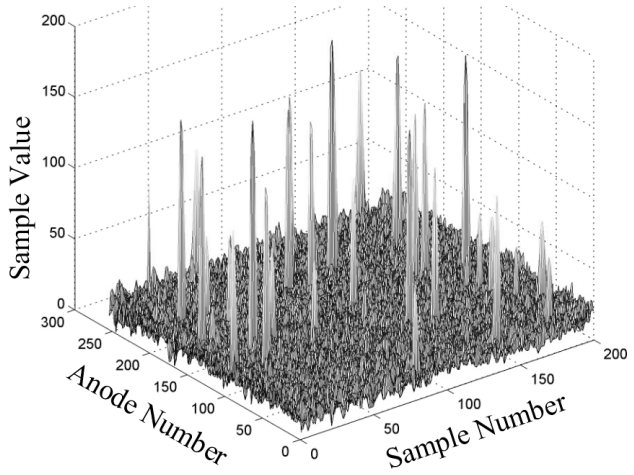

Fig. 3a: Original 256 x 200 event before 2D compression

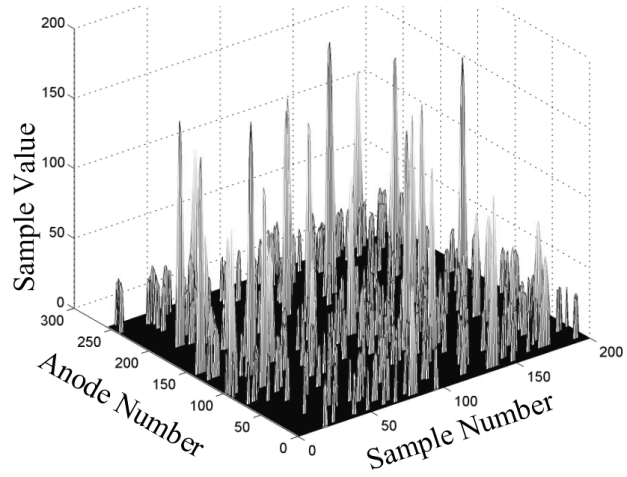

Fig. 3b: Reconstructed 256 x 200 event after 2D compression

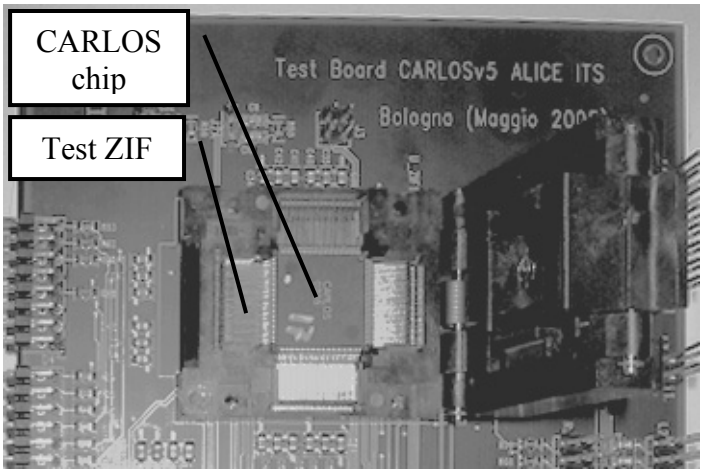

Fig. 4: CARLOS Test Board