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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

A multi-channel integrated circuit for the readout of a microstrip gas chamber

F. Krummenacher and C. Enz
Smart Silicon Systems S.A., Avenue de Chailly 23, CH-1012 Lausanne, Switzerland

R. Bellazzini
Dipartimento di Fisica and INFN-Pisa, Via Livornese 582/a, I-56010 Pisa, Italy

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The design and test of an 8 channel integrated circuit for the readout of the microstrip gas chamber and other multielectrode detectors are described. The circuit is composed of 8 identical channels, each providing the amplification and the shaping of the signal delivered by the detector. The peaking time of the shaper is 25 ns and the overall amplifier gain is 8 mV/1000 e^-. In addition to the analog output, each channel provides a TTL compatible digital output. The equivalent input noise is less than 700 e^- rms and the total dc power consumption is about 5 mW/channel. To avoid a baseline shift due to the tail of the current issued from the detector, an adjustable pole-zero cancellation circuit has been included.

1. Introduction

The microstrip gas chamber overcomes by two orders of magnitude the rate capability of standard wire counters. Since its introduction [1,2] it has been therefore considered one of the most promising detectors for the instrumentation of high intensity experiments (high-energy physics with fixed target, synchrotron radiation, etc.). This detector is being considered also for the tracking system of experiments at the next generation of high energy, high luminosity hadron colliders (LHC–SSC). This is due to the very good detector performance, now very close to those of solid state microstrip detectors, as well to the simplicity, low cost and radiation resistance that are intrinsic to a flushed detector with internal gas gain.

As for all the detectors with a large number of channels, the efficient organization of the front-end electronics in terms of dead-space and power dissipation, is one of the most challenging problems. Furthermore, any high intensity application needs fast signal shaping and strong reduction of the transmission bandwidth, because the particle production rate can be extremely high (10^{11} particles/s at LHC). Particularly important, from this point of view, is the position interpolation strategy (analog versus digital charge centroid).

To study all these points (density, power dissipation, interpolation) we have designed and tested a prototype multichannel integrated circuit having both analog and digital output. Obviously, until radiation hard processes become available, the problem of the radiation resistance of these devices, which is of primary importance for any LHC–SSC application, will remain an open one.

2. The detector electrical characteristics and summarized specifications

2.1. The detector structure

The microstrip gas chamber is a proportional detector made with microelectronics technology. By means of a lithographic technique, a closely spaced sequence of alternating thin conductive anode and cathode strips is placed on an insulating support; a drift electrode defines a region of collection of charges and the application of the appropriate potentials on anodes and cathodes creates a proportional gas multiplication (see fig. 1). One can understand the operation of the device as follows: drift lines connecting the upper (far) cathode to the anode concentrate on the thin anode strips, even more so due to the high potential difference between anode and close cathode strips; the high elec-

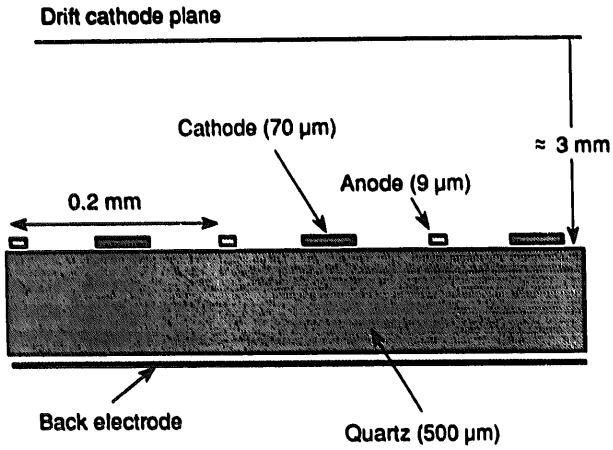

Fig. 1. A cross section of the detector.

tric field in the neighborhoods of the anode strip results in gas amplification (see fig. 2) A proportional gain of 10^4 has been achieved [2] in detectors with 200 μm anode pitch. The major part of the positive ions created during the avalanche process drift back to the close (≈ 50 μm) cathodes along the field lines, inducing signals on both anode and cathode strips. The duration of the ion current is of the order of 1 μs or less.

2.2. The detector equivalent circuit

As shown in fig. 3, the detector has been modeled by a time dependent current source I_{in} in parallel with a capacitance C_D.

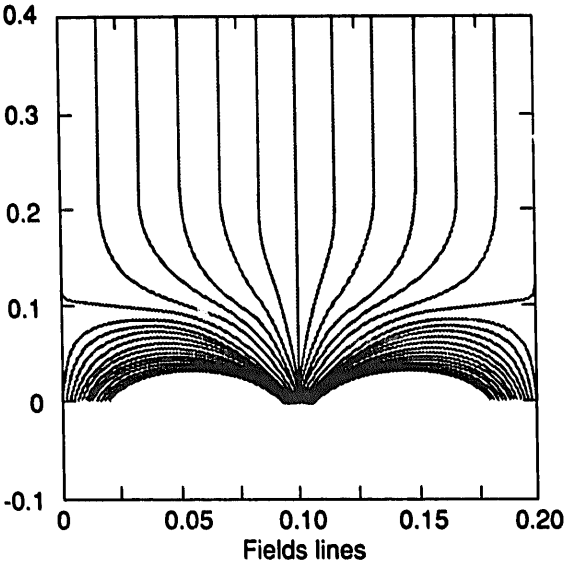

Fig. 2. The field-line map within one detector cell.

The charges are assumed to be delivered exponentially:

$$Q_{in}(t) = qQ_D\left\{1 - \exp\left(-\frac{t}{T_t}\right)\right\}, \quad (1)$$

where $q = 1.6 \times 10^{-19}$ C, Q_D is the total number of electrons delivered by the detector and T_t the transition time constant. The time dependent current $I_{in}(t)$ is thus given by:

$$I_{in}(t) = q\frac{Q_D}{T_t}\exp\left(-\frac{t}{T_t}\right). \quad (2)$$

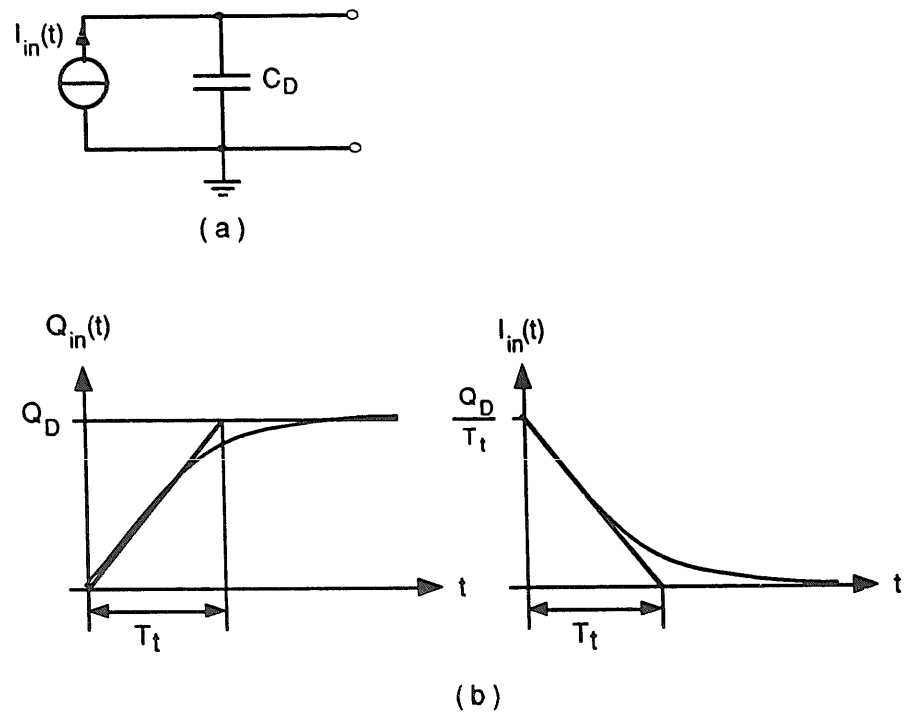

Fig. 3. (a): The detector equivalent circuit; and (b): The current source modeling.

The typical values used for the simulations are: $C_D = 5$ pF, $Q_D = 250000$ electrons, $T_f = 200$ ns.

2.3. Summarized specifications

For this application, the typical input signal to be detected is assumed to be roughly equal to 10% of the total charge Q_D, which corresponds typically to 25000 electrons delivered after about 20 ns. The peaking time at the analog output should be 30 ns. The gain should be larger than 4 mV/1000 electrons (25 mV/fC), corresponding to an output pulse with an amplitude larger than 100 mV. The equivalent input noise for 5 pF should be less than 1000 electrons rms.

Furthermore, due to the high voltages applied to the detector, the input protection should be able to tolerate a 1 kV spike assuming a total input capacitance of 10 pF (including the capacitances of the detector, the bonding and the preamplifier input).

3. Circuit description

3.1. General circuit principle

The circuit block diagram of one channel is presented in fig. 4. Each signal strip (anode and/or cathode) will be connected to the input pad (INPUT) of each channel. The first block represents a charge preamplifier combined with a filter (or shaper) to perform a nearly Gaussian output voltage. The peaking time can be adjusted around its nominal value by injecting (subtracting) a current to (from) the peaking time pad (PT). The same procedure can be applied to the tail cancellation pad (TC) to adjust the tail cancellation time constant around its nominal value.

To bring the signal to the desired output level, a second amplifier stage has been added which is followed by the comparator and the analog buffer. The comparator performs the differential-to-single-ended conversion and insures the compatibility with the TTL-AS gates. The threshold can be adjusted externally. Note that changing the threshold potential also changes the output dc voltage. This effect has been modelled by the analog adder appearing in fig. 4. The different blocks presented in fig. 4 are detailed in the next paragraphs.

3.2. The preamplifier combined with the shaper

The circuit principle of the combined preamplifier/shaper is given in fig. 5. It uses essentially four differential transconductance stages g_{m1} to g_{m4} and two capacitors C_f and C_1. The first differential transconductance stage operates as a current follower with a low-pass characteristic having a time constant given by:

$$T_{in} = \frac{C_{in} + C_D}{g_{m1}}. \tag{3}$$

It also provides a low input impedance in order to compensate for the detector small leakage current.

The second part of the circuit simulates the transadmittance of a RLC network. As a matter of fact, for $g_{m4} R_{tc} \gg 1$ the circuit is equivalent to the one presented in fig. 6, with a transimpedance given by:

$$Z_m(s) = \frac{V_{out1}}{I_1} = -\frac{1}{g_{m3}} \frac{s2dT_p}{(sT_p)^2 + s2dT_p + 1} \tag{4}$$

where T_p is the peaking time and $d = 1/2Q$ the damping factor, respectively given by:

$$T_p^2 = \frac{C_f}{g_{m3}} \frac{C_1}{g_{m4}}, \tag{5}$$

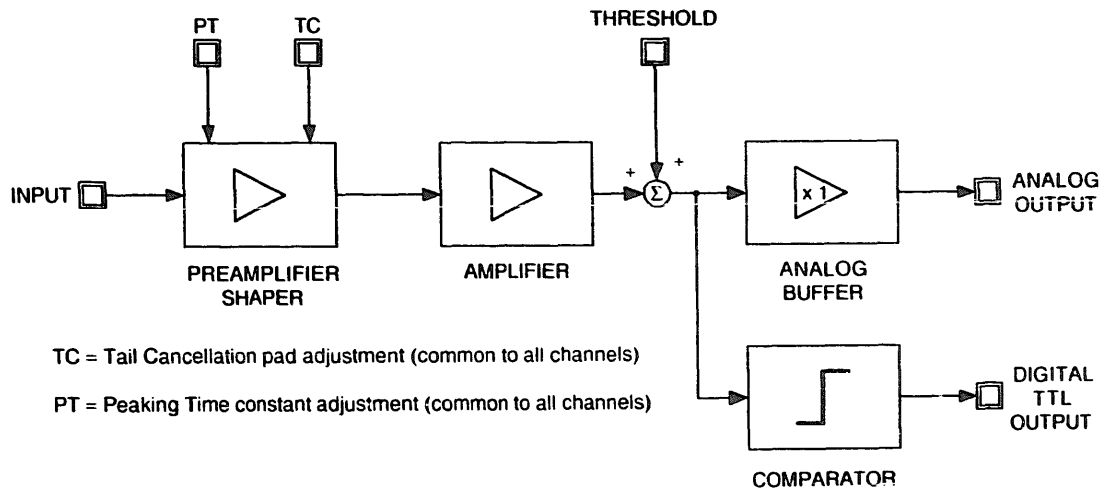

Fig. 4. The circuit block diagram.

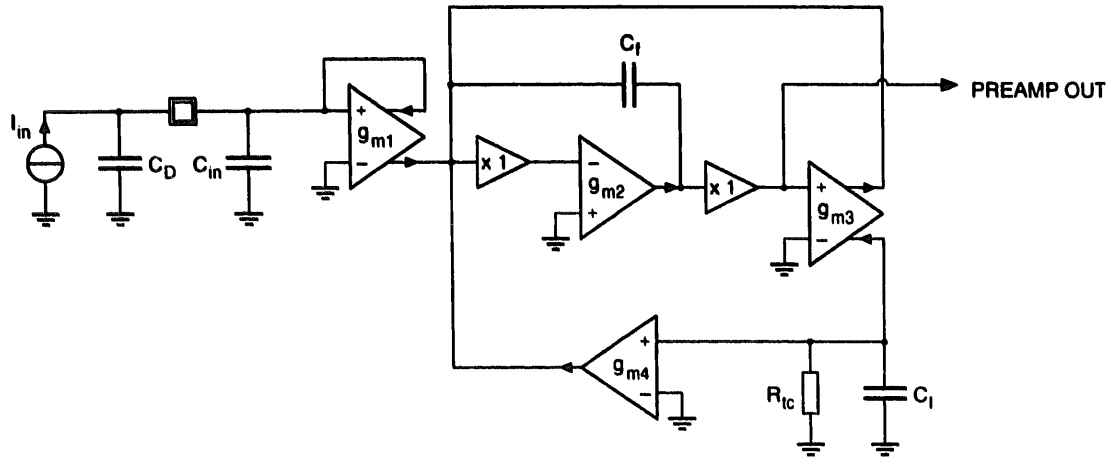

Fig. 5. The circuit principle of the combined preamplifier/shaper.

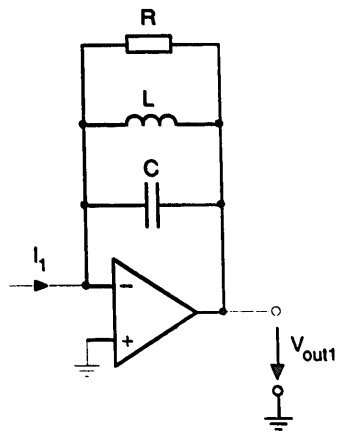

Fig. 6. The equivalent circuit of the preamplifier/shaper.

$$2dT_p = \frac{C_l}{g_{m4}}. \tag{6}$$

To compensate for the tail of the input current I_{in}, a pole/zero cancellation is realized by introducing the resistance R_{tc} in parallel with capacitor C_l. The time constant $R_{tc}C_l$ should thus be matched with the tail decaying time constant T_t defined in fig. 3.

The small buffers connected to the negative input of transconductor g_{m2} and g_{m3} have been added to reduce the capacitive load on the corresponding nodes.

To insure stability, g_{m2} has been chosen much larger than g_{m3}, shifting the positive zero given by C_f/g_{m2} to higher frequency. Thus, assuming $g_{m2} \gg$

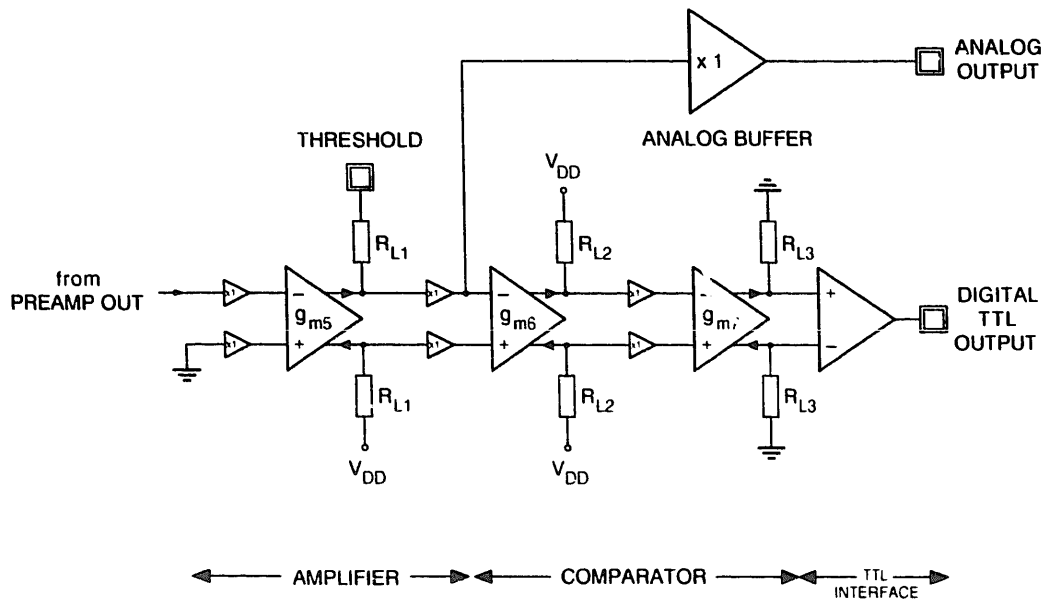

Fig. 7. The circuit principle of the amplifier, comparator and TTL interface.

g_{m3}, the transimpedance of the preamplifier circuit of fig. 3 is given by:

$$Z_m(s) = \frac{V_{out1}}{I_{in}} = -\frac{1}{g_{m3}} \frac{1}{1+sT_{in}} \frac{s2dT_p(1+sT_{tc})}{(sT_p)^2 + s2dT_p + 1} \tag{7}$$

where:

$$T_p^2 = \frac{T_{tc}T_3}{g_{m4}R_{tc}+1}, \tag{8}$$

$$2dT_p = \frac{T_{tc}+T_3}{g_{m4}R_{tc}+1}, \tag{9}$$

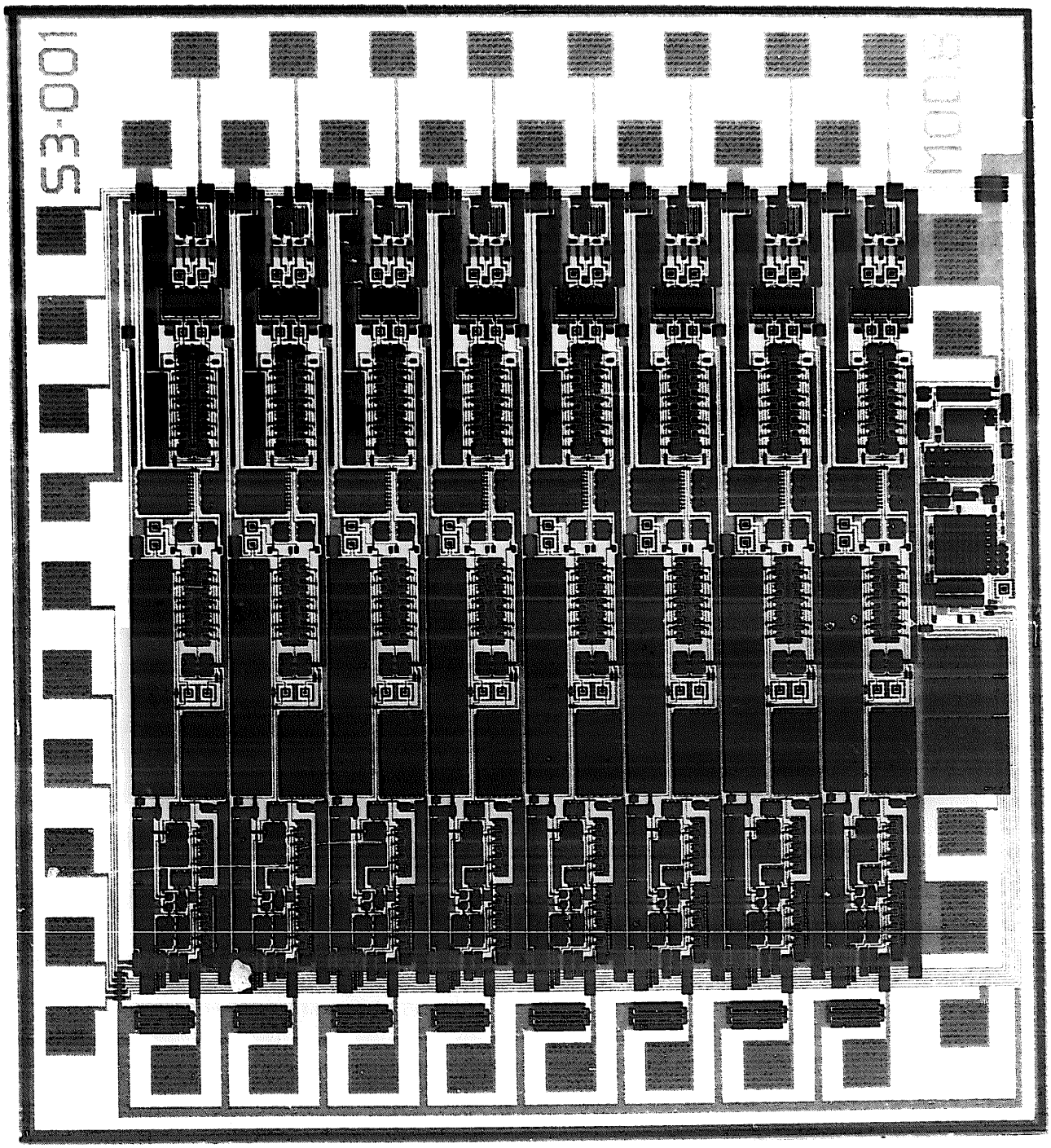

Fig. 8. The final circuit layout.

$$T_{tc} = R_{tc}C_1, \tag{10}$$

$$T_3 = \frac{C_f}{g_{m3}}, \tag{11}$$

After some simulations using the ESACAP program [3], the following values have been chosen: $T_p = 20$ ns, $d = 0.8$ ($Q \approx 0.6$), $T_{in} = T_p/3 = 6.7$ ns, $C_{in} = 1$ pF, $C_f = 40$ fF, $g_{m1} = (C_D + C_{in})/T_{in} = 900$ μA/V, $g_{m2} = 400$ μA/V, $g_{m3} = 2dC_f/T_p = 3.2$ μA/V, $g_{m4} = g_{m1}/12 = 75$ μA/V, $C_1 = 2dT_p g_{m4} = 2.4$ pF, $R_{tc} = T_t/C_1 = 83.3$ kΩ.

3.3. The amplifier, the comparator and the TTL interface

The circuit principle of the amplifier, the comparator and the TTL interface is given in fig. 7. The amplifier is a simple differential-input/differential-output transconductor stage, the differential dc gain of which is given by:

$$A_{5\text{-}DC} = g_{m5}R_{L1} \approx 8. \tag{12}$$

A buffer has been added to drive the analog output load.

The comparator is formed by two cascaded differential-input/differential-output transconductance stages. The differential dc gains have been chosen to be:

$$A_{6\text{-}DC} = g_{m6}R_{L2} \approx 10, \tag{13}$$

$$A_{7\text{-}DC} = g_{m7}R_{13} \approx 4. \tag{14}$$

The output of the comparator is followed by a TTL-compatible differential-to-single-ended stage.

4. The circuit layout

A plot of the circuit layout, including the input protection network, is shown in fig. 8. The size of the overall circuit, including pads, is 2.1 × 2.1 mm. The masks were made at CSEM-Neuchatel, Switzerland, within a multi-project wafer (MPW) while the circuit has been integrated on silicon by FASELEC A.G. -Zurich, Switzerland, using a 3 μm self-aligned-contact CMOS technology (SACMOS). The integration density of this technology corresponds to a 1.5 μm standard CMOS technology.

5. Simulation results

One channel of the circuit has been simulated using the ESACAP program. Figs. 9a and 9b respectively show the shape of the input charge and current signals that were assumed for the simulation of the circuit. The pulse in fig. 10 represents the output voltage of the preamplifier, while the analog output voltage is

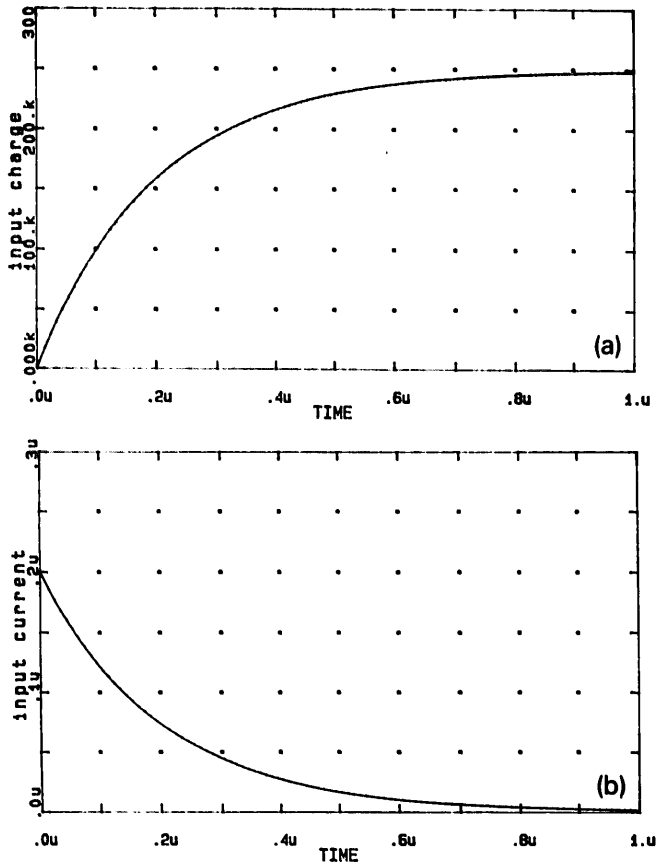

Fig. 9. (a) The shape of the input charge for simulation; (b): The shape of the corresponding current signal.

presented in fig. 11. The peaking time is found to be 30 ns and the width about 38 ns (FWHM). The peak amplitude is 225 mV. Assuming the signal corresponds to 10% of the total charge Q_D (i.e. 25 000 electrons), which are assumed to be delivered after about 20 ns, the gain of the amplifier can be estimated to be 9 mV/1000 electrons or 56 mV/fC.

The digital part has been simulated assuming a typical TTL input characteristic [3]. The TTL output

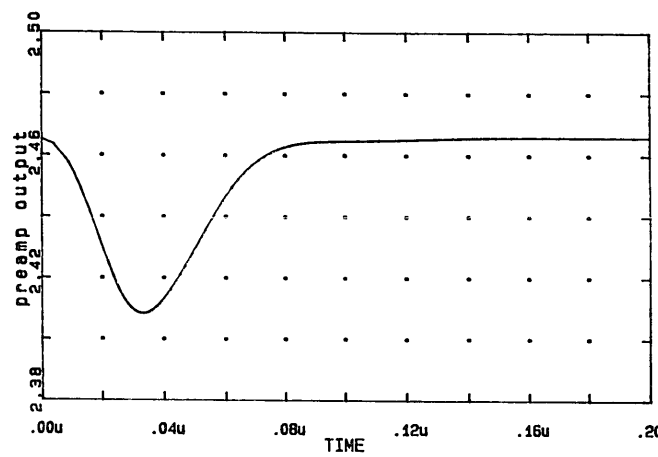

Fig. 10. The simulated output signal from the preamplifier.

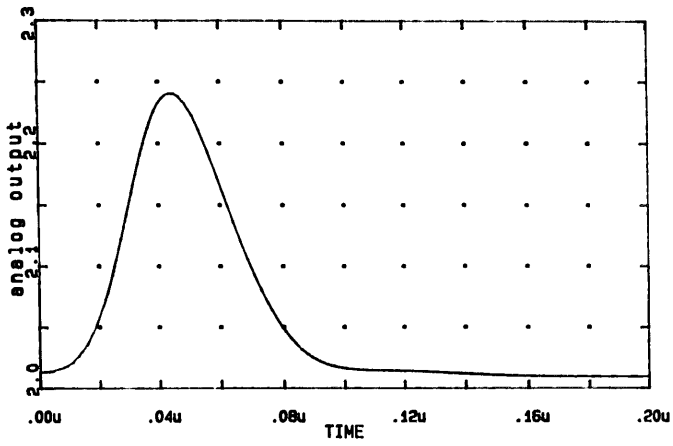

Fig. 11. The simulated analog output voltage.

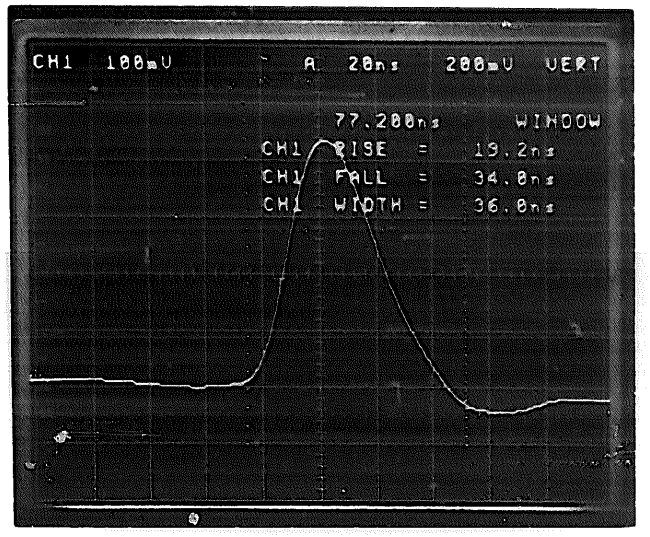

Fig. 13. The averaged delta current response of the analog chain.

voltage has been plotted in fig. 12. The delay is about 30 ns, while the fall time is around 7 ns.

6. Experimental results

Several chips were encapsulated in a dual-in-line ceramic package and extensively measured in the laboratory. Fig. 13 shows the averaged delta current response of the amplifier to an injected charge of 50000 electrons. The peaking time is 25 ns, the full width at half maximum (FWHM) is 36 ns and the peak amplitude is 440 mV. The measured overall gain of the analog chain is therefore 8.5 mV/1000 electrons or 50 mV/fC. The analog output is proportional to the input charge up to 10^5 electrons.

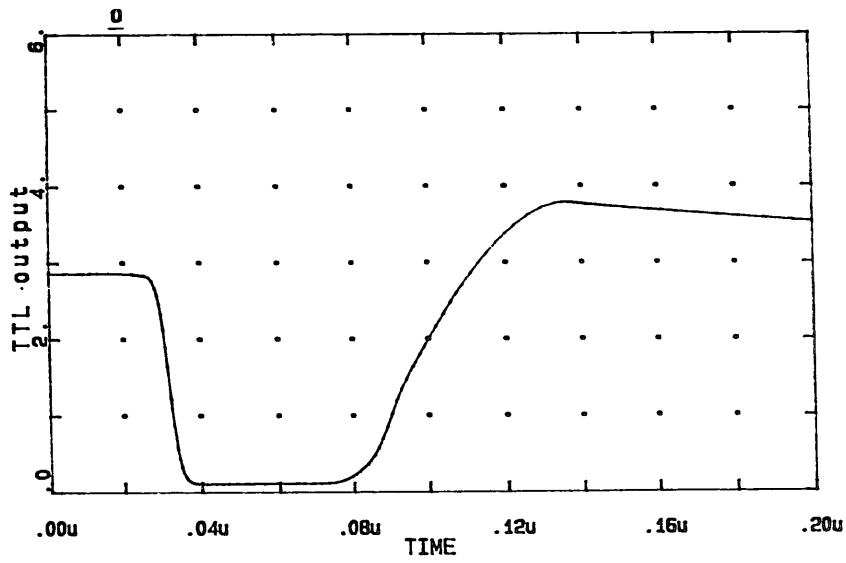

Fig. 12. The simulated TTL output voltage.

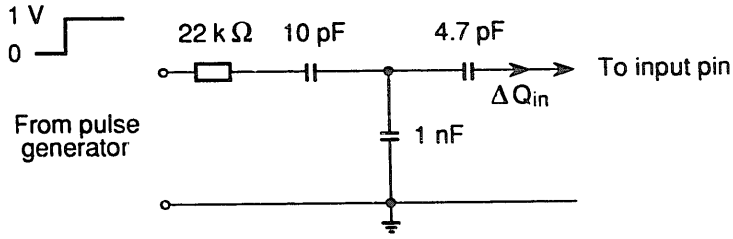

Fig. 14. The passive network used to model an exponentially decaying input current.

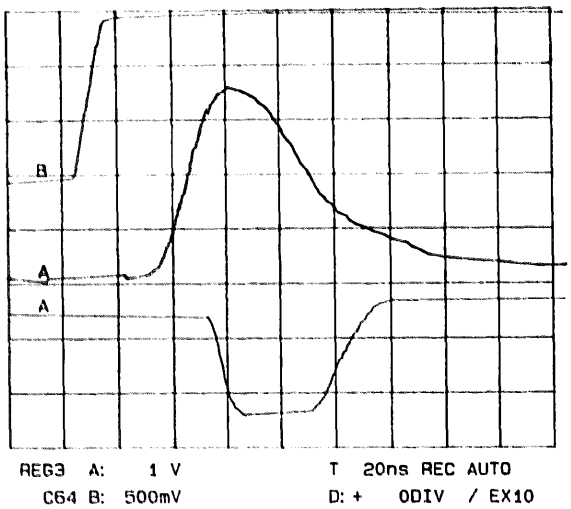

Fig. 15. The averaged analog (middle trace) and digital (lower trace) response to an exponentially decaying current. The top trace is the step function sent through the passive network of fig. 14.

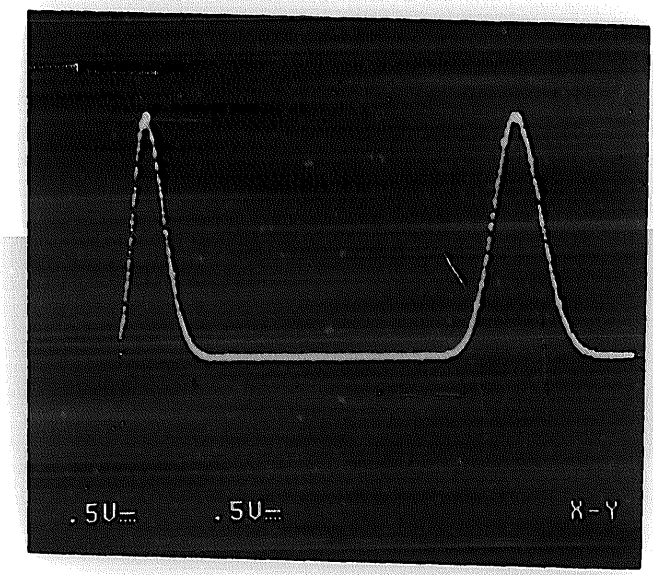

Fig. 16. The pulse-height spectrum of the noise (left peak) and of the analog response to 10000 electrons (right peak).

To model the tail of the detector ion current, the passive network of fig. 14 was connected to the channel input. The step response of this network is an exponentially decaying pulse with ≈ 200 ns time constant. Fig. 15 shows the averaged analog output (middle trace) and digital output (lower trace) obtained when the step of the upper trace was sent to the input through the passive network. The shapes of these signals are very close to those obtained with the simulation, indicating that the tail cancellation circuit works as expected and the good reliability of the simulation procedure. The lowest digital threshold which can be applied to have stable operation at the same time of the analog and digital section corresponds to 35000 electrons. Below this value the circuit starts to oscillate, probably because the gain of the TTL stage becomes too high. Disconnecting the digital part, this oscillation disappears.

The noise performance of the circuit is described by the pulse-height spectrum of fig. 16. The left peak is the pedestal distribution, while the right peak is the response to 10000 electrons. From this measurement an ENC of 615 electrons for 0 pF detector capacitance is obtained. Fig. 17 shows the dependence of the noise on the input capacitance. A sensitivity of 26 electrons/pF has been measured.

The typical performance characteristics of the integrated amplifier are summarized in table 1.

After the bench test, a printed circuit board containing 32 channels of the amplifier was prepared and mounted on a microstrip gas chamber. The analog output was connected to a fast line driver to reduce the capacitive load and to observe the signals on a remote digital oscilloscope. Fig. 18 shows the output signal (one shot) from an individual strip when the detector

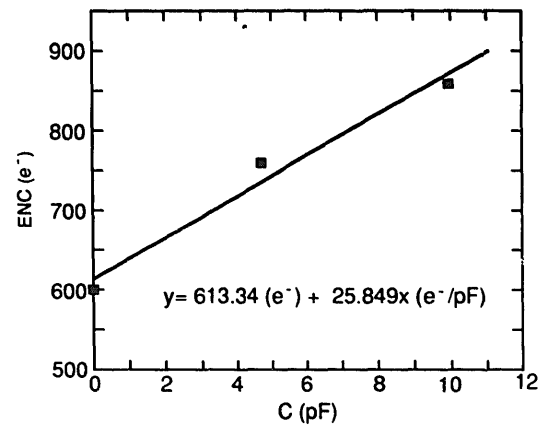

Fig. 17. The dependence of the noise on the input capacitance.

Table 1
Typical performance characteristics of the integrated amplifier

Test conditions	
VDD supply voltage	5 [V]
Detector capacitance	5 [pF]
Measured performance	
Time constants:	[ns]
rise time	19
peaking time	25
FWHM	36
Gain	8.5 [mV/1000 e⁻] (50 [mV/fC])
Equivalent noise charge:	
extrapolated at Cdet = 0	615 [e⁻ rms]
noise slope	26 [e⁻/pF]
Dynamic range	100000 [e⁻]

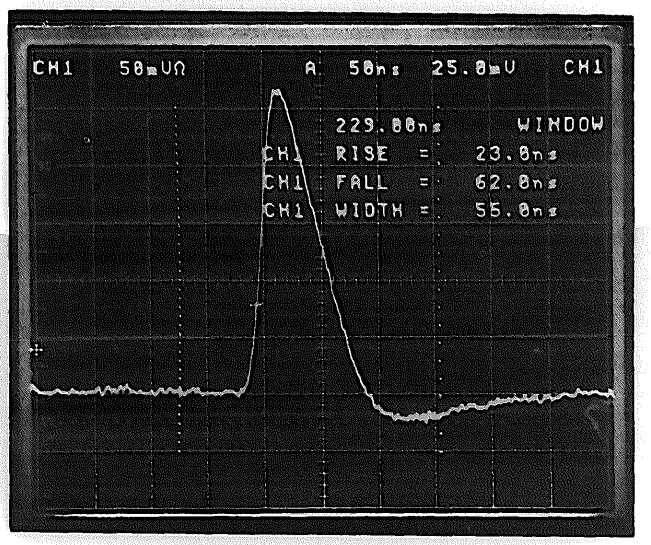

Fig. 18. The analog signal obtained from one strip of a microstrip gas chamber illuminated with ^{55}Fe X-rays.

was illuminated by the 6 keV X-rays of a ^{55}Fe radioactive source. The S/N ratio for a primary ionization release of 220 electrons is larger than 100.

7. Conclusions

A multichannel integrated circuit has been designed and successfully tested in the laboratory and on the detector. It combines fast shaping (25 ns peaking time) with good noise performance (700 electrons for 5 pF input capacity). The availability of both analog and digital output will allow to study experimentally the best position interpolation strategy. It seems well suited also for many other multi-electrode devices, like microstrip silicon detectors, especially if very fast shaping is needed. A second version of this chip is now under design, aiming mainly to lower the digital threshold down to 10000 electrons.

Acknowledgement

We thank C. Magazzu' of INFN-Pisa for the enthusiastic and skilled technical support.

References

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