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FAST FRONT-END ELECTRONICS FOR EXPERIMENTS USING SILICON CALORIMETERS AT SSC/LHC COLLIDERS

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A fast VLSI preamplifier using HF2CMOS technology was designed and built. The preamplifier meets the requirements for silicon calorimetry application in experiments at hadron colliders SSC/LHC. The overall power consumption is less than 45 mW for a maximum output voltage swing of 5 V (≈ 7 ns rise time). The slew rate is about 700 V/μs for an input capacitance of 150 pF. The measured value of ENC (equivalent noise charge), for an RC–CR shaping time of 20 ns and an input capacitance of 150 pF, is 17 ke_{RMS}.

1. Introduction

The interest of the high-energy physics community is turning nowadays to several ambitious projects, such as the hadron collider LHC (in the LEP tunnel at CERN) and the SSC in the USA, involving multi-TeV proton beams. Being the core element of the central detection system, the calorimeter must face the exceptional experimental conditions [1] created by very high luminosity, and high multiplicities and the large variety of physics phenomena to study. The following features are thus required of such calorimeters: compact construction, flexibility, fine segmentation, fast charge collection, easy calibration, good radiation hardness, good energy resolution, and ability to satisfy the compensation condition ($e/\pi = 1$).

The calorimeter which fulfils all those requirements is a sampling calorimeter with silicon as active medium [1–3]. The silicon detector thickness (about 400 μm) and its thin support allows sampling gaps of less than 2 mm. Furthermore, the silicon devices enable a flexible and very thin longitudinal and lateral segmentation, providing precise angle measurement and separation of very close jets and/or photons. The high granularity currently achievable is a necessary condition to resolve possible complex interaction configurations. Silicon detectors have fast response (for standard silicon detectors, the electron transit time is 2 ns or less, whereas the whole transit time is 6 ns or less) and request low operating voltage.

The problem of the silicon hardness to radiation damage is presently being investigated [2,4]. The experimental results have allowed a conceptual design of a radiation-resistant calorimeter for an SSC experiment [2]. In the proposed calorimeter, the dominant passive absorber is iron leading to a small number of generated neutrons and a minimal neutron damage condition. Furthermore, the addition of polyethylene (in front and rear of the silicon detectors) moderates these neutrons and further minimizes their impact on the detectors and the electronics, located on the silicon devices supports.

Electromagnetic calorimeters using silicon as active medium have been demonstrated to have a good energy resolution. Measurements performed by the SICAPO (silicon calorimeter and polarimeter) collaboration (Florence, Hamburg, McGill, Messina, Milan, Tel-Aviv, Trieste and Turin) with an electromagnetic calorimeter (24 radiation lengths deep), using silicon as active material and tungsten or uranium as passive material, have shown an energy response which is linear and stable up to better than 1%, and an energy resolution of $\sigma(E)/E = (17.6 \pm 0.3)\%\sqrt{\tau/E(\mathrm{GeV})}$, where τ is the thickness of each absorber layer in radiation length (i.e. the sampling frequency) [5].

Obtaining a good hadron energy resolution necessitates the achievement of the so-called compensation condition. The experimental data, presented by the SICAPO collaboration, have proven that the compensation condition can be reached by tuning the calorimeter response (i.e. the visible energy) to the energy deposited by the electromagnetic component of a hadronic shower [6]. By exploiting the so-called "local hardening effect" [7] or the "filtering effect" [8], it is possible to equalize the response to electrons and hadrons (with the same

incoming energy) for Si calorimeters with high-Z passive absorber (like U or W) or with a mixture of low-Z and high-Z passive absorbers (like Fe and Pb).

The high granularity required is obtained by using silicon detectors of about 2×2 cm^2 active area [1,2].

In this paper, we describe the performance of a VLSI preamplifier realized in HF2CMOS * technology, to be used in silicon calorimeters for experiments at SSC /LHC hadron colliders.

The VLSI readout front-end electronics has to be located as close as possible to the detector (namely on the detector support) in order to avoid cross-talk and minimize the stray capacitance.

2. Design analysis of the front-end electronics

In devices like the calorimeter under analysis, in which a very high number of channels is required, the design of the front-end electronics needs a special approach. In addition to the preamplifier noise, the main parameters are: the power dissipation and the space taken up by the electronics itself.

The input capacitance of the preamplifier plays an essential role in the total energy resolution, thus the parasitic capacitance due to the connecting cables must be minimized by putting the preamplifier as close as possible to the detector. Consequently, if the number of channels is very large, every preamplifier must occupy a small area. Moreover, the total power dissipation has to be kept low in order to avoid excessive heating of the calorimeter. Since the noise and the speed of the preamplifier improve with increasing power dissipation, a compromise between those three variables must be found in order to get an adequate solution.

* Developed by SGS-THOMSON Microelectronics.

Not in every interaction, in experiments at SSC/LHC machines, individual detectors would be traversed by particles. Nevertheless, the interaction event rate to be taken into account, is about 50 MHz. This consideration is crucial when technology is to be chosen. The shaping time for such a high rate must be very short. Consequently, the preamplifier series input noise is dominant with regard to parallel noise. Thus, it is advantageous to use a bipolar transistor, rather than a JFET at the preamplifier input, since the former has a higher g_m to I_C (bias current) ratio. For the required values of the detector capacitance C_D (100–200 pF) in SSC/LHC experiments [2], a high g_m to C_D ratio is needed to obtain a suitable bandwidth. Furthermore, a preamplifier employing bipolar transistors allows the use of high-speed monolithic technology, which needs a minimum occupied area.

Since the energy range deposited in silicon detectors varies from about 0.1 up to about 500 MeV, the dynamic range of preamplifier output must also be large, so that linearity and speed characteristics are being maintained at both small and large signals. The new process in mixed technology bipolar–CMOS, called HF2CMOS, is able to satisfy the required specifications as a result of the very small dimensions of the integrated transistors and the low parasitic capacitance inside the monolithic chips.

3. Technology

The current availability of mixed technology combining very-high-speed bipolar transistors with 2 μm CMOS, enables the design of a high-speed, very-high-slew-rate, monolithic charge-sensitive preamplifier. By using this technology, namely HF2CMOS, it is possible to implement on the same silicon chip both bipolar transistor (npn, lateral pnp, vertical pnp, isolated collec-

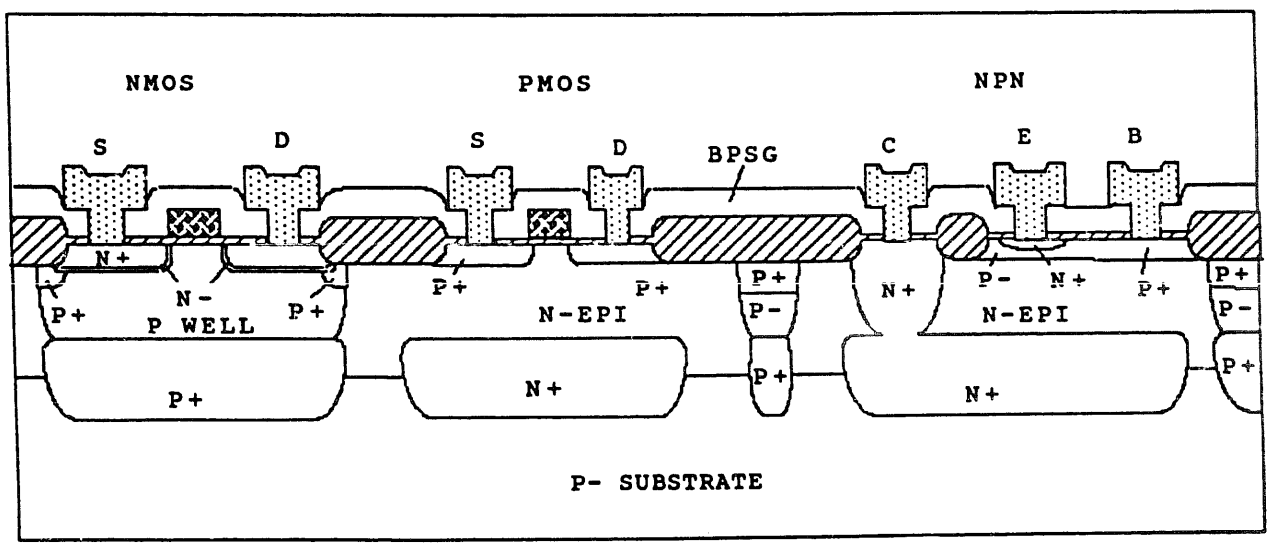

Fig. 1. Transistor cross section of the process HF2CMOS.

Table 1
Main features of the basic components of the charge-sensitive preamplifiers

	Bipolar (npn)		p-CHA.MOS	n-CHA.MOS
V_{CEO}	15 V	BV_{dss}	15 V	15 V
h_{FE}	100 typ	KL	20 μA/V²	60 μA/V²
f_T	≥ 4 GHz			

tor vertical pnp) and CMOS devices, well suited for both analog and digital applications.

The compactness due to the reduced space occupied by the basic structures and to a triple interconnecting level (two metal layers with planarized interlevel dielectric in addition to a polysilicon layer) permits the implementation of extremely complex systems, including high-precision analog circuits and a large number of logic functions (3000 MOS transistors/mm²).

The CMOS is a p-well on an n epitaxy process with silicon gate and a minimum channel length of 2 μm, as shown in fig. 1, where a p-channel and an n-channel transistor can be seen. The p-channel transistor is built directly on the epitaxial layer, while the n-channel device is realized on a p-well diffusion which is common to the top–bottom isolation step. In the same picture the classical npn bipolar transistor is also presented. In fig. 1, the deep n^+ collector diffusion, and the p base and n^+ emitter steps are shown.

The main features of the basic components used to realize the charge-sensitive preamplifier are presented in table 1. The values of f_T as a function of I_C for an npn transistor are shown in fig. 2.

In the design of the charge preamplifier a p-type element is necessary for the purpose of level shifting: in a classical bipolar technology either a lateral pnp or an isolated collector vertical pnp transistor could be used. They are shown in figs. 3 and 4, respectively. The p^+

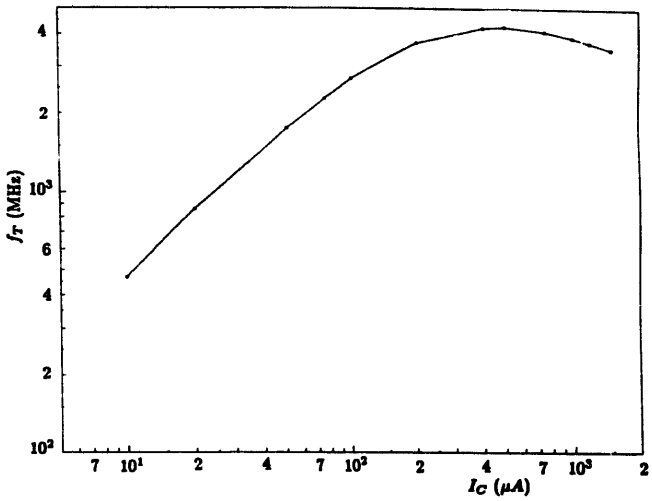

Fig. 2. $f_T - I_C$ plot of the HF2CMOS npn transistor with 356 μm² area.

emitter of the lateral pnp transistor is surrounded by p^+ collector diffusion, both of them are placed in an n epitaxial layer: the current flows laterally on the surface of the devices from the emitter to the collector. The gain and frequency performance are usually very poor and such a device cannot be used in high-speed applications.

Vertical pnp transistors cannot be used as level shifter, since its collector is directly connected to the substrate, the negative supply voltage.

The isolated collector vertical pnp is implemented as the complementary device of the npn one. The current flows vertically from the emitter to the collector and the collector is isolated from the substrate, from a deep n^+ ring. In order to avoid breakdown phenomena, such a ring has to be tied to the p^+ collector, thus creating large parasitic capacitance between the collector and the substrate. This prevents employing such devices in high-slew-rate applications.

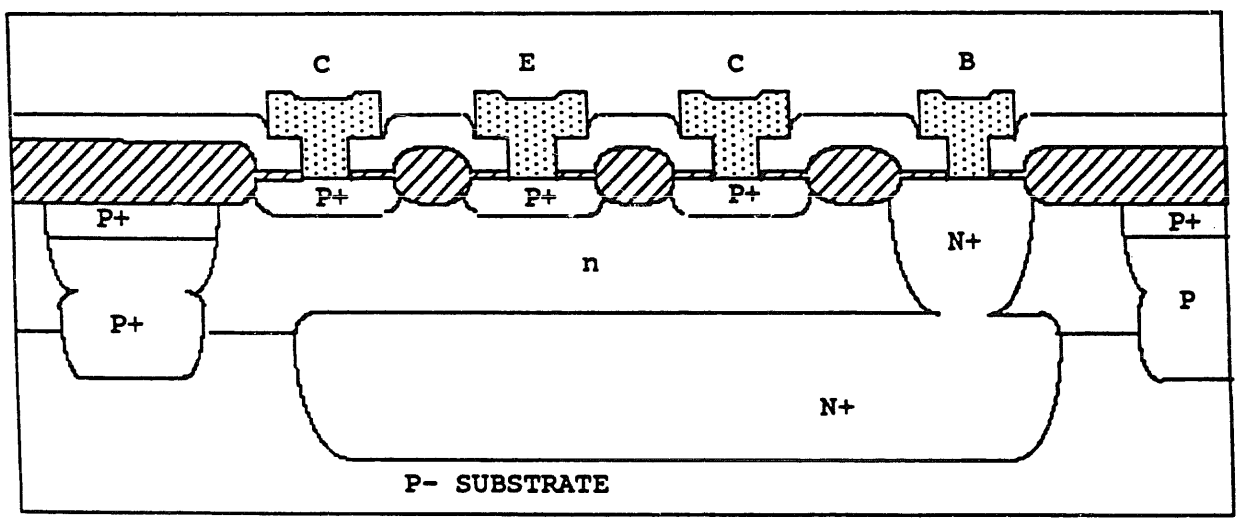

Fig. 3. Cross section of a lateral pnp transistor of the process HF2CMOS.

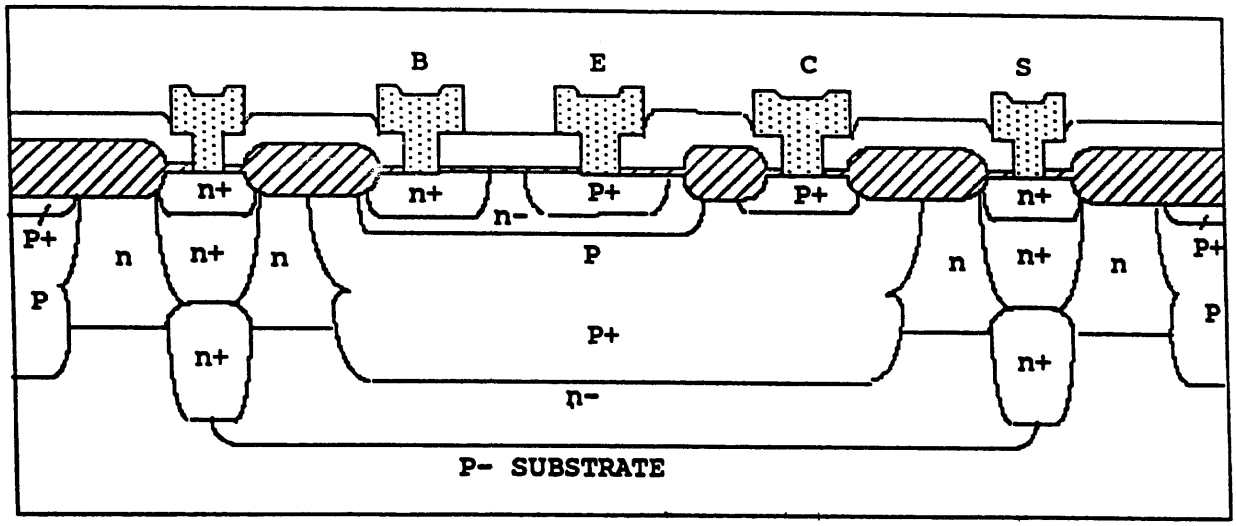

Fig. 4. Cross section of an isolated collector vertical pnp transistor of the process HF2CMOS.

To avoid speed problems, a p-channel MOS transistor was chosen to be used as level shifter. The purpose of using the selected 5 μm channel length is to increase the voltage performance of the devices and to avoid short-channel effects.

To design a radiation-hard device for the new generation of hadronic colliders, bipolar npn and pnp, and p-channel and n-channel MOS transistors have been irradiated with a neutron dose. The neutrons, in those experiments, are generated during the hadronic shower development by the nuclear breakup. In the region of shower maximum the expected fluences/cm^2, in one year of machine operation, vary from about 10^{11} n/cm^2 in the hadronic calorimeter section surrounding the interaction point up to about 10^{13} n/cm^2 in the section below 5° from the beam direction. Neutrons are expected to be one of the main sources of radiation damage for the electronics.

The dose of the first irradiation of the bipolar and MOS transistors under investigation was 0.4×10^{12} n/cm^2. The neutron source is ^{252}Cf with an average energy of about 1 MeV.

The characteristics of such devices (available as kit parts), performed before and after the irradiation, have not shown any deterioration of the performance of npn and MOS transistors.

The performances of pnp transistors, which were not supposed to be used for this application, degraded considerably after that irradiation.

Further investigation to neutron-fluences/cm^2 up to about 10^{13} n/cm^2 will be carried out in order to establish the limitation of this kind of technology.

4. Dynamic performances

In fig. 5, the circuit diagram of the charge-sensitive preamplifier using a bipolar input device is shown. For small signals and low power consumption, high speed can be achieved if the transistors obtain large values of their transition angular frequency ω_T at low standing current, a characteristic that depends on the technology employed.

The frequency ω_T is given by

$$\omega_T = g_m/C_B, \tag{1}$$

where $g_m = I_C/V_T$, ($V_T = kT/q$, where k is the Boltzmann constant), I_C being the biasing current and C_B the transistor input capacitance. Thus ω_T is dependent on the transistor dimension through the capacitance C_B. The above-mentioned condition is satisfied by the HF2CMOS process (fig. 2).

To obtain the same speed for large signals, another variable has to be taken into account. When the signal, generated by the Si detector, is such that the preampli-

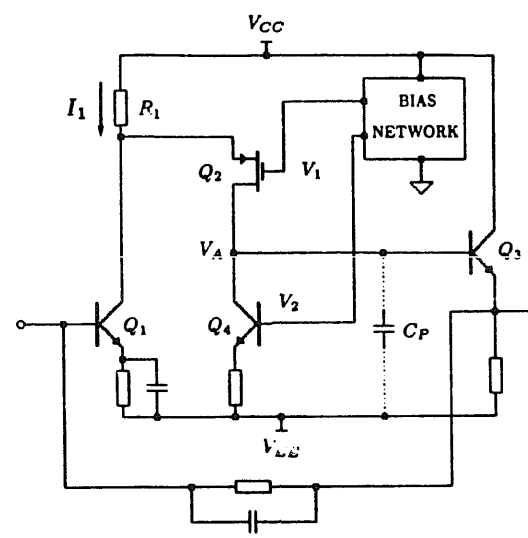

Fig. 5. Charge-sensitive preamplifier using a bipolar input npn transistor and MOS transistor as level shifter element.

fier output voltage has a large positive swing, due to the buffer action of Q_3 at node A, the same voltage swing appears across C_P. The maximum rate of change of the potential V_A will take place when Q_1 is cut off, causing all the current I_1 to be carried by Q_2 on C_P, that is the preamplifier compensation capacitor, linearly charging it:

$$V_A = \frac{I_1 - I_2}{C_P} t, \tag{2}$$

where I_2 is the biasing current of Q_2 and Q_4. The total transition time is

$$t_M = \frac{C_P}{I_1 - I_2} V_{AM}; \tag{3}$$

where V_{AM} is the final output voltage change, and the quantity

$$\frac{I_1 - I_2}{C_P} \tag{4}$$

is the slew rate, measured in V/μs [9].

Then, the current consumption is tied to the C_P capacitance value, if there are constraints on the t_M length.

If the integrated process employs very-high-speed transistors, like in our case, C_P needs a negligible value and is mainly given by the parasitic capacitances, both at the current generator Q_4 and Q_2 outputs. The aim of the circuit design was its minimization. In the adopted solution in fig. 5, the current generator Q_4 has a low parasitic collector capacitance; while Q_2 is a MOS transistor, which, besides having a low drain capacitance, has not shown radiation damage like the pnp bipolar counterpart.

A test pattern, namely a first integrated circuit version of the circuit in fig. 5, has been realized (the monolithic layout is shown in fig. 6).

With 3 mA standing current for Q_1 the measured slew rate is larger than 750 V/μs, while, when the preamplifier input capacitance is 150 pF (simulating the actual Si-detector impedance for a SSC/LHC experiment), the slew rate becomes 700 V/μs (≈ 7 ns rise time for 5 V output voltage swing); thus the high speed required by the high rate of the incoming events is well satisfied.

Transistor Q_1 (fig. 5) works at a standing current of 3 mA, while transistors Q_2, Q_3, Q_4, and the bias networks V_1 and V_2 consume less than 400 μA. The minimum supply voltage of the whole preamplifier is the sum of the potential across resistor R_1, that is about 3 V, of the 2 V minimum V_{DS} MOS voltage working point, and of the output voltage over V_{EE} negative supply that, as will be seen later, must be 3 V. Thus,

$(V_{CC} + |V_{EE}|)_{MIN} = 8$ V.

If we call V_{OM} the maximum expected positive output voltage swing, the total power dissipation of the preamplifier becomes ($I_{TOT} = 3.4$ mA)

$$P = I_{TOT} \times 8 \text{ V} + I_{TOT} V_{OM}$$
$$= 27.2 \text{ mW} + I_{TOT} V_{OM}. \tag{5}$$

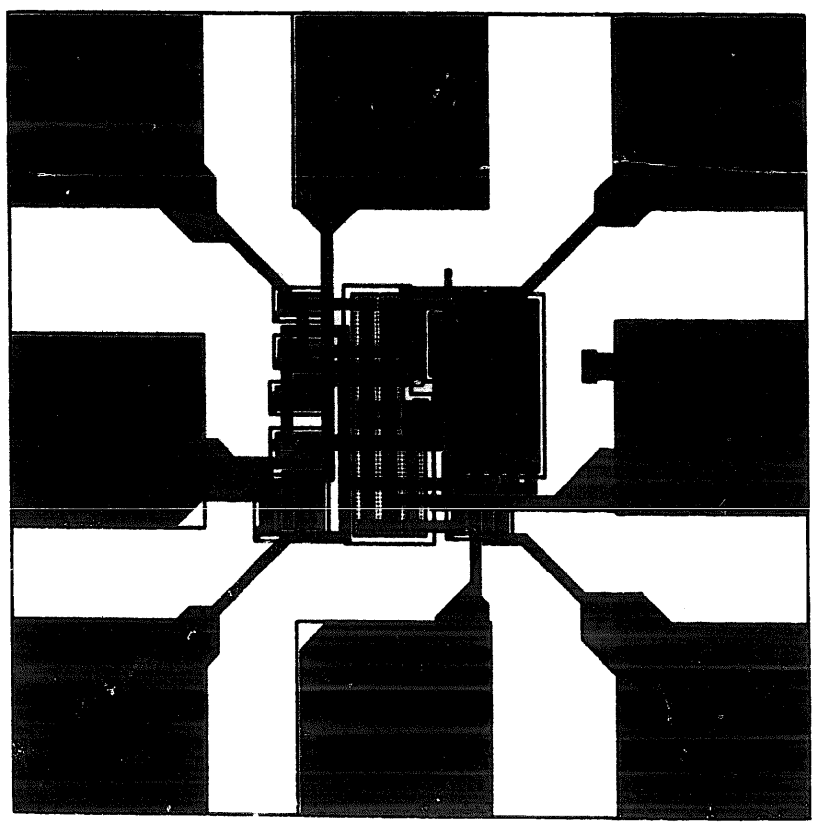

Fig. 6. Photograph of the monolithic layout of the charge-sensitive preamplifier shown in fig. 5.

If V_{OM} is about 5 V we get

$P = 44.2$ mW,

which is low enough for our purpose.

5. Preamplifier noise performance

5.1. Noise sources of the preamplifier

Fig. 7 shows the noise sources playing the main role in the noise analysis [10,11]:

$\overline{i_f^2} = \frac{4kT}{R_f}$ thermal feedback resistance noise,

$\overline{e_{BB'}^2} = 4kTR_{BB'}$ Q_1 base spreading resistance thermal noise,

$\overline{e_T^2} = \frac{4kT \times 0.5}{g_m}$ collector shot noise referred to the input,

$\overline{i_B^2} = 2qI_B$ input current shot noise,

$\overline{e_M^2} = \frac{A_f}{(g_m R_1)^2}\frac{1}{f}$ $1/f$ MOS noise referred to the input.

For Q_1 with a low $R_{BB'}$ of about 5 Ω, where $R_1 = 1$ kΩ and $I_C = 3$ mA, the corner frequency (i.e. the frequency where $1/f$ noise equals the white noise) becomes

$$f_c = \frac{A_f}{(R_1 g_m)^2}\frac{1}{(\overline{e_T^2} + \overline{e_{BB'}^2})} \approx 4.9 \text{ kHz},$$

where the measured A_f coefficient is about 10^{-11} V^2 for the employed MOS. Therefore, since $1/f$ noise is independent of the shaping time τ_M, if we have [12]:

$\tau_M \ll 1/(2\pi f_c) \approx 30$ μs,

it is possible to neglect the $1/f$ MOS noise contribution. Since the experiment requires $\tau_M \approx 20$ ns we can get for the equivalent noise charge (ENC) [13]:

$$\text{ENC(e)} = \frac{1}{q}\left\{\frac{\alpha_1}{\tau_M}\left[(C_D + C_f + C_B)^2\overline{e_T^2} + (C_D + C_f)^2\overline{e_{BB'}^2}\right] + \alpha_2\tau_M\left(\overline{i_B^2} + \overline{i_f^2}\right)\right\}^{1/2}, \quad (6)$$

where α_1 and α_2 are constants depending upon the shaper employed.

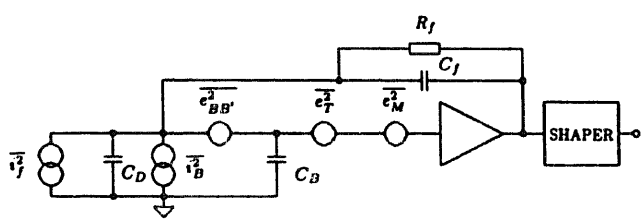

Fig. 7. The main noise sources of the signal acquisition chain.

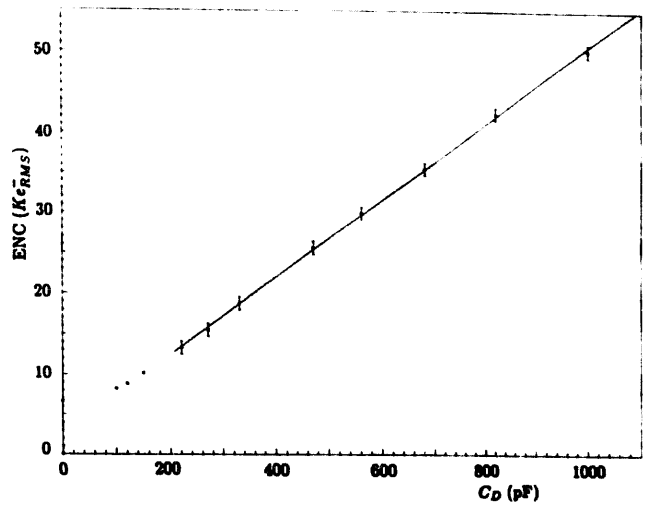

Fig. 8. Measured ENC(e) as a function of the input capacitance with an RC–CR shaper with 100 ns peaking time.

In eq. (6) the series noise contribution is inversely proportional to the shaping time τ_M and the parallel noise is proportional to τ_M. With the value of τ_M in the range of our requirements, the high parallel noise of a bipolar transitor becomes less important, so the advantage in the use of this kind of device with respect to the JFET lies in the lower input series thermal noise $\overline{e_T^2}$ due to the higher g_m/I_{BIAS} ratio [14]:

$$\frac{g_{m\,npn}}{I_{BIAS}} = \frac{q}{kT} = \frac{1}{26 \text{ mV}} \approx 40 \text{ V}^{-1} \quad \text{in bipolar,}$$
$$\frac{g_{m\,FET}}{I_{BIAS}} = \frac{3}{V_P} \approx \frac{3}{1 \text{ V}} = 3 \text{ V}^{-1} \quad \text{in JFET.} \quad (7)$$

This permits a lower power dissipation of the input devices to obtain the matching to the large detector capacitive impedance C_D with npn bipolar than with JFET [15].

Nevertheless, in bipolar transistors the base spreading resistance $R_{BB'}$ is a further source of series noise that cannot be neglected. In fact, the next improvements in the design of the test pattern (realized in order to check the dynamic performance of the process) will be devoted to minimize $R_{BB'}$ of the preamplifier npn input transistor, which now has a 110 μm^2 area, namely a three times larger area than the minimum possible to realize with this technology (A_{min}). The value of the base spreading resistance was measured in an indirect way, by means of noise measurements performed with the preamplifier.

In eq. (6) one expects a linear ENC dependence on C_D (at high values):

$$\text{ENC(e)} \approx \frac{1}{q}\sqrt{\frac{\alpha_1}{\tau_M}}\sqrt{(\overline{e_T^2} + \overline{e_{BB'}^2})}\,(C_C + C_f), \quad C_D \gg 0, \quad (8)$$

where C_B was neglected, being less than 1 pF.

Fig. 8 shows the experimental results. An RC–CR shaping time $\tau_M = 100$ ns was used ($\alpha_1 = \alpha_2 = \exp(2)/8$). Hence, for eq. (8) and the angular coefficient of the linear part of the curve, $R_{BB'} \approx 370\ \Omega$. The result is in good agreement with the ST-SPICE program simulation, predicting a weak dependence of $R_{BB'}$ on the bias current. For $C_D = 150$ pF, $\tau_M = 20$ ns (equivalent to the expected electronics operating conditions), $C_f = 10$ pF and $R_f = 100\ k\Omega$, the measured ENC is about 17 ke_{RMS}. This result is in agreement with the predicted value of the series noise generated by the above $R_{BB'}$.

5.2. Design improvements and shaper

The preamplifier series noise can be improved, if the value of $R_{BB'}$ is reduced. This can be done by increasing the transistor area. In discrete devices, the value of $R_{BB'}$ decreases when more transistors are connected in parallel [16], which is equivalent to a larger-area transistor in integrated devices.

The preamplifier input transistor is three times larger than the A_{min}. Thus, the estimated $R_{BB'}$ of an A_{min} is about 1100 Ω. It is possible to decrease $R_{BB'}$ by using an input transistor N times larger than the A_{min}, with $N \gg 1$. The value of N is limited by the power dissipation (less than 45 mW). Every A_{min} will work with a standing current I_C/N. If I_C has to be kept constant, the largest number N is such that (at the standing current per A_{min}) the transistor f_T is still adequate for the speed requirements. In fig. 2, it can be seen that at 20 μA, $f_T \approx 850$ MHz, suitable for our purpose. Thus we get

$$N_{max} \approx \frac{I_C}{20\ \mu A} = \frac{3\ mA}{20\ \mu A} = 150.$$

For $I_c = 20$ μA for each A_{min} we can evaluate C_B. In bipolar transistors the C_B value is linearly dependent on the collector current up to the maximum in the f_T–I_C plot [17]. From fig. 2 ($f_T - I_C$), eq. (1) and ST-SPICE simulation we can get from the low I_C region

$C_{B\,min} \approx 128$ fF at 20 μA,

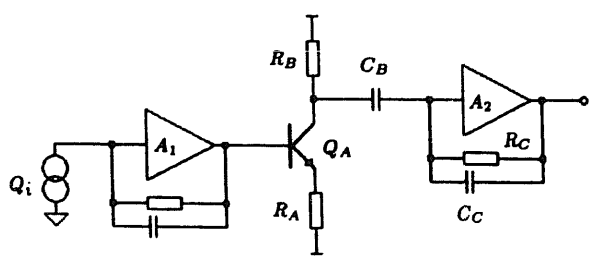

Fig. 9. The monolithic acquisition chain. The second stage A_2 is able to drive a coaxial cable terminated at its ending points. Shaping of the signal with an RC–CR filter is also realized. The diagram to be integrated on a single chip.

where $C_{B\,min}$ represents the A_{min} input capacitance. With these assumptions, eq. (6) becomes

$$ENC(e) = \frac{1}{q}\left\{\frac{\alpha_1}{\tau_M}\left[(C_D + C_f + NC_{BMA})^2 \frac{4kTV_T}{2NI_{C\,min}} + (C_D + C_f)^2 \frac{4kTR_{BB'\,min}}{N}\right] + \alpha_2\tau_M\left(\frac{2qI_{C\,min}N}{h_{Fe}} + \frac{4kT}{R_f}\right)\right\}^{1/2}. \quad (9)$$

By differentiating eq. (9) with respect to N, the optimum value, N_{opt}, is

$$N_{opt} = \left[\frac{\frac{\alpha_1}{\tau_M}(C_D + C_f)^2\left(\overline{e^2_{T\,min}} + \overline{e^2_{B\,min}}\right)}{\alpha_2\tau_M\overline{i^2_{B\,min}} + \frac{\alpha_1}{\tau_M}\overline{e^2_{T\,min}}C^2_{B\,min}}\right]^{1/2}. \quad (10)$$

For $C_D \approx 150$ pF, $C_f = 10$ pF, $\tau_M = 20$ ns and $\alpha_1 = \alpha_2$ (RC–CR shaping), $N_{opt} \approx 170$. Thus the value of N_{opt} is only about 12% larger than that of N_{max} and the expected ENC for N_{max} is about 4.1 ke_{RMS}. For a triangular shaper with the same peaking time we expect about 3.6 ke_{RMS}, which is approximably 13% better than an RC–CR shaper. Nevertheless, the latter one is easier to implement on the integrated chip of the preamplifier.

Since more than one preamplifier can be realized on the same integrated chip, the biasing network is common to all the preamplifiers, giving a saving in area occupied and in current consumption.

The acquisition system is expected to be located remote from the preamplifier. Hence, the preamplifier output signal must be carried on a line, terminated at its ending points. A second stage, acting as a buffer, able to drive the line, has to be implemented on the same preamplifier chip. A very useful solution consists in having the signal shaping done by the second stage (fig. 9).

If Q_i is the charge delivered from the detector, the network output signal of fig. 9 becomes in the frequency domain ($S = j\omega$):

$$V_0(S) = -\frac{R_C}{R_A}\frac{SC_BR_B}{(1 + SC_BR_B)(1 + SC_CR_C)}\frac{Q_i}{SC_f}. \quad (11)$$

The inverting action of the transistor Q_A is such that the signal polarity of preamplifiers A_1 and A_2 is equal, hence the A_2 work conditions are equal to that of the A_1 preamplifier so its schematic circuit is similar to the one seen before. Dynamic considerations at the Q_A collector and emitter signals require $R_A \gg R_B$. By setting $R_A = 10R_B$ and $\tau_M = C_BR_B = C_CR_C$, we get

$$V_0(S) = -\frac{R_C}{R_A}\frac{S\tau_M}{(1 + S\tau_M)^2}\frac{Q_i}{SC_f}. \quad (12)$$

An RC–CR shaper and preamplifier are thus realized on the same integrated chip.

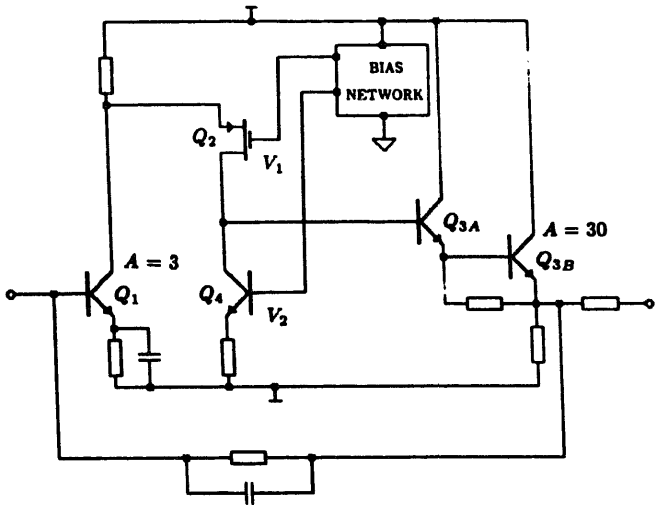

Fig. 10. Schematic diagram of the driver amplifier. The output stage is a Darlington configuration able to drive a 50 Ω coaxial cable terminated at its ending points.

By defining τ_M and R_A, C_B and R_B are determined. Hence, a degree of freedom is left for the values of C_C and R_C. At the peaking time τ_M, we expect that the maximum value of V_0, from eq. (12), is

$$V_0(\tau_M) = \frac{R_C}{R_A} \exp(-1) \frac{Q_i}{C_f}. \quad (13)$$

For $R_C = \exp(1) R_A$, we get

$$C_B = \frac{10\tau_M}{R_A}, \quad R_B = \frac{R_A}{10},$$

$$C_C = \frac{\tau_M}{\exp(1) R_A}, \quad R_C = \exp(1) R_A.$$

With $R_A = 20$ kΩ (if $V_A - V_{EE} \approx 3$ V the Q_A standing current is about 150 μA), one obtains $C_B = 10$ pF and $C_C = 0.37$ pF if $\tau_M = 20$ ns. These low capacitance values can have a monolithic implementation. The condition $C_B R_B = C_C R_C$ reaches a 1% accuracy, while the τ_M value attains 40% uncertainty (the peaking time is at τ_M, but the maximum value of V_0 is independent of the τ_M value, see eq. (13)).

The network in fig. 9 can be implemented on a single monolithic chip. The components R_f, C_f have to be external to the integrated chip in order to get an accurate overall gain.

The buffer amplifier A_2 is shown in fig. 10. The transistor Q_1 does not need a large area since the second stage noise does not degrade the resolution. The output stage is a Darlington configuration, able to drive 50 Ω coaxial cable terminated at its ending point.

The preamplifiers response to the detector signal is

$$V_0(S) = \exp(1) \frac{S\tau_M}{(1 + S\tau_M)^2} \frac{1}{SC_f} Q_i,$$

$$V_{0\,MAX}(t = \tau_M) = \frac{1}{C_f} Q_i.$$

As already mentioned, the amplifier can drive a 50 Ω coaxial cable to carry the signal far from the calorimeter, in the acquisition room.

6. Conclusions

A fast VLSI preamplifier using HF2CMOS technology has been realized. The preamplifier meets the requirements for silicon calorimetry application for experiments at the hadron collider SSC/LHC.

Overall power consumption is less than 45 mW for a 5 V maximum output voltage swing.

The slew rate is about 700 V/μs for an input capacitance of 150 pF (≈ 7 ns rise time for a 5 V output swing).

The measured value of ENC for an RC–CR shaping time of 20 ns and an input capacitance of 150 pF is 17 ke_{RMS}. A next version of the preamplifier will have an input transistor about 50 times larger than the present one. In this way, the expected ENC value will be reduced to about 4 ke_{RMS}, with similar power consumption.

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