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# The Readout and Biasing System for the MARE Experiment in Milan

**C. Arnaboldi · A. Giachero · C. Gotti · M. Maino · G. Pessina**

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**Abstract** The complete readout and biasing system for the MARE experiment in Milan is presented. The experiment aims at a direct measurement of the neutrino mass, and is based on an array of microcalorimeters coupled to semiconductor thermistors. The readout is based on JFETs operated inside the cryostat at cold (130 K), to buffer the voltage signal from the thermistors. The sources of the JFETs are fed into second stage amplifiers with very low noise (less than 0.5 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ white noise) and programmable high gain. The outputs are then processed by Bessel filters and acquired with a commercial DAQ system. Every 20 channels, an additional group of 4 is used to amplify the ground reference from inside the cryostat; this common ground signal is then subtracted from each channel. This approach allows to recover a fully differential readout with a smaller number of cables with respect to the standard differential configuration. The detector bias is programmable in voltage and sign with 8-bit resolution. A test signal can be superimposed on the bias voltage, in order to test each channel individually. All the readout system is remotely programmable from a PC, coupled through optical fibers.

**Keywords** Low noise · Front-end · Read out · Electronic system · Low temperature · Bolometers

C. Arnaboldi · A. Giachero · C. Gotti (✉) · M. Maino · G. Pessina
INFN Sez. Milano-Bicocca and Università di Milano-Bicocca, Piazza della Scienza 3, 20126, Milano, Italy
e-mail: claudio.gotti@mib.infn.it

C. Gotti
Università di Firenze, Via S. Marta 3, 50139, Firenze, Italy

## 1 Introduction

Electronics System is the definition that must be adopted when speaking about the readout of an array of detectors. In that case the system becomes complex and does not consist only of the very front-end preamplifiers. This is particularly the case with arrays of bolometers where every detector has its own individual characteristics that the electronics must match in order to exploit fully the dynamic of the DAQ. In addition, for this class of detectors, the biasing needs to be optimized and must satisfy stringent requirements concerning noise and stability.

Examples of complex bolometer readout systems in the field of neutrino physics are those of the CUORICINO [1] and CRESST [2] experiments. Another example is the system we designed and developed to readout the bolometric detectors of MARE-1, 72 $AgReO_4$ (Silver Perrhenate) small crystals (about 0.5 g) [3] glued on 2 arrays of 36 Si thermistors [4]. In the following sections both the strategy adopted for MARE-1 and its implementation will be described in detail.

## 2 System Set-up

The signal bandwidth of our detectors extends from DC to a few tens of kHz. EMI interference and the influences from the main supply are sources of disturbances that need to be taken into account. One way to do this is to adopt the differential biasing and readout [1] that allows a natural rejection of these disturbances, processed as common mode signals. The drawback of a differential configuration is that its noise power is larger by a factor of 2 with respect to the single sided input, since twice the number of input transistors are needed. $\mu$-bolometers have low noise, and we tried to optimize the limitation of a pure differential configuration with a solution that we call an adaptable-differential configuration. In the classical scheme the differential circuit is completely symmetric within its structure. In our set-up we customized the input stage to match the characteristics of the sources of its input signals.

A block scheme of the whole readout chain for one channel is shown in Fig. 1. The resistance of the bolometers $R_B$ is in the MΩ range, depending on their temperature of operation. For each bolometer, the detector signal is readout from a cold

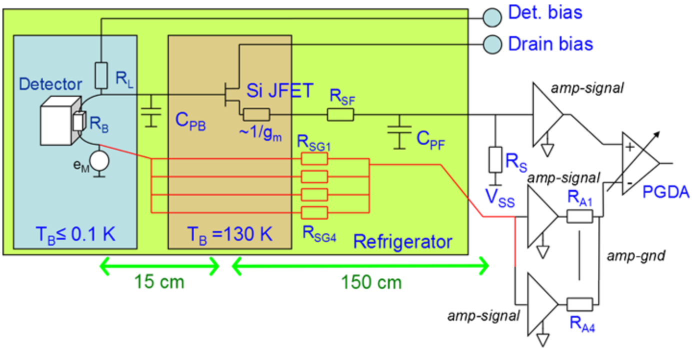


**Fig. 1** (Color online) Very front-end scheme for the readout of the bolometers of MARE-1

buffer stage composed of a SNJ450 Si-JFET from Interfet in unity gain follower configuration, the Si-JFET being held at its optimum temperature of operation, around 130 K. The parasitic capacitance $C_{PB}$ at the JFET input is of the order of 15 pF. The signal at the source of the Si-JFET is read at room temperature by the very low noise single sided input preamplifier [5, 6], amp-signal. The connecting cables from the cold to the warm stage contribute with about 200 pF of parasitic capacitance $C_{PF}$. The input stage of amp-signal matches, at moderate frequency, the impedance seen at its input, $1/g_m + R_{SF}$, between 200 and 300 Ω, where $g_m$ is the transconductance of the Si-JFET and $R_{SF}$ is the parasitic resistance of the connecting wires. The suppression of the common mode disturbances, $e_M$, is done with the help of amp-gnd that reads $e_M$ only, but with the same gain of amp-signal. This time the impedance of the link is implemented with more wires in parallel and results in a few tens of Ω, $R_{SG1} \| \cdots \| R_{SG4}$. The matching of such impedance can be done with an input stage having a very wide area. In our set-up we put 4 amp-signal in parallel to form amp-gnd and take their average output with resistors $R_{A1}$ to $R_{A4}$. As known, series input noise is inversely proportional to the area of the input transistor: in our system we have now optimized such parameter. The resulting noise power is 1.25 that of a single sided amplifier, a degradation of only 25%. The values of the above source impedances are quite small and the parallel noise of our selected transistors present at the inputs of amp-signal and amp-gnd, proportional to the transistor area, has no influence at all. A Programmable Gain Differential Amplifier, PGDA, subtracts the signals of amp-gnd from amp-signal, rejecting the spurious disturbances from $e_M$ at the output of the chain.

The detectors are small and very close together. The GND node is found therefore at the same potential for all channels and only a few amp-gnd can be used, each one serving as the reference for many detectors. We chose to share one amp-gnd every 20 readout channels, as the result of our layout organization. This is shown in Fig. 2. In this way we obtain the second benefit of saving the number of connecting wires, very remarkable with low temperature detectors. Figure 3 shows a photograph of the main-board where 4 preamplifiers can be found. It is laid-out on a 4 layers 230 × 250 mm$^2$ PCB standard for 19″-rack (6 units in height). There is no distinction between main-boards with amp-signals or amp-gnd: only one type of PCB was designed. The only difference is that in the amp-gnd boards the PGDA is not used,

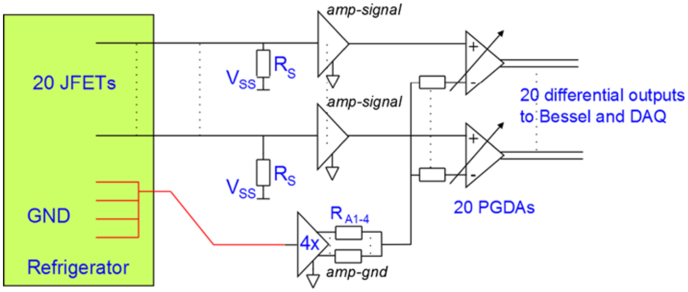


**Fig. 2** (Color online). Channel organization in the front-end main boards. Each group of 20 detectors and 4 grounds is managed by 6 main boards

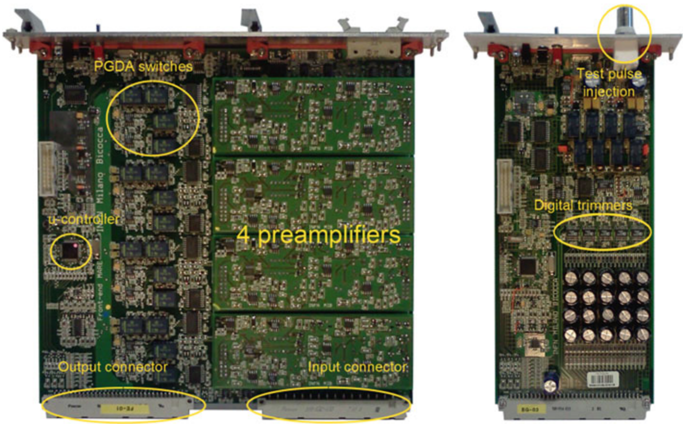


**Fig. 3** (Color online) Photographs of the main board (*left*) and of the bias generator (*right*) of MARE-1

so it was not populated. The identification of the function implemented is done on the back-panels of the racks, where the input/output connectors are sorted on purpose. On the back-panel the pattern repeats every 6 main-boards slots. After 5 slots where the amplification of 20 detectors is done, the sixth has the outputs of its 4 preamplifiers averaged with 4 resistors on the back-panel (connected as in Fig. 1) and buffered to drive the 20 channels, as in Fig. 2. On this sixth slot the input of each preamplifier is the detector GND. On every main-board the amp-gnd is routed from the input connector to a digital trimmer and then subtracted from the amp-signal at the PGDA differential amplifier. The digital trimmer allows to add a small attenuation on the amp-gnd path to compensate for the gain of the cold stage that is slightly smaller than one. The main-board is remotely programmable. The voltage gain of the amplification chain is settable with 4 bits of resolution. Parasitic capacitances from the switches that select the feedback resistors of the PGDA are minimized thanks to the use of relays. The AC coupling frequency is settable in 2 steps: normal mode and DC mode with small gain, to allow the DC characterization of the bolometers. The gain can span between a few V/V up to 30 kV/V. A 24-bits sigma delta ADC on the main-board is used to measure the critical nodes of the first and second stage of amplification and the supply voltages.

Communication between the main-board and the remote system is via optical fibers with a I2C serial bus. A $\mu$-controller of the ARM series, LPC2134 from NXP, manages the board. A rack accommodates 2 sets of 6 slots for a total of 40 channels. Part of the room in every rack is occupied by 2 low noise and low drift linear voltage supplies [7], one on top of the other. The analog outputs from the main-boards are differential signals that are sent to the antialising filters located in a cage close to the DAQ system. The filters are 6 poles active Thomson or Bessel filters with four switchable frequency bandwidths [8], settable remotely.

Finally we have to mention the bolometer biasing system. It consists of a set of cards, each able to manage 20 bolometers. The input voltage to this card can be derived from the supply of the rest of the system or from batteries, in order to suppress ground loops. Digital trimmers are present with which it is possible to tune the opti-

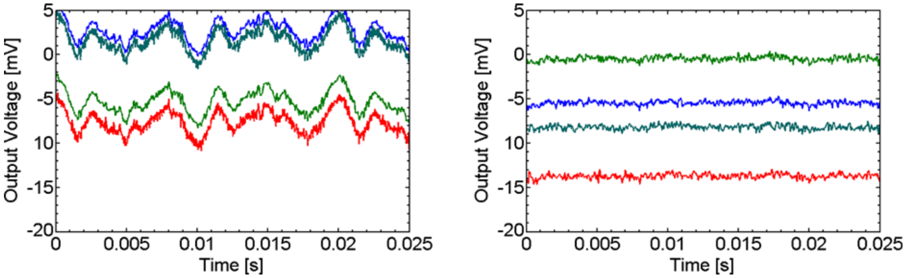


**Fig. 4** (Color online) Baselines of a few detectors (shifted to guide the eyes) when the buffer suppression is not active on the *left panel*: fluctuations are due to EMI. The effect of the buffer suppression is evident in the *right panel*, where the same baselines have now the fluctuations almost completely suppressed

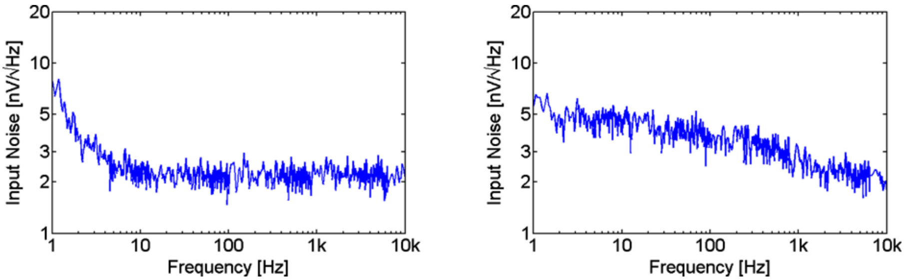


**Fig. 5** (Color online) Series noise of one front-end channel (detector with negligible Ohmic value) at a temperature larger than 120 K, *left panel*, and between 100 K and 120 K, *right panel*

mal biasing for each individual channel. A calibration pulse, enabled with relays, can be injected in series with the bias and applied across the thermistor. Again a LPC2134 ARM $\mu$-controller manages the board and the communication with the remote system. Figure 3 shows the photograph of the bias generator card, 4 layers with an area of $100 \times 230\ \text{mm}^2$.

## 3 Measurements Results

As examples of performance we show the power of the EMI suppression of our adaptable-differential set-up and the series noise. Figure 4 shows the baselines of a few detectors channels for the two cases where the adaptable-differential configuration is not active, left panel, compared with the case where it is fully active, right panel. As it can be seen there is a noticeable improvement, with a rejection capability that can be estimated to be better than 40 dB.

Noise performance at low frequency of Si-JFETs at cryogenic temperature is strongly dependent on temperature [9, 10]. Our set-up is not an exception to this and Fig. 5 illustrates two cases. In the left panel the temperature of operation of the cold stage is about 130 K, close to the optimum temperature. At lower temperature, the worsening in the performance is mainly observable in the low frequency region of the spectrum. White noise is less sensitive to temperature, unless it is below 90 K, where freeze-out from donor dopants starts to take effect. Between 100 K and 120 K a Lorentzian is visible in the right panel of Fig. 5 that spans to large frequency. The noise we have at 130 K is adequate for our set-up and we will run in this condition in MARE-1.

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