IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.DOI

Output Capacitance Minimization for Converters in DC Microgrids via Multi-objective Tuning of Droop-based Controllers

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This research is partially funded by: the Spanish Ministry of Industry, Economy and Competitiveness with grant number DPI2017-88505-C2-2-R; the Spanish Ministry of Science, Innovation and Universities with grant number RTI2018-098865-B-C33 and as part of the scholarship "Formación de Profesorado Universitario"; and Project "Innopower" by Fondazione Cariverona, Italy.

ABSTRACT This paper proposes a controller tuning methodology for voltage-current droop-based DC-DC converters in DC microgrids to reduce the output capacitance. This minimization is cost saving and implies lower fault currents. However, it leads to higher DC voltage variability during load transients, which requires an output impedance shaping by control means to reduce over or undershoot. The proposed control structure and problem definition simultaneously takes into account that the solution must achieve the impedance shaping, performance and stand-alone stability objectives. This comprises a multi-objective problem which is effectively formulated here and, then, solved by a non-smooth $\mathcal{H}_\infty$ optimization technique that tunes all free parameters. For comparison purposes, this tuning methodology is applied to several droop proposals, and the proposed droop is able to reduce the output capacitance of bidirectional buck-type and boost-type half-bridge converters by 37.5% and 23.08%, respectively, with respect to previous proposals. The designs are validated in time and frequency domains by means of theoretical analysis and experimental results on DC microgrid prototypes with bidirectional buck-type or boost-type half-bridge converters.

INDEX TERMS DC-DC power conversion, DC microgrids, Multi-objective tuning, H-infinity control, Impedance shaping.

I. INTRODUCTION

THE development of power electronic converters for Distributed Energy Resources (DERs) has led to the evolution of microgrids, which are the association of DERs with local customers loads. Most microgrids have adopted AC distribution as consequence of conventional power systems. However, DC microgrids have some advantages when facing DC output sources, such as photovoltaic or energy storage elements [1]. The connection of energy storage elements or interlinking between DC buses [2] is accomplished by DC-DC bidirectional topologies, such as the half-bridge converter (or bidirectional buck-boost converter) [3], which is the simplest topology to fulfill the requirements. In order to ensure stable and well-performing control of microgrids, these converters usually regulate the DC bus voltage with droop strategies [4], [5].

Droop control is a decentralized control strategy that allows an automatic load distribution among parallel sources by varying the DC bus voltage within a predefined range. Both voltage-current (V-I) and current-voltage (I-V) droops strategies share the same steady-state behavior with loads, but their dynamic performances are different [6], [7]. The V-I droop method is preferable for parallel operation because the converter behaves like a voltage source following a

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reference, given by the secondary control, with an output impedance characterized by the controller capabilities and output capacitance. Then, the DC bus voltage is restored to its nominal value, and power sharing is guaranteed regardless of cable impedance [8], [9]. For reliable DC bus voltage, the total DC bus impedance [10] may be characterized by each converter output impedance to avoid excessive voltage sags or surges during transients.

By increasing the output capacitance, the DC microgrid inertia increases, and the system voltage variations during load changes are negligible. However, it increases the weight, size, and cost of power converters, which are determinant in some applications like, for example, aircrafts [11]. Besides, large bus capacitance leads to more energy stored on the bus. In case of a DC bus short-circuit fault, it would induce a high fault current in magnitude and duration. This makes fault isolation difficult [12].

As long as the voltage is within the admissible range during any transient, the bus capacitance could be reduced. One of the first approaches, involving low output capacitance, constrained the load rate of change to fulfill the bus voltage objective [13], and described these systems as voltage weak DC microgrids [14]. However, such proposal is impractical considering the unknown behavior of loads. Then, it is more convenient to shape the output impedance by control means.

Previous control solutions looked for diminishing the output impedance magnitude in certain frequencies by means of additional output voltage feedback loops [15] or frequency-dependent droop loops [16]–[20]. This last technique is the Virtual-Capacitor (VC) control, which is also known as integral droop control or virtual inertia control. In droop-controlled converters, the desired output impedance should have a resistive-capacitive behavior because the output voltage variations related to load step changes need to be damped. Following this idea and output capacitance minimization, reference [21] and its extension [22] give a design guideline. However, both lack a systematic problem formulation that encompasses the whole controller tuning to reach the minimum capacitance for that specific power electronic converter. Besides, the controller design faces a trade-off between performance objectives and output impedance shaping. This multi-objective approach requires controller synthesis methodologies that can cope with it.

When looking for optimal controller designs, the design preference is always convex formulations because they ensure a global optimum solution for the specified problem. For instance, Linear Matrix Inequalities (LMIs) for each specification [23], [24] or, if all of them are gain constraints, a mixed-sensitivity $\mathcal{H}_\infty$ design approach [25]. However, an actual multi-objective control problem following convex formulations has some difficulties as conservatism [24] and high-order structures. Besides, industrial applications are more keen to fixed-structure control system like proportional-integral (PI) loops that facilitate implementation, validation, and re-tuning. Then, non-smooth optimization techniques [26] are a very convenient option

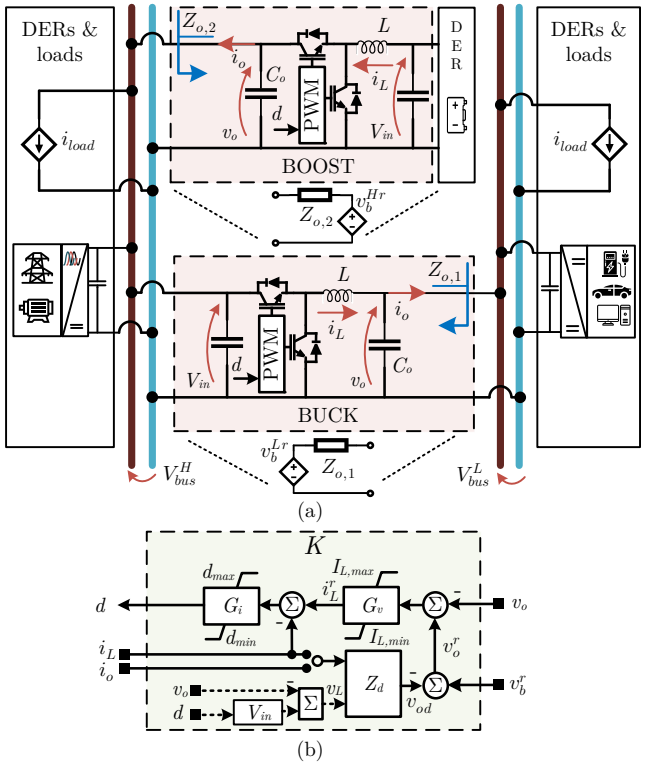

FIGURE 1. (a) DC microgrid example with high voltage, V_{bus}^H, and low voltage, V_{bus}^L, buses connected through an interlinking converter. Each converter dynamics can be equivalently defined as voltage source following a reference, v_b^r, with an output impedance, Z_o. (b) Controller, K, structure selected for buck or boost-type.

to find feasible solutions for multi-objective fixed-structure controller tuning [27], [28].

Our contributions in terms of droop-based controller design procedure are: 1) it is performed in a single-step, minimizing iterations over current and voltage loops because they are jointly designed; 2) it synthesizes low-order industry-suitable fixed-structure controllers; 3) it minimizes output capacitance; and 4) it guarantees the converter output voltage within the DC bus nominal range. The methodology is applied to control a bidirectional half-bridge converter operating as buck and boost, where the desired behavior depends on the application. For instance, Figure 1.(a) depicts a DC microgrid, where an interlinking half-bridge converter regulates the low DC voltage bus (buck-type), whereas another half-bridge converter interfacing an energy storage element regulates the high DC voltage bus (boost-type).

Section II introduces the proposal and underlying control objectives. Section III describes the theoretical limit for output impedance shaping. Section IV presents the controller tuning methodology. The experimental results for DC microgrids are given in Section V.

II. PROPOSAL DESCRIPTION

Detailed descriptions of bidirectional half-bridge converters operating as buck and boost are depicted in Figure 1.(a) and the corresponding controller for both in Figure 1.(b). The

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selected DC-DC converter topology is bidirectional, so that the mode of operation is always continuous current mode (CCM) because there is path for the inductor current on every possible switching state.

A. CONTROL OBJECTIVES

The ideal droop-controlled converter should behave as a voltage source with an output impedance, $Z_o(s)$, which is the parallel of the droop resistance, r_d, and output capacitance, C_o. Then, an output current, i_o, step leads to a smooth change of output voltage, v_o, because $Z_o(s)$ behaves as a first-order system. Simple control solutions imply undesired dynamics or additional capacitance leads to unnecessary oversizing. Alternatively, this proposal looks for output capacitance minimization and $Z_o(s)$ shaping by control means while keeping acceptable performances.

The most practical controller scheme for droop-based converters, see Figure 1.(b), is composed of three cascaded loops: inductor current, i_L, loop; output voltage, v_o, loop; and droop loop. The current and voltage controllers are $G_i(s) = k_{pi} + k_{ii}/s$ and $G_v(s) = k_{pv} + k_{iv}/s$, respectively. PI controllers are very convenient for the implementation of straightforward saturators as well as anti-windup structures. The droop loop sets the output voltage reference as

$$v_o^r = v_b^r - i_o \cdot Z_d(s), \tag{1}$$

where v_o^r is the output voltage reference, $Z_d(s)$ is the generalized frequency-dependent droop impedance to vary the output voltage depending on the load, and v_b^r is the DC bus voltage set point. This proposal will also use i_L instead of i_o at equation (1) because it is very convenient for $Z_o(s)$ shaping in buck-type converters.

Summarizing, this proposal aims to minimize C_o, while achieving the following control objectives by tuning only the parameters of $G_i(s)$, $G_v(s)$ and $Z_d(s)$:

1) Output impedance with resistive-capacitive behavior in order to reduce bus voltage sags and surges.
2) Good stand-alone robustness.
3) Damped tracking of v_o^r.

B. MULTI-OBJECTIVE CONTROLLER DESIGN

The control proposal will be approached within the framework of the generalized control problem shown in Figure 2 [29]. The generalized plant, $P(s)$, is a dynamic multiple-input multiple-output (MIMO) model composed of: the system to be controlled; and interconnected weighting functions that serve as a vehicle to translate design(er) control objectives into a design problem. Variable u (controller actuation vector) and y (measured output vector available for control) define the input-output structure of the controller. The relationship between w (disturbance input vector, including references) and z (error output vector desired to be kept small, specially on certain frequencies) defines the performance objectives.

The synthesized controller, $K(s)$, complies with the specifications or constraints which are imposed over each

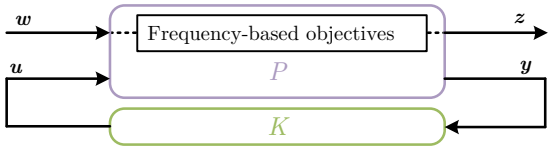

FIGURE 2. Controller, K, synthesis with requirements projected in generalized plant, P. Notation of (s) is avoided when derived from context.

channel of w and z, that is $w_j \rightarrow z_j$, by using frequency-dependent proper weighting functions identified by $W(s)$ and proper subscripts.

The proposed K has a predefined fixed-structure, see Figure 1.(b), and it is composed of tunable real-valued parameters. Then, any convex formulation [23]–[25] to synthesize K is not a possibility. The selected option is a non-smooth optimization technique using a first-order descent method explained in [26]. This computational tool is able to evaluate and enforce $\mathcal{H}_\infty$ (peak gain), $\mathcal{H}_2$ (average gain) as well as other frequency-based objectives for controller tuning [28]. This tool is fully implemented in `systune` and `hinfstruct` [27], [30].

Considering that a good gain objective achievement would be $\left\| z_j w_j^{-1} \right\|_\infty \leq 1$, our goals are translated as:

1) The control objectives 2) and 3) are defined between reference, $w_1 = v_b^r$, and voltage error, $z_1 W_s^{-1}(s) = e_u = v_b^r - v_o$. In order to ensure zero steady-state error in the inner current controller, an additional channel is projected between $w_1' = v_b^r$, and current error, $z_1' W_s^{-1}(s) = e_i = i_L^r - i_L$, where i_L^r is the inductor current reference. Besides, these objectives need an actuation constraint between reference, $w_2 = v_b^r$, and duty cycle, $z_2 W_u^{-1}(s) = d$.
2) The control objective 1) is defined over output current, $w_3 = i_o$, and output voltage, $z_3 W_z^{-1}(s) = v_o$.

The selection of what channels should be *soft*, function to be minimized, or *hard*, design constraints, requirements is up to the designer decision for a well-defined optimization problem. Taking into account the non-smooth $\mathcal{H}_\infty$ optimization framework, the local solution is a locally optimal controller in the set of *hard* requirements feasible controllers. Then, we must carefully select the constraints.

III. OUTPUT IMPEDANCE SHAPING BY THE DROOP LOOP

This section generalizes the output impedance shaping analysis for a general linearized DC-DC converter. Then, considering the shaping capabilities of the controller, a minimum capacitance value is derived. Additionally, the analysis allow us to define a droop impedance transfer function for achieving the required output impedance shaping.

A. THEORETICAL LIMITS

The general linearized model of a DC-DC converter can be expressed as follows: $G_{id}(s)$ and $G_{ii_o}(s)$ are the transfer functions from $\hat{d}$ and $\hat{i}_o$ to $\hat{i}_L$, respectively, and $G_{vi}(s)$ and

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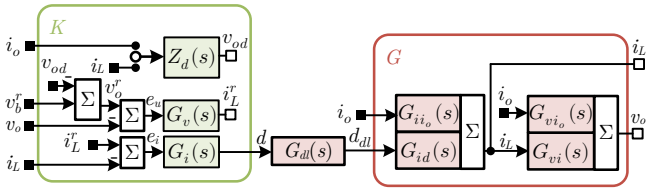

FIGURE 3. Linearized model of a general droop-controlled DC-DC converter, G, and controller, K.

$G_{vi_o}(s)$ are the transfer functions from $\hat{i}_L$ and $\hat{i}_o$ to $\hat{v}_o$, respectively. The diacritic mark $\hat{}$ indicates small-signal, and it will be removed in the following for the sake of clarity.

Following Figure 3, the current open-loop and closed-loop tracking transfer functions respectively are

$$L_i(s) = G_i G_{dl} G_{id}(s), \tag{2}$$

$$T_i(s) = \left.\frac{i_L}{i_L^r}\right|_{i_o=0} = L_i(s)/[1+L_i(s)], \tag{3}$$

where the zero-order-hold (ZOH) with sampling period T_s and the overall time delay T_d are given by

$$G_{dl}(s) = e^{-sT_d} \cdot \frac{1-e^{-sT_s}}{sT_s}. \tag{4}$$

For controller synthesis purposes, a first-order Padé approximation is enough for the exponential expressions of $G_{dl}(s)$.

The selection of i_L as input for Z_d implies that the closed-loop transfer function from v_o^r and v_b^r to v_o are slightly different. The voltage open-loop considering i_L and i_o, and closed-loop tracking transfer functions for both cases are, respectively,

$$L_v(s) = [G_v T_i G_{vi}(s)]/[1+T_i Z_d G_v(s)], \tag{5}$$

$$L_v(s) = [G_v T_i G_{vi}(s)], \tag{6}$$

$$T_v(s) = \left.\frac{v_o}{v_b^r}\right|_{i_o=0} = L_v(s)/[1+L_v(s)]. \tag{7}$$

Taking into account that the open-loop output impedance can be expressed as

$$Z_{ol}(s) = -\left.\frac{v_o}{i_o}\right|_{d=0} = -G_{vi}G_{ii_o}(s) - G_{vi_o}(s), \tag{8}$$

the closed-loop output impedance using i_L or i_o for droop, respectively, are

$$Z_o(s) = \frac{Z_{ol}(s) - G_{vi_o}L_i(s)}{1+T_i Z_d G_v(s)} S_i S_v(s) - T_v Z_d(s)\frac{G_{vi_o}(s)}{G_{vi}(s)}, \tag{9}$$

$$Z_o(s) = [Z_{ol}(s) - G_{vi_o}L_i(s)]S_i S_v(s) + T_v Z_d(s), \tag{10}$$

where $S_i(s) = 1 - T_i(s)$ and $S_v(s) = 1 - T_v(s)$ are the sensitivity transfer functions for the current and voltage loops, respectively. Let us define the voltage closed-loop bandwidth, ω_{Bv}, as the frequency where $|S_v(j\omega)| = 1/\sqrt{2}$ first crosses from below. Besides, the bandwidth in terms of T_v, ω_{BTv}, is the highest frequency at which $|T_v(j\omega)| = 1/\sqrt{2}$ from above. Then, up to ω_{Bv}, control is still effective improving the performance and allowing output impedance shaping. From ω_{Bv} to ω_{BTv}, control still affects response, but it degrades. Finally, at frequencies higher than ω_{BTv} control has no significant effect on the response [29]. The gain crossover frequency, $\omega_{cv} = 2\pi f_{cv}$, defined as the frequency where $|L_v(j\omega)|$ first crosses from above, usually lies between ω_{Bv} and ω_{BTv}. Although T_v depends on Z_d in expression (9), the closed-loop behavior is mainly commanded by G_v. Moreover, the effect of Z_d on the denominator of T_v, see expression (7) by using (5), could be neglected because, usually, $|G_{vi}(j\omega)| \gg |Z_d(j\omega)|$ at low and medium frequencies for buck-type converters. Consequently, the second addend of expressions (9) and (10) show that T_v lets Z_d to shape the low frequency behavior of Z_o in both cases. The medium and high frequency are determined by the first addend of expressions (9) and (10) because it is multiplied by S_v. Then, the actual output impedance shaping control limit is set to ω_{Bv}, and the controller should be able to shape the output impedance as a resistance, r_d, up to that frequency.

Considering the previous analysis and the parallel of r_d and C_o as ideal Z_o, the theoretical minimum output capacitance is derived from this first-order system pole as

$$C_o \geq \frac{1}{\omega_{Bv} r_d}. \tag{11}$$

The maximum attainable bandwidth, ω_{Bv}, may be limited by the time delay as well as the magnitude of the non-minimum phase zero of the system on the real axis in the right-half s-plane (real RHP-zero) [29], [31]. Usually, $\omega_{Bv} < 1/T_d$ for the former and $\omega_{Bv} < z_s/2$ for the latter, where z_s is the location of the real RHP-zero. Therefore, we will push the controller design up to these limits to reach the minimum capacitance. This minimum value is higher than the one required by the desired output voltage ripple and maximum output current of the application [32], [33].

B. DROOP IMPEDANCE PROPOSAL

The current and voltage controller structures have been defined, thus we must select a structure for Z_d. Considering $Z_o(s) = r_d$ on expressions (9) and (10), the droop impedance using i_L or i_o should be, respectively:

$$Z_d(s) = -\frac{r_d G_{vi}(s)}{G_{vi_o}T_v(s)} - \frac{G_{vi}G_{ii_o}S_i(s) + G_{vi_o}(s)}{T_i G_v G_{vi_o}(s)}, \tag{12}$$

$$Z_d(s) = \frac{r_d}{T_v(s)} - \frac{Z_{ol}S_i(s) - G_{vi_o}T_i(s)}{L_v(s)}. \tag{13}$$

Within $\omega < \omega_{Bv}$, T_v and T_i can be approximately considered as a unit gain, which respectively leads expressions (12) and (13) to:

$$Z_d(s) \approx -\frac{r_d G_{vi}(s)}{G_{vi_o}(s)} - \frac{1}{G_v(s)}, \tag{14}$$

$$Z_d(s) \approx r_d + \frac{G_{vi_o}(s)}{G_{vi}G_v(s)}. \tag{15}$$

Then, Z_d depends on r_d, the voltage controller and converter topology via G_{vi} and G_{vi_o} [22]. It is deduced from (14) that not all DC-DC converters can use i_L measurement for droop because expression G_{vi}/G_{vi_o} may depend on the operating point. This paper analyzes both cases: i_L for droop on buck-type converters; i_o for droop on boost-type converters.

Expressions (14) and (15) demonstrate that a frequency-dependent droop is required to achieve the desired performance, so that we are going to generalized the droop impedance, $Z_d(s)$, as

$$\begin{bmatrix} \dot{x}_z \\ v_{od} \end{bmatrix} = \left(\begin{array}{c|cc} -d_0 & d_0(r_d - D_{z1}) & 0 \\ \hline 1 & D_{z1} & D_{z2}/L \end{array}\right) \begin{bmatrix} x_z \\ i_L|i_o \\ v_L \end{bmatrix}, \quad (16)$$

where d_0 defines the location of the pole, D_{z1} sets a zero and D_{z2} adds a theoretical derivative term. They are tunable parameters and L is the power filter inductance. The inductor voltage, v_L, is an indirect measurement to improve the output impedance shaping capabilities when i_L is used for droop because of its derivative behavior to counteract the gain falling of T_v in (9). In our case of study for buck-type, such derivative is indirectly defined by $s \cdot i_L = v_L/L = (V_{in}d_{dl} - v_o)/L$, where V_{in} is the converter input voltage and d_{dl} is the output of G_{dl}.

If the operating conditions require a different r_d, the control system can change its value according to (16). Although it will change the dynamic behavior of Z_o, the system stability is ensured without changing the designed control parameters. Controller and capacitance are going to be tuned for a given operating point, so that lower r_d will lead to higher over or undershoot, whereas higher r_d will lead to totally damped voltage transients.

IV. CONTROLLER DESIGN BY MULTI-OBJECTIVE OPTIMIZATION

The proposed multi-objective controller design is applied to buck-type and boost-type converters. Here, we introduce both linearized models and constraints over the droop impedance proposal for each case as well as the optimization problem formulation to tune the controllers.

A. CASES UNDER STUDY

The linearized state-space model of buck-type half-bridge converter, $G(s)$, see Figure 1.(a), is given as follows [34]:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 0 & \frac{V_{in}}{L} \\ -\frac{1}{C_o} & 0 \end{bmatrix} \begin{bmatrix} i_o \\ d \end{bmatrix}, \quad (17)$$

where V_{in} is considered constant. The cases under study for buck-type converter use i_L as input on (16) and the following constraints:

1) *TR-BK*: Traditional approach where $Z_d(s) = r_d$.
2) *C1-BK*: Reference case where the tunable variables are constrained, according to [22] and (14), as the value of other tunable parameters, that is $d_0 = k_{iv}/k_{pv}$, $D_{z1} = r_d - 1/k_{pv}$ and $D_{z2} = 0$.
3) *C2-BK*: Proposed case for additional C_o minimization capabilities where d_0, D_{z1} and D_{z2} are independently tunable.

The linearized state-space model of boost-type half-bridge converter, $G(s)$, see Figure 1.(a), is given as follows [34]:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D_p}{L} \\ \frac{1-D_p}{C_o} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 0 & \frac{V_{op}}{L} \\ -\frac{1}{C_o} & -\frac{I_{lp}}{C_o} \end{bmatrix} \begin{bmatrix} i_o \\ d \end{bmatrix}, \quad (18)$$

where V_{op} is the static output voltage, I_{lp} is the static inductor current, and D_p is the static duty cycle. In steady state, $V_{in} = (1 - D_p)V_{op}$ and $I_{op} = (1 - D_p)I_{lp}$, where V_{in} is considered constant, $V_{op} = V_b^r/(1 + r_d/R_{load})$, being R_{load} the equivalent resistive load, and $I_{op} = V_{op}/R_{load}$. We will consider the full load model for controller analysis because the dynamics does not change a lot with respect half or null load [22]. The cases under study for boost-type converter use i_o as input on (16) and the following constraints:

1) *TR-BT*: Traditional approach where $Z_d(s) = r_d$.
2) *C1-BT*: Modified proposed case inspired by [22] where d_0 is independently tunable and $D_{z1} = 0$ and $D_{z2} = 0$.
3) *C2-BT*: Proposed case with a zero to counteract the gain falling of T_v, where d_0 and D_{z1} are independently tunable and $D_{z2} = 0$.

For buck-type cases, the sampling period equals the switching period, $T_s = T_{sw}$, and $T_d = T_s/2$. For boost-type cases, the sampling period is half the switching period, $T_s = T_{sw}/2$, and $T_d = T_s$.

B. OPTIMIZATION PROBLEM FORMULATION

The objectives presented in Section II-A can be translated to a formal definition by using the corresponding plant model, weighting functions and controller as Figure 4 depicts. Such definition helps to find feasible solutions because known structures from controller K are encapsulated into P. System K_c encloses tunable parameters as $K_{ic} = [k_{pi}, k_{ii}]^T$, $K_{vc} = [k_{pv}, k_{iv}]^T$, and those involved in Z_d as d_0, D_{z1} and D_{z2}. Please note that x_{ri} and x_{ru} are the integrator states of the current and voltage controllers, respectively. It also let us weight the current control error, e_i, to ensure zero steady-state value.

The multi-objective optimization problem that formally defines the goals in Section II-B becomes

$$\begin{aligned} \underset{K}{\text{minimize}} \quad & \left\| \begin{matrix} W_s S_v \\ W_s S_i G_v S_v \\ W_u S_{ur} \end{matrix} \right\|_\infty, \\ \text{subject to} \quad & \|W_z Z_o\|_\infty \leq 1 \end{aligned} \quad (19)$$

where $W_s(s)$, $W_u(s)$ and $W_z(s)$ are the tracking, control effort and output impedance weights, respectively. The control action sensitivity transfer function from v_b^r to d is defined as $S_{ur}(s) = G_i S_i G_v S_v(s)$

Cases *TR-BK*, *C1-BK*, *TR-BT* and *C2-BT* may not be able to fulfill the *hard* requirement, so that $\|Z_o\|_\infty \leq r_d$

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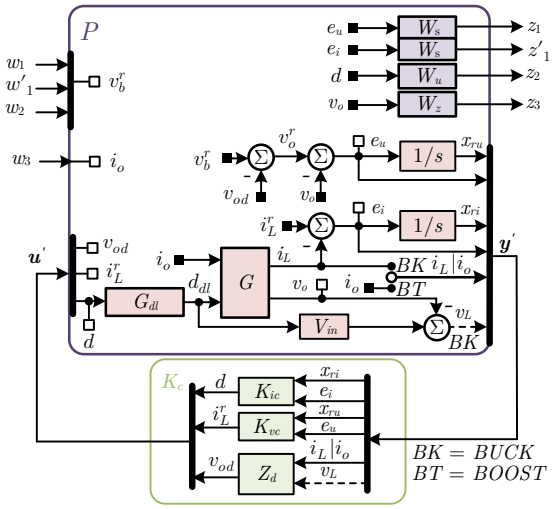

FIGURE 4. Proposed multi-objective problem (19) (or (20) using $q = 4$ channels over the generalized plant, P, to synthesize K_c, which is composed of all tunable parameters of K.

becomes a *soft* requirement. Besides, the structure on case *C1-BK* only depends on the voltage controller, and it is ready to shape the output impedance. The multi-objective optimization problem is posed as

$$\underset{K}{\text{minimize}} \left\| \begin{matrix} W_s S_v \\ W_s S_i G_v S_v \\ W_u S_{ur} \\ W_z Z_o \end{matrix} \right\|_\infty . \tag{20}$$

This non-smooth optimization tool allows multi-model problem definition, so that it is able to synthesize a static controller that fulfills all objectives for a set of R_{load} in the boost-type cases. The resulting controllers, even considering negative R_{load} when the converter operates as load, are similar to the ones designed with the full load model for boost-type.

C. WEIGHTING FUNCTION SELECTION

The desired tracking performance objective is defined [29] by

$$W_s(s) = \frac{s + \omega^*_{Bv}}{s}, \tag{21}$$

where ω^*_{Bv} is the desired voltage closed-loop bandwidth, which is associated to the minimum C_o as expressed by (11). Let us recall that the selection ω^*_{Bv} depends on the presence of time delays and/or RHP-zeros. This weighting function shapes S_v by multiplying by its ideal inverse. If W_s has infinity DC gain, the controller K must be synthesized so that S_v has zero DC gain. This would mean that the system follows references. In order to ensure zero steady current control error, this function serves to independently weight both e_u and e_i. Both current and voltage loops are simultaneously tuned, so that this approach will let us to tighten their bandwidths and achieve the best output voltage tracking response in a one-step design. Besides, we consider that this weight also tries to minimize the stand-alone robustness indicator given by $\|S_v\|_\infty = \|1/(1 + L_v)\|_\infty < 6$ dB, which guarantees a gain margin, $GM \geq 6$ dB, and phase margin, $PM \geq 29°$ [29]. For *C2-BK*, $S_{vt}(s) = 1 - T_v(s)$ is not exactly the sensitivity transfer function, S_v, due to v_o measurement for Z_d, but they are similar.

The control effort objective is imposed with $W_u(s) = k_u$, where k_u is the inverse of the desired $\|S_{ur}\|_\infty$. Additionally, the maximum spectral radius for stabilized dynamics has been set to the Nyquist frequency, $\omega_N = \pi T_s$. Both definitions constrain all stabilized poles and zeros from going to infinity as a result of algebraic loops becoming singular or control effort growing unbounded.

The output impedance objective is defined by the inverse of the maximum allowed droop value, that is $W_z(s) = 1/r_d$.

All gain objectives are evaluated by computing a normalized scalar value of the infinity norm via a fast algorithm [30]. Please note that this is a offline tuning methodology for static controllers.

Finally, we must evaluate the main tuning goals, that is, the gain requirements over $\|Z_o\|_\infty \leq r_d$ and $\|S_v\|_\infty < 6$ dB. If they are not accomplished, it means that the output capacitance cannot be further reduced using this control structure, filter inductor, switching frequency and selected closed-loop bandwidth, ω^*_{Bv}, among other factors. In our case, we only iterate over ω^*_{Bv} and its related C_o, by using (11). The resulting closed-loop bandwidths may be lower than the ones selected, ω^*_{Bv}, using (21). However, as long as the control requirements are fulfilled, we accept the resulting bandwidth and keep the desired C_o.

D. CONTROL PARAMETERS TUNING

The initial tunable parameters values are key point to find acceptable solutions. The initial values can be given by previous knowledge about them or random values for every new run of the optimization problem. However, a mix of both of them is considered here by constraining the possible random values for each parameter as: $k_{pi},\ k_{ii},\ k_{pv},\ k_{iv} \in \mathbb{R}^+$; $0 < d_0 < \omega^*_{Bv}$; and $D_{z1},\ D_{z2} \in \mathbb{R}$. The parameter d_0 is constrained so that the pole introduced by Z_d is stable and slow enough.

The optimization problem (20) always falls in exactly the same solution, whereas (19) requires at least 100 random initial points to ensure finding an acceptable solution.

V. RESULTS

This section presents the results of the selected cases with the aim of demonstrate the capabilities of the proposed controller design methodology to reduce C_o.

The time-domain results are collected considering a DC microgrid with two equivalently controlled half-bridge converters, see Figure 5, connected to a load. The system parameters are collected in Table 1, and they have been selected to compare this proposal with the methodology and droop structures presented in [22]. We are following two comparison methodologies to demonstrate the improvement

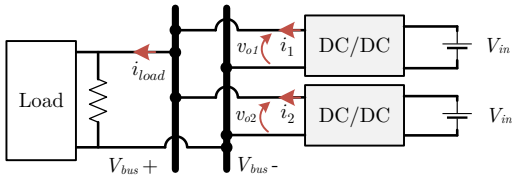

FIGURE 5. Experimental setup with 2 droop-based buck-type or boost-type half-bridge converters equally designed.

TABLE 1. System setup parameters

Parameter	Symbol	Buck	Boost
Input voltage	V_{in}	380 V	200 V
Voltage set point	V_b^r	200 V	380 V
Nominal power	P_n	3 kW	3 kW
Inductance	L	1.6 mH	1 mH
Output capacitance	C_o	100|160 µF	100 µF
Switching frequency	f_{sw}	12.5 kHz	10 kHz
Droop resistance	r_d	1.33 V/A	2.53 V/A

of proposed cases, *C2-BT* and *C2-BK*. For boost-type, C_o is kept constant to show better results, while, for buck-type, C_o is reduced to show the same results.

A. BOOST-TYPE DC MICROGRID

Cases *TR-BT*, *C1-BT* and *C2-BT* are designed with the same objectives. The maximum desired voltage closed-loop bandwidth that fulfills the objectives for the latter case is $\omega_{Bv}^* = 2\pi 628$ rad/s, which is lower than the theoretical limit considering the RHP-zero location with full load, $\omega_{Bv} < z_s/2 = V_{in}^2 R_{load}/(2LV_{op}^2) = 2\pi 1061$ rad/s, which is the most restrictive situation. Please note that such limit is expressed for an ideal controller [29], and we are dealing with a cascaded voltage control which is only able to achieve a bandwidth close to that limit. Following equation (11), the minimum output capacitance is 100 µF, if we round it up. The constants for the other weighting function are $k_u = 10$ and $r_d = 2.53$.

The optimization solution for both current and voltage controller are summed up in Table 2.

1) Frequency-domain analysis

Figure 6 compares the main closed-loop dynamics. Figure 6.(a) depicts the frequency response in magnitude of W_s^{-1} against the resulting S_v for each case. All cases accomplish objective $\|S_v\|_\infty < 6$ dB with considerably good phase and gain margins, see Table 2. Both cases *C1-BT* and *C2-BT* share similar dynamics because they have reached similar current controller solutions, while *TR-BT* is slower than both of them. Figure 6.(b) shows that both *C1-BT* and *C2-BT* have high $\|S_{ur}\|_\infty$, which means a high control effort because of their higher bandwidth, see f_{cv} in Table 2.

The output impedance, Z_o, Bode plots are compared in Figure 6.(c). It also displays the measured Z_o in a switching simulation, where all cases match the theoretical characteristic up to 5 kHz. On the one hand, *C2-BT* is the most similar one to a first-order system and $Z_o(s) < r_d$, so that the load changes cause minimum under or overshoot. On the other hand, *TR-BT* completely fails on the requirement of $\|Z_o\|_\infty < r_d$, and any load change will lead to significant under or overshoot, whereas *C1-BT* only reduced $\|Z_o\|_\infty$. These results demonstrate that low output capacitance requires a well-designed controller and, specifically, the droop control structure, Z_d. Please note the differences on S_v and Z_o between *C1-BT* and *C2-BT*

The tracking, T_v, Bode plots are compared in Figure 6.(d), where *TR-BT* is expected to have a small overshoot on step changes of v_b^r. Cases *C1-BT* and *C2-BT* share similar tracking characteristics. However, *C2-BT* is the most damped case.

Table 2 sums up the evaluation indices, where the stand-alone stability margins of the voltage loop come from the definition $L_v(s) = 1/S_v(s) - 1$ for the voltage open-loop considering the whole system. Case *C2-BT* is able to achieve the objectives with good stability margins and reduce the output capacitance by 23.08% with respect to [22], which is a considerable value by control means.

2) Experimental results

Figure 7 depicts the DC bus voltage, V_{bus}^H, or, equivalently, the output voltage of each converter, v_{o1} and v_{o2}, variation under the same load step for each boost-type case. When both converters are designed following case *TR-BT*, V_{bus}^H has a significant transient sag of 13.75 V and a settling time, within a ±2%, of 12.5 ms, see Figure 7.(a). Considering that the voltage droop variation is 5.06 V, the voltage undershoot is 171.74%, which is unacceptable. For case *C1-BT*, see Figure 7.(b), the voltage sag is lower than the previous case with an undershoot of 97.6% and a settling time of 45 ms. Still, the voltage is kept within the admissible range in 10 ms, which is acceptable. Case *C2-BT*, see Figure 7.(c), leads to a very low undershoot of 24.7% and the voltage reaches steady-state in 5 ms. Then, only case *C2-BT* has an acceptable response with a considerably low output capacitance.

As conclusion, *C2-BT* performs generally better because it strictly achieves all control objectives with a 23.08% lower C_o with respect to reference [22]. Please note that the considered switching frequency, f_{sw}, is half the one considered in reference [22]. Case *C1-BT* replicates the controller structure proposal in such reference. However, the solution does not achieve the requirements because the overall time delay, T_d, is higher.

B. BUCK-TYPE DC MICROGRID

The maximum voltage closed-loop bandwidth that fulfills the objectives for *TR-BK* and *C1-BK* is $\omega_{Bv}^* = 2\pi 750$ rad/s, which corresponds to $C_o = 160$ µF. Case *C2-BK* achieves

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2020.3044171, IEEE Access

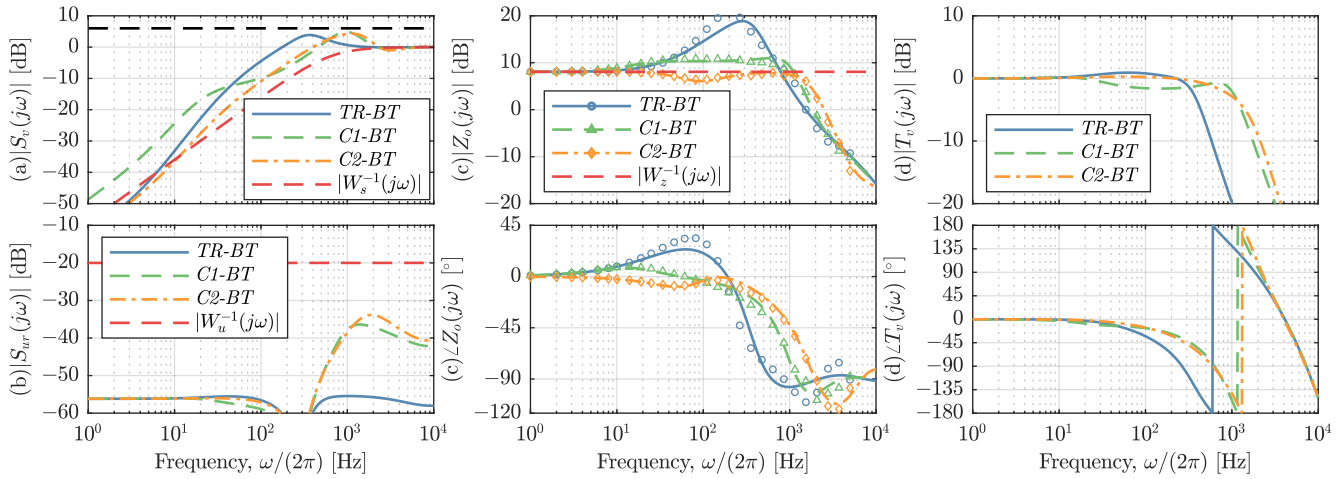

FIGURE 6. Design objectives comparison for boost-type cases *TR-BT*, *C1-BT* and *C2-BT* (solid, dashed and dash-dot lines, respectively) with full load model: (a) Bode magnitude of sensitivity, S_v, related to design channel $w_1 \rightarrow z_1$ with weight W_s considering $\omega^*_{Bv} = 2\pi 628$ rad/s; (b) Bode magnitude of control effort, S_{ur}, related to channel $w_2 \rightarrow z_2$ with weight W_u; (c) Bode plot of theoretical and simulated measured (circle,○, triangle, △, and diamond, ⋄, respectively) output impedance, Z_o, related to channel $w_3 \rightarrow z_3$ with weight W_z; (c) Bode plot of tracking, T_v.

TABLE 2. Comparison of goals and synthesized controller gains for boost-type

Case	C_o[μF]	$\|S_v\|_\infty$	$\|Z_o\|_\infty$	$\|S_{ur}\|_\infty$	PM[°]	f_{cv}[Hz]	GM[dB]	k_{pi}	k_{ii}	k_{pv}	k_{iv}	d_0	D_{z1}	D_{z2}
TR-BT	100	1.56	8.77	0.002	57.9	184	12.8	0.01	1.59	0.14	260.1	-	-	-
C1-BT	100	1.75	3.54	0.015	70.1	402	8.01	0.02	2.37	0.43	72.37	162.9	0	0
C2-BT	100	1.64	2.53	0.02	63.6	374	8.48	0.025	3.71	0.39	258.3	520.4	−1.67	0

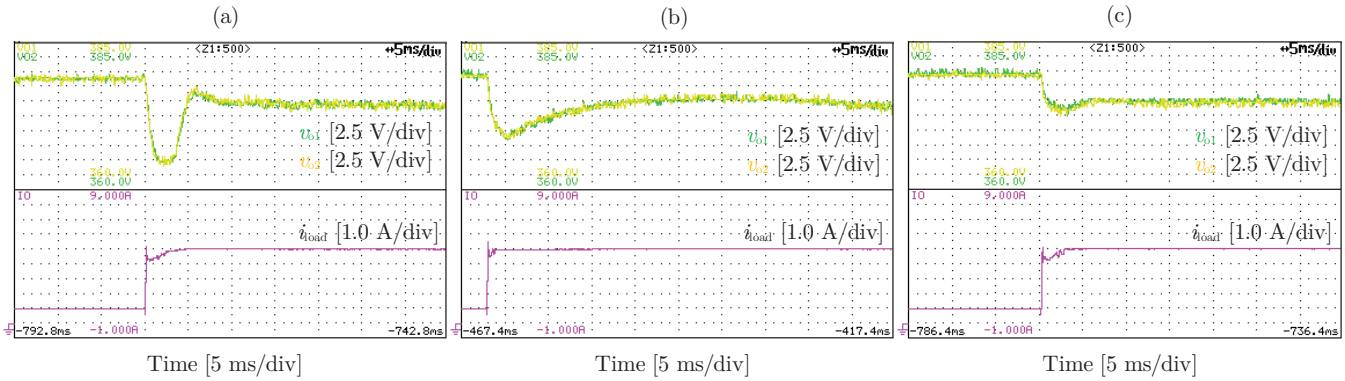

FIGURE 7. Experimental results of boost-type DC microgrid under a power load step change: (a) *TR-BT*; (b) *C1-BT*; (c) *C2-BT*.

the objectives with $\omega^*_{Bv} = 2\pi 1150$ rad/s, which corresponds to $C_o = 100$ μF, if we round it down. Both desired bandwidths are lower than the theoretical limit considering the time delay, $\omega_{Bv} < 1/T_d = 2\pi 3979$ rad/s. The constants for the other weighting function are $k_u = 10$ and $r_d = 1.33$

The optimization solution for both current and voltage controller are summed up in Table 3.

1) Frequency-domain analysis

Figure 8.(a) depicts the frequency response in magnitude of two ideal sensitivity goals, W_s^{-1}, against the resulting one, S_v, for each case, which are close for cases *C1-BK* and *C2-BK*, respectively. Still, *C1-BK* with even more capacitance than *C2-BK*, fails to accomplish the objective $\|S_v\|_\infty < 6$ dB. Figure 8.(b) shows that *C2-BK* requires higher $\|S_{ur}\|_\infty$ at higher frequencies, which means a high control effort. A lower capacitance requires higher voltage loop bandwidth, and it leads to higher control efforts, that is, a faster control action.

The output impedance, Z_o, Bode plots are also compared in Figure 8.(c). The actual output impedance, which is also depicted, is experimentally measured using the Software Frequency Response Analyzer (SFRA) library embedded in the Texas Instruments digital controllers. Under a steady-

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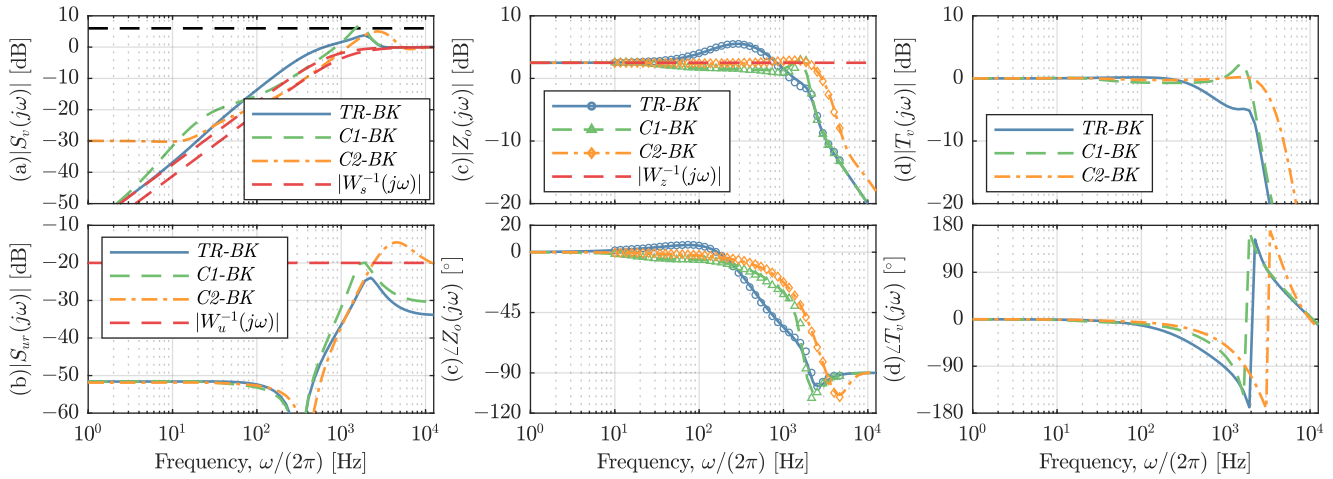

FIGURE 8. Design objectives comparison for each buck-type cases *TR-BK*, *C1-BK* and *C2-BK* (solid, dashed and dash-dot lines, respectively): (a) Bode magnitude of sensitivity, S_v, related to design channel $w_1 \rightarrow z_1$ with weight W_s considering two possibilities ($\omega^*_{Bv} = 2\pi 1150$ rad/s and $\omega^*_{Bv} = 2\pi 750$ rad/s); (b) Bode magnitude of control effort, S_{ur}, related to channel $w_2 \rightarrow z_2$ with weight W_u; (c) Bode plot of theoretical and experimentally measured (circle,$\circ$, triangle, $\triangle$, and diamond, $\diamond$, respectively) output impedance, Z_o, related to channel $w_3 \rightarrow z_3$ with weight W_z; (c) Bode plot of tracking, T_v.

TABLE 3. Comparison of goals and synthesized controller gains for buck-type

Case	C_o[µF]	$\|S_v\|_\infty$	$\|Z_o\|_\infty$	$\|S_{ur}\|_\infty$	PM[°]	f_{cv} [Hz]	GM[dB]	k_{pi}	k_{ii}	k_{pv}	k_{iv}	d_0	D_{z1}	D_{z2}
TR-BK	160	1.55	1.89	0.063	72.7	459	9.19	0.023	4	0.87	1176	-	-	-
C1-BK	160	2.23	1.41	0.104	61.2	843	5.6	0.032	4.4	0.95	133.5	139	0.28	0
C2-BK	100	1.78	1.36	0.19	61.3	1170	7.62	0.015	2.5	5.05	951	148	1.19	$5 \cdot 10^{-5}$

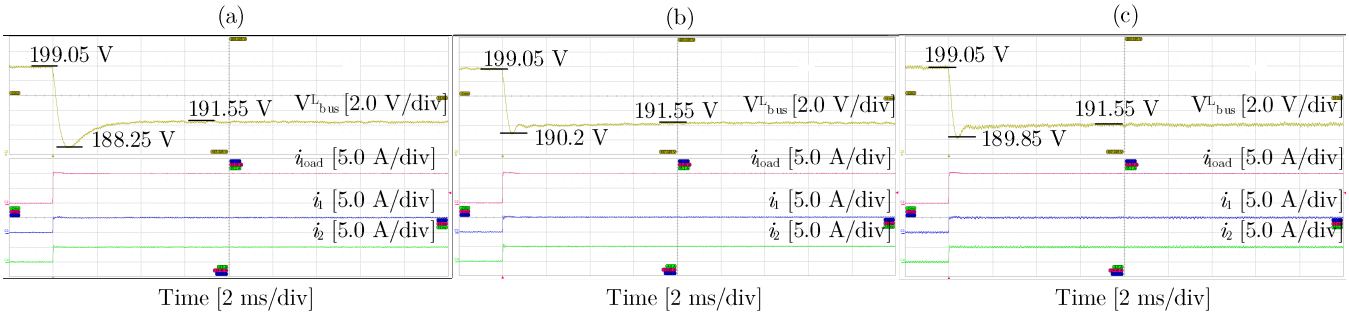

FIGURE 9. Experimental results of buck-type DC-microgrid under a power load step change: (a) *TR-BK*; (b) *C1-BK*; (c) *C2-BK*.

state operation point, one converter injects sinusoidal small-signal perturbation into the DC microgrid for each frequency. Meanwhile, the converter under measurement collects its output current and output voltage signals. Then, the fast Fourier transform is applied on the collected data. We may anticipate that case *TR-BK* has under or overshoot with any load step change because the requirement $Z_o(s) < r_d$ is unaccomplished. On the other hand, although its closed-loop dynamics are characterized by two complex conjugate poles, *C2-BK* is the most similar one to a first-order system. Then, along with case *C1-BK*, minimum under or overshoot is expected.

Figure 8.(d) depicts the voltage tracking, T_v, frequency responses agreement with Z_o, as expression (9) establishes. It demonstrates that Z_d must be frequency-dependent to keep the output impedance gain below the maximum value. Besides, T_v is slightly more damped in *C2-BK* than *C1-BK*.

Table 3 sums up the evaluation indices. Case *C2-BK* has been able to partly achieve the objectives (high control effort) and reduce the output capacitance by 37.5% with respect to case *C1-BK* [22].

2) Experimental results

The experimental tests are carried out in a laboratory-scale DC microgrid prototype with bus voltage V^L_{bus}. The load, i_{load}, is changed using a Chroma DC electronic load 63204A. The system parameters for both converters are reported in Table 1.

Figure 9 depicts the DC bus voltage variation under the same load step for each droop impedance case. When both converters are designed as *TR-BK*, V_{bus}^{L} has a significant transient sag of 10.8 V, as depicted in Figure 9.(a). The steady-state voltage variation caused by the droop is 7.5 V, which means a considerably high voltage undershoot of 44%. For *C1-BK*, the bus voltage sag is 8.85 V, as depicted in Figure 9.(b). The voltage undershoot is 18%, which is a significant reduction of the voltage sag only by control means. Besides, the voltage sag lasts 1 ms, whereas in the previous case it lasts 3 ms. A slightly higher capacitance would damp even better the voltage variations. However, the objective of this research is to find the output capacitance limit. Finally, Figure 9.(c) depicts the bus voltage sag of case *C2-BK*. This experiment shows a voltage sag of 9.2 V, that is translated into a 22.66% undershoot. This voltage sag lasts 1 ms with less oscillations, which equals *C1-BK* case. The dynamic behavior of the proposed design droop, *C2-BK*, is very similar to *C1-BK* [22], but it must be noted that the output capacitance is a 37.5% lower.

VI. CONCLUSION

This systematic controller design approach has been proven to be helpful on limiting the capacitance oversizing that designers tend to do. This approach is repeatable and it is not only based on simple common sense and trial and error. Cascaded controllers tuning is usually performed loop by loop. However, once the droop loop is closed, the designed voltage closed-loop response changes, because the droop is out of the analysis. Therefore, it is interesting to design the controller as a whole that complies with the desired voltage control loop performance and output impedance objectives.

The proposed design has explored the limits of this control structure by means of multi-objective optimization techniques that can manage such designs in an automatic fashion. The multi-objective optimization problem proposed here may be extrapolated for other controller organizations and hardware characteristics. However, the designer should always take into account that the objectives must be in accordance with the proposed control structure and plant.

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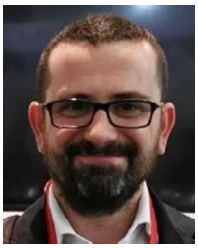

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