Monolithic active quenching and picosecond timing circuit suitable for large-area single-photon avalanche diodes

A. Gallivanoni, I. Rech, D. Resnati, M. Ghioni and S. Cova

Politecnico di Milano, Dipartimento di Elettronica e Informazione, and IFN-CNR Sezione di Milano
Piazza Leonardo da Vinci 32, 20133 Milano
gallivan@elet.polimi.it

Abstract: A new integrated active quenching circuit (i-AQC) designed in a standard CMOS process is presented, capable of operating with any available single photon avalanche diode (SPAD) over wide temperature range. The circuit is suitable for attaining high photon timing resolution also with wide-area SPADs. The new i-AQC integrates the basic active-quenching loop, a patented low-side timing circuit comprising a fast pulse pick-up scheme that substantially improves time-jitter performance, and a novel active-load passive quenching mechanism (consisting of a current mirror rather than a traditional high-value resistor) greatly improves the maximum counting rate. The circuit is also suitable for portable instruments, miniaturized detector modules and SPAD-array detectors. The overall features of the circuit may open the way to new developments in diversified applications of time-correlated photon counting in life sciences and material sciences.

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1. Introduction

Time-correlated single photon counting [1] (TCSPC) is the technique of choice for time-resolved measurement of fast and/or weak fluorescent emissions in a wide range of applications in chemistry, biology, medicine and material science. Typical examples are: single molecule detection and spectroscopy [2-4], DNA sequencing [5-7] and fluorescent lifetime imaging [8]. It is also widely employed in various other fields, such as fiber optic characterization with optical time domain reflectometry [9-11]; profiling of remote objects

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with optical radar techniques [12, 13]; quantum cryptography [14, 15]; picosecond imaging circuit analysis [16, 17]. The time resolution obtained fundamentally depends on the precision with which the instant of arrival of a photon on the detector is identified. Because of the presence of strong background and/or of the requirement of limiting the time required to collect sufficient information, in various cases it is necessary to operate at high counting rates, up to a few Mcount/s. Fast TCSPC instruments and PC cards have been developed and are nowadays currently available for this purpose [18, 19]. Avoiding degradation of the photon timing resolution at high counting rates is therefore an important requirement for the single-photon detector and associated circuit.

Photon timing systems have been introduced and developed over four decades relying on photomultiplier tubes (PMTs), that is, vacuum tube devices. In more recent years, several alternative to PMTs have been investigated [20]. Among all these, a solid state example has been provided by the development of special avalanche photodiodes able to detect single optical photons by working in Geiger mode at voltage higher than the breakdown level, which are therefore called Single-Photon Avalanche Diodes [21-23] (SPADs). Besides the well known advantages of solid state versus vacuum tube devices (small size, ruggedness, low power dissipation, low supply voltage, high reliability, etc.), SPADs provide higher quantum efficiency, particularly in the red and near infrared spectral regions. A dedicated circuit must be associated to a SPAD for quenching the avalanche and resetting the detector after the detection of each photon. The introduction of monolithic integrated Active Quenching Circuits (iAQC) [24] opened the way to the design and implementation of miniaturized detector systems [25]. As concerns photon timing, the data reported in the literature provide evidence that the same SPAD device can exhibit remarkably different performance working with different types of quenching circuits, showing that the features of the circuit play an important role in this respect. In fact, in order to best exploit the detector performance a dedicated timing circuit that can be added to any existing type of active-quenching circuit has been devised [26,27].

We present in this paper a new integrated active quenching circuit that includes in a single chip (i) a complete quenching and timing circuitry that avoids recourse to a separate additional timing circuit, (ii) a circuit capable of exploiting the inherent photon timing resolution of the detector up to high counting rate and (iii) a circuit that can efficiently work with any existing SPAD device, including diodes with wide area and devices operating in cryogenic conditions. Section 2 briefly deals with the operation of SPADs, summarizes the different timing performances obtained with the various available SPAD devices in operation with different circuits and outlines the reasons for such differences. Section 3 describes the design of the new monolithic integrated circuit that includes an improved active quenching loop and a fast timing section. Section 4 reports and discusses the results of experimental tests.

2. SPADs, quenching circuits and photon timing performance

SPADs are p-n junctions that have uniform breakdown voltage over the active area and low rate of thermal generation of carriers and can thus be operated at bias voltages higher than the breakdown level. In this condition a single carrier generated or injected in the depletion region can trigger a self-sustaining avalanche current (Geiger mode). The current swiftly rises (with subnanosecond risetime) to a macroscopic level in the milliampere range and can thus be easily sensed. If the primary carrier is photogenerated, the leading edge of the avalanche pulse marks the arrival time of the detected photon. The SPAD operation is fundamentally different from that of PMTs and of ordinary APDs, because SPADs do not provide a linear amplification of the primary photogenerated carriers, but they rather behave like a bistable trigger circuit. After the triggering of the avalanche, the current goes on flowing until the avalanche is quenched by lowering the bias voltage down to the breakdown level or below it. SPADs must therefore be operated with suitable quenching circuits, which terminate the avalanche and then restore the detector bias to the operating level, in order to detect another photon. Passive Quenching Circuits, PQCs, and Active Quenching Circuits, AQCs, can be

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employed to this end [23]. In the PQCs the avalanche current quenches itself by developing a voltage drop on a high impedance load. In the AQCs, the leading edge of the avalanche current is sensed by a threshold circuit that drives a controlled voltage source, which forces very fast quenching and reset transitions.

SPADs can be fabricated with planar processing in CMOS compatible technology [28]. Many data reported in the literature show that for such SPAD devices with very small active area (diameter less than 10 μm) photon timing resolution with better than 50 ps full width at half maximum (FWHM) is currently obtained with different types of quenching and timing circuits. By monolithically integrating a passive quenching circuit with the SPAD device and therefore by drastically reducing the capacitance discharged and speeding up the reset transition, Rochas *et al.* have experimentally demonstrated that such a resolution can be attained even with a PQC and maintained up to high counting rate [29]. However, as the diode diameter is increased a progressive degradation of the timing resolution obtained with planar CMOS compatible SPADs is observed [30] and the actual performance markedly depends on the type of circuit employed.

Silicon SPADs fabricated with a proprietary dedicated technology by Perkin Elmer Optoelectronics [31,32] (formerly EG&G Optoelectronics) and called Slik^{TM} have wide area (180 micron diameter), low noise and very good photon detection efficiency also in the red spectral range; they are employed in popular Single Photon Counting Modules (SPCM-AQR).

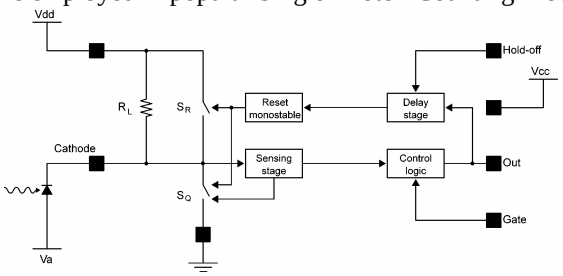

Fig. 1. Simplified block diagram of the integrated active-quenching and active-reset circuit previously developed by our group.

The photon timing resolution obtained with these wide-area devices strongly depends on the circuit employed. Less than 200 ps FWHM has been obtained with Slik^{TM} detectors operating with dedicated circuits, specifically devised for timing [23, 33, 34], but remarkably higher FWHM values have been reported from tests on SPCM-AQR modules [35]. The SPCM-AQR data sheet [32] quoted a typical time resolution of 350 ps FWHM and fairly wider FWHM is often measured for the SPCM-AQR samples.

The marked dependence of the resolution obtained for SPAD devices with active area wider than 10 μm on the circuit employed for timing the pulses can be understood by taking into account the physical processes that determine the rise of the avalanche current. As illustrated and discussed in [30, 36, 37] it turns out that, after the very first part where the multiplication of carriers is localized within a small area around the seed point (the point of incidence of the photon) and the current rises with fairly small statistical fluctuations, the rise to the final value corresponds to the progressive spreading of the multiplication over all the sensitive area of the detector and has stronger statistical fluctuations. Consequently, if the triggering threshold of the circuit that senses the avalanche pulse is reached during the spreading of the avalanche over the area instead of the very first part of the rise, the resulting timing jitter is remarkably larger, since it depends on the cumulative fluctuation of the current rise up to that level. Any low-pass filtering effect that slows down the rise of the pulse sensed by the timing circuit will have the effect of shifting the triggering instant to later time along the avalanche rise and it will therefore degrade the timing resolution. For SPAD devices with

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wider area the lateral propagation effect is stronger; furthermore, the larger intrinsic capacitance of the diode significantly contributes to the parasitic low-pass filtering action.

We have recently demonstrated that the trade-off between active area diameter and time resolution may be overcome by detecting the avalanche current during the initial part of the rise, about at a hundred microampere level [38]. By employing a separate current pick-up circuit, we obtained an unprecedented time resolution of 35 ps with a 100 μm active area diameter SPAD. This technique opens the way to the use of large-area SPADs in high-performance TCSPC measurements. Large-area devices represent a definite advantage in these applications, since they make it possible to relax the optical alignment requirements without sacrificing the photon collection efficiency. Furthermore, fiber pigtailing may be routinely made on these devices, thus allowing for more flexible optical detection systems.

3. Integrated active quenching and timing circuit

The starting point of the design was a critical analysis of the previous active-quenching and active-reset circuit integrated in a 0.8 μm CMOS high-voltage technology [24]. Figure 1 shows a simplified block diagram. The SPAD is biased above the breakdown voltage at $V_B = V_{DD} - V_A$ through a high resistance load. A mixed passive-active quenching is exploited to minimize the avalanche charge and the related afterpulsing effect due to carrier trapping [22, 33]. Once an avalanche is triggered the cathode parasitic capacitance is swiftly discharged, thus reducing the avalanche current. The sensing stage detects the avalanche rise and causes the switch S_Q to close, starting the active quenching. The control logic delivers a standard TTL-level output pulse that is used for pulse counting. The control logic output pulse propagates through a delay stage, which determines the time interval where the SPAD is kept biased under breakdown (hold-off), and then triggers the reset monostable. This last block causes switches S_Q to open and S_R to close, thus restoring the SPAD bias to quiescent value. Eventually, the switch S_R is opened and the detector is ready to detect another photon.

A first drawback of this circuit is that the voltage signal on the cathode terminal is inherently unsuitable for high resolution photon timing. In fact, this signal is generated by the integration of the avalanche current on the SPAD capacitance plus the stray capacitance of the cathode terminal. The avalanche rise is thus sensed by the trigger circuit after a low pass filtering action, which makes it not possible to trigger on the very first part of the avalanche rise even with a very low level of the sensing threshold.

A second drawback is due to the reset circuit. In general, the reset transitions must be as short as possible to minimize the probability that a photon triggers an avalanche during the reset transition. Such a triggering event is detected only at the end of the reset pulse, leading to incorrect timing information. Moreover, the avalanche current triggered during the reset is not sensed until the reset phase is over, therefore the avalanche charge is increased with associated detrimental effects (after pulsing etc.). A fast reset transition is usually achieved by designing the reset MOS transistor (switch S_R in Fig. 1) with a very high size ratio. A drawback of such a design is associated to the high parasitic capacitance C_{GD} between gate and drain terminals. When the reset MOS is turned off, the gate command is capacitively coupled through C_{GD} to the cathode terminal, causing a voltage overshoot that decays with a long time constant, given by the product of the cathode parasitic capacitance and the load resistance (a few microseconds in the current design). At high counting rate, the random superposition of such overshoots causes a random shift of the baseline, that is, a shift of the SPAD bias voltage that degrades the timing performance. This problem might be in principle overcome by reducing the load resistance value. However, a load resistor of a few tens of kilo-ohms is mandatory for obtaining the initial passive quenching of the SPAD device [24].

The integrated circuit was therefore extensively redesigned for circumventing the drawbacks above described. A further objective of the design was to obtain stable and reliable operation of the circuit over a wide temperature range, making the circuit able to operate also in deeply cooled ambient, at least down to -60 °C. The most significant modifications, namely

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the addition of a fast timing stage and the replacement of the load resistance by an active load, will be described in some detail.

3.1. Timing stage

The stage is based on the technique introduced in our laboratory and patented [26] for extracting the avalanche pulse produced by a SPAD device. The basic idea is to implement a suitable pick-up of the fast avalanche current signal from the SPAD terminal connected to the

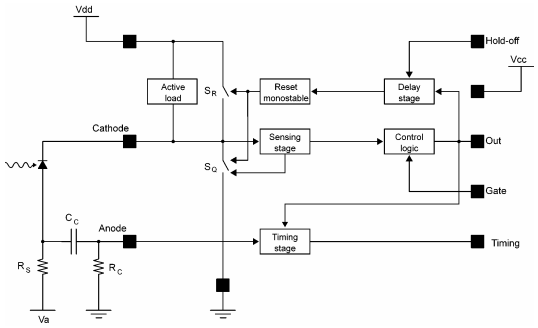

Fig. 2. Simplified block diagram of the modified i-AQC.

high bias voltage, leaving the low-voltage SPAD terminal connected to the AQC. As outlined in Fig. 2, the solution is an AC (alternating current coupling) network, consisting of a signal resistor R_s, a coupling capacitor C_c and a coupling resistor R_c. The time constant of the linear network must be longer than the risetime of the avalanche current, in order to extract the detector signal without affecting its initial rise. This is mandatory for allowing a true low-level sensing of the avalanche current. On the other hand it must be much shorter than the average interval between pulses (i.e., than the reciprocal of the repetition rate). Otherwise, the random superposition of the long tails generated by the differentiation after every pulse causes a shift of the baseline, with a mean value and statistical fluctuations that have adverse effect on the photon timing resolution (peak shift and widening of the resolution curve) that increase with the counting rate. The voltage signal which develops on $R_s//R_C$ is fed to the inverting input of a fast comparator which performs the timing discrimination. A high-sensitivity, fast-switching voltage comparator has been designed, based on the work of Kim *et al* [39]. A simplified schematic of the comparator is shown in Fig. 3. It includes two differential pairs (M_1-M_3; M_2-M_4), each one with its tail current source (M_5, M_6). The tail sources are themselves biased by one of the outputs of the differential pairs to increase the tail current when switching and, thus, the speed of the output transitions. From experimental measures employing artificial test pulses, we observed comparable intrinsic time jitter figures from the new comparator shown in Fig. 3 and the previously used comparator, connected on the cathode side.

During the reset phase, the voltage at the SPAD anode is increased to V_{DD} in less than 10 ns. Due to the coupling through the photodiode capacitance, a spurious pulse is generated on the anode. This pulse is potentially dangerous, since it may retrigger the comparator resulting in a self-sustaining oscillation of the circuit. In order to avoid this drawback, a latch pulse that masks the comparator during the reset phase is provided by the Control Logic.

The pick-up network with Rs = 1 kΩ, Rc = 1 kΩ, Cc = 4.7 pF was connected to the anode of the SPAD. This network performs a high-pass filtering of the avalanche current with a time constant variable between 5 ns and 10 ns depending on the intrinsic diode resistance, which is sufficiently longer than the risetime of the avalanche pulse. Reliable operation free from false triggering was achieved with a minimum threshold voltage of 30 mV, which corresponds to a current threshold level of about 120 μA.

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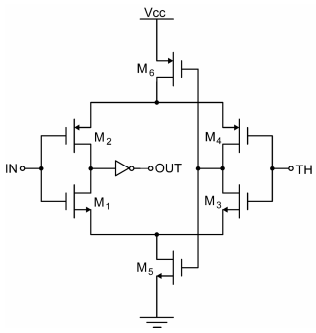

Fig. 3. Simplified schematic of the voltage comparator used in the timing stage.

3.2. Active load

Instead of the load resistor of the previous circuit, an active load was employed. The scheme adopted is essentially a current mirror, as shown in Fig. 4. While the SPAD is in quiescent

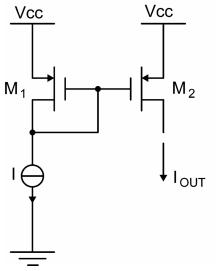

Fig. 4. Simplified schematic of the active load that replaces the load resistor of the previous i-AQCs.

state, current cannot flow in the output MOS transistor, thereby keeping it in the ohmic region. As the avalanche is triggered, the current starts flowing in the diode and discharges the cathode capacitance, lowering the cathode voltage. M_2 exits ohmic region and enters saturation region, where the current mirror behaves like a current generator with an output resistance given by the Early resistance of M_2. This high resistance causes the avalanche current to be swiftly reduced by the passive quenching action, until it approaches the level of the mirror output current. Complete quenching of the avalanche current is anyway ensured if the mirror output current is sufficiently small. However, after the first passive quenching action, active quenching sets in and active reset is finally performed as usual in AQCs. At the end of the reset phase, the mirror output transistor M_2 finds itself in the reverse ohmic operating region, where the MOS channel is not pinched off, neither on the Source side nor on the Drain side, but unlike in the usual ohmic region, the channel is deeper near the Drain. This is due to the voltage overshoot that makes the drain voltage to go higher than the source voltage. A beneficial effect is that the MOS channel resistance in this operating region is quite small; therefore, the time constant of the recovery of the cathode voltage from the overshoot to quiescent level is short and the recovery is fast.

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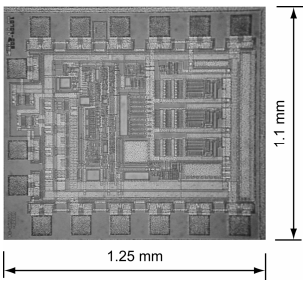

Fig. 5. Microphotograph of the new i-AQC chip.

4. Experimental results

The new iAQC chip is shown in Fig. 5. It is fabricated with a high-voltage 0.8 μm CMOS technology with two metals and a high-resistive poly. Its size is 1.25 mm × 1.1 mm. The quiescent power dissipation is about 20 mW.

We first evaluated the performance of the timing stage. Time resolution measurements were performed in a time-correlated single photon counting (TCSPC) setup employing an ultrafast laser diode (Antel MPL-820 laser module) emitting optical pulses at 820 nm wavelength with about 10 ps FWHM. Table I shows a comparison of the FWHM time resolution obtained with SPAD devices having different active area diameters. Planar CMOS compatible SPADs [28] were operated at room temperature with low counting rate (10 kHz).

Table I. Comparison of the time resolution FWHM obtained with SPAD devices having different active area diameters. Devices were operated at room temperature with low counting rate (10 kHz). The two series of results were obtained by operating the SPADs at 5 V and 10 V excess bias voltage and by using the output signal from the active quenching circuit (counting out) and the output signal from the timing stage (timing out).

SPAD diameter (μm)	Time resolution FWHM @ 5 V (ps)		Time resolution FWHM @ 10 V (ps)	
	COUNTING OUT	**TIMING OUT**	**COUNTING OUT**	**TIMING OUT**
10	35	35	33	32
50	250	80	120	48
100	260	200	130	80

The two series of results obtained by using the output signal from the active quenching circuit (counting out) and by using the output signal from the timing stage (timing out) are reported.

As expected, with small area devices there is practically no advantage in using the fast timing out, whereas for large area SPADs the advantage is very evident. The improvement of the performance achieved with the fast timing out is more evident in Fig. 6, where the time resolution curves for a 50 μm SPAD are shown.

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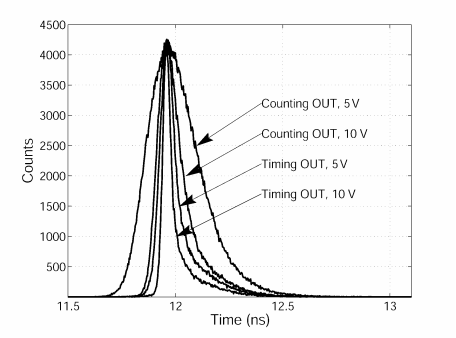

Fig. 6. Time resolution curves of a 50 µm SPAD measured at different excess bias voltages by using the output signal from the active quenching circuit (counting out) and the output signal from the timing stage (timing out).

Although it is still possible to achieve moderately improved performance with discrete components [38], the results of this work are nearly as good and they are fully integrated into a monolithic detector unit, which makes it possible to easily implement detector arrays. Moreover, the performances of the integrated voltage comparator are limited by the technology employed, characterized by a fairly long channel (0.8 µm). Further improvement can be gained by exploiting more advanced CMOS technologies for implementing a faster comparator, capable of operating with lower voltage threshold.

Figure 7 compares the cathode voltage recovery at the end of the reset phase observed with the new active load to that of the previous circuit with a high-resistance load. The recovery of the voltage overshoot is exponential with a time constant shorter than 100 ns in the case of the active load, whereas the recovery time constant is well above a microsecond for the high-

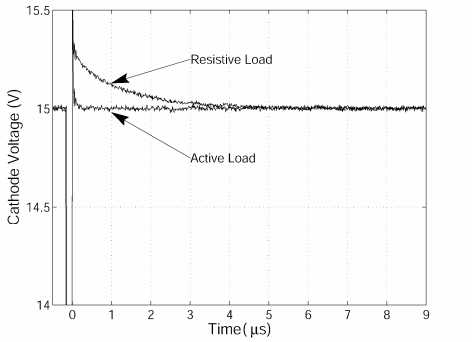

Fig. 7. Cathode voltage recovery at the end of the reset phase observed with the new active load compared to that of the previous circuit with a high-resistance load. The recovery of the voltage overshoot is exponential with a time constant shorter than 100 ns in the case of the active load, whereas the recovery time constant is well over a microsecond for the high-resistance load.

resistance load. Such a remarkable improvement makes it possible to operate the SPAD at counting rates well above 1 Mcount/s without suffering a degradation of the FWHM value and a systematic shift of the centroid and of the peak of the photon timing distribution. This is confirmed by the experimental measurements reported in Fig. 8, where no appreciable degradation of the time resolution is observed for counting rates up to 5 Mcount/s.

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Extensive experimental tests were carried out at -60 °C. All tests confirmed that the circuit reliably operates in ambient at low temperature without showing significant variation of the characteristic parameters with respect to operation at ambient temperature.

Tests were also carried out with other types of SPAD devices with satisfactory results. In particular, the timing results obtained with Slik^{TM} devices were equivalent to the best previously reported as obtained with dedicated circuits [2, 23, 27, 34].

It can be concluded that the new integrated active quenching circuit is suitable for operating with any available SPAD type over a wide temperature range and provides remarkably improved time resolution with large area SPAD detectors.

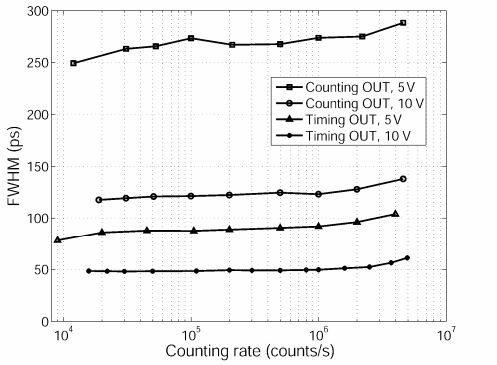

Fig. 8. Time resolution FWHM of a 50 µm SPAD operated at 5 V and 10 V excess bias voltage as a function of the counting rate. Curves are obtained by using the output signal from the active quenching circuit (counting out) and the output signal from the timing stage (timing out). No appreciable degradation of the time resolution is observed for counting rates up to 5 Mcount/s.

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