THERMAL MANAGEMENT OF THE THROUGH SILICON VIAS IN 3-D INTEGRATED CIRCUITS

by

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The through silicon via technology is a promising and preferred way to realize the reliable interconnection for 3-D integrated circuit integration. However, its size and the property of the filled-materials are two factors affecting the thermal behavior of the integrated circuits. In this paper, we design 3-D integrated circuits with different through silicon via models and analyze the effect of different material-filled through silicon vias, aspect ratio and thermal conductivity of the dielectric on the steady-state temperature profiles. The results presented in this paper are expected to aid in the development of thermal design guidelines for through silicon vias in 3-D integrated circuits.

Key words: *thermal, through silicon via, 3-D integrated circuit; nanoscale flow*

Introduction

With the rapid development of electronic science and technology, 3-D integrated circuit (3-D IC) technology emerging as a powerful tool for satisfying requirements for the challenging integrated circuit packaging has received tremendous attention in the semiconductor community [1-4]. By expanding the design space into the third dimension, 3-D IC obtains significant electrical performance benefits compared with previous packaging technologies, such as better performance, reduced average wire length, wire delay, lower power consumption and footprint, *etc.* [5-9]. However, with the increasing integration of 3-D IC, the power consumption per unit volume increases dramatically, which makes effective cooling more challenging due to the higher power density [10-14]. Once a system fails to remove these heat, the temperature rises. A chip's ability to sufficiently remove the generated heat has become a dominant factor in determining performance and reliability of IC. In the era of 3-D IC, the problems of heat dissipation are more serious than those in the traditional single IC package. Hence, the thermal management of the 3-D IC becomes a major concern [15-18].

Through silicon via (TSV) technology is one of the key technologies of 3-D IC, which can provide vertical internal electrical connection functions between multilayer chips in the advanced 3-D IC. Vertical integration provides a promising solution to reduce interconnect power and delay while increasing transistor density independent of costly device scaling. The TSV based 3-D IC packaging mainly consists of via formation, via filling, wafer thin-

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ning, and chip stacking. The TSV are essentially metal pillars that penetrate the silicon substrate to engage the metal pads of the layer below [19-23]. With the introduction of TSV, its special structure and thermal properties have some influences on the peak temperature of 3-D IC. So, in this paper, the effects of material filled, aspect ratio (AR) and the thermal conductivity on TSV thermal behavior were investigated by the finite element model established in the paper. The TSV with different materials filled, AR and thermal conductivity of dielectric were set up, respectively. The results presented in this paper are expected to aid in the development of thermal design guidelines for TSV in 3-D IC.

Analysis model

The physical and thermal model of the 3-D IC are shown in fig. 1, where the different layers are bonded by the bonding-layer to form a 3-D structure, and different layers are inter connected using TSV, while the number of devices that can be integrated within the system is limited [24]:

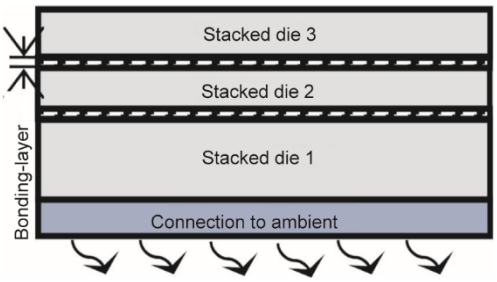

Figure 1. The 3-D IC model

$$\frac{\alpha N_{\mathrm{G}} E}{t_{\mathrm{pd}}} \le g\Delta T \tag{1}$$

where α is their activity rate, N_{G} – the number of gates that can be integrated within a system with a clock period t_{pd}, g – the average thermal conductance, ΔT – the temperature gradient between the dissipating elements and the ambient air, and E – the energy dissipation.

Heat flow in the 3-D IC is governed in a control volume of a solid with an isotropic thermal conductivity by the following equation [25]:

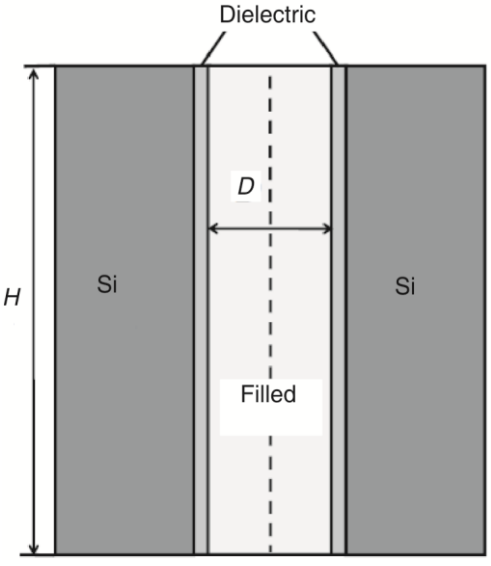

Figure 2. The TSV structure

$$C_{\mathrm{v}} \frac{\mathrm{d}T}{\mathrm{d}t} + (-k\nabla^2 T) = \dot{q} \tag{2}$$

where C_{v} is the volumetric specific heat of the material, T – the temperature of the control volume, k – the thermal conductivity of the material, and $\dot{q}$ – the volumetric rate of generation of the heat inside the volume.

As the key technology, TSV technology provides vertical inter-electrical connection functions between different layers in the 3-D IC. The TSV consists of the dielectric isolation layer, metal filled layer and diffusion barrier layer. In general, the thickness of the diffusion barrier is on nanoscale, and the nanoscale hydrodynamics can deal with the velocity distribution and temperature distribution across the thickness [26-29], which is, however, far less than the dielectric barrier-layer, and its effect on thermal effect is very small, so the diffusion barrier layer is omitted in this model, as shown in fig. 2.

With the introduction of TSV, its special structure and thermal properties will affect the temperature characteristics of 3-D IC, the thermal conductivity of the die can be described as effective thermal conductivity k_{eff}, which is written:

$$k_{\text{eff}} = k_{\text{mat}}\left(1 - \frac{A_{\text{TSV}}}{A_{\text{die}}}\right) + k_{\text{TSV}}\frac{A_{\text{TSV}}}{A_{\text{die}}} \tag{3}$$

where k_{mat} and k_{TSV} are the thermal conductivities of the layer material and the TSV material, respectively, A_{die} – the area of die, and A_{TSV} –the area of the TSV. From eq. (3), we can find that TSV has a certain influence on the thermal distribution of 3-D IC. In the following contents, we mainly study the influence of the structure and the related thermal properties of TSV on the temperature distribution of 3-D IC.

Experimental results

In this section, we study the effect of TSV structure such as the AR, the TSV thermal properties such as the material filled and the thermal conductivity of the dielectric on the temperature distribution of the 3-D IC, respectively.

Case 1. Effect of the aspect ratio

In this case, we study the effect of different AR on temperature in the 3-D IC. The AR are 10, 12, 15, 20, 25, and 30, respectively. The maximal temperature of 3-D IC in different AR of different material filled was shown in fig. 3(a). It can be seen from the diagram that the AR has a certain influence on the temperature of 3-D IC, where the effect on temperature is large when the AR is between 10 and 20, and when the AR is greater than 20, the effect on temperature is small.

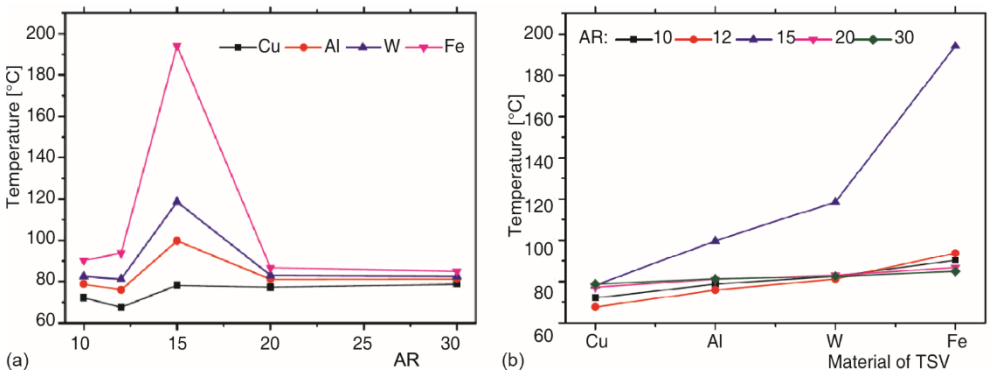

Figure 3. (a) temperature profile *vs.* AR, (b) temperature of different material-filled TSV

Case 2. The impact of different material filled TSV

In this case, we change the material of the TSV-filled to find out the impact on the temperature, where the filled material are Cu, Al, W, and Fe. As shown in fig. 3(b), it is found that the temperature of the 3-D IC increases according to the order of Cu, Al, W, and Fe, which is related to the gradual decrease of their thermal conductivity. In order to observe the effect of different material-filled, we change the AR to observe the experimental results. The results show that when the AR is different, the curves of different filled material are the same,

that is the temperature of the 3-D IC increases according to the order of Cu, Al, W, and Fe in different AR.

Case 3. The impact of different material of the dielectric

The impact of different material-filled dielectric is studied in this case, the dielectric constants for used materials are 8, 20, 40, and 60 W/(m°C), respectively. Figures 4(a)-4(d) show the temperature variation of 3-D IC of different material-filled dielectric in different AR with Cu-filled TSV, Al-filled TSV, W-filled TSV, and Fe-filled TSV, respectively. Obviously, for different AR of different TSV-filled materials, temperature curves decrease with the increase of thermal conductivity of the dielectric.

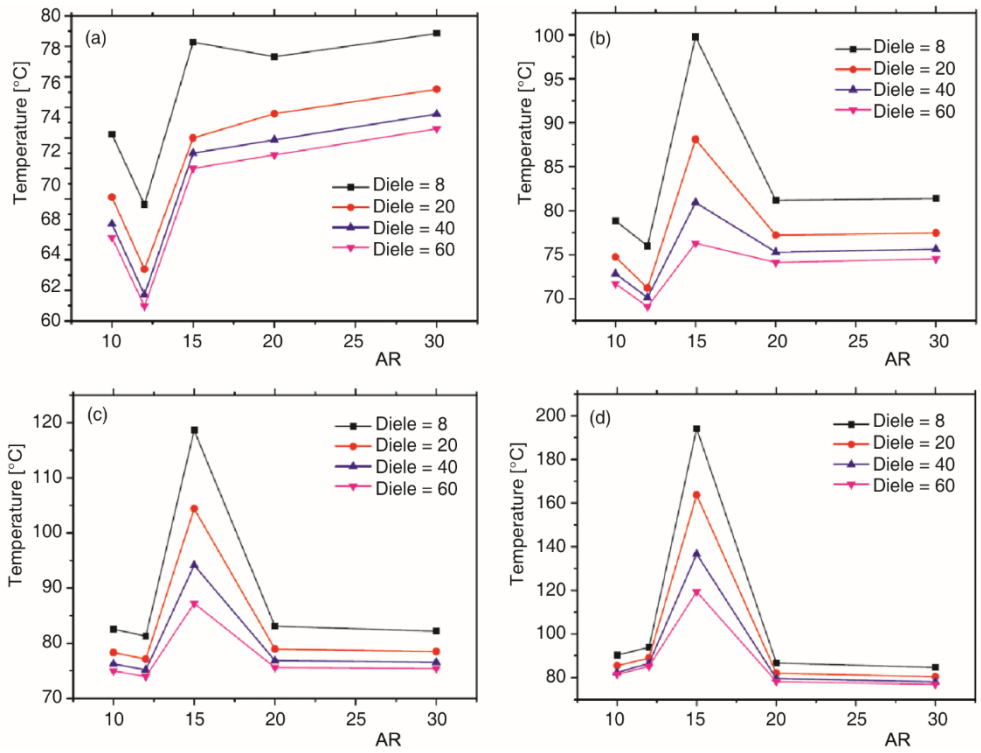

Figure 4. Temperature of different material-filled dielectric

On the basis of the previous analysis, and from the point of the thermal management of the TSV based 3-D IC, the following design guidelines can be concluded.

– Cu is a better material for the TSV-filled than Al, W, and Fe.
– The thermal conductivity of dielectric materials should be as large as possible.
– In the design of TSV, the AR should be selected properly.

Conclusion

In this paper, the effects of 3-D IC with different TSV models and different material-filled, AR and dielectric thermal conductivity on the steady-state temperature profiles are

studied. The results presented in this paper are expected to aid in the development of thermal design guidelines for TSV in 3-D integrated circuit.

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