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Research Article

A Cost-Effective 10-Bit D/A Converter for Digital-Input MOEMS Micromirror Actuation

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The design of a 10-bit resistor-string digital-to-analog converter (DAC) for MOEMS micromirror interfacing is addressed in this paper. The proposed DAC, realized in a 0.18-μm BCD technology, features a folded resistor-string stage with a switch matrix and address decoders plus an output voltage buffer stage. The proposed DAC and buffer circuitry are key elements of an innovative scanning micromirror actuator, characterized by direct digital input, full differential driving, and linear response. With respect to the the state-of-the-art resistor-string converters in similar technologies, the proposed DAC has comparable nonlinearity (INL, DNL) performances while it has the advantage of a smaller area occupation, 0.17 mm^2, including output buffer, and relatively low-power consumption, 200 μW at 500 kSPS and few μW in idle mode.

1. Introduction

Nowadays, the market of microelectromechanical systems (MEMS) and micro-opto-electromechanical systems (MOEMS) is rapidly increasing with many target applications in consumer, industrial, automotive, avionic, and biomedical fields. Particularly, MOEMS micromirrors are enabling new market applications such as front and palm-sized projectors for office or consumer scenarios and head-up display for automotive infotainment. MOEMS micromirrors combine optical and actuator components on the same chip and hence they have the advantage of being smaller, less power consuming and cheaper with respect to existing macromirror devices [1, 2].

The challenging driving and sensing of these micromechanical structures often require a heavy digital signal-processing chain. Therefore, a key element in the MOEMS interfacing electronics is the availability of cost-effective DACs. In this work, first we present an innovative driver scheme for digital-Input actuation of a double-axis micromirror, and then we present an optimized area and power-efficient 10-bit DAC which can be integrated as a hard macro in the single-chip realization of the driver. This system is intended to be used in a high-resolution projection display together with an RGB laser source system. To enable the development of portable projection systems the DAC has stringent target requirements in terms of power consumption, which should be in the order of hundreds of μW, and area occupation, with a target occupation much lower than 1 mm^2.

The paper is organized as follows. The scanning micromirror system and the new actuation scheme are described in Section 2. Section 3 presents the DAC architecture and the design optimizations followed to minimize area and power consumption costs: design space exploration to find a resistor-string sizing with optimal trade-off between area and linearity (INL and DNL), new decoding logic, and power-idle circuitry. Implementation results and comparison with the state of the art are presented in Section 4. The DAC has been implemented in the 0.18-μm Bipolar CMOS DMOS (BCD) technology of STMicroelectronics which provides high-voltage (HV) devices and low-power cells on the same chip [3–6]. Conclusions are drawn in Section 5.

2. Scanning Micromirror System and Driver

2.1. Scanning Micromirror. A micromirror is a micromechanical actuator designed for the continuous deflection

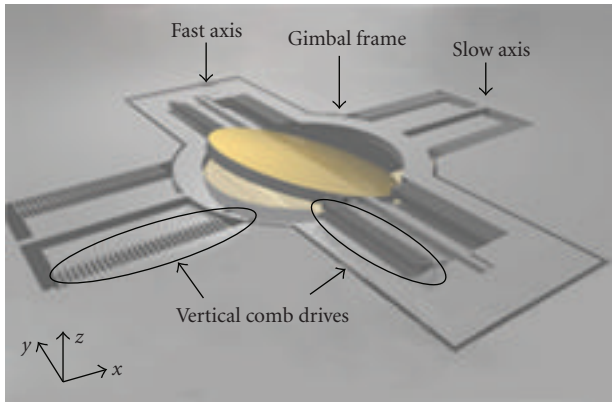


Figure 1: Scanning micromirror layout.

of light. It is characterized by large scan angle, high flatness and high scanning frequency [1, 2]. The electrostatically actuated double-axis micromirror used as reference for the design of the laser projection system, the DAC works for is developed within a collaboration between SensorDynamics AG and the Fraunhofer Institute for Silicon Technology (ISIT) [2, 7–10]. As reported in Figure 1 it consists of a circular polysilicon mirror plate covered with aluminum and connected to a gimbal frame by a pair of polysilicon torsion springs. The two axes operate at two different resonating frequencies. Many prototypes of this MOEMS micromirror have been developed operating at different frequencies. The slow axis frequency, which allows the micromirror to be tilted around x direction, ranges from 300 Hz to 1 kHz, while the fast axis frequency ranges from 15 kHz to 30 kHz and allows the micromirror to be tilted around y direction. Thus, scanning of all the columns (y direction) and rows (x direction) of a video display can be obtained with this MOEMS. Both axes are actuated by electrostatic vertical comb drives that consist of a set of moving electrodes and a set of rigid electrodes suspended over an etched pit.

2.2. Digital-Input Actuation Scheme. Applying a voltage between the fixed fingers (fixed electrodes) and the movable fingers (movable electrodes), an electrostatic torque arises between the two electrodes. Consequently, the movable fingers rotate around the torsional axis until the electrostatic torque (T_e) and the mechanical restoring torque (T_m) of the springs are equal. The equations describing the micromirror motion are the following:

$$T_m = H \cdot \alpha, \qquad T_e = 0.5 \cdot N_f \cdot V^2 \cdot \frac{dC}{d\alpha}, \tag{1}$$

where N_f is the number of the fingers of the comb drives, V is the voltage applied, α is the rotation angle, C is the capacitance between a fixed finger and a movable finger which depends on the angle α, and H is the torsional spring constant. Hence, from (1), the electrostatic torque T_e depends quadratically on the driving voltage signal.

The MOEMS requires a vacuum package and has to be actuated in resonance in order to reach large enough optical scan angle, about 15 degrees on the fast axis, and 10 degrees on the slow axis to match the VGA standard requirements in a projection system with peak-to-peak driving voltages higher than 10 V [2].

In the proposed system for each micromirror axis there are three actuators, see Figure 2: two are represented by the fixed fingers bound to the substrate and one is represented by the movable fingers electrically and mechanically connected to the micromirror. The micromirror can be actuated connecting to electrical ground the movable fingers and applying two 180° out-of-phase sine waves of same amplitude ($\pm v$) summed to a constant voltage Vb to the fixed fingers thus forcing two torques T_1 and T_2. The total resulting applied torque will be $T_{\text{etot}} = T_1 - T_2$, and we can write

$$\begin{aligned} T_{\text{etot}} &= 0.5 \cdot N_f \cdot \frac{dC}{d\alpha} \cdot (Vb + v)^2 \\ &\quad - 0.5 \cdot N_f \cdot \frac{dC}{d\alpha} \cdot (Vb - v)^2 \\ &= 0.5 \cdot N_f \cdot \frac{dC}{d\alpha} \cdot 4Vb \cdot v = K \cdot v. \end{aligned} \tag{2}$$

As reported in Figure 2, the driving signals $V_1 = Vb + v$ and $V_2 = Vb - v$, thanks to the adoption of the D/A converters with buffer circuitry, can be directly provided through a digital interface that can be connected to a host digital system.

Differently from other actuation schemes for MEMS/MOEMS proposed in literature [11], which are based on switching amplifiers, the approach we propose implements a linear topology thus meeting the stringent linearity requirements coming from the video projection application. Indeed from (2), there is a linear relationship between the resultant torque T_{etot} and the amplitude of the applied differential signals $+v/-v$ with a sensitivity K that can be regulated through the bias voltage Vb ($K = 0.5 \cdot N_f \cdot dC/d\alpha \cdot 4Vb$).

Moreover, the proposed driving scheme has also several advantages versus single-ended MEMS/MOEMS drivers [12]: the gain is twice with respect to a single-ended solution; the harmonic distortions are reduced thanks to the inherently symmetry of the circuit; the immunity to common mode noise sources is higher.

Finally, it is worth noting that differently from other biasing options considered in [13] (such as using a nonnull constant low-voltage value ζ, different from Vb, to supply the moveable fingers) the scheme in Figure 2 simplifies the actuation electronics.

The proposed innovative driving principle is implemented by a driving interface, fully integrated in BCD technology, whose architecture is sketched in Figure 2. It is composed by the analog-input HV fully differential driver we presented in [13] together with the DAC whose design is detailed in Sections 3 and 4. Particularly from the MOEMS transducer driving specification two equal 10-bit DACs have to be used to generate the $V1$ and $V2$ stimulating waves that are separately buffered and amplified to the required voltage range by the HV driver.

The HV driver, whose circuit details and BCD implementation results are presented in [13], is basically an inverting

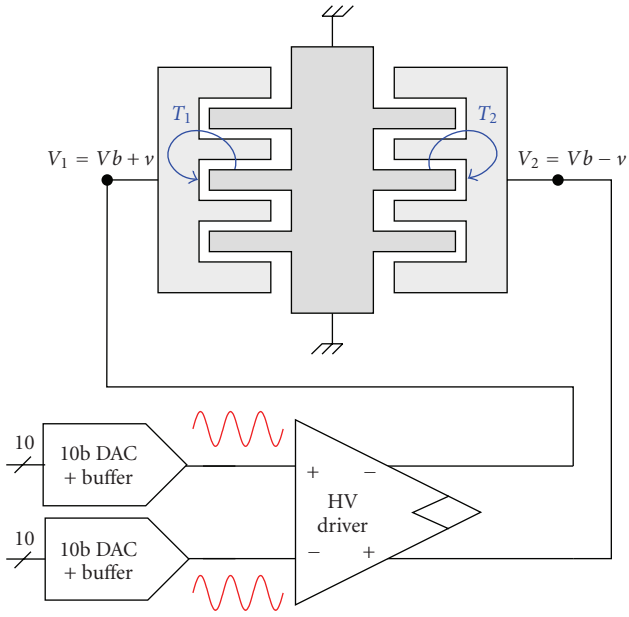


Figure 2: Innovative actuation scheme and architecture of the driving circuit.

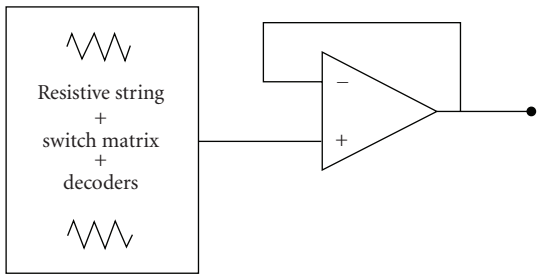


Figure 3: Overall architecture of the DAC.

fully differential amplifier. The input stage of the HV driver has a 1.8 V supply (being compliant with input signals up to 1,024 V coming from the 10-bit DAC) while the output stage is connected to the two fixed fingers of one axis and has a 25 V supply. The driver is characterized by a bandwidth higher than 1 MHz, a slew-rate higher than 2 V/μs, a total harmonic distortion (THD) lower than 10^{-3}, and from the DAC, it is seen as a load of 1 pF.

3. DAC Converter Design

3.1. DAC Architecture. For the DAC design, a resistor-string-based converter topology has been selected. By exploiting a folded string scheme, we were able to minimize both the converter's area and the effects of doping gradients. Besides, resistor-string DACs are intrinsically monotonic.

As showed in Figure 3 the overall DAC architecture is composed by a folded resistor-string core with switch matrix and address decoders plus a cascaded voltage buffer stage.

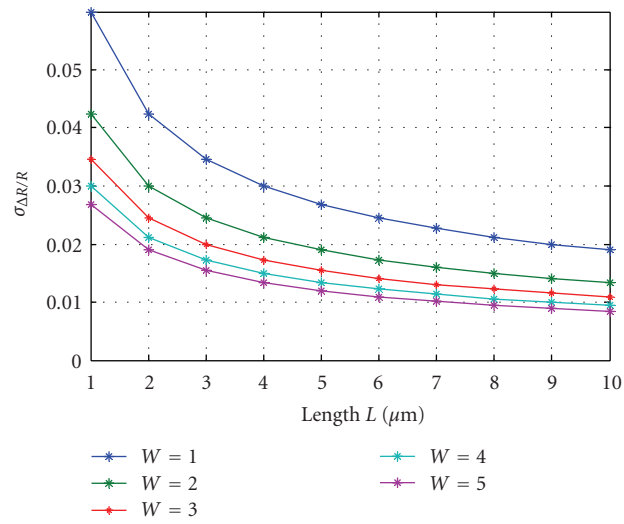
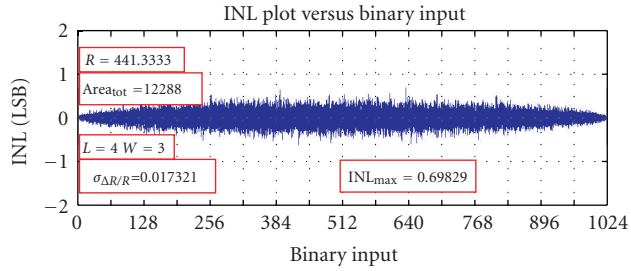


Figure 4: $\sigma_{\Delta R/R}$ value versus W and L.

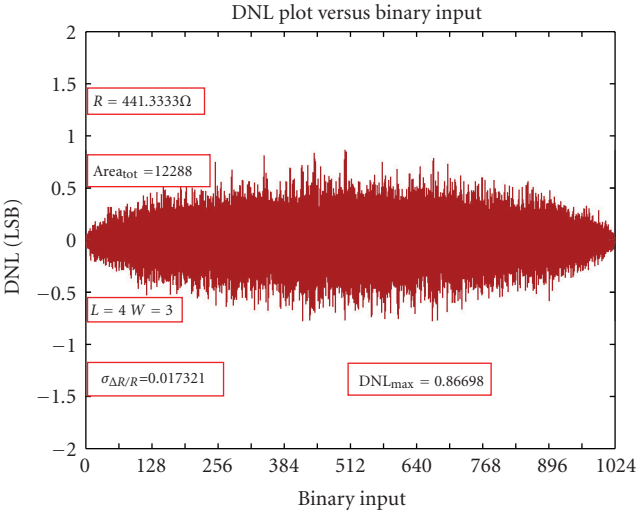
Indeed, the output voltage coming from the decoder has to be buffered before going to the HV driver. As a first step of the DAC design, we focused on the critical issue of sizing the resistors. The higher the resistor-string size (and hence the chip area), the lower the DAC nonlinearity. At the state of the art the resistor-string sizing is often done *a priori* or after comparisons by transistor-level simulations of few sizing alternatives, since transistor-level simulations are too time consuming. On the contrary, in this work we use a previously developed [14] high-level model of resistor-divider-based DACs, much faster than transistor-level simulations, to find a trade-off between good performances on nonlinearities (such as DNL and INL) and area occupation. As an example of the considered BCD technology and 10-bit resolution specifications Figure 4 shows how $\sigma_{\Delta R/R}$ (which is a resistor-string mismatch parameter directly proportional to DNL and INL) varies verus resistor size W and L. The plot, that depicts the behavior of $\sigma_{\Delta R/R}$ versus resistor length (L), is parametrized with W, the resistor width. Thus we can check from a graphical point of view which are the solutions, in our design space, providing a good trade-off between area occupation and linearity.

As a result of the design exploration based on the proprietary tool [9], considering target INL and DNL values below 1 LSB, polysilicon resistors have been used of dimensions of $L = 4\,\mu$m and $W = 3\,\mu$m with a resistance value of about $R = 550\,\Omega$ for each module. The total resistance of the 10-bit string is $R_{\text{tot}} = 550\,\Omega \cdot 1024 = 563.2\,\text{k}\Omega$. The static current flowing in the string is around 1.8 μA. Figure 5 shows the plots of DNL and INL obtained for the designed string-array. DNL and INL values lower than the target 1 LSB have been obtained.

3.2. Switch Matrix and Decoding Logic. As mentioned before the resistive string is folded and it features 8 rows, each one made of 128 resistors. To address all the nodes of the string



(a)



(b)

Figure 5: INL and DNL results.

starting from a 10-bit digital input, it is necessary to use a thermometric decoder.

The design of a thermometric decoder is a key issue to minimize area and power consumption. At the state of the art, for example, in [10, 12, 15], to reduce complexity in N-bit DACs, a single N-to-2^N decoder is split into two decoders M-to-2^M and H-to-2^H having $H + M = N$.

In our design, a new decoding architecture, more flexible and modular, has been used to further reduce decoding logic complexity. First of all, the single decoder is split into two groups of decoders (the other group for the rows, one group for the columns). The configuration described, with 8 rows of 128 resistors, would require a 3-to-2^3 decoder to select the row and a 7-to-2^7 decoder to select the column. However, a 7-to-2^7 decoder is still quite complex, so a further optimization has been adopted.

As shown in Figure 6 pass-gate switches to access the string nodes are alternatively disposed on the two sides of the string and they are connected to two buses, named EVEN and ODD. In this manner, even if there are physically 8 rows of resistors, there are virtually 16 output rows, each one made of 128 resistors. Each row is organized in 8 modules of 16 resistors.

Assuming $b0, b1, \ldots, b9$ as the digital input, where $b0$ is the least significant bit (LSB) and $b9$ is the most significant bit (MSB), we used $b1, \ldots, b7$ to address the columns and $b0$, $b7$, $b8$, $b9$ to address the rows. Since the resistors are placed in a folded way, each row has to be scanned towards the right and the left alternatively. To realize this alternation, we used the block *Dec_updown*, which receives $b7, b6, \ldots, b1$ as input. Depending on the value of $b7$ this block enables the scanning of the string in the two directions. The column decoders have a modular architecture, organized as follows: eight equal 3-to-2^3 decoders (*dec_321*) and one 3-to-2^3 decoder (*dec_1_of_8*), as outlined in Figure 7.

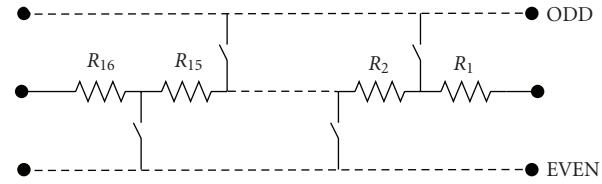


Figure 6: Schematic of a 16-resistor block with switches and output buses.

The *dec_321* logic drives the column switches directly, while the purpose of *dec_1_of_8* is to generate an enabling signal for one of the eight *dec_321* decoders. The whole digital logic circuitry has been implemented with the standard cells available in the technology library. Finally, the output decoder is used to activate one of the 16 output row buses. Through bits $b7$, $b8$, and $b9$, this logic block selects one of the eight EVEN/ODD bus couples then, using the least significant bit $b0$, one of the two buses is connected to the output node.

The proposed modular decoding circuitry ensures a reduction of the logic gates of a factor 36 versus a straigtforward solution adopting a single $N = 10$-bit decoder. With respect to the state-of-the-art solutions using two $N/2 = 5$-bit decoders (row/column), the proposed approach ensures a further complexity reduction of roughly 15%.

3.3. Converter Voltage Output Buffer Stage. The output voltage coming from the decoder has to be buffered before going to the HV driver in Figure 2. To this aim, we designed a voltage buffer capable of a very high-input impedance to not load the voltage divider, therefore performing a voltmetric measurement, and a low output impedance for properly driving the HV driver.

The initially proposed architecture was based on the state-of-the-art folded cascode amplifier topology with PMOS differential input pair. We chose PMOS transistors for the differential pair because we wanted an amplifier whose input range extends to the ground rail. Moreover, PMOS transistors are less noisy than NMOS. Since the supply voltage is only 1.8 Volt, we noticed transistor biasing issues in some PVT (process-voltage-temperature) corners of the considered BCD technology. The folded branch has 4 MOSFETs in series, which in typical conditions are correctly biased, but their bias point is hardly depending on process variations. To overcome this issue, the topology of the circuit has been modified versus the above state-of-art approach as shown in Figure 8. The folded structure has been maintained, but we substituted the cascode current mirror

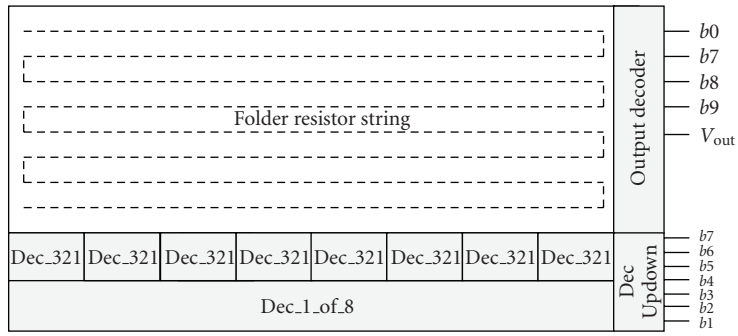


Figure 7: Block schematic of the designed D/A converter.

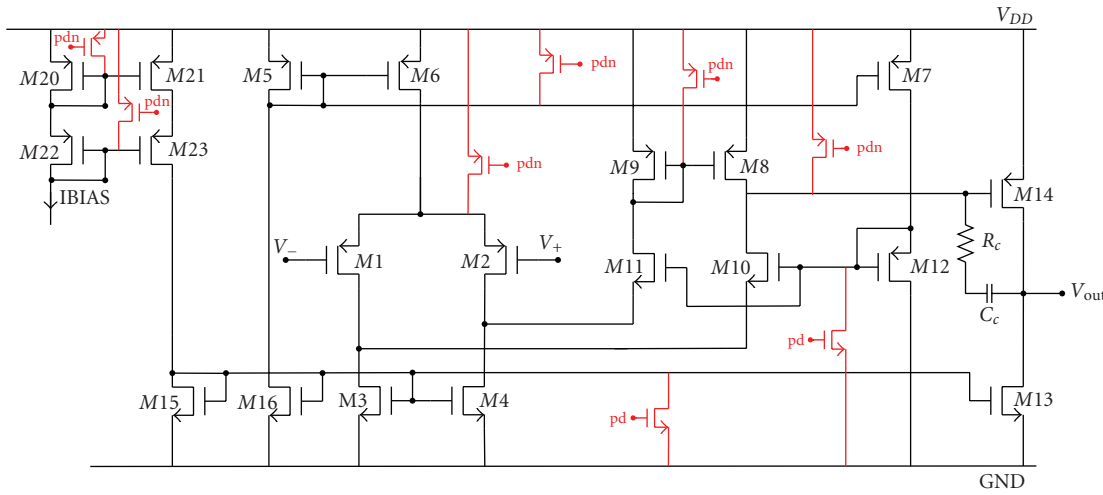


Figure 8: Output stage of the resistor-string DAC.

with a simple one. This way the robustness of the circuit to PVT variations in the considered BCD technology has been improved (almost eliminating biasing issues) at the price of losing some gain. To compensate this gain loss, a common source (CS) gain stage has been added, made by transistors $M13$ and $M14$, as depicted in Figure 8. A compensating network R_c-C_c has been also inserted to provide sufficient stability margins.

The sizing of the circuit has followed the design requirements coming from the application: gain-bandwidth product (GBP) higher than 300 kHz, open-loop DC gain higher than 70 dB, slew rate higher than 0.3 V/μs, supply voltage of 1.8 V ± 10%, power consumption below 200 μW, and phase margin of 60 degrees.

Table 1: Characteristics of the DAC considering MIN and MAX process conditions.

	Min	Max
Rout DC	1.7	4.4
Rout @ 30 kHz	1.5	4.8
PSRR (dB)	−115	−67
Slew rate	2.3 V/μs typical	
GBP (MHz)	1.69	2.96
INL (LSB)	—	0.7
DNL (LSB)	—	0.87

4. Implementation Results and Comparison to the State of the Art

The 10-bit resistor-string DAC plus the output voltage buffer has been first characterized by simulations with SPECTRE in CADENCE environment and then implemented in the 0.18 μm BCD technology. The converter has been tested on all device corners, in the temperature ranges −40 to 160°C. The results obtained from simulations and chip measurements confirm the correct operation of the converter whose DNL and INL are both below the 1 LSB original target. AC and DC measurements on the DAC converter are reported in Table 1 considering MIN and MAX process conditions.

The layout of the converter, shown in Figure 9, measures 550 μm × 220 μm for an area of 0.12 mm^2. The buffer stage has an area of 0.05 mm^2, and hence the whole circuit has an area of 0.17 mm^2. Particular care has been taken in the realization of the layout of resistors and the switch matrix.

Table 2: Comparative table of similar DAC architectures found in literature.

	Our	[15]	[16]	[17]	[18]	[19]	[20]
bit	10	10	8	10	16	8	12
Area, mm^2	0.12, 0.17 with buffer	0.25	N/A	0.18	4	0.28	0.25
Power	0.2 mW at 0.5 MSPS	0.054 mW, speed N/A	1 mW at 1 MSPS	0.5 mW at 2 MSPS	3.75 mW at 0.1 MSPS	0.34 mW/MSPS	0.54 mW, speed N/A
INL, LSB	<0.7	0.8	1.6	<2	<8 calibr. <29 not calibr.	0.6	<0.8
Tech., μm	0.18	0.18	0.18	0.13	0.5	0.13	0.18

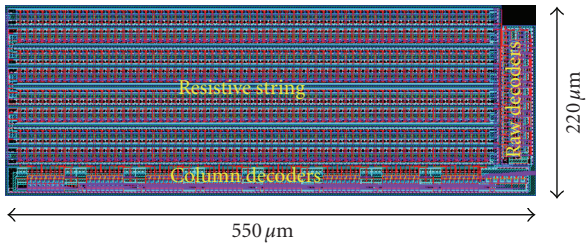


Figure 9: Layout of the converter.

Dummy structures have been extensively used to minimize the mismatches due to the fabrication process.

The power consumption of the DAC with a 1.8 V supply and working at 500 kHz amounts to roughly 200 μW; 45% are due to the folded string with the switch matrix and the decoders and 55% are due to the buffer output stage. The circuit can be put in power-down mode to reduce power consumption when the converter is not used: in idle mode the power consumption is reduced to roughly 2 μW. The power-down mode can be enabled by setting a bit in the digital part, pd in Figure 8 where pdn is not equivalent to (pd). This bit controls a set of CMOS switches (for example, those outlined in red in Figure 8 as far as the buffer amplifier is concerned) that short every important node of the circuit to power or ground rails. Then the consumption is due only to leakage current and to the current flowing in the resistor-string.

Table 2 shows a list of DACs recently presented in literature, targeting various technologies (4 DACs included our design are in a 0.18-μm technology node, 2 DACs are in a more recent 0.13-μm technology node while 1 DAC uses a 0.5-μm technology) and bit resolutions (from 8 to 16 bits). A comparison among the main parameters of the proposed DACs is reported. When compared to the state-of-the-art resistor-string converters our proposed DAC has comparable linearity performances, but it has the advantage of the smallest area occupation (mainly due to optimal resistor-string sizing and optimization of decoding logic) and low power cost.

5. Conclusion

The design of a 10-bit resistor-string DAC, which is part of an innovative MOEMS micromirror digital actuation scheme, to be integrated in laser projection video systems [21–24], has been presented in this work. The DAC, integrated in a 0.18-μm BCD technology, is composed of a first folded resistor-string stage with switch matrix and address decoders plus an output voltage buffer stage. When compared to the state-of-the-art resistor-string converters, realized in similar technologies, the proposed DAC has the advantage of the smallest area occupation (due to optimal resistor-string sizing and optimization of decoding logic) and comparable figures in terms of bit resolution, linearity, and power consumption. Power-down circuitry has been also implemented.

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