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MONOLITHIC READ-OUT ELECTRONICS FOR THE SILICON CALORIMETERS AT SSC/LHC COLLIDERS

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A very fast monolithic charge sensitive preamplifier using HF2CMOS technology featuring less than $45mW$ power dissipation for a $5V$ maximum output voltage swing, with a slew rate about $700V/\mu sec$ for $150pF$ input capacitance ($\approx$ $7nsec$ rise time), has been realized.

A front-end set up for the read out of more detectors and the shaping of the signal with a $20nsec$ RC-CR filter employing only monolithic preamplifiers is described and tested. The measured value of ENC (Electronic Noise Charge) for the arrangement with $150pF$ input capacitance is $17ke_{RMS}$.

The preamplifier meets the requirements for silicon calorimetry application for experiments at the hadron colliders SSC/LHC.

1. INTRODUCTION

New generation hadron colliders such as the super conducting supercollider (SSC in Texas) and the large hadron collider (LHC at CERN), which will yield multi-TeV proton beams, are expected to be built in the 1990s. The calorimeter of the central detection system will have to withstand the severe experimental conditions of those colliders: very high luminosity and high multiplicities. Therefore, it is required to have the following features: compact construction, fine segmentation, flexibility, fast charge collection, good energy resolution, ability to satisfy the conpensation condition ($e/\pi = 1$), easy calibration, and good radiation hardness.

A silicon calorimeter with silicon as active medium[1-3] is able to fulfil the above mentioned requirements.

2. READOUT APPROCH

The new machines at SSC/LHC experiments have as main features a very high number of channels and a high counting rate of the incoming events. The design for the readout is in this respect more complicated, not only speed and noise of the preamplifiers are to be taken into account, but also power dissipation and occupation area are as important as the former two.

The parasitic capacitance shunting the detector (capacitance in the range of $100 \div 200pF$), has to be kept low, otherwise it can affect the resolution considerably. For this reason the preamplifiers have to be located close to the detector. Since the number of channel is very large, every preamplifier must occupy a small area in order to satisfy this constraint. With such an arrangement, the total power dissipation has to be

kept low enough to avoid excessive heating of the calorimeter. Since the noise and the speed of the preamplifier improve with increasing power dissipation, a compromise between those variables must be found in order to get a suitable solution.

The counting rate of the incoming events in a SSC/LHC collider experiment is about $50MHz$, so that the shaping time of the preamplifier output signal must be very short. Because of the very short shaping time, the series noise of the preamplifier is the main source of noise which affect the resolution. The source of the series noise can be reduced by employing a bipolar devices as the input stage of the preamplifier, since this transistor has a large transconductance[4]. It also permits the use of high speed monolithic technology, which enables a minimum occupation area, with high capacitive matching when using bipolar transistor, like in our experimental application. While, in the low detector capacitance region and large shaping time, the JFET-CMOS tecnhology gives also good performances[5].

The dynamic range of the preamplifier output must be large, because of the range of the energy deposited in the silicon detector (0.1 to $500MeV$), so that linearity and speed characteristics have to be maintained for both small and large signals. A new process of bipolar-CMOS mixed technology, called HF2CMOS, developed by SGS-THOMSON Microelectronics, is able to satisfy the required specifications because of the very small dimensions of the integrated transistors and the low parasitic capacitance inside the monolithic chip.

3. TECHNOLOGY

The availability of mixed technology combining very high speed bipolar transistor with $2\mu m$ CMOS, allows to design a high speed, very high slew rate monolithic charge sensitive preamplifier.

By using this technology, named HF2 CMOS, it is possible to implement on the same silicon chip both bipolar transistor (*npn*, lateral *pnp*, vertical *pnp*, isolated collector vertical *pnp*) and CMOS devices well suited for both analog and digital applications.

The compactness due to the reduced space occupied by the basic structures and to a triple interconnecting level permits the implementation of extremelly complex systems including high precision analog circuits and a large number of logic functions (3000 MOS transistor/mm^2).

The CMOS is a p-well on an n epitaxial layer, with silicon gate and a minimum channel length of $2\mu m$, as represented in fig.1, where a p-channel and an n-channel transistor can be seen. The p-channel is grown directly on the epitaxial layer, while the n-channel device is realized on a p-well layer which is common to the top-bottom isolation zone. In the same picture, the classical *npn* bipolar transistor, is also presented. In fig.1, the deep n^+ collector diffusion, the p base and n^+ emitter steps are shown.

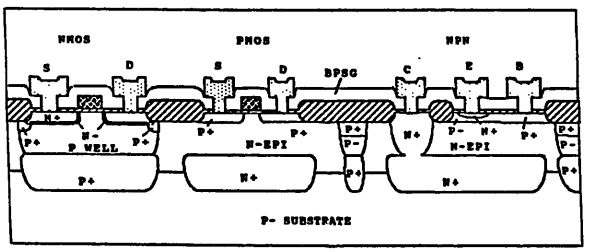

Fig.1
Cross section of transistors in the process HF2CMOS.

In the design of the charge preamplifier a p-type element is necessary for level shifting purpose. In this application, were a high slew rate is needed, his choice has the con-

straint of a low output capacitance. This limits the use of a *p*-MOS transistor rather than a *pnp* bipolar transistor due to the relatively high collector parasitic capacitance of the latter one[6].

The main features of the basic components used to realize the charge sensitive preamplifier, are a current gain, $h_{FE} \approx 100$ and a transition frequency, $f_T \geq 4GHz$ (fig.2), for the *npn* transistor and $5\mu m$ channel length for the *p*-MOS transistor (in order to have suitable current capability).

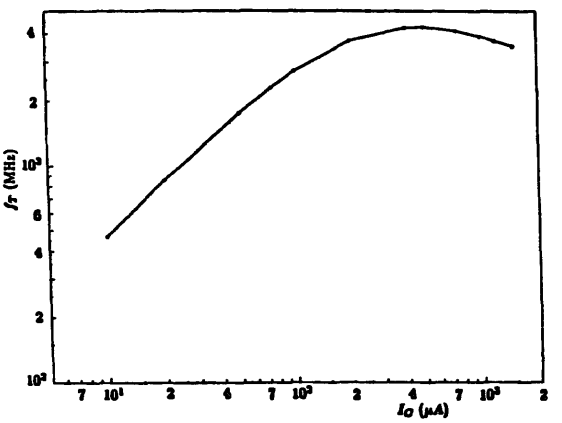

Fig.2
$f_T - I_C$ plot of the HF2CMOS *npn* transistor with $356\mu m^2$ area.

To design a radiation hard device for new collider experiments bipolar *npn*, *p*-channel and *n*-channel MOS transistor were irradiated, with a dose of 1.2 10^{12} $neutr/cm^2$.

The characterisics of such devices (available as individual structures), performed before and after irradiation, show that no significant change occured in the performance of *npn* and MOS transistors, since the damage in bipolar transistors is proportional to the inverse of the transition frequency ω_T, which is very large in the *npn* transistors of HF2CMOS process. MOS devices, especially *p*-MOS, are neutron radiation hard devices for their intrinsic structure[7].

4. CIRCUITS DESCRIPTION

A fast and high slew rate amplifier has low power consumption, if the transistors employed reach large values of their transition angular frequency ω_T at low standing current, and very low input and output capacitances. This occurs because ω_T is proportional to the biasing current and inversely proportional to the input capacitance, and the slew rate creases with the decrease of the capacitance shunting the high impedance nodes.

Fig.3 shows the used configuration. Q_1 is the input transistor whose dimensions depend upon the matching with the detector capacitance. Q_2 is the p-MOS transistor that cascodes Q_1, and is loaded with the current generator Q_4. Finally Q_3 is the output buffer, where the capacitive feedback is closed.

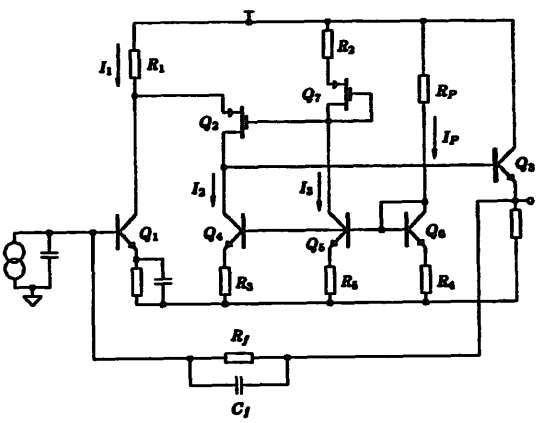

Fig.3
Charge sensitive preamplifier using a bipolar *npn* input transistor and a *p*-MOS cascode transistor.

The high speed in this amplifier is ob-

tained, since Q_1 has a very high transition frequency at low standing current (fig.2) and Q_2 has a little gate length. The high slew rate stems from the low value of the capacitance shunting the high impedance node at the Q_2 drain, as Q_2 and Q_4 have very small dimensions with, consequently, a negligible output parasitic capacitance.

In fig.3 the biasing network of the preamplifier is also shown. The resistor R_P, external to the chip, sets the biasing current I_P for Q_6. Since Q_4, Q_5 and Q_6 are equal, the ratios of resistors R_3 and R_5 to R_4 establish the biasing current of Q_2 and Q_7. By setting $Q_7 = Q_2$ it is easy to show that current I_1 is given by the ratio of resistors R_2 and R_1. For $R_3 = R_5 = R_4/10$ and $R_2 = 30R_1$, the biasing current of Q_2 and Q_4 is only 4% of the biasing current of Q_1. In this way, by setting a very little reference current through R_P, it is possible to set up the working points of the whole circuit. All the components, except R_P, are on the same chip. A high accuracy is obtained with this arrangement, since ratios of the components on the monolithic chip, have a precision of better than 1%.

In order to get the best compromise between speed, noise and power dissipation in the actual experimental setup, the biasing of the preamplifier can be thus modified (by means of R_P).

As will seen later, it is advantageous to have more amplifiers on a single integrated circuit. In this respect only one biasing network consisting of Q_5, Q_6, Q_7, R_2, R_4, R_5 and R_P is needed for every chip, saving in occupation area and current consumption.

A first integrated circuit version of the preamplifier has been realized[8]. With $3mA$ standing current for Q_1 the measured slew rate is larger than $700V/\mu sec$. In fig.4, a $5V$ preamplifier output voltage swing is shown, as a response to a simulated $312.5Me$ input charge corresponding to $1.125GeV$ particle energy. The feedback capacitance is $10pF$, the preamplifier input capacitance is $150pF$, simulating the detector impedance. The high speed required by the high rate of the incoming events is, therefore, well satisfied. With this bias condition and output range the power dissipation is less than $45mW$.

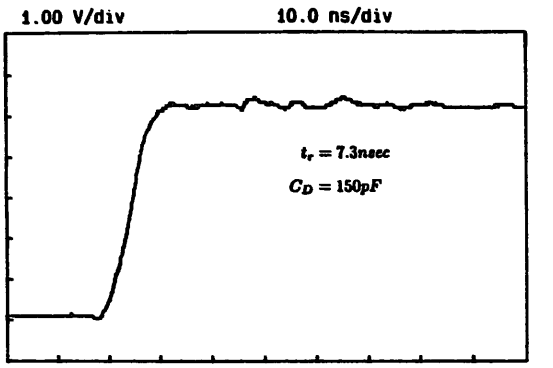

Fig.4
$5V$ output voltage swing for the monolithic preamplifier. The slew rate is about $700V/\mu sec$.

5. FRONT-END SET UP

The realized integrated preamplifier satisfies the dynamic requirements imposed by the future experiments at SSC/LHC machines. In the new version we are going to develop the matching with the detector impedance and the shaping of the signal will be implemented on a single chip.

In[8] the analysis of the matching condition has shown that with an input transistor 50 times larger than that now used it is possible to meet the typical actual detector capacitance of $150pF$ mantaining the same dynamic and static characteristic.

The calorimeter cell is composed of stacks

of 4 detectors having about $150pF$ capacitance each as proposed in the silicon calorimeter conceptual design for SSC[2]. Only one signal from every stack is necessary to reconstruct the electromagnetic or hadronic shower. Two solutions are available: to connect in parallel the detectors ($600pF$ of total capacitance) and then to read the signal with a preamplifier or to read the signal from every detector with a preamplifier making the sum of all preamplifier outputs.

The two solutions can be implemented as indicated in fig.5.

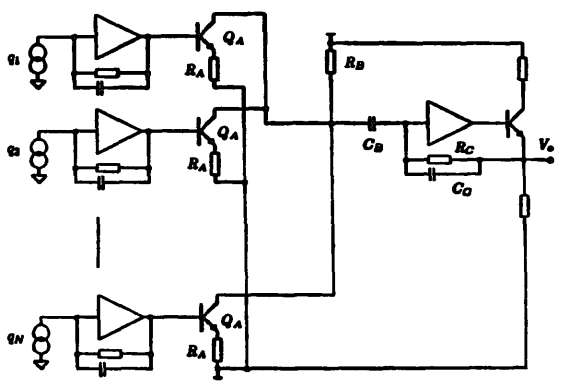

Fig.5
Front-end set up for the read out: the detectors signal in the stack are added and filtered by a RC-CR shaper at $20nsec$ peaking time. Every preamplifier is monolithic.

Suppose the stack is split into N detectors ($N \geq 1$); every detector signal is read by a preamplifier, whose output voltage is converted in a current by the Q_A's transistors and then added to each other. The resultant current is converted again to a voltage with the same polarity of the input preamplifier, by the output amplifier, where a loop network acts as a RC-CR shaper. All the amplifiers employed are of the same kind as in fig.3, the output amplifier, having as a final stage a Darlington, in order to drive a coaxial cable terminated at its ending point. By putting $\tau_M = R_B C_B = R_C C_C$ the output voltage of the shaper is given by[8]:

$$V_o(S) = \frac{S\tau_m}{(1+S\tau_M)^2} \sum_{i=1}^{N} \frac{Q_i}{SC_f}. \qquad (1)$$

The whole arrangement is to be monolithically integrated. A printed board has been realized (fig.6 shows the output signal of the whole circuit when $\tau_M = 20nsec$).

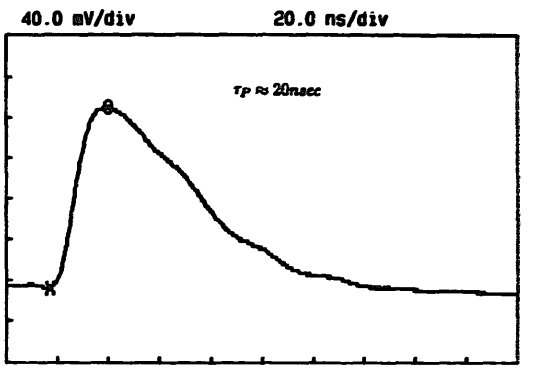

Fig.6
Output signal of the network of fig.5. The peaking time is at $20nsec$.

The resolution in ENC (Electronic Noise Charge) of the above acquisition chain is given by (in RMS electron):

$$ENC(e_{RMS}) = \frac{exp(1)}{2q}\sqrt{N}\left\{ \frac{(\frac{C_{DT}}{N} + C_f + C_B)^2 \overline{e_T^2} + (\frac{C_{DT}}{N} + C_f)^2 \overline{e_{BB'}^2}}{2\tau_M} + \right.$$
$$\left. + \frac{\tau_M}{2}\left(\frac{\overline{i_D^2}}{N} + \overline{i_B^2} + \overline{i_f^2}\right)\right\}^{1/2} \qquad (2)$$

Here, C_B is the preamplifier input capacitance, while C_{DT} is the stack detector capacitance, N is the number parts in which the stack is divided. $\overline{e_T^2} = 4KT0.5/g_m$ and $\overline{e_{BB'}^2} = 4KTR_{BB'}$ are, respectively, the collector and the base spreading resistance thermal series noise of the input device; the parallel noise is contributed by the shot noise of the detector and of the input current of the preamplifier ($\overline{i_D^2}(\overline{i_B^2}) = 2qI_{D(B)}$), and the thermal noise of the feedback resistor ($\overline{i_f^2} = 4KT/R_f$). τ_M is the shaping time of the filter.

By varying the input capacitance C_{DT} when $N = 1$ it is possible to evaluate the series input noise from the slope of ENC versus C_{DT} plot of fig.7. Taking into account that $g_m = 115mA/V$, if the input device standing current is $3mA$ and $\tau_M = 20nsec$, one can extract for $R_{BB'}$ a value less than 370Ω for the realized preamplifier.

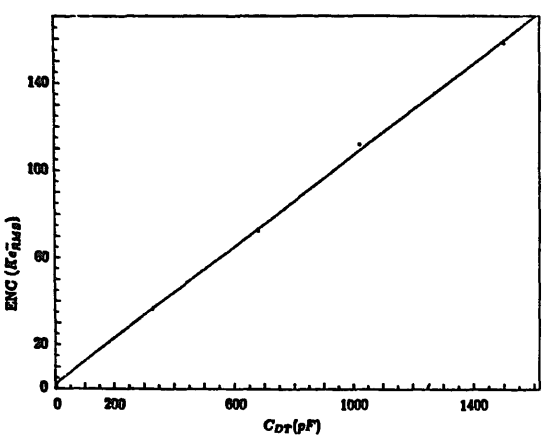

Fig.7
Measured ENC(e_{RMS}) as a function of the input capacitance C_{DT} with the RC-CR filter of fig.5 at $20nsec$.

This corresponds to a resolution of $17ke_{RMS}$ at $C_D = 150pF$: Future version will obtain $R_{BB'} \approx 7\Omega$ which means $4ke_{RMS}$ resolution with the same condition.

It can be seen in eq.(2) that the split of the stack has an optimum value N_{OPT} since for $N \gg 0$ or $N \to 0$ the resolution gets larger and larger values. By differentiating eq.(2) in respect to N the resulting N_{OPT} is:

$$N_{OPT} = \left[\frac{\frac{1}{2\tau_M}(\overline{e_T^2} + \overline{e_{BB'}^2})C_{DT}^2}{\frac{(C_f+C_B)^2\overline{e_T^2}+C_f^2\overline{e_{BB'}^2}}{2\tau_M} + \frac{\tau_M}{2}(\overline{i_B^2} + \overline{i_f^2})} \right]^{1/2} \quad (3)$$

independent of the detector leakage current I_D.

Eq.(3) has an interesting physical interpretation: N_{OPT} fulfill the condition in which the whole preamplifier noise, asymptotic to N in eq.(2), equals the series noise, asymptotic to $1/N$ in eq.(2).

For the new version of the preamplifier eq.(3) gives a N_{OPT} so that the stack must be split into 4 detectors having $150pF$ each one ($C_B = 19pF$, $I_B = 30\mu A$ and $R_f = 100k\Omega$). These were found for a design which must take into account mathing with $150pF$. The resolution is 44% better than the read out with a single preamplifier with the same features, namely $ENC = 8ke_{RMS}$ for the whole stack. If an evaluation of the matching of a single preamplifier to a detector of $600pF$ capacitance be made, the result should be very similar (less than 4% difference) to that obtained above both for the resolution and power dissipation. This is important because the above arrangement which we intend to develop is easier to realize from the technological point of view.

For the actual version of the preamplifier $ENC \approx 32ke_{RMS}$.

Finally, we observe that the use of a small shaping time is advantageous for the parallel noise of the detector leakage current. In fact, the contribution to ENC given only by

I_D, rises only at large values of current if τ_M is as low as $20nsec$. As an example a contribution to ENC of $15ke_{RMS}$ is given by a leakage current of $1mA$, which is out of the range of the detectors employed.

6. CONCLUSIONS

A very fast monolithic charge sensitive preamplifier, using HF2CMOS technology, has been realized.

The overall power consumption is less than 45 mW for a $5V$ maximum output voltage swing, with a slew rate of about $700V/\mu sec$ for $150pF$ input capacitance ($\approx 7nsec$ rise time for $5V$ output swing).

A new acquisition chain where signal, delivered from several detectors, are summed and an RC-CR shaping of $20nsec$ is used is realized, employing monolithic preamplifier only. It was succesfully tested in view of future experimental application. This way, the measured value of ENC for a $150pF$ detector capacitance is $17ke_{RMS}$.

In the next monolithic version the whole network will be integrated, and the input device will have an area of 50 times larger than the present one in order to reduce the ENC to about $4ke_{RMS}$ under the same static and dynamic conditions.

The preamplifier meets the requirements for silicon calorimetry applications for experiments at the hadron colliders SSC/LHC.

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