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Room temperature differential voltage sensitive preamplifier for large mass bolometric detectors

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Abstract

The present version of the very front-end preamplifier which readouts an array of 20 large mass TeO_2 bolometric detectors is reported. It operates at room temperature and has low series and parallel noise. The thermal drift has been maintained at negligible levels thanks to a correcting circuit especially designed for this purpose.

1. Introduction

In the Underground Laboratory of Gran Sasso an array composed of 20 TeO_2 bolometric detectors, having a mass of 340 g each, is running [1]. The very front-end preamplifiers which readout these bolometers are differential voltage sensitive preamplifiers (DVP), designed to operate at room temperature with low series and parallel noise. The differential configuration for the signal readout allows minimizing microphonism of the connecting wires and cross-talk of adjacent channels, since both problems show up in the form of signals having common mode origin.

Large mass bolometers have a very small signal bandwidth, of a few Hz. The readout system must be DC coupled to the detector to exploit on the information contained in the signal. Any drift of the front-end is therefore a source of low-frequency noise that may impair the energy resolution.

The detector energy response is correlated with the base temperature fluctuations. One very efficient way of correcting this deficit is to correlate the detector baseline to the signal amplitude. Of course this procedure is efficient only if there is a negligible contribution coming from the front-end preamplifier.

In the following sections we will describe our preamplifier solution to the above requirements. The experimental results will also be shown.

2. The differential voltage sensitive preamplifier (DVP)

2.1. The biasing of the input JFETS

The DVP, subject of this contribution, is a simplified and more efficient new version of the preamplifier described in Ref. [2]. The circuit solution is shown in Fig. 1. The preamplifier has at the input a pair of low-noise silicon JFET, Q_1 and Q_2, biased

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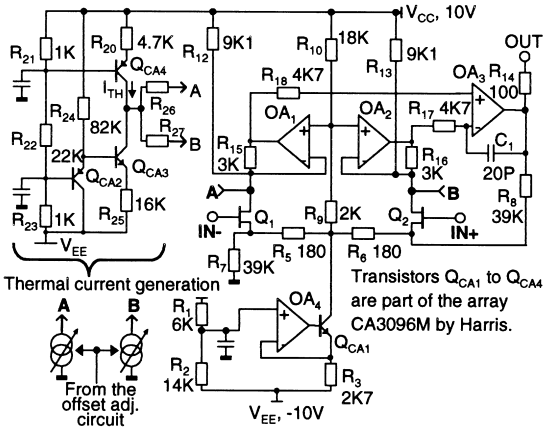

Fig. 1. Schematic circuit of the differential voltage sensitive preamplifier.

to minimize their noise contribution, as described in the following.

Parallel noise is proportional to the input current of Q_1 and Q_2, which depends on the amplitude of the reverse voltage present between the gate and the channel, which forms a pn junction. A small electrical field applied to the channel minimizes the input current. This task can be obtained following two steps. By optimization of circuit design the biasing of the drain to source voltage of the JFETs, V_{DS}, can be chosen the minimum which assures the device to operate in saturation region, in order to obtain the right dynamic behavior. Once the drain current is fixed, the source voltage is smaller for the devices having small pinch-off voltage, V_P (V_P is the gate to source voltage, V_{GS}, for which the drain current is nulled).

The origin of the gate current, I_{GS}, seems largely contributed also by the effects of the intensity of the electric field applied (impact ionization) and on the doping concentration level, to which V_P is proportional, in addition to the Generation Recombination, G–R current. The G–R current is proportional to the width of the depletion region [3]. It is possible to calculate its contribution by taking into account that the depletion region varies along the channel profile, when the JFET is connected to the circuit. Using the gradual channel approximation [4] and considering the device at the onset of the saturation region, after some mathematical manipulations, we have

$$I_{GS} = I_{G0}t\left\{1 - \frac{1}{6}\left(\frac{V_P}{V_P - V_{bi}}\right)\left(1 - \frac{V_{GS}}{V_P}\right)\right\}. \quad (1)$$

In Eq. (1) $I_{G0}t$ (t being the thickness of the device) is the leakage current of G–R type when the channel is totally depleted, and the source and the drain are shorted together, emulating the case of a uniform depletion set along the channel profile. The effect of the bias, drain and source at different potential, is taken into account in the term inside the brackets, where V_{bi} is the intrinsic build-in voltage. From Eq. (1) it is evident that the maximum saving in G–R current is obtained when the terms inside the two round parenthesis (always ≤ 1, consider that $V_P < 0$) are both close to unity. The saving of current obtainable in this condition is only 16%, with respect to the case in which the channel is totally depleted. Consequently, being limited by the total depletion of the channel, this current depends only slightly on any further increase of V_{DS}. This behavior is not observed in practice and I_{GS} depends on both V_P and V_{DS}. One practical example is given by the JFETs we have selected to fulfill our technological requirements: the pair Toshiba 2SK146, that has a pinch-off voltage having an absolute value of about 0.5 V, and the equivalent pair Interfet IFN146 with a larger V_P (0.8 V). Fig. 2 shows the measured leakage current of one of the two gates of a 2SK146 and one of the two gates of the IFN146

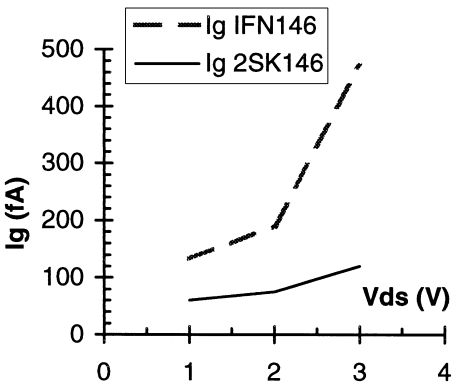

Fig. 2. Leakage current as a function of the drain to source voltage for the Interfet IFN146, dashed line, and the Toshiba 2SK146, solid line.

as a function of V_{DS}, when each device pair is connected as input device of the DVP. It can be seen that both JFETs have low leakage current, somewhat larger for the IFN146 than for the 2SK146, as expected from the larger value of V_P. But both the leakage currents are dependent on the amplitude of V_{DS}, confirming a non-G–R origin for them. The comparison made in Fig. 2 is consistent, as the two devices are made with similar technological processes.

2.2. Preamplifier circuit configuration and results

The JFET input devices Q_1 and Q_2 have their V_{DS} fixed to about 0.8 V thanks to the cascode connection realized with the two Operational Amplifiers, OA, OA_1 and OA_2, see Fig. 1. The reference voltage for the two OAs is taken at the virtual ground present at the common node of R_5 and R_6. The voltage drop V_{DS} of the JFETs results in this way independent of the common mode input voltage. The bias current for Q_1 and Q_2 is determined for each to be about 1 mA by the current generator formed with OA_4 and transistor Q_{CA1}. Another OA, OA_3, is used to convert the double-ended signal at the outputs of OA_1 and OA_2 to a single ended one. The feedback of the structure is taken from the output of OA_3 to the source of Q_2. The feedback network is formed with the four resistors R_5 to R_8. The gain is given by $1 + R_8/R_6$ (≈ 218). The overall DC offset can be adjusted by adding suitable currents at nodes A and B. In our front-end implementation the offset is adjusted firing an automatic circuit [5].

As mentioned in the introduction, an important requirement for the preamplifier is to have a very low drift. The intrinsic drift is not small, mainly due to the JFETs. Our approach to compensate the drift was not based on the selection of temperature-matched JFETs, a very time-consuming solution, but in trying to compensate the intrinsic drift by adding in certain nodes an ad hoc current, designed for having a known thermal behavior. In the first version of our preamplifier, a proportional to absolute temperature current, PTAT current, has been derived from a commercial temperature to voltage transducer integrated circuit. In this version the PTAT current is generated from a dedicated circuit obtained from a monolithic array of low noise, matched, bipolar transistors, (CA3096M by Harris). The new solution minimizes any possible noise contribution, otherwise obtainable only by the use of very large value low pass filtering capacitances. The realized circuit is very simple and is shown in the section indicated by the horizontal bracket in Fig. 1. It is based on the fact that the base to emitter voltage of a bipolar transistor, a pn junction, is linearly dependent on temperature, with a slope of about 2 mV/°C. Transistor Q_{CA4}, having the base at a fixed potential, and resistor R_{20} exploit this fact and generate the thermal current I_{TH}, of about 400 nA/°C. Transistor Q_{CA2} and Q_{CA3} generate a constant, temperature independent, current that equals the bias current of Q_{CA4}. As a consequence the DC current which may flow trough R_{26} and R_{27} has a negligible value, while the thermal current shared by the resistors is I_{TH}. This current is injected into the nodes A and B, the cascode nodes, which have the same potential. By proper selection of the ratio of R_{26} and R_{27} a thermal current, having a suitable value, can be added or subtracted from the output, correcting the original drift. The maximum DVP input drift that can be compensated in this way is about $\pm 100\,\mu V/°C$.

The selection of resistors R_{26} and R_{27} is made after having measured the intrinsic drift of the preamplifier inside a climatic room. So far the results obtained are very good. The intrinsic drift recorded from 45 preamplifiers, part of them having at the input the IFN146, the others the 2SK146, had an average value of 18.7 μV/°C, with a standard deviation of 28.1 μV/°C. After correction application, the average drift obtained on the 45 samples has become only 0.2 μV/°C, with a standard deviation of 0.14 μV/°C, Fig. 3. The correcting method allows therefore to reduce the drift even a factor of hundred.

The series noise of the DVP is about 30 $nV/\sqrt{Hz}$ at 0.1 Hz and 7 $nV/\sqrt{Hz}$ at 1 Hz. To save the amount of current needed for offset compensation, relatively large value feedback resistors have been used, R_5 and R_6 in Fig. 1, which limit the white noise to be about 3 $nV/\sqrt{Hz}$. This noise level does not affect the detector performance since the detector bandwidth is only a few Hz. The series noise

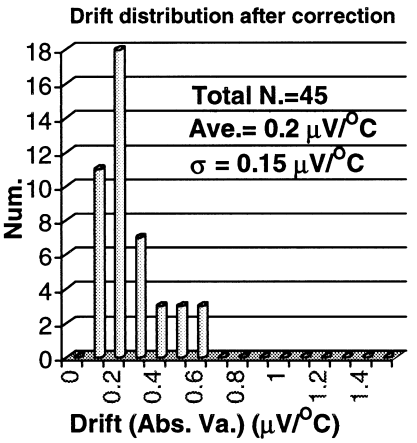

Fig. 3. Drift distribution after drift compensation for 45 preamplifiers.

at low frequency is quite similar for both cases, in which the 2SK146 or IFN146 are used as input devices. The parallel noise is given by $\sqrt{[2(2qI_{GS})]}$, and is about 0.2 fA/$\sqrt{\text{Hz}}$ for the Toshiba 2SK146, becoming 0.3 fA/$\sqrt{\text{Hz}}$ for the Interfet IFN146.

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