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Daedalus: a hardware signal analyser for Icarus

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Abstract

Icarus detector [1] is a large-volume (400 cm) liquid Argon TPC that requires continuous high rate sampling signal recording on each channel (about 50 000) to produce event images quite similar to the ones from bubble chambers. In order to optimize the memory usage, a signal feature extractor, that commands memory writing only upon signal detection, has been designed in VLSI CMOS.

1. Daedalus chip

The signals from a set of 16 channels are converted by a single 40 MHz ADC (10 bit), after passing a 16-to-1 analog multiplexer. Each channel is then sampled every 400 ns. A set of four adjacent channels is processed by a Daedalus chip that implements a feature extraction scheme already proven to be very efficient on the data from the 3 ton Icarus prototype module [2,3].

Typical signals are voltage steps rising in few microseconds and with a much slower decay (about 100 μs); feature extraction is based on the recognition of the rising edge, using a time-sliding window strategy. The differences between every two consecutive signal samples are computed inside this time window: positive values are accumulated while negative and zero values are counted. When the window overlaps a rising edge, the positive sum increases while the negative and zero values keep low. The slope is recognized looking at the threshold conditions on sum value and on negative and zero counts. Edge detection is stated for every channel through a *hit-found* output signal and Daedalus also gives a filtered output containing only the edge shape.

In order to reduce high-frequency noise, a median filter is first applied to the input signal. In Fig. 1 an Icarus collection signal and the related filtered output are shown.

The VLSI has been realized in 0.7 μm CMOS technology, on a 4.4 mm × 4.4 mm silicon area and it works up to 50 MHz. Its architecture is pipelined at $\frac{1}{16}$ of the external clock frequency. The chip features many programmable operating parameters: median filter order (up to 15 samples), time window size (up to 15 samples) and all the thresholds. Latency depends on the median filter order and on the time window size chosen and it ranges from 2.8 to 14 μs. Daedalus chip is fully testable and it has a fault coverage around 100%.

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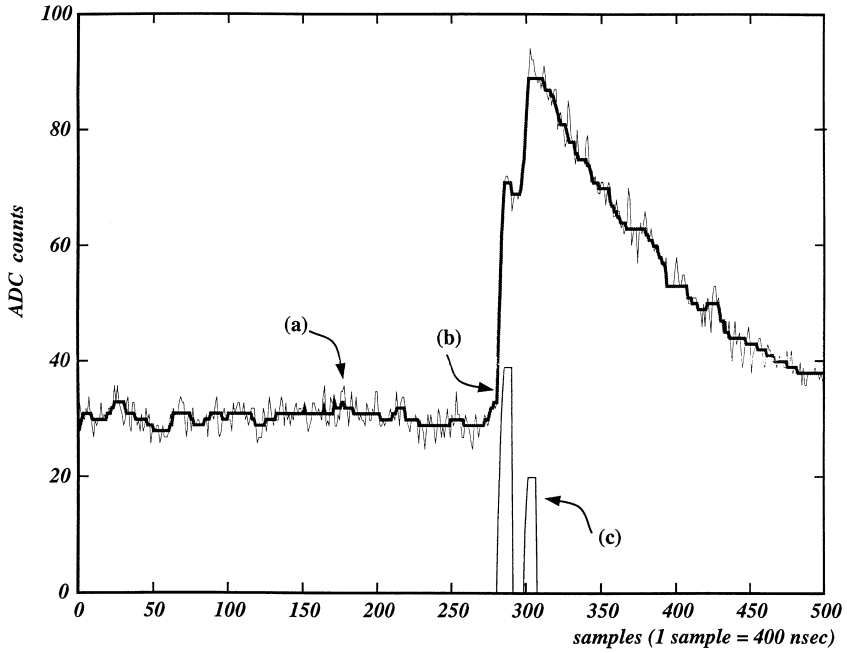

Fig. 1. Icarus collection signal before (a) and after (b) median filtering; Daedalus filtered output (c).

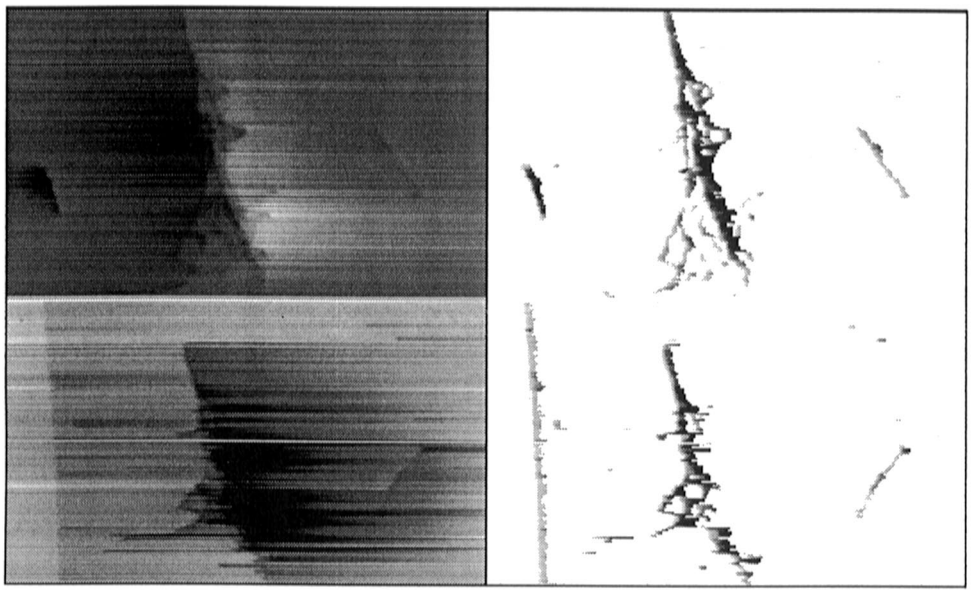

Fig. 2. Collection and induction image of an Icarus event before (left) and after (right) filtering.

2. Readout module

A 16 channel readout module prototype has been designed and built in VME standard [4]. Four Daedalus chips have been connected together sharing the same data buses (in/out) to serve the 16 channels; a SYNC signal keeps synchronization between the outer analog multiplexing and the digital demultiplexing realized inside the Daedalus chips.

Each channel has a 8 Kbyte dual port memory that records the signal profile when Daedalus recognizes an *interesting* feature. The memory is organized in programmable length circular buffers (from 128 up to 8 Kbytes per channel) that can be read through VME bus while data are being recorded.

In Fig. 2 a set from some 128 collection and 128 induction signals is shown in the raw form (more dark grey corresponds to higher signals) and after Daedalus filtering, where reconstructed tracks are evident.

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