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A new electronic read-out for the YAPPET scanner

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Abstract

A small animal PET-SPECT scanner (YAPPET) prototype was built at the Physics Department of the Ferrara University and is presently being used at the Nuclear Medicine Department for radiopharmaceutical studies on rats. The first YAPPET prototype shows very good performances, but needs some improvements before it can be fully used for intensive radiopharmaceutical research. The main problem of the actual prototype is its heavy electronics, based on NIM and CAMAC standard modules. For this reason a new, compact read-out electronics was developed and tested. The results of a first series of tests made on the first prototype will be presented in the paper. © 2002 Published by Elsevier Science B.V.

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Keywords: Small animal PET; Read-out; TDC

1. Introduction

The YAPPET scanner, a small animal positron emission tomograph, has been recently built at Ferrara University. A complete set of studies on the first YAPPET prototype and its performances has been published [1]. Preliminary studies on rats have been already reported [2]. During the last year, the scanner was equipped to be used also as a SPECT scanner [3,4] and it is actually used as Single Photon Emission Tomograph at the Nuclear Medicine Department of the University of Ferrara for studies of new Radiofarmaceuticals on rats. The experimental results obtained with the first YAPPET prototype were encouraging and convinced us to study further improvements for the scanner so as to make it easier its transport and use by medical doctors and biology researchers. The main problem with the use of the first YAPPET prototype is the read-out and data acquisition system, which is made of standard NIM and CAMAC modules and it is too heavy to transport and unfriendly to use. For this reason, a new electronic read-out was designed, realized and tested in collaboration with the Electronic Group of Ferrara Branch of the National Institute of Nuclear Physics (INFN). The basic project and the first preliminary test measurement on the new

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YAPPET read-out electronics will be presented in this paper.

2. The new electronic read-out for the YAPPET scanner

The YAPPET tomograph is made of two pairs of opposite detectors mounted on a rotating gantry. Each single detector is made of a matrix of 400 YAP:Ce finger crystals (dimensions $2 \times 2 \times 30\ mm^3$ each) coupled to position sensitive photomultipliers Hamamatsu R2486-06. Each finger YAP:Ce crystal is optically insulated from adjacent ones by a thin reflective layer and the same type of coating is deposited on the back of each crystal, so that light generated by a 511 keV photon interaction in a finger crystal is collected at the side coupled to the photomultiplier window. The position sensitive photomultiplier has an intrinsic spatial resolution of about 0.5 mm for 2000 *photon* signals (511 keV photon interaction in a YAP:Ce $2 \times 2 \times 30\ mm^3$ finger crystal) and can recognise the position of the illuminated crystal. Each pair of opposite detectors is in coincidence and can be positioned at a distance ranging from 10 to 25 cm allowing both high spatial resolution (1.6 mm radial FWHM, 2.0 mm tangential FWHM and 1.8 mm axial FWHM) and high sensitivity (640 cps/μCi at centre). A description of the actual YAPPET read-out system can be found in [1].

The basic observation which suggested the new YAPPET electronic read-out is the fact that a time measurement is necessary together with charge measurements. The time difference between signals coming from the two PMTs of each pair has to be measured for rejecting noise due to random coincidences. In the actual YAPPET electronic read-out the time difference between coupled PMT signals is converted to a voltage value and measured by a peak sensing ADC. This is the standard technique used in small animal PET scanners which use PSPMTs for position measurements [5–7]. In this new project, we convert all charge signals to a time gate, whose length is proportional to the input charge, and we measure all time signals with a time to digital converter (TDC). TDCs are commonly used in high-energy physics [8,9] and industry being a powerful link between the analog world of the physical quantities and the digital world of todays electronics. In our application, the advantages of this new approach are a direct measurement of the time difference between the coincidence signals and the use of digital instead of analog signals holding position and energy informations from the front end electronics placed on the scanner gantry, to the data acquisition system, which can be placed few meters far from the scanner.

The schematic diagram of the new electronic read-out is shown in Fig. 1 for one pair of opposite detectors. Each PMT last dynode output is sent to a first amplification stage and then to a constant fraction discriminator (CFD in Fig. 1) which starts a 10–15 ns long digital signal which is used to start acquisition. The constant fraction discriminator is

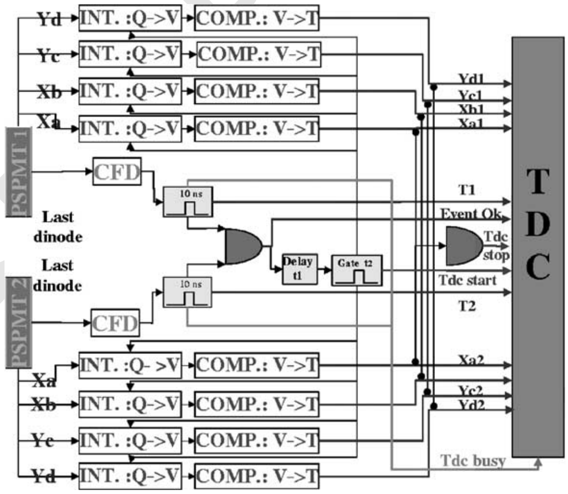

Fig. 1. Schematic diagram of the new YAPPET read-out electronics for a pair of position sensitive photomultiplier tubes (PSPMT). Anodic signals (Xa, Xb, Yc, Yd) are sent to a processing circuit which first integrates the signals transforming the charge information in voltage information ($Q- > V$), and than transforms, using a comparator, the voltage information in a time window ($V- > T$), whose length is proportional to the input charge signal (see text for details). Dynode signals are sent to a pair of constant fraction discriminators (CFD) which generate two 10 ns long signals used to detect the coincidence event (AND gate in the diagram) and to start the acquisition. All time windows are sent to the time to digital converter (TDC) to be digitized.

realized with the following procedure. First of all the last dynode output is inverted and amplified by a two-stage amplifier with a total gain of about 120. The amplifier output signal is sent to a second processing stage in which the signal is splitted in two. The first of the two resulting signals is delayed by 10 ns; the second signal is inverted and attenuated by a factor 3. After that the two signals are summed. The resulting signal is a bipolar pulse which is finally sent to a comparator with variable threshold. In this way, we obtain two results: we have an output signal only if the input signal is greater than a variable threshold and the position of the second edge of the output signal is fixed with respect to the starting time of the signal, as can be seen in Fig. 2.

The second edge of the comparator output signal has two main functions: the first one is to give the synchronisation time for the integration of the PMT anodic signals, the second one is to start a fixed length (15 ns) pulse which is used by the control logic to generate the trigger of the acquisition system. As far as the anodic signal processing is concerned, R2486-06 Hamamatsu amplification board is used in this first prototype to integrate and amplify the four PMT position signals. Each of the four PMT outputs is integrated for a small time window over the signal peak charging a 150 pF capacitor. When the integration window is finished the charged capacitor begins to discharge until a reference voltage level is reached (see Fig. 3) and a time window is generated during the discharge whose length results to be proportional to the initial voltage across the capacitor and to the anodic signal amplitude (see Fig. 4). The four resulting time windows for each PMT are sent to a 32 channel time to digital converting system to be measured.

The main component of the read-out control logic is a programmable Field Programmable Gate Array (FPGA) which has several tasks. The main FPGA function is to start the acquisition system once the correct logic requirements are achieved by the two 15 ns wide signals that come from the last dynode signal processing of the PMT pair. Trigger conditions can be decided by changing a triple switch among the following possibilities:

(1) coincidence (logical *AND*) of the dynode signals;
(2) exclusive *OR* of the dynode signals;
(3) first PMT signal alone;

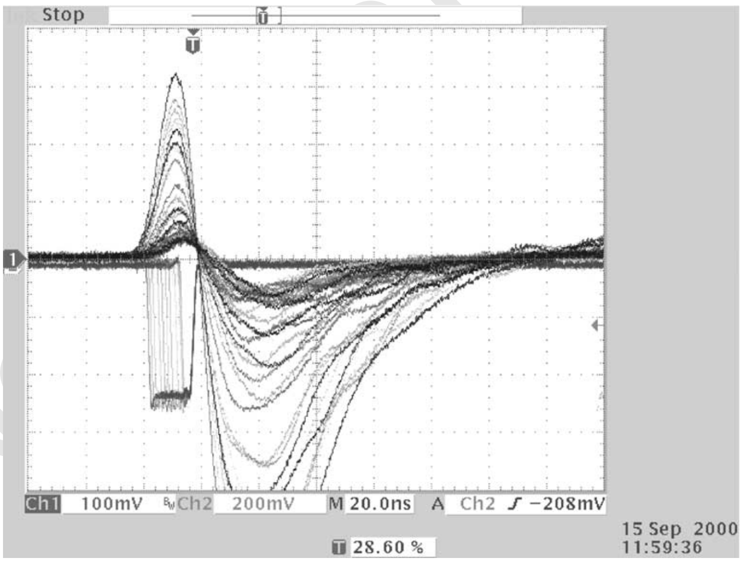

Fig. 2. Bipolar pulse obtained by the amplified and splitted last dynode output and gate generated after the comparator which gives the start to the trigger logic.

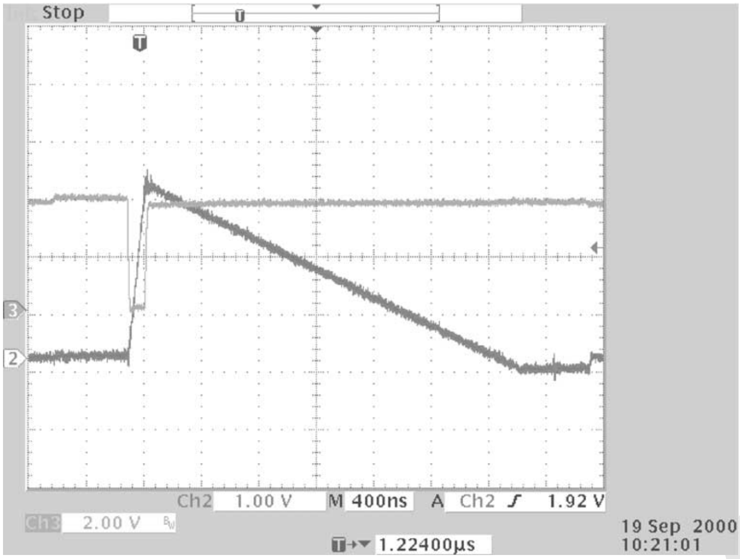

Fig. 3. Integration gate over anodic signal peak and capacitor charge–discharge signal that allows voltage to time conversion.

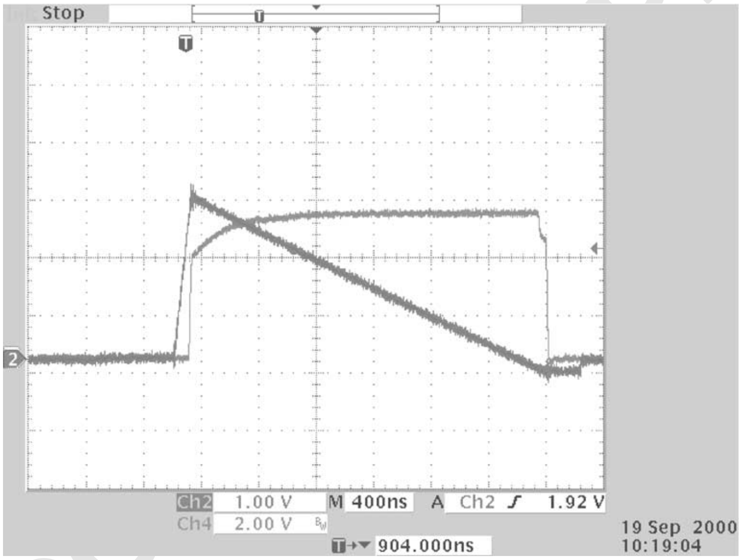

Fig. 4. Capacitor charge–discharge signal and time window generated during the discharge phase. The length of the time window is proportional to the corresponding anodic signal peak. This time signal is sent to the time to digital converter after a TTL to ECL conversion.

(4) second PMT signal alone;
(5) coincidence between the first dynode signal and the second dynode signal, delayed by a fixed time;
(6) external trigger signal;
(7) internal test pulse generation.

These possibilities allow a wide range of functionalities: the read-out can work in PET logic (case 1), or in SPECT logic (case 2); the two PMTs can be tested alone (case 3 and 4); the amount of random coincidences can be estimated with the delayed coincidence method (case 5); the logic can be tested without PMT signals (case 6) and finally electronic pedestals can be measured by generating an internal gate (case 7). The FPGA also decides the error conditions of the logic and resets all the read-out system if an "end of conversion signal" is not generated after a fixed time (5 μs) and sends to the time to digital converting system the signal which starts the conversion. This signal is a time window which starts when the anodic capacitors begin their discharge and stops when all the anodic discharge signals reach the threshold level. Together with the eight anodic signals coming from the detector pair other time signals are sent to the TDC system. The most important ones are last dynode 15 ns wide signals from which the coincidence time can be measured and other important signals are the time window used to detect delayed coincidences (if the logic is enabled to generate a delayed coincidence window) and a signal generated if an error condition took place. The time to digital converting system we used in these preliminary measurements is a TDC chip mounted on a test VME board developed by KLOE collaboration to be used for high energy experiment purposes [10].

3. New YAPPET read-out prototype test results

Up to now, two prototypes of the new YAPPET electronics have been built and tested. The first one was a completely home made board. It had several noise and cross talk problems, but showed the feasibility of the project. The second prototype was an improved version of the first one. Noise and cross talk problems were almost completely eliminated and an FPGA was added to allow the use of a more sophisticated control logic. In this section, the results of a complete series of tests made on the second YAPPET electronic prototype (see Figs. 5 and 6) will be presented. We tested the electronics in standard PET mode, using a point-like ^{22}Na source in between two detectors; we tested one single detector using a ^{57}Co source, to study the electronics performances at low energy; we made a series of count rate studies on a single detector with and without the acquisition chain (TDC and VME bus).

PET mode tests: We used two detectors placed one in front of the other about 50 cm apart. One detector was equipped with a $4 \times 4 \times 3$ cm^3 YAP:Ce matrix (400 $2 \times 2 \times 30$ mm^3 finger crystals) and the second one with a $1 \times 1 \times 3$ cm^3 YAP:Ce matrix (25 $2 \times 2 \times 30$ mm^3 finger crys-

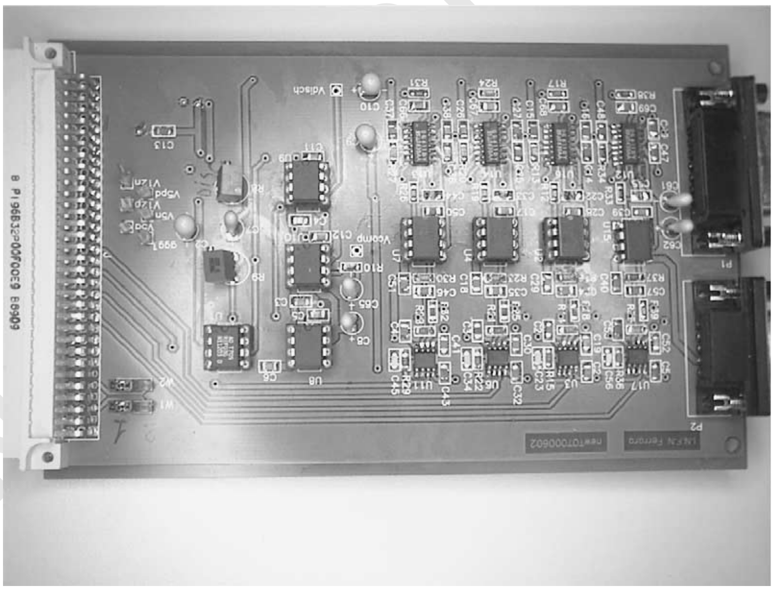

Fig. 5. Photograph of the board used for the processing of the anodic signals of one R2486 PSPMT.

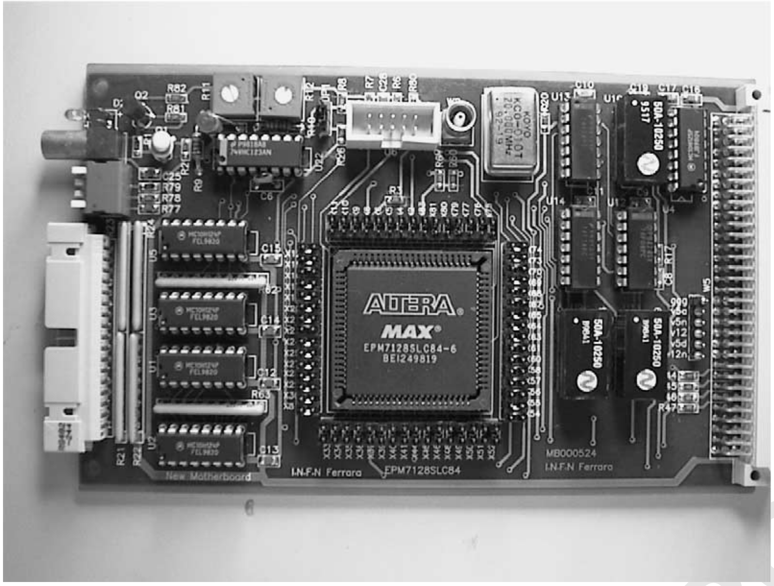

Fig. 6. Photograph of the mother board of the electronic read-out. The Altera FPGA can be seen at the centre of the picture.

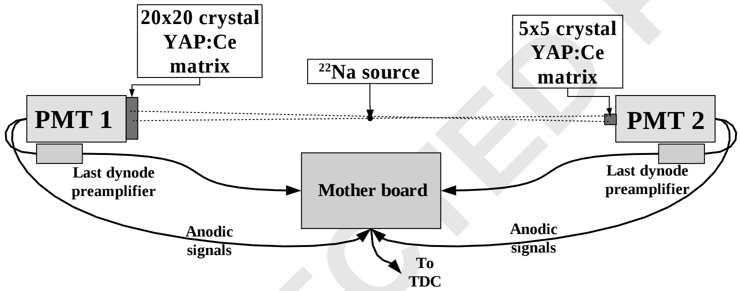

Fig. 7. Schematic diagram of the experimental set up used to test the new YAPPET electronic read-out in PET mode (coincidence of the two opposite detectors).

tals). A point-like ^{22}Na source was placed at about 20 cm from the 5×5 matrix. The trigger to the acquisition system was given by the logical *AND* of the last dynode signals of the two PSPMTs. In Fig. 8, the image of the 5×5 matrix as obtained on the PSPMT with this set up is shown. Each single $2 \times 2 \times 30$ mm^3 finger crystal can be clearly distinguished in the image. In Fig. 9, the energy spectrum of the same detector is shown: the photo-peak is placed at about channel 1800 of the TDC and Compton contribution extends almost constant from about channel 1200 to the electronic threshold, that can be estimated at about 50 keV. The distribution of time differences between the signals from the two detectors is shown in Fig. 10. The time spectrum has a FWHM of about 1.5 ns. The binning of the spectrum is limited by the TDC resolution (1 ns/channel); anyways it should allow the rejection of random events with a time difference between the coincidence signals >4 or 5 ns.

Single detector acquisition mode: We acquired a set of data with the same set up as shown in Fig. 7, using a ^{57}Co source, emitting a 122 keV photon, and the trigger to the acquisition system was started by the signal of one detector. This test is

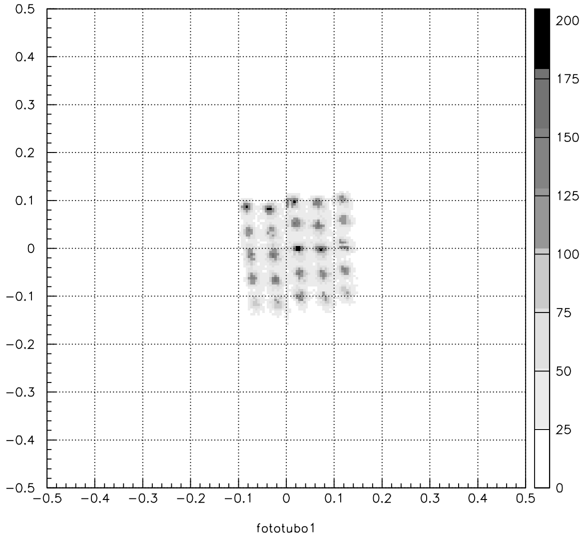

Fig. 8. Image of the 5 × 5 matrix on the PSPMT obtained with the set up shown in Fig. 7 used in coincidence mode and with a ^{22}Na source.

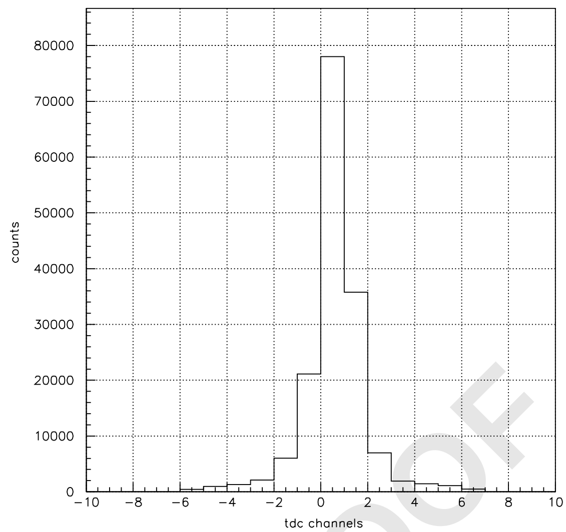

Fig. 10. Distribution of the time differences between the signals of the two detectors. The FWHM of the distribution is about 1.5 ns. The measurement was done with the set up shown in Fig. 7.

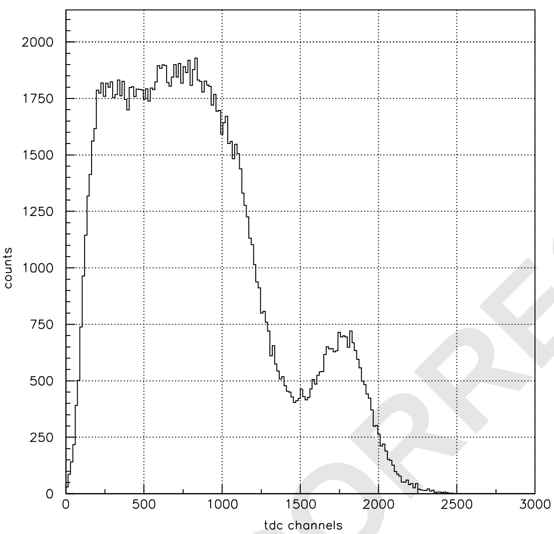

Fig. 9. Energy spectrum of 511 keV photons interacting in the 5 × 5 matrix obtained with the set up shown in Fig. 7. Electronic threshold is set at 50 keV.

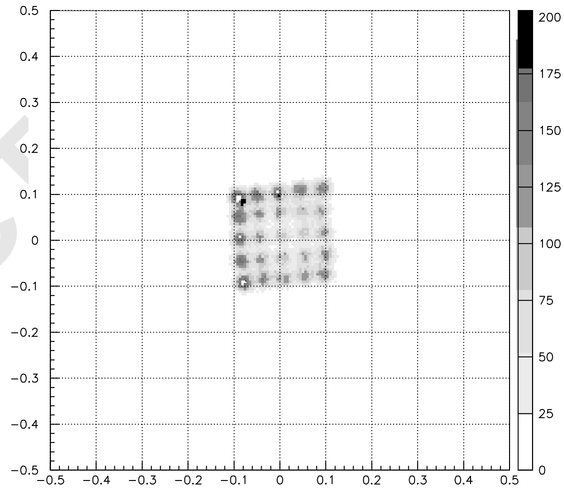

Fig. 11. Image of the 5 × 5 matrix on the PSPMT obtained with the set up shown in 7 used in single detector mode and with a ^{57}Co source.

important because it allows to verify the performance of the system at low energy and in SPECT mode. The results of the measurement are shown in Figs. 11 and 12. Each single crystal of the matrix can be distinguished in the image of Fig. 11. The energy spectrum is acceptable too, even if a better detector shielding should be used when working with detectors in SPECT mode, to eliminate the tail at very low energy due to background noise.

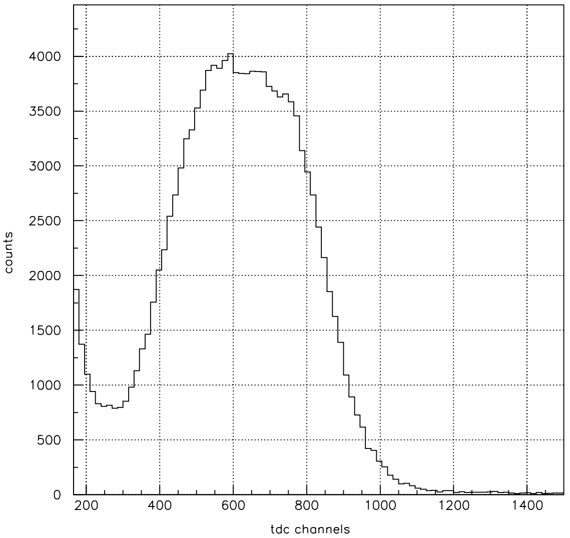

Fig. 12. Energy spectrum of 122 keV (^{57}Co photons interacting in the 5×5 matrix obtained with the set up shown in Fig. 7 used in single detector mode). Electronic threshold was set to 20 keV.

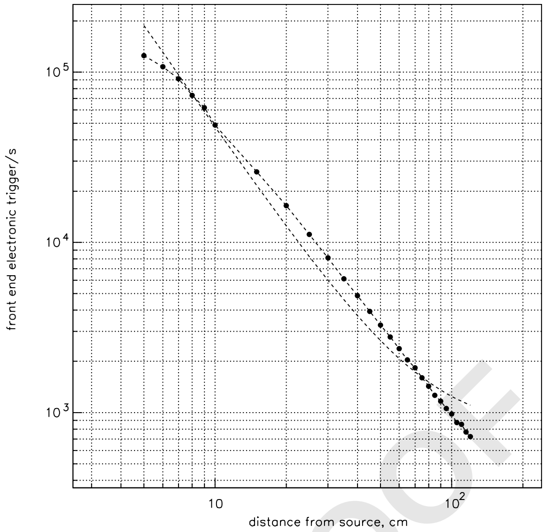

Fig. 13. Number of triggers generated by the front end electronics as a function of the distance of the ^{57}Co source from the detector. The expected $1/d^2$ behaviour is shown by the dashed line. The discrepancy is due to source-detector alignment inaccuracies.

The peak due to electronic noise can be seen in the spectrum because the threshold was set to a very low value (20 keV).

Rate performance study: We used a ^{57}Co source and the electronic read-out in single detector acquisition mode to study the rate performance. The detector was equipped with a $6 \times 6 \times 3$ cm^3 YAP:Ce matrix (900 finger crystals), which was slightly greater than the PSPMT photocathode window. We changed the system count rate modifying the distance of the source from the detector. In Fig. 13 the number of the front end electronic triggers as a function of source distance d from detector is shown. The dependence should be proportional to $1/d^2$ in the case of a pointlike source placed on the detector axis. The experimental curve deviates a little from the $1/d^2$ dependence due to alignment inaccuracies. The maximum count rate of the front end electronics (fixed by the FPGA 5 μs anodic signal time out) reaches the maximum signal rate of the PSPMT (about 10^5 count/s).

We repeated the same measurement, moving the source along the detector axis, and recording the time necessary to the acquisition system to process an event. We distinguished the time necessary to read all data on the VME bus and to recognise good events from the time necessary to write all data on disk. In Fig. 14, the number of events per second detected by the acquisition system (TDC and VME bus) as a function of the number of triggers per second of the electronic read-out is shown. The time spent to write data on disk is not included in the measurement. The behaviour is linear up to 20 kcnt/s and the saturation rate is about 30 kcnt/s. In Fig. 15, the number of events per second detected by the acquisition system (TDC and VME bus) as a function of the number of triggers per second of the electronic read-out is shown when the time spent to write data on disk is included in the measurement. The behaviour is linear up to 3 kcnt/s and the saturation rate is about 8 kcnt/s which is the same obtained with the actual YAPPET electronics. Our aim is to improve these numbers. At the moment the more critical point is the access to disk and an improvement is possible with some parallelization of the processes. The second critical point, the access to the TDC and to VME bus, can be improved with a better

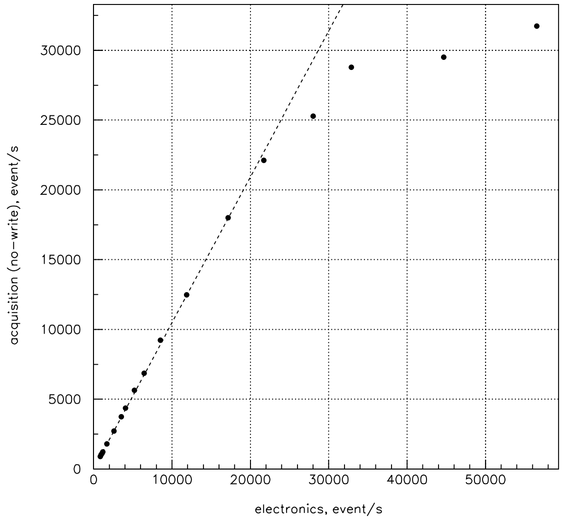

Fig. 14. Number of events per second detected by the acquisition system as a function of the number of triggers per second of the electronic read-out. The time spent to record data on the hard disk is *not* included. The straight line shows the ideal behaviour.

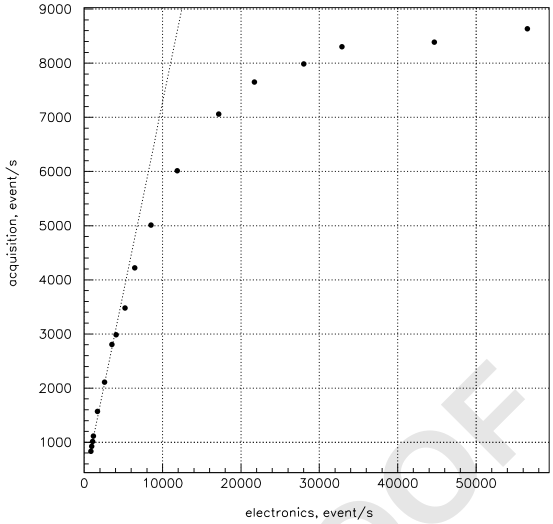

Fig. 15. Number of events per second detected by the acquisition system as a function of the number of triggers per second of the electronic read-out. The time spent to record data on the hard disk is included. The straight line shows the ideal behaviour.

design of the TDC board and with the use of a faster CPU.[1]

4. Further improvements

The main goal to reach now is the read-out rate performance enhancement. At present a critical point is the VME bus and the CPU used as crate master. Many solutions are possible to fix the problem. The first one could be the development of a dedicated PCI board for the KLOE TDC chip to be controlled by an acquisition PC. The second possible solution could be the use of other general purpose TDC chips. At present, we are testing the TDC-F1 chip, developed by ACAM[2] on behalf of and in collaboration with the Faculty of Physics of the University of Freiburg, Germany. The F1 [11] is a general purpose, commercially available TDC chip, and can be sold together with a dedicated read-out board which can host up to four chips and requires a very simple digital acquisition interface to be programmed and read-out. The possibility of using the F1 chip with our PET electronic read-out is presently under study.

5. Conclusions

The project of a new read-out electronics for the YAPPET scanner and a complete set of tests on the first realized prototype were presented. The new read-out satisfies the compactness needs and showed to reach the performances of the actual YAPPET electronics. Furthermore, possible improvements are expected.

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[1] At the moment we are using a PowerPC 601 CPU on a Cetia VMTR2 board placed directly on the VME bus.

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