Proposal for a new ALICE CPV-HMPID Front-end Electronics Topology

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***Abstract*— This paper presents the proposal of a new front-end readout electronics (RO) architecture for the ALICE Charged-particle Veto detector (CPV) located in PHOton Spectrometer (PHOS), and for the High Momentum particle IDentification detector (HMPID). With the upgrades in hardware typology and proposed new readout scheme in FPGA design, the RO system shall achieve at least five times the speed of the present front-end readout electronics. Design choices such as using the ALTERA Cyclone V GX FPGA, the topology for parallel readout of Dilogic cards and an upgrade in FPGA design interfaces will enable the RO electronics to reach an approximate interaction rate of 50 kHz. This paper presents the new system hardware as well as the preliminary prototype measurement results. This paper concludes with recommendations for other future planned updates in hardware schema.**

Keywords*— *Front-end electronics for detector readout Introduction, interaction rate, FPGA, CPV, HMPID, ALICE.

I. Introduction

The project CPV-HMPID at a readout rate of 50 kHz was set up to provide a new RO electronics able to cope with Pb-Pb 50 kHz collision rate provided by LHC. A setup based on the parallel RO of all Dilogic chips is proposed in this work and preliminary results for a developed prototype are presented in this paper. The CPV detector [1] and the HMPID modules are based on multiwire proportional chambers (MWPC) with cathode pad readout. The electronics scheme consists of a charge-sensitive preamplifier with a shaping time of more than 800ns, analog charge measurements, and multiplexed operation. The CPV electronics design is based on the HMPID electronics which satisfies the present ALICE interaction rate requirement of 10 kHz and 100 kHz in the ion and proton collider modes respectively. Using Detector Data Link version one (DDL1) protocol, the recorded pattern, after the on-line trigger selection is transferred to the experiment data acquisition system (DAQ) for event building over a 2.125 Gb/s full duplex, multipurpose optical fiber link. To fulfil such requirements two dedicated ASIC devices are used: Gassiplex for analogue signal processing and Dilogic for handling the digital information. Each column is made out of 10 Gassiplex cards, called 3-GAS cards directly connected on the backside of the MWPC cathode. A specific customized board called 5-DIL is accommodating five channels of 12-bit ADC and Dilogic-3. Two 5-DIL cards are required to process the signal from a column of 480 pads. A set of FPGAs are used to generate the required control signals, providing the necessary interface to the DAQ experiment and Trigger systems.

During Run3 of the Large Hadron collider (LHC) at CERN the sub-detectors in ALICE will be grouped in the continuous and triggered read-out mode detectors. CPV and HMPID belong to the second group where the trigger L2 latency, of approximately 108 µs, will be eliminated. This work focuses on upgrading the RO FPGA firmware and hardware electronics for the Dilogic and Column Controller cards respectively shown in Fig. 1 and Fig. 2.

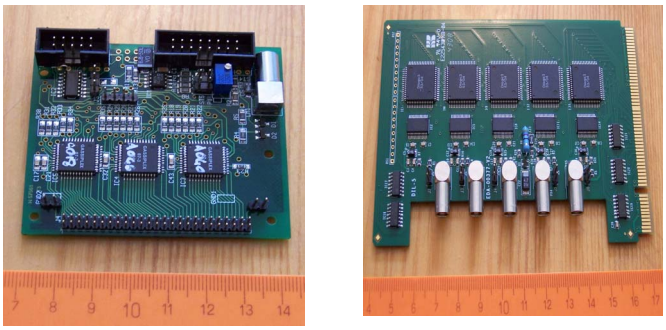

Fig. 1. 3-GAS (left) and 5-DIL (right) cards.

Fig. 2. Column Controller Card.

II. Technical Limitations

Three levels of triggers, L0, L1 and L2, are used for the reduction of overall dataflow and the selection of events in the ALICE experiment. L0, L1 and L2 are required to arrive at the front end electronics at 1.2 µs, 6.5 µs, and 88 µs respectively after the collisions take place [2, 3]. The busy time is the

period from the arrival of the L0 trigger to the end of the transmission of an event data. Therefore, it includes the waiting time of a L2 trigger (about 108 µs) and the transmission time depending on the number of words. The busy time conditions the event rate and it decreases with the number of transmitted words. In fact, in the data block that the RO electronics sends to the DAQ, there is a fixed part and another of variable length adding up to 1280 bytes in total.

The fixed part consists of headers and markers:

- CDH (10 words, 40 bytes);
- CPV header (5 words, 20 bytes);
- Column headers (24 words, 96 bytes);
- DILOGIC markers (240 words, 960 bytes);
- Segment markers (3 words, 12 bytes).

The present maximum event rate which the detector can reach is about 10 kHz, when the detector occupancy is around 1% and including the L2 latency (the busy time is minimum [4]. Therefore because of the ALICE upgrade strategy based on collecting >10 nb^{-1} of Pb-Pb collisions at luminosities up to $L = 6x10^{27}$ $cm^{-2}s^{-1}$ corresponding to collision rates of 50 kHz, a new architecture for the front-end read-out electronics is being proposed in this paper and described in the following sections.

III. Proposed New Architecture Upgrade

The proposed architecture includes the re-design of the interface between Dilogic cards and column controller, use of new FPGA 28nm Cyclone V GX technologies with 3.125 Gb/s transceiver full duplex serial links, and the re-design of firmware for continuous read-out trigger.

Any detector is segmented in sub-parts (modules, partitions, etc) with a finite number of channels. Taking the CPV as an example, it is based on three independent modules with two DDL version two (DDL2) interfaces running at 5.3125 Gb/s each per module. Fig.3 shows a module consisting of two segments, where every segment consists of eight columns with an FPGA column controller per column, ten Dilogic chips per column and 480 channels per column in total, 3840 channels per segment.

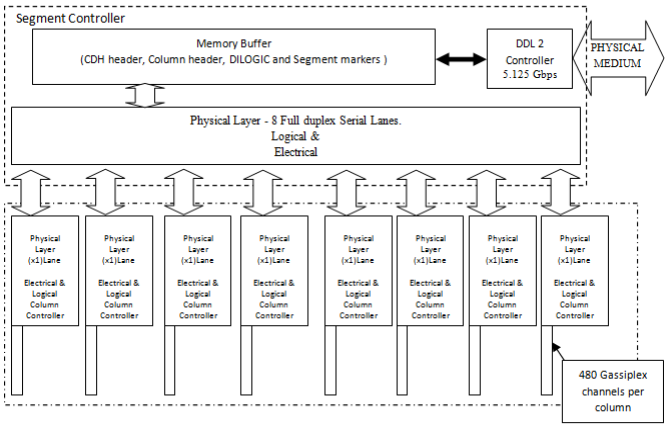

Fig. 3. CPV detector new partitioning scheme for one segment.

The schema implements VHDL for both segment and column controllers on the Cyclone V GX FPGA technology. The selection of FPGA was based on a trade-off between cost and performance.

In the present system, the sequential analogue readout from the daisy chained Dilogic chips, performed after arrival of asynchronous L1 message trigger done by FPGA column controller, is estimated to take 100µs depending on Dilogic clock readout frequency ranging between 5 MHz and 20 MHz. To reach an event readout rate of 50 kHz, the Dilogic card analogue pattern readout time must be reduced drastically.

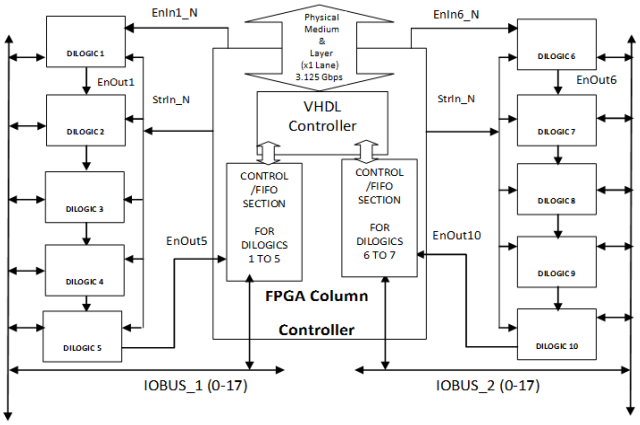

Fig. 4. Layout topology for Column Controller.

Therefore parallel readout of DILOGIC chips can be performed simultaneously. Reading all ten DILOGIC chips could lead to many copper traces on PCB thus contributing to trace resistance and degrading effects. This is due to the fact that each Dilogic has an 18-bit digital Bus. Additionally, a bigger FPGA footprint and also the re-design of Dilogic PCB boards, would be required leading an increase in implementation costs for such an upgrade. Therefore a second approach considered, is to have independent IOBUS data buses and a VHDL controller for the two groups of 5 DILOGIC chips, each as shown in Fig. 4. This approach can be implemented on the current available Dilogic cards without including extra cost to manufacture Dilogic PCB boards. With this architecture, the transfer of data through IOBUS_1 and IOBUS_2, can be done simultaneously.

The digitised amplitude information (12-bits) and address of selected channel will be stored in two different FIFO buffers (256 x18-bit words per buffer) each containing raw data from the each respective column. A VHDL controller scans both FIFO buffers and transmits serially the collected data to the segment controller using a full duplex serial link running at an estimated lane speed rate in a single direction of 3.125 Gb/s.

IV. Implementation Status

The hardware prototype shown in Fig. 5, provides the parallel readout for two 5-DILOGIC cards in one column controller. The Segment controller implements VHDL logic for DDL2 protocol and the data transfer from memory buffer to DAQ experiment for event logging using fiber optic

medium. The estimate of read-out rate calculations for the simultaneous read-out of two 5-Dilogic cards described in Table 1, is done for a Dilogic clock frequency of 7.5 MHz and an occupancy of 15% (72 channels) per column.

	Estimated Transfer Time (us)
Analogue readout by Gassiplex	5
Parallel Readout of all DILOGIC	11.2
Parallel Readout of all Columns	3
Estimated Transfer time to DAQ using DDL2	8
Estimated Total Write Transfer Time	27.2

TABLE I. ESTIMATE READ-OUT RATE FOR PARALLEL RO OF TWO 5-DILOGIC CARDS

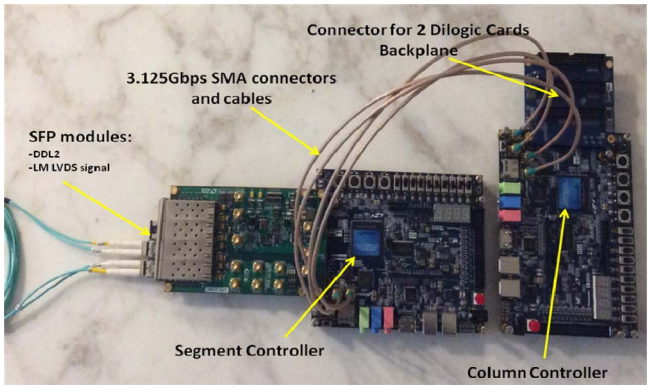

Fig. 5. Prototype Implementation of CPV detector front-end read-out electronics.

VHDL implementation for data transfer between column and segment controller is shown in Fig. 6. Two 100 MHz internal FPGA PLL clocks drive FPGA logic, while a reference clock of 156.25 MHz is necessary for clocking the 3.125 Gb/s serial full duplex transceivers implemented using Altera PHY IP core. FPGA logic transmits and receives 32-bit parallel data words to and from both transceivers respectively.

Segment controller includes the implementation of the standard DDL2 Source Interface Unit (SIU) necessary for the event data transmission to DAQ experiment recorders [4]. ALICE DDL has been designed to address all the requirements for data transfer between the detectors and the ALICE Data Acquisition system.

The maximum DLL version 2 data rate is 5.125 Gb/s full duplex, through a multipurpose optical fiber link having enough bandwidth for the prototype DDL2 transceiver to allow the bi-directional transmission of data between the front-end electronics and the data acquisition system during data taking. During the start of each run, it is possible to send configuration control messages to the detector using the opposite communication channel.

The critical part in the DDL protocol is the implementation of the SERDES. ALTERA delivers strong and flexible solutions in their FPGA to access the high speed serial links. Delay lines and synchronization FIFOs are necessary and they have to be inserted between the user logic and the SERDES, for both receiving and transmitting channels.

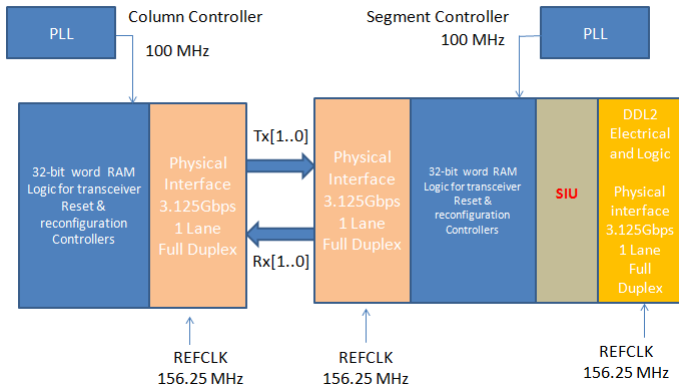

Fig. 6. VHDL Implementation for data transfer between column and segment controllers, and SIU to data acquisition system via DDL2 protocol.

V. INITIAL MEASUREMENT RESULTS

The following measurement results were obtained using Altera Signal Tap 2 embedded Logic Analyzer and a 1 GHz digital oscilloscope.

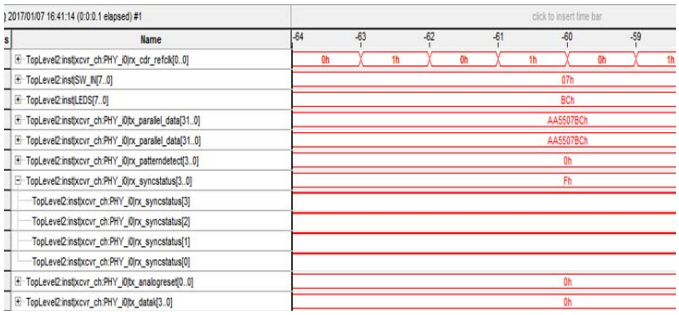

Fig. 7. Timing diagram for data transfer between column and segment controllers, obtained using Altera Signal Tap 2 Embedded Logic Analyzer.

The transfer of a 32-bit data word between column and segment controllers shown in Fig.7, has been tested in a stable way at 3.125 Gb/s. The timing diagram shown in Fig.8, shows a total transfer time of 20.2µs for 8192 bytes of data. For an occupancy of 15%, the equipment will have a total of 1280 bytes, therefore leading to a transfer time of around 3.2µs slightly higher than expected (3µs) estimated value shown in Table 1 concerning the parallel read-out of all columns. The slight overhead may be related to the firmware.
The initial measurement results for data transfer between column and segment controller were compared with those obtained in the Scalable Read-out Unit (SRU) as reported in [5].

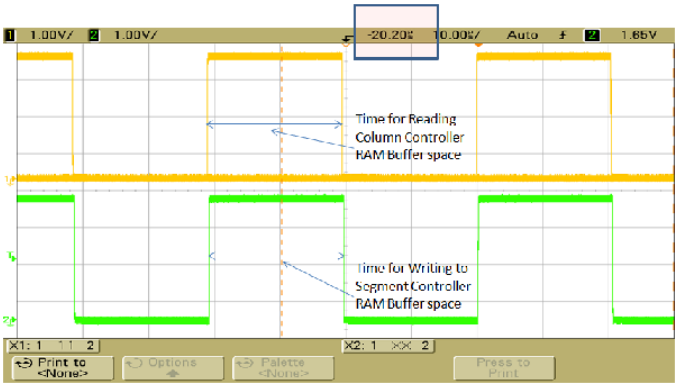

Fig. 8. Transfer time from Column Controller RAM to Segment controller RAM buffers. Total Time = 20.20us, 2048 words, 32-bits/word, 8192 bytes.

For the SRU, the event data is transmitted through three stages: (1) from ALTRO chips to FEE FPGA via the ALTRO bus; (2) from FEE FPGA to the SRU through DTC links; (3) from SRU to DAQ through the DDL link. For the SRU topology, an estimated transfer time of 5.2µs is required to transfer 1280 bytes of data between FEE over DTC link (Data, Trigger, Clock, and Control) to the SRU DTC memory buffer. The maximum bandwidth of a DTC link on the SRU is 2 Gbps As described in [6] the time to transfer the FEE data over the DTC link is calculated as follows:

$$t_{DC} = \frac{N_{FEE}}{2Gb/s} \quad (1)$$

where N_{FEE} in Eq. (1) is the number of bytes of data from all channels of a single FEE board. Therefore, comparing the preliminary results of this work with the SRU t_{DC} transfer time of , shows an improvement in data transfer rate between column and segment controller rate by almost a factor of two.

CONCLUSION

This paper presented the proposal of a new CPV-HMPID front-end read-out electronics architecture implemented using Cyclone V FPGAs and 3.125Gb/s serial transceivers.

Preliminary test results with a detector occupancy of 15% per column indicate an event read out rate up to 37 kHz. Further upgrades to reach a read out rate higher than 50 kHz is expected. Upgrades include to replace the old 700nm Dilogic card technology with a low cost 28nm FPGA, or ASIC module leading to better system performance, throughput and maintainability.

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