PIEZOELECTRIC ACTUATORS CONTROL UNIT

Franco Bedeschi, Stefano Galeotti, Alberto Gennai, Carlo Magazzu, Diego Passuello, Elena Pedreschi, Franco Spinella (INFN Pisa, Italy), Federico Paoletti, (INFN Pisa and EGO, Italy)

Abstract

Superconductive cavities for future linear accelerators, such as ILC, have extremely large quality factors that require an effective stabilization with both slow and fast tuners. Piezoelectric actuators are the most common choice for fast tuners, but one drawback for large scale applications is the limited bandwidth and the large cost of commercially available drivers. In this paper we present a low cost driver which is ideally suited for fast tuner application, large system packaging and has an extremely flexible design. Driving piezoelectric actuators having capacitive loads up to a few microFarads in the kHz range requires amplifiers with good current output capabilities at a few hundred Volts. The Piezo Control Unit we developed for the ILC Test Area at Fermilab is composed by a 6U Eurocard crate hosting 5 Piezo Driver modules capable of driving up to 10 piezoelectric actuators. The unit main specifications include large voltage rails (-175 V to +175V), wide signal bandwidth (DC to10 kHz) and low output noise (<10 mVrms). The driver is equipped with both output voltage and output current monitor.

OVERVIEW

Several tuner design employing piezoelectric actuators have been developed for the compensation of Lorentz force detuning in superconducting cavities under high gradient pulsed operation as foreseen for XFEL and ILC experiments [1][2].

In ILC the drivers for the piezo crystals should be properly engineered, having in mind the expected large scale production: > 16,000 components for the baseline 500 GeV design. This consideration led us to develop a driver that is flexible, since the type of crystal to be used is not yet decided, and very low cost, given the large number of units required.

Piezoelectric actuators have capacitive loads ranging from hundreds of nanoFarads up to a few microFarads. Driving such actuators at relatively high frequency (100Hz-1kHz) requires amplifiers with good current output capabilities at a few hundred volts. A preliminary list of piezoelectric actuators that could be used includes devices with a capacitance ranging from 1 to 40 microFarads and requiring voltages up to 150V.

PIEZO CONTROL UNIT

We designed a Piezo Control Unit (PCU) constituted by a single standard subrack/19"-chassis 6U, 84HP. The PCU can host up to 5 dual channel piezo driver modules (iPZD). Both Low Voltage and High Voltage power supplies are hosted in the case. The main specifications for the iPZD module are the following:

- Bipolar voltage rails (-175 V to +175V)
- Full Power Bandwidth: 100 Hz
- Small Signals Bandwidth: 10 kHz
- 3 A max peak current
- Noise on electrical output: <10 mVrms

Since the gain of the amplifier are adjustable from 20x up to 400x, the external control inputs are low voltage DC signals.

The driver is equipped with both output voltage and output current monitor. Additional features are an on-board Digital Signal Controller for circuit supervision and protection, CANbus and RS-232 interfaces.

The Output Stage consists of a complementary MOSFET output (source followers) with low output resistance (RDS On), that is implemented with multiple MOSFETs operating in parallel in AB class.

While the whole bandwidth of the piezo driver is in the kHz range, it operates in closed loop up to 30 Hz, thus allowing an optimal control of the piezo dc bias without limiting the driver bandwidth.

Figure 1 shows a conceptual block diagram of the system.

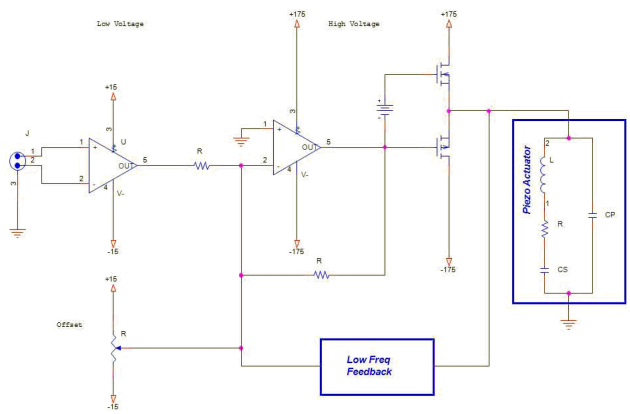

Figure 1: Conceptual Schematic

PCU can be operated with a wide range mains/line input voltage (from 90 - 264 VAC) 50/60Hz. This option will allow testing both in Europe and USA.

Terminals

Each iPZD module is provided with independent connectors for high and low voltage input/output. All signals are single ended (ground referred). Internal cabling makes the signals available on the back of the PCU case on specified connectors. Figure 2 shows PCU back panel with an insight view of High Voltage DC-DC converters.

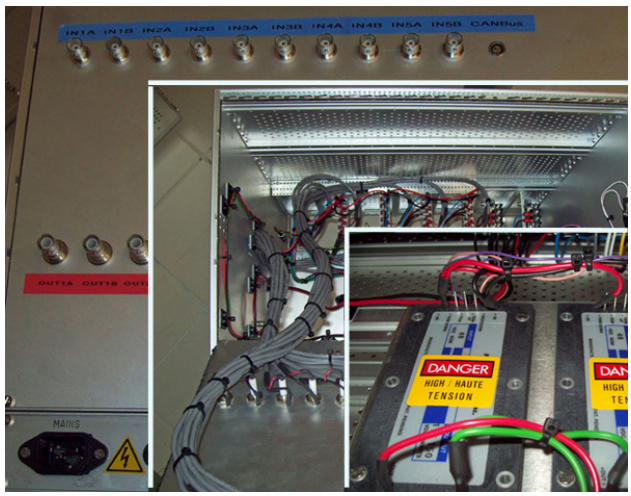

Figure 2: Piezo Control Unit back panel and insight view evidencing cabling and high voltage dc-dc converters

IPZD MODULE

Each of the five iPZD modules is hosted in a shielded plug-in module (6U, 12HP, Depth 167mm).

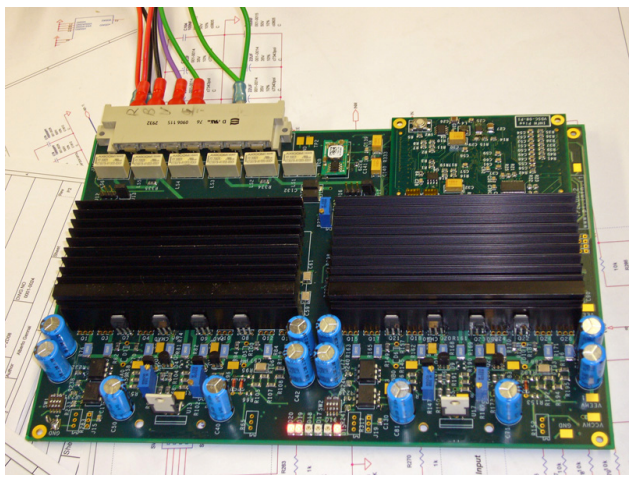
Figure 3: iPZD Module. Each module drives two independent channels.

Capacitors

In standard working conditions, piezo driver will operate driving a short (5 msec) burst of current with a peak value in the 1.0-3.0A range. Burst repetition period is expected to be in the 200 msec range (5 Hz). Using up to eight channels could require the same amount of current at the same time, bringing the total peak current to a value between 8 and 24A and the required power supply to 1.6- 4.8 kWatt (with a HV supply of 200 Volt).

In order to reduce the power of supplies we can take advantage of the low duty cycle (5/200) and let the on-board capacitors provide the requested current. In this case, taking a factor two margin on the duty cycle (5/100), we could use a supply with power in the 80 to 250 Watt range.

According to simulation, the piezo driver output stage has a Power Supply Rejection Ratio (PSRR) greater than 80 dB (test condition: 1V ripple on HV, 10 uF load). Since the output noise shall be less than 10 mVrms, we can tolerate a maximum output ripple of 5 mVpp. This output oscillation is produced by a 50 Vpp ripple of the supply voltage (80 dB PSRR). Such value can be obtained using capacitors (about 100 uFarad of total capacitance) when driving a 10 uF load with 1.5A peak current.

The total energy stored per board (1/2 C V^2), using a +/-175V power supply and 100 uF capacitors, is about 3 Joule.

Input Stage

Each channel has a single low voltage input. Input is DC coupled and single ended (ground referred). Maximum and minimum input signals are +/-10V. Input impedance is 10 kOhm.

Amplification Factor

Amplification factor can be set independently for each channel. Two dip switches located on board set the required amplification factor among one of the predefined values (20x 40x 200x 400x).

Output Voltage and Current Monitor

Output voltage divided by 50 is available on a low voltage output ground-referred. Voltage monitor, obtained dividing output voltage with resistors, has a bandwidth at least equal to piezo amplifier bandwidth. Each channel has a low voltage output proportional to the current flowing into the load. This is obtained reading the flow into the load hot terminal.

Microcontroller

Each iPZD module is equipped with a 32-Bit Digital Signal Controller. Main functionalities include General supervising, Power protection, Thermal protection, Soft Start and Digital output.

Overload Protection

Output current is limited to about 3.0A. Overload status is acquired by the on board microcontroller and signalled on a front panel led.

Instantaneous Power Protection

Current flowing into the load and voltage are continuously estimated by the microcontroller. In case the power averaged over 100 msec reaches values that could damage mosfets, gate-source junctions are shortcut and a resistor is inserted in series with the load. Status is updated and signalled on a dedicated front panel led.

Thermal Protection

MOSFETs temperature is acquired by the microcontroller. In case the value exceeds a given threshold, a resistor is inserted in series with load and HV supply is disconnected from module. Status is updated and signalled on front panel with a dedicated led.

Figure 4: Two iPZD Modules. Com port is used to program the Digital Signal Controller.

Soft Start

Piezo driver is equipped with a soft start circuit that virtually eliminates any switch-on transient. At power-on a resistor is inserted in series with load. After a few seconds (1-2) the series resistor is short-circuited with a bypass relay.

Digital Interface

Digital outputs from each iPZD module are collected by a digital I/O device equipped with a Controller Area Network (CAN) interface. CAN interface is then cabled to PCU case back. Optionally a CAN/Ethernet bridge could be added.

PERFORMANCES

Output Voltage

Output voltage is limited by the voltage amplifier section of the circuit. This section allows a maximum 350V difference between positive and negative supply. Assuming a symmetrical supply, maximum positive and negative supplies are +/-175V. In addition, a few Volts headroom should be taken into account; therefore maximum/minimum output voltage is close to +/-165V.

Output Current

Output stage makes use of 2+2 power MOSFETs having each a maximum drain current limited to about 1.5A. The maximum output current is therefore +/-3.0A.

Output Power

The iPZD circuit was designed to operate with short current burst and low duty cycle. A typical value for continuous output power is 20 Watt. When the circuit is instead operating with a pulsed signal, the instantaneous peak apparent power can be in the order of 300 Volt-Ampere

Bandwidth

While the definition of the small signal bandwidth is straight forward, the meaning of large signals bandwidth requires some additional explanation. For large signals the continuous wave output power is limited and therefore is not possible to make a large signal bandwidth measurement using continuous waves. However such measurement is still possible using a pulsed sine wave where only a few periods of the sine wave are applied with a proper time interval. With such pulsed sine wave we measured values reported in Table 1.

Table 1: Summary of Performances

Load	Volt (peak-to-peak)	Bandwidth (Hz)
500 Ohm	100	4800
500 Ohm	200	4700
500 Ohm	300	4500
100 Ohm	100	4600
100 Ohm	200	4300
100 Ohm	300	2200
10 microFarad	10	2900
10 microFarad	50	850
10 microFarad	100	580

REFERENCES

[1] G. Devanz, P. Bosland, M. Desmons, E. Jacques, M. Luong and B. Visentin, "Compensation of Lorentz force detuning of a TTF 9-cell cavity with a new integrated piezo tuner",c Jun 2006. Prepared for European Particle Accelerator Conference (EPAC 06), Edinburgh, Scotland, 26-30 Jun 2006. Published in *Edinburgh 2006, EPAC* 378-380

[2] A. Bosotti, C. Pagani and N. Panzeri, "Improved Design of the ILC Blade Tuner for Large Scale Production", Proceedings of Particle Accelerator Conference (PAC 07), Albuquerque, New Mexico, 25-29 Jun 2007