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Study of indium bumps for the ATLAS pixel detector

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Presented by Claudia Gemme on behalf of the ATLAS Pixel Collaboration

Abstract

The bump-bonding technology is used to join the front-end read-out chips to the silicon substrate of the ATLAS pixel detector. We review the current status of the technology used by Alenia Marconi Systems and we report on the electrical and mechanical properties and the defect rate of the Indium bumps. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

The building blocks of the ATLAS pixel detector [1] are modules basically constituted by a silicon sensor tile (sensitive area 16.4 mm × 60.8 mm) and 16 front-end (FE) integrated circuits, each serving 18 × 160 pixels. In the modules bumps are at the same time the electrical and the mechanical connection between sensor and electronics and they constitute a crucial component of the detector assembly. The general ATLAS requirements for bump deposition are:

- a bump pitch of 50 μm;
- a density of 5000 contacts/cm^2;
- ~50,000 channels/module, ~ 10^8 in ATLAS.

Even if the number of wafers to be processed for the ATLAS pixel project is modest by the industrial standards, the 50 μm pitch requirement is very challenging and only a limited number of firms have shown interest in developing this capability. In the following, we will review the results obtained by one of these firms, the Alenia Marconi Systems (AMS), which uses an Indium evaporative bump-deposition technology.

2. Bump-bonding technique

The bump-bonding technique to join the 16 front-end chips to the sensor is a two-step process: the bump deposition on both the silicon sensor and the integrated circuit wafers and the flip-chip assembly.

The first process is schematized in Fig. 1: the Indium bumps evaporated through a polyamide mask are 6.8 ± 0.2 μm high, with a thickness uniformity of 0.3 μm over a 6″ wafer. The fault

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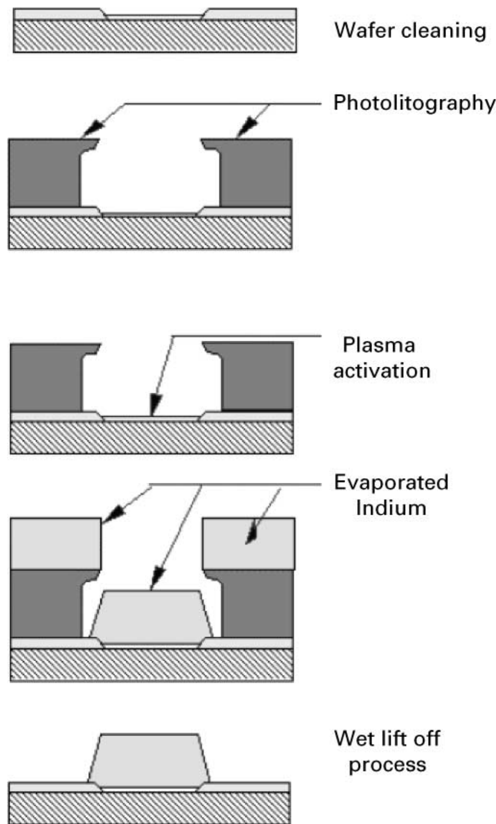

Fig. 1. Schematic representation of the bump-deposition process.

rate found by optical inspection is very low $((2.0 \pm 0.6) \times 10^{-5})$.

After having protected bumps by a polyamide layer, the electronics wafers are thinned to 150–170 μm by back grinding. Then the sensor and electronics wafers are cut to get the sensor tiles and the FE chips.

The read-out chips are aligned one by one on the sensor tile in such a way that the FE bumps face the relative sensor bumps. A cycle with controlled temperature and pressure allows the bumps to melt and to establish the electrical connections. This operation, performed in AMS with a FC6 Karl Suss bonder, is called flip-chip. The tuning of the process parameters has been performed using glass substrates in order to better investigate the effects on bumps by simple inspection under microscope. The chosen mating pressure is 25 N/FE chip, applied for 42 s on the wafers heated at 90°C. The resulting bump height is 8 μm($\sim$ 20 μm in diameter); the tensile strength to detach the two substrates is $\sim$ 0.1 g/bumps, i.e. $\sim$ 300 g/FE chip. Glass substrates are also used to periodically check the flip-chip planarity and the alignment of the mating parts, monitoring the shape of the FE corner bumps, the most sensitive to the machine settings: small distortions can determine defects in the read-out if bumps are shorted.

3. Mechanical stresses on bumps

In the ATLAS pixel detector the modules will be glued on a carbon–carbon (C–C) support. The backside of the FE chips will face the C–C and therefore bumps will be mechanically stressed during thermal cycles because of the different Coefficient of Thermal Expansion (CTE) of the silicon and of the carbon–carbon (CTE(Si) = $\sim 2.5 \times 10^{-6}$°C^{-1}, CTE(C–C) $= \sim -0.8 \times 10^{-6}$°C^{-1}). Some thermal stresses will be unavoidable as the detector will be assembled at room temperature but will operate below 0°C.

In order to study the effects of these stresses, we built a dummy module using a tile of 300 μm thick glass (pyrex) with In bumps on which we flip-chipped some 550 μm thick chips with In bumps. The mechanical stresses depend also on the elastic properties of the glue used to join the module to the C–C support: we used cyanoacrylate, a very rigid glue to enhance stresses. We performed a dozen thermal cycles (−20°C, +20°C), sometimes rising up to +40°C. Using a microscope we measured the bumps transverse displacements and we checked the bumps connectivity by measuring the bump gap with the microscope focus: this gap was constant after each cycle and equal to 8 ± 1 μm (it is typically $\sim$ 30 μm when bump is disconnected). We observed a maximum displacement of $\sim$ 7.5 μm for a $\Delta T = 50$°C with no problem for the bump connectivity: this also made possible the measurement of this glass CTE ($\sim 4.0 \times 10^{-6}$°C^{-1}). Due to the different CTE between this type of glass and silicon, we expect using a Si tile a maximum displacement of $\sim$ 3 μm for a more realistic ΔT of 30°C.

4. Electrical resistance

The bump electrical resistance must be small, so as not to contribute significantly to the front-end electronic noise. Indium develops an oxide layer once taken out of the vacuum tank where the bump deposition is done; In_2O_3 is an insulator. Fortunately, this oxide layer automatically breaks when the bias is applied to the electronics.

The bumps resistance was measured with a digital ohm-meter before and after applying 3 V. The results of these measurements for a sample of single bumps are shown in Fig. 2:

- only 10% of the bumps have initially an oxide layer ($\sim$ 500 kΩ) which is broken applying the 3 V supply;
- the measured resistance after the 3 V supply is uniformly low ($\sim$10 Ω). We also checked that the bump resistance after oxide breaking is stable in time and after thermal cycles.

5. Defects yield: merged and missing bumps

During the prototyping phase, AMS produced both full modules and single-chip assemblies. Single-chip devices consist of one FE chip and a small sensor with a sensitive area of $\frac{1}{16}$ of a full module. These reduced assemblies have been produced to better characterise the electronics, the sensors and the bump-bonding process without the complications of a full-scale module. For the present analysis we made tests on four full modules and some single chips, analysing an overall sample of about 10^5 channels. We mainly find two types of defects due to bump-bonding:

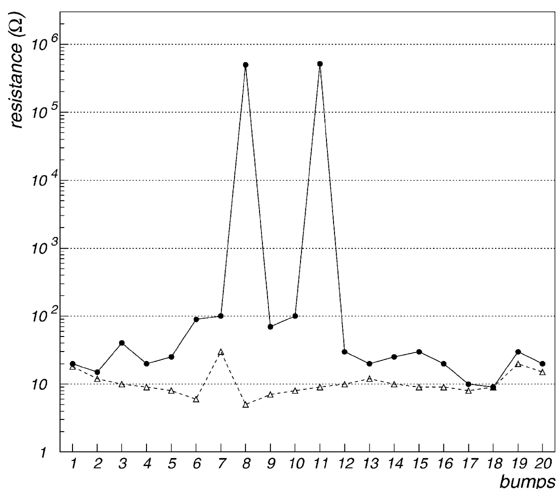

Fig. 2. Electrical resistance measured for a sample of bumps before (black circles) and after (open triangles) having applied 3 V supply.

- merged pixels: when neighbouring bumps are connected each other;
- missing pixels: when there is no contact between sensor and electronics.

Some flip-chipped devices were scanned with the X-ray and this analysis was used to correlate the bumps defects and the electrical behaviour of the pixels. The read-out electronics offers the opportunity to individually test each pixel: the block diagram of a pixel cell is shown in Fig. 3. The analogue part consists of a charge preamplifier followed by a discriminator. The preamplifier is connected to the detector diode through a bump bond pad and to an injection capacitor for calibration purposes. The procedure we use to test each pixel is the following:

(a) a digital injection to test the digital part of the pixel electronics and the overall FE electronics;
(b) an analogue injection, i.e. a signal injected at the input of each pixel amplifier, to measure threshold and noise of each channel;
(c) a scan using a radioactive source to test the overall chain (sensor and electronics).

The analogue scan identifies the *bad* pixels which never respond to the injection. In this case, if the digital part of the pixel is working, the fault can be due to the following reasons: a non-working preamplifier, a very high threshold, a merged bump. In this last case the injected charge goes in a neighbouring pixel which results noisier as it copes with a larger input capacitance. Merged bumps can be easily identified using an automatic program which processes threshold and noise values for each pixel and exploits this typical feature of the merged pixels (bad near noisy). The number of merged pixels is $\sim$ 0.1%, i.e.

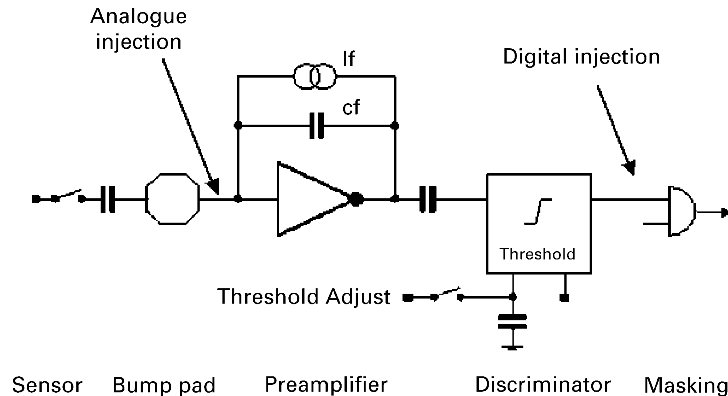

Fig. 3. Schematic view of a pixel cell.

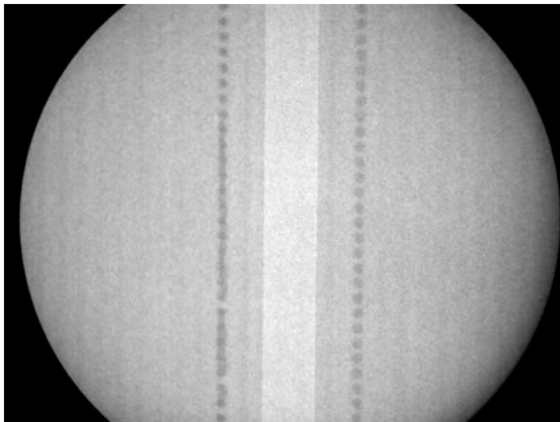

Fig. 4. X-ray image of some bumps in a flip-chipped device: some merged bumps (on the left) can be compared with the normal size bumps.

2 pixels/FE but some large zones ($\sim$ 20 pixels) of merged pixels in column 0 are present in 15% of the front-ends, which could be due to a non-perfect planarity in the flip-chip (i.e. excess of pressure in one corner). An example of merged bumps as seen in the X-ray images is shown in Fig. 4.

Missing pixels could be due to missing bumps in the deposition process (isolated channels) or to detachment during handling (mainly large zones of 50–200 pixels at the corners of the FEs). The missing pixels can be found in two steps:

- from the analogue scan suspected missing pixels are identified as good electronics channels with a very low noise ($< 100e^-$);
- with the source analysis the previous channels are confirmed as missing if they have no hits.

The rate of missing channels is $\sim 2 \times 10^{-5}$ (not including those due to bad handling).

6. Conclusions

The AMS bump-bonding technology has been reviewed and main properties of In bumps have been presented:

- bumps have an electrical resistance ($\sim 10\ \Omega$) which fits the FE electronics requirements;
- bumps can stand transverse displacements of $\sim 8\ \mu m$ without problems on the connectivity (to be confirmed after long-term tests);
- the defect yield is low: $\sim 0.1\%$ of merged pixels and $\sim 2 \times 10^{-5}$ of missing pixels.

AMS has shown a good control in the bump-bonding and flip-chip processes, obtaining reproducibility in bumps quality and fitting the ATLAS pixel detector requirements.

References

[1] The ATLAS Pixel Collaboration, ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13, 1998.