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Advanced pixel sensors and readout electronics based on 3D integration for the SuperB Silicon Vertex Tracker

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Abstract

The potential of 3D integration of sensors and readout electronics is being explored in view of the demanding requirements of the innermost layer of the SuperB Silicon Vertex Tracker. This paper reviews the 3D designs that are targeting SuperB, which include CMOS active pixel sensors and front-end chips for fully-depleted, high-resistivity pixel sensors.

Keywords: MAPS; CMOS pixels; Charged particle tracking; 3D integration; Front-end electronics

1. Introduction

The SuperB project was approved in December 2010 by the Italian government and foresees the construction of a high luminosity (> 10^{36} cm^{-2} s^{-1}) asymmetric e^+e^- collider in the campus of the University of Rome "Tor Vergata". In the SuperB detector, the Silicon Vertex Tracker (SVT) [1] is based on the BaBar vertex detector layout with an additional innermost layer (Layer0) close to the interaction point, with a radius of about 1.5 cm. This Layer0 has to provide high position resolution (10-15 μm in both coordinates), low material budget (< 1% X_0), and tolerance to a high background rate (several tens of MHz/cm^2) and to ionizing radiation (3 Mrad/year). The baseline design of the SuperB SVT presently adopts the technically conservative solution of using short strip detectors (striplets) in the Layer0. However, the stringent experimental requirements stimulate an R&D program on low-mass pixel sensors

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[2], which is exploring CMOS MAPS technology as well as 3D integration. The ambitious goal is to build a monolithic device with similar electronic functionalities as in hybrid pixel readout chips, such as pixel-level sparsification and time stamping.

This paper presents the status of the R&D activity that the VIPIX collaboration [3] is carrying out to achieve this goal. The effort is presently focused on the design of two different devices. The first one is a deep N-well active pixel sensor based on the interconnection of two layers fabricated in the same 130 nm CMOS technology. The second one is aimed at the ultimate goal of fabricating a 3D device based on heterogeneous technologies, i.e. a high resistivity sensor layer interconnected to a 2-tier CMOS readout integrated circuit. Both devices include a high performance readout architecture which is able to handle a very large data flow. The paper reviews the technical details concerning how these two different designs may fit the requirements of the SuperB SVT Layer0 and the present status of VIPIX 3D developments.

2. 3D integration and advanced pixel sensors

In the past few years, the developments in the field of 3D integration have suggested that this technology could bring along a performance leap for semiconductor radiation detectors [4] in future high energy physics experiments at particle accelerators (HL-LHC, ILC/CLIC), of course including SuperB. In these applications, a fundamental problem will be the reconstruction of charged particle tracks with high resolution pixelated sensors. These sensors, along with the readout electronics, will be required to have a small pixel pitch (≤ 20 μm in some applications), a high degree of radiation tolerance (up to 350 Mrad of ionizing radiation and 10^{16} neutrons/cm^2), an adequate signal-to-noise ratio for the detection of small signals (from a few hundreds to a few thousands of electrons), a low mass (down to 0.1% radiation length for a detector layer) to minimize particle scattering, a low power dissipation (down to 100 μW/cm^2) and the capability of handling very high hit rates (up to 10 MHz/mm^2). To meet such requirements, advanced functions have to be performed in the electronics elementary cell of each pixel to cope with signal-to-noise ratio and high data rate requirements. These functions include amplification, filtering, calibration, discriminator threshold adjustment, zero suppression (also called data sparsification) and time stamping. 3D integration can be a solution to the problem of integrating all these functions inside a small pixel, avoiding the use of aggressively scaled CMOS, below 100 nm feature size, which can be expensive and challenging for analog circuit design [5].

Two main research lines and technical solutions are being followed to exploit 3D vertical integration for SuperB pixels. The first one can be seen as a development of the classical CMOS MAPS (Monolithic Active Pixel Sensors) concept of signal charge generation and collection by diffusion in an undepleted silicon region. Since several years, MAPS have demonstrated their capability to perform charge particle tracking. The MIMOSA chips series is an excellent example of an R&D program that was able to qualify MAPS for application in a high energy physics experimental apparatus, such as the STAR PXL detector [6]. Although these developments have already achieved very good results, 3D integration is very attractive for the development of CMOS sensors suitable to the SuperB vertex detector. Vertical integration of two (or more) CMOS layers makes it possible to separate the analog front-end electronics from the digital readout sections, with great advantages in terms of pixel size, functionalities and performance. Different readout architectures have been designed to handle a large data flow without the constraints that may arise when digital electronics is implemented on the same substrate as the sensor (as in standard MAPS) [7, 8].

The second research line explores the possibility of using 3D integration to interconnect layers fabricated in different technologies, i.e. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in a deep submicron CMOS process. This can provide a large benefit in terms of radiation hardness and signal-to-noise ratio with respect to MAPS. In this case, 3D integration can lead to an extension of the hybrid pixel concept that was adopted by LHC experiments [9].

Besides an increase of the functional density of the electronic readout chip, the use of 3D techniques could lead to a substantial reduction (with respect to classical bump bonding) of the amount of material and of the pitch associated to the interconnection between the pixel sensor and the front-end chip itself [4, 10].

This paper will present a review of the ideas and of the devices that are being developed to satisfy the needs of the SuperB SVT Layer0 with the help of 3D integration technologies by the R&D collaboration VIPIX. The VIPIX 3D devices are presently based on the Tezzaron "via middle" process with the face-to-face bonding of two 130 nm CMOS wafers by GlobalFoundries [11]. In such a process, the Through-Silicon Vias (TSV) are etched in the silicon wafers in the early stages of the CMOS fabrication, just after transistor processing steps and before the deposition of the various levels of metal interconnects. A high density of TSVs (with a pitch of a few μm) can be achieved with this kind of processing. In order to provide an electrical connection between the two tiers, a bonding interface consisting of copper pads is laid out on the top metal layer of the wafer. This interface allows for a thermocompression bonding between two wafers. Figure 1 shows the double layer structure (with two "tiers") of the resulting 3D devices. After bonding, one of the two wafers is thinned to expose TSVs and provide vertical interconnections from the two device tiers to the bonding pads.

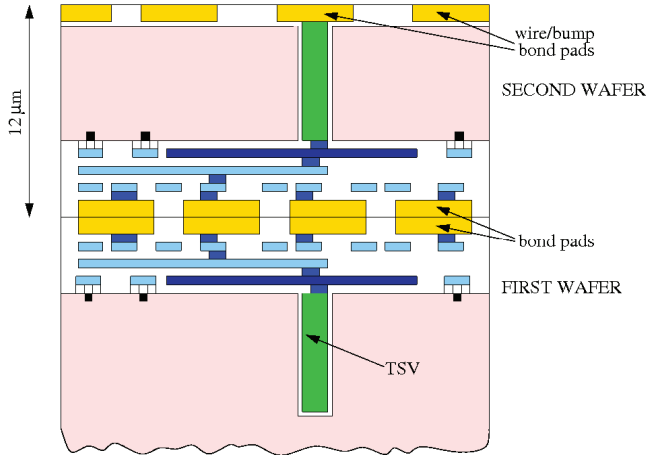

Fig. 1. Structure of the two-tier devices fabricated with the Tezzaron/GlobalFoundries 3D integration process.

3. 3D CMOS pixel sensors

3D vertical integration technologies appear to be extremely attractive for the development of MAPS. In standard MAPS, it is difficult to integrate advanced functionalities in the pixel cell, since PMOSFETs are avoided; they are located inside N-type wells which compete for charge collection with the signal electrode (also N-type), and degrade the fill factor [12]. Different concepts are being developed with the aim of using full CMOS circuits in the pixel without degrading charge collection, such as the use of large deep N-well electrodes [13], of an SOI process [14], or of a quadruple well CMOS technology [15]. Although these developments are very interesting, a 3D multilayer sensor structure promises to overcome typical limitation of MAPS in a very effective way. In a 3D MAPS device, for example, a layer may host sensing electrodes and analog circuits, whereas digital electronics may be located in upper layers. A multilayer structure allows also for a smaller pixel pitch and a smaller sensor capacitance, leading to a better trade-off between noise and power dissipation. The removal of layout constraints related to

efficiency problems may also have a beneficial impact on the digital readout architecture, adding more complex functionalities and increasing flexibility.

The VIPIX collaboration is planning to apply 3D integration to Deep N-Well (DNW) MAPS [8] with the goal of complying with the SuperB Layer0 specifications. In the pixel cell of DNW devices, the charge collecting electrode is the deep N-well that is available in modern CMOS processes. This electrode is extended over a relatively large fraction of the cell area. In this way, fully CMOS analog and digital circuit blocks can be used in the pixel, provided that the area of standard N-wells housing PMOSFETs is small compared to the deep N-well electrode, with which they compete for charge collection. As for standard MAPS, a 3D implementation promises to deliver several important performance advantages to DNW devices as well. Most (if not all) PMOSFETs with their competitive N-wells can be removed from the layer where the sensing electrode is located, improving the charge collection efficiency. This allows the designer to remove several important constraints both in the analog and digital circuits that are integrated in the pixel cell.

When a DNW MAPS evolves from a standard 2D CMOS process to a 3D technology, the basic idea is to keep the DNW charge collecting electrode and the analog electronics section in the first layer, whereas the digital readout section is located in the second CMOS layer. As shown by Fig. 2, a charge-sensitive preamplifier is the first stage of the analog section [16], so that the gain is set by its feedback capacitance and is instead independent of the value of the capacitance of the sensing electrode. The C_{FB} feedback capacitor in the preamplifier is continuously discharged by an NMOS transistor biased in the deep subthreshold region by the voltage V_{FB}.

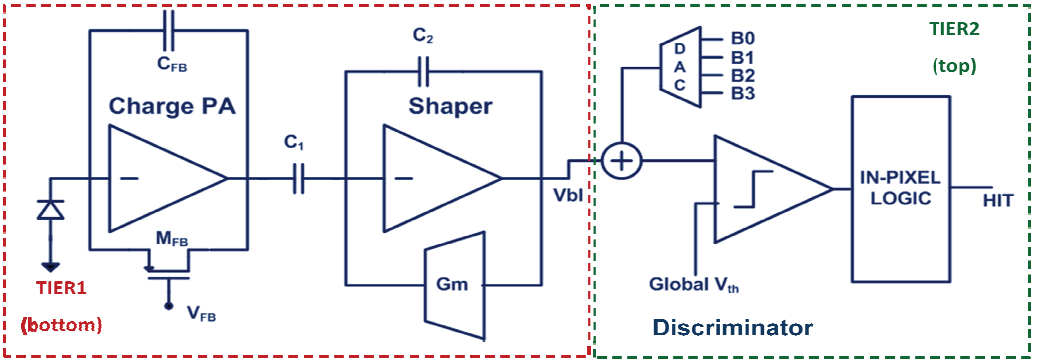

Fig. 2. Block diagram of the front-end circuit for a 3D DNW MAPS.

The preamplifier is followed by a continuous time, RC-CR shaper, where the capacitance C_2 is discharged by a transconductor G_m. After signal shaping and filtering, the signal is applied to the input of a hit / no hit discriminator. The size of the pixels (50 x 50 μm^2) is compliant with SuperB Layer0 specifications, considering that each pixel provides this binary information about particle hits. The discriminator is located in the digital tier and is followed by a latch and by the sparsification and time stamping logic integrated in the pixel. Because of the functional density allowed by 3D integration, in the pixel cell it is possible to include a 4-bit digital-to-analog converter (DAC) for a local correction of the threshold voltage. This makes it possible to reduce the threshold dispersion across the pixel matrix to an acceptable level. The target design values of noise and threshold dispersion are determined by considering that they set the lower limit for the discriminator threshold which gives a negligible noise hit rate. To this purpose, a "4σ" rule was applied to maintain the noise occupancy at acceptable levels (discriminator threshold $Q_{th} > 4 \cdot ENC + 4 \cdot \sigma_{Qth}$, where σ_{Qth} is the threshold dispersion expressed in units of electric charge), while allowing a threshold corresponding to ¼ of the charge delivered by a minimum ionizing

particle. From the previous experimental characterization of 130 nm DNW CMOS MAPS, ¼ M.I.P. charge corresponds to 200-250 electrons [13].

Figure 2 shows the block diagram of the analog channel in this 3D MAPS design. Table 1 summarizes the main performance parameters of the 3D DNW MAPS, that is currently at an advanced design stage. Dedicated R&D studies demonstrated that in the SuperB Layer0 the 30 μW/pixel power dissipation, while not strictly low, can be effectively handled by a cooling system based on a light carbon fiber support with integrated microchannels for the coolant fluid (total material budget for support and cooling below 0.3% X_0) [2].

Table 1. Main performance parameters of the 3D DNW MAPS prototype.

Charge sensitivity	850 mV/fC
Shaper peaking time	300 ns
Equivalent Noise Charge	35 e rms (for an estimated sensor capacitance of 300 fF)
Threshold dispersion before DAC correction	100 e rms
Threshold dispersion after DAC correction	15 e rms
Analog power consumption	30 μW/pixel
Pixel array size	128 x 96
Pixel size	50 μm x 50 μm

In the digital tier, the pixel-level logic (not shown in Figure 2) enables a sparsified, time-ordered triggered readout of the pixel matrix [17]. To accomplish this, a time stamp information is stored in the pixel and is compared to a time stamp provided by the triggering system and broadcasted to the matrix by the readout blocks located in the chip periphery. Only pixels where the two time stamps are the same send a "data out" bit to the periphery, where their address is formatted and sent off-chip. This readout architecture allows a big reduction of the amount of information that has to be transmitted off-chip, relaxing the requirements of the on-chip data output interface. VHDL simulations of this architecture show that hit detection efficiency is limited by the trigger latency, since in the present version each pixel can store only one hit. For example, at a 6 μs trigger latency (the presently expected value in SuperB), the simulated efficiency is about 98 %. The possibility of storing multiple hits associated to different time stamps is presently being investigated [7, 17]. This architecture can also be operated in a data push fashion, reading out all the hits in a time ordered way. Obviously, a data push readout, with respect to a triggered one, puts much more demanding requirements on the chip data output bandwidth and on the interconnection bus which transfers data off the detector. In the data push case, simulations show that the high degree of parallelization of the architecture may lead to an efficiency exceeding 99%, even at the background rate of 100 MHz/cm^2 that is expected (with a factor of five safety factor) in the SuperB Layer0. These simulation results are relevant to a 200x256 matrix model, which was subdivided in 4 submatrices, each operating at 50 MHz readout clock and using a time stamp clock period ranging from 0.2 to 2 μs. A data concentrator at the back-end of the four submatrices drives the output data bus, which is synchronous to a 200 MHz clock. This bus can use up to 20 output lines (depending on the expected hit activity), achieving a maximum throughput of 4 Gbps.

4. 3D CMOS readout chip for high resistivity, fully-depleted pixel sensors

The standard substrates or epitaxial layers of CMOS technologies have a relatively low resistivity as compared to the high resistivity bulk that is typical of dedicated fabrication processes for fully-depleted pixel sensors. This results in a higher sensitivity of CMOS sensors to bulk displacement damage. This is a non negligible problem in SuperB, where an equivalent neutron fluence (mainly due to electrons in the MeV energy range) of about 3.5 x 10^{12} n/cm^2/year is expected. This may give an advantage to high resistivity pixel detectors, which are more tolerant to displacement damage because charge collection is governed by a drift process, and not by a diffusion one as in the undepleted epitaxial layer of standard CMOS sensors.

3D integration can be used to interconnect layers fabricated in different technologies, e.g. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in a commercial ultra deep submicron process. Note that the readout electronics itself may already be produced in a 3D process, as in the example shown in Figure 3. The challenge then is the formation of a strong, reliable, low-mass bond between the sensor and the readout electronics. For high energy physics applications, several 3D techniques have been explored for sensor and readout integrated circuit integration to overcome the limitations of standard bump bonding technology in terms of pitch and of material [4]. A decrease of the amount of material in the system is crucial to reduce errors in track reconstruction due to multiple scatterings of particles in the detectors.

The schematic of the pixel cell that the VIPIX collaboration is presently integrating in a 3D chip for the readout of a 32x128 high resistivity pixel matrix is very similar to what Figure 2 shows in the case of 3D DNW MAPS. This includes a preamplifier and a shaper in the first (analog) tier, and the discriminator with the DAC for threshold adjustment in the second (digital) tier. The pixel-level logic and the global readout architecture are also the same as for the 3D MAPS. However, there are some important differences in the design of the analog blocks, as dictated by the different parameters of the sensor. In a CMOS sensor, signal charge is collected in a layer of a thickness of the order of 10-15 μm, and seldom exceeds 1000 electrons. Instead, the entire bulk (of a typical thickness of 100-300 μm) of a fully-depleted high resistivity pixel sensor delivers the charge carriers generated by radiation to the collecting electrodes.

In the case of the minimum ionizing particles that are relevant for high energy physics experiments, this gives a considerably larger signal than in MAPS. It is then possible to relax the requirements on the noise and the threshold dispersion, which allows the analog pixel cell to operate at a lower power dissipation. This is apparent in Table 2, showing the main simulation parameters for the 3D CMOS readout chip that is currently being designed by the VIPIX collaboration.

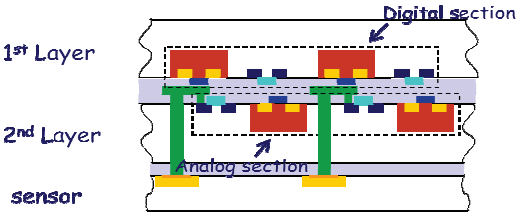

Fig. 3. Concept for the interconnection between a 3D CMOS readout chip and a high resistivity pixel sensor.

Table 2. Main performance parameters of the 3D CMOS chip for the readout of high resistivity pixel sensors.

Charge sensitivity	50 mV/fC
Shaper peaking time	250 ns
Equivalent Noise Charge	130 e rms (for an estimated capacitance of sensor and strays of 150 fF)
Threshold dispersion before DAC correction	550 e rms
Threshold dispersion after DAC correction	65 e rms
Analog power consumption	10 μW/pixel
Pixel array size	128 x 100
Pixel size	50 μm x 50 μm

5. Status and plans for the R&D on 3D integration

To meet the challenges associated with design, fabrication and testing of 3D vertically integrated pixel sensors, the radiation detector community has organized itself in various consortia, with the goal of tackling different technologies and design solutions. The 3D-IC Consortium [18] was promoted by Fermi National Accelerator Laboratory to explore various issues associated to 3D integration. European and U.S. institutions are presently members of this Consortium, which, as a first step, is going to investigate 3D devices based on two layers ("tiers") of the 130 nm CMOS technology by GlobalFoundries, vertically integrated with the previously described Tezzaron interconnection technology.

The 3D MAPS and the 3D CMOS readout chip that were discussed in the previous sections are presently (September 2011) at an advanced design stage. However, the submission and fabrication of these devices will be put on hold, waiting for the experimental results from the first 3D prototypes that the 3D-IC consortium submitted to Tezzaron in a 2009 multiproject wafer (MPW) run. The 130 nm CMOS wafers from this run were fabricated by GlobalFoundries; one of these wafers was diced before the 3D interconnection, so that it was possible to test separately analog and digital circuits in the two tiers. All these tests were successful, showing that the various blocks are fully functional; a DNW MAPS structure was also tested with radioactive sources, proving that the substrate of these CMOS devices is able to detect ionizing particles [19]. Tezzaron has very recently delivered the first completed 3D wafers. After dicing, 3D chips will be tested and it will be possible to give the green light for the next 3D-IC MPW run, with the larger structures described in Sections 3 and 4. This new run will be managed by the MOSIS and CMP MPW services [20].

Another 3D-related initiative is taking place in the frame of the AIDA project, a EU-funded FP7 program addressing infrastructures for detector development for future particle physics experiments. In AIDA, WorkPackage3 aims to establish a network of groups from European universities and high energy physics research institutes working collaboratively on 3D integration technology for thin pixel sensors with complex pixel-level functionality, with small pixel size and without dead regions. A major goal of AIDA WP3 is to build a demonstrator based on 3D integration. WP3 plans to follow a "via last" approach to 3D integration to build a 2-layer device in heterogeneous technologies (e.g., high-resistivity pixel sensors and CMOS readout chips). In a "via last" 3D process, TSVs are fabricated on fully processed CMOS wafers [21]. The density of vertical interconnections is in this case considerably smaller (more than one order of magnitude) than for a "via middle" process. However, the "via last" approach can be useful when vertical interconnections are needed only in the peripheral regions of the chips, close to bonding pads for external connection.

6. Conclusions

3D integration is stimulating new concepts in the field of radiation detectors and readout electronics. This paper discussed a research program that aims at realizing expectations of substantial performance improvements with this technology. So far, progress in R&D activities is generally slow, also because of industry trends in the semiconductor market. However, the expanding interest of the sensor community and the exploration of different technologies are expected to lead very soon to 3D integrated circuits and radiation sensors working in real applications, especially where there is a need for small pitch pixels that are capable of handling high data rates.

The R&D on pixel sensors for the SuperB Layer0 will proceed to a technology choice in a couple of years from now, taking into account that an advanced pixelated system will be needed when the machine will operate at full luminosity, about two years from the first collisions expected in 2016. 3D integration may provide the solutions to the challenges of Layer0 in terms of both electronics and sensors. However, besides technical issues, an answer is expected from the 3D MPW runs about the possibility for the detector community of accessing this technology in a reliable and stable way.

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