Development of a triple well CMOS MAPS device with in-pixel signal processing and sparsified readout capabilities

SLIM5 Collaboration

A. Gabrielli[c], G. Batignani[a], S. Bettarini[a], F. Bosi[a], G. Calderini[a], R. Cenci[a], M. Dell'Orso[a], F. Forti[a], P. Giannetti[a], M.A. Giorgi[a], A. Lusiani[a], G. Marchiori[a], F. Morsani[a], N. Neri[a], E. Paoloni[a], G. Rizzo[a], J. Walsh[a], L. Gaioni[e], M. Manghisoni[b], V. Re[b], G. Traversi[b], M. Bruschi[c], B. Giacobbe[c], N. Semprini[c], R. Spighi[c], M. Villa[c], A. Zoccoli[c] G. Verzellesi[d] C. Andreoli[e], E. Pozzati[e], L. Ratti[e], V. Speziali[e], D. Gamba[f], G. Giraudo[f], P. Mereu[f], L. Bosisio[g], G. Giacomini[g], L. Lanceri[g], I. Rachevskaia[g], L. Vitale[g]

[a]Pisa University, INFN-Pisa and Scuola Normale Superiore,
[b]Bergamo University & INFN-Pavia, [c]Bologna University & INFN-Bologna,
[d]Modena & Reggio University & INFN-Padova, [e]Pavia University & INFN-Pavia,
[f]Torino University & INFN-Torino, [g]Trieste University & INFN-Trieste, Italy.

Abstract

The **SLIM5 collaboration** has designed, fabricated and tested several prototypes of CMOS Monolithic Active Pixel Sensors (MAPS). The key feature of these devices, with respect to traditional MAPS is to include, at the pixel level, charge amplification and shaping and a first sparsification structure that interfaces with on-chip digital readout circuits. Via the 3-well option of the applied **0.13μm ST-Microelectronics CMOS** technology each pixel includes a charge preamplifier, a shaper, a discriminator, an output latch, while retaining a fill factor of the sensitive area close to 90%. The last device of the family was submitted on Q4 2006 and the tests are ongoing. On this sensor, an on-chip, off-pixel digital readout block (streamout data sparsification) was added to implement, to control and to readout a test matrix built up of 4 x 4 pixels. It is aimed at proposing solutions that will overcome the readout speed limit of future large-matrix MAPS chips.

SLIM5 project

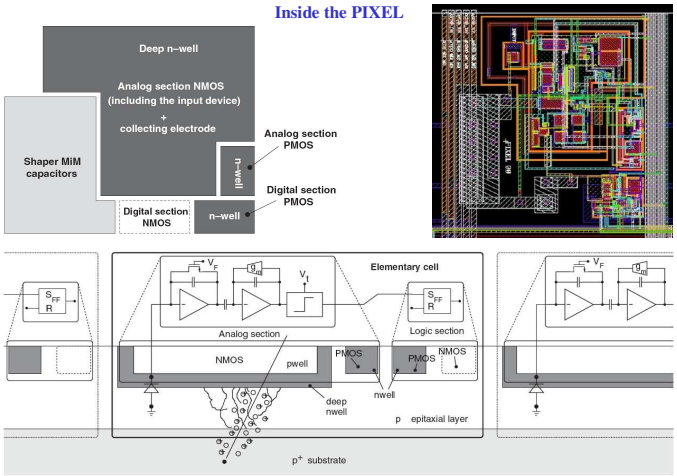
Aim

Improve the state-of-the-art of slim tracking system construction for high-energy physic applications

Applications

Low material budget silicon tracking systems (detector/ mechanics/cooling) relevant for the future experiments (SuperB, ILC) to reduce multiple scattering

Inside the PIXEL

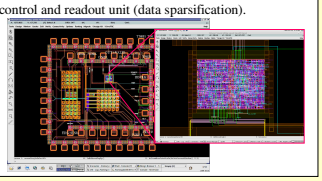


MAPS

Monolithic Active Pixels Sensors (MAPS) represent a good candidate technology for the innermost layers of the vertex detector where the background rate is relatively high and it is important to keep the material content at minimum. The sensitive zone of the detector is about 10-20 μm thick and the front-end electronics is integrated on the same silicon substrate, allowing a significant reduction of the material budget with respect to standard hybrid pixel systems, while at the same time simplifying detector assembly. The high segmentation of the detector, with very small pixel cells, improves the position resolution and reduces the occupancy. All these prototype chips have been built with three different substrate thicknesses (250 μm, 120 μm, 80 μm) to test the possible dependence of the sensor response.

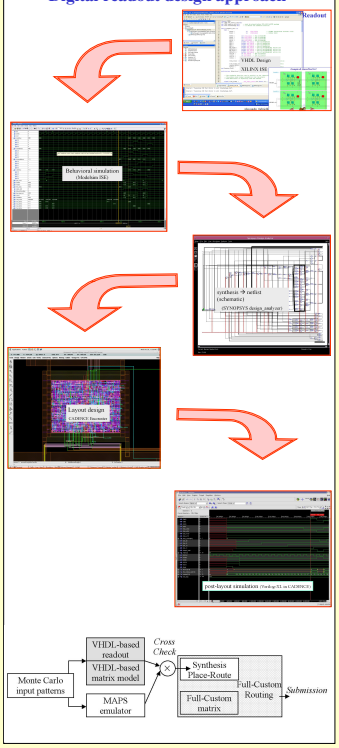
APSEL2D design

This prototype was submitted on Nov. 2006 in 0.13μm CMOS ST-Microelectronics technology. It is a mixed-mode component with a 4 x 4 pixel matrix of MAPS. The chip also implements a first off-matrix digital control and readout unit (data sparsification).



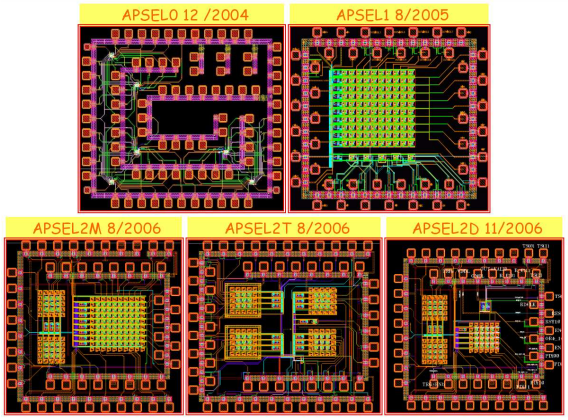
APSEL2D

Digital readout design approach



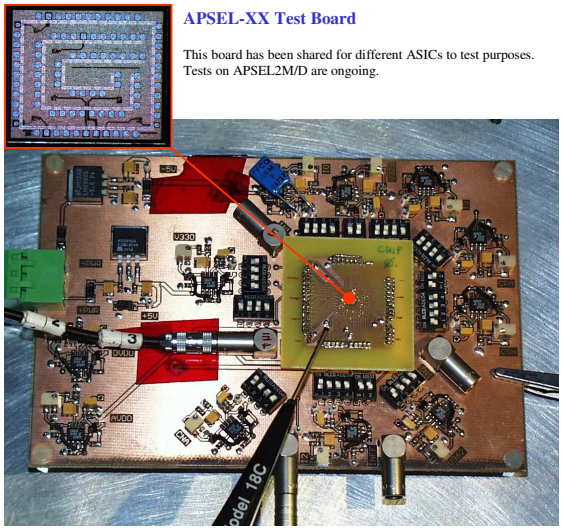
Fabricated chips

APSEL0, APSEL1, APSEL2M/T are **full-custom** designed ASICs while **APSEL2D**, which includes a standard-cell-based readout logic, is a **mixed-mode** component.



APSEL-XX Test Board

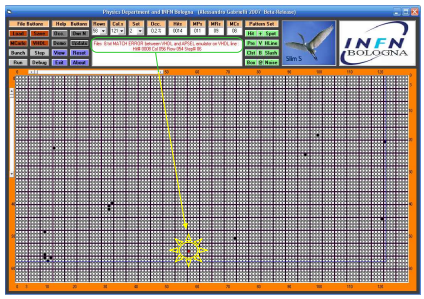
This board has been shared for different ASICs to test purposes. Tests on APSEL2M/D are ongoing.



Tests

The APSEL0/1 chips were tested and characterised with radioactive sources, while APSEL2M/T/D tests are ongoing. An X-ray ^{55}Fe source was used to calibrate pixel noise and gain in channels and the response to MIP from a ^{90}Sr β-source was used to measure S/N ratio for MIPs. For the APSEL0 prototype a pixel noise of 125 e– ENC and a S/N = 10 were reported. After a direct measurement of the sensor capacitance, the front-end was further optimized, achieving a pixel noise of about 40 e– ENC in the APSEL1 chip. A large threshold dispersion (about 1/4 of a MIP) and a pixel noise of about 50-70 e– ENC have been measured in the pixel matrix present in the APSEL1 chip. The noise is slightly higher than the measured on single pixels, probably because of the indirect measurement method (only the digital information is available) and to some digital interference in the matrix. An improved front end has been implemented in the successive prototypes chips, presently under test, to reduce the threshold dispersion at the level of the pixel noise, and to cure the cross-talk effects.

Pixel-Matrix Emulator, VHDL Dubugger



Conclusions

In this paper, a novel concept of CMOS monolithic active pixel sensor is presented. The collecting electrode consists of an n-well with a deep junction, of the kind of those available in modern deep submicron technologies aimed at shielding NMOS transistors from substrate noise. The signal is readout via a charge preamplifier, whose charge sensitivity is independent of the collecting electrode capacitance. Tests performed via radioactive sources proved that the sensor collects and processes the charge released in the epitaxial layer under the deep n-well sensitive electrode. New tests are ongoing, which should provide a more precise calibration of the system. These results confirm circuit simulations and will be carefully considered in the design and optimization of future versions of the readout electronics. Different detector geometries will also be considered for parasitic capacitance minimization and charge collection efficiency optimization. By following the improvements on the different prototypes an 8 x 8 matrix detector was developed. The work will lead to future improvements to design a high-density thin MAPS detector with an on-chip sparsified digital readout system, for particle tracking, aimed at matching the requirements of future HEP experiments. In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex detectors.