GAS PIXEL DETECTORS

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ABSTRACT

We present a new class of Micro Pattern Gas Detectors in which a complete integration between the gas amplification structure and a pixelized read-out electronics has been reached. We call this device the Gas Pixel Detector (GPD). On this purpose we have developed and built two generations of an Application-Specific Integrated Circuit (ASIC) in deep sub-micron VLSI technology. The CMOS chip has the top metal layer patterned in a matrix of 80μm pitch hexagonal pixels used as charge collecting pads and directly connected to the underneath electronics chain which has been realized using the remaining five layers of the 0.35μm VLSI technology. In this way gas detectors performances approach solid state device standards in terms of spatial resolution ($\sim 30\mu$m) and rate capability (a few MHz/mm^2). Results from tests on a first prototype of such detector with 2k pixels and on its further implementation to 22k pixels are presented. An application of this device for Astronomical X-Ray Polarimetry is discussed.

1   Introduction

Gas Pixel Detectors are MPGD type proportional counters obtained by coupling a gas amplifying stage to a pixelized charge collection plane [1]. Indeed, the real challenge of Micro Pattern Gas Detectors is the design of a read-out system which should not spoil the intrinsic performance of the device. The introduction of the Gas Electron Multiplier (GEM) as separate charge amplification structure has opened the possibility to pattern the collecting electrode in a fine multi-pixel array. This has been obtained initially by using an advanced, fine line, multi-layer PCB technology to achieve true 2D imaging capability and high rate operation. The high granularity of the pixels array preserves, in this way, the intrinsic resolving power of the device which should be otherwise lost with a conventional projective read-out scheme [2]. Nevertheless, at very small pixel size (less than

100μm) and large number of pixels (more than 1000) is virtually impossible to transfer the signal charge from individual pixels to the correspondent external electronics channels. Technological constraints limit, in fact, the dimension of the fan-out (number of connection lines) to the front-end electronics. Furthermore, cross-talk between channels and noise due to the high input-capacitance become not negligible. To overcome these limitations a custom CMOS ASIC, in deep sub-micron VLSI technology, has been developed. The chip realizes, at the same time, the charge collecting anode structure and the read-out electronics.

The top metal layer has been patterned in a honeycomb pixel array with a pitch of 80μm. Each single pad acts as individual charge collecting electrode and it is connected to a full electronics chain (pre-amplifier, shaping amplifier, sample and hold, multiplexer) built immediately below it, in the remaining five layers of the VLSI CMOS technology.

In the next section a first prototype of the chip with 2101 pixels and its successive implementation to 22000 pixels are presented. The coupling of the chip die to the gas amplifying electrode and the assembly of the micro-mechanics of the detector is also shown. Results of laboratory tests obtained with a 5.9keV X-ray source on both prototypes are reported.

The use of this new detection concept for Astronomical X-Ray Polarimetry and other applications are discussed in the last section.

2   The CMOS VLSI chip

Both prototypes have been realized using a 0.35μm, 3.3V CMOS technology. Advantages of this approach are a very low noise (~ 100 e$^-$ ENC) due to a very small pixel capacitance and a fast, asynchronous and externally triggerable read-out. Requested specifications for the ASIC prototypes are:

- 3.5-4 μs shaping time;
- 50-60 μW per pixel, typical power consumption;
- up to 10 MHz system clock;
- 0.2-20 fC dynamic range;
- 100 mV/fC amplifier gain.

2.1   The 2K prototype

A photo of the first prototype of the VLSI chip with 2101 active pixels is shown in fig.1. The chip is bonded to a ceramic CLCC68 package. In the close-up view of the hexagonal pixel pattern the four vias to the underneath pre-amp input are visible in each pixel.
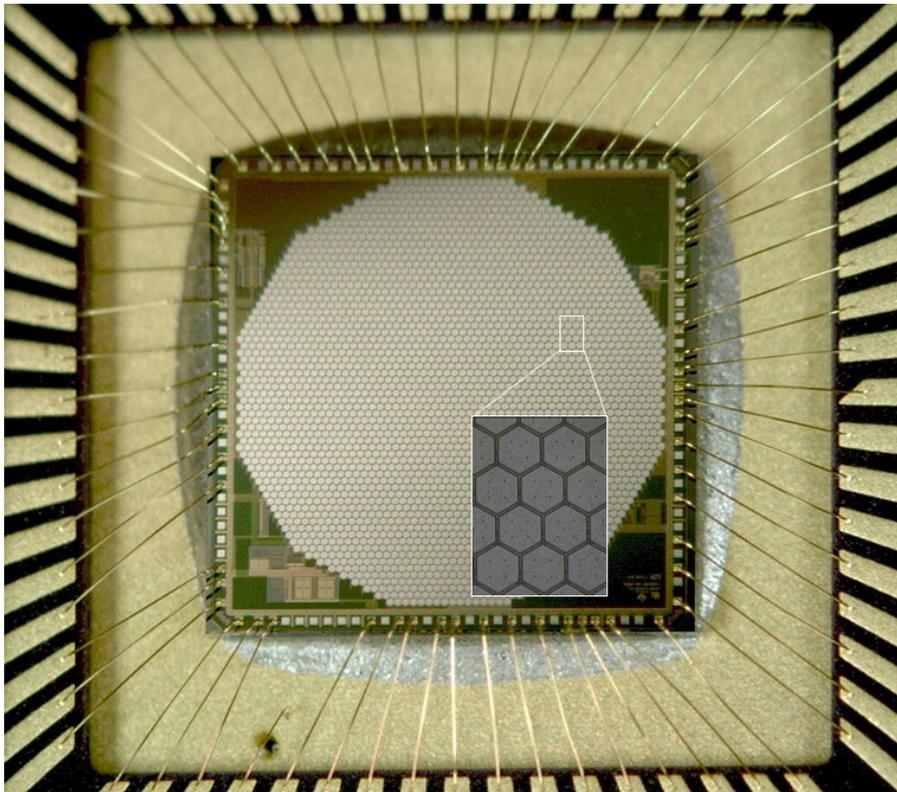
Figure 1: A photo of the chip bonded to the CLCC68 ceramic package and a zoomed view of the pixel matrix.

Fig.2 shows the simplified equivalent scheme of the full chain of *nuclear type* electronics (pre-amplifier, shaping-amplifier, sample & hold and multiplexer) for one pixel. Upon activation of an external asynchronous trigger (in our case provided by amplifying and discriminating the fast signal obtained from the top GEM electrode) and within a 10μs window, the automatic search of the maximum of the shaped signal starts. If the MaxHold signal is set, the maximum is held for the subsequent read-out which is accomplished by sequentially connecting the output of each pixel to a common analog bus. A pixel is selected by introducing a token into the shift register. Tokens are shifted one cell forward at the falling edge of the input clock. With a 5 MHz clock the total read-out time for 2100 pixels is 400μs (200 ns/pixel). By keeping the MaxHold signal low, the chip operates also in *Track mode*, namely the shaped pulse from a pixel can be observed on the analog output bus. Each pixel can be electrically stimulated at the rising edge of the Write signal, injecting a charge -Qin (10fC/V typical response) proportional to the voltage difference between Vtest and Vss (fig.3 left). In fig.3 (right) three different shaped signals obtained injecting a charge of 1000, 6000 and 60000 electrons, respectively, in the calibration capacitance are shown. Strobing each pixel with 1V signal (1000 ADC counts) a uniformity of response of 3% rms for all the 2101
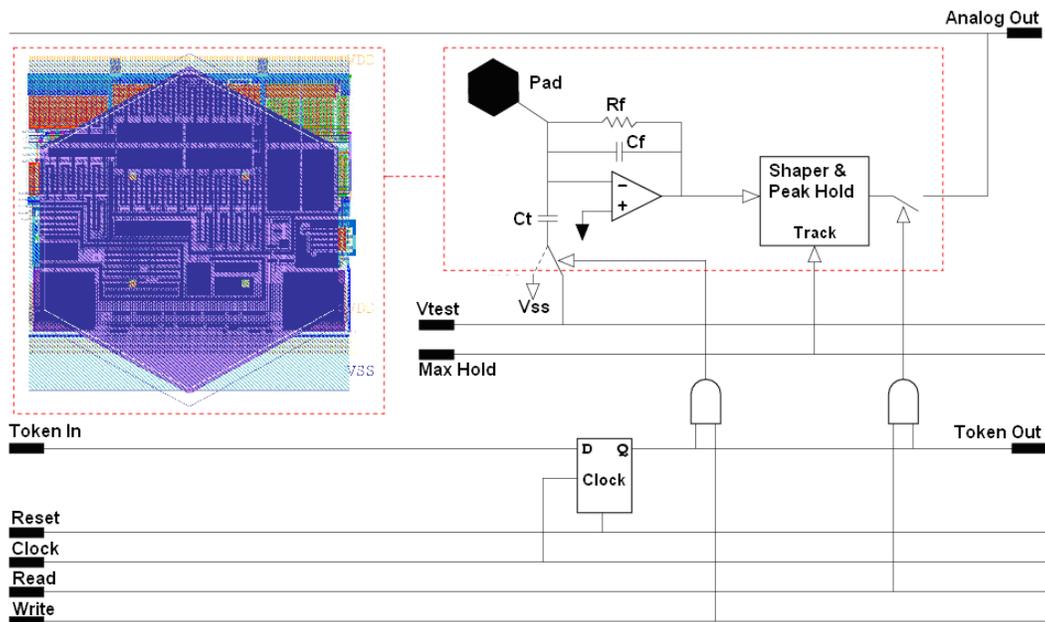
Figure 2: A drawing of the pixel layout with underlying electronics and its simplified equivalent electronic scheme.

channels has been observed. Negligible cross-talk has been measured in the channels adjacent to the ones pulsed with 1V signal. Thanks to the very low pixel capacity a noise level of 1.8mV, corresponding to 100 electrons, has been measured. This implies, at gas gain values of about 1000, a significant sensitivity to a single primary electron.

2.2 The 22K prototype

As first upgrade of the VLSI chip the active area has been incremented of roughly a factor ten, that is from $\sim$12mm^2 (4mm diameter) of the first prototype to the actual 11$\times$11mm^2 corresponding to a 22080 pixels (fig.4). The pixel elements are still hexagonally shaped but arranged according to a honeycomb pattern on a squared area (fig.5). The circuit is organized in 8 identical clusters of 2760 pixels (20 rows of 138 pixels each) with an independent differential analog readout buffer. Each cluster also features customizable self-triggering capability with independently adjustable thresholds. Upon the activation of an external digital control input, or from on-chip wired-OR combination of each cluster self-triggering circuit, the maximum of the shaped pulse is stored inside each pixel cell for subsequent readout. The chip has been tested at 10MHz read-out frequency corresponding to a frame rate (read-out time per cluster) of 280μs. In this condition a source rate of 1kHz is possible. Clock drivers, bias circuitry, trigger output & analog buffer are placed on the left- and right-hand sides of the chip. By the point of view of amplification, shaping and sampling
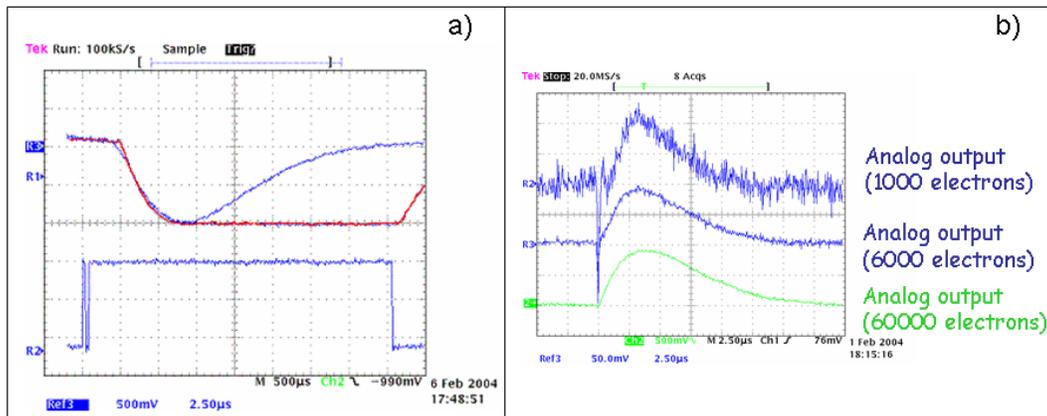
Figure 3: Signals at the analog out obtained in *Hold* and *Track mode* (a) and for three different value of input charge at 100 mV/fC amplifier gain (b).

of the analog signal the electronics chain is like the previous prototype. Fig.6 shows a photo of both chips bonded to their respective packages (left side) and an enlarged view on the large area ASIC. A complete set of tests has been performed on the chip. A noise level of ∼100 electrons (rms) has been measured also for this prototype. Fig.7 shows a photo of the large area ASIC mounted on the control motherboard.

3   The detector assembly

The same micro-mechanics components developed for the small area chip prototype have been used also for the large area chips. Two complete Gas Pixel Detectors of less than 1cm³ have been built. A drawing of all the mechanical details (spacers, GEM, entrance window) is shown in fig.8. The GEM has a standard thickness of 50μm and holes of 50μm diameter at 90μm picth on a triangular pattern. A 25μm thick Mylar foil (aluminized on one side) has been used for the entrance window. The absorbtion gap (drift region) is about 6mm thick while 1mm thick spacer defines the collection gap between the lower GEM side and the pixel matrix on the top metal layer of the chip. The photos of fig.9 show some phases of the assembly of the top section of the detector over the small area chip. Typical voltages of -1kV on the drift electrode, ∼ 400V through the GEM (-500V on top of the GEM) and ∼0V on the collecting pads have been applied during the tests. In these conditions the detector operates at gas gain of ∼1000.
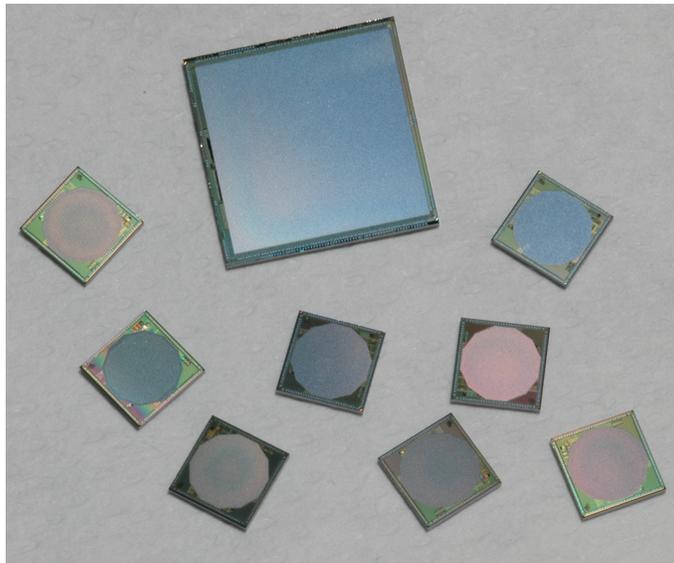
Figure 4: The photo of both bare prototypes shows the large increase in active area of the new chip.

4 Test results and applications

The first application of this new detector is for an Astronomical X-ray polarimeter in the low energy band 1-10keV. The aim of this application is to reconstruct the photoelectron track produced in the gas by the incoming X-ray (fig.10). The measurement of an asymmetry in the angular distribution of the photoelectrons tracks allows to estimate the polarization angle of the parent X-ray. The photoelectric effect is in fact very sensitive to photon polarization: the differential cross section for linearly polarized photons has a maximum in the plane orthogonal to the direction of the incoming photon and varies with the polar angle θ and the azimuthal angle ϕ as follows:

$$\frac{d\sigma}{d\Omega} = r_0^2 Z^5 \alpha^4 \left(\frac{m_e c^2}{hv}\right)^{\frac{7}{2}} \frac{4\sqrt{2}\sin^2\theta\cos^2\phi}{(1-\beta\cos\theta)^4}$$

Photoelectrons are therefore preferentially emitted in the plane orthogonal to the photon direction, with a $\cos^2\phi$ modulation arount the direction of the Electric Field vector (the Polarization vector). By reconstructing the photoelectron tracks projected onto the finely segmented collection plane of the Gas Pixel Detector and, in particular,the angular distribution of the initial part of the tracks, information on the degree and angle of polarization of astronomical sources can be derived. The morphology of a real track obtained by illuminating with a low energy radioactive source (5.9keV X-ray from ^{55}Fe) the detector mounted on the 2K pixels chip is shown in fig.11. The small cluster due to the Auger electron and the initial part of the track are well distinguishable from the larger Bragg peak. Examples of real track as reconstructed with the detector mounting the 22K pixel chip are shown in fig.12.
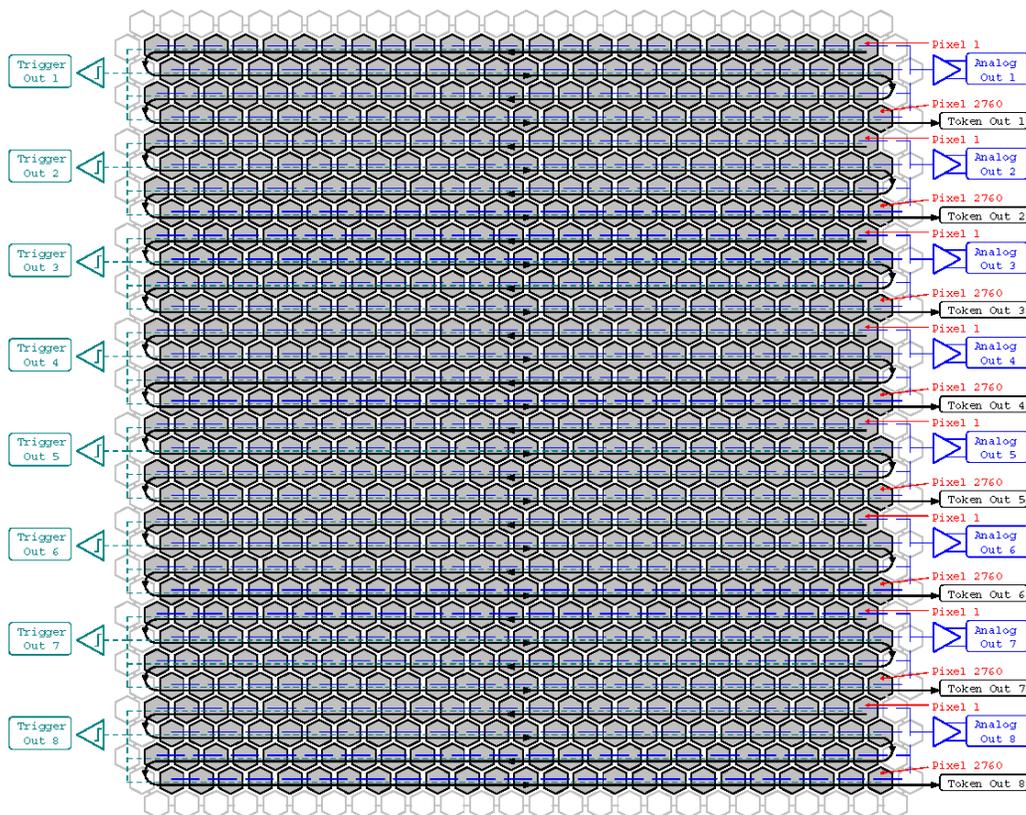
Figure 5: ASIC simplified pixel layout and serial readout architecture (actual number of pixels is larger than shown).

5   Conclusions

A system in which the GEM foil, the absorption gap and the entrance window are assembled directly over a CMOS chip die has been developed. The ASIC itself becomes at the same time, the charge collecting anode and the pixelized read-out of a Gas Pixels Detector. The full electronics chain and the detector are now completely integrated. At a gain of 1000 a good sensitivity to the single primary electron detection is reached. No problems have been envisaged up to now in operating the system under HV and in gas environment. This read-out approach has the advantage, respect to similar ones (TFT [5]or CCD[6] read-out) of being fully asynchronous and externally triggerable. An astronomical application in X-ray Polarimetry has been presented. Nevertheless, depending on pixel and die size, electronics shaping time, analog vs. digital read-out, counting vs. integrating mode, many others applications can be proposed. For example, at the 10th Vienna Conference on Instrumentation, a similar approach using an existing CMOS chip (MediPix2) coupled to two different types of gas amplifying structure (a triple GEM and a Micromegas mesh)
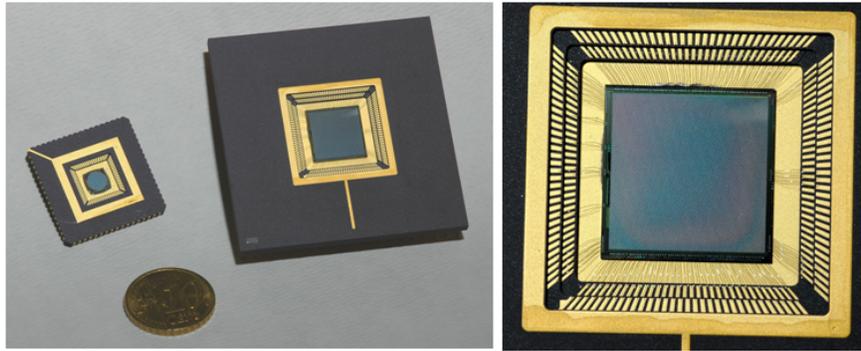
Figure 6: Photo of the two prototypes bonded to their ceramic package (left). Close-up of the 22k pixels chip (right).
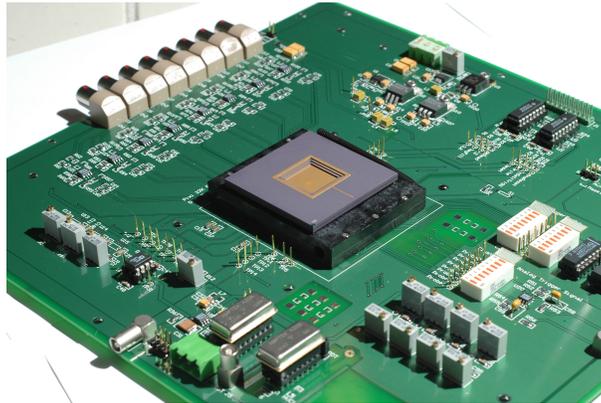
Figure 7: Photo of the large area ASIC mounted on the control motherboard.

has been presented for a TPC application [7]. Our final design will have around 100k channels and 50μm pixel size. This new chip implementation will be realized in 0.18μm CMOS technology. This would open new directions in gas detector read-out, bringing the field to the same level of integration of solid state detectors.
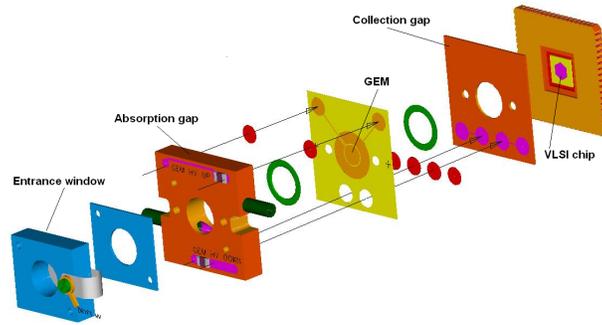
Figure 8: Mechanical details of the top section of the detector.
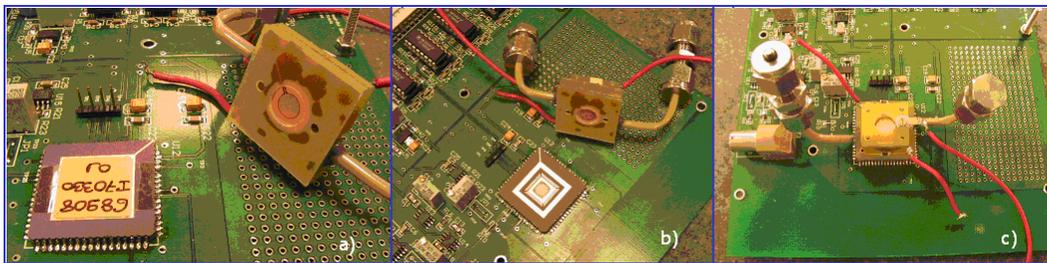
Figure 9: Assembly phases of the MPGD over the chip: a) all the mechanical details of the top section of the detector are glued together while the chip is still protected by a metallic cover, b) the chip is exposed and the mechanics glued upon it, c) the MPGD is ready for test.
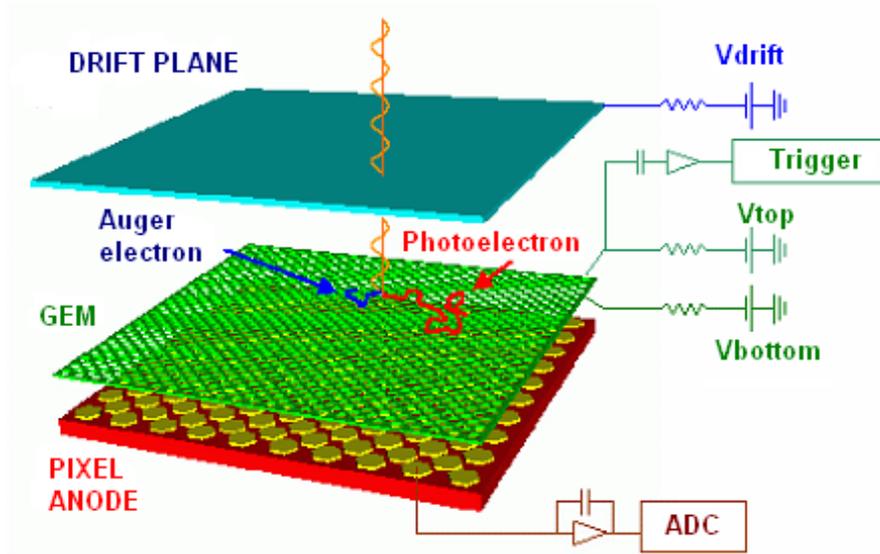
Figure 10: Polarization information is derived from the tracks of the photoelectron, imaged by the finely subdivided collection plane of the gas detector.
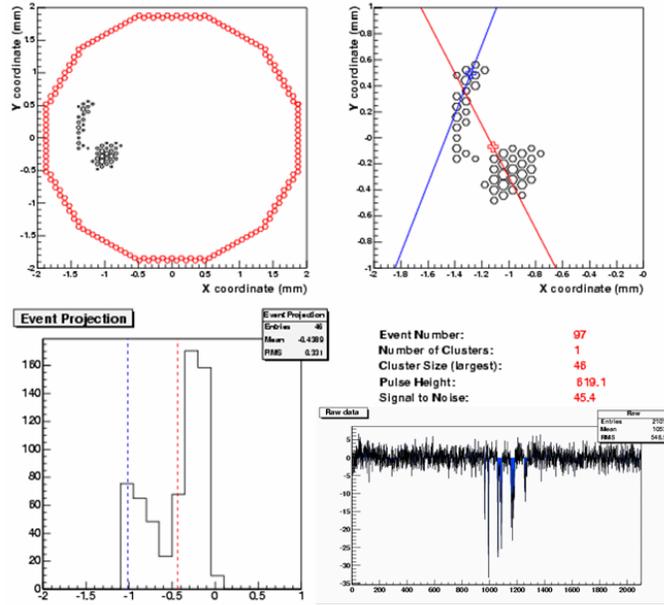
Figure 11: Reconstructed track of a 5keV photoelectron. A two step reconstruction algorithm is used([3],[4]): red line, first step; blue line, second step. The initial direction is assumed to be that one indicated by the blue line. The plot of the raw signals of all the channels for the same event (lower left side) shows the optimal signal to noise ratio obtained with this detector. (Read-out frequency 5 MHz, gas mixture 80% Neon, 20% DME, 6mm absorption gap
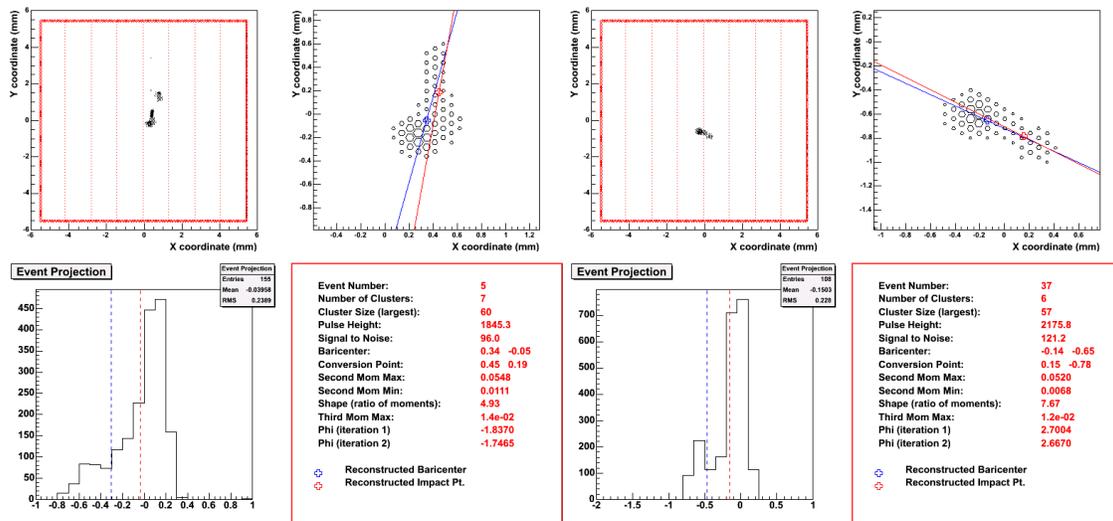
Figure 12: Reconstructed tracks of 5keV photoelectrons. (Read-out frequency 10MHz, gas mixture 50% Neon, 50% DME, 3cm absorption gap)

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