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Millimeter-Wave Avalanche Noise Sources based on p-i-n Diodes in 130 nm SiGe BiCMOS Technology: Device Characterization and CAD Modeling

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ABSTRACT Integrated noise sources (or hot loads) are essential to enable precise gain and noise figure Built-In Test Equipment (BITE) measurements. The present paper describes a millimeter-wave, solid-state noise source implemented in a standard, 130-nm Silicon-Germanium (SiGe) Bipolar-Complementary Metal Oxide Semiconductor (BiCMOS) process. This device is based on a p-i-n (varactor) diode that has two states: a cold state, when it is off, and an hot state when the diode is driven into avalanche breakdown. Two noise diodes with 10 and 20 square microns area have been fabricated and experimentally characterized. The measurements highlight a breakdown voltage is close to 10.7 V, whereas Excess Noise Ratio (ENR) equal to 16 dB (10 square microns diode) and 19 dB (20 square microns diode) are observed at 40 GHz, for a current density of 0.1 mA per square micron. For the first time the ENR is studied as a function of the physical device temperature, showing a slight decrease of -0.008 dB/K as the temperature increases from 298 to 358 K. An accurate modeling of the noise source is finally provided through a small-signal equivalent circuit that can be easily implemented into Computer Aided Design (CAD) tools. This contains some modifications with respect to the original Gliden and Hines model. The obtained results enable the employment of p-i-n avalanche noise diodes for the automatic characterization of integrated circuits in the production environment, as well as for the calibration of millimeter-wave receivers and radiometers during their operational life.

INDEX TERMS microwave noise sources, avalanche noise, noise diodes, Built-In Test Equipment (BITE).

I. INTRODUCTION

A Telecommunication major step is expected in the near future with a deep impact on automotive, naval, aeronautic and space industries. Communication systems based on 5G and 6G standards will be on the market in 10 years with unprecedented performance in terms of data rate, flexibility and coverage. These systems will use Multiple-Input-Multiple-Output (MIMO) radio terminals and active antennas with real time beam steering capability [1]. All the available frequency bands up to millimeter-waves (mm-waves) will be exploited in order to improve both speed and link robustness. Self-driving electric cars, robotic ships [2], drones and constellations of nano-satellites (CubeSats) will be used for mobility, logistic and monitoring purposes, as well as to bring the Internet to remote places, perform meteorological forecasts and many other commercial and scientific missions [3], [4]. In all these applications an impressive amount of miniaturized, low-cost and high reliability electronics is required. Silicon Systems-on-Chips (SoC) will be extensively adopted to this purpose since nanoscale Complementary Metal Oxide Semiconductor (CMOS), Silicon-Germanium (SiGe) Bipolar-CMOS (BiCMOS) and Silicon-Carbide (SiC) processes allow for state-of-the-art integration densities of the digital sub-systems, and have the capability

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to cover both the mm-wave frequency range (SiGe) and the high power market segment (SiC).

Despite to the development of modern microelectronic technologies, a considerable fraction of the production costs is associated to the complexity of tests on these new radio chips. On one hand, each fabricated chip should be tested in order to guarantee for the specifications in life-critical or mission-critical applications, e.g., self-driving cars, drones and nano-satellites. On the other hand, the time spent for extensive tests during production and the use of expensive millimeter-wave instruments (vector network analyzers, spectrum analyzers, noise figure analyzers, etc.) have remarkable impact on the final costs of the integrated circuits itself, estimated between 25% and 50% of the total cost, if every chip is tested.

A possible solution to these problems is the usage of Built-In Test Equipment (BITE), i.e., miniaturized measurement instruments, integrated in the Silicon (Si) chip together with the mm-wave radio components [5]. With this new methodology, the measurement cost and time can be dramatically reduced as no expensive instrument is needed, and each chip can communicate the results via a digital interface. Furthermore, tests can be repeated when the chips are mounted on their target application, in order to check the electronics also during the operative life.

In this perspective, the adoption of avalanche noise diodes in radio frequency on-chip BITEs is a novel and scarcely investigated research topic. With these devices it is possible to perform simultaneous noise figure and gain measurements, two tests that are very important for future 5G and 6G receivers. To this purpose the noise diode is coupled to the receiver input in such a way as to inject a known amount of noise power [6], and the above measurements are based on the Y-factor method [7]. Such an approach is quite similar to those adopted for the calibration of radio astronomy receivers and microwave radiometers [8]-[11] and, recently, has been applied to a fully integrated 60 GHz radiometer fabricated in SiGe BiCMOS technology [12]. Finally, noise diodes could be used in cryptography BITEs to realize high-speed true random numbers generators [13]. For the development of all these BITEs, however, noise diodes should be available in mainstream nanoscale CMOS and SiGe BiCMOS processes.

Avalanche noise diodes have been introduced in the late 1960 and are based on pn junctions in reverse breakdown [14]-[20]. They can generate two noise power levels by the application of an external bias voltage. When the diode is not biased, it can be assimilated to a resistive termination at a temperature that, in a first approximation, is close to the physical temperature of the junction (cold state). On the contrary, when the diode is driven into breakdown, an avalanche discharge takes place generating a large amount of noise power (hot state). Typical hot temperatures produced by these devices are in the order of 10^3 to 10^5 K.

In 2016 the first avalanche noise diode in a 90-nm commercial CMOS technology was demostrated and modeled [21]. The device exploited the source-drain to bulk pn junction of a standard NMOS transistor and was able to produce an Excess Noise Ratio (ENR) of 25 dB at 24 GHz, when biased with a current density of $0.14\,\mathrm{mA}/\mu\mathrm{m}^2$. In 2019 the avalanche from a Schottky diode built in 55-nm SiGe BiCMOS technology was reported [22]. The study was refined in 2020 both in terms of experiments and modeling, achieving a record ENR of 20 dB in a frequency range up to 260 GHz [23]. Finally, in 2020, another avalanche noise source is demostrated using the collector-base junction of a SiGe Heterojunction Bipolar Transistor (HBT) in a 130-nm SiGe BiCMOS process [12]. This device attains a 18.7 dB ENR at 60 GHz.

In this paper, for the first time, the microwave avalanche noise generated by a p-i-n diode is considered. The device, implemented in a 130-nm commercial SiGe BiCMOS technology, is a varactor diode: a standard cell already available in the Process Design Kit (PDK). Two diodes with a junction area of 10 and $20\,\mu\mathrm{m}^2$ have been fabricated and experimentally characterized. They can be driven into breakdown by applying a reverse voltage greater than 10.7 V and, with a $0.1\,\mathrm{mA}/\mu\mathrm{m}^2$ avalanche current density, they show an ENR of 16 and 19 dB respectively at 40 GHz. Although it is known that the avalanche noise generation mechanism is a high stability process [24], there are no study about the ENR behavior as a function of the device temperature. To fill this gap, the ENR is measured at both ambient temperature (298 K) and at 85 °C (358 K). It is demonstrated that the ENR slightly decreases with the temperature with a sensitivity of about -8×10^{-3} dB/K.

In order to design future noise BITEs, an accurate Computer Aided Design (CAD) model of the diode is needed. To this purpose, the equivalent circuit developed in [21] and [25] is adapted to the studied p-i-n diodes. The model, compatible with modern software tools, is able to predict both the diode impedance and the generated noise as a function of the applied bias. Furthermore, a modification of the basic Gliden model [14], [15] is proposed to account for the low-frequency impedance behavior. This has been observed in the experiments, and could be related to microplasma and electro-thermal coupling effects that were originally described by Haitz in [18], [20].

The importance of the obtained results, together with those recently published by other research groups, is that it is possible to achieve a comprehensive view on avalanche noise diodes that are compatible with commercial CMOS and BiCMOS technologies: pn junctions, Schottky diodes, collector-base juntions and p-i-n diodes. All these devices can be used for the effective implementation of on-chip noise BITEs. In summary, the original elements of the present paper are:

- first characterization of a p-i-n diode avalanche noise source in a commercial 130-nm SiGe BiCMOS processes;
- first study of the ENR stability as a function of the physical device temperature;
- accurate CAD modeling of both impedance and noise by means of an equivalent circuit that is compatible with modern software tools;

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- empirical modeling of the low-frequency impedance behavior (microplasma and electro-thermal coupling).

II. NOISE DIODES

The devices used in the experiments, realized using the double epi concept, are represented in Fig. 1. According to [26], [27], the cathode region of the p-i-n diode (K in Fig. 1) is formed by implanting the buried subcollector layer (n+ in Fig. 1) of a High-Voltage (HV) bipolar transistor. Then, the n epi-layer (n in Fig. 1) and the intrinsic epi-layer (i-layer in Fig. 1) are grown in subsequent steps. Finally a p+ polysilicon (p+ poly in Fig. 1) electrode is deposited and patterned to realize the diode anode (A in Fig. 1).

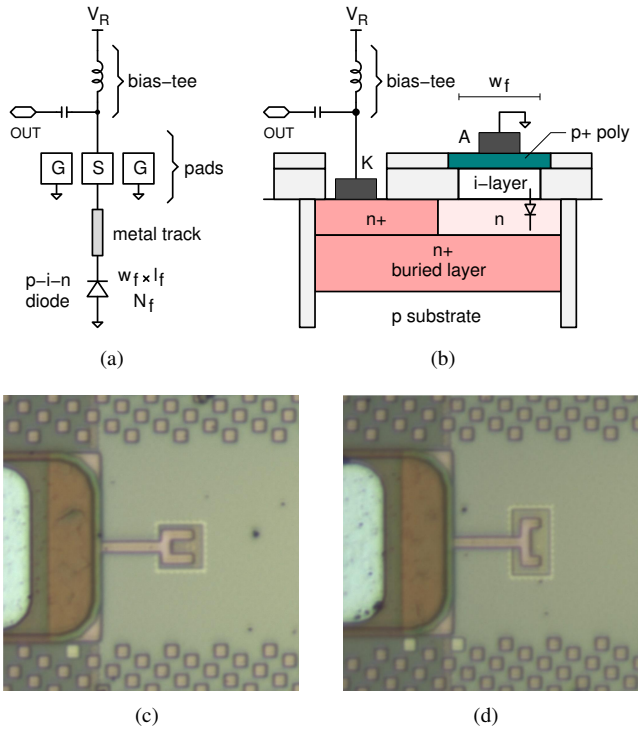

FIGURE 1. Integrated mm-wave p-i-n noise diode in 130-nm SiGe BiCMOS technology. Schematic (a), structure of the device (b), fabricated prototypes: $10\,\mu\text{m}^2$ area (c) and $20\,\mu\text{m}^2$ area (d). The diode is derived from the collector region of a high-voltage bipolar and is constituted by N_f fingers in parallel. The width of each finger is $w_f = 1\,\mu$m, whereas its length is $l_f = 5\,\mu$m. The $25\,\mu$m long metal track connecting the diode to the pad can be assimilated to a short transmission line section: its effects, together with that of the pad, are de-embedded from the measurements (see below).

The intrinsic layer is obtained by counterdoping, and it was originally conceived with two purposes: first, it is used to reduce the junction capacitance of the diode, since it is typically employed as a mm-wave varactor. Second, such a layer is adopted to increase the breakdown voltage of the device. The diode is isolated by shallow/deep trenches, while the substrate is kept at ground potential by means of a p+/p guard ring (not shown in the figure). Each device is constituted by N_f fingers in parallel: their width is $w_f = 1\,\mu$m, whereas their length is $l_f = 5\,\mu$m. In particular 2 and 4 fingers are used to form the $10\,\mu\text{m}^2$ and $20\,\mu\text{m}^2$ devices, respectively.

The test chip ground network is implemented short-circuiting together all the metal planes from M1 to M4; this in order to minimize the parasitic ground inductance. The diode is connected to the signal pad by a track at M6 featuring a $25\,\mu$m length and a $2.4\,\mu$m width. The pad size is $58 \times 75\,\mu\text{m}^2$. The track behaves like a short transmission line section loaded by the pad capacitance, and its effect is de-embedded from the impedance measurements by a suitable on-chip calibration procedure (see Sec. IV). The vertical connections are constituted by contacts (from the diode active regions to M1) and by a stack of vias (from M1 to M6). In order to reduce both the parasitic resistance and inductance, several contacts and vias in parallel are used. The total resistances of these connections are 0.56 and $0.28\,\Omega$ for the 10 and the 20 square microns diodes respectively.

III. MODELING

The small-signal equivalent circuit of a diode in avalanche region is depicted in Fig. 2(a). According to [14], [25] it consists of 6 elements, namely: C_a, L_a, Z_d, R_j, R_s and $\bar{i}^2_{na}$. In particular, C_a and L_a describe the avalanche region of the diode, whereas Z_d models its drift zone, [14], [15]. The resistors R_j and R_s represent, respectively, the depletion zone resistance [25] and the contact resistance. Finally, the current source $\bar{i}^2_{na}$ accounts for the avalanche noise generation.

In the following discussion only the modifications with respect to the basic Gliden and Hines model will be addressed. A complete description of this model can be found in [21] but, for the sake of readers, a summary with the basic equations is reported in the Appendix A.

The first modification concerns the ionization coefficient derivative with respect to the E-field, α'. According to [15, p. 161] and [19, p. 3380] it is directly related to the reverse voltage V_R:

$$\alpha' = \frac{m}{\kappa\, V_R} \tag{1}$$

were $m_0 = m/\kappa$ is a bias independent parameter. Using this relationship it is possible to reduce the model complexity, since there are less parameters depending on the reverse voltage.

The second modification is related to the contact resistance R_s. This is empirically modeled to account for microplasma and electro-thermal coupling effects [18], [20], that are responsible for a low-frequency resistance increase:

$$R_s = R_0 + \frac{R_i}{1 + (\omega\,\tau_i)^\gamma} \tag{2}$$

where ω is the angular frequency, R_0 is the contact resistance at high frequency, $R_0 + R_i$ is the same resistance at DC and τ_i represents a suitable time constant. In this relationship R_0 and R_i are bias-dependent parameters, typically increasing at low avalanche currents. The transition between low- to high-frequency is determined by the exponent γ that, in the present paper, is assumed equal to 2.

Avalanche diode models are not available in modern CAD tools, thus circuit simulations involving this kind of devices

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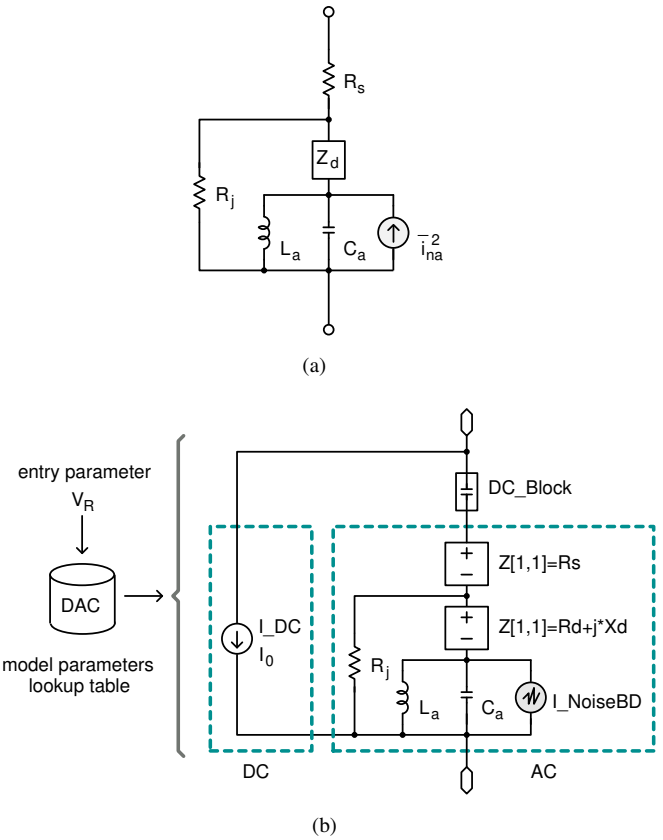

FIGURE 2. Small-signal equivalent circuit of the p-i-n diode in avalanche region (a) and corresponding implementation within ADS of Keysight Technologies (b). The model parameters are described in the text. The current source $\bar{i}^2_{na}$ accounts for the avalanche noise generation within the device. In ADS this is obtained using the instance `I_NoiseBD`.

are not possible. The above equivalent circuit overcomes this limitation, and in order to prove its accuracy, it is implemented within ADS of Keysight Technologies, along with the corresponding equations, from (9) to (13), described in Appendix A. Fig. 2(b) shows that the ADS avalanche diode schematic is based on a Data Access Component (`DAC`) instance. The DAC behaves as a lookup table whose entry variable is the reverse voltage V_R. It contains the measured relationship between the reverse voltage and the avalanche current I_0 (which is a nonlinear relationship) and all the bias-dependent device parameters.

The current I_0 is taken from the lookup table and applied to a DC current source. In this way I_0 can be used as the reference current for the computation of the avalanche noise. To this purpose the instance `I_NoiseBD` is adopted since, with suitable parameters, it generates the noise current spectral density given by (13). The other equivalent circuit elements are computed, as a function of I_0, by equations. First, the avalanche frequency ω_a is evaluated using (9). Then, such a value is used to compute L_a, by reversing the first equality in (9), and Z_d with (11). The latter, separated in real and imaginary parts, is applied to an equation-based one-port block (instance `Z1P_Eqn`), which is how ADS models an impedance in the frequency domain. R_s is evaluated according to (2) and inserted in ADS with another `Z1P_Eqn` block.

The advantage of the above approach is that ADS can be used to simulate both the impedance and noise within a single framework. In particular, the AC simulator is employed for the computation of the spectral noise power (i.e., the noise power in a unit bandwidth), which is evaluated from the noise voltage across a reference resistor R_ℓ. Afterward, the equivalent noise temperature T_H can be found dividing the spectral noise power by the Boltzmann constant, see (17).

In order to describe the noise source behavior, the Excess Noise Ratio (ENR) is used. This parameter is defined by:

$$\mathrm{ENR} = \frac{T_H - T_C}{T_0} \tag{3}$$

T_H being the hot temperature (noise source switched on), T_C the cold temperature (noise source switched off), and $T_0 = 290\,\mathrm{K}$ the IEEE standard temperature. Note that, according to [7, p. 19], T_H and T_C should be "effective" noise temperatures. For this reason $R_\ell = 50\,\Omega$ (nonreflecting load assumption) and the simulator does not evaluate its thermal noise (nonemitting load assumption, equivalent to consider the load resistor at 0 K). The ENR is finally obtained as ENR $\approx T_H/T_0 - 1$, since $T_C \approx T_0$. Such an approach is used in all the presented results.

In the off condition the diode is modeled as the resistance R_s in series with the junction capacitance C_j. Considering Fig. 2(a), for $I_0 \to 0$ the equivalent circuit reduces to R_s in series with C_a and C_d, since both L_a and R_j go to infinity. In particular Z_d reduces to the drift capacitance C_d for $\omega_a \to 0$, i.e., in the considered limit case, see Appendix A. As a consequence, if the series between C_a and C_d is adjusted to equate C_j for a zero avalanche current, the diode model in the off condition is obtained as a limit case of the one in avalanche condition. Experimentally we found that, at zero bias, C_j is equal to 17 and 29 fF for the $10\,\mu\mathrm{m}^2$ and $20\,\mu\mathrm{m}^2$ devices respectively. Such a value is about 100% higher than that obtained using the l_a and l_d values reported in Sec. V. This, however, can be explained observing that the depletion zone of the diode, at zero voltage, is thinner with respect to the one in the avalanche (breakdown voltage around 10.7 V).

IV. METHODS

The experimental characterization of the fabricated avalanche diodes requires that both the impedance and the generated noise are measured at different frequencies, bias conditions and temperatures. In order to minimize the systematic errors due to the experimental setup (parasitic effects are particularly severe at mm-wave frequencies), on-wafer measurements were used extensively. To this purpose, in all the cases, the test chips were contacted by means of a probe station equipped with micro-manipulators and $100\,\mu$m pitch, Ground-Signal-Ground (GSG) coplanar probe tips (up to 40 GHz). The experiments were repeated on four chips of the same wafer lot by two laboratories, namely the

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Infineon Technologies laboratory at Villach, Austria and the University of Perugia laboratory at Perugia, Italy.

The impedance measurements were performed with two Vector Network Analyzers (VNA): the Rohde & Schwarz ZVA50 at Infineon and the Keysight PNA N5230A at the University of Perugia. In both cases the bias-tee internal to the VNA was used to bias the diodes and to drive them into avalanche. The VNAs were calibrated by means of a Short-Open-Load-Through (SOLT) procedure using the CS-5 substrate from GGB Industries. This way the reference plane is exactly located at the probe tip contacts.

Fig. 3 shows the small-signal equivalent circuit of the avalanche p-i-n diode including the pad and the metal track used for connection purposes. After the above SOLT calibration the reference plane is set at port 1, this meaning that the VNA measures the impedance of the whole network. To recover the diode impedance, the reference plane has to be moved to the internal port T of Fig. 3(a). This is done by de-embedding the pad and metal track parasitics from the impedance measurements, i.e., the Y_p network depicted in Fig. 3(a). To this purpose two additional test structures are fabricated on the diode test chip. The first structure is the open pad represented in Fig. 3(b), i.e., the pad and the metal track left open at the diode location. The second structure is the shorted pad illustrated in Fig. 3(c), i.e., the pad with the metal track short-circuited to ground at the diode location. The measurements of these two test structures are then used to derive, by a best fitting approach, an equivalent circuit representation of the network Y_p, see Fig. 3(a). In particular, the metal track can be assimilated to a short transmission line section: as a consequence it is modeled with the series inductance L_p, and with the lossy network R_p, R_k and L_k, accounting for the skin effect. The pad is represented by capacitance C_p in series with R_{sub}, the latter modeling the power dissipation in the substrate. These parameters are reported in the caption of Fig. 3 and are capable to accurately describe the Y_p behavior up to 40 GHz.

For the noise characterization, the setup illustrated in Fig. 4 is used. The system is composed of a bias tee (Marki Microwave BTN2-0050), a Low Noise Amplifier (A1) and a spectrum analyzer with internal preamplifier (Rohde & Schwarz FSW-50, up to 50 GHz) for the measurement of the spectral noise power densities. Two different external LNAs are used, namely the ZVA-213-S from Mini-circuit, with 25 dB gain and 3 dB noise figure from 1 to 12 GHz, and the ERZ-LNA-1800-4000-15-4 from Erzia, with 15 dB gain and 5 dB noise figure from 10 to 40 GHz. The data obtained with the two LNAs are then combined in order to give a full 1 to 40 GHz noise characterization. The system is calibrated by means of a reference noise source (Noisewave NW346KA). A variable power supply in series with a resistor $R_b = 470\,\Omega$ is used to bias the diode. Two precision multimeters are adopted to measure both the avalanche current I_0 and the reverse voltage V_R. The experimental setup has two modes: a measurement mode when B is connected to A and a calibration mode when C is connected to A.

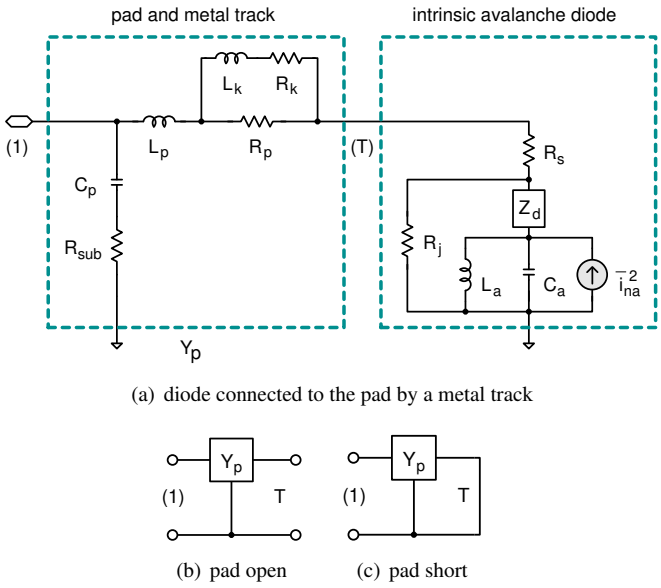

FIGURE 3. Small-signal equivalent circuit of the p-i-n diode in avalanche region connected to the pad (a) and determination of the pad parasitics through open (b) and short (c) impedance measurements. C_p and R_{sub} represent the pad parasitic capacitance and the substrate resistance respectively, L_p is the parasitic inductance of the metal track, whereas R_p, R_k and L_k are used to describe its power losses (and the skin effect). To determine these parameters two calibration structures are implemented on-chip, with the internal port T left open or shorted to ground. Y_p parameters: $C_p = 32\,\text{fF}$, $R_{sub} = 6\,\Omega$, $L_p = 20\,\text{pH}$, $R_p = 0.5\,\Omega$, $R_k = 0.9\,\Omega$, $L_k = 50\,\text{pH}$.

The excess noise ratio of the Device Under Test (DUT), i.e., of the avalanche noise diode, is experimentally evaluated using the Y-factor method by:

$$\text{ENR}_D = \frac{(Y_D - 1)}{(Y_R - 1)}\,\text{ENR}_R \tag{4}$$

where, for each frequency, ENR_D is the excess noise ratio of the DUT (subscript D), ENR_R is that of the reference noise source adopted for the system calibration (subscript R), and Y_j, with $j = D, R$, are the corresponding Y-factors. The derivation of such a relationship is reported in the Appendix B for the sake of readers.

According to the definition of "effective" noise temperature, the Y-factors should be evaluated considering the power spectral densities emerging from the noise source when it is connected to a nonreflecting load. If these quantities are defined to as N_i^j, with $i = H, C$ (Hot and Cold measurements) and $j = D, R$, we have:

$$Y_j = \frac{N_H^j}{N_C^j} \tag{5}$$

In general, with a practical setup, the "nonreflecting load" assumption is not verified. This means that the mismatch between the noise source (reference noise source or DUT) and the measurement system should be corrected. The measured

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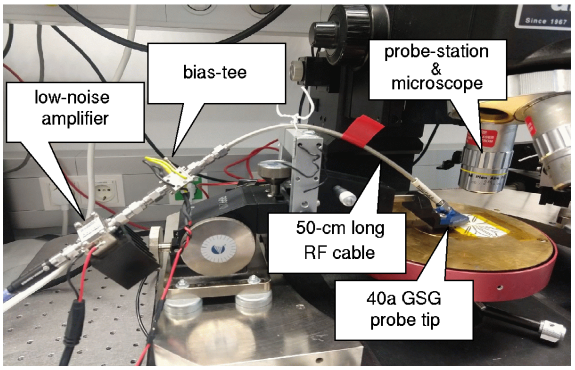
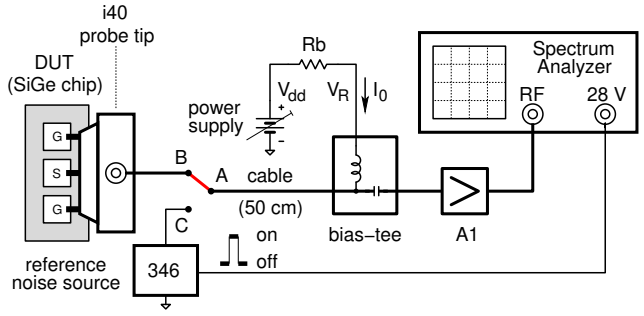


(a)



(b)

FIGURE 4. Experimental setup used, at Infineon, for the on-chip ENR characterization of the fabricated diodes: photograph (a) and schematic (b). The measurement chain is composed by a bias tee, a low noise amplifier (A1) and a spectrum analyzer (Rohde & Schwarz FSW-50, up to 50 GHz) with internal preamplifier. The system is calibrated by means of a reference noise source (Noisewave NW346KA). The p-i-n avalanche noise diode (DUT) is contacted through a GSG probe tip with a $100\ \mu$m pitch (Infinity Probe model i40, up to 40 GHz). A variable power supply in series with a resistor $R_b = 470\,\Omega$ is used to bias the diode. Two precision multimeters are adopted to measure either the avalanche current I_0 and the reverse voltage V_R. There are two modes: measurement (B – A), calibration (C – A).

spectral noise power densities, S_i^j, are thus directly related to the N_i^j, used for the Y-factor, by:

$$N_i^j = \frac{S_i^j}{M_j^i} \tag{6}$$

M_j^i being the mismatch factors defined in [7, p. 21]:

$$M_j^i = \frac{1}{\left|1 - \Gamma_j^i\,\Gamma_j^{rec}\right|^2} \tag{7}$$

In this expression Γ_j^{rec} is the reflection coefficient of the measurement system (i.e. of the noise receiver) and Γ_j^i is that of the reference or DUT noise sources (j index) in each of the two states (hot or cold, i index). These coefficients have been carefully measured with the Vector Network Analyzer at the probe tip reference plane (exploiting a second probe tip), and have been used to correct all the reported ENR measurements. In calibration mode ($j = R$) these reflection coefficients have been measured at point A of Fig. 4 for the receiver, and at the output coaxial connector of the reference noise source, point C of Fig. 4.

Finally, to verify the above noise measurements, a second setup based on a down-conversion receiver architecture, was implemented at the University of Perugia. Such a setup is described in the Appendix C, along with a comparison among the results obtained at the two test facilities. In both the cases (Infineon and University of Perugia labs.) the probe tip attenuation as a function of frequency is considered in the data post-processing, as suggested in [22].

V. RESULTS

This section is devoted to the quantitative data presentation and discussion. These are constituted by the experimental results, the comparison with the developed model, and the tables of model parameters. The section starts with the static curves of the avalanche diodes and then illustrates the impedance results. The diode ENR and its variation with the temperature is described in two following subsections. A comparison with the State-of-the-Art is finally proposed.

A. STATIC CURVES

The measured avalanche current as a function of the reverse voltage applied to the fabricated diodes is reported in Fig. 5. These values have been obtained at thermal equilibrium, and thus account for the junction temperature increase due to the self power dissipation, [28].

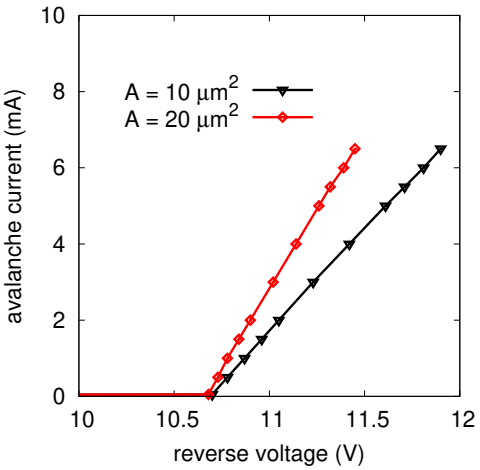


FIGURE 5. Measured avalanche current of the p-i-n diodes as a function of the reverse voltage applied to the junction. The experiments are repeated for devices with a junction area of 10 and $20\ \mu\text{m}^2$ respectively. The breakdown voltage is about 10.7 V in both cases. The measurements are taken at 298 K.

The static curves of Fig. 5 are well represented by the following piecewise linear model:

$$I_a(V_R) = \begin{cases} g_a\ (V_R - V_b) & V_R \geq V_b \\ 0 & \text{elsewhere} \end{cases} \tag{8}$$

where I_a is the avalanche current, V_b is the breakdown voltage and g_a is the slope factor. With a curve fitting procedure it is found that $V_b = 10.68$ V while g_a is about 5.4 mA/V and 8.4 mA/V for the $10\ \mu\text{m}^2$ and $20\ \mu\text{m}^2$ diodes respectively.

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The current-voltage curve in the direct region has also been measured, verifying that it is accurately described by the PDK models available for these p-i-n diodes.

B. IMPEDANCE RESULTS

The fabricated p-i-n diode prototypes have been characterized up to mm-wave frequencies. First, the diode impedance is measured for each of the two implemented devices with different junction area, and for several biasing conditions in the avalanche regime. As described in the previous section, these experiments were carried out with a probe station and a VNA in order to obtain reliable and high accuracy data. The probe station closeup is illustrated in Fig. 6.

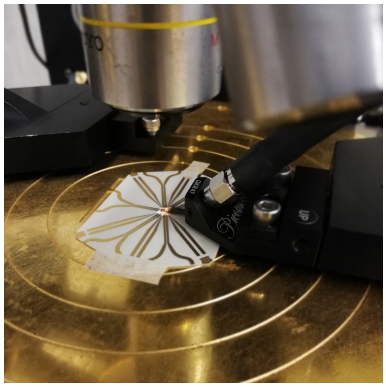

FIGURE 6. Image of the p-i-n diode test chip during the on-wafer impedance measurement. The picture is taken under the Alessi REL-4500 probe station: it is possible to note to note the Picoprobe 40a $100\,\mu$m pitch GSG probe tip touching the die (University of Perugia laboratory).

Then, the contribution of both the signal pad and the metal track connected to the diode were de-embedded from the measurements in order to set the reference plane at the internal port T of Fig. 2(a). The resulting impedances are reported in Fig. 7 for the $10\,\mu\text{m}^2$ diode and in Fig. 8 for the $20\,\mu\text{m}^2$ device. Both figures represent the real and the imaginary parts of the intrinsic diode impedances for three avalanche currents, namely: 1, 1.5 and 2 mA. A resonance at the avalanche frequency is apparent in all the cases, as well as the electronic tuning effect due to the current, as described in (9). It is interesting to note that, for the same current, the smallest diode shows higher resonance frequencies since $f_a = \omega_a/2\,\pi$ is a function of the current density square root.

After the impedance measurements, the equivalent circuit parameters of the avalanche p-i-n diode are extracted by the fitting procedure described in [25]. To this purpose the optimizer tool of Keysight ADS is adopted. Such a procedure is repeated for the two junction areas and for each bias current. The saturated carrier velocity is assumed equal to 1×10^5 m/s, as reported in [27], [29]. The extracted model parameters, divided in bias-dependent and bias-independent, are quoted in Tab. 1 to Tab. 4. Thanks to (1), only three bias-dependent parameters are needed to describe the diode impedance, namely R_j, R_0 and R_i. Note that, if the low-frequency impedance behavior is neglected, only one bias-dependent parameter (R_j) is necessary.

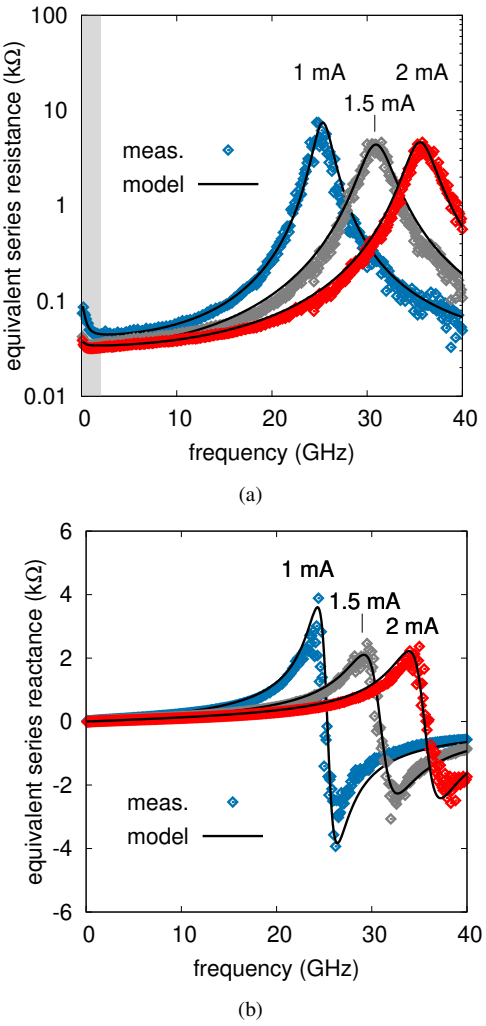

FIGURE 7. Small-signal impedance of the $10\,\mu\text{m}^2$ p-i-n noise diode in avalanche as a function of frequency: real (a) and imaginary (b) parts. The measurements are compared with the equivalent circuit simulations. The pad parasitics are de-embedded from the measurements. The model parameters are reported in Tab. 1 and Tab. 2. The real part is drawn with the y-axis in log scale to emphasize the low-frequency behavior

.

TABLE 1. Bias Dependent Parameters – $10\,\mu m^2$ Diode

V_R (V)	I_0 (mA)	J_0 (mA/μm^2)	α' (1/V)	f_a (GHz)	R_j (Ω)	R_0 (Ω)	R_i (Ω)
10.87	1.0	0.100	0.133	25.29	7445	24	50
10.96	1.5	0.150	0.132	30.85	4375	15	6
11.05	2.0	0.200	0.131	35.49	4635	15	4
11.42	4.0	0.400	0.126	49.23	5100	15	4

The equivalent circuit is then used to simulate the intrinsic diode impedance, whose results are depicted again in Figs. 7 and 8 (solid lines). The comparison highlights the capability of the model to correctly predict the impedance over a wide frequency range and at different avalanche currents. The model is within $\pm 20\,\%$ with respect to the measurements for each device size and in all the reported bias conditions.

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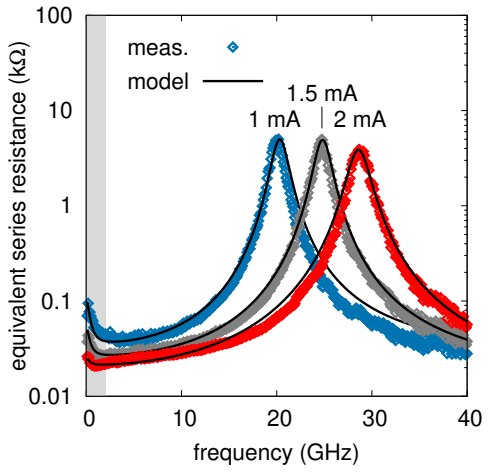
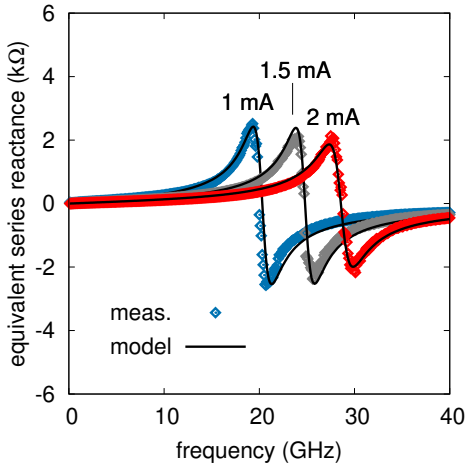


(a)



(b)

FIGURE 8. Small-signal impedance of the $20\ \mu m^2$ p-i-n noise diode in avalanche as a function of frequency: real (a) and imaginary (b) parts. The measurements are compared with the equivalent circuit simulations. The pad parasitics are de-embedded from the measurements. The model parameters are reported in Tab. 3 and Tab. 4. The real part is drawn with the y-axis in log scale to emphasize the low-frequency behavior.

TABLE 2. Bias Independent Parameters – $10\ \mu m^2$ Diode

m_0	ϵ_r	v_d (m/s)	l_a (nm)	l_d (nm)	τ_d (ps)	τ_i (ps)	τ_x (ps)
1.45	11.9	1×10^5	40	63	0.63	425	0.42

The low-frequency behavior, depicted by an increase of the impedance real part below 2 GHz is apparent, and is more significant at low avalanche currents, i.e., in the shadow area of Figs. 7(a) and 8(a). This effect, probably due to micro-plasma and electro-thermal coupling effects, has already been discussed in the scientific literature and is described here by a frequency dependent contact resistance, (2). It is important to underline that the found equation parameters R_0 and R_i provide a best fitting of both the low-frequency impedance and the low-frequency ENR response (see below).

Finally, the Smith charts of Fig. 9 represent the reflection

TABLE 3. Bias Dependent Parameters – $20\ \mu m^2$ Diode

V_R (V)	I_0 (mA)	J_0 (mA/μm^2)	α' (1/V)	f_a (GHz)	R_j (Ω)	R_0 (Ω)	R_i (Ω)
10.78	1.0	0.050	0.172	20.33	4990	24	70
10.84	1.5	0.075	0.171	24.83	4930	15	26
10.90	2.0	0.100	0.170	28.59	3870	10	4
11.14	4.0	0.200	0.166	39.95	4000	10	2

TABLE 4. Bias Independent Parameters – $20\ \mu m^2$ Diode

m_0	ϵ_r	v_d (m/s)	l_a (nm)	l_d (nm)	τ_d (ps)	τ_i (ps)	τ_x (ps)
1.86	11.9	1×10^5	60	69	0.69	425	0.48

coefficient of the avalanche p-i-n diodes for 1 and 2 mA. These coefficients are referred to the input pads, i.e., the port 1 of Fig. 3. They include both the pad and metal track parasitics and represent the diode impedance as it is seen from the external circuits. In the on condition the diodes are biased in the reverse breakdown whereas, in the off condition, the devices are at 0 V.

Above the avalanche frequency the diodes are poorly matched, and this has been considered in the noise measurement by the careful evaluation of the mismatch factors. In future applications such a problem can be mitigated by properly sizing the devices, by setting the avalanche current, and by using suitable on-chip attenuators, [30].

C. ENR RESULTS

The ENR of each diode is measured following the approach described in Sec. IV, using the setup of Fig. 4, and processing the data according through (4) to (7). As specified previously, the mismatch factors M_j^i have been carefully determined by measuring with the VNA both the diode and the measurement system impedances. The spectral noise power is corrected to account for the probe tip attenuation.

Fig. 10 reports the ENR as a function of frequency and for three biasing currents (1, 2 and 4 mA). The experimental data (represented with dots in the graphs) are compared with the model simulations (black lines) obtained with the parameters of Tab. 1 to Tab. 4. The model fitting is obtained assuming the average time between two ionizations, τ_x, equal to 0.42 and 0.48 ps for the $10\ \mu$m^2 and $20\ \mu$m^2 diodes respectively. The agreement between model and experiments is within ± 1.5dB at all frequencies.

Although the model is extracted for currents between 1 and 4 mA, the measurements extend from 0.5 to 6 mA. In order to further study the avalanche diode noise, another experiment is carried out. At the fixed frequency of 35 GHz the measured ENR is analyzed as a function of the current density. The result of this experiment is illustrated by Fig. 11, where measurements are again compared to the model. As visible, the $10\ \mu$m^2 diode behavior is very close to the $20\ \mu$m^2 one, translated by a factor 2. According to (13), indeed, the

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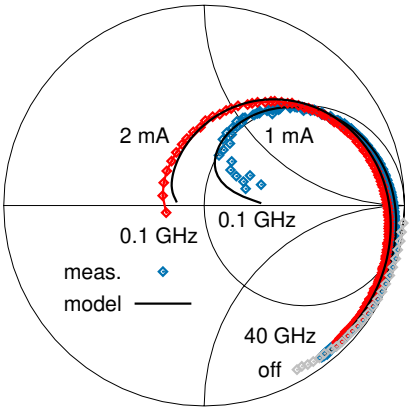
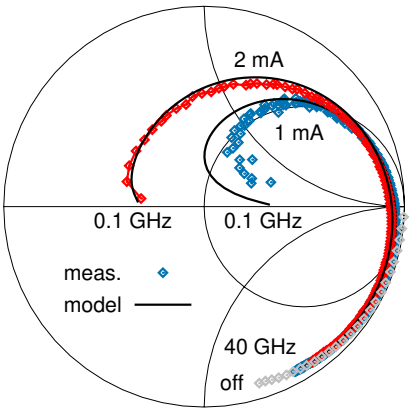
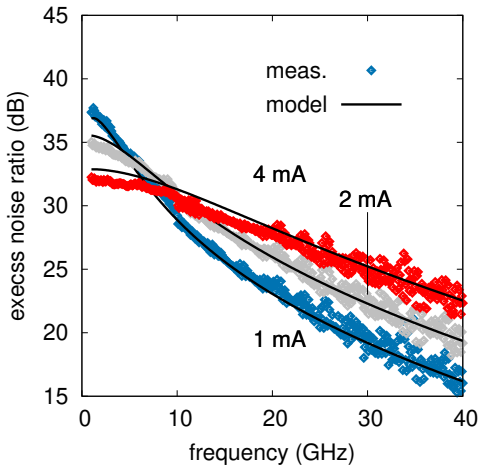


(a) $10\,\mu\mathrm{m}^2$ area

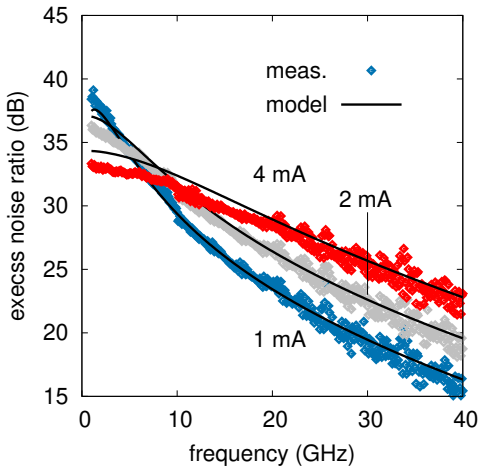


(b) $20\,\mu\mathrm{m}^2$ area

FIGURE 9. Reflection coefficients of the p-i-n avalanche noise diodes versus bias and frequency for the $10\,\mu\mathrm{m}^2$ (a) and $20\,\mu\mathrm{m}^2$ (b) device respectively. In the off condition the diodes are biased at 0 V. The measurements are compared with the proposed model and, in both the cases, pad parasitics are included (i.e. the reference plane is set at port 1 of Fig. 3).



(a) $10\,\mu\mathrm{m}^2$ area



(b) $20\,\mu\mathrm{m}^2$ area

FIGURE 10. Comparison between measured and modeled ENR versus the frequency for different avalanche current densities: $10\,\mu\mathrm{m}^2$ (a) and $20\,\mu\mathrm{m}^2$ (b) devices. The pad are included in the simulations. The deviation between model and experiments is within ± 1.5dB over the whole frequency range.

spectral current density depends on the avalanche current that, in turns, is proportional to the device area. The curves of Fig. 11 suggest that the ENR can be controlled by the avalanche current: this way more than 10 dB of dynamic is achieved.

As previously stated, the noise experiments are repeated on four chips of the same wafer lot. Considering the $20\,\mu\mathrm{m}^2$ diode at 30 GHz we get an average ENR of 18, 21.2 and 24.1 dB for an avalanche currents of 1, 2 and 4 mA respectively. In all the cases, the ENR standard deviation across the different chips is less than 0.2 dB (4.7% in linear scale).

Appendix C reports the comparison of the above noise measurements (Infineon laboratory) with those obtained at the University of Perugia. Fig. 16 confirms the previous data within a 1.3 dB overall uncertainty.

D. ENR VERSUS TEMPERATURE

The probe station at the Infineon laboratory is also equipped with an hot plate and this has been used to perform impedance and avalanche noise measurements as a function of the temperature. The hot plate was set to $25\,^{\circ}$C (298 K, hot plate off) and $85\,^{\circ}$C (358 K, hot plate on).

The results of these experiments are illustrated in Fig. 12 for the $10\,\mu\mathrm{m}^2$ device and in Fig. 13 for the $20\,\mu\mathrm{m}^2$ device. In both the cases it is observed a 0.5 dB ENR decrease from 298 to 358 K, i.e., in a 60 K temperature range. Furthermore, it is observed that this phenomenon happens at all the avalanche currents, i.e., from 1 to 4 mA. To put this effect at the evidence, the panel (b) of the figures reports the ratio between the ENR at 358 K to that at 298 K. This ratio is just the difference of the previous ENR expressed in dB.

In parallel to the noise, also the impedance measurements are carried out at the two temperatures. For clarity only the impedance real parts are depicted in the panel (c) of the figures. As is apparent from the graphs, the resonance frequency (i.e., the avalanche frequency) decreases with temperature of about 6% in the whole range. Analyzing these data in terms of the developed model, it seems that the ω_a variation is a consequence of the drift saturation velocity v_d reduction

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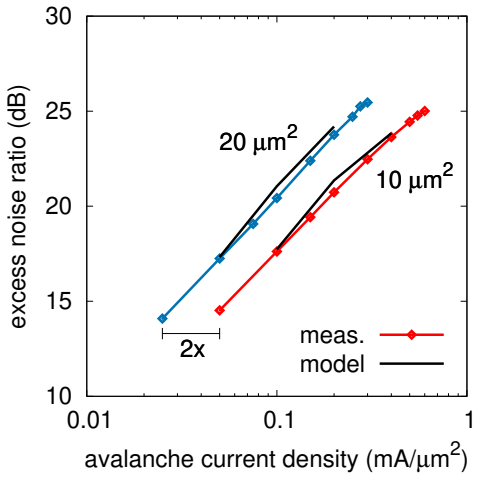

FIGURE 11. Measured ENR at 35 GHz versus the avalanche current density. The $10\ \mu\text{m}^2$ diode behavior is very close to that of the $20\ \mu\text{m}^2$ diode translated to the right by a factor 2. According to (13), indeed, the spectral current density depends on the avalanche current that, in turns, is proportional to the device area (impedance scaling effects neglected in a first approximation).

with temperature that, in turn, was already documented in the scientific literature. According to [31, p. 152], indeed, v_d drops of about 8×10^3 m/s for a 60 K temperature increase around 300 K. This corresponds to a 8% variation with respect to the 1×10^5 m/s value assumed at 300 K. Now, since ω_a is proportional to the square root of v_d, the 8% velocity drop justifies a 4% reduction of the avalanche frequency, which is in line with the experiments.

Although the observed impedance variations seem to be mainly associated with the saturation drift velocity decrease as a function of temperature, the ENR drop cannot be easily explained in the same way. Using the equivalent circuit and the simulator, indeed, we have seen that the ENR is practically not affected by a v_d change of the order of 10%. Furthermore, panels (b) of Figs. 12 and 13 show that the 0.5 dB ENR drop is almost constant in the whole frequency range. This effect can be explained assuming a slight increase of τ_x with temperature. For example, a variation from 0.48 ps to 0.51 ps (which is a 6% increase) justifies the observed ENR variation in the whole 60 K temperature range ($20\ \mu\text{m}^2$ case).

E. COMPARISON WITH THE STATE-OF-THE-ART

A table of comparison with the State-of-the-Art for avalanche noise diode integrated in commercial Si technologies is reported in Tab. 5. From this table emerges that the present study is the only one dealing with p-i-n diodes, and this is useful to complete the picture about the available device options. In particular it is found that p-i-n diodes operate well in the mm-wave frequency range. The ENR values, indeed, are comparable with those of other published researches but they can be attained at a significantly lower current and current density, thus resulting in a lower device stress that, in turn, is important for long term stability. For example, in [23] a 21 dB ENR is reported at 30 GHz for a $3.4\ \mu\text{m}^2$ Schottky diode biased at 7 mA. The same ENR is obtained, in our case,

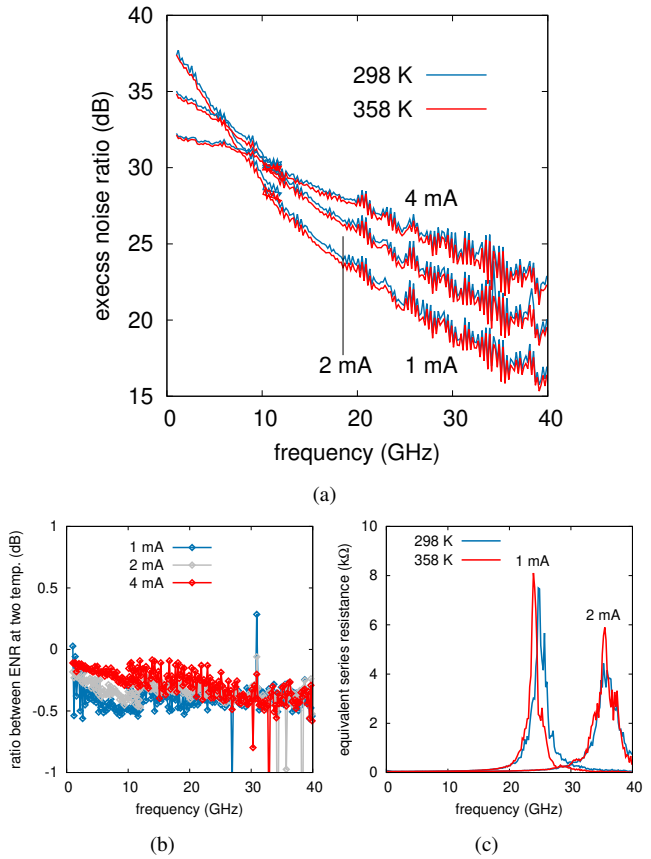

FIGURE 12. Measured ENR versus the frequency of the $10\ \mu\text{m}^2$ device for different avalanche currents and for two temperatures, (a). Ratio between the ENR measured at 358 K and that recorded at 298 K, (b). Real part of the diode impedance over temperature for the 1 and 2 mA cases, (c). The overall temperature variation is 60 K. The ENR decreases with temperature and such a variation is within 0.5 dB for all the reported avalanche currents.

at 2 mA for a $20\ \mu\text{m}^2$ device.

Concerning to breakdown voltage, instead, the experimented p-i-n diode is better than simple pn junctions, but the Schottky diode has an even lower voltage. Finally the proposed device shows an ENR sensitivity with respect to temperature of about -0.008 dB/K (i.e. -0.5 dB for a temperature variation of 60 K). This data is not reported by the other cited works.

VI. CONCLUSION

In this paper, for the first time, a mm-wave avalanche noise source is implemented using a p-i-n diode in a 130-nm commercial SiGe BiCMOS technology. The noise is generated when a reverse voltage greater than 10.7 V is applied to the device and the junction is driven into reverse breakdown. Two diodes, having an area of 10 and $20\ \mu\text{m}^2$, were fabricated and tested. These devices show an ENR of 16 and 19 dB respectively at 40 GHz, when they are biased with a $0.1\ \text{mA}/\mu\text{m}^2$ avalanche current density. Furthermore, in order to verify the noise generation mechanism stability, the ENR is also measured as a function of the temperature. It is found that the ENR sensitivity with respect to temperature

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TABLE 5. Comparison with the State-of-the-Art

Ref.	tech.	device	V_R (V)	I_a (mA)	A (μm^2)	f (GHz)	ENR (dB)	dENR$/dT$ (dB/K)
[21]	90-nm CMOS	pn diode	12.4	4	30	3-26.5	25-27	n.a.
[22] [23]	55-nm BiCMOS	Schottky diode	6	7	7	130-325	5-20	n.a.
[12]	130-nm BiCMOS	HBT bc	12.2	5	(*)	50-70	15-20	n.a.
this work	130-nm BiCMOS	p-i-n diode	10.7	2	20	1-40	19-36	-0.008

(*) base-collector (bc) diode, 2 transistors in parallel, 18 μm emitter length each

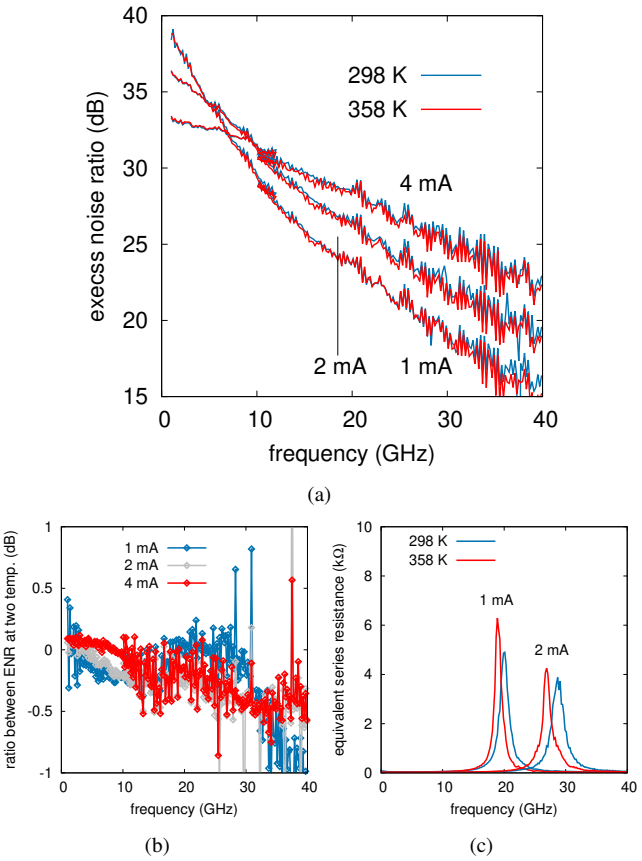

FIGURE 13. Measured ENR versus the frequency of the $20\ \mu$m^2 device for different avalanche currents and for two temperatures, (a). Ratio between the ENR measured at 358 K and that recorded at 298 K, (b). Real part of the diode impedance over temperature for the 1 and 2 mA cases, (c). The overall temperature variation is 60 K. The ENR decreases with temperature and such a variation is within 0.5 dB for 2 and 4 mA. With an avalanche current of 1 mA, instead, a 1 dB variation at 40 GHz is observed.

is, in average, about -8×10^{-3} dB/K at 40 GHz. This means that the ENR decreases only of 0.8 dB for a physical temperature variation of 100 K, a performance that suggest the applicability of the device even in harsh environments. The performance spread with respect to different chips has also been estimated. Although preliminary, the experiments indicate an ENR standard deviation below 0.2 dB for a $20\ \mu$m^2 diode at 30 GHz with currents in the range 1–4 mA.

Finally, an equivalent circuit model for the p-i-n noise diode is developed and compared to the experiments, both in terms of impedance and ENR. The proposed model is compatible with modern CAD tools and includes an empirical correction for the low impedance behavior probably due to microplasma and electro-thermal coupling effects.

The proposed study demonstrates that a standard p-i-n diode cell, typically used to implement varactor diodes, can be turned in a quite effective mm-wave avalanche noise source. The obtained results, together with those recently published by other research groups, complete the picture of avalanche noise diodes that are compatible with commercial CMOS and SiGe BiCMOS technologies. With these studies the design and the implementation of effective noise BITEs will be possible in the near future, opening the way to on-chip noise figure and gain measurement instruments.

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APPENDIX A MODEL EQUATIONS

This appendix briefly describes the small-signal model equations for an avalanche diode. These equations were published in 1966 by Gliden and Hines [14], [15], and successively improved by Maya et al. in 2003 [25] in order to account for the resistive losses that occur around the avalanche frequency, as suggested by Haitz in 1968 [19].

Fig. 2 illustrates the small-signal equivalent circuit of an avalanche diode. The avalanche zone is the region where the carriers are formed by impact ionization. It is modeled by the parallel of two elements, namely: L_a (avalanche inductance) and C_a (avalanche capacitance). Using [14], such a region is responsible for a resonant frequency $\omega_a = 2\,\pi\,f_a$ which can be tuned with the square root of the avalanche current I_0:

$$\omega_a = \frac{1}{\sqrt{L_a\,C_a}} = \sqrt{\frac{2\,\alpha'\,v_d\,I_0}{\epsilon_0\,\epsilon_r\,A}} \tag{9}$$

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In this equation α' is the ionization coefficient derivative with respect to the E-field, v_d is the saturated carrier speed in the crystal, ϵ_0 is the vacuum dielectric constant, ϵ_r is the silicon relative permittivity and A is the diode area. C_a is given by:

$$C_a = \epsilon_0\,\epsilon_r\,\frac{A}{l_a} \tag{10}$$

Once generated, the carriers leave the avalanche zone and enter in a drift region of length l_d experimenting, under the effect of a space-charge, a finite transit time $\tau_d = l_d/v_d$. In the ADS simulator such a region is modeled by the full drift impedance equation reported in [14, p. 171], see Z_d in Fig. 2. For better readability, however, an approximated Z_d version is reported here. The approximation holds for $\theta \ll 1$, where $\theta = \omega\,\tau_d = \omega\,l_d/v_d$ is the transit angle. At small transit angles $\sin\theta/\theta \approx 1$, $(1-\cos\theta)/\theta \approx \theta/2$, and Z_d becomes:

$$Z_d \approx \frac{1}{1-\left(\frac{\omega}{\omega_a}\right)^2}\left(\frac{\tau_d}{2\,C_d} + j\,\frac{\omega}{\omega_a^2\,C_d}\right) \tag{11}$$

C_d being the equivalent capacitance of the drift zone:

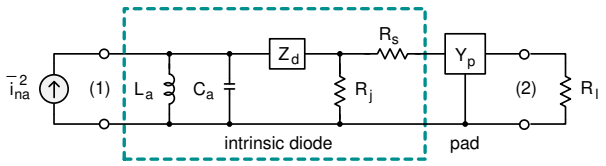
$$C_d = \epsilon_0\,\epsilon_r\,\frac{A}{l_d} \tag{12}$$

In the considered cases $\theta < 0.35$ radians at 100 GHz, and the resulting impedance approximation is better than 2%.

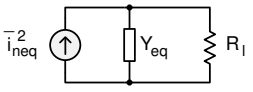
The diode ENR can be computed from the noise current spectral density $\bar{i}^2_{na}$, which is given in [15, eq. (33)]:

$$\bar{i}^2_{na} = \frac{2\,q\,I_0}{\omega^2\,\tau_x^2} \tag{13}$$

where $q = 1.6\times10^{-19}$ C is the elementary charge of the electron, τ_x is the average time between two ionizations and I_0 is the avalanche (i.e., the bias) current. The thermal noise associated to the series parasitic resistance R_s has been neglected with respect to that produced by the avalanche mechanism.



(a) model for ENR computation



(b) Norton equivalent circuit

FIGURE 14. Two-ports model that can be adopted for the ENR computation (a) and corresponding Norton equivalent circuit (b). Y_p represents the pad (and metal track) equivalent circuit, whereas R_ℓ is the load resistance used for the spectral noise power calculation.

The output noise power generated by the diode can be evaluated also following a different approach with respect to that described in Sec. III, i.e. without using an explicit noise source like the `I_NoiseBD` instance in ADS. To this purpose the equivalent circuit in Fig. 14(a) can be reduced to the model of Fig. 14(b) by applying the Norton's theorem. The quantity $\bar{i}^2_{neq}$ is the short-circuit current at port 2:

$$\bar{i}^2_{neq} = |h_{21}|^2\,\bar{i}^2_{na} \tag{14}$$

where $h_{21} = y_{21}/y_{11}$ is the short-circuit current gain and y_{ij}, $i,j = 1,2$ are the admittance parameters of the network. The equivalent Norton admittance y_{eq}, instead, is determined by observing the network from port 2 when $\bar{i}^2_{na}$ is de-activated:

$$y_{eq} = y_{22} - \frac{y_{12}\,y_{21}}{y_{11}} \tag{15}$$

The spectral noise power N_a^{del} delivered to the resistor R_ℓ (i.e., the noise power in a unit bandwidth dissipated in R_ℓ) can be evaluated using the Norton equivalent circuit:

$$N_a^{del} = \frac{\bar{i}^2_{neq}}{R_\ell\,|y_{eq}+1/R_\ell|^2} \tag{16}$$

Now, the diode in avalanche state is considered equivalent to a resistor at temperature T_H (hot temperature), where T_H is an "effective" noise temperature. Thus, according to [7, p. 19]:

$$T_H = \frac{N_a^{del}}{k_B} \tag{17}$$

where $k_B = 1.38\times10^{-23}$ J/K is the Boltzmann constant. Substituting (16) in (17) one gets:

$$T_H = \frac{|h_{21}|^2}{k_B\,R_\ell\,|y_{eq}+1/R_\ell|^2}\,\bar{i}^2_{na} \tag{18}$$

Using (3) one obtains ENR $\approx T_H/T_0 - 1$, if $T_C \approx T_0$ is assumed.

APPENDIX B Y-FACTOR METHOD AND ENR

Purpose of this formulation is to directly relate the ENR of our p-i-n diode avalanche noise source (DUT) to the power measured by the spectrum analyzer. In this derivation the spectrum analyzer input impedance will be assumed as an ideal "nonreflecting, nonemitting" load, according to [7, p. 19]. The correction for real case situations include the mismatch factor concept which is already discussed in Sec. IV.

Let's first consider the calibration process: in this case C is connected to A of Fig. 4(b). If the reference noise source is switched on, it generates avalanche noise being equivalent to a hot (H) load. Under these conditions the ideal spectrum analyzer will measure a noise power spectral density N_H^R:

$$N_H^R = k_B\,\left(T_H^R + T_{sys}\right)\,G_{sys} \tag{19}$$

where k_B is the Boltzmann' constant, while G_{sys} and T_{sys} are the (measurement) system gain and equivalent noise temperature respectively. The last two parameters are related to the gain and the noise figure of the amplification chain (noise receiver). If the reference noise source is switched off

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it is similar to a cold (C) load. The measured noise power spectral density N_C^R will be:

$$N_C^R = k_B \left(T_C^R + T_{sys}\right) G_{sys} \tag{20}$$

Taking the ratio between (19) and (20) the unknown system gain and the other parameters simplify, so one obtains:

$$Y_R = \frac{T_H^R + T_{sys}}{T_C^R + T_{sys}} \tag{21}$$

where $Y_R = N_H^R/N_C^R$ is the Y-factor associated to the reference (R) noise source. Equation (21) is very important since, the only unknown in it, is the equivalent noise temperature of the measurement system. Solving for T_{sys} one obtains:

$$T_{sys} = \frac{T_H^R - T_C^R\, Y_R}{Y_R - 1} \tag{22}$$

In the above expressions, T_H^R and T_C^R are the "effective" noise temperatures of the reference noise source in its two states. Exploiting the general definition of ENR, see equation (3), these two temperatures can be related to one another:

$$T_H^R = T_C^R + T_0\, \mathrm{ENR}_R \tag{23}$$

Inserting (23) in (22) and approximating $T_C^R \approx T_0$ one get:

$$T_{sys} = T_0 \left(\frac{\mathrm{ENR}_R}{Y_R - 1} - 1\right) \tag{24}$$

where ENR_R is factory provided (i.e. each laboratory noise source has its own calibration table). In conclusion, the calibration process allows for the determination of T_{sys}. The system gain G_{sys} is not needed because of the adopted Y-factor method [7]. The last point is, of course, an approximation based on the fact that G_{sys} does not change when N_H^R and N_C^R are subsequently measured.

Let's now focus on the measurement of the avalanche p-i-n diode noise source, i.e. our DUT. Apart for B being now connected to A of Fig. 4(b), all the previous considerations can be repeated. From a mathematical point of view one has simply to replace the reference noise source (index R) with the DUT (index D). The Y-factor becomes:

$$Y_D = \frac{T_H^D + T_{sys}}{T_C^D + T_{sys}} \tag{25}$$

Using (3) and (25), after simple manipulations, one get:

$$\mathrm{ENR}_D = (Y_D - 1)\, \frac{T_C^D + T_{sys}}{T_0} \tag{26}$$

Finally, substituting (24) in (26) and approximating $T_C^D \approx T_0$, (4) is obtained.

APPENDIX C NOISE SETUP VALIDATION

In order to validate the results obtained at the Infineon laboratories in Villach, the $20\,\mu\mathrm{m}^2$ p-i-n diode was also measured using the University of Perugia facilities. The impedance experiments were carried out with a PNA N52230A, a 10 MHz–40 GHz Vector Network Analyzer form Keysight Technologies. A semiautomatic ALESSI REL-4500 probe station equipped with a $100\,\mu$m pitch GSG probe tips (Picoprobe model 40a) was used to contact the test chip. A SOLT calibration was performed with a Picoprobe calibration substrate. The measured impedance values are in close agreement with those obtained in Villach and are not discussed further.

Concerning the ENR experiments, instead, the setup illustrated in Fig. 15 was adopted. The main difference with respect to the Villach equipment is that, at the University of Perugia, a mm-wave to VHF down-conversion of the input noise was performed. In this way the accuracy is improved, since the spectrum analyzer measuring the spectral noise power is more sensitive at low frequencies.

The measurement chain is composed by a bias-tee (Keysight 11612A), a noise receiver and a spectrum analyzer (Keysight N9918A, up to 26.5 GHz). An isolator in WR28 waveguide is inserted to provide a good matching at the receiver input port (reflection coefficient lower than $-17\,$dB). The system is calibrated with the Agilent 346C-K01 reference noise source. The noise receiver is composed by a low noise amplifier (A1), a Sub Harmonic Mixer (SHM) and an Intermediate Frequency (IF) amplifier (A2). The Local Oscillator (LO) is implemented by a laboratory microwave generator (HP 8350A). The IF frequency is set to 150 MHz and the corresponding Displayed Average Noise Level (DANL) of the spectrum analyzer is $-141.4\,$dBm/Hz. In the range 20 to 30 GHz the overall receiver gain is greater than $50\,$dB whereas its noise figure (i.e. the system noise figure) is better than $6.6\,$dB, including the 30-cm cable, the bias-tee and the isolator.

The noise power measurements and the Y-factors are processed with the same equations reported in Sec. IV. The ENR obtained with the described setup is reported in Fig. 16 and is compared with the Villach results. As visible from the graph, the maximum discrepancy between the two experiments is within $1.3\,$dB. The test chip measured at the University of Perugia, however, is different with respect to that used in Villach, although both belong to the same wafer lot.

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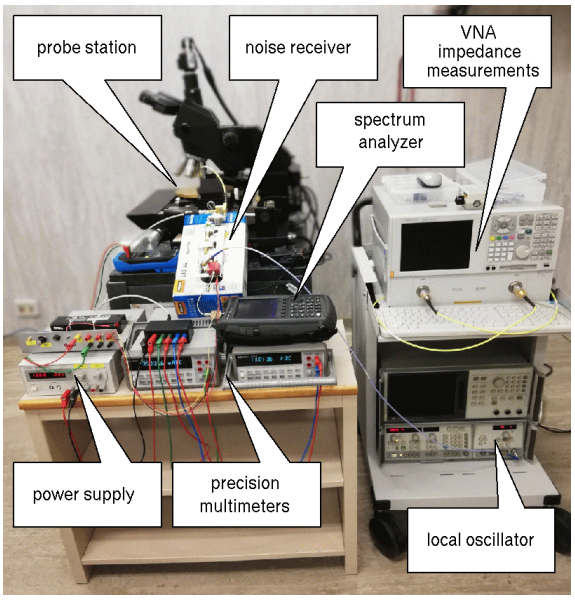
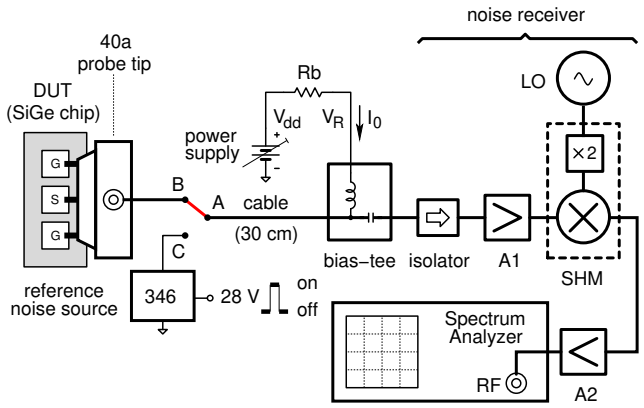


(a)



(b)

FIGURE 15. Experimental setup used, at the University of Perugia, for the on-chip noise diodes ENR characterization: photograph (a) and schematic (b). The measurement chain is composed by a bias-tee (Keysight 11612A), a noise receiver and a spectrum analyzer (Keysight N9918A, up to 26.5 GHz). The system is calibrated with a reference noise source (Agilent 346C-K01). The p-i-n avalanche noise diode (DUT) is contacted through a GSG probe tip with a $100\ \mu$m pitch (Picoprobe model 40a, up to 40 GHz). The noise receiver performs a down-conversion of the mm-wave signal to VHF. It is composed by a low noise amplifier (A1), a Sub Harmonic Mixer (SHM) and an intermediate frequency amplifier (A2). The Local Oscillator (LO) is implemented by a laboratory microwave generator (HP 8350A). The overall gain on the noise receiver between 20 to 30 GHz is greater than 50 dB. Similarly to the Infineon setup, a variable power supply in series with a resistor R_b is used to bias the diode, and two precision multimeters are adopted to measure the avalanche current I_0 and the reverse voltage V_R. Again, there are two modes: measurement (B – A) and calibration (C – A).

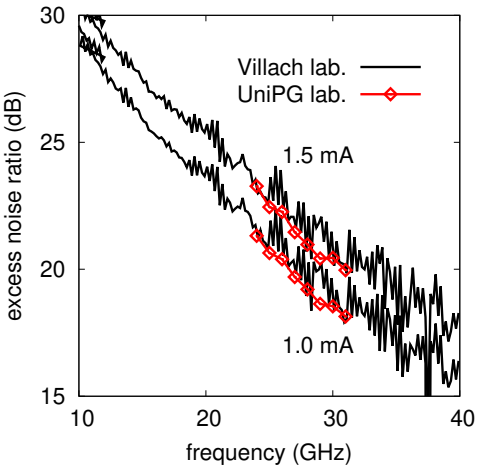


FIGURE 16. Comparison between ENR measurements obtained at the Infineon (Villach) and at the University of Perugia labs. A $20\ \mu\text{m}^2$ p-i-n diode biased with an avalanche current of 1 mA and 1.5 mA are considered in both the cases. The University of Perugia experiments are not corrected for the input mismatch but an input isolator (in WR28 waveguide) is used. In these conditions the maximum discrepancy between the two experiments is 1.3 dB.

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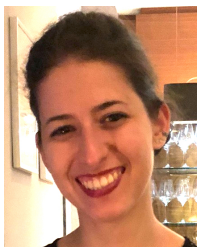

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