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ELSEVIER

Monolithic current-sensitive preamplifier for the Accordion LAr calorimeter

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Abstract

Monolithic current-sensitive preamplifiers matching large detector capacitances, suitable for the Accordion LAr calorimeter prototype, have been designed and fabricated in an ion-implanted GaAs MESFET process. After pulse shaping with an CR–RC^2 filter, the equivalent noise charge is at least a factor of 2 lower than the value reached so far with existing hybrids circuits, without increasing the power dissipation. This preamplifier has a fast response and large dynamic range. Results show that it is still possible to further reduce the noise and extend the dynamic range; this is likely to be obtained in a new version presently being developed.

1. Introduction

The use of current-sensitive preamplifiers for the readout of the accordion LAr calorimeter has been considered as an efficient way to cope with the large dynamic range expected at LHC [1,2].

Assuming that the search for a Z′ extends up to 5 TeV, the maximum energy deposition in a single cell of the electromagnetic LAr calorimeter at LHC gives about 1.5 TeV [3]. As the sampling ratio is 0.23 and the drift time 400 ns, the maximum value of the triangular detector current is almost 4 mA. Reading out this large current with a charge-sensitive preamplifier would cause very large output voltage excursions, larger than 20 V even using a feedback capacitor larger than 30 pF. One solution to this problem of handling large dynamic range is to use non-linear charge preamplifiers [4]. Alternatively, a current-sensitive configuration would produce a voltage signal at the preamplifier output that, for the above-mentioned detector signal and for a feedback resistor of 1500 Ω, would be less than 6 V.

Fast current-sensitive preamplifiers can be realized using dominant-pole amplifiers that have very large gain-bandwidth product (GBW). Large GBW is essential to assure that the pole determined by the feedback network is well separated from the second pole determined by the preamplifier's input resistance [5]. The cell's capacitances of the final detector for large rapidity may have values of a few nanofarads, from about 300–400 pF at zero rapidity. The input FET must match such values.

After designing GaAs MESFETs with 12000-μm gate width, which demonstrated very attractive noise performance with low power dissipation [6], we have designed a dual preamplifier chip for the readout of a 2-meter LAr calorimeter prototype with integrated preshower [7]. More than 300 of those chips have been installed in the detector for a beam test foreseen for the end July 1994 at CERN.

In this work we report the results obtained at the laboratory with the present monolithic version of the current-sensitive preamplifier. The chip was fabricated using an ion-implanted GaAs MESFET process, TriQuint's QED/A, already evaluated at cryogenic temperatures [8] and tested for radiation damage [9].

2. Configuration of the monolithic preamplifier

Two channels have been accommodated in a single chip occupying an area of 2.5×1.5 mm^2, Fig. 1. The circuit configuration, Fig. 2, is basically similar to our previous designs: an input FET (B1) followed by a dual cascode (B2, B3) necessary to obtain a high impedance at the drain of B3, and a bootstrapped current source (B4, B5) acting as a dynamic load. The biasing current of B1 is supplied with a separate power supply V_{CO}, through a resistance of 500 Ω (R1). In this way the main power supply V_{CC} can be fixed at a suitable voltage depending on the desired dynamic range, while the power consumption, a large part of which takes place in the input FET B1 and resistor R1, is kept low. Diodes B11 to B19 fix, through the buffer B6, the drain voltage of B3. A large-value, 120 kΩ, feedback resistor (R_F) is internally connected to stabilize the loop at DC. Two buses ADJ and RTEM have

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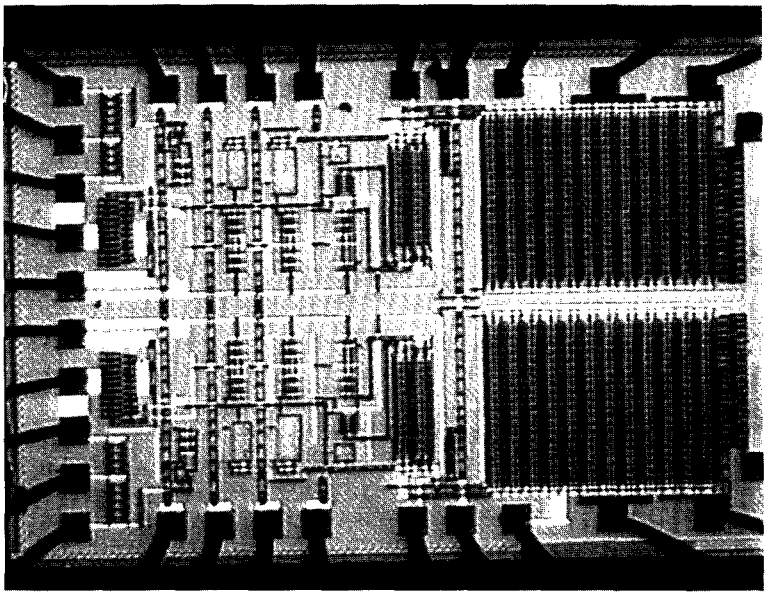

Fig. 1. The chip occupies 2.5 × 1.5 mm^2 and accomodates two channels. Note the large area of the input FETs.

been added to trim the output voltage when tests are performed at room temperature. Frequency compensation can be introduced by switching on FETs BW3 and/or BW2. Diode PD has been included to protect the input FET from large negative voltage excursions possibly resulting from high-voltage discharges in the detector.

In order to facilitate use of the preamplifier in different experimental conditions, the feedback components are external to the chip. However, the available process would allow stable NiCr resistors and capacitors to be incorporated on the chip.

3. Dynamic performance

The input transistor B1 dimensions are 3×24000 μm^2 ($L \times W$), and it is biased at $I_D = 8$ mA and $V_{DS} = 1$ V. At these conditions its transconductance g_m is 180 mS at 77 K. The input capacitance is about 120–140 pF. These data have been determined in FETs with large gate-width that have been previously developed [6]. Measurements of noise have been performed at 77 K. Two devices of 3×12000 μm^2 put in parallel, with a total biasing current of 16 mA, gave a white noise term of 0.19 nV/$\sqrt{\text{Hz}}$ and a corner frequency slightly lower than 1 MHz [6]. To substantially reduce the power dissipation of the whole preamplifier we decided for the present case to decrease the bias current by a factor 2 improving the ratio of g_m/I_D to 22 V^{-1} and dissipating only 8 mW in the FET. The series white noise increased, as expected, by $2^{0.25}$ up to 0.24 nV/$\sqrt{\text{Hz}}$.

SPICE simulations have been done to design the preamplifier. The parameters of the monolithic MESFETs had been previously extracted at 77 K. Simulations and measurements have been done for the following operating conditions: $V_{CC} = 7$ V, $V_{CO} = 5$ V, $V_{EE} = -2.5$ V. Simulation of the open-loop voltage gain gives 60 dB at DC and a main pole at about 6 MHz with a compensating capacitor of 1 pF. Direct measurement of open-loop gain gave a low-frequency value close to the simulated one. Speed measurements have been done using a charge-sensitive feedback configuration and injecting a delta current excitation. The preamplifier response, when an external capacitor $C_D = 390$ pF is connected at the input and the feedback capacitor is $C_F = 8.2$ pF, has a rise time $t_r = 4.3$ ns and

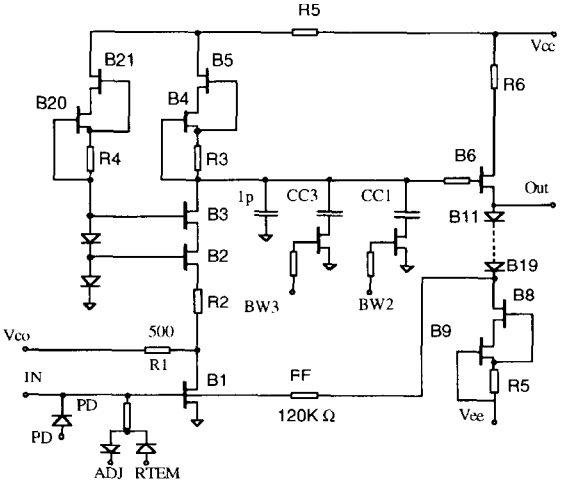

Fig. 2. Circuit diagram of the monolithic GaAs preamplifier. The AC feedback network, not shown, is external to the chip.

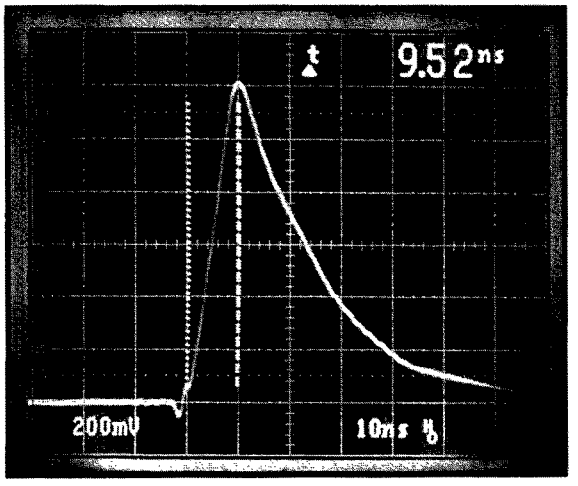

Fig. 3. Large signal δ response of the current-sensitive configuration. The pulse was measured at the receiving end of a 50 Ω coaxial cable terminated also at the sending end. $C_D = 390$ pF, $R_F = 1.5$ kΩ and $C_F = 12$ pF. The slew rate is 240 V/μs.

exhibits a slight overshoot. From the measurement we can establish a limit of 5 GHz for the GBW product. The total power dissipation is 54 mW.

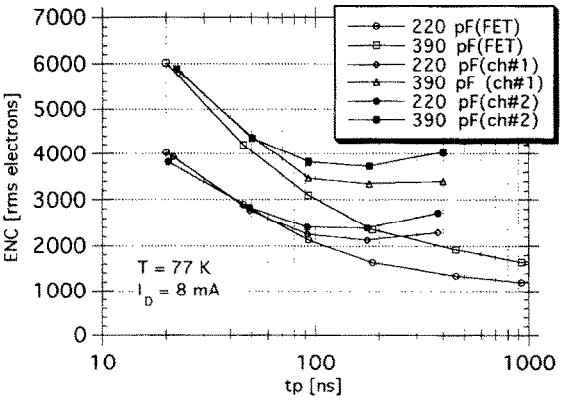

Fig. 4. ENC as a function of peaking time of a charge-sensitive configuration using a) the monolithic preamplifier b) the input MESFET of the chip followed by an hybrid preamplifier. The shaper is a CR^2-RC^2.

The feedback network consisted of a 1500 Ω resistor and a 1 nF decoupling capacitor connected in series from OUT to IN pins. A compensating capacitor $C_F = 12$ pF was connected in parallel to the 1500 Ω feedback resistor. The delta response for $C_D = 390$ pF can be observed in Fig. 3. The pulse shape was taken at the receiving end of a

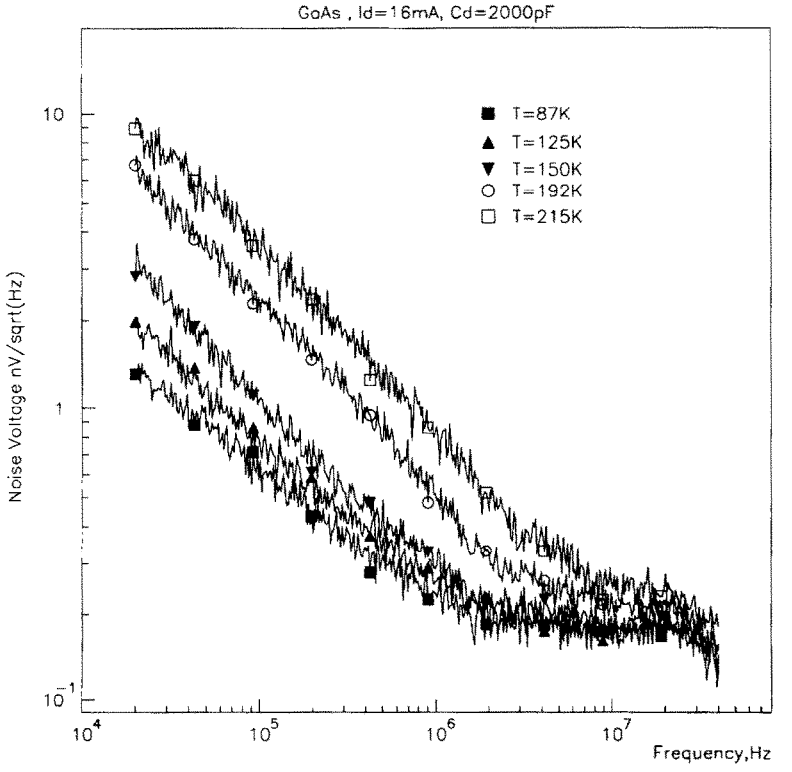

Fig. 5. Series noise spectral density for different temperatures, of a 3×24000 μm^2 MESFET made with the same GaAs process used to make the monolithic preamplifier.

Table 1
Main parameters of the monolithic current-sensitive preamplifier

Gain bandwidth product (BW2, BW3 off)	~ 5 GHz
P_D per channel	54 mW at $I_D = 8$ mA with $V_{CC} = 7$ V, $V_{EE} = -2.5$ V.
f_T/P_D	~ 92 MHz/ mW
Input capacitance	140 pF
Maximum voltage swing	4.5 V on 100 Ω load ($V_{CC} = 9$ V)
Noise at $t_p = 20$ ns (δ response) bipolar shaping	ENC = 1700 el. + 12 el/pF
Integral nonlinearity at $t_p(\delta) = 20$ ns, $C_D = 390$ pF and $V_{0\,max} = 4.5$ V	< 0.5%

terminated 50 Ω coaxial cable. At the preamplifier output the pulse height is larger than 2 V, twice the value shown in Fig. 3, since the cable is also terminated at the sending end with a 50 Ω resistor. The rise time is slew-rate limited at 240 V/μs.

4. Noise performance

The evaluation of the noise was done in three ways:

1) the equivalent noise charge (ENC) of a hybrid charge-sensitive preamplifier having at its input a MESFET from the monolithic process with the same dimensions and at the same biasing conditions as the input transistor B1, was determined. An RC^2–CR^2 shaper followed the preamplifier. The peaking time $t_p(\delta)$ was varied and the measurements were repeated for several external capacitances.

2) the ENC of the whole monolithic circuit fed back as a charge-sensitive preamplifier was determined in a similar way as in 1).

3) the ENC in the current-sensitive configuration was determined only for $C_D = 390$ pF and for $t_p(\delta) = 20$ ns. An CR-RC^2 shaper was used in this case.

The results of 1) and 2) are shown in Fig. 4. It can be noted that:

a) At short peaking times the noise of the monolithic preamplifier is virtually the same as that of the input FET alone (case 1). A white noise density of 0.23 nV/$\sqrt{\text{Hz}}$ can be extracted from the measurements.

b) There is a small dispersion between channels in the same chip.

c) In the monolithic preamplifier an additional noise source increases the ENC at long shaping times. This additional noise source has a $1/f^{\alpha}$ series component (with $1 < \alpha < 2$) and a parallel component. The $1/f^{\alpha}$ component is attributed to noise coming from later stages, mainly transistors B2 and B4. The parallel noise originates in the feedback resistor which in this case is 120 kΩ instead of 1 MΩ as used in case 1.

The noise in the current-sensitive configuration (case 3) is about 10% higher than the ENC determined in the charge-sensitive configuration. This noise increase is attributed to the slightly different weighting functions of the two systems and to some parallel noise contribution due to the small-valued feedback resistor.

In order to evaluate the effect on noise if the cryogenic liquid is different from LAr, measurements of the input FET series noise were done for several temperatures at $I_D = 16$ mA. The results show that there is no change in the white component from 87 K (minimum temperature used) up to 150 K, making these FETs useful for LAr, LKr and LXe applications, Fig 5. A slight increase of the low-frequency component can be observed in the same figure for the mentioned temperature range, whereas there is no difference at frequencies larger than 2 MHz. At temperatures higher than 150 K the corner frequency increases strongly, deteriorating the noise even at frequencies higher than 20 MHz. Still, the white noise is lower than 0.3 nV/$\sqrt{\text{Hz}}$. Measurements of ENC have shown that it is virtually constant from 87 K up to 150 K even at $t_p(\delta) = 200$ ns.

5. Summary and conclusions

Monolithic current-sensitive preamplifiers suitable for detector capacitances of a few hundred picofarads have been designed and fabricated using an ion-implanted GaAs MESFET process. Two channels have been included in a single chip. The main characteristics of the preamplifer are sumarized in Table 1.

The chips recently fabricated have shown high uniformity in static and dynamic parameters, but a larger dispersion (~ 20% rms) in noise. The noise level is in any case a factor of 2 smaller than the hybrid circuits used up to now with the LAr Accordion calorimeter. However, the power dissipation is at the same level, i.e. 54 mW. An excess noise above the noise of the input FET was measured at long shaping times; it is attributed to later stages. A new version of the chip with reduced second stage noise contribution is under development. More than 300 chips of the present version have been installed in the 2-m LAr Accordion calorimeter prototype which will be tested at CERN in summer 1994.

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