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Technological strategies for self-assembly of PS-*b*-PDMS in cylindrical sub-10 nm nanostructures for lithographic applications

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ABSTRACT

The continuous demand for small portable electronics is pushing the semiconductor industry to develop novel lithographic methods to fabricate the elementary structures for microelectronics devices with dimensions below 10 nm. Top-down strategies include multiple patterning photolithography, extremeultravioletlithography(EUVL),electronbeam lithography (EBL), and nanoimprint lithography. Bottom-up approaches mainly rely on block copolymers (BCPs) self-assembly (SA). SA of BCPs is extremely appealing due to its excellent compatibility with conventional photolithographic processes, high-resolution patterns, and low process costs. Among the various BCPs, the polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS) represents the most investigated material for the fabrication of sub-10 nm structures. However, PS-*b*-PDMS cannot be easily processed by conventional thermal treatments due to its slow SA kinetic coupled with a relatively low thermal stability. This review focuses on the available annealing methods to promote the SA PS-*b*-PDMS in parallel-oriented cylindrical sub-10 nm structures. Moreover, literature data regarding the annealing time, defects density, line edge roughness (LER) and line width roughness (LWR) are discussed with reference to the stringent requirements of semiconductor technology.

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1. Introduction

The progressive integration of different technologies, such as sensors, mems, camera, etc., in a single portable or wearable device connected to Internet, has been referred to as ‘Internet of Things’ and represents the major societal revolution of the last decade. Semiconductor industries that develop the elementary blocks making up the above devices are the major players for this epochal change. In this context, the need of high-speed microprocessors and high storage hard disk drives with reduced size and energy consumption represents the main driving force for microelectronic industry toward the progressive miniaturization of the structures [1]. The microelectronic devices are usually obtained by means of photolithography. This technique exploits the properties of a light sensitive polymer (resist) that becomes soluble (positive photoresist) or insoluble (negative photoresist) once subjected to UV light exposure after deposition on a substrate. The selective removal of the exposed area with a proper solvent leads to a polymeric mask whose features can be easily transferred to the underlying substrate [2,3].

ArF immersion 193 nm photolithography is the most commonly employed technology in semiconductor manufacturing. However, due to the physical limitation imposed by the diffraction of light, the resolution limit of this technique is about 40 nm [4]. Nanostructures with lower size, up to 10 nm [5], can be obtained by multiple patterning steps. Unfortunately, the multiplication of the patterning steps increases dramatically the process complexity, thus making this approach extremely expensive [6,7]. Extreme UV lithography (EUVL) [8,9] and electron beam lithography (EBL) [10,11], based on photons with wavelength of 13.5 nm and electrons, respectively, present higher resolution, leading to nanostructures with dimensions <10 nm. Nevertheless, the high cost of EUVL apparatus and the low EBL production throughput prevented so far their industrial exploitation [4,12,13].

Alternatively, cost-effective lithography approaches, that complement the conventional 193 nm photolithography, have been successfully developed to fabricate structures with characteristic dimensions below 10 nm. For instance, nanoimprint lithography involves the physical contact of a stamp mold on a wafer coated with a resist, UV exposure to cross-link the resist and the removal of the unpatterned resist [14–16]. Although significant advantages are obtained in terms of resolution, the high defectivity of the transferred pattern and the short lifetime of the masks represent important limitations towards the industrial exploitation of this technology [4].

A different perspective is given by bottom-up approaches involving lithography processes based on self-assembly (SA) of block copolymers (BCPs). This approach exploits the intrinsic propensity of BCPs to self-assemble (SA) in periodic nanostructures having specific morphologies [17]. The size of the nanostructures depends on the molecular weight of the BCPs. Proper design of BCP characteristics allows nanostructured polymeric films with characteristic dimensions below 10 nm to be obtained [18]. In addition, BCP-based lithography can be easily integrated in existing microelectronics production lines [5,19,20].

In this work, we critically discuss the most recent results about BCPs SA, focusing on polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS). After a brief introduction on BCP self-assembly, different approaches to drive phase separation and self-assembly in BCP thin films are discussed, highlighting the main advantages and limitations.

2. BCPs background

BCPs are macromolecules consisting of two or more polymeric segments covalently bonded [21]. This segmented structure makes the BCPs apt to phase separate in periodic nanostructures with various morphologies [22]. The AB diblock copolymer (DBC) structure represents the simplest architecture. In this case, phase separation is due to the free energy cost of contact between the different segments, as quantified by the Flory–Huggins interaction parameter, χ_{AB} [23,24]. χ_{AB} is inversely dependent on temperature. Accordingly, the driving force to phase separation increases as temperature decreases. From a structural point of view, the degree of polymerization (N), that corresponds to the numbers of monomer units in the BCP, determines the effective size of the nanostructures [25] whereas the morphology depends on the volume fraction (f) of A and B segments. In this respect, cylindrical ($f = 70:30$) and lamellae ($f = 50:50$) morphologies are perfectly suited to form dot or line patterns [2,26].

As in case of conventional photoresists, DBCs can be spin-coated onto substrates to form ultrathin films where the surface interactions determine the parallel or perpendicular orientation of the nanofeatures with respect to the substrate (Figure 1) [26]. To obtain the perpendicular orientation of the nanofeatures, it is usually necessary to neutralize the interactions between the DBC segments and the substrate [27,28]. Directed self-assembly (DSA) of BCPs allows fabricating

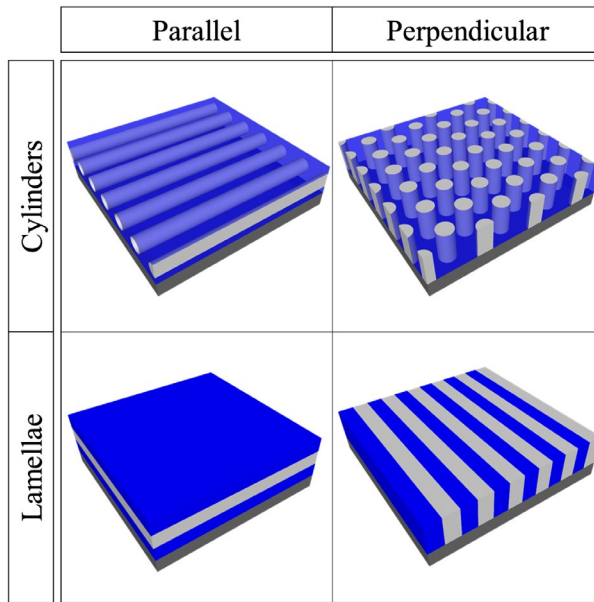


Figure 1. Schematic representation of lamellae and cylinder forming DBC thin films featuring parallel or perpendicular orientation of the nanofeatures with respect to the substrate.

all the essential geometries for building up integrated circuits. Figure 2 illustrates the set of available geometries which includes periodic or isolated lines, sharp 90° bends, jogs, T-junctions, periodic or isolated spots and their combinations [29]. The directing of the SA process is usually promoted by chemoepitaxy or graphoepitaxy. In the former, the DBC patterns are directed by substrate surface regions featuring distinct affinities for the different polymer segments whereas in the latter, lithographically printed guides are employed [30].

Polystyrene-block-poly(methyl methacrylate) (PS-*b*-PMMA) DBCs are a viable solution for patterning of sub-20 nm nanostructures [5,19,20,34]. For this system, phase separation can be induced even by simple thermal treatments in a timescale compatible with the requirements of the microelectronics industry [35–37] and vertical orientation can be achieved by several techniques including the formation of a suitable random copolymer brush layer onto the silicon substrate prior to the deposition of the DBC thin film [38–40]. As the vertical orientation of the nanofeatures occurs for a wide range of DBC film thickness [33,41–43] these DBCs represent interesting scaffolds for the synthesis of lithographic masks with stripes or vertical pillars having tailored characteristic dimensions and heights. The lateral order within the nanodomains is controlled by the annealing time and temperature, eventually exploiting the residual solvent trapped in the polymeric film [44,45]. Topographical [46–48] or chemical pre-patterning [49,50] of the substrate allows registering the in-plane orientation of the nanodomains thus further improving the lateral order.

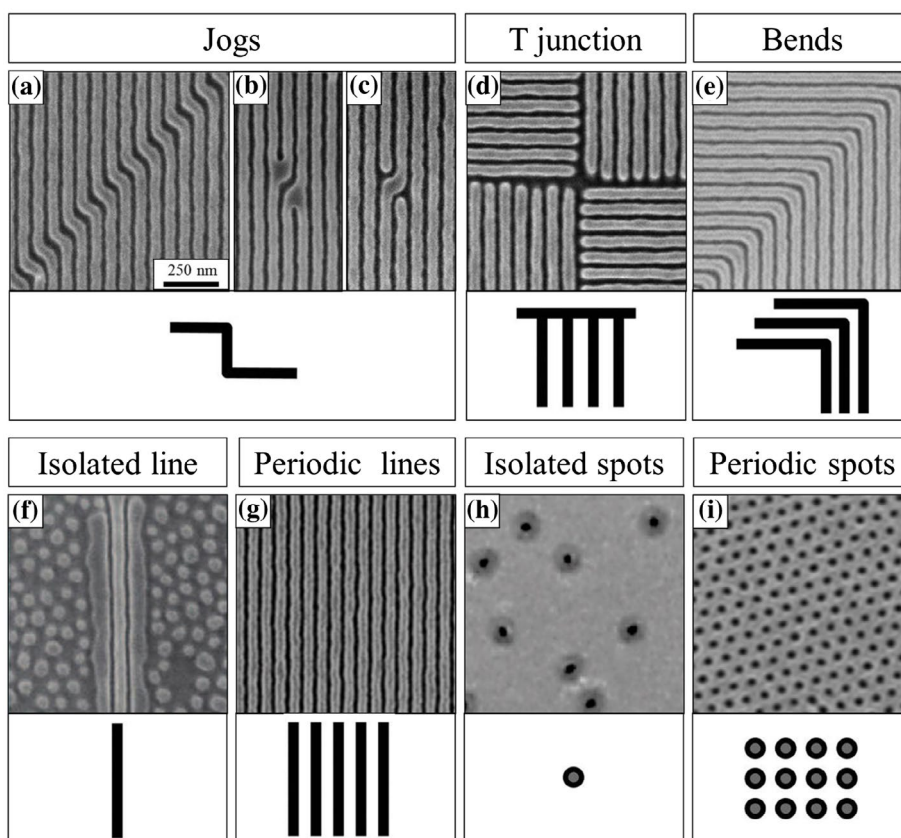


Figure 2. SEM images of PS-*b*-PMMA self-assembled morphologies (perpendicular lamellae (a–g) and cylinders (h, i)), and their geometrical translation in building blocks for integrated circuits setting up [29]. PS and PMMA domains are light gray and dark, respectively. (a–f) adapted from [29]; (g) adapted from [31]; (h) adapted from [32]; (i) adapted from [33].

While PS-*b*-PMMA copolymers show a remarkable technological potential, their low χ_{AB} value (0.06 at 300 K) [51] limits the minimum domain dimension to approximately 12 nm [52,53]. Consequently, DBCs with higher χ_{AB} were developed scaling down the domain resolution well below 10 nm. In this context, organic DBCs systems having high- χ_{AB} such as: polystyrene-block-poly(2-vinylpyridine) (PS-*b*-P2VP), polystyrene-block-poly(4-vinylpyridine) (PS-*b*-P4VP), polystyrene-block-polyethylene oxide (PS-*b*-PEO), polystyrene-block-poly(lactide) (PS-*b*-PLA) are extremely appealing to achieve ultra-small features. Unfortunately, the low etch selectivity between blocks limits their application [20,54]. The incorporation of inorganic segments into the DBC could be an attractive solution to solve this issue. Among the inorganic DBCs, silicon-containing DBCs are particularly interesting because upon exposure to oxygen plasma, the silicon segment is converted to SiO_x forming nanostructures that provide enhanced contrast for subsequent pattern transfer into the underlying substrate, while the organic segment degrades under the same treatment [54]. This property can be exploited

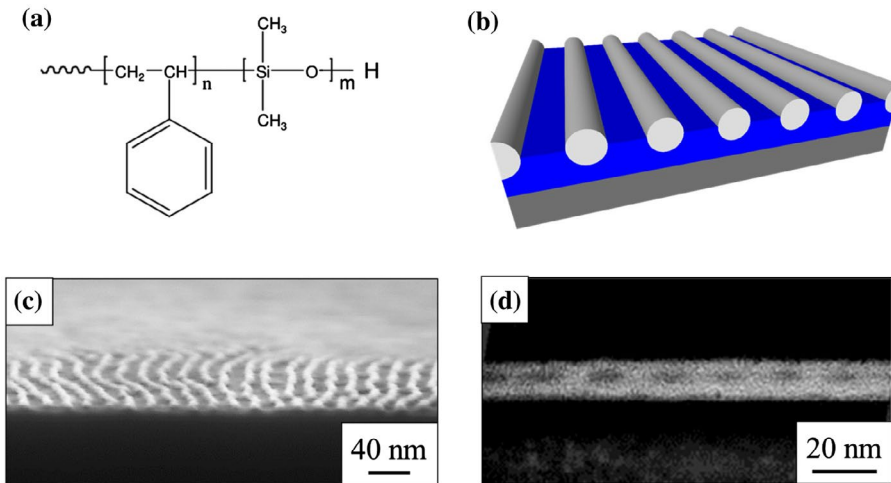


Figure 3. (a) Chemical structure of PS-b-PDMS. (b) Schematic picture of the system where the PDMS cylinders are in gray and the PS matrix in blue. (c) Cross-sectional SEM image of PDMS cylinders parallel to the substrate, adapted from [69]. (d) Cross-sectional TEM image of PDMS cylinders parallel to the substrate, adapted from [70].

for lithographic applications [55]. Among the various silicon-containing BCPs, polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS) DBC [20,56] (Figure 3(a)) has been recognized as the reference material, because of its high Flory–Hugging interaction parameter χ_{AB} (0.26 at 300 K) [57] resulting in the formation of nanostructures with minimum feature size around 8 nm [58,59]. Moreover, this material is commercially available and well characterized [60]. In addition, the good etching contrast between the PS and PDMS segments provides a robust hard mask that can be exploited to transfer into the underlying substrate by means of dry etching techniques such as reactive ion etching (RIE) which involves plasma etch gases. The selectively etching of the substrate compared to the oxidized PDMS (SiO_x) mask depends to the etch gas employed. In this context, Jung et al. [61] exploited parallel cylinders self-assembled PS-*b*-PDMS on patterned silica substrate to fabricate wire structures by means of 300 W CF_4 RIE process for 30 s. In the condition described in the article, the etching rates of the oxidized PDMS and of the silica are quite similar (~ 0.7 nm/s), permitting an etching ratio cylinder/wire around 1:1. Alternatively, Girardot et al. [55] fabricated periodic silicon line patterns using the hard mask generated by the self-assembly of PS-*b*-PDMS in parallel-oriented cylinder deposited on spin-on-carbon (SoC)/silicon-containing anti-reflective coating (SiARC) layer. The transferring of the oxidized PDMS stripes pattern was performed by a dedicated pulsed Hbr/O_2 plasma etching condition. In this case, the etching ratio cylinder/stripes is around 1:6.

The high incompatibility between PS and PDMS segments induces the PDMS to preferentially wet the free surface of the DBC film leading to the parallel orientation of the self-assembled nanostructures [62]. Actually, it is very difficult to achieve the perpendicular orientation of the nanostructure in order to create the

periodic spots, as shown in Figure 2(h)–(i). Kim et al. exploited partially hydrolyzed polyvinyl alcohol (PVA) topcoat with solvent annealing process in acetone. The PVA topcoat reduces the incompatibility between the PS and PDMS segments inducing the perpendicular orientation of PDMS cylinders upon controlled rate of solvent evaporation [63]. Son et al. achieved the perpendicular orientation of PDMS cylinders by means of solvent annealing in acetone with a subsequent slow drying of the BCP films [64]. Recently, Bates et al. [65], Durand et al. [66], and Maher et al. [67], achieved the perpendicular orientation of nanostructures by means of switching-polarity topcoat control methods during a thermal treatment. Alternatively, Seshimo et al. [68] obtained the perpendicular orientation of nanostructures in thin films consisting of modified PS-*b*-PDMS where vinyl groups were introduced in the PDMS block. These vinyl groups were exploited to introduce hydroxyl groups in the modified PDMS block. These hydroxyl groups permits proper balancing of the incompatibility between modified PDMS and PS blocks preventing the preferential wetting at the free surface of one of the two blocks and consequently leading to a perpendicular orientation of the nanostructures with respect to the substrate. Apart from these few examples of perpendicular orientation of the nanofeatures, foreseeing the development of complex experimental setup, most studies focus on PS-*b*-PDMS systems where PDMS cylinders lie parallel to the substrate (Figure 3(b)). Figure 3(c) and (d) show a cross-section SEM and TEM images of PDMS cylinders parallel oriented with respect to the substrate [69,70]. In this context, Ross and coworker developed a method to easily control the in plane orientation of PS-*b*-PDMS cylindrical microdomains parallel oriented with respect to the substrate by designed post arrays to generate complex integrated circuits with the stripes geometries shown in Figure 2(a)–(g) [71,72]. These experimental results suggest that parallel-oriented cylinder forming PS-*b*-PDMS thin films could represent a viable solution to synthesize nanofeatures with characteristic dimensions below 10 nm.

In the following sections, state-of-art process strategies to promote the order development of PS-*b*-PDMS thin films with PDMS cylinders parallel oriented to the substrate are illustrated and literature data regarding defectivity, line edge/width roughness (LER, LWR) of the self-assembled templates are discussed as a function of the annealing time, in view of the technological exploitation of these materials as lithographic mask for the fabrication of future generations of microelectronic devices.

3. PS-*b*-PDMS self-assembly strategies

The SA kinetic of DBCs depends on the segregation strength ($\chi_{AB}N$) [73,74]. The high $\chi_{AB}N$ of silicon-containing DBCs, such as PS-*b*-PDMS, is expected to cause an extremely slow self-assembly and lateral ordering kinetic [75]. In principle, thermal treatments in furnace at high temperatures could speed up the ordering kinetics. However, the maximum processing temperature is severely limited by

the low thermal stability of the PDMS segment [76]. In fact, thermal treatments of PS-*b*-PDMS thin films in conventional furnace under vacuum are conducted at temperatures lower than 200 °C [58,77,78]. In this regard, several annealing methods have been developed as alternative solutions to conventional furnace in order to enhance the self-assembly kinetic, while preventing thermal degradation of the silicon-containing segment.

3.1. Next generation thermal annealing methods

Degradation of PS-*b*-PDMS [69] starts at approximately 200 °C when the sample is heated at 5 °C/min. However, by increasing the heating rate, a remarkable shift of the onset of the degradation process is observed at temperatures higher than 200 °C, thus increasing the processing window for the self-assembly and ordering of PS-*b*-PDMS block copolymers. [69,76].

Rapid thermal processing (RTP) machine was successfully exploited to promote self-assembly and increase the lateral ordering of sub-10 nm cylinder-forming PS-*b*-PDMS. RTP utilizes halogen lamps and N₂ flow to precisely control all the relevant parameters involved in thermal processing, including heating rate, target temperature with minimum overshooting, annealing time, and cooling steps. Figure 4(a) and (b) show representative pictures of RTP apparatus and annealing process profile, respectively. The high precision of the thermal treatments is precious in performing efficient ordering of PS-*b*-PDMS copolymers without any degradation. In particular, operating at the annealing temperature of 310 °C in the 1–900 s time range with a fixed heating rate of 18 °C/s, the lateral order of

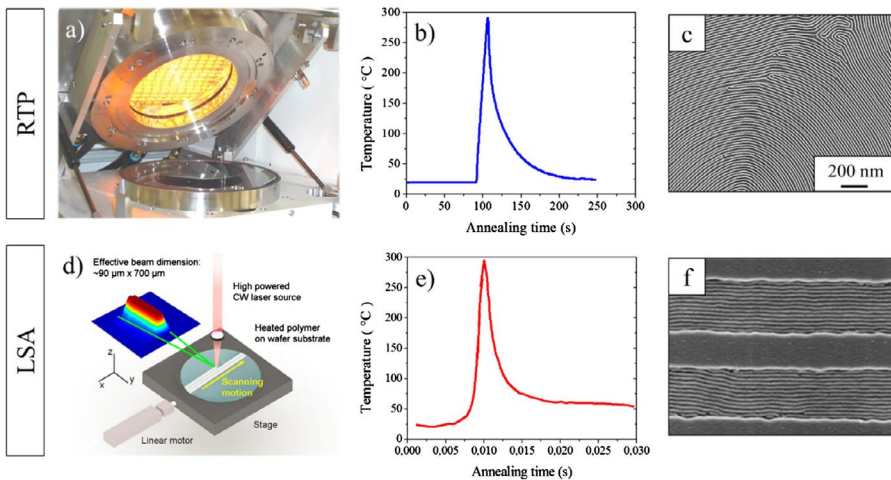


Figure 4. (a) RTP and (d) LSA apparatus, adapted from [80]. Annealing temperature profile of representative (b) RTP with heating rate of 17 °C/s and (e) LSA processes with heating rate of 62000 °C/s at 290 °C. Representative top-down SEM images of parallel-oriented PS-*b*-PDMS on flat surface annealed at 310 °C for 300 s, adapted from [69] (c) and confined in trenches with 275 nm width annealed at 440 °C for 20 ms (f) adapted from [79].

the cylindrical nanostructures on flat substrates was increased up to the correlation length of 1.25 μm , without any evidence of degradation [69], as shown in Figure 4(c).

Highest heating rates were also exploited by laser spike annealing (LSA). The samples treated by LSA undergo an ultrafast heating ramp in the range of 3000–75000 $^{\circ}\text{C}/\text{s}$. In this way, the DBC may be heated to very high temperatures for extremely short time periods thus allowing ultrafast ordering kinetics. Figure 4(d) and (e) show representative LSA schematic apparatus and annealing process profile. Jiang et al. reported the direct self-assembly of PS-*b*-PDMS with 23% of vinyl methyl siloxane by means of LSA [79]. They obtained a fingerprint like arrangement of parallel PDMS cylinders with dimension below 10 nm across large area of the sample upon 3 ms annealing at temperatures >440 $^{\circ}\text{C}$. When the DBC film is confined in topographically defined trenches, the resulting cylindrical nanostructures are well aligned inside the guiding pattern upon a 20 ms long LSA treatment at 440 $^{\circ}\text{C}$ [79], as shown in Figure 4(f).

3.2. Solvent vapor annealing (SVA) methods

Solvent vapor annealing (SVA) processes exploit the addition of solvents in the DBC film in order to increase the mobility of the PS-*b*-PDMS polymeric chains speeding up the self-assembly kinetic [81]. Unfortunately, there is no SVA standard setup apparatus since most of the processes have been developed and tested on a laboratory scale in homemade systems. This makes quite difficult the comparison among the experimental data collected by different research groups. Nevertheless, two main categories, usually referred as static and flow SVA, can be identified depending on the solvent process conditions [82].

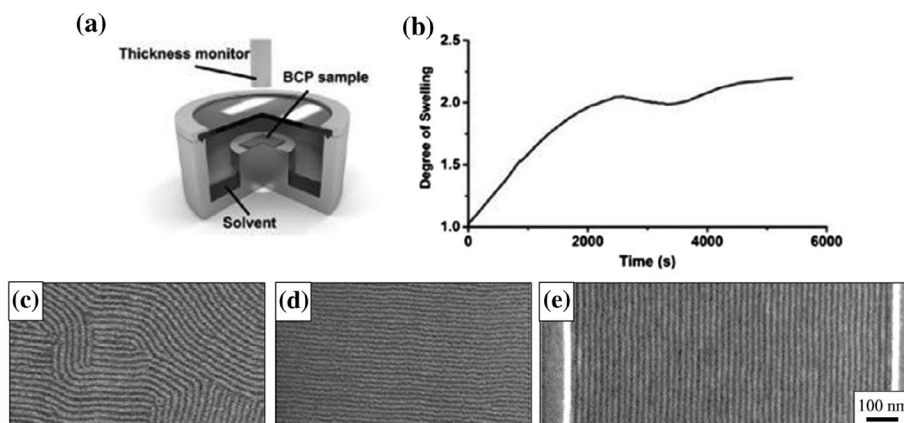


Figure 5. Static SVA apparatus (a) with representative swelling profile (b) adapted from [82]. Top-view SEM images of cylindrical PS-*b*-PDMS obtained by means of (c) 4 h of SVA at room temperature, adapted from [64], (d) 15 min of SVA with PVA topcoat at room temperature, adapted from [83], and (e) 5 min of SVA at 85 $^{\circ}\text{C}$ in trenches, adapted from [77].

In static SVA, the PS-*b*-PDMS thin films spun onto the substrates are exposed to the vapor of one or more solvents in a saturated sealed chamber at high pressure, in order to obtain swollen DBCs thin films. Figure 5(a) shows a simple scheme of a static SVA apparatus [82]. The solvent entrapped in the swollen DBC films promotes the self-assembly of the DBC molecules even at room temperature. The subsequent removal of solvent vapor from the chamber causes the evaporation of the solvent entrapped in the swollen DBC film. During this evaporation step, well-organized nanostructures are formed parallel or perpendicularly oriented with respect to the substrate. Two optically transparent windows are usually present on the chamber for real-time measurements of the DBC film thickness by ellipsometry in order to monitor the degree of swelling, determined by the adsorbed solvent. A typical swelling profile of PS-*b*-PDMS film is reported in Figure 5(b) [82]. Although static SVA represents the simplest SVA method, the control of the processing parameters (swelling rate, annealing time, purging) is very difficult. Consequently, process reproducibility is limited. In addition, very long annealing times, on the order of several hours, are commonly required to achieve a high level of lateral order. Figure 5(c) depicts representative top-view SEM images of a self-assembled PS-*b*-PDMS film obtained after 4 h of SVA at room temperature in acetone vapor [64].

Further modifications to static SVA were proposed by several authors in order to reduce processing time. Jeong et al. obtained highly ordered sub-10 nm cylindrical nanostructures in only 15 min by static SVA performed at room temperature in acetone vapor, exploiting the dewetting property of a poly(vinyl alcohol) PVA topcoat deposited onto the PS-*b*-PDMS film, [83] (Figure 5(d)). Conversely, Park et al. introduced a preheating step of the chamber to speed up the kinetic of the ordering process. The chamber, filled with one or more solvents, was preheated at temperatures ranging from 25 to 85 °C. Once the solvent vapor is formed, the DBC thin film sample is introduced in the chamber and annealed for time periods ranging from 60 to 300 s. Highly ordered sub-10 nm nanostructures on pre-patterned substrates were obtained (Figure 5(e)) [77].

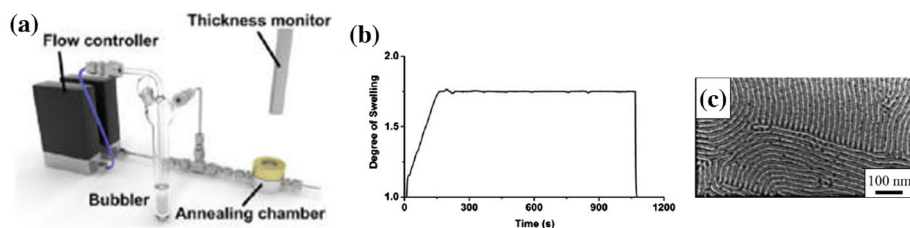


Figure 6. Flow solvent vapor annealing apparatus (a) with the corresponding swelling profile (b) adapted from [82]. Top-view SEM images of cylindrical PS-*b*-PDMS obtained by means of flow SVA at room temperature after 50 min of annealing in toluene/heptane 5:1 vapor flow (c) adapted from [84].

Flow SVA requires a much more sophisticated apparatus (Figure 6(a)) consisting of several interfaced instruments to control the flow of solvent in the chamber and the inert gas in the purge line. Moreover, *in situ* monitoring of the DBC film thickness is necessary during the sample processing [82]. With this experimental setup, the swelling of the PS-*b*-PDMS films can be precisely controlled by a feedback loop that adjusts the solvent flow in the chamber as a function of the measured thickness. The thickness is determined by means of laser reflectometry or ellipsometry, while the solvent flow is controlled by adjusting the flow rates of the selected solvent vapor with pure N₂ or Ar gases. As flow SVA enables a high level of control of the different steps of the SVA process (Figure 6(b)) [82], this method guarantees good reproducibility and good lateral order of the self-assembled nanostructures within annealing time in the range of minutes, even operating at room temperature. As an example, Figure 6(c) shows a representative top-view SEM image of a PS-*b*-PDMS film obtained by means of flow SVA at room temperature for annealing time of 50 min in a vapor flow of toluene/heptane 5:1. Unfortunately, only few research groups effectively exploited the potential of the flow SVA method because of its complex setup [84].

3.3. Exotic annealing processes

Borah et al. reported a fast microwave-assisted solvothermal process to achieve the self-assembly of cylinder forming PS-*b*-PDMS. In this technique, the DBC samples are placed inside a sealed reaction vessel with solvent at the bottom. The vessel is introduced in a microwave synthesizer and irradiated with microwaves to evaporate the solvent and heat the sample. The combined effect of solvent evaporation and temperature promotes phase separation and lateral ordering of the microdomains in the PS-*b*-PDMS thin films. Figure 7(a) shows the reactor

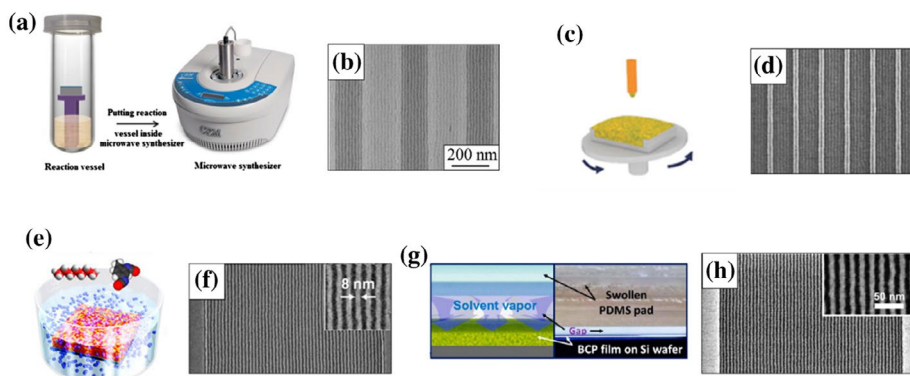


Figure 7. Schematic representation of different annealing methods with the corresponding representative top-view SEM images of ordered nanostructures (a, b) Microwave assisted, adapted from [85]. (c, d) WSC, adapted from [86]. (e, f) iDSA, adapted from [87] (g, h) PDMS gel pad solvent assisted annealing, adapted from [88].

vessel and the microwave reactor. The evolution of lateral order in PS-*b*-PDMS thin films with parallel-oriented cylinders on flat surfaces was studied as a function of annealing temperature at 50, 100, and 150 °C fixing the annealing time at 30 s and as a function of annealing time at fixed temperature of 50 °C for 30, 60, and 180 s. In both cases, the cylinder ordering decreases with increasing annealing temperature and time demonstrating limited capability to control the evolution of the system by tuning the processing parameters. Nevertheless, the proposed method allows achieving well-ordered cylindrical nanostructures in topographical patterns by processing the samples at low annealing temperature (50 °C) for very short time (30 s), (Figure 7(b)) [85].

Lee et al. introduced the so-called warm spin-casting (WSC) method to induce the self-assembly of sub-10 nm cylindrical nanostructures in PS-*b*-PDMS thin film without any post-annealing process. In this method, the vial that contains the DBC solution, the substrates and the chuck of the spin coater were preheated to temperatures ranging from 25 to 55 °C. The PS-*b*-PDMS solution is spun onto the warm substrate. The SA occurs in short time, as shown in Figure 7(c). High level of lateral order of the cylindrical nanostructures was obtained in patterned topographic templates performing the WSC at 40 °C for 30 s (Figure 7(d)) [86].

Park et al. presented the immersion-triggered directed self-assembly (iDSA) method to achieve the SA of sub-10 nm nanostructures in PS-*b*-PDMS thin films by a very simple and controllable process. The iDSA is a vapor-free method where DBC thin films are immersed in a chamber containing a solvent mixture consisting of toluene/ethanol with toluene fraction $f_{\text{TOL}} = 0.09$. The chamber is preheated at 85 °C. Figure 7(e) depicts a schematic representation of this system. The immersion in this solvent mixture permits to control the swelling ratio of the DBC thin film because toluene and ethanol are swelling and non-swelling solvents for PS-*b*-PDMS. In these experimental conditions, highly ordered parallel cylinders with dimension below 10 nm were obtained on topographically patterned substrates (Figure 7(f)) [87].

Finally, Jeong et al. proposed the application of solvent-swollen PDMS gel pad to achieve fast SA of sub-10 nm nanostructures in PS-*b*-PDMS films over large areas, (Figure 7(g)). The PDMS gel pad can adsorb molecules when immersed in solvent and gradually releases solvent vapor when the pad is exposed to air. This technique exploits the solvent vapor flux emitted from the gel pad that can be directly injected in the DBC thin film to induce the SA. The PDMS pad is either placed at distance of 1 mm from the DBC thin film or directly in contact with it. In the latter case, SA of sub-10 nm nanostructures was achieved on wafer substrate in short processing time (<60 s) at 100 °C (Figure 7(h)). In the former case, the application of moderate shear force is reported to drive the alignment of sub-10 nm parallel cylinders in the direction of the shear force without any topographical guide in process time of only ~5 s at 100 °C [88].

Table 1. Information about PS-b-PDMS under consideration.

	M_n (kg/mol)	f_{PS}	f_{PDMS}	PDI	Reference
PS-b-PDMS	16	0.67	0.33	1.08	[64,77,83–88]
PS-b-P(DMS-r-VMS)	22	0.72	0.28	1.03	[69,79]
PS-b-PDMS	28	0.67	0.33	/	[89]

Note: Molar mass (M_n), PS volume fraction (f_{PS}), PDMS volume fraction (f_{PDMS}), Polydispersity index (PDI).

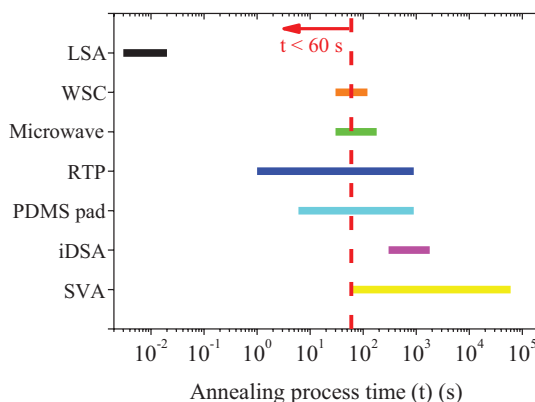


Figure 8. Process time range of various annealing technologies to achieve the SA of PS-b-PDMS. For LSA [79] and RTP [69], the Molar mass (M_n) of the PS-b-PDMS employed is 22 (kg mol^{-1}). For WSC [86], Microwave [85], PDMS pad [88], and iDSA [87] $M_n = 16$ (kg mol^{-1}). For SVA [64,77,83,84,89], the $M_n = 16$ (kg mol^{-1}) and 28 (kg mol^{-1}). The resulting cylindrical PDMS nanostructures is comparable for all the annealing methods, around 8–9 nm. Dashed red line indicates the ITRS limit.

4. Discussion

The integration of BCP self-assembly as lithography tool in a standard process flow of semiconductor industry is challenging because several stringent requirements must be fulfilled. In this regard, the last edition of the International Technology Roadmap for Semiconductor (ITRS) identified a series of critical key metrics. First of all, BCPs are requested to self-assembly in sub-10 nm features in annealing time shorter than 60 s. Moreover, defect density of the SA pattern is expected to be lower than 0.01 cm^{-2} . Finally, line edge/width roughness (LER, LWR 3σ) values have to be smaller than 0.6 and 0.8 nm, respectively [4].

Table 1 reports the physical-chemical characteristics of the PS-b-PDMS block copolymers under consideration. Figure 8 summarizes the standard range of processing time required to achieve SA and lateral order in PS-b-PDMS for the described methods. With the exception of iDSA, the SA of PS-b-PDMS can be effectively achieved in processing time equal or shorter than 1 min. Nevertheless, many of these methods cannot be easily scaled up from laboratory scale to an industrial context. For instance, methods involving the presence of solvent during the SA process, such as SVA, PDMS gel pad annealing, and microwave methods are very sensitive to process conditions. A small variation of the environmental

temperature modifies the swelling ratio of the DBC film thus significantly affecting the ordering process. Consequently, the reproducibility of these processes is not fully guaranteed. Commercial development of SA system is ongoing, but no standard systems are currently available on the market. The iDSA method represents a more industrial friendly process because the DBC film is immersed in liquid solvent. In fact, this guarantees accurate control of the swelling ratio. Nevertheless, the processing time for this method is usually much longer than 60 s, exceeding the time limit imposed by ITRS. Actually, the WSC method permits to spin-coat and achieve the SA of the DBC in a single step further reducing the processing time. Nevertheless, this method needs the preheating of the DBC solution, chuck and substrate before the WSA process thus limiting the reproducibility of the SA process. The RTP and LSA are very attractive approaches because they are easily integrated into an industrial environment. Moreover, both approaches guarantee the SA in less than 1 min when operating at high annealing temperature. Following this technology line, further reduction of the annealing time could be envisioned using flash lamp annealing (FLA) machine, i.e. a semiconductor equipment quite similar to RTP. FLA allows the samples to be heated to the annealing temperature in milliseconds, that is with heating rates comparable to LSA, using Xe lamps [90]. Although, the use of FLA to achieve the SA of BCPs has not yet demonstrated, FLA could represent an interesting development of the RTP-based process.

Figure 9 shows the topological defects typically encountered in self-assembled DBC thin films with cylinders parallel oriented with respect to the substrate [91]. The elementary defect components are classified in junctions, terminal points, and dots and they exist in the positive phase (PDMS parallel cylinders) and negative

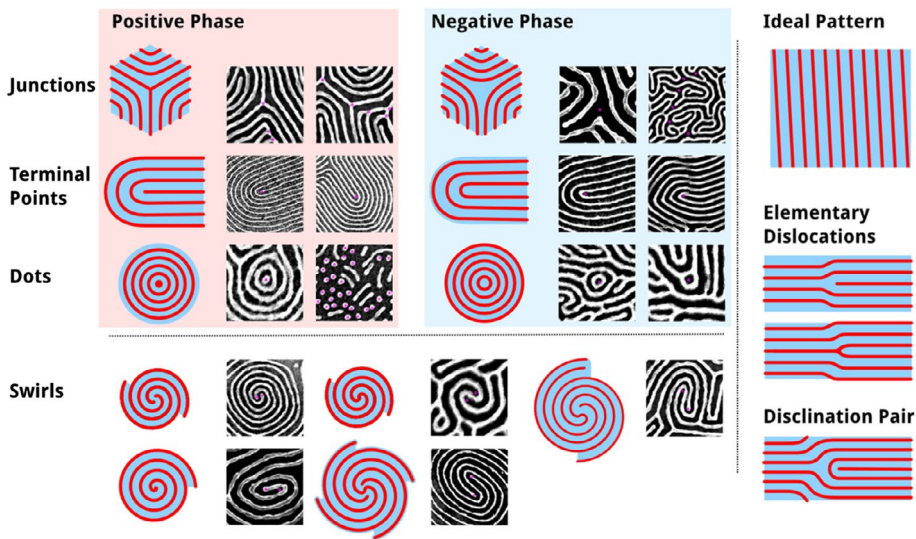


Figure 9. Scheme and top-view SEM images of topological defects in self-assembled PDMS cylinders (white phase) embedded in a PS matrix (black phase), adapted from [91].

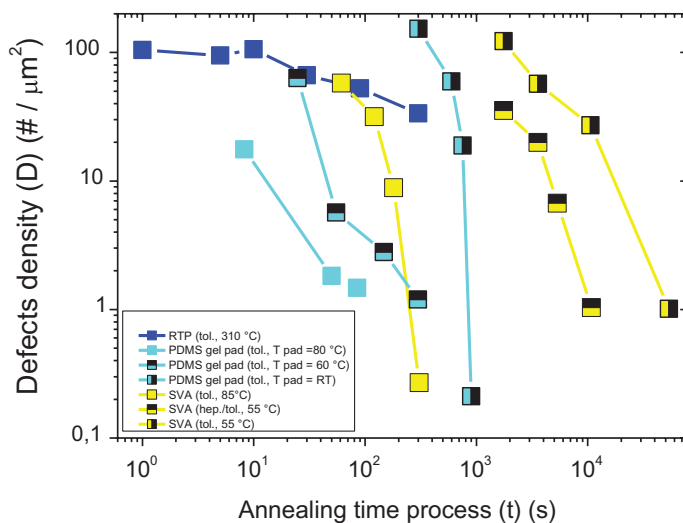


Figure 10. Defects density evolution as a function of the annealing time process for RTP [69] ($M_n = 22 \text{ kg mol}^{-1}$), SVA [77,89] ($M_n = 16$ and 28 kg mol^{-1}), and PDMS gel pad methods [88] ($M_n = 16 \text{ kg mol}^{-1}$).

phase (PS matrix). The combination of adjacent terminal points and junctions forms the so-called dislocations and disclinations [92].

The defects creation and removal from a physical point of view represent one of the most fascinating processes in the self-assembly of block copolymers. Li et al. [93] recently published a review where they described in detail this complex process. They concluded by stating that there are still several open questions that are relevant to DSA. In particular, comparison of ordering mechanisms and removal of defects between block copolymers that self-assembly with and without guiding fields are poorly explored. Figure 10 reports the data available in literature concerning the evolution of defect density (D) as a function of the annealing time (t) for RTP [69], SVA [77,89], and PDMS gel pad [88] methods. Data for the RTP method were extracted from SEM images of flat substrates using the procedure described in the literature [91] while all the other data reflect the evolution of defect density in topographically defined patterns having the same dimensions (width = $1 \mu\text{m}$, depth = 40 nm). Actually, the comparison of defect density evolution as function of annealing time on a flat surface and within topographical patterns is not formally correct because the mechanisms of defect annihilation are expected to be remarkably different in the two cases [93].

For all the methods, the defects density evolution follows a power law (Figure 10), which can be expressed as $D \sim t^{-n}$. The time-decay exponent (n) for the samples processed in RTP at $310 \text{ }^\circ\text{C}$ for 1–300 s using toluene as a solvent during the spinning process, was estimated to be ~ 0.2 [69]. When the PS-*b*-PDMS films are confined in topographical patterns, the time-decay exponents are significantly higher for both SVA and PDMS gel pad methods. Moreover, it is quite clear that

higher annealing process temperature promotes faster decay of the defect density. For instance, time-decay exponents of $n \sim 1.4$ and $n \sim 2$ were obtained when SVA was conducted at 55°C for time in the range of hours using toluene and mixed heptane/toluene [89]. By increasing the annealing temperature to 85°C for annealing time in the range of minutes, time-decay exponent of $n \sim 2.5$ was measured in toluene atmosphere [77]. Comparison between the defect density evolution on flat substrates in RTP treated samples and data obtained by other methods on pre-patterned substrates suggests that further reduction of defects could be obtained by RTP processing of DBC films confined in topographically defined structures. However, it is worth to note that even in the best case, the defects density is $0.2 \text{ defects } \mu\text{m}^{-2}$ [88] which is much higher than the limit indicated by ITRS [4]. Significant improvements in terms of defect density are expected to occur by processing the samples in a clean industrial environment. Nevertheless, the effective achievement of the target indicated by the ITRS is not straightforward.

LER and LWR represent the deviation from a straight line edge, and the deviation from a uniform line width, respectively, as depicted in Figure 11(a) and (b), [91]. According to ITRS [4], LER and LWR of sub-10 nm nanostructures are requested to be lower than 0.6 and 0.8 nm, respectively, because higher values could be highly detrimental for the performance of the resulting microelectronics devices [94–97]. Figure 11(c) reports the LER and LWR literature values of sub-10 nm PDMS parallel cylindrical nanostructures, in self-assembled PS-*b*-PDMS thin films treated by different annealing methods. The blue and red dashed lines represent the LER and LWR ITRS limit values, respectively. In case of iDSA [87] and RTP [69] methods, experimental LER and LWR values are almost twice the

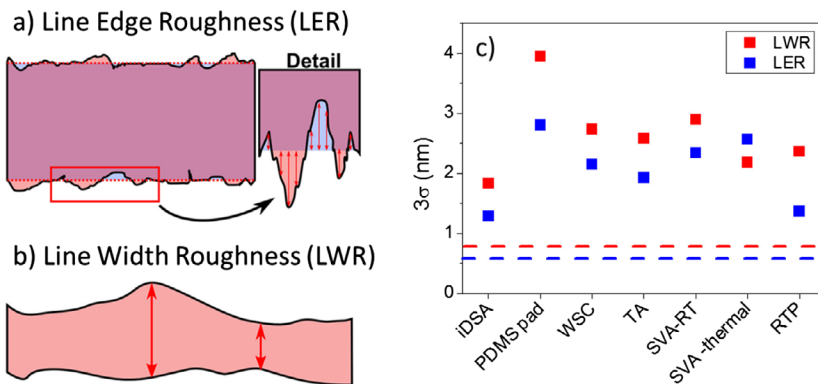


Figure 11. Sketch of the LER (a) and LWR (b) adapted from [91]. LER and LWR values for various annealing methods that include iDSA [87], PDMS gel pad [88], WSC [86], conventional Thermal annealing (TA) [86], SVA at room temperature (RT) [86], SVA-thermal at 85°C [77], RTP at 310°C [69]. The LWR value of iDSA method was calculated assuming $\text{LWR} = \sqrt{2} \text{ LER}$. The LER value of PDMS pad method was calculated assuming $\text{LER} = \text{LWR}/\sqrt{2}$ [91,98,99]. The solvent used during the annealing processes was toluene. For RTP $M_n = 22 \text{ (kg mol}^{-1}\text{)}$. For iDSA, PDMS pad, WSC, TA, SVA-RT, SVA-thermal $M_n = 16 \text{ (kg mol}^{-1}\text{)}$.

limit values imposed by ITRS. In the remaining cases, LER and LWR values are more than three times higher than the ITRS limit.

It is worth to remember that the 2015 release of ITRS represents the last edition of this document that has been almost yearly updated since 1993 and that guided the technology evolution of microelectronics for more than 20 years. This final report clearly highlights the end of conventional scaling in microelectronics, suggesting a progressive transition from planar to 3D architectures in order to further increase the density of devices maintaining their performance and reliability. In this respect, conventional scaling of planar microelectronic devices is expected to stop at the 5 nm scaling node. In the near future, semiconductor industries will be necessarily forced to choose between DSA, EUVL, and EBL in order to identify the effective lithographic approach to guide microelectronic devices toward the end of conventional scaling. However, irrespective of the final solution adopted by the semiconductor companies, the tremendous research effort on DSA lithography suggests that this technology could provide competitive solutions adapted to specific niche applications by complementing existing lithographic technologies.

5. Conclusion

In this review, we described state-of-art methodologies available in literature to achieve the SA of PS-b-PDMS films forming silicon-containing parallel cylinders with dimension below 10 nm. Literature data suggest that SA could be efficiently achieved in less than 1 min, fulfilling one of the metric targets of semiconductor technology. Nevertheless, all the current methods fail to fulfill these requests in terms of defects density, LER and LWR. In particular, the defect densities are several orders of magnitude higher than the metric target of 0.01 cm^{-2} . Similarly, LER and LWR values appear to be 2–3 times higher than those requested. Consequently, further developments are necessary in the processing of DBC thin films for SA technology to be industrially exploited in preparation of polymeric masks to be used for the fabrication of ultra-scaled microelectronic devices.

Disclosure statement

No potential conflict of interest was reported by the authors.

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