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Citation: AIP Advances **6**, 075021 (2016); doi: 10.1063/1.4960213
View online: http://dx.doi.org/10.1063/1.4960213
View Table of Contents: http://aip.scitation.org/toc/adv/6/7
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AIP ADVANCES **6**, 075021 (2016)

Negative charge trapping effects in Al_2O_3 films grown by atomic layer deposition onto thermally oxidized 4H-SiC

Emanuela Schilirò,[1,2,a] Raffaella Lo Nigro,[1] Patrick Fiorenza,[1] and Fabrizio Roccaforte[1]

[1]*Consiglio Nazionale delle Ricerche - Istituto per la Microelettronica e Microsistemi (CNR-IMM), Strada VIII 5, Zona industriale – 95121 Catania, Italy*

[2]*Dipartimento di Scienze Chimiche, Università degli Studi di Catania, and INSTM udr Catania, viale Andrea Doria 6, 95125, Catania, Italy*

(Received 12 May 2016; accepted 18 July 2016; published online 28 July 2016)

This letter reports on the negative charge trapping in Al_2O_3 thin films grown by atomic layer deposition onto oxidized silicon carbide (4H-SiC). The films exhibited a permittivity of 8.4, a breakdown field of 9.2 MV/cm and small hysteresis under moderate bias cycles. However, severe electron trapping inside the Al_2O_3 film (1×10^{12} cm^{-2}) occurs upon high positive bias stress (>10V). Capacitance-voltage measurements at different temperatures and stress conditions have been used to determine an activation energy of 0.1eV. The results provide indications on the possible nature of the trapping defects and, hence, on the strategies to improve this technology for 4H-SiC devices. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4960213]

The wide band gap semiconductor silicon carbide (4H-SiC) is characterized by a high critical electric field, a high electron mobility and a high thermal conductivity that make it an excellent material for a new generation of power devices, whose performances are expected to go well beyond the silicon limits.[1] An important advantage of SiC substrate for power devices fabrication is the possibility to form the same native oxide as in silicon (i.e., SiO_2), which can be used as gate insulator in metal-oxide-semiconductor field-effect transistors (MOSFETs).[2] Typically, special attention is focused on post-growth thermal annealings in appropriate ambient to improve the quality of the SiO_2 and its interface with SiC.[3] However, another issue to be considered for the gate insulator in 4H-SiC MOSFETs is the capability to withstand a high electric field. In particular, in blocking configuration, the electric field in the gate insulator (E_{ins}) is related to the electric field in the semiconductor (E_s) by the Gauss' law, $E_{ins} = (\kappa_s/\kappa_{ins})E_s$, where κ_{ins} and κ_s are the insulator and semiconductor permittivity values. Hence, considering the permittivity values of 4H-SiC and SiO_2 (9.7 and 3.9, respectively), the electric field in the gate oxide of a 4H-SiC MOSFET is typically a factor of 2.5 higher than in the 4H-SiC drift layer.[4] Consequently, in order to fully exploit the high electric field strength of the 4H-SiC (3MV/cm), the electric field in the SiO_2 gate oxide would approach the breakdown value, thus compromising the overall device reliability. In this context, high permittivity (high- κ) insulators could allow to overcome this limitation, enabling a better redistribution of the electric field between insulator and SiC and guaranteeing safer operation conditions for the insulator in high voltage applications.

Aluminum oxide (Al_2O_3) can be an appropriate candidate as gate insulator for SiC, due to its high dielectric constant (κ ∼ 9), good thermal stability, relatively large band gap (∼ 9 eV) and high critical electric field (10 MV/cm).[5] As a matter of fact, in the last decade, Al_2O_3 thin films have been already proposed as an alternative insulator to SiO_2 for SiC[6,7] and several methods have been used for their fabrication. Among them the Atomic Layer Deposition (ALD) technique is one of the more appealing because it provides a *layer-by-layer* growth, allowing an accurate control of the interfaces

[a]corresponding author: emanuela.schiliro@imm.cnr.it

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and conformal coverage.[8] Owing to these properties, high-κ Al_2O_3 films deposited by ALD could be interesting for the next generation of 4H-SiC trench MOSFETs operating at high voltage.[4]

In regards to the physical and applicative issues, a common literature finding[9] has been the high leakage current attributed to a theoretical Al_2O_3/4H-SiC band offset value (ΔE_C = 1.5-1.7 eV[10,11]), lower with respect to that of the SiO_2/4H-SiC system (ΔE_C = 2.7 eV).[12,13] The experimental Al_2O_3/4H-SiC band offset value is typically even lower ($\Delta E_C \sim$ 2eV[5,14–16]). For those reasons, some reports suggested the introduction of a thin thermally grown SiO_2 interfacial layer, in order to increase the conduction/valence band offset between the insulator and the SiC substrate.[9,17] In addition, large hysteresis and deviations of the flat-band voltage (V_{FB}) in the capacitance-voltage (C-V) curves of MOS capacitors with respect to the ideal ones have been observed, due to significant charge trapping phenomena in the oxide and at the interfaces.[6,9,18]

In this context, although Al_2O_3/SiO_2 stacks have been already used as gate dielectrics to demonstrate high channel mobility MOSFETs,[19,20] a better understanding of the trapping phenomena in Al_2O_3/SiO_2/SiC systems remains an open issue to define the strategy for a future implementation of this technology.

In this paper, the charge trapping effects in Al_2O_3 thin films grown by plasma enhanced atomic layer deposition (PEALD) onto thermally oxidized 4H-SiC substrates were investigated.

N-type 4° off-axis (0001) oriented 4H-SiC substrates were used for the devices fabrication. Prior to SiO_2 thermal growth, the 4H-SiC wafers were treated with piranha solution (H_2SO_4:H_2O_2 = 1:3 for 10 min) to remove eventual carbon contaminations and with diluted hydrofluoric acid (H_2O:HF = 10:1 for 5 min) to remove the sacrificial oxide. After these cleaning treatments, the 4H-SiC substrates were subjected to a controlled dry oxidation process at 1150°C in dry O_2-atmosphere to growth 5 nm of SiO_2 layer.[21] Al_2O_3 films were deposited at 250°C by a PE-ALD LL reactor from SENTECH Instruments GmbH, using trimethylaluminum (TMA) as aluminum precursor and O_2-plasma as oxygen source. TMA was delivered from the bubbler to the reactor chamber with N_2 carrier gas at a flow rate of 40 sccm. The O_2-plasma was generated by capacitively coupled source, with a 13.56 MHz RF-generator and a power of 200W. For plasma run, a 150 sccm O_2 flow was released into the plasma source in order to generate more reactive species, namely, oxygen radicals. During the ALD cycle, the TMA and O_2-plasma pulse times of were 0.06 s and 1 s, respectively, and after each precursor pulse, the deposition chamber was purged with 40 sccm N_2 for 2 s, to remove unreacted precursors.[22,23]

The microstructural characterization of Al_2O_3/SiO_2/4H-SiC stacks was performed by Transmission Electron Microscopy (TEM) using a FEG-TEM JEOL 2010F microscope. Atomic Force Microscopy (AFM) was used for a check of the surface roughness of the grown films.

Al_2O_3/SiO_2/4H-SiC MIS capacitors with sputtered Ni electrodes were fabricated for the electrical characterization. Capacitance- and current-voltage measurements (C-V, I-V) were performed on the capacitors to evaluate the insulator properties and the interface quality, considering also the effect of bias stress cycles. In particular, the amount of interface traps were estimated using frequency dependent parallel conductance measurements (G_p/ω vs ω). Furthermore, the maximum amount of negative charge trapped until the dielectric breakdown was estimated using C-V measurements under positive bias stress. From C-V measurements performed at different temperatures (25-125°C) and positive bias stress conditions (up to 28V), an activation energy for the electron traps could be estimated. These measurements were performed using a Microtech Cascade probe station equipped with a Keysight B1505 parameter analyzer.

Fig. 1 shows the cross section TEM micrograph of the Al_2O_3/SiO_2/4H-SiC sample. As can be seen, the interfacial SiO_2 (5 nm thick) layer is clearly visible, while the total Al_2O_3 film thickness is 30nm. According to ellipsometric measurements the films exhibit very good thickness homogeneity, with a lack of uniformity of less than ± 0.9%. Moreover, the TEM analysis showed the amorphous nature and the good adhesion of the Al_2O_3 film (i.e., no voids have been detected at the interfaces with 4H-SiC and SiO_2). It is worth mentioning that in spite of the initial amorphous nature of the deposited film, a crystallization process of the Al_2O_3 can locally occur under electron beam irradiation during TEM analyses, as already reported in literature.[24] The surface roughness (RMS) of the deposited film was 0.56 nm, as determined by AFM analysis.

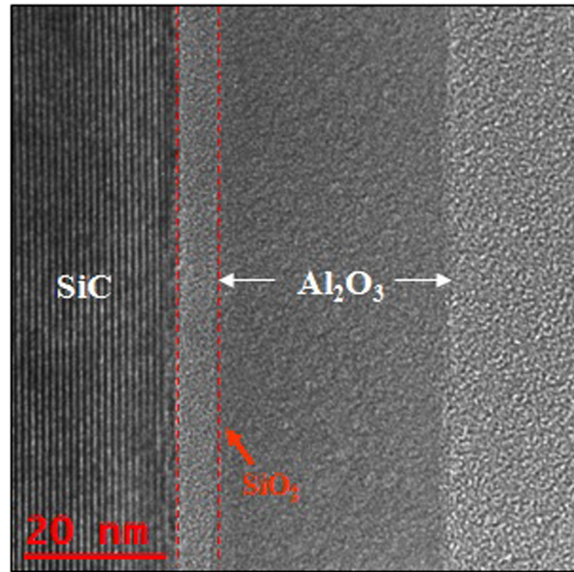

FIG. 1. Cross section TEM micrograph of the Al_2O_3/SiO_2/4H-SiC sample.

Initially, the electrical characterization of the system has been carried out by C-V analysis on the MIS capacitors, under the application of moderate bias cycles. In particular, C-V hysteresis curves (shown in Fig. 2(a)) have been acquired by sweeping the bias from -1V to +6V and backwards, i.e., keeping the oxide electric field below 2 MV/cm. The first C-V curve acquired on a "fresh" device sweeping the bias from depletion to accumulation exhibits an experimental flat band voltage value of V_{FB} = 2.8 V, which is positively shifted with respect to the theoretical one (V_{FBth}=+1.28V) calculated considering the work-function of the Ni gate electrode. From this shift, an effective negative fixed charge $N_{eff} \sim 1.4 \times 10^{11}$ cm^{-2} was determined. Moreover, a permittivity value of $\varepsilon \sim 8.4$ for the bare Al_2O_3 film has been calculated from the value of the accumulation capacitance, taking into account the presence of the 5 nm SiO_2 interfacial layer. In Fig. 2(a) a positive shift of the second C-V curve acquired sweeping the bias backwards (from the accumulation to the inversion) with respect to the first one acquired in the forwards sweep (from the inversion to the accumulation) is observed. This behavior is an indication of the presence of oxide trapping states (N_{ot}) which can be filled under operation of the capacitor, producing a shift of the experimental flat band voltage (V_{FB}) during the C-V hysteresis measurement. These trapping states can be regarded as "slow states" as they are detected during the C-V measurements performed on a time scale in the order of hundred seconds. The density of these slow oxide traps (N_{ot}) could be quantified using the common relation[25]:

$$N_{ot} = (\Delta V_{FB} \times C_{ox}) / q, \quad (1)$$

where q is the electron charge, C_{ox} is the accumulation capacitance and ΔV_{FB} is the shift between the forward and backwards C-V curve. From Eq. (1) a density of the trapping states $N_{ot} = 4 \times 10^{10}$ cm^{-2} was estimated.

Clearly, faster states located at the insulator/SiC interface cannot be extracted by the C-V hysteresis curves. The density of interface states (D_{it}) has been evaluated using the conductance method (in the 1kHz-1MHz range) and their energy distribution with respect to the conduction band edge is reported in Fig. 2(b). As can clearly be seen in Fig. 2(b), in the energy range between 0.2 and 0.6 eV below the 4H-SiC conduction band, the values of D_{it} decrease of a factor of four, i.e., going from 4×10^{12} and 1×10^{12} cm^{-2}eV^{-1} respectively. These values are in good agreement with the typical results that can be obtained for SiO_2/SiC interfaces.[26]

In order to get further information on the mechanisms of charge trapping in the states inside the insulating stack, the C-V curves on Al_2O_3/SiO_2/4H-SiC MIS capacitors were acquired performing

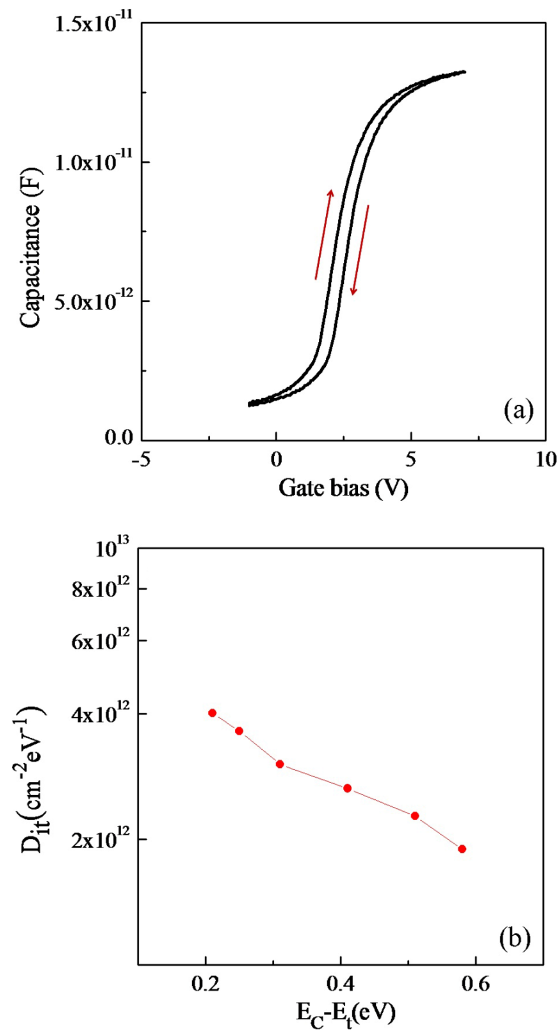

FIG. 2. (a) C-V hysteresis curves acquired on Al_2O_3/SiO_2/4H-SiC capacitors sweeping the bias from inversion (−1V) to accumulation (+6V) and backwards; (b) Interface state density D_{it} as a function of the energy with respect to the conduction band edge of 4H-SiC (E_t-E_c).

sequential bias sweeps from the inversion ($V_G = -1V$) to the accumulation, increasing the value of the final positive accumulation bias stress. In this way, under the application of an increasing electric field, electrons can be injected from the semiconductor into the insulator. Fig. 3(a) shows the C-V curves after each positive bias stress. From the progressive positive flat band voltage V_{FB} shift of the C-V curves it can be deduced that the injected negative charges (electrons) are accumulated inside the Al_2O_3 film, and their amount increases with increasing the positive bias stress. Fig. 3(b) reports the values of the negative trapped charges density, extracted from the shift of the C-V curves (Fig. 3(a)), as a function of the positive gate bias stress. Evidently, while a moderate charge trapping effect is occurring for positive bias stress values lower than +10 V, a severe increase of the trapping phenomena takes place at higher bias stress, thus indicating the onset of the dielectric degradation, which ultimately leads to the dielectric breakdown (BD). In particular, a maximum positive bias stress of +26V can be applied, corresponding to a negative trapped charge density of 1×10^{12} cm^{-2}. Beyond this bias stress (e.g., at 28V) the BD of the insulating film is observed. This situation is clearly visible in Fig. 3(c), which shows the current flowing through the MIS capacitor as a function of the electric field up to the BD. As can be seen between +6.2 MV/cm and +9.2 MV/cm the current exceeds the ground level due to the electrons injection from the bottom of the conduction band of the semiconductor through the insulating stack; then the abrupt increase of the current when the

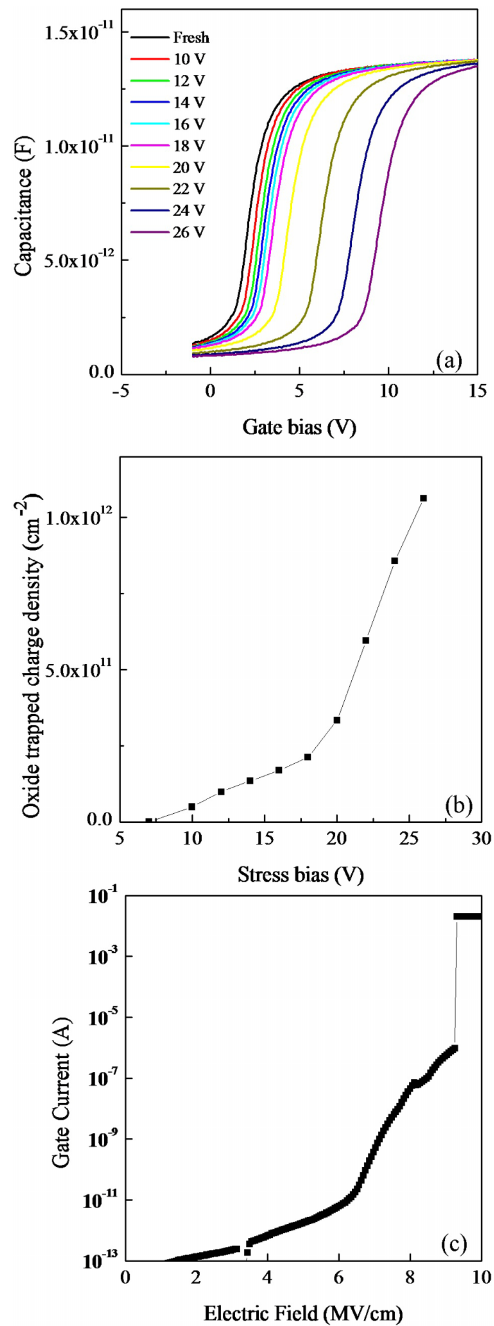

FIG. 3. (a) C-V curves acquired on Al_2O_3/SiO_2/4H-SiC capacitors sweeping the bias from inversion to accumulation, for different values of the final positive bias stress; (b) Density of trapped charge N_{trap} as a function of the positive bias stress, determined from the shift of the flat band voltage of the C-V curves with respect to the initial value; (c) Gate current as a function of the electric field acquired on a Al_2O_3/SiO_2/4H-SiC capacitor, up to the breakdown.

dielectric BD occurs is visible. This last point corresponds to a critical electric field of ∼9.2 MV/cm, i.e., close to the theoretical dielectric strength of the Al_2O_3 (10 MV/cm).

Further physical information on the nature of the trapping states present in the insulating stack could be obtained by an analysis of the C-V hysteresis curves at different temperatures. Fig. 4(a) shows the C-V curve acquired from depletion to accumulation and the curves acquired backwards from accumulation to depletion at different temperatures. Interestingly, the shift of the flat band

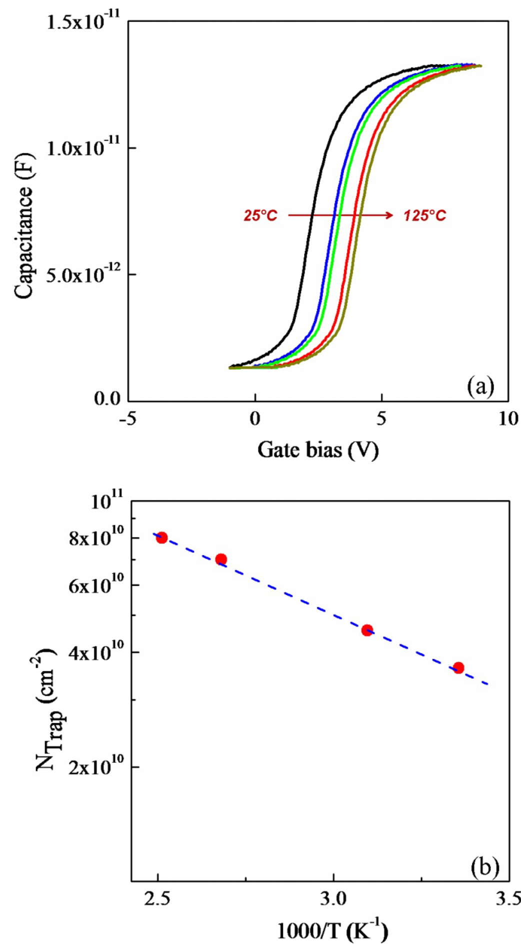

FIG. 4. (a) C-V hysteresis curves acquired on Al_2O_3/SiO_2/4H-SiC capacitors sweeping the bias from inversion (−1V) to accumulation (+9V) and backwards at different temperatures; (b) Arrhenius plot of the trapped charge density determined from the C-V curves in (a).

voltage, already described in Fig. 3(a), increases upon increasing the temperature. This latter suggests the occurrence of a thermally activated charge trapping process. Hence, in Fig. 4(b) the trap density, determined from the flat band voltage shift measured at each temperature, is reported in a semilog scale as a function of the reverse of the temperature. Evidently, the experimental data follows an Arrhenius dependence, as they can be well fitted by a linear relation. From the linear fit of the Arrhenius plot data, an activation energy of 0.1eV could be determined. Clearly, ab initio simulations would be required to associate our experimental activation energy to some specific defect of the material justifying the negative charge trapping. However, according to theoretical calculations reported in literature, point defects (e.g., oxygen vacancies) that act as electron trapping.[27] Moreover, also contaminants and residual carbon-related defects (which in our case can come from the ALD process or sample cleaning) have been demonstrated to act as electron traps in the Al_2O_3.[28]

In summary, in this letter the electrical properties of Al_2O_3 films grown by PEALD on thermally oxidized 4H-SiC have been investigated. The films exhibited high values of the permittivity (8.4) and breakdown strength (9.2MV/cm). Nevertheless, significant charge trapping phenomena take place upon positive bias stress (>10V), due to electron injection in the Al_2O_3 film. Electrical measurements at different temperatures and stress conditions allowed to determine the activation energy for this process (0.1 eV), which can be associated to the presence of points defects in Al_2O_3 (e.g., oxygen vacancies or carbon-related impurities). These results represent a step forward in the

comprehension of the trapping phenomena in Al_2O_3 films for 4H-SiC devices. In particular, these finding suggest to provide additional in oxygen-rich conditions (e.g., during ALD growth or post annealing treatments) as the main strategy to improve the properties of the Al_2O_3 films.

The authors would like to thank S. Di Franco and C. Bongiorno for their technical support during device processing and TEM analysis. Moreover, STMicroelectronics of Catania is acknowledged for the partial financial support under the research contract CDR.ST.CNR-IMM.06.03. 2014.007 D.B. Leg. Dept. n.7153.

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