Low-temperature all-solution-derived amorphous-oxide thin-film transistors

Phan Trong Tue, Jinwang Li, Takaaki Miyasako, Satoshi Inoue, and Tatsuya Shimoda

***Abstract*—We prepared thin-film transistors (TFTs) in which all the layers were fabricated using simple chemical solution-processed, vacuum-free routes, followed by thermal annealing at 400°C. A ruthenium oxide (RuO_2) film prepared via low-temperature processing was used for both gate and source/drain electrodes. Amorphous lanthanum–zirconium oxide (LZO) and zirconium–indium–zinc oxide (ZIZO) films were used as the gate insulator and channel layer, respectively, which enabled the fabrication of a TFT with the desired performance at a sufficiently low temperature. The ultraviolet-ozone (UV/O3) treatment was adopted to channel layer in order to facilitate precursor decomposition and condensation processes. As a result, the obtained "on/off" ratio, sub-threshold swing voltage, and channel mobility were approximately 6×10^5, 250 mV/decade, and 5.80 $cm^2V^{-1}s^{-1}$, respectively. This result contributes to the development of sustainable "completely printed inorganic electronics."**

***Index Terms*—chemical solution deposition, oxide thin-film transistors, transparent amorphous oxide semiconductors, low-temperature process, Zr-In–Zn–O**

I. Introduction

Oxide thin-film transistors (TFTs) are attractive building blocks for future display and optoelectronic devices because of their high-performance characteristics [1-3]. However, these TFTs are typically fabricated using cost-intensive vacuum-processing methods. Therefore, a lot of researches have been conducted on the development of chemical solution deposition (CSD) process as a true alternative for the fabrication of oxide TFTs [4-6], because CSD can offer many advantages such as low fabrication cost, high throughput, large area deposition, direct patternability, and direct printing of devices. However, these devices are only partially fabricated using CSD processes, with the other components still produced using conventional vacuum-based processes. Therefore, for further cost reduction, it is critical to utilize an all-CSD process in which all of the device components are fabricated from solution-derived materials.

In this study, by using low-temperature solution-processable RuO_2 electrodes for both gate and source/drain electrodes, an all-solution-processed high-performance all-oxide TFT was produced for the first time at a maximum process temperature of 400°C. Moreover the combination of a solution-processed La–Zr–O (LZO) gate insulator and a Zr–In–Zn–O (ZIZO) channel layer was contrived to have both high performance and good stability. For further improvement of TFT performance, ultraviolet-ozone (UV/O3) treatment was adopted.

II. Experimental

To prepare the TFT, a RuO_2 bottom gate (120 nm) was first formed using a CSD process. A RuO_2 precursor solution (0.35 mol/kg) was prepared by dissolving ruthenium (III) nitrosylnitrate [$Ru(NO)(NO_3)_3$, Sigma-Aldrich] in 2-methoxyethanol at room temperature (RT). The RuO_2 solution was spin-coated on a SiO_2/Si substrate, dried at 250°C for 5 min, and then annealed at 400°C for 20 min on a hotplate in ambient air. Second, an amorphous LZO gate insulator (120 nm) was deposited via CSD and annealed at 400°C for 10 min in O_2 using a rapid thermal annealing (RTA) system. In the third step, a ZIZO channel layer was formed using a CSD process and annealed at 400°C for 20 min in O_2 using the RTA system. Details of the LZO and RuO_2 precursor solutions and fabrication processes have been reported previously [7]. Fourth, a RuO_2 film was fabricated via CSD and dried at 200°C. Subsequently, the source and drain electrodes were patterned using photolithography and a dry-etching process. In the fifth step, the channel area was also patterned using photolithography and a dry-etching process, followed by post-annealing at 400°C in O_2 for 10 min. The fabricated TFT had a bottom gate electrode and a bottom contact structure with the channel length and width of 5 μm and 60 μm, respectively. For comparison, the devices fabricated with UV/O3 treatment for channel layers were evaluated. The details of UV/O3 treatment condition can be found elsewhere [8].

III. Results and Discussion

The thermal behavior of the precursor solutions was investigated using thermal gravimetric-differential thermal analysis (TG-DTA), as shown in Fig. 1. The first endothermic reactions involved large weight losses at temperatures below 110°C, which were due to solvent evaporation at low

Manuscript received Sep. 29, 2013. This work was supported by the ERATO, Shimoda Nano-Liquid Process Project, Japan Science and Technology Agency.

P. T. Tue, J. Li, S. Inoue, and T. Shimoda are with the Green Devices Research Center, Japan Advanced Institute of Science and Technology (JAIST), 2-13 Asahidai, Nomi, Ishikawa 923-1211, Japan (e-mail: phan-tt@jaist.ac.jp; lijw@jaist.ac.jp; s-inoue@jaist.ac.jp; tshimoda@jaist.ac.jp).

T. Miyasako is with JSR Corporation, Yokkaichi Research Center, Yokkaichi, Mie, Japan (e-mail: takaaki_miyasako@jsr.co.jp).

temperature. Exothermic peaks at approximately 250°C (RuO_2), 345°C (LZO), and 335°C (ZIZO), which corresponded to abrupt weight losses in the TG analysis, were observed. These losses were interpreted as the decomposition of the metal precursors to the corresponding metal oxides. Above these temperatures, no significant thermal reactions were observed, indicating that the thermal decomposition was complete, and that the organic groups were removed. Therefore, the annealing temperature was set at 400°C for the fabrication of all of the thin-film layers.

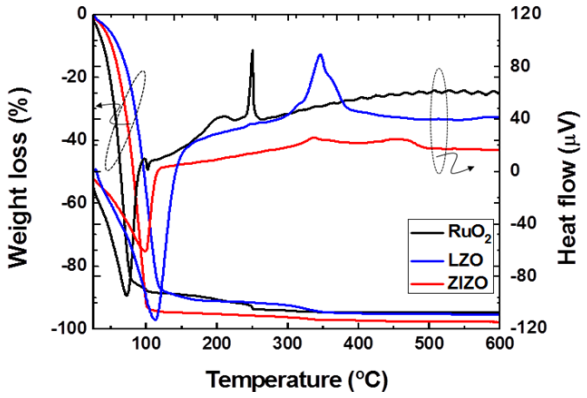

Fig. 1. TG-DTA analysis of the precursor solutions.

The crystallization of RuO_2 film was initiated at 250°C and facilitated with an increase in temperature. Consistently, the resistivity decreased at higher annealing temperatures. In particular, the 400°C-annealed film exhibited a resistivity of 4.3×10^{-4} Ωcm, which was several times lower than that of the reported solution-processed conductive oxides [9] and comparable to that of vacuum-processed films [10], even at a far lower processing temperature. In addition, atomic force microscopy (AFM) and scanning electron microscopy (SEM) images revealed a smooth (root mean square (RMS) ~ 2.8 nm) and homogeneous surface with particle sizes of 40–45 nm, which were suitable for insulator growth.

The LZO film exhibited a low leakage current density of < 10^{-6} A/cm^{-2} at an electric field of 1.0 MV/cm, which is consistent with the high film density of 4.65 g/cm^{-3}, as estimated from a X-ray reflectometry analysis. The dielectric constant and dielectric loss of the LZO film were determined to be 28 and 0.22%, respectively, at a frequency of 10 kHz. These values are typical for La-based high-κ dielectrics [11]. The large capacitance of the LZO was expected in order to realize a high-performance TFT. In addition, an atomically flat surface (RMS ~ 0.47 nm) was obtained with no crystalline grains, which is a key characteristic of the amorphous state.

A cross-sectional, high-resolution transition electron microscopy (TEM) image of the ZIZO/LZO interface region revealed a smooth and uniform interface without voids, signifying that there was no evident element interdiffusion (Fig. 2(a)). Halo patterns observed in the electron diffraction patterns of the ZIZO and LZO layers indicated the amorphous state of both layers (Fig. 2(b)), which was consistent with the XRD analysis (not shown here). Furthermore, the *secondary*

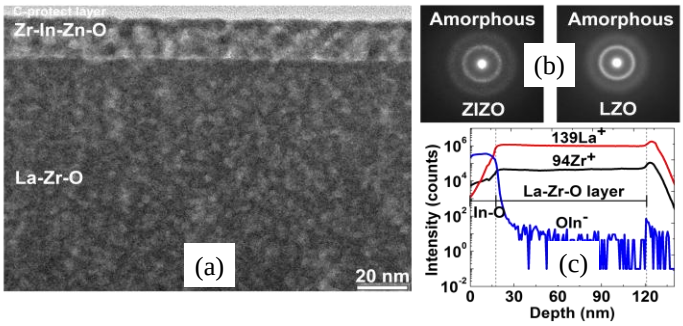

Fig. 2. (a) High-resolution TEM image, (b) electron diffraction patterns, and (c) SIMS profile across the ZIZO/LZO interface region.

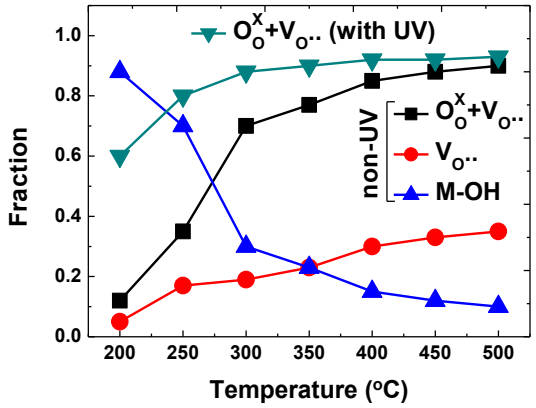

Fig. 3. Semiquantitative analysis of each component of XPS O1s spectra for ZIZO films annealed at different temperatures. O_O^x, $V_O^{\cdot\cdot}$, and M-OH denote the oxide lattice without oxygen vacancy, with oxygen vacancy, and hydroxide, respectively.

ion mass spectrometry (SIMS) analysis across the ZIZO/LZO interface region confirmed the occurrence of negligible elemental interdiffusion (Fig. 2(c)). Here, the $^{131}OIn^-$ ion was selected to eliminate the effect of sputtering and knocking during the SIMS measurement of In^+ ions. Consequently, a good MOS interface property was realized in the solution-derived ZIZO/LZO system. Note that the low-temperature process may have also minimized the interdiffusion.

In order to evaluate the electronic structure of the ZIZO films, X-ray photoelectron spectroscopy (XPS) was conducted. The O1s spectrum was deconvoluted into three peaks. These peaks, centered at 529.9, 531.5, and 532.7 eV, corresponded to lattice oxygen atoms in a fully coordinated environment, oxygen atoms in the vicinity of an oxygen vacancy, and hydroxide related group, respectively [6]. According to a semiquantitative analysis of each component for ZIZO films, as the annealing temperature increases from 200 to 500°C, the fraction of both oxide lattices increases from 0.12 to 0.9, whereas the fraction of hydroxide decreases from 0.88 to 0.1 (Fig. 3). In particular, the fraction of oxide lattice with oxygen vacancies ($V_O^{\cdot\cdot}$) rises from 0.11 to 0.35. . On the other hand, in order to effectively decompose organic- and hydrogen-based contents and to enhance the condensation in the ZIZO gel films, an UV/O3 treatment was carried out [8]. As a result, lower decomposition temperature and higher conversion rate from precursor to oxide were observed (Fig. 3). Particularly, both oxide lattices are present when the film is annealed at

200°C, and their fraction (~ 0.9) gets saturated when the films are annealed at below 300°C. It was also observed that the quantity of carbon-related impurities determined from the in-depth XPS profile of the C1s spectrum was very small in the bulk. Such a high-quality channel layer is of great importance for the production of high-performance and high-stability TFTs.

The transfer curves (Fig. 4(a)) clearly shows a typical n-channel characteristic with low operation voltage (less than ±10 V) because of the large capacitance of the LZO insulator. The obtained "on/off" current ratio, sub-threshold swing (*SS*) factor, and electron mobility (μ) were 2×10^5, 164 mV/decade, and 0.66 $cm^2V^{-1}s^{-1}$, respectively. The small *SS*-factor may originate from the large capacitance of the insulator and the good ZIZO/LZO interface properties, as anticipated from the TEM analysis. The transfer characteristics were greatly improved with the UV/O3 treatment (Fig. 4(b)). It has been reported that the mobility of metal oxide semiconductor films depends on the carrier concentration because the carrier transport is governed by the percolation conduction over the trap states and is enhanced at higher carrier concentrations by filling the trap states [1]. In addition, the conduction band minimum in metal oxide semiconductors should be primarily composed of dispersed vacant s-states with short interaction distances for efficient carrier transport, which can be achieved in ionic oxide but not obviously in hydroxide [12]. Therefore, in both cases, the observed degradation of the device performance with a decrease in the annealing temperature is related to the decrease of both oxide lattices and the increase of hydroxide. The improved mobility in the UV/O3 treated TFTs can be attributed to the higher conversion to the oxide from the precursor. The performance parameters of TFTs with and without UV/O3 treatment as a function of annealing temperature are summarized in Table 1.

TABLE 1. ELECTRICAL PERFORMANCE PARAMETERS OF TRANSISTORS FABRICATED WITH AND WITHOUT UV/O3 TREATMENT AS A FUNCTION OF THE ANNEALING TEMPERATURE

Annealing temp. (°C)	μ ($cm^2V^{-1}s^{-1}$)		SS (V/dec.)		V_T (V)	
	Non-UV	UV	Non-UV	UV	Non-UV	UV
250	0.0012	0.091	1.10	0.45	2.22	1.67
300	0.20	1.36	0.39	0.16	1.88	1.60
400	0.66	5.80	0.16	0.25	2.66	1.62
500	2.24	7.31	0.18	0.12	2.01	1.98

IV. CONCLUSION

A TFT was fabricated using only CSD processing for all of the layers, including the gate electrode, gate insulator, channel, and source–drain electrodes, at a maximum process temperature of 400°C. The UV/O3 treatment is effective for lowering process temperature and enhancing the performance through decomposition of organic- and hydrogen-based elements. This result is promising for the complete printing of sophisticated inorganic TFTs that could enable ultra-low-cost and low-energy devices.

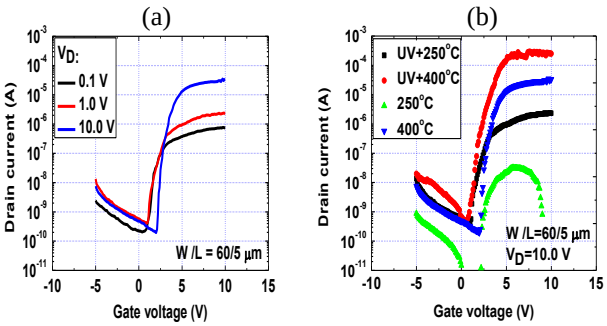

Fig. 4. Transfer characteristics of the TFT: (a) fabricated at 400°C without UV/O3 treatment, and (b) with UV/O3 treatment at different annealing temperatures.

REFERENCES

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488-492, Nov. 2004.

[2] J. F. Wager, "Transparent Electronics," *Science*, vol. 300, pp. 1245-1246, May 2003.

[3] L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, and T. J. Marks, "High-performance transparent inorganic-organic hybrid thin-film n-type transistors," *Nat. Mater.*, vol. 5, pp. 893-900, Nov. 2006.

[4] M.-G. Kim, H. S. Kim, Y.-G. Ha, J. He, M. G. Kanatzidis, A. Facchetti, and T. J. Marks, "High-Performance Solution-Processed Amorphous Zinc−Indium−Tin Oxide Thin-Film Transistors," J. Amer. Chem. Soc., vol. 132, pp. 10352-10364, Jul. 2010.

[5] D. H. Lee, Y. J. Chang, G. S. Herman, and C. H. Chang, "A General Route to Printable High-Mobility Transparent Amorphous Oxide Semiconductors," *Adv. Mater.*, vol. 19, pp. 843-847, Mar. 2007.

[6] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Sirringhaus, "Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process," *Nat. Mater.*, vol. 10, pp. 45-50, Jan. 2011.

[7] P. T. Tue, T. Miyasako, L. Jinwang, H. T. C. Tu, S. Inoue, E. Tokumitsu, and T. Shimoda, "High-Performance Solution-Processed ZrInZnO Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 60, pp. 320-326, Jan. 2013.

[8] K. Umeda, T. Miyasako, A. Sugiyama, A. Tanaka, M. Suzuki, E. Tokumitsu, and T. Shimoda, "Impact of UV/O_3 treatment on solution-processed amorphous $InGaZnO_4$ thin-film transistors," *J. Appl. Phys*, vol. 113, May 2013.

[9] T. Miyasako, B. N. Q. Trinh, M. Onoue, T. Kaneda, P. T. Tue, E. Tokumitsu, and T. Shimoda, "Totally solution-processed ferroelectric-gate thin-film transistor," *Appl. Phys. Lett.*, vol. 97, pp. 173509-3, Oct. 2010.

[10] C. Guerrero, J. Roldán, C. Ferrater, M. V. Garcia-Cuenca, F. Sánchez, and M. Varela, "Growth and characterization of epitaxial ferroelectric $PbZr_xTi_{1-x}O_3$ thin film capacitors with $SrRuO_3$ electrodes for non-volatile memory applications," *Solid-State Electronics*, vol. 45, pp. 1433-1440, Aug. 2001.

[11] Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, "Dielectric and electrical properties of amorphous $La_{1-x}Ta_xO_y$ films as higher-k gate insulators," *J. Appl. Phys*, vol. 105, pp. 034103-5, Feb. 2009.

[12] S. Jeong, Y. G. Ha, J. Moon, A. Facchetti, and T. J. Marks, "Role of Gallium Doping in Dramatically Lowering Amorphous-Oxide Processing Temperatures for Solution-Derived Indium Zinc Oxide Thin-Film Transistors," *Adv. Mater.*, vol. 22, pp. 1346-1350, Mar. 2010.