A WN_x Gate Self-Aligned GaAs p-Channel MESFET for Complementary Logic

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Abstract—**The Schottky barrier of reactively sputtered WN_x to p-type GaAs has been investigated. Postdeposition heat treatments above 500°C led to a reduction in the barrier height but for lamp annealing at 740°C the barrier heights are 0.68 eV. Self-aligned p-channel MESFET's were fabricated with WN_x gates by a refractory metal process involving the above heat treatment. The Schottky-barrier heights were close to the expected values. *K*-values of FET's with 2 μm × 24 μm gates were 0.088 mA/V², consistent with previously reported results. SPICE simulation studies carried out for a variety of complementary-type logic gates, indicate that power dissipation × delay time products of less than 10 fJ may be achievable over the power range 5–50 μW/gate. Thus complementary logic may be useful for applications where low power dissipation is at a premium.**

I. Introduction

THE DEVELOPMENT of GaAs IC technology has concentrated almost exclusively on logic systems, such as SCFL, BFL, or DCFL, which require only n-channel FET's. Complementary logic has received relatively little attention; mainly because p-channel FET's are expected to have poor performance due to the low hole mobility in GaAs. However, Zuleeg *et al.* [1] recently fabricated a 256-bit SRAM in GaAs using complementary JFET devices. They reported that the access time was poor but that the power dissipation was very low and this attribute might prove valuable for certain applications.

An alternative approach that may give higher speed is complementary MESFET circuitry (CMES), but a major problem is that Schottky-barrier heights to p-type GaAs are usually low, seriously limiting the logic swing of such systems. Nakayama *et al.* [2] developed a p-channel MESFET in GaAs using WSi_x as the gate metal, but the low Schottky-barrier height (~0.5 eV) prevented them from using enhancement-mode logic and instead they proposed a more complex circuitry based on depletion-mode devices.

We believe that the development of a gate metal with a higher Schottky barrier to p-type GaAs would be a significant advance for CMES technology. In the present work we have considered reactively sputtered WN_x as a gate metal. This material has been previously used as a Schottky contact for n-channel MESFET's [3] and the application of the same material to n- and p-channel devices would significantly simplify the complementary fabrication process. The work reported here deals with three aspects of CMES technology: Firstly, we evaluate WN_x as a Schottky metal to p-type GaAs. We describe the effect of postdeposition heating and suggest that WN_x might be applicable to p-channel MESFET's produced by a refractory-metal process [4].

In the next section we describe the fabrication of self-aligned p-channel GaAs MESFET's with WN_x gates. We show that these devices function successfully but that the transconductances are low, consistent with other workers' results [2]. However, our devices have relatively high Schottky barriers (0.68 eV), and we therefore believe that the WN_x gate is a very promising technology.

Finally, we use SPICE circuit simulations to investigate possible applications of these MESFET's to various complementary/quasi-complementary type logic circuits.

II. WN_x Schottky Contacts to p-Type GaAs

In the fabrication of self-aligned FET's using refractory metal technology the gate material is used as a mask for high dose implants to the source and drain regions. It is subsequently necessary to anneal the wafers at high temperature to activate these implants and the Schottky contact is required to withstand this heat treatment. Thus, in this work we have studied the effect of heating on the barrier height of WN_x Schottky contacts to p-type GaAs.

The wafer used in this study was from a horizontal Bridgemann crystal highly doped with Zn. Onto this had been grown a Zn-doped MOCVD epitaxial layer with a hole concentration of 5×10^{17} cm^{-3}. WN_x was deposited on the front face of the wafer by reactive sputtering of a tungsten target in a mixed Ar/N_2 atmosphere where the N_2 content was 12 percent. Just prior to mounting in the sputtering apparatus the wafer was dipped in HCl for 2 min to remove any native oxide and then rinsed in water. The WN_x film was patterned into Schottky diodes by using conventional photolithography followed by chemical dry etching in CF_4/O_2 mixed gas. At this stage the wafer was cut into 8 samples. The WN_x was then encapsulated in 3000 Å of phospho-silicate glass (PSG) and samples

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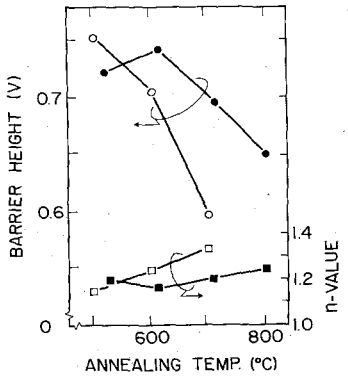

Fig. 1. Schottky-barrier height and ideality factor of WN_x on p-type GaAs as a function of postdeposition heat treatment. Open symbols refer to furnace annealed samples and solid symbols to lamp annealed.

either furnace annealed for 10 min or subjected to a rapid thermal pulse by lamp annealing. In the latter case samples spent about 4 s above 90 percent of peak temperature. Fabrication was completed by evaporating Au/Zn/Au ohmic contacts onto the back faces and alloying for 12 min at 400°C.

The Schottky-barrier heights (φ_B) and ideality factors (n) of the diodes were determined from the I–V characteristics using the standard thermionic emission model

$$\varphi_B = \frac{kT}{q} \ln\left(\frac{A^*T^2}{J_s}\right) \tag{1}$$

$$n = \frac{q}{kT}\left(\frac{\partial V}{\partial \ln I}\right) \tag{2}$$

where J_s is the current density at the zero voltage intercept of the I–V graph. A^* is the effective Richardson constant taken as 74 A · cm^{-2} · K^{-2} [5].

Fig. 1 shows the Schottky-barrier height and n-value for these diodes as a function of postdeposition annealing temperature. It is clear that postdeposition annealing has a serious adverse effect on the barrier height. These results can be compared with those previously reported by Uchitomi *et al.* [3] for WN_x Schottky barriers on n-type GaAs. In that work they found that annealing above 500°C caused an increase in the barrier height. Since the sum of the Schottky barriers to p-type and n-type material is understood to be equal to the bandgap [6], the present results and those of Uchitomi *et al.* [3] are consistent. The change in barrier height in n-type GaAs has been attributed to the annealing of surface damage that had been introduced during sputtering [7]. With our present data we cannot comment on that interpretation; for the purposes of the current work we simply note that reproducible Schottky barriers can be formed and that after lamp annealing at 740°C the barrier height is 0.68 eV. The latter point is stressed because this is the annealing condition we used in the fabrication of the p-channel MESFET described in the next section.

III. A p-Channel MESFET in GaAs

p-channel self-aligned GaAs MESFET's were fabricated by the process set out schematically in Fig. 2. The

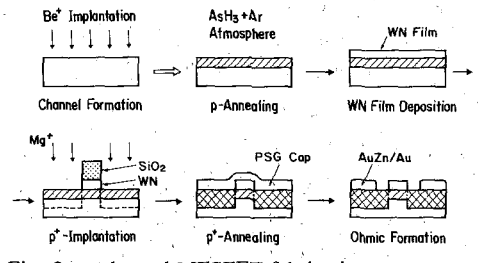

Fig. 2. p-channel MESFET fabrication process.

active channel was formed by selective 30-keV Be ion implantation at a dose of 5×10^{11} cm^{-2} directly into an undoped GaAs substrate. This implant was activated by capless annealing in flowing Ar/AsH_3, at 850°C for 15 min. Van der Pauw and C–V measurements on wafers implanted at slightly higher energies (50 and 70 keV) suggest that we should achieve an activation around 75 percent with negligible diffusion. The WN_x gate metal was deposited as described earlier and patterned by reactive ion etching [3]. The p^+ source and drain regions were fabricated by Mg ion implantation at 130 keV with a dose of 1×10^{13} cm^{-2} self-aligned to the WN_x gate. These implants were activated by lamp annealing at 740°C for 4 s; a higher temperature desirable to achieve higher activation efficiency could not be used since it would lead to an unacceptable deterioration in the Schottky-barrier height.

The first stage in the evaluation of the MESFET's was to check the performance of the WN_x Schottky gates. The forward I–V characteristics of 4 μm × 24 μm gates were measured and typical barrier heights were 0.68 ± 0.02 eV with n-values of 1.4 ± 0.1. The barrier height agrees well with the data of the last section, but the n-values are rather larger.

The voltage–current relationship of the FET's is given by the equation

$$I_{DS} = K(V_G - V_{th})^2 \tag{3}$$

where I_{DS} is the saturated drain–source current and V_G is the gate voltage. The parameters that characterize the FET are the threshold voltage V_{th} and the K-value. Fig. 3 shows the threshold voltages as a function of gate length. These FET's were operating in the enhancement mode with typical threshold voltages of −200 mV for long-gate devices. For FET's with a gate length of 1.5 μm or less the threshold voltage was higher indicating the presence of the so-called short-channel effect. Fig. 4 shows the K-value versus gate length, for 24-μm-width FET's. Typical K-values for 2 μm × 24 μm dimension were 0.088 ± 0.010 mA/V^2. The I–V characteristics of such a FET are shown in Fig. 5, where the maximum transconductance at $V_{DS} = -1.5$ eV and $I_{DS} = 20$ μA was 4.2 mS/mm. Two comments are relevant at this stage. Firstly, both the K-value and g_m are about a factor of 20 lower than is typically found for n-channel MESFET's of the same dimensions, presumably due to the difference in the electron and hole mobilities in GaAs.

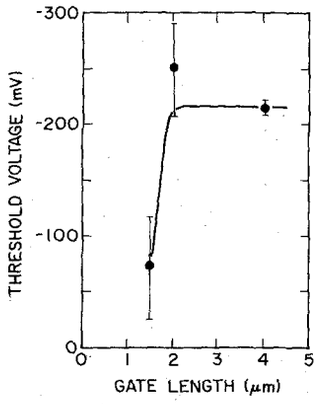

Fig. 3. Threshold voltage as a function of gate length in p-channel GaAs MESFET.

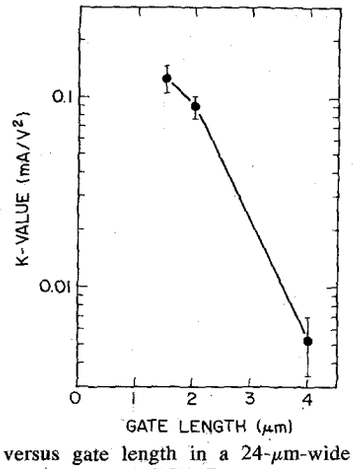

Fig. 4. K-value versus gate length in a 24-μm-wide p-channel GaAs MESFET.

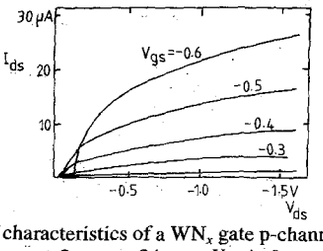

Fig. 5. Typical *I–V* characteristics of a WN_x gate p-channel MESFET. Gate dimensions are 2 μm × 24 μm. V_{GS} is 0 to −0.6 V.

Secondly, Nakayama *et al.* [2] reported *K*-values of 0.15 mA/V^2 for p-channel MESFET's of gate dimensions 1 μm × 20 μm. The difference in the *K*-value between those devices and the ones reported here is almost certainly due to differences in the gate size. However, it is not clear why Nakayama *et al.* could fabricate devices with 1-μm gate lengths with no short-channel effect, while in our wafers the effect occurs below 2 μm. Nevertheless, since this topic is of great technical importance a few comments are in order. The short-channel effect is often attributed to the lateral diffusion of the high-dose implant during its activating anneal. Comparing our process with that of Nakayama *et al.*, we used a lower implantation energy (130 compared with 150 keV) and a lower temperature anneal (740 compared with 950°C). Intuitively, we would expect our lower anneal temperature to cause less diffusion while our shallower implant means that any diffusion that does occur should have less influence on the threshold voltage.

However, short-channel effects are also influenced by piezoelectric effects arising from stress in the dielectric overlayer [8]. Unfortunately, comparative data for the two sets of devices are not available and we can only speculate that such effects might be significant in this case. Clearly this complex subject would warrant further work.

In conclusion, p-channel MESFET's were produced with Schottky-barrier heights of 0.68 ± 0.02 eV and *K*-values of 0.088 mA/V^2 for 2 μm × 24 μm gate dimensions.

IV. Complementary Logic Simulations

Our motivation for developing a p-channel MESFET was to assess complementary logic in GaAs. In this section we present the results of SPICE circuit simulations for various complementary/quasi-complementary logic circuits.

In this study we have used device parameters for n- and p-channel MESFET's with gate dimensions of 1.2 μm × 10 μm as set out in Table I. In Fig. 6 we show the four types of complementary/quasi-complementary logic gates considered in this study. The first (Fig. 6(a)) is entirely conventional enhancement-mode complementary logic. In an attempt to speed up the operation of this circuit we also considered a modification (Fig. 6(b)) where the p-channel device was operating in the depletion mode—in other words it never turned off. In this case the circuit operates in a quasi-complementary mode. A problem for both these circuits is that the supply voltage had to be limited to 0.75 V to prevent excessive leakage current across the p-channel Schottky contact as well as the n-channel Schottky contact. This limited both the logic swing and the speed of operation. This problem was solved by inserting level shifting diodes as indicated in Fig. 6(c). This enabled us to raise the supply voltage to 1.2 V which is an acceptable figure. Once again, we considered a modification (Fig. 6(d)) where the p-channel FET was operating in the depletion mode, as was the case for the type in (b).

To assess the transient behavior of these logic gates we simulated unloaded nine-stage ring oscillators for each circuit varying the sizes of each of the components. The results are shown in Fig. 7 on a graph of power dissipation against propagation delay time. Power-delay products of better than 10 fJ were found for power dissipations over the range 5–50 μW/gate, which could not be realized by using only n-channel FET circuitry. For certain configurations of circuit types *A* and *B*, high current densities were observed that were not accompanied by high switching speeds. For these circuits there was significant leakage across the p-channel Schottky contacts that contributed to the power dissipation without providing drive for the next inverter stage. It should be noted here that quasi-complementary circuit approaches offer a variety of selections with respect to power level. This enables designers to choose the most desirable power dissipations for

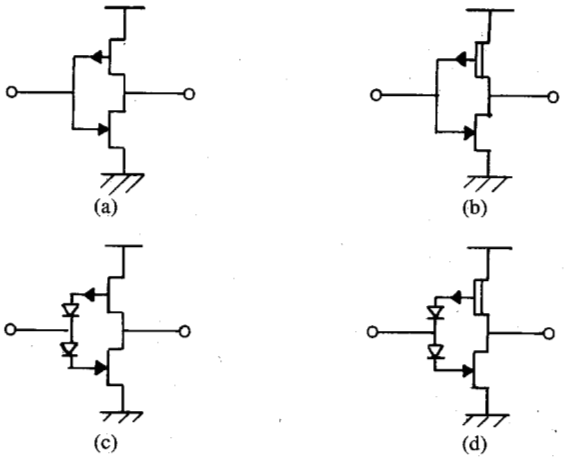

Fig. 6. Four alternative complementary-type logic gates studied by SPICE simulation. (a) Conventional complementary logic. (b) Quasi-complementary logic. (c) Complementary logic with level-shifting diodes. (d) Quasi-complementary logic with level-shifting diodes.

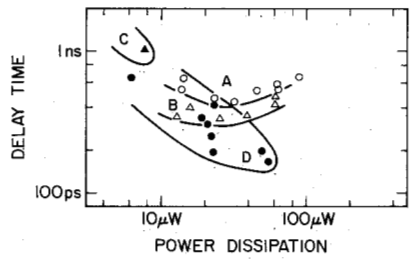

Fig. 7. Simulated power dissipation and propagation delay times for nine-stage ring oscillators using different configurations of the complementary type circuits shown in Fig. 5. Letters indicate the gate type using the naming convention of Fig. 4, where ○ indicates circuit type *A*, △ ≡ *B*, ▲ ≡ *C*, and • ≡ *D*.

TABLE I
FET PARAMETERS USED FOR SPICE SIMULATION STUDIES
(Each value represents a FET with gate dimensions of 1.2 μm × 10 um.)

Parameter	n-channel FET	p-channel FET
K-value (A/V^2)	1.2E-3	0.06E-3
Lambda (V^{-1})	0.14	0.14
Rs (Ω)	100	500
Rd (Ω)	100	500
C_{GS}(F)	6.7E-15	6.7E-15
C_{GD}(F)	6.7E-15	6.7E-15
φ_B(eV)	0.73	0.66
Is (A)	5E-17	5E-16

their particular application considering speed–power trade-offs.

The fastest gate simulated was for a configuration of the gate in Fig. 6(d) where the delay time was 164 ps with a power dissipation of 54 μW. This result is very similar to that found previously by Nakayama *et al.* [2] except that their gate involved four transistors compared with the two used here. These gates are operating very slowly compared with DCFL [3] but at much lower power dissipation. Thus complementary logic seems most promising for applications where low power dissipation is of prime importance.

V. SUMMARY

In this study we have been assessing GaAs MESFET technology that includes p-channel FET's for circuit operation in a complementary fashion. We have shown that WN_x can provide a good Schottky barrier to p-type GaAs that can withstand a limited amount of postdeposition heating. A Schottky-barrier height of 0.68 eV was found after lamp annealing at 740°C.

Self-aligned p-channel GaAs MESFET's were fabricated with WN_x gates. *K*-values of 0.088 mA/V^2 were measured for FET's with 2 μm × 24 μm gate dimensions.

SPICE simulation studies indicated power-delay products lower than 10 fJ over a range of power dissipations.

There remain some problems. The performance of complementary/quasi-complementary circuits has only been simulated and fabrication will require adjustments to the n-channel and p-channel processes to allow integration on the same chip. In particular, the adverse effect of heating on the WN_x Schottky contact to p-type GaAs is expected to be a limitation. Nevertheless, complementary MESFET logic in GaAs appears to be a promising technology for the future, especially in applications where low power dissipation is important.

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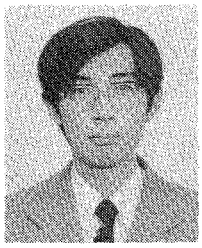

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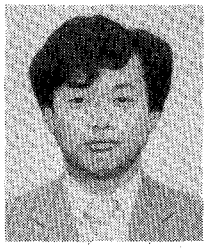

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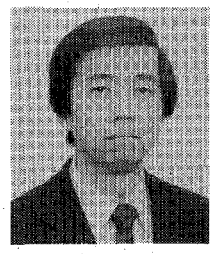

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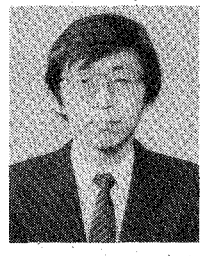

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