Low Power CMOS Chopper Preamplifier Based on Source-Degeneration Transconductors

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***Abstract*—This paper describes the design of a low-power, low noise CMOS chopper preamplifier for sensor signal conditioning. The core amplifier and the Gm-C output low pass filter of the proposed fully differential preamplifier are based on a source degeneration transconductor. The circuit was designed in a standard $0.18\mu m\ CMOS$ process with $1.8V$ supply voltage. It shows $42dB$ gain, $1\ kHz$ bandwidth and a total power consumption of $84\ \mu W$. The proposed configuration achieves a noise efficiency factor of 4.6 and a total input-referred noise of $560\ nV_{rms}$ integrated from 0.1 to $1\ kHz$.**

***Index Terms*—Low-noise Preamplifier, Chopping Technique, Analog Front-End.**

I. Introduction

Preamplifiers are fundamental building blocks in sensor signal conditioning, as they primarily determine the performance of the whole acquisition system. They are required to amplify, with a well-defined gain, very weak differential signals, in the order of mV or μV, with minimum power consumption in order to comply with portable, wearable and implantable application requirements [1-2]. High common-mode rejection ratio (CMRR) and high power supply rejection ratio (PSRR) are also necessary to attenuate environmental interference. Furthermore, many sensors provide output signals near DC with a few Hz bandwidth, especially in biosignal acquisition systems [3-6], so flicker noise is the main source of intrinsic noise. In order to reduce the low frequency noise, dynamic offset cancellation techniques are used, which can be classified into two groups: auto-zero and chopping [7]. The auto-zero technique consists in first sampling and then subtracting the offset and low frequency noise of the amplifier, but undersampling of the broadband noise results in an increased thermal noise contribution. The chopping technique, in turn, is a continuous time modulation technique in which the signal is translated to higher frequency, amplified and demodulated back to baseband, whereas the flicker noise is only modulated once and then filtered. As there is no noise undersampling, the residual noise is lower than with the auto-zero technique.

In this paper a fully differential low power chopper preamplifier is presented. The core amplifier is based on a source-degenerated transconductor to provide a well-defined gain and higher bandwidth than open-loop operational transconductance amplifiers, thus avoiding phase shift between the input and output modulators. The output low-pass filter is based on the same transconductor with reduced power consumption, so a low noise efficiency factor (NEF) is achieved for the whole preamplifier. The paper is organized as follows. Section II presents the block diagram of the proposed system and some design considerations. The core amplifier and its characteristics are described in Section III, and the low power first-order $Gm-C$ filter is presented in Section IV. Simulation results and comparison with previous low noise preamplifiers are provided in Section V. Finally, some conclusions are drawn in Section VI.

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II. Proposed Preamplifier

Figure 1 shows the block diagram of the proposed preamplifier. It is designed to process input signals from $5\mu V$ to $1mV$ with frequencies from $0.1Hz$ to $250Hz$. The core amplifier (CA) must provide a gain about $40dB$ or higher, to ensure that it determines the overall noise of the acquisition system, and must be carefully designed to reduce its intrinsic noise contribution. The chopper technique is applied to the CA by means of an external chopper modulator $CH1$, an internal chopper modulator $CH2$ embedded in the output stage of the CA, and a $Gm-C$ low-pass filter (LPF).

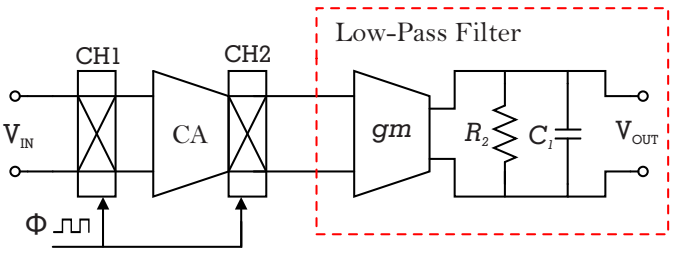


Fig. 1. Proposed Low-Noise System.

The input modulator $CH1$ consists of four transmission gates to reduce charge injection [7], whereas the output modulator $CH2$ makes use of the low impedance nodes generated

by cascode transistors, as shown in the next Section, thus reducing glitches and resulting in a more compact solution. The chopper modulators are controlled by a square wave signal with frequency $f_{chop} = 100kHz$. Finally, the LPF is based on the same transconductor cell as the CA, with reduced power consumption and a cut-off frequency of $1kHz$ to eliminate the modulated noise components.

III. Core Amplifier (CA)

The CA consists of a flipped-voltage follower (FVF) based source degenerated transconductor, as shown in Figure 2. The DC current through the input transistors M_1 and M_2 is held constant which, together with the low impedance node established at their source terminals, results in unity voltage gain and high current sourcing capability [8]. The output current through M_5 and M_6 is therefore determined by the differential input voltage and the degeneration resistor R_S. The output current is copied through M_7 and M_8 and converted into a differential output voltage by means of resistor R_L, so the gain of the CA is $M \cdot R_L/R_S$, where M is the gain of the current mirror. Cascode transistors M_{SW} in the output branches constitute the output modulator $CH2$, whereas M_3 and M_4 were added to increase the accuracy in the copy of currents. The common mode feedback (CMFB) circuit, not shown in the Figure, consists of a differential difference amplifier [9].

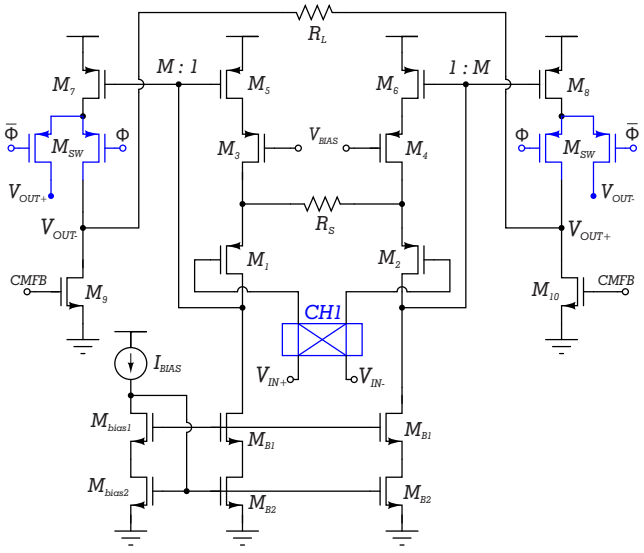


Fig. 2. Core Amplifier.

The input-referred flicker noise of the CA is given by:

$$V_{n,1/f}^2 = \frac{2}{C_{ox}f}\left[\frac{K_p}{(WL)_1} + g_{m5}^2 R_S^2\left[\frac{K_p}{(WL)_5} + \frac{K_p}{(WL_7)}\right]\right] + \frac{2}{C_{ox}f}\cdot\frac{g_{mB2}^2(1+g_{m1}R_S)^2}{g_{m1}^2}\cdot\frac{K_n}{(WL)_{B2}} + \frac{2}{C_{ox}f}\cdot\frac{g_{m9}^2}{g_{m7}^2}\cdot g_{m5}^2 R_S^2\cdot\frac{K_n}{(WL)_9} \quad (1)$$

where K_n and K_p are technology dependent constants, C_{ox} is the oxide capacitance, f is the frequency, and g_{mi} and $(WL)_i$ are the transconductance and area of transistor M_i, respectively. As R_S and R_L are linear polysilicon resistors, they only contribute with thermal noise, which is not taken into account in eq. (1). If transistors M_7-M_8 are designed M times wider than M_5-M_6 to provide some gain to the current mirror, their area and transconductance are also M times higher. Therefore, assuming $g_{m1}R_S >> 1$, eq. (1) can be rewritten as:

$$V_{n,1/f}^2 = \frac{2\cdot K_p}{C_{ox}f}\left[\frac{1}{(WL)_1} + \frac{g_{m5}^2 R_S^2(1+M)}{M(WL)_5}\right] + \frac{2\cdot K_n}{C_{ox}f}\left[\frac{g_{mB2}^2 R_S^2}{(WL)_{B2}} + \frac{g_{m9}^2 R_S^2}{M^2(WL)_9}\right] \quad (2)$$

The gain M of the current mirror should be chosen higher than 1 to reduce flicker noise. However, there is a trade-off between the reduction in flicker noise and the increase in power consumption due to the increase in the current through the output branches. For this reason, $M = 1.5$ was chosen. Also, as K_p is lower than K_n, it is preferable to use a PMOS FVF input, and in order to obtain the highest power efficiency, and thus the best noise-power trade-off, large area transistors operating in the weak inversion region are used. Table I summarizes the sizes of the transistors. The bias current of the amplifier is $I_{bias} = 5\mu A$, the degeneration resistance $R_S = 1k\Omega$, and the output resistance $R_L = 100k\Omega$. The main characteristics of the CA are shown in Table II. The amplifier shows an input-referred noise of $9.7\mu V_{rms}$, integrated in the noise-bandwidth (from 0.1 to $880kHz$), and $70\mu W$ power consumption. The input-referred noise integrated from 0.1 to $1kHz$, which will be the integration range after applying the chopping technique to the CA, is $1\mu V_{rms}$.

TABLE I
Transistor Sizes

	$W(\mu m)$	$L(\mu m)$
$M_{1,2}$	528	1
$M_{3,4}$	28	1
$M_{5,6}$	88	1
$M_{7,8}$	132	1
$M_{9,10}$	352	1
M_{B1}	112	1
M_{B2}	352	1

TABLE II
Characteristics of the Core Amplifier

	Core Amplifier
Gain	40 dB
Bandwidth	560 kHz
Power	70 μW
CMRR	74 dB @250 Hz
PSRR	70 dB @250 Hz
THD @$1mV_{pp}$	0.5 % @250 Hz
Input-Referred Noise	9.7 μV_{rms}

IV. Filter Design

Figure 3 shows the first-order fully differential Gm-C filter used as the output LPF in the chopping technique. Although it is based on the same FVF transconductance topology as the CA, it was redesigned to contribute less than 20% to the power consumption of the whole preamplifier. This implies higher noise, but as the filter is preceded by the low noise high gain CA, its noise contribution to the proposed preamplifier is still negligible.

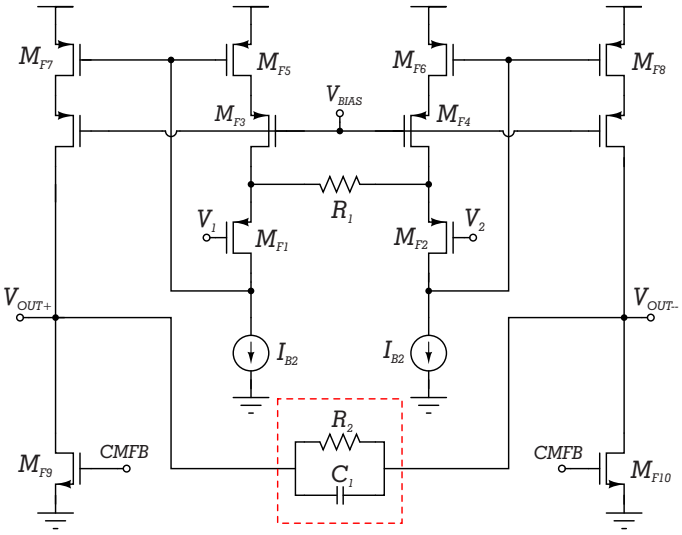


Fig. 3. First-order Gm-C filter.

The transfer function of the filter is given by:

$$H(s) = \frac{R_2}{R_1(1 + sC_1R_2)} \tag{3}$$

The cut-off frequency was chosen $f_c = 1kHz$ to filter out the noise components modulated by $CH2$ and process input signals up to $250Hz$. To achieve such a low cutoff frequency, large capacitive and resistive values are required, which implies large area consumption if passive components are used. For this reason, resistors R_1 and R_2 were implemented as pseudo-resistors, as shown in Figure 4. The PMOS transistors are biased in the weak inversion region with bulk-drain or bulk-source terminals shorted. This pseudo-resistor exhibits a weak dependence on V_{12}, which results in a large resistance with moderate linearity for the input voltage ranges of the system [10].

In this way, a resistance $R_2 = 4.5M\Omega$ is achieved, which only takes $0.52\mu m^2$ active area, as each transistor size is $W/L = 0.36\mu m/0.36\mu m$. To establish the $1kHz$ cut-off frequency, a capacitance $C_1 = 35pF$ is required. The DC gain of the filter is 2, providing some additional gain to the preamplifier. Finally, the power consumption of the proposed Gm-C filter is $14\mu W$ and its input-referred noise is $6\mu V_{rms}$.

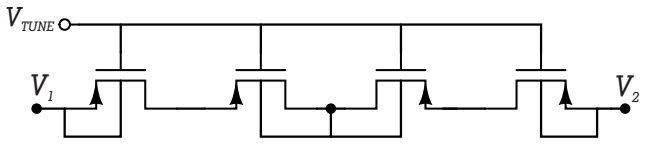


Fig. 4. Pseudo-Resistor Implementation.

V. Simulation Results

The proposed circuit was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage, and consumes $84\mu W$ total power. The preamplifier frequency response is shown in Figure 5. The circuit presents a differential gain of $42dB$ and $1kHz$ bandwidth. Figure 6 shows the time response for a $500\mu V$ amplitude sine input signal at $250Hz$. The demodulated and amplified input signal is shown before filtering the modulated noise (Fig. 6a), and the output of the LPF (Fig. 6b). The total harmonic distortion under these conditions is 1.5%.

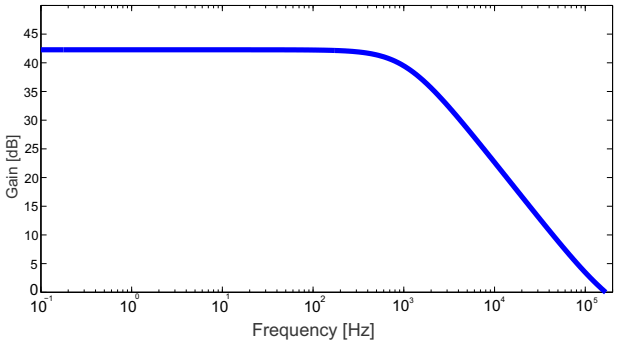
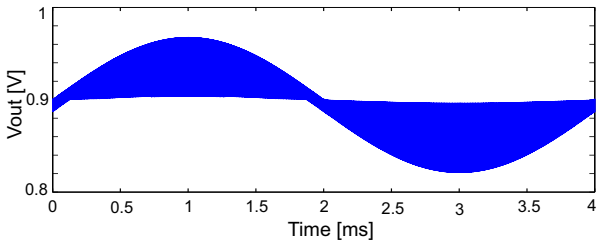
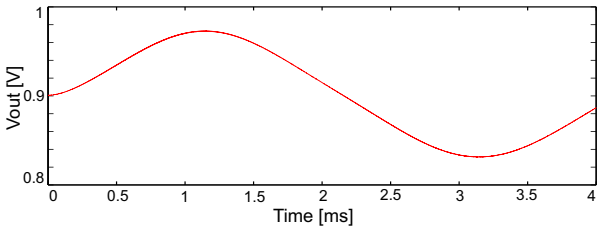


Fig. 5. Preamplifier frequency response.



(a)



(b)

Fig. 6. Waveforms at the a) input and b) output of the LPF.

The trade-off between the input-referred noise and the current consumption of the amplifier is usually expressed in terms of the noise efficiency factor (NEF) [11]:

$$NEF = V_{ni,rms} \cdot \sqrt{\frac{2 \cdot I_{total}}{\pi \cdot 4kT \cdot V_t \cdot BW}} \quad (4)$$

where $V_{ni,rms}$ is the input-referred noise voltage integrated in the bandwidth of the preamplifier BW, I_{total} is the current consumption, V_t is the thermal voltage, k is the Boltzmann constant and T is the temperature. Another figure of merit used to compare the design of amplifiers operating with different supply voltages is the power efficiency factor (PEF), defined as $NEF^2 \cdot V_{DD}$. The smaller the PEF, the better the trade-off between noise and power consumption.

The equivalent input-referred noise power spectral density of the core amplifier and the proposed chopper preamplifier is shown in Figure 7. At $250Hz$ the input-referred noise decreases from $24.5nV/\sqrt{Hz}$ without the chopping technique, to $14.5nV/\sqrt{Hz}$ with the chopping technique. When integrated from $0.1Hz$ to $1kHz$, the input-referred noise is $1\mu V_{rms}$ for the CA, and $0.56\mu V_{rms}$ for the whole configuration. The efficiency factors of the proposed preamplifier are $NEF = 4.6$ and $PEF = 38V$.

Table III shows a comparison with previous implementations found in the literature. Although reference [5] achieves the lowest NEF and PEF, no information about linearity is provided. As shown in the table, the proposed preamplifier is very competitive, as it provides an excellent trade-off between all the relevant parameters, with low NEF and PEF, high CMRR and PSRR and moderate linearity.

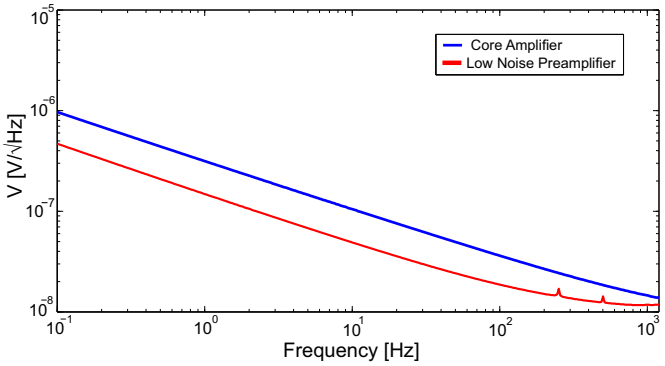


Fig. 7. Square root of the input-referred power spectral density.

VI. Conclusions

A low power low noise preamplifier designed in a $0.18\mu m$ CMOS process with $1.8V$ supply was presented in this paper. It uses a source degeneration transconductor as building block to design the core amplifier (CA) and the Gm-C output filter. A careful design process was undertaken to achieve the best noise-power trade-off in the CA and thus achieve the best efficiency factors after applying the chopping technique. The proposed preamplifier shows an input-referred noise of $0.56\mu V_{rms}$ in an integration bandwidth of $0.1Hz$ to $1kHz$, 1.5% THD for a $1mV_{pp}$ input signal at $250Hz$, and power consumption of $84\mu W$. The efficiency factors are $NEF = 4.6$ and $PEF = 38V$.

TABLE III
Performance Comparison of Preamplifiers

	[4]	[5]	[6]	This Work
Technology (μm)	0.18	0.18	0.13	0.18
Power Supply (V)	1.8	1.2	1	1.8
Gain (dB)	48/60	40-54	55	42
Bandwidth (Hz)	1-8000	1-100	0.01-100	0.1-1000
Power (μW)	11	0.8	2.3	84
CMRR (dB)	48	105	125	74 *@250 Hz*
PSRR (dB)	55	-	-	70 *@250 Hz*
THD (%)	1.2 *@1 mV*	-	-	1.5 *@1 mV*
Input-Referred Noise (μV_{rms})	5	1	0.75	0.56
NEF	5.3	3.3	4.5	4.6
PEF (V)	50	13	20	38

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