A 50μW 2.45GHz Direct-Conversion RX with On-Chip LO with -84dBm Sensitivity for 1Mb/s GFSK

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ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC) | 979-8-3503-0420-6/23/$31.00 ©2023 IEEE | DOI: 10.1109/ESSCIRC59616.2023.10268743

***Abstract*— In this paper, an ultra-low-power 2.45GHz mixer-first low-IF receiver front-end is presented. To have extremely low power consumption, a technique for implementing an on-chip low-power local oscillator is proposed that contains a 9-stage pseudo-differential ring oscillator operating at 1/9 of the RF frequency. As well as reducing the power consumption, this technique results in having a lower $1/f^3$ phase noise corner frequency. The proposed front-end is fabricated in GF22nm FDSOI technology. It consumes 50μW and has 2x less power than the state-of-the-art while having competitive calculated sensitivity of -84dBm for 1MHz GFSK demodulation.**

***Keywords*— 2.4GHz RX, harmonic down-conversion, mixer-first RX, N-path passive mixer, ultra-low-power, wake-up receiver (WuRX)**

I. Introduction

The Internet of Things (IoT) requires ultra-low-power RF receivers (RXs) for e.g. Bluetooth Low Energy (BLE), wake-up RXs (WuRXs) [1], and clock harvesting RXs [2]. Energy detectors [3] burn sub-micro-watt power but they are optimized for low data rate (8.192kb/s). They disqualify as WuRX for BLE/WiFi as they have about 30dB inferior sensitivity compared to the main RX [4]. Low-IF RXs offer a better trade-off in power vs sensitivity but most of the power is burned in the local oscillator (LO) and its buffers [2].

This paper focuses on minimizing the power of the RX including generating LO signals. Extremely low power consumption of 50μW is achieved by 1) avoiding gain at RF by having a mixer-first RX, 2) having a ring oscillator (RO) operating at 9x lower frequency than f_{RF} (f_{RO}=f_{RF}/9), 3) introducing an edge-combiner (EC) circuit to have 3x frequency multiplication and generate proper phase differences for a 3-path differential mixer, and 4) using the 3rd harmonic of the LO for down-conversion with a 3-path mixer to achieve input matching with small mixer switch size. These design choices enable us to have the minimum possible transistor size (80nm/20nm in GF22nm) for the RO, ECs, and LO buffers for a record low power consumption that may further scale with technology.

II. General Concept of the Proposed Circuit

Fig. 1a shows the general concept of the proposed RX structure consisting of LO generation, passive mixer, and IF amplifiers. Here, M is the factor that we multiply our RO frequency with, and N is the harmonic of the LO used for down-conversion. This is a generalized mixer structure of the three-phased version proposed in [5] that only retains the

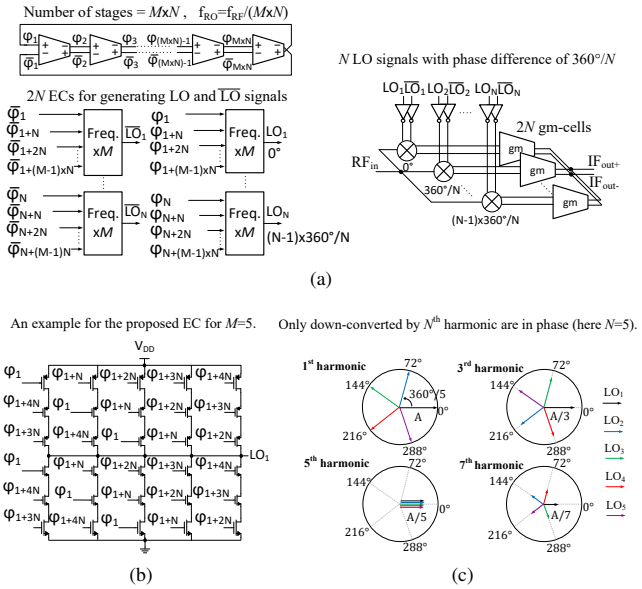

Fig. 1. (a) Proposed structure for the RX front-end; (b) Suggested implementation of ECs; (c) Illustration of N^{th} harmonic down-conversion.

down-converted signal by the N^{th} harmonic. It requires N LO signals with 360°/N phase difference and 50% duty-cycle for each mixer switch, which can be efficiently produced with our proposed LO generation technique. With N paths in parallel, the same conversion gain that could have been achieved by the main harmonic is obtained even if the N^{th} harmonic is used (see Fig. 1c). The equivalent LTI circuit of the N-path mixer structure is shown in Fig. 2 and its input impedance is [5]:

$$Z_{\text{in},N} = \frac{R_{\text{SW},N} + (R_{\text{sh,N}} \,\|R_{\text{IF}}\|\, Z_{\text{C}_{\text{IF}}})}{N} \tag{1}$$

If $R_{\text{IF}}, Z_{\text{C}_{\text{IF}}} \to \infty$, for the equivalent shunt resistor, we have:

$$R_{\text{sh},N} = \frac{2\gamma\,(R_{\text{S}} + R_{\text{SW},N})}{N^2 - 2\gamma}, \quad \gamma = \frac{2}{\pi^2} \approx 0.203 \tag{2}$$

If $Z_{\text{in},N} = R_{\text{S}}$, for the switch resistance, we have:

$$R_{\text{SW},N} = R_{\text{S}} \times \frac{N\left(N^2 - 2\gamma\right) - 2\gamma}{N^2} \tag{3}$$

Using (3), mixer switch sizes for different harmonics are:

$$\begin{aligned} \text{R}_{\text{SW}[1,3,5]} &= [0.2, 2.7, 4.9] \cdot \text{R}_{\text{S}}, \\ \text{W}_{\text{SW}[1,3,5]} &= [1, 0.07, 0.04] \cdot \text{W}_{\text{S}} \end{aligned} \tag{4}$$

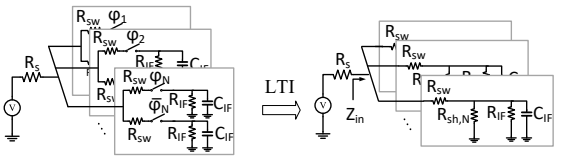

Fig. 2. Linear time-invariant model of the N-path mixer used in [5].

As a result, this mixer structure enables us to use smaller mixer switch size to achieve input matching and also leads to LO buffers operating at N times lower frequency. In subsection A, it is explained that combining this mixer structure with the proposed ECs can lead to a much lower power LO by further reducing its frequency, a fully symmetrical design for better phase noise (PN), and lower $1/f^3$ PN corner frequency [6].

A. Constraints for M and N

Table 1 shows the effect of M and N on power consumption and $1/f^3$ PN corner of the RO. Larger N leads to the LO operating at a lower frequency, while requiring smaller mixer switches for input matching (see (4)) and consequently smaller LO buffer size. The proposed structure scales the required buffer size so aggressively, that $N = 3$ already corresponds to the minimum buffer size in our IC process. Also, the number of switches increases with N, leading to burning more power on the IF side to get the same noise figure (NF) and not degrade the sensitivity. So N is chosen to be 3 in this design because of this power-sensitivity trade-off. Increasing M increases the number of stages at a very low power penalty (see Table 1) as ECs are minimum-sized and are switching at speeds well below f_{RF}, but will result in pushing the $1/f^3$ corner to lower frequencies as it decreases inversely with the number of stages [6]. Going for more than 3-stages also means sharper edges, higher oscillation amplitude, and not requiring any level-shifting for LO buffers. However, a higher M requires more complex ECs, that burn more power and need higher oscillation amplitude (supply voltage) to work properly, as more transistors are being stacked (see Fig. 1b). Also, further increasing M starts to degrade the PN as the number of RO inverters (noise contributors) becomes too high [6]. That is why M is chosen to be 3. Although minimizing power while achieving input matching is the main focus, NF and PN of the RO also need to meet targeted system requirements of sensitivity <-80dBm for GFSK (BER of 10^{-3}), resulting in NF < 24dB with 10dB SNR and 1MHz bandwidth, and PN<-80dBc/Hz at 1MHz offset [7].

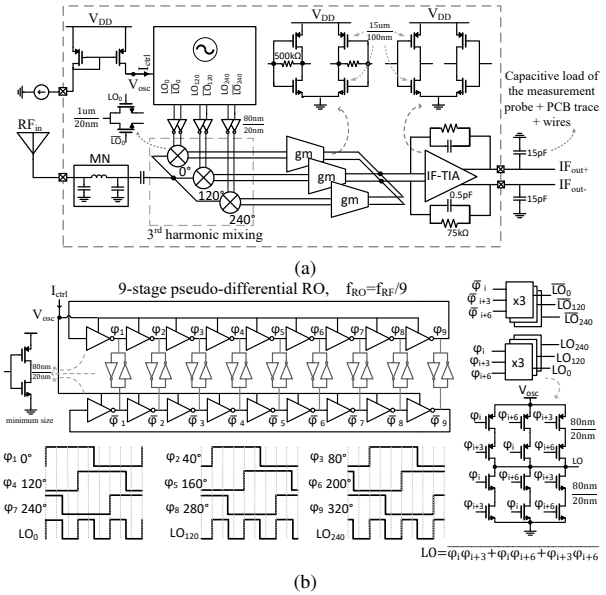

Fig. 3. (a) Implemented RX with M=N=3; (b) LO generation technique.

B. Block diagram of the implemented ultra-low-power RX

The block diagram of the implemented ultra-low-power RX can be seen in Fig. 3a. After 7.5dB of passive voltage gain via the on-chip matching network (MN) (to be shared with a higher-end RX of which the estimated parasitics have been included), the RF input is down-converted to IF with a 3-path differential mixer. The optimum mixer switch size for impedance matching is given in (3), but it can be compromised to improve the NF of the mixer. As a larger mixer switch leads to less noise, we increased the calculated value and settled on 1μm/20nm which could still be driven by minimum buffer size and yet achieve S_{11}<-10dB, while reducing the NF of the mixer from 23dB to 19dB. The parasitic capacitors of the

Table 1. The effect of M and N on power consumption and PN $1/f^3$ corner frequency.

M	N	# RO stages	f_{RO}	$I_{\text{RO}}^{\diamond}$	PN $1/f^3$ corner	# ECs	Mixer switch width$^{\bullet}$	Buffer width$^{\bullet}$	# gm-cells	P_{RO}	P_{ECs}	P_{Buffers}	$P_{\text{gm-cells}}$	P_{calc} (μW)	P_{sim} (μW)
1	1	3	f_{RF}	I	f_C	0	W_S	W_B	1	P_{RO}	0	P_{Buff}	P_{gm}	80.6	85.0
1	3	3	$f_{\text{RF}}/3$	I/3	f_C	0	$0.07W_S$	$0.07W_B$	3	$1/3P_{\text{RO}}$	0	$0.07P_{\text{Buff}}$	$3P_{\text{gm}}$	26.3	26.5
1*	3	9	$f_{\text{RF}}/3$	I	$f_C/3$	0	$0.07W_S$	$0.07W_B$	3	P_{RO}	0	$0.07P_{\text{Buff}}$	$3P_{\text{gm}}$	41.5	45.0
3**	3	9	$f_{\text{RF}}/9$	I/3	$f_C/3$	6	$0.07W_S$	$0.07W_B$	3	$1/3P_{\text{RO}}$	$6P_{\text{x3EC}}$	$0.07P_{\text{Buff}}$	$3P_{\text{gm}}$	27.5	27.5
1	5	5	$f_{\text{RF}}/5$	I/3	$3f_C/5$	0	$0.04W_S$	$0.04W_B$	5	$1/3P_{\text{RO}}$	0	$0.04P_{\text{Buff}}$	$5P_{\text{gm}}$	34.7	36.0
3	5	15	$f_{\text{RF}}/15$	I/3	$f_C/5$	10	$0.04W_S$	$0.04W_B$	5	$1/3P_{\text{RO}}$	$10P_{\text{x3EC}}$	$0.04P_{\text{Buff}}$	$5P_{\text{gm}}$	36.7	38.0
5	5	25	$f_{\text{RF}}/25$	I/3	$3f_C/25$	10	$0.04W_S$	$0.04W_B$	5	$1/3P_{\text{RO}}$	$10P_{\text{x5EC}}$	$0.04P_{\text{Buff}}$	$5P_{\text{gm}}$	37.7	38.5

$\star\star$ Our design (in gray) $\star$ M=1, N=3 and 9 stage RO is the structure used in prior art [5] $\bullet$ Minimum L is considered for both L_S and L_B
$\diamond$ Current consumption of I is considered for RO stages=3 and f_{RO}=f_{RF} $\rightarrow$ I_{RO}=I$\times$($f_{\text{RO}}/f_{\text{RF}}$)$\times$(# RO stages/3)
Parameters' value for P_{calc}: P_{RO}=22.8μW, P_{Buff}=52.8μW, P_{gm}=5μW, P_{x3EC}=0.2μW, P_{x5EC}=0.3μW, f_{RF}=2.4GHz, W_S=14.3μm, W_B=1.1μm

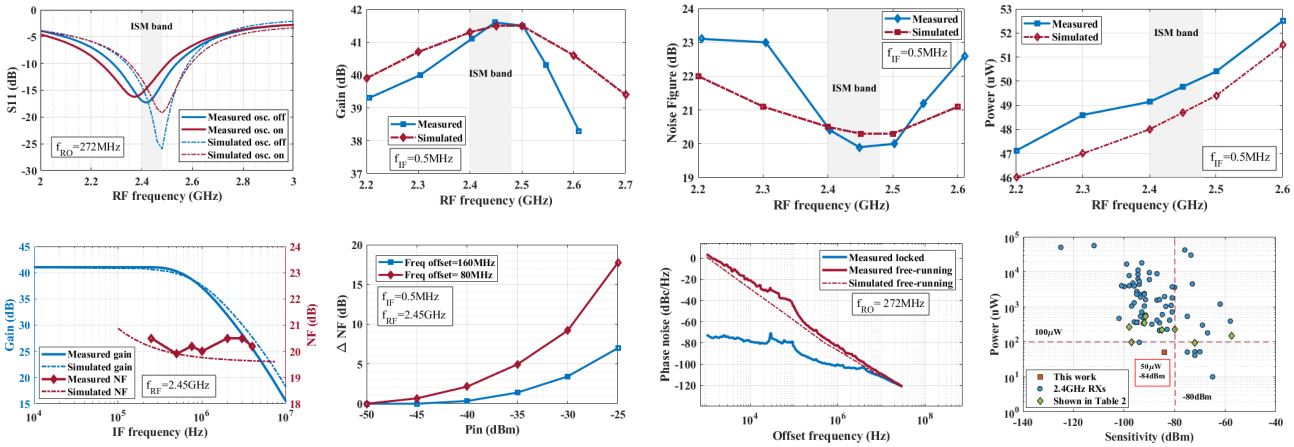

Fig. 4. Measurements and post-layout simulations of S_{11}, and gain, NF, power vs f_{RF} (1st row) and frequency response and NF, NF degradation due to interference while free running, LO PN while free running and locked, and power vs sensitivity of 2.4GHz RXs with similar-range IF BW [4] (2nd row).

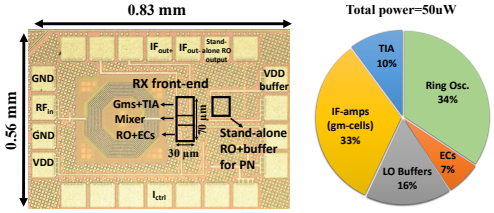

Fig. 5. Die photograph and RX power consumption break-down.

gm-cells act as the mixer load and no extra capacitor is used. The size of the IF gm-cells was reduced to decrease their power until a NF of 20dB was achieved for the RX front-end to satisfy the sensitivity requirement with sufficient margin. The down-converted IF signals by the 3rd harmonic are added up in-phase after the gm-cells by the TIA which provides further amplification and filtering.

Fig. 3b shows the LO generation block in detail. Having $M = N = 3$, a current-controlled 9-stage pseudo-differential RO is designed that benefits from high oscillation amplitude, sharper edges, and has lower $1/f^3$ PN corner frequency compared to a 3-stage RO [6], while sacrificing only 1μW in power (see Table 1). The RO is tuned to operate at around 272MHz (2.45GHz/9), burning only 17μW. Considering each group of RO nodes that have the desired phase difference of 120°, a signal with 3x higher frequency can be obtained by the proposed EC as shown in the bottom right corner. As well as multiplying the frequency by 3, these ECs also provide perfectly symmetrical loading for all the stages of the RO. The 9-stage RO gives enough oscillation amplitude to have 2 PMOS and 2 NMOS transistors stacked and no level-shifting is needed for the LO buffers. A 9-stage RO with $M = 1$ (no EC) and $N = 3$ is used by [5]. It consumes more power than the proposed design as it runs at $f_{RF}/3$ instead of $f_{RF}/9$ and suffers from non-symmetrical loading. Our addition of the ECs with $M = 3$ improves the symmetry of the circuit by loading all RO cells equally and reduces the power by 40% independent of technology scaling (see Table 1).

III. Measurement Results

The proposed receiver is fabricated in GlobalFoundries' 22nm FDSOI technology (22FDX^{TM}) and is wire-bonded in a QFN package. Chip area is 0.14/0.002mm^2 with/without the MN. The MN is there for the higher-end RX and the proposed front-end adds negligible area. Measurements can be seen in Fig. 4 and die photograph and RX power break-down is shown in Fig. 5. The total power consumption of the RX is measured to be 50μW with a V_{DD} of 0.63V. S_{11}<-10dB is achieved from 2.26GHz to 2.52GHz, making the RX suitable for the ISM band. The front-end is tuned by injection locking the RO with an external signal through the control current input (see Fig. 3a). Overall gain is 41dB with a -3dB bandwidth of 1MHz, in-band IIP3 is -20dBm, and NF is measured to be 20dB, corresponding to a calculated sensitivity of -84dBm for 1MHz BW GFSK in a complete system using the formula in Table 2 and prior-art [8]. LO leakage to the antenna is <-80dBm thanks to the small mixer switch size. A duplicate RO with custom output buffer was placed on the chip for PN measurement. The measured PN at 1MHz offset of 272MHz is -84dBc/Hz while free-running and -100dBc/Hz when injection-locked. Degraded by 20log(9)dB when translated to 2.45GHz, PN is -65dBc/Hz free-running and -81dBc/Hz locked (the noise bump around 30-100kHz is from our reference current source). As a result, the lowest published power of 50μW is achieved for the proposed 2.45GHz mixer-first RX while free-running, making it a suitable option for e.g. a WuRX that does not necessarily need to demodulate data. By having a PLL with the power consumption of $0.6P_{VCO}$ as in [2], power will increase to 68μW, which would still be the lowest reported for the given sensitivity and BER of 10^{-3} for GFSK demodulation.

Fig. 4 (bottom right) and Table 2 show the comparison with prior-art 2.4GHz RXs. The proposed RX has 2x lower power consumption than others while having competitive (calculated) sensitivity. Also, its small active area without the

Table 2. Comparison with 2.4GHz state-of-the-art RXs.

	[1] JSSC2018	[2] JSSC2022	[8] ISSCC2022	[9] CICC2018	[10] JSSC2019	[11] ISSCC2019	[12] JSSC2021	[13] JSSC2016	**This work**
CMOS Tech.	14nm FinFET	65nm	28nm	65nm	65nm	65nm	65nm	65nm	**22nm FDSOI**
Architecture	Mixer first Low IF	Low IF+ CE-OOK	Low IF	Low IF +correlator	Mixer first Low IF	Low IF+ Energy detection	Zero-IF	Uncertain IF	**Mixer-first Low IF**
LO generation	RO+FLL	Free running LC	Off-chip LO	Free running LC	RO+FLL	RO+PLL	RO+Freq. Tripler+ PLL	LC-DCO	**Free running RO**
Image rejection	No	No	Yes	No	Yes	Yes	Yes	No	**No**
NF (dB)	NA	12 $\star$	6.1	24 $\diamond$	9 $\star$	22.6 $\star$	16 $\star$	27	**20**
Sensitivity Modulation BW	-72 dBm OOK 3MHz	-91.5 dBm CE-OOK 2MHz	-98 dBm $\bullet$ GFSK 1MHz	-80 dBm GFSK 1MHz	-57.5 dBm FSK 2MHz	-85 dBm GFSK NA	-92 dBm GFSK NA	-97 dBm OOK NA	**-84 dBm $\bullet$ GFSK 1MHz**
V_{DD} (V)	0.95	0.6/1	0.6/1	0.75	0.9/1.1	0.5	0.5	0.5	**0.63**
Total Power Excluding	95 μW DSP,XTAL	539 μW PLL	266 μW LO,ADC, DSP	230 μW XTAL	150 μW ADC,DSP XTAL	220 μW XTAL	352 μW XTAL	99 μW Calib. circuit	**50 μW PLL,ADC, DSP**
Power burnt in LO (μW)	55	363	191 Div.+Buffs.	N/A	120	166	211	66.5	**28.5**
External components	None	None	None	None	None	FBAR filter	None	SMD inductor	**None**
Chip area (mm^2)	w/o pads 0.19	w/ pads 2.24	w/o pads 0.5	w/ pads 4.0	w/ pads 1.1	w/ pads 2.4	w/o pads 0.6	w/o pads 0.05	**w/ pads 0.46 w/o pads 0.14 w/o MN 0.002**

$\bullet$ Calculated sensitivity (dBm)= -174+10log(BW)+NF+10 for GFSK [8] $\diamond$ Calculated NF based on reported sensitivity $\star$ Simulated value

MN ($0.002mm^2$) makes it a suitable option for any auxiliary RX, e.g. wake-up or clock harvesting, as well.

IV. Conclusions

A -84dBm sensitivity 2.45GHz mixer-first low-IF RX is presented that consumes 50μW including LO generation. The proposed front-end is fabricated in GF22nm FDSOI and has better sensitivity than prior energy-detecting RXs, as it benefits from down-conversion to IF, and yet burns 2x less power than any low-IF prior-art RX with better than -80dBm sensitivity in the 2.4GHz band (see Fig. 4, bottom right). The power consumption is minimized for the given process by optimum choice of the design parameters N and M, while this architecture can yield even lower power consumption for smaller geometry process nodes.

Acknowledgment

We thank G. Wienk for CAD assistance, A. Rop for measurement support, and GlobalFoundries for providing silicon fabrication through the 22FDX university program.

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