Design and realization of a miniature capacitive silicon force sensor for loads up to 500 kg

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Abstract

In this paper, a micromachined silicon load cell (force sensor) is presented for measuring loads up to 500 kg. The load cell has been realized and tested. Measurement results show a hysteresis error of ±0.02 % of full-scale. Creep at 500 kg after 30 minutes is within 0.01 %. These measurements show that the performance has improved by a factor of 10 compared to the previous design.

Introduction

Most conventional load cells for loads of 500 kg and more are made from steel. Hysteresis and creep limit the accuracy of these load cells which is in the order of magnitude of ±0.03 %. To minimize these effects, expensive high-grade steels and labor intensive fabrication methods are required. Silicon does not suffer from hysteresis or creep and, therefore, it is an ideal material for use in load cells.

This paper presents the latest results on a silicon capacitive force sensor of which the basics where presented before by the authors of this paper [1],[2]. New is that the influence of non-homogeneous loads on the linearity is investigated. In addition, the influence of parasitic capacitances and resistances in the leading wires on the frequency of the oscillator circuit is treated. Then, the use of a new metal layer (titanium-platinum) and its consequences for the production process is discussed. Finally, results of hysteresis and creep measurements are given which show the improved performance with respect to the old design.

Operation

The layout and package of the chip are shown in figure 1 and 2 respectively. The load is applied to the 1 cm^2 area. The bottom wafer contains an electrode pattern that forms an array of capacitors with the top wafer as a common electrode. On application of the load, the bearing poles will be compressed and the distance between between the metal electrodes and the top-wafer at the position of the capacitors is decreased thereby increasing the capacitance. In [1] it was derived that the sum of reciprocal values of all capacitances is independent of the total load F_{tot} :

$$Sum_1 = \sum_{i=1}^{n^2} \sum_{j=1}^{1} \sum_{k=1}^{1} \frac{1}{C_{i,j,k}} \approx n^2 \frac{d_0}{eA_{cap}} - \frac{l_{pole}}{EeA_{cap}A_{pole}} F_{tot} , \tag{1}$$

where $C_{i,j,k}$ are the sensor capacitors located at position (i,j,k) , n^2 is the total number of capacitors (in figure 1 n equals 6), e is the dielectric constant in air, A_{cap} the area of one capacitor, d_0 the plate distance, A_{pole} the area of a bearing pole, l_{pole} its length and E Young's modulus of silicon. However, in case n^2 becomes large it is no longer possible to determine the value of all n^2 capacitors. Therefore, the capacitors are clustered in m^2 groups (in figure 1 m equals 3), one group consisting of n^2 / m^2 parallel capacitors. Now (1) is changed to

$$Sum_2 = \sum_{i=1}^{m^2} \frac{1}{\sum_{j=1}^{n/m} \sum_{k=1}^{n/m} C_{i,j,k}} , \tag{2}$$

Only when, the load is uniformly distributed Sum_1 will be equal to Sum_2 . In the case of a non-uniform load distribution Sum_2 is a non-linear function of F_{tot} . Three different loading situations were considered as is shown in figure 3. The resulting change with respect to a uniform load distribution is shown in figure 4. It is concluded that for $m \geq 5$ the non-linearity is within 0.03 %.

Electronics

The values of the m^2 capacitor groups are one by one determined in a modified Martin oscillator circuit [3] where multiplexers are used to select a capacitor. The circuit is shown in figure 5. The circuit was analyzed analytically by using Laplace transformations. The analysis gives an indication of the influence of the parasitic capacitance from the common top electrode to bottom wafer, the parasitic capacitance from the metal electrodes to the bottom wafer and the resistances in the leading wires to the electrodes on the oscillation frequency. It follows that the influence of parasitic components on the oscillating frequency is less than $0.13 \cdot 10^{-6}$ %.

Processing

The sensor was realized in the MESA cleanroom with parameters $n = 40$ and $m = 5$, resulting in 25 groups of each 64 capacitors. In the previous designs [1],[2] aluminum was used for the electrodes which resulted in hillocks after wafer bonding. Therefore, in the new design a Ti/Pt-layer (40 nm/270 nm) was patterned by using a lift-off technique [4]. This layer was able to survive the pirana clean just before bonding and an annealing step of 600 ºC after bonding. The hillock height was drastically reduced thereby reducing the chance of short-circuits with the top wafer. The poles in the top wafer were etched by using Reactive Ion Etching (RIE). They have a height of 185 um. A picture of the chip is shown in figure 6.

Measurements

Hysteresis measurements were done up to 500 kg with a test setup. The result is shown in figure 7. As expected from the theory the output is non-linear function of the applied load. The hysteresis error is shown in figure 8. Clearly, this error is within ±0.02 %. Creep was tested at 500 kg during 30 minutes (see figure 9). The change in output after 30 minutes is within 0.01 %.

References

[1] R.J. Wiegerink, R.A.F. Zwijze, G.J.M. Krijnen, T.S.J. Lammerink and M.C. Elwenspoek, Silicon load cell for loads up to 1000 kg with insensitivity for inhomogeneous loads, *Sensors and Actuators*, 80(2000), 189-196.

[2] Remco Wiegerink, Robert Zwijze, Richard Mateman, Gijs Krijnen, Theo Lammerink, Miko Elwenspoek, "Quasi Monolithic Silicon Load Cell for Loads up to 1000 kg with Distributed Capacitive Sensing", *Proceedings of Eurosensors XIII*, The Hague, September 12-15, 1999, 545-546.

[3] F.N. Toth, and G.C.M. Meijer, A low-cost, smart capacitive position sensor, *IEEE Trans. Instrum. Meas.*, 41(1992), 1041-1044.

[4] D. Wijngaards, M. Bartek, R.F. Wolffenbuttel, Silicon IC compatible thin metal film post-processing module, *Sensors and Actuators*, A68(1998), 419-428.
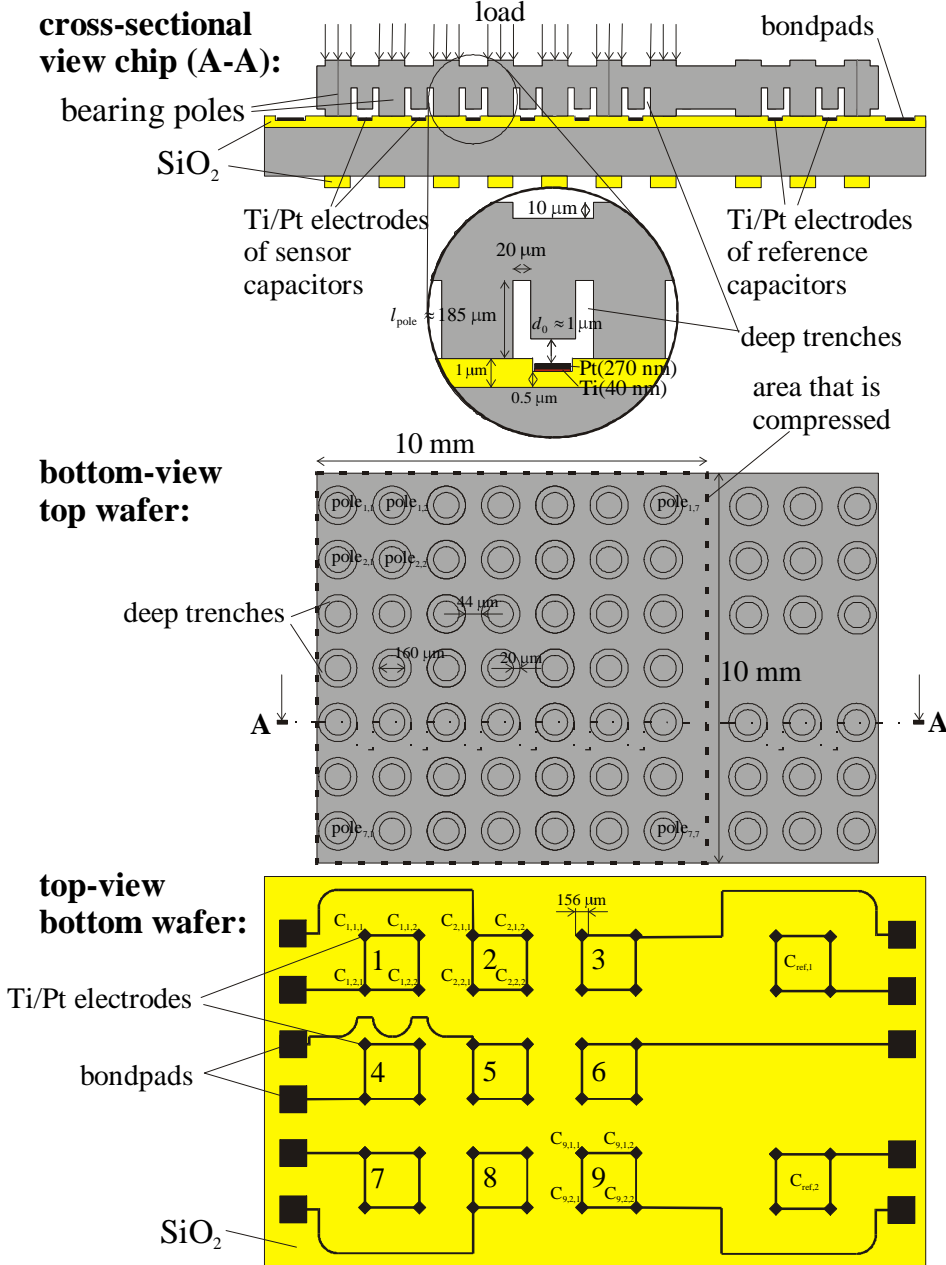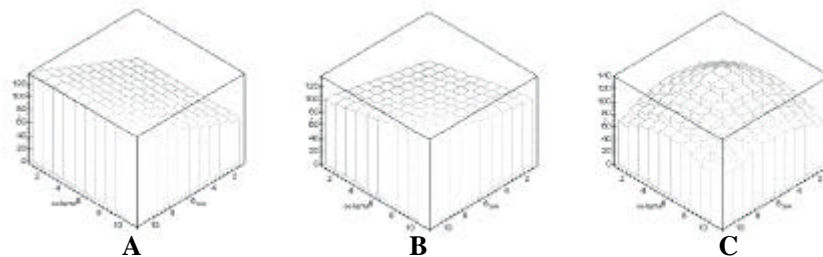
cross-sectional view chip (A-A):

load

bondpads

bearing poles

SiO_2

10 µm

20 µm

$l_{pole} \approx 185$ µm

$d_0 \approx 1$ µm

1 µm

0.5 µm

Pt(270 nm)
Ti(40 nm)

Ti/Pt electrodes of sensor capacitors

Ti/Pt electrodes of reference capacitors

deep trenches

area that is compressed

bottom-view top wafer:

10 mm

10 mm

deep trenches

$pole_{1,1}$ $pole_{1,2}$ $pole_{1,7}$

$pole_{2,1}$ $pole_{2,2}$

44 µm

160 µm 20 µm

$pole_{7,1}$ $pole_{7,7}$

A A

figure 2: Package.

membrane

force

springs

chip

chip holder

PCB

ceramic pressing block

top-view bottom wafer:

Ti/Pt electrodes

bondpads

SiO_2

156 µm

$C_{1,1,1}$ $C_{1,1,2}$ $C_{2,1,1}$ $C_{2,1,2}$

1 2 3 $C_{ref,1}$

$C_{1,2,1}$ $C_{1,2,2}$ $C_{2,2,1}$ $C_{2,2,2}$

4 5 6

$C_{9,1,1}$ $C_{9,1,2}$
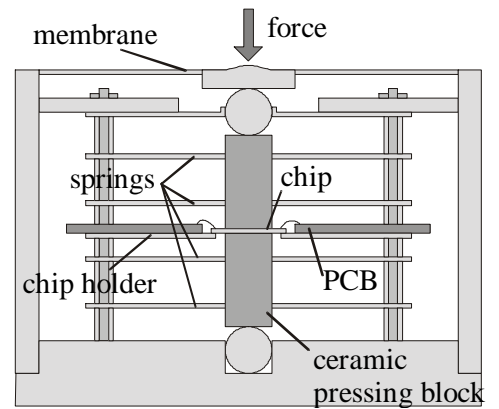
7 8 9 $C_{ref,2}$

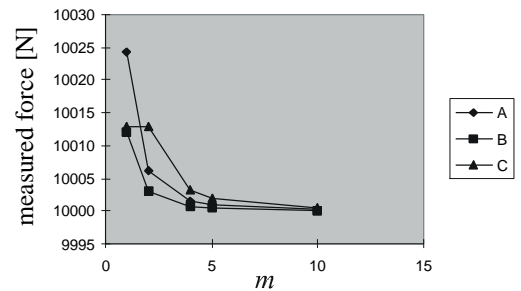$C_{9,2,1}$ $C_{9,2,2}$

figure 1: Layout chip.

figure 4: Measured force as a function of different load distributions and number of capacitor groups. The output is compared to the output that would be measured for a uniform load distribution.
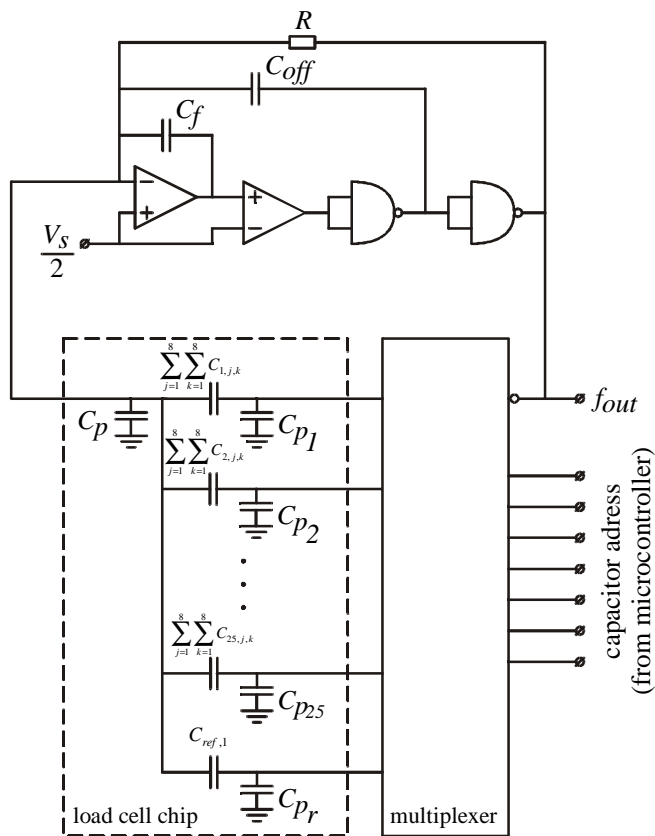
A B C

figure 3: Three examples of an inhomogeneous load distribution.

Figure 5: Modified Martin oscillator circuit used for measuring the 25 capacitor ratio's $\dfrac{C_{ref,1}}{\sum\limits_{j=1}^{8}\sum\limits_{k=1}^{8}C_{i,j,k}}$ (i =1..25).

C_p , C_{p_i} are parasitic capacitances and f_{out} the block signal containing the frequency of the circuit.
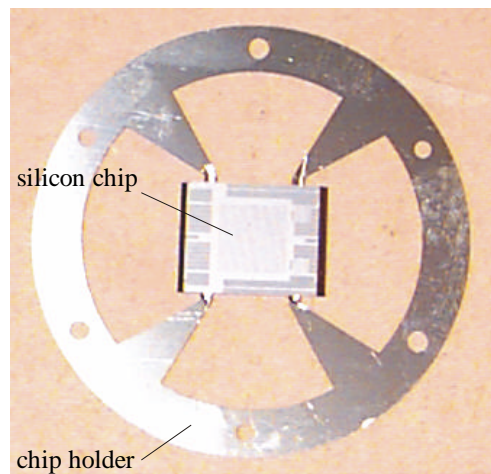

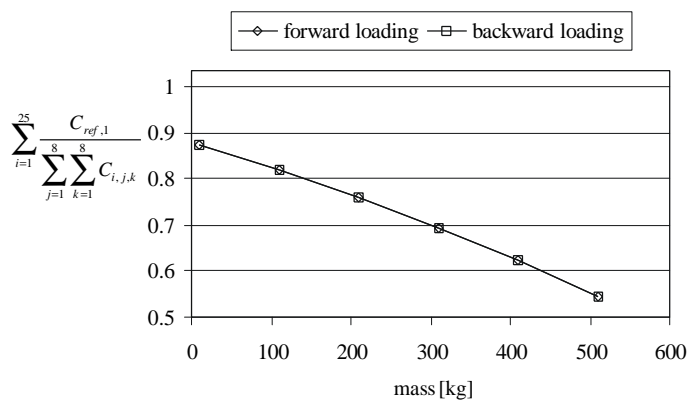figure 6: Picture of chip glued on the chip holder.

Figure 7: Measured output as a function of the applied mass. $C_{ref,1}$ is the value of the reference capacitor.
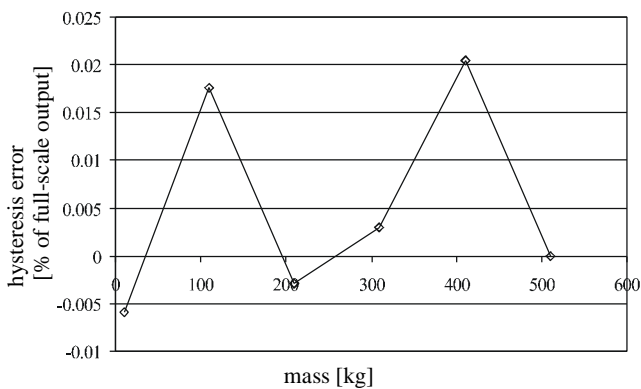

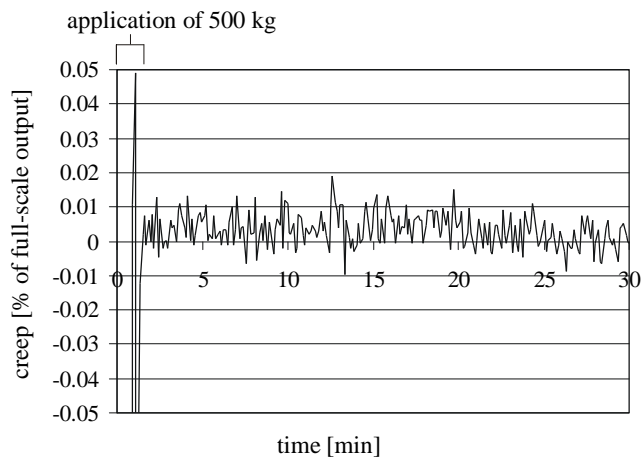Figure 8: Hysteresis error as a percentage of the full-scale change in output.

Figure 9: Creep at 500 kg as a percentage of the full-scale output.