Inverter Chain Buffer Optimization for N-path Filter Switch Drivers and Validation through Simulations in 22nm FD-SOI Technology

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***Abstract*—In this paper, the CMOS inverter chain buffer is optimized for N-path filter switch drivers in a technology-agnostic way. Figures-of-merit are proposed to minimize jitter for minimal power dissipation with consideration of rise/fall-time. Using these, mathematical models are derived based on a simple circuit model and expressed for optimization as a function of the technology-specific inverter output/input capacitance ratio, the number of inverters, and their taper factors. This enables finding designs with any set of taper factors that have lower jitter than common designs for the same power dissipation by sweeping many designs orders of magnitude faster than using circuit simulations. Additionally, analytical equations are derived to quickly allow a designer to find the optimal number and sizing of inverters for the constant and exponential taper designs, either of which is shown to be near-optimal depending on the set of specifications.**

***Index Terms*—N-path filter, inverter chain, buffer, switch driver optimization, jitter, rise-time, CMOS**

I. Introduction

The number of wireless communication technologies supported in one device is ever-increasing. To tackle the accompanying technical difficulties, flexible filters are required. N-path filters offer excellent programmability and scale well with advancing CMOS technology [1], [2]. The disadvantage of N-path filters is the high power dissipation for the clock-generation circuitry and the drivers of their relatively large switches [3]. The clock drivers in N-path filters are commonly designed with inverter chains to buffer the clock generator's high-impedant output to the switches' large capacitive input.

There is extensive literature available on CMOS inverter chain buffer optimization for digital applications tailored towards minimizing propagation delay [4]–[6], in many instances also combined with area and power optimization [7]–[13]. The propagation delay, however, is not a key concern for N-path filter switch drivers, because only relative phase differences between the clock paths matter. Optimization of inverter chain buffers for N-path filters is lacking in the literature; only phase variation caused by mismatch has been analyzed [14], [15]. The goal of this paper is, therefore, to optimize the CMOS inverter chain specifically for N-path filters.

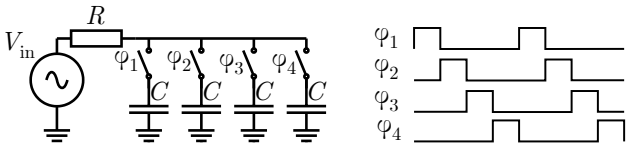

Fig. 1. Clock signals driving the switches in a 4-path filter.

To optimize the inverter chain, a basic inverter chain model will be created and the key N-path filter specifications and their trade-off with power dissipation will be expressed in figures-of-merit (FOMs) in Section II. In Section III, the FOMs will be expressed in mathematical models for optimization. For these, numerical simulations are set up in Section IV to find the optimal designs. The results are validated with circuit simulations in GlobalFoundries' 22nm FD-SOI technology in Section V. Conclusions are drawn in Section VI.

II. System Model

The most basic N-path filter with four paths and the clock signals that drive the switches is shown in Fig. 1. During one clock cycle, each switch is closed and opened once, such that always just one switch is conducting. After many clock cycles, only input signals close to the clock frequency remain on the capacitors: the N-path filter behaves like a band-pass filter [1].

A. Assumptions

In this paper, assumptions are made to reduce the design space and simplify the calculations. The impedance that is driven by the inverter chain buffer is assumed to be an NFET switch that is modeled as a load capacitance (C_{L}) to ground. One unit inverter with equal rise (t_{r}) and fall-time (t_{f}) is assumed to be available that is scaled to the required width depending on the position in the buffer chain. Equal t_{r} and t_{f} is used to minimize the off-time for preventing clock overlap, because it reduces N-path filter attenuation [16], [17] and its duration is determined by the slowest edge. The t_{r} is defined here from 20% to 80% of the supply voltage V_{DD} and t_{f} vice-versa based on the assumption that the input of the N-path

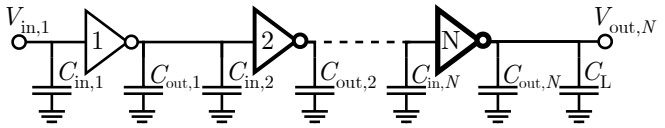

Fig. 2. Generalized inverter chain model with explicit parasitic capacitances.

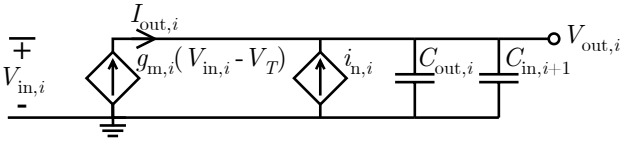

Fig. 3. Circuit model of the i^{th} inverter in a chain.

filter switch is well below its threshold voltage (V_{T}) at 20% of V_{DD} and well above V_{T} at 80% of V_{DD}. It is assumed that leakage power dissipation (P_{leak}) can be neglected, as N-path filters operate at relatively high frequencies.

B. Specifications

Local oscillator jitter (J_{LO}) is a key metric, as it degrades the N-path filter's performance [18], [19]. Two significant contributors to J_{LO} are stochastic jitter (J_{stoch}), due to noisy transistors, and deterministic jitter (J_{det}), due to mismatch between chains. The inverter chain can be scaled together with the clock generator to trade power dissipation (P) for J_{LO}, as both J_{stoch} [20] and J_{det} [21] are inversely proportional to P, which is also a key metric for N-path filters. Hence, a FOM can be defined as the product of P and J_{LO} [15], which for J_{stoch} and J_{det} then are

$$\text{FOM}_{\text{PJ}_\text{s}} \triangleq P \cdot J_{\text{stoch}} \tag{1}$$

$$\text{FOM}_{\text{PJ}_\text{d}} \triangleq P \cdot J_{\text{det}} \tag{2}$$

The chain output rise-time ($t_{\text{r},N}$) should be low enough to negligibly impact the N-path filter's noise performance [22]. By scaling, t_{r} is decreased at the cost of P, which is roughly inversely proportional when operating well below the transit frequency. Hence, $t_{\text{r},N}$ should also be considered when optimizing for minimum jitter.

C. Inverter Chain Model

A basic inverter chain model with N inverters is shown in Fig. 2. The i^{th} inverter is the $(i-1)^{\text{th}}$ inverter scaled by the i^{th} taper factor (ρ_i). Each inverter has an input ($C_{\text{in},i}$) and output capacitance ($C_{\text{out},i}$), which is equal to the average equivalent input and output capacitance, respectively, during a clock edge. The ratio between C_{out} and C_{in} is technology-dependent and denoted here by λ, commonly assumed to be approximately 1 in bulk CMOS [12], [13], [15], but is expected to be lower in SOI technology where source-bulk and drain-bulk parasitics are reduced. To keep the model generalized, the first inverter can either model the clock output impedance in the optimization or the first inverter can be sized such that $C_{\text{in},1}$ is equal to a specified clock load capacitance. The product of the taper factors up to and including the i^{th} inverter and the product of all the taper factors are defined as

$$\Gamma_i \triangleq \prod_{j=1}^{i} \rho_j \quad \text{and} \quad \Gamma_N \triangleq \frac{C_{\text{L}}}{C_{\text{in},1}} = \prod_{i=1}^{N} \rho_i \tag{3}$$

The inverter chain buffer was originally proposed with a uniform taper that is calculated by [4], [23]

$$\rho_i = \sqrt[N]{\Gamma_N} \quad \forall i \tag{4}$$

A more accurate constant taper model includes C_{out} [5]. However, any set of taper factors is possible and could outperform a constant taper design on some specifications. Examples include a uniform taper chain with a different taper factor in the last inverter [8], a non-uniform taper chain optimized for minimum power-delay product [11], a variable taper chain that depends on a unified design metric [13], and an exponential taper chain that is calculated by [10]

$$\rho_i = \Gamma_N^{\frac{2i}{N(N+1)}} \tag{5}$$

D. Inverter Model

As shown in Fig. 3, the i^{th} inverter of a chain is modeled as a voltage-dependent current source with additional noise current $i_{\text{n},i}$ that drives its load (inverter $i+1$ or the N-path filter switch) by charging $C_{\text{out},i}$ and $C_{\text{in},i+1}$. It assumes no output current ($I_{\text{out},i}$) if the input voltage ($V_{\text{in},i}$) is below V_{T}, which is assumed to be equal for the rising and falling edge for simplicity. The thermal noise is assumed to be dominant over $1/f$ noise because in clock buffers there is no jitter accumulation from feedback [24], [25]. The current thermal noise spectral density is $4k_{\text{B}}T\gamma g_{\text{m},i}$ [26], where k_{B} is the Boltzmann constant, T is the temperature, and γ is a noise coefficient that is typically between 2/3 and 3/2 [27]. In the next section, the FOMs are derived using the models from this section.

III. Deriving Figures-of-Merit

A. Dynamic Power Dissipation

As P_{leak} is ignored here, the dynamic (P_{d}) and short-circuit (P_{sc}) dissipation are left. A mathematical model for P that generates a technology-independent optimization scheme requires a separable product of a function of only inverter chain parameters and a function of technology-dependent constants for P_{d} and P_{sc}. This is not possible, however, because unlike P_{d}, P_{sc} is dependent on t_{r}. The relation between P_{sc} and t_{r} is approximately proportional [7]. As $t_{\text{r},N}$ needs to be small enough and both P_{d} and P_{sc} are proportional to transistor width, only P_{d} is considered here, similarly to [15]. By approximation, $P_{\text{d}} = f_{\text{c}}V_{\text{DD}}^2 C$ [28], where C is the capacitance that is switched each clock cycle and f_{c} is the clock frequency. The capacitance driven by the i^{th} inverter is $\Gamma_{i-1}C_{\text{in},1}(\rho_i+\lambda)$, which results in

$$P_{\text{d}} = f_{\text{c}}V_{\text{DD}}^2 C_{\text{in},1} \sum_{i=1}^{N} \Gamma_{i-1}(\rho_i + \lambda) \tag{6}$$

B. Stochastic Jitter

To find an expression for J_{stoch} using the circuit model in Fig. 3, it is taken that $I_{\text{out},i}$ is constant and approximately equal to $g_{\text{m},i}\,(V_{\text{DD}} - V_{\text{T}})$, where $g_{\text{m},i}$ is the average equivalent transconductance during a transition. The delay of the i^{th} inverter ($t_{\text{d},i}$) is then implicitly defined by the time $I_{\text{out},i} + i_{\text{n},i}$ requires to charge $C_{\text{out},i}$ and $C_{\text{in},i+1}$ to $V_{\text{DD}}/2$. Following [29], the variance of $t_{\text{d},i}$ is

$$\sigma^2_{t_{\text{d},i}} = \frac{1}{I^2_{\text{out},i}} \left\langle \left(\int_0^{t_{\text{d},i}} i_{\text{n},i} \text{d}t \right)^2 \right\rangle = \frac{k_{\text{B}} T \gamma V_{\text{DD}} g_{\text{m},i} (C_{\text{out},i} + C_{\text{in},i+1})}{I^3_{\text{out},i}} \quad (7)$$

where $\langle \cdot \rangle$ denotes the expected value. Due to noise independence, the sum of the jitter generated by each individual inverter is equal to the total J_{stoch}. As $C_{\text{out},i} + C_{\text{in},i+1} = C_{\text{in},i}(\rho_i + \lambda)$ and $g_{\text{m},i}$, $C_{\text{in},i}$, and $I_{\text{out},i}$ are Γ_{i-1} times larger than $g_{\text{m},1}$, $C_{\text{in},1}$, and $I_{\text{out},1}$, J_{stoch} can be calculated with

$$J_{\text{stoch}} = \frac{k_{\text{B}} T \gamma V_{\text{DD}} g_{\text{m},1} C_{\text{in},1}}{I^3_{\text{out},1}} \cdot \sum_{i=1}^{N} \frac{\rho_i + \lambda}{\Gamma_{i-1}} \quad (8)$$

Combining (6) and (8) shows that $\text{FOM}_{\text{PJ}_\text{s}}$ is proportional to

$$\text{FOM}_{\text{PJ}_\text{s}} \propto \left(\sum_{i=1}^{N} \Gamma_{i-1}(\rho_i + \lambda) \right) \cdot \left(\sum_{i=1}^{N} \frac{\rho_i + \lambda}{\Gamma_{i-1}} \right) \quad (9)$$

C. Deterministic Jitter

Expressed as a function of constant taper factor ρ, N, and λ, J_{det} is proportional to $\sigma^2_{t_{\text{det\_int},1}}$, the intrinsic deterministic jitter of the first inverter when it is unloaded [15]. Due to its independence from ρ_i, N, and λ, it can be considered a constant in the optimization. Rewriting with this paper's definitions, J_{det} for any set of taper factors is

$$J_{\text{det}} = \sigma^2_{t_{\text{det\_int},1}} \cdot \sum_{i=1}^{N} \frac{\left(1 + \frac{\rho_i}{\lambda}\right)^2}{\Gamma_{i-1}} \quad (10)$$

Combining (6) and (10) shows that $\text{FOM}_{\text{PJ}_\text{d}}$ is proportional to

$$\text{FOM}_{\text{PJ}_\text{d}} \propto \left(\sum_{i=1}^{N} \Gamma_{i-1}(\rho_i + \lambda) \right) \cdot \left(\sum_{i=1}^{N} \frac{\left(1 + \frac{\rho_i}{\lambda}\right)^2}{\Gamma_{i-1}} \right) \quad (11)$$

D. Rise-time

Fig. 3 is used as circuit model for t_{r}, where $V_{\text{in},i}$ is the previous output voltage ($V_{\text{out},i-1}$). As long as $V_{\text{out},i-1} < V_{\text{T}}$, $I_{\text{out},i} = 0$ A. When $V_{\text{out},i-1} > V_{\text{T}}$, $I_{\text{out},i} = g_{\text{m},i}(V_{\text{out},i-1} - V_{\text{T}})$ until it is turned off again when $V_{\text{out},i} = V_{\text{DD}}$. The model is simplified by considering every edge a rising edge as $t_{\text{r}} = t_{\text{f}}$ and by assuming the intrinsic t_{r} of an unloaded inverter ($t_{\text{r\_int}}$) is independent of its size. The resulting model is

$$V_{\text{out},i}(t) = \min\left(V_{\text{DD}}, \max\left(0, \frac{0.8 V_{\text{DD}}}{t_{\text{r\_int}}(V_{\text{DD}} - V_{\text{T}})} \cdot \frac{\lambda}{\rho_i + \lambda} \cdot \int_0^t (V_{\text{out},i-1}(t) - V_{\text{T}}) \text{d}t \right) \right) \quad (12)$$

By iterating this from the first to the last inverter, $V_{\text{out},N}$ is found numerically. To obtain $t_{\text{r},N}$, the time between the points that $V_{\text{out},N}$ is at 20% and 80% of V_{DD} is calculated. The input signal of the inverter chain is modeled as a finite ramp function ($\min(V_{\text{DD}}, \frac{0.6 V_{\text{DD}}}{t_{\text{r,in}}} t)$) with some reasonable rise-time ($t_{\text{r,in}}$). No analytical expression can be found for $t_{\text{r},N}$ because (12) can only be solved numerically.

IV. Analytical and Numerical Optima

The constant taper factor, as defined in (4), optimized for $\text{FOM}_{\text{PJ}_\text{s}}$ ($\rho_{\text{c,s}}$) and $\text{FOM}_{\text{PJ}_\text{d}}$ ($\rho_{\text{c,d}}$) can be derived analytically by equating the FOM's derivative with respect to $\rho_{\text{c,s}}$ or $\rho_{\text{c,d}}$ to 0 and then solving for $\rho_{\text{c,s}}$ or $\rho_{\text{c,d}}$ to find

$$\rho_{\text{c,s}} = 1.5 + 0.5\lambda + \sqrt{0.25(\lambda + 5)^2 - 4} \quad (13)$$

$$\rho_{\text{c,d}} = 1 + 0.25\lambda + \sqrt{(0.25\lambda + 2)^2 - 3} \quad (14)$$

As $\lambda > 0$, there is no physically possible λ that results in $\rho_{\text{c,s}} = \rho_{\text{c,d}}$, indicating a trade-off between J_{stoch} and J_{det}. The variables should be equal in the mathematical models and the circuit simulations for the validation. Hence, $C_{\text{in},i}$ and $C_{\text{out},i}$ can be found by curve-fitting a rising edge. For a 22nm FD-SOI circuit simulation, this gives $\lambda \approx 0.5$, which results in $\rho_{\text{c,s}} \approx 3.6$ and $\rho_{\text{c,d}} \approx 2.4$. As N can only be an integer, it was verified numerically that rounding $\ln(\Gamma_N)/\ln(\rho_{\text{c,s/d}})$ to the nearest integer gives the N that results in a minimum for (9) and (11). For example, optimizing for $\text{FOM}_{\text{PJ}_\text{s}}$ with $\Gamma_N = 100$ gives $N = 4$ and $\rho_i = 3.16$.

Matlab scripts are written that calculate the FOMs and search for optimal designs by randomly generating 1,000,000 sets of taper factors for all $N \leq N_c + 3$, where N_c is the calculated optimal N for the constant taper design, with each factor uniformly distributed between 0 and 1 and normalizing each set such that its product is equal to Γ_N. The design that has the lowest simulated FOM is extracted as the optimum. Optimization algorithms could be used for even lower computation time. Both in the numerical and the circuit simulations, $t_{\text{r,in}}$ is set to 5 ps and V_{DD} to 0.8 V. With a circuit simulation it was found that $t_{\text{r\_int}} \approx 2$ ps and $V_{\text{T}} \approx 0.2\ V$.

V. Simulation Results

The designs found in the previous section are simulated in 22nm FD-SOI on schematic level with the tt_pre simulation setting that includes the most relevant layout parasitics including lower metals. Super-low V_{T} FETs are used with minimum channel length (20 nm) and 80 nm and 96 nm gate finger width for NFET and PFET, respectively, to achieve equal t_{r} and t_{f}. The first inverter has 26 gate fingers ($C_{\text{in},1} \approx 10$ fF) to minimize quantization effects. To get Γ_N equal to 100, which is reasonable for N-path filters, C_{L} is set to 1 pF. The

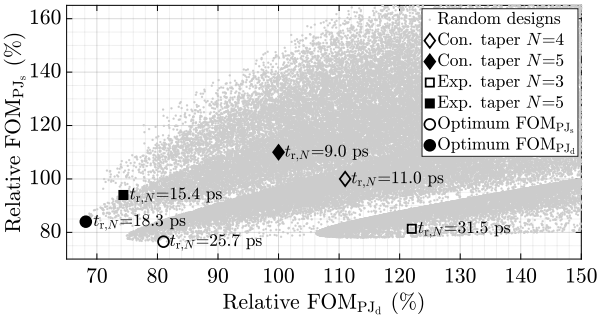

Fig. 4. Numerical simulations of the $\mathrm{FOM_{PJ_s}}$ and $\mathrm{FOM_{PJ_d}}$ design space including the randomly generated designs with $\Gamma = 100$, showing that the simple exponential tapers are near-optimal for these individual metrics. The axes are relative to the constant taper designs. A lower FOM is better.

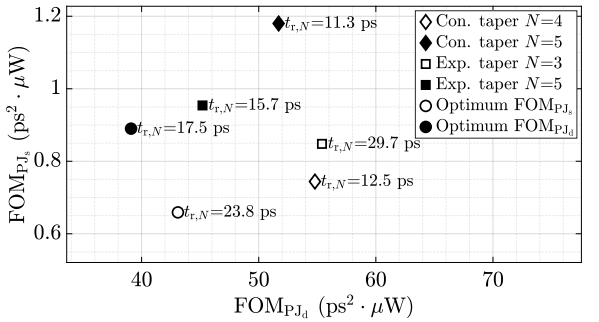

Fig. 5. Circuit simulations with $\Gamma = 100$ in 22nm FD-SOI that verify the numerical simulation results.

i^{th} inverter is sized by setting the number of gate fingers to $\lfloor 26 \cdot \Gamma_{i-1} \rceil$. The input signal is a 25% duty cycle 2 GHz pulse wave. Using a periodic steady state noise simulation with SpectreRF, J_{stoch} is found directly, while J_{det} is found from the variance in propagation delay in 500 Monte Carlo simulations for local mismatch.

The results of the numerical simulations with $\Gamma_N = 100$ using the mathematical models are shown in Fig. 4 for the exponential taper, as defined in (5), and the best designs from the random generations in Matlab relative to the constant taper designs, as defined in (4). The optimum set of taper factors for $\mathrm{FOM_{PJ_s}}$ is $\{2.14, 2.10, 2.76, 8.05\}$ and for $\mathrm{FOM_{PJ_d}}$ $\{1.80, 1.85, 2.00, 2.68, 5.59\}$. To show the effect of optimization for one FOM on the other, $\mathrm{FOM_{PJ_s}}$ is plotted on the y-axis, $\mathrm{FOM_{PJ_d}}$ on the x-axis, and the predicted $t_{\mathrm{r},N}$ in 22nm FD-SOI is annotated. The results of the 22nm FD-SOI circuit simulations of these designs are shown in Fig. 5. The prediction of $t_{\mathrm{r},N}$ is reasonably accurate, but some errors are caused by the simplification that $t_{\mathrm{r\_int}}$ is independent of the inverter size, which neglects the metalization effects in the 22nm FD-SOI models. However, the mathematical models can predict which designs have a certain relative improvement, as is verified in Fig. 5. The exponential taper designs shown here have a lower $\mathrm{FOM_{PJ_s}}$ and $\mathrm{FOM_{PJ_d}}$ than the constant taper designs not because they produce less jitter, but because they dissipate significantly less power due to their smaller size.

The circuit simulations, as shown in Fig. 5, indicate that the exponential taper design is near-optimal for $\mathrm{FOM_{PJ_d}}$. It has 4.4 ps more t_{r} than the constant taper design that is optimized for $\mathrm{FOM_{PJ_d}}$, but has a better $\mathrm{FOM_{PJ_s}}$ as well as a better $\mathrm{FOM_{PJ_d}}$. For the 125 ps pulse width in these simulations, 4.4 ps is rather insignificant, which makes the exponential taper preferable. However, at frequencies where the increase in t_{r} is significant, the constant taper is preferable.

It was assumed that P_{sc} is a negligible part of P. However, because input and output transition times are typically approximately equal, P_{sc} can be similar to P_{d}, as was verified with circuit simulations. Including P_{sc} will increase the accuracy of the mathematical models and, hence, likely reduce the deviations between the numerical and circuit simulations in Fig. 4 and Fig. 5.

The numerical simulations found designs that improve $\mathrm{FOM_{PJ_s}}$ and $\mathrm{FOM_{PJ_d}}$ relative to the constant and exponential designs, as is verified in Fig. 5 for the individual designs that achieved either the best $\mathrm{FOM_{PJ_s}}$ or $\mathrm{FOM_{PJ_d}}$. Furthermore, the circuit simulations show that the optimized N for the constant taper design (which is 4 for $\mathrm{FOM_{PJ_s}}$ and 5 for $\mathrm{FOM_{PJ_d}}$, as shown in Fig. 4) is also optimal for the exponential taper design (with only one exception, not shown in Fig. 5, that occurred in the simulations that degraded the FOM by a mere 3%). Hence, (13) and (14) provide a quick method to find the optimal constant and exponential taper designs analytically, as is verified with 22nm FD-SOI simulations.

VI. Conclusions

In this paper, a CMOS inverter chain is optimized for N-path filters in a technology-agnostic way. The inverters are modeled as voltage-dependent current sources with input and output capacitance. The most critical parameters for N-path filters, stochastic and deterministic jitter, rise and fall-time, and power dissipation are expressed as a function of the technology-specific inverter output/input capacitance ratio, the number of inverters, and their taper factors. Using FOMs that relate stochastic and deterministic jitter to power dissipation, the optimal designs are found empirically, which are then simulated in GlobalFoundries' 22nm FD-SOI technology. The simple models enable one to quickly find solutions with less jitter than existing solutions for the same power dissipation using numerical simulations. Still, it is shown that the exponential taper design is near-optimal due to its power efficiency, as long as the resulting rise and fall-times are well below the local oscillator's period. The constant taper design is better at (much) higher frequencies, as its rise and fall-times are lower. For both, a simple equation is presented that calculates the optimum number of inverters in the chain (and thereby also their sizing), such that very little time is required for a near-optimal buffer design.

References

[1] E. A. M. Klumperink, H. J. Westerveld, and B. Nauta, "N-path filters and mixer-first receivers: A review," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2017, pp. 1–8.

[2] P. Song and H. Hashemi, "RF filter synthesis based on passively coupled N-path resonators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2475–2486, 2019.

[3] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera, and B. Nauta, "A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1139–1150, 2019.

[4] R. C. Jaeger, "Comments on "An optimized output stage for MOS integrated circuits" [with reply]," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 3, pp. 185–186, 1975.

[5] N. C. Li, G. L. Haviland, and A. A. Tuszynski, "CMOS tapered buffer," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 1005–1008, 1990.

[6] C. Prunty and L. Gal, "Optimum tapered buffer," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 1, pp. 118–119, 1992.

[7] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, 1984.

[8] N. Hedenstierna and K. O. Jeppson, "CMOS circuit speed and buffer optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 6, no. 2, pp. 270–281, 1987.

[9] A. J. Al-Khalili, Y. Zhu, and D. Al-Khalili, "A module generator for optimized CMOS buffers," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 9, no. 10, pp. 1028–1046, 1990.

[10] S. R. Vemuru and A. R. Thorbjornsen, "Variable-taper CMOS buffers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 9, pp. 1265–1269, 1991.

[11] J.-S. Choi and K. Lee, "Design of CMOS tapered buffer for minimum power-delay product," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 9, pp. 1142–1145, 1994.

[12] B. S. Cherkauer and E. G. Friedman, "A unified design methodology for CMOS tapered buffers," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 3, no. 1, pp. 99–111, 1995.

[13] S. Liu, S. O. Memik, and Y. I. Ismail, "A comprehensive tapered buffer optimization algorithm for unified design metrics," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, 2011, pp. 2277–2280.

[14] A. J. Aragao, J. Navarro, and W. A. M. Van Noije, "Mismatch effect analyses in CMOS tapered buffers," in *2006 IEEE International Symposium on Circuits and Systems*. IEEE, 2006, pp. 4–pp.

[15] R. Dutta, T. K. Bhattacharyya, X. Gao, and E. A. M. Klumperink, "Optimized stage ratio of tapered CMOS inverters for minimum power and mismatch jitter product," in *2010 23rd International Conference on VLSI Design*. IEEE, 2010, pp. 152–157.

[16] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, 2011.

[17] S. Hameed, M. Rachid, B. Daneshrad, and S. Pamarti, "Frequency-domain analysis of N-path filters using conversion matrices," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 1, pp. 74–78, 2015.

[18] T. Tapen, Z. Boynton, H. Yüksel, A. Apsel, and A. Molnar, "The impact of LO phase noise in N-path filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 5, pp. 1481–1494, 2017.

[19] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 5, pp. 879–892, 2010.

[20] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 117–121, 2009.

[21] X. Gao, E. A. M. Klumperink, and B. Nauta, "Advantages of shift registers over DLLs for flexible low jitter multiphase clock generation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 3, pp. 244–248, 2008.

[22] A. Nikoofard, S. Kananian, A. Khorami, and A. Fotowat-Ahmady, "Analysis of the effects of clock imperfections in N-path filters," in *2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)*. IEEE, 2015, pp. 1–4.

[23] H. C. Lin and L. W. Linholm, "An optimized output stage for MOS integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 2, pp. 106–109, 1975.

[24] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-state circuits*, vol. 34, no. 6, pp. 790–804, 1999.

[25] C. Liu and J. A. McNeill, "Jitter in oscillators with 1/f noise sources," in *2004 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 1. IEEE, 2004, pp. I–773.

[26] B. Razavi, *Design of analog CMOS integrated circuits, second edition*. McGraw-Hill Education, 2017.

[27] A. J. Scholten, L. F. Tiemeijer, R. Van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 618–632, 2003.

[28] D. Liu and C. Svensson, "Power consumption estimation in CMOS VLSI chips," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 6, pp. 663–670, 1994.

[29] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, 2006.