CHALMERS
UNIVERSITY OF TECHNOLOGY

Multilayer integration in silicon nitride: decoupling linear and nonlinear functionalities for ultralow loss photonic integrated systems

Research Article | Vol. 31, No. 19 / 11 Sep 2023 / Optics Express 31435

Optics EXPRESS

Multilayer integration in silicon nitride: decoupling linear and nonlinear functionalities for ultralow loss photonic integrated systems

MARCELLO GIRARDI,* ÒSKAR B. HELGASON, ALEXANDER CAUT, MAGNUS KARLSSON, ANDERS LARSSON, AND VICTOR TORRES-COMPANY

Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Göteborg, Sweden
girardi@chalmers.se

Abstract: Silicon nitride is an excellent material platform for its extremely low loss in a large wavelength range, which makes it ideal for the linear processing of optical signals on a chip. Moreover, the Kerr nonlinearity and the lack of two-photon absorption in the near infrared enable efficient nonlinear optics, e.g., frequency comb generation. However, linear and nonlinear operations require distinct engineering of the waveguide core geometry, resulting in a tradeoff between optical loss and single-mode behavior, which hinders the development of high-performance, ultralow-loss linear processing blocks on a single layer. Here, we demonstrate a dual-layer photonic integration approach with two silicon-nitride platforms exhibiting ultralow optical losses, i.e., a few dB/m, and individually optimized to perform either nonlinear or linear processing tasks. We demonstrate the functionality of this approach by integrating a power-efficient microcomb with an arrayed waveguide grating demultiplexer to filter a few frequency comb lines in the same monolithically integrated chip. This approach can significantly improve the integration of linear and nonlinear optical elements on a chip and opens the way to the development of fully integrated processing of Kerr nonlinear sources.

1. Introduction

Photonic integrated circuits (PICs) are devices that manipulate light by confining it in a core material with a high refractive index, surrounded by a cladding material, typically silicon oxide (SiO_2), which displays a lower refractive index [1]. These devices are usually fabricated on a wafer in a planar process, where only one core material with a defined thickness is included. The core material and geometry play a key role in determining what functionalities can be integrated into a single PIC. The silicon-on-insulator (SOI) platform has been extremely successful in PIC development because most basic optical operations can be implemented in this material, such as low-loss routing [2], modulation [1] and detection [3], and the manufacturing cost is low thanks to the direct compatibility with the CMOS processes. However, dedicated platforms generally outperform Si in specific operations, such as ultralow-loss routing [4] and near-infrared nonlinear optics in silicon nitride [5–7], detection in germanium [8], electro-optic modulation in lithium niobate [9], and light generation in, e.g., indium phosphide [10]. Therefore, when designing a PIC, the specific trade-offs of the platform of choice have to be considered. To overcome this limitation, numerous efforts have been made to integrate multiple materials and platforms on the same PIC. By combining multiple platforms, the PIC can achieve denser routing [11], better fiber-to-chip coupling [12], integration of light sources [13,14], or more efficient modulation [15].

#492977 https://doi.org/10.1364/OE.492977
Journal © 2023 Received 16 Apr 2023; revised 25 Jul 2023; accepted 29 Aug 2023; published 8 Sep 2023

Optics EXPRESS

Among the different material platforms, silicon nitride (Si_3N_4) stands out for ultralow-loss PICs thanks to the broad transparency window, from visible to mid-infrared [16,17], and the compatibility with CMOS processes, which guarantees reliability and scalability. Moreover, Si_3N_4 displays high Kerr nonlinearities and lacks two-photon absorption in the near-infrared, which makes it an excellent platform for nonlinear optics, e.g., microcomb generation [5,18–22], noiseless parametric amplification [23] and supercontinuum generation [24–28].

Ultralow-loss (few dB/m) Si_3N_4, has been demonstrated in single-mode waveguide geometries [4,29] and in dispersion-engineered, strong-confinement strip waveguides [23,30]. The latter structure, however, typically results in waveguides that support more than one spatial mode (see further detailed analysis in the following section). Single-mode operation is necessary to realize optical signal processing [31], where dispersion-engineering is not paramount. In a planar integrated platform, with a thickness chosen to satisfy dispersion-engineering requirements, the single-mode-condition can only be attained by sufficiently decreasing the width of the waveguide, resulting in increased interaction with the sidewalls and enhanced scattering losses due to roughness [32,33]. This indicates a fundamental tradeoff between optical confinement, scattering loss, and single-mode operation in silicon nitride as we analyzed in [34]. This tradeoff affects the performance of practical systems that rely on or can benefit from the co-integration of linear and nonlinear processing blocks [35–38]. Here, we overcome this problem by integrating two distinct layers, individually optimized to perform either linear processing (single-mode waveguide geometry) or nonlinear Kerr applications (dispersion-engineered silicon nitride). Adiabatic interposers are designed to interface these two layers. We demonstrate a bi-layer integration architecture (Fig. 1(a)) operating in the ultralow loss regime. As a proof of concept, we designed a comb demultiplexer, shown if Fig. 1(b), which can be employed in comb-based wavelength division multiplexing transmitters [39].

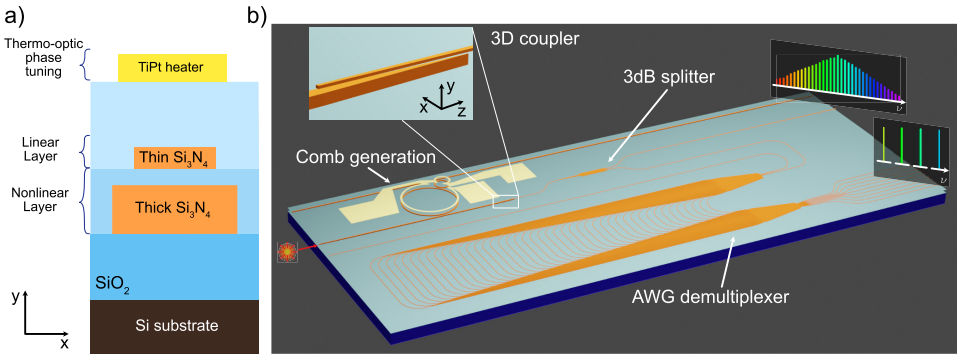

Fig. 1. Multilayer integrated Si_3N_4 platform. (a) Layer stack of the platform with the nonlinear layer fabricated in a strong-confinement dispersion-engineered Si_3N_4 and the linear layer fabricated in single-mode geometry Si_3N_4 waveguide. Metal traces are included for thermo-optic phase tuning of the Si_3N_4 waveguides. (b) Frequency comb demultiplexer exploiting the multi-platform approach.

2. Linear and nonlinear performance tradeoffs

In this section, we analyze the tradeoff between dispersion engineering and single-mode operation in strip silicon nitride waveguides operating in the telecom range (1.5 µm). We consider the term dispersion engineering as the capability of the waveguide to offset the inherent material dispersion for the fundamental mode. In the NIR, both bulk silicon nitride and silica exhibit normal dispersion. We illustrate the examples here with the rectangular geometries that bring the overall dispersion of the fundamental TE mode close to zero.

Optics EXPRESS

Figure 2(a) analyzes the dispersion of the fundamental TE mode and the number of modes sustained by a rectangular core structure. The refractive index data used in the simulation are obtained by spectroscopic ellipsometry in the wavelength range 210 to 2500 nm. Two aspects are clearly apparent, namely, that attaining anomalous dispersion is concomitant with having a waveguide geometry that sustains more than two modes, and reaching single-mode behavior in a strongly-confined geometry forces the mode to have significant interaction with the sidewalls. Because one of the primary sources of scattering loss in a waveguide is the sidewall roughness [17,32], the above analysis demonstrates a complex tradeoff between dispersion engineering, single-mode condition, and scattering loss. Ultralow-loss single-mode waveguides can be achieved by abandoning a strong-confined geometry, i.e., by considering a much thinner waveguide core [4] at the expense of larger bending radii. It is possible to achieve anomalous dispersion in thin Si_3N_4 by coupling two waveguides with dissimilar cross-sections on the same layer [40–42], where the desired dispersion is obtained via the linear coupling between the modes. However, this approach is narrowband and is suitable mainly for telecom or microwave photonics [41].

The tradeoff between scattering loss, single-mode operation, and dispersion engineering has been widely discussed and analyzed in the literature [17,33]. To the best of our knowledge, however, no experimental study analyzes waveguide geometries with different core thicknesses in detail. In this section, we test (and later validate) the general assumption that thinner single-mode waveguides display lower losses than thicker single-mode geometries. We consider three particular waveguide geometries: a dispersion-engineered waveguide with core thickness 740 nm and width 1900 nm (A), a single-mode waveguide with the same thickness and width 800 nm (B) and a thinner single-mode waveguide with core thickness 200 nm and width 1500 nm. The thickness of the latter waveguide was selected to achieve moderate confinement of 34% compared to 90% of waveguide A and 80% of waveguide B. Waveguide C maintains a reasonably small critical bending radius of 100 µm despite the reduced confinement. The modes and core geometries are displayed in the insets of Fig. 2(b), (c), and (d).

To evaluate the loss of the three selected waveguide geometries we fabricated two samples, one for each thickness. The fabrication process was performed on a 100 mm wafer following the same process reported in our previous work [6,43], adapting the process parameters to the two different Si_3N_4 thicknesses. The samples include multiple ring resonators with point coupling and a radius of 227 µm. This value minimizes the bending loss in both platforms and results in a free spectral range (FSR) of approximately 100 GHz. The ring resonator response was evaluated in the wavelength range 1500-1600 nm using a frequency comb calibrated swept-wavelength interferometry setup, as reported in [44]. The histogram of the intrinsic linewidth ($\kappa_0/2\pi$) is reported in Fig. 2(b), (c), and (d). The histograms report the statistical distribution of the linewidth for all the resonances measured.

The dispersion-engineered waveguide (A) displays the best equivalent propagation loss with the most probable value of the histogram at 2.7 dB/m. The increased interaction with the sidewall roughness of the single-mode waveguide (B), results in higher propagation losses (30 dB/m). However, when the platform is optimized for single-mode operation as in waveguide C, the propagation loss is 4.1 dB/m and the waveguide supports only the TE_{00} and TM_{00} modes.

From the characterization of the three core geometries, we conclude that a platform dedicated to linear operation would provide a seven-fold improvement in terms of propagation loss. This analysis motivates the development of the bi-layer approach presented in the following section.

Optics EXPRESS

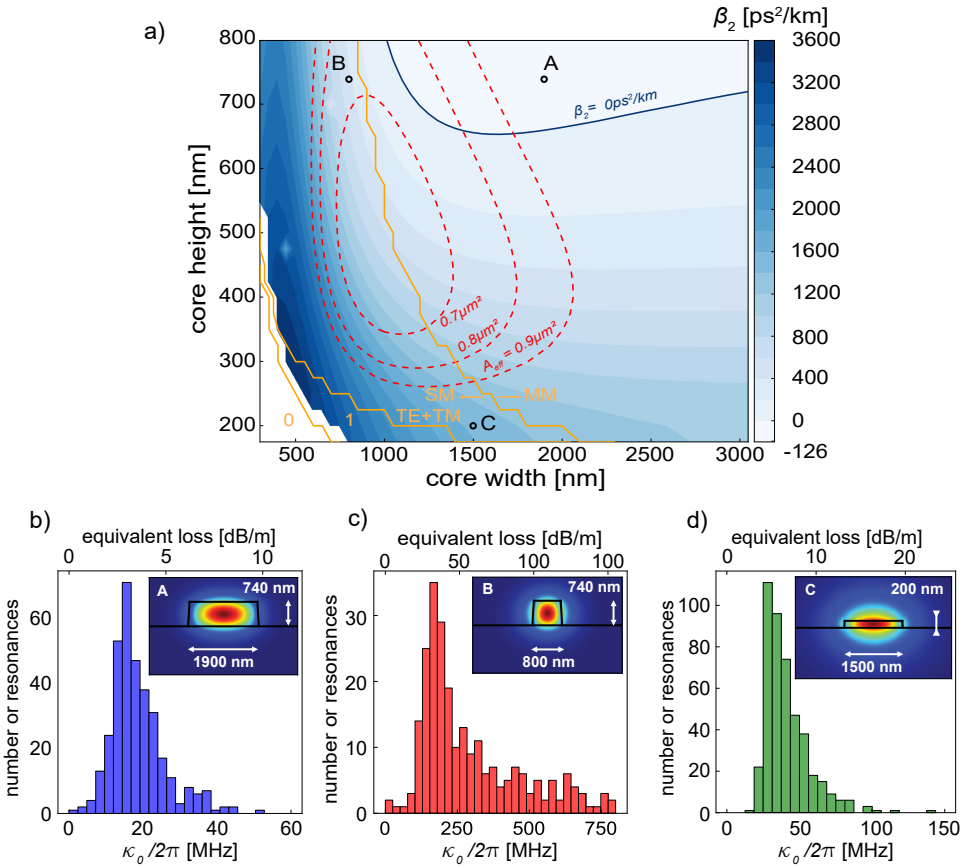

Fig. 2. Performance tradeoffs. (a) The color map shows the simulated group velocity dispersion coefficient (β_2) as a function of the core geometry at wavelength 1550 nm for a waveguide with 87° sidewall angle. The zero dispersion line (blue) denotes the boundary between anomalous dispersion (β_2<0 above the line) and normal dispersion (below the line). The bottom left corner does not support any mode, hence β_2 is not defined. The yellow solid lines mark the core geometries that either do not support any mode (bottom left corner), support one mode or support the fundamental mode in both polarizations. We consider the latter area as the single-mode (SM) waveguide. On the right of the SM line, the waveguide is multimode (MM) in at least one polarization. The red-dashed lines show the effective area of the fundamental TE mode. The points marked with A, B, and C show the core geometries considered in this study. (b)-(d) Histograms of the measured intrinsic linewidth $\kappa_0/2\pi$) and the equivalent propagation loss for the three geometries fabricated. In the insets, we show the x component of the electric field of the fundamental TE modes of the waveguides with the respective core dimensions.

Optics EXPRESS

3. Multilayer integration

Multilayer integration of photonic integrated circuits has been investigated to combine different materials [45–48], to improve the density of interconnects [49] and improve the coupling to optical fibers [12,50]. In this work, we combine two platforms fabricated in the same material (Si_3N_4) but with different thicknesses.

The two photonic layers are fabricated at the wafer level with a process compatible with front-end-of-line CMOS manufacturing [51] starting from a 100 mm Si wafer, oxidized to obtain 3 µm of thermal SiO_2. The steps of the fabrication are reported in Fig. 3(a). After oxidation, we pattern stress release structures to avoid cracks in the SiN layer [52] and we deposit a thickness of 740 nm of stoichiometric Si_3N_4 via low-pressure chemical vapor deposition (LPCVD). This forms the nonlinear layer (NLL) with the dispersion-engineered Si_3N_4 waveguides. Electron beam lithography (EBL) is used to define the waveguides and we etch the wafer with CHF_3 based inductive coupled plasma etching. A buffer layer of SiO_2 is deposited via LPCVD with precursor tetraethyl orthosilicate (TEOS). This buffer layer is used as a top cladding for the first layer and it serves as a sacrificial layer for the planarization process which is performed via chemical mechanical polishing to a target thickness. We deposit 200 nm of Si_3N_4 for the linear layer (LL) on the planarized surface and pattern it with a second EBL exposure, aligned to the NLL. A second deposition of 3 µm of TEOS serves as top cladding. On top of the cladding, we fabricate metal heaters via a lift-off process of evaporated TiPt. Patterning is performed via maskless UV lithography. Finally, the chips are singulated with a combination of SiO_2 etching and deep Si etching. The process of the two individual layers is what we reported in our previous work [6,43] with the exception of the SiO_2 deposition. In this work, it is crucial to have a homogeneous layer of SiO_2, because different deposition techniques give different material density and hardness. The hardness of the material determines the CMP removal rate thus an interface between two materials in the buffer layer can introduce unwanted residual morphology [53].

The LPCVD deposition of TEOS is a conformal process that produces a layer of high quality SiO_2, which copies the etched morphology on the top surface of the PIC (Fig. 3(a) iv). The surface morphology needs to be removed to have a flat surface for the next layer to be fabricated without any extra loss. Moreover, the surface roughness of the deposited TEOS can be significantly higher compared to the surface roughness of the thermal SiO_2 and the deposited Si_3N_4, as reported in Fig. 3(c). This could lead to additional scattering loss in the second layer. Therefore, the planarization step plays a crucial role in the performance of a multilayer PIC.

We used chemical mechanical polishing (CMP) to planarize the surface morphology and define the residual thickness on top of the dispersion-engineered waveguides. We initially calibrated the removal rate of TEOS on unpatterned wafers by measuring the SiO_2 thickness across the wafer before and after polishing with white light reflectance spectroscopy. The removal rate was used to decide the thickness of the TEOS buffer layer to completely planarize the surface morphology given a pattern density of 1%, comparable to the average pattern density of our design. Indeed, the removal rate of the surface morphology depends on the pattern density of the bottom layer [54]. Therefore, we added dummy structures to homogenize the pattern density and we deposited a thick buffer oxide layer to attain a homogeneous residual thickness between the NLL and the LL.

This allowed us to reach a 389±70 nm residual thickness on top of the dispersion-engineered layer with a target residual thickness of 300 nm. The error is calculated as the standard deviation of the residual thickness distribution. The average value is larger than the target, but we decided not to perform a correction polishing step because some points on the wafer had a residual thickness as low as 220 nm. Further polishing would have increased the risk of removing the buffer layer between NLL and LL, compromising the performance of the devices. We confirmed via eigenmode expansion simulation that a residual thickness between 100 nm and 600 nm does not significantly affect the performance of the coupler.

Optics EXPRESS

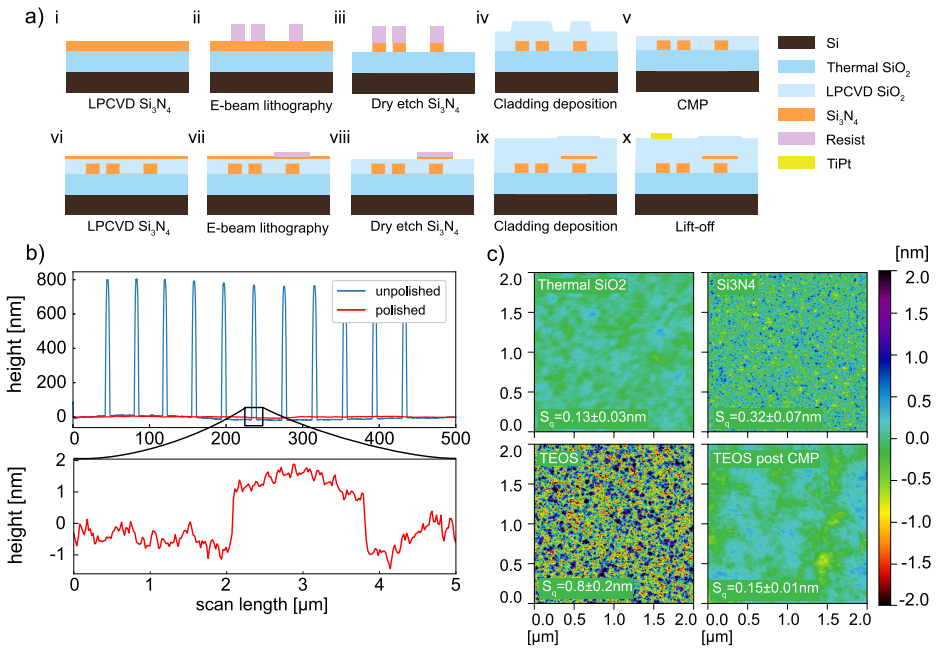

Fig. 3. Multilayer integration process. (a) Fabrication flow of the multilayer device. (b) Surface profiler scan (top) of an array of waveguides before (blue) and after (red) polishing. Atomic force microscopy (AFM) micrograph was acquired on the sample after polishing and a profile is reported (bottom) showing a small residual step. (c) AFM micrographs of the sample in different phases of the process. From top left clockwise: thermal oxide before Si_3N_4 deposition, deposited Si_3N_4, TEOS after and before polishing. All the micrographs share the same colormap scale, reported on the right.

It is crucial to preserve the performance with the added fabrication complexity. CMP is a process that involves chemicals that can affect the optical performance, e.g., KOH [53,55], and nanoparticles of SiO_2, which can adhere to the surface and be difficult to remove. To minimize the added loss due to CMP we cleaned the wafer by submerging it in a megasonic bath and we performed RCA cleaning maintaining the wafer in wet condition. This helps minimize the number of particles that bond on the wafer surface before they are removed by the cleaning process.

After polishing, the surface morphology is completely removed, as shown in Fig. 3(b). Only a step of a few nanometers is present, akin to the waveguide morphology. Since the two layers are not optimized for waveguide crossings, this residual step will affect the two platforms only where the NLL and the LL overlap, which happens only at the 3D couplers shown in Fig. 4(a).

Another advantage of the CMP process is the reduction of the surface roughness of the deposited TEOS layer. In Fig. 3(c) are reported atomic force microscopy (AFM) scans of the oxidized Si wafer, the LPCVD Si_3N_4 and the LPCVD TEOS before and after polishing. All the raw scans were processed by removing a second-degree polynomial plane and rows alignment via slope removal (polynomial of degree 1). The roughness error was calculated as the standard deviation of three measurements taken on different wafers with the same material and similar processing parameters. The thermal SiO_2 displays the best roughness and the Si_3N_4 deposited with LPCVD shows a moderate increase in roughness. The TEOS after deposition displays the worst surface roughness, approaching the nanometer scale. However, after CMP the residual

Optics EXPRESS

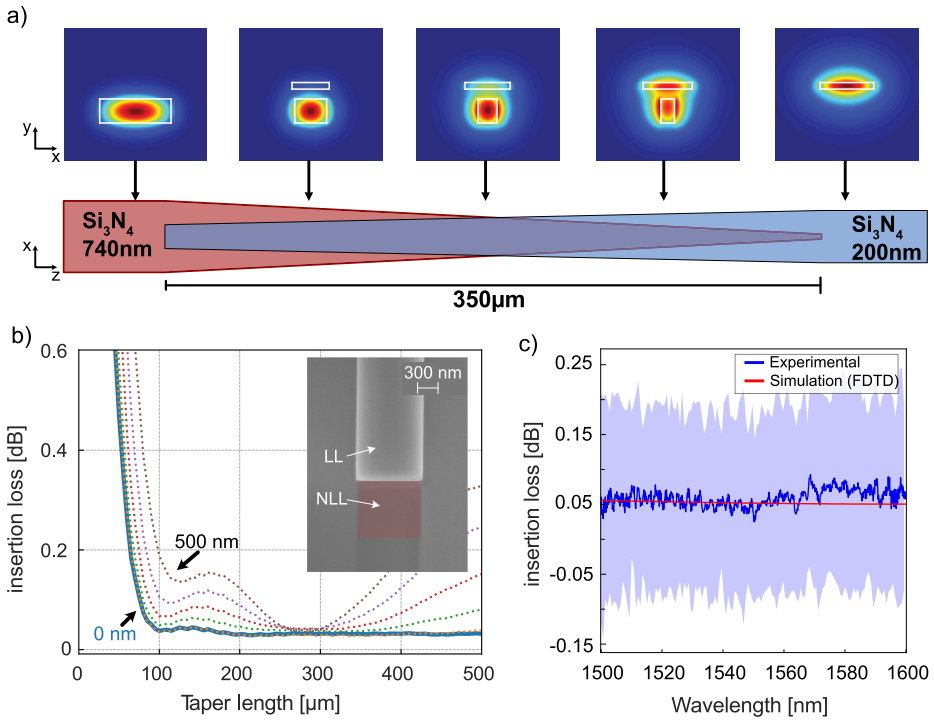

Fig. 4. Interlayer coupling. (a) Schematic of the 3D coupler and evolution of the mode along the double adiabatic taper. (b) Simulation of the alignment tolerance of the 3D taper for shifts of the top layer in the x direction. The solid line represents zero offset and the dashed lines have an offset increment of 100 nm. Inset: SEM top view of the alignment marker with the LL marker and the buried NLL marker (partially highlighted in red). (c) Experimental insertion loss (blue) of a 3D coupler with error bar and simulated loss obtained with FDTD simulation.

roughness is equivalent to the thermal SiO_2, thus restoring a pristine surface where to fabricate the second layer of Si_3N_4.

To couple the two platforms we used a 3D coupler based on a double inverted taper structure [45,49], as shown in Fig. 4(a). This type of coupler adiabatically transfers the mode from the bottom waveguide to the top waveguide.

The double tapered geometry makes this coupler broadband, with an FDTD simulated 0.1dB bandwidth of ~600 nm, and resilient to misalignment, as shown in Fig. 4(b). Shifting the top taper up to 100 nm in the x direction does not affect significantly the transmission efficiency of the coupler as shown in the eigenmode expansion simulations reported on 4(b). Nevertheless, an alignment better than 100 nm must be achieved to not introduce any extra loss in the transition. For this reason, we used buried Si_3N_4 markers, detectable with a deep scan of the EBL at 100 keV acceleration. The alignment between the two layers was measured with a Vernier scale and scanning electron microscopy (SEM) as reported in the inset of Fig. 4(b). Here we can see a top view of the Vernier scale after etching the LL. The LL marker is clearly visible on the top and the buried NLL marker is partially highlighted in red to improve the contrast. The shift between the markers of the Vernier scale is lower than the resolution of the measurement, therefore, we can estimate it to be better than 100 nm.

We used the cut-back method to experimentally evaluate the performance of the 3D couplers. We measured the response of different waveguides where we cascaded an increasing number of

Optics EXPRESS

paired 3D couplers. We linearly interpolated the responses of the devices and obtained the loss per 3D coupler as the slope of the fitted data. The uncertainty reported is calculated from the covariance matrix of the linear fitting. The uncertainty is relatively large and reaches negative values. The negative values have no physical meaning, and they occur due to the uncertainty of the slope calculation when fitting the signal. Indeed, the response of the cascaded couplers is dominated by the insertion loss of the facet (≈1.5 dB/facet), which is affected by the quality of the fiber-to-waveguide alignment. Nevertheless, we can see good agreement between the experimental data and the FDTD simulation, thus, we can conclude that the coupling between the two layers introduces negligible loss across a large bandwidth.

After fabrication of the two layers, we tested the waveguide designs A and C with the same methods described in section 2; now the two ring resonators are fabricated in the same chip. The performance of both platforms is maintained with the multilayer integration. Indeed, we measured an equivalent propagation loss of 3.6 dB/m for design A and 5 dB/m for design C, in line with what we observed in the two independent wafers. This is the first time to our knowledge that a dispersion-engineered silicon nitride layer is co-integrated with a linear single-mode processing unit while preserving ultralow losses.

4. Linear processing of power-efficient microcombs

The multilayer approach is beneficial when a combination of linear and nonlinear operations must be performed on the same chip. As a proof of concept, we designed a power-efficient microcomb [56] and combined it with the LL in two distinct devices: one simple demonstration of the stability of the comb with a 3D coupler and the demultiplexing of the frequency comb.

In the first test (Fig. 5(a)), we combined the microcomb with a 3 dB splitter based on a multimode interference (MMI) coupler, fabricated in the NLL. One of the two branches is coupled out of the chip and used as a reference arm (NLL output in Fig. 5(a)). On the other branch, we added a 3D coupler as described in section 3. The 3dB coupler was characterized to have 0.35 ± 0.09 dB loss by using the cut-back method and cascading seven couplers. Using a splitter before the 3D transition guarantees that the signal at the NLL output is comparable to the one before the 3D coupler. After the coupler, the signal is routed to the edge of the chip to the LL output. In Fig. 5(b) we show the two combs generated and measured from the two different ports and the respective beat notes. Both combs display conversion efficiency >34% and >52 lines with power above -20 dBm. This means that neither the power splitter nor the 3D coupler significantly affects the performance of the generated comb. Moreover, by monitoring the repetition rate beatnotes in Fig. 5(c) we can see that the coherence of the microcomb is maintained in the transition between the platforms. This is crucial for coherent optical communication [57].

In the second demonstration, we combine the same power-efficient microcomb with a demultiplexer on chip based on an arrayed waveguide grating (AWG) designed to filter nine lines of the frequency comb. The AWG is designed and fabricated in the LL. A microscope picture of the device is reported in Fig. 5(d). As in the previous demonstration, we included a 3dB splitter to monitor the frequency comb before it is processed by the AWG. However, in this demonstration, the splitter is added in the thin layer. This allows us to have a more consistent reference of the comb measured at the monitor port and at the input of the device under test, i.e., the AWG. The MMI coupler designed in the LL was characterized to have 0.3 ± 0.1 dB of insertion loss.

The AWG is designed as a 2x9 channel device with 100 GHz channel spacing. One of the two input channels is used as a comb input, the other one is included as a monitor. The nine output channels of the AWG are routed to the edge of the chip and coupled to the measurement setup via tapered fibers. Before demultiplexing the microcomb, we characterized the response of the AWG with a broadband laser frequency comb with 250 MHz spacing to evaluate the response of the device, reported in Fig. 5(f). The AWG shows an insertion loss of 2.5 dB for the best channel. The channel spacing is >90GHz for channels 1-5 and then it drops to 80GHz. The high

Optics EXPRESS

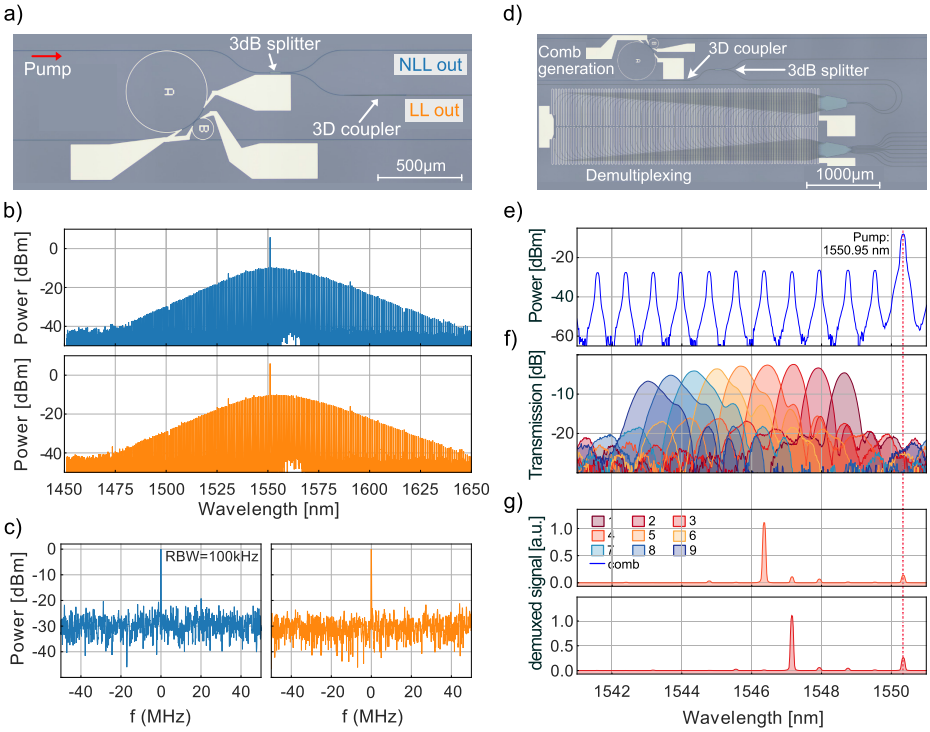

Fig. 5. Linear processing of microcomb. (a) Microscope picture of the power-efficient comb generator combined with a 3dB splitter and a 3D coupler. The NLL and the LL outputs are marked with blue and orange respectively to identify the lines in (b) and (c). The bright lines and pads are the metal heaters and probe pads. (b) On-chip power of the power-efficient microcomb measured at the NLL (blue) and the LL (orange) output. Both display conversion efficiency >34% and >52 comb lines have power > − 20 dBm. (c) Repetition rate beat notes of the soliton generated. The resolution bandwidth (RBW) is 100 kHz. (d) Microscope picture of the power-efficient comb generator combined with an AWG to demultiplex nine frequency lines. (e) Comb lines from the microcomb with conversion efficiency 27% and 69 lines with power > − 20 dBm. The pump location is 1550.95 nm. (f) Characterization of the AWG channels. (g) Demultiplexed comb lines from channels 3 and 4 of the AWG.

Optics EXPRESS

insertion loss and low channel spacing accuracy are due to Si_3N_4 residuals at the interface with the waveguides and the free propagation region. In this region, the pattern density and the narrow gaps of 300 nm make the resist developing and etching more challenging, hence they are more prone to unetched Si_3N_4 residuals. Further process calibration for densely patterned areas can drastically improve the performance of this device.

The demultiplexing of the microcomb was done by tuning the comb so that one of the frequency lines matched one of the channels of the AWG. The generated frequency comb matched to the response of the AWG is reported in Fig. 5(e). In Fig. 5(g), we report two of the demultiplexed lines.

5. Conclusions

In the telecom range, a Si_3N_4 platform designed for Kerr nonlinear optics displays a fundamental tradeoff between loss, confinement, and multimode behavior, which hinders ultralow-loss linear operations. In this work, we have reported an approach to overcome these limitations by monolithically integrating two layers of Si_3N_4 operating in the ultralow-loss regime and tailored for nonlinear and linear operations, respectively. The linear and nonlinear platforms are integrated without significant degradation of the waveguide propagation loss and with negligible transition loss.

This work opens an avenue of opportunities for high-performance linear processing of Kerr nonlinear sources, ranging from quantum optics [38] to chip-scale synthesizers [35]. Furthermore, the additional layer would allow for the development of low-loss fiber-coupling interfaces [58] and a decrease in reflections to slab waveguides of higher-refractive index materials [59], thus facilitating the dense heterogeneous integration with ultralow-loss silicon nitride for high-performance PICs.

Funding. Vetenskapsrådet (2016-06077, 2020-00453, 2019-07048); European Research Council (DarkComb).

Acknowledgments. This work was performed in part at Myfab Chalmers and KTH.

Disclosures. M. G.: Iloomina AB (I,P), O. B. H.: Iloomina AB (I,E), V. T.-C.: Iloomina AB (I,P)

Data availability. Data underlying the results presented in this paper are available at [60].

References

1. S. Y. Siew, B. Li, F. Gao, H. Y. Zheng, W. Zhang, P. Guo, S. W. Xie, A. Song, B. Dong, L. W. Luo, C. Li, X. Luo, and G. Q. Lo, "Review of silicon photonics technology and platform development," J. Lightwave Technol. **39**(13), 4374–4389 (2021).
2. T. Aalto, M. Cherchi, M. Harjanne, S. Bhat, P. Heimala, F. Sun, M. Kapulainen, T. Hassinen, and T. Vehmas, "Open-Access 3-μm SOI Waveguide Platform for Dense Photonic Integrated Circuits," IEEE J. Sel. Top. Quantum Electron. **25**(5), 1–9 (2019).
3. C. De Vita, F. Toso, N. G. Pruiti, C. Klitis, G. Ferrari, M. Sorel, A. Melloni, and F. Morichetti, "Amorphous-silicon visible-light detector integrated on silicon nitride waveguides," Opt. Lett. **47**(10), 2598 (2022).
4. J. F. Bauters, M. J. R. Heck, D. D. John, J. S. Barton, C. M. Bruinink, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding," Opt. Express **19**(24), 24090 (2011).
5. M. H. P. Pfeiffer, C. Herkommer, J. Liu, H. Guo, M. Karpov, E. Lucas, M. Zervas, and T. J. Kippenberg, "Octave-spanning dissipative Kerr soliton frequency combs in Si_3N_4 microresonators," Optica **4**(7), 684–691 (2017).
6. Z. Ye, K. Twayana, P. A. Andrekson, and V. Torres-Company, "High-Q Si_3N_4 microresonators based on a subtractive processing for Kerr nonlinear optics," Opt. Express **27**(24), 35719–35727 (2019).
7. B. Shen, L. Chang, J. Liu, H. Wang, Q. F. Yang, C. Xiang, R. N. Wang, J. He, T. Liu, W. Xie, J. Guo, D. Kinghorn, L. Wu, Q. X. Ji, T. J. Kippenberg, K. Vahala, and J. E. Bowers, "Integrated turnkey soliton microcombs," Nature **582**(7812), 365–369 (2020).
8. H. T. Chen, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, P. Absil, G. Roelkens, and J. Van Campenhout, "High-responsivity low-voltage 28-Gb/s Ge p-i-n photodetector with silicon contacts," J. Lightwave Technol. **33**(4), 820–824 (2015).
9. C. Wang, M. Zhang, X. Chen, M. Bertrand, A. Shams-Ansari, S. Chandrasekhar, P. Winzer, and M. Lončar, "Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages," Nature **562**(7725), 101–104 (2018).

Optics EXPRESS

10. S. Arafin and L. A. Coldren, "Advanced InP Photonic Integrated Circuits for Communication and Sensing," IEEE J. Sel. Top. Quantum Electron. **24**(1), 1–12 (2018).
11. C. T. DeRose, A. L. Lentine, D. C. Trotter, A. L. Starbuck, and R. A. Norwood, "Ultra-low crosstalk, CMOS compatible waveguide crossings for densely integrated photonic interconnection networks," Opt. Express **21**(4), 5198 (2013).
12. Y. Lin, J. C. C. Mak, H. Chen, X. Mu, A. Stalmashonak, Y. Jung, X. Luo, P. G.-Q. Lo, W. D. Sacher, and J. K. S. Poon, "Low-loss broadband bi-layer edge couplers for visible light," Opt. Express **29**(21), 34565–34576 (2021).
13. C. Xiang, J. Guo, W. Jin, L. Wu, J. Peters, W. Xie, L. Chang, B. Shen, H. Wang, Q. F. Yang, D. Kinghorn, M. Paniccia, K. J. Vahala, P. A. Morton, and J. E. Bowers, "High-performance lasers for fully integrated silicon nitride photonics," Nat. Commun. **12**(1), 1–8 (2021).
14. S. Cuyvers, B. Haq, C. Op de Beeck, S. Poelman, A. Hermans, Z. Wang, A. Gocalinska, E. Pelucchi, B. Corbett, G. Roelkens, K. Van Gasse, and B. Kuyken, "Low Noise Heterogeneous III-V-on-Silicon-Nitride Mode-Locked Comb Laser," Laser Photonics Rev. **15**, 2000485 (2021).
15. M. He, M. Xu, Y. Ren, J. Jian, Z. Ruan, Y. Xu, S. Gao, S. Sun, X. Wen, L. Zhou, L. Liu, C. Guo, H. Chen, S. Yu, L. Liu, and X. Cai, "High-performance hybrid silicon and lithium niobate Mach–Zehnder modulators for 100 Gbit s- 1 and beyond," Nat. Photonics **13**(5), 359–364 (2019).
16. P. Mu noz, G. Micó, L. A. Bru, D. Pastor, D. Pérez, J. D. Doménech, J. Fernández, R. Ba nos, B. Gargallo, R. Alemany, A. M. Sánchez, J. M. Cirera, R. Mas, and C. Domínguez, "Silicon nitride photonic integration platforms for visible, near-infrared and mid-infrared applications," Sensors **17**(9), 2088 (2017).
17. X. Ji, S. Roberts, M. Corato-Zanarella, and M. Lipson, "Methods to achieve ultra-high quality factor silicon nitride resonators," APL Photonics **6**(7), 071101 (2021).
18. J. S. Levy, A. Gondarenko, M. A. Foster, A. C. Turner-Foster, A. L. Gaeta, and M. Lipson, "CMOS-compatible multiple-wavelength oscillator for on-chip optical interconnects," Nat. Photonics **4**(1), 37–40 (2010).
19. Y. Xuan, Y. Liu, L. T. Varghese, A. J. Metcalf, X. Xue, P.-H. Wang, K. Han, J. A. Jaramillo-Villegas, A. A. Noman, C. Wang, S. Kim, M. Teng, Y. J. Lee, B. Niu, L. Fan, J. Wang, D. E. Leaird, A. M. Weiner, and M. Qi, "High-q silicon nitride microresonators exhibiting low-power frequency comb initiation," Optica **3**(11), 1171–1180 (2016).
20. J. Liu, A. S. Raja, M. Karpov, B. Ghadiani, M. H. P. Pfeiffer, B. Du, N. J. Engelsen, H. Guo, M. Zervas, and T. J. Kippenberg, "Ultralow-power chip-based soliton microcombs for photonic integration," Optica **5**(10), 1347–1353 (2018).
21. Ó. B. Helgason, F. R. Arteaga-Sierra, Z. Ye, K. Twayana, P. A. Andrekson, M. Karlsson, and J. Schröder, "Dissipative solitons in photonic molecules," Nat. Photonics **15**(4), 305–310 (2021).
22. Z. Ye, F. Lei, K. Twayana, M. Girardi, P. A. Andrekson, and V. Torres-Company, "Integrated, Ultra-Compact High-Q Silicon Nitride Microresonators for Low-Repetition-Rate Soliton Microcombs," Laser Photonics Rev. **16**, 2100147 (2022).
23. Z. Ye, P. Zhao, K. Twayana, M. Karlsson, V. Torres-Company, and P. A. Andrekson, "Overcoming the quantum limit of optical amplification in monolithic waveguides," Sci. Adv. **7**(38), 8150 (2021).
24. R. Halir, Y. Okawachi, J. S. Levy, M. A. Foster, M. Lipson, and A. L. Gaeta, "Ultrabroadband supercontinuum generation in a CMOS-compatible platform," Opt. Lett. **37**(10), 1685–1687 (2012).
25. A. R. Johnson, A. S. Mayer, A. Klenner, K. Luke, E. S. Lamb, M. R. Lamont, C. Joshi, Y. Okawachi, F. W. Wise, M. Lipson, U. Keller, and A. L. Gaeta, "Octave-spanning coherent supercontinuum generation in a silicon nitride waveguide," Opt. Lett. **40**(21), 5117–5120 (2015).
26. M. A. Porcel, F. Schepers, J. P. Epping, T. Hellwig, M. Hoekman, R. G. Heideman, P. J. van der Slot, C. J. Lee, R. Schmidt, R. Bratschitsch, C. Fallnich, and K.-J. Boller, "Two-octave spanning supercontinuum generation in stoichiometric silicon nitride waveguides pumped at telecom wavelengths," Opt. Express **25**(2), 1542–1554 (2017).
27. H. Guo, C. Herkommer, A. Billat, D. Grassani, C. Zhang, M. H. Pfeiffer, W. Weng, C.-S. Brès, and T. J. Kippenberg, "Mid-infrared frequency comb via coherent dispersive wave generation in silicon nitride nanophotonic waveguides," Nat. Photonics **12**(6), 330–335 (2018).
28. I. Rebolledo-Salgado, Z. Ye, S. Christensen, F. Lei, K. Twayana, J. Schröder, M. Zelan, and V. Torres-Company, "Coherent supercontinuum generation in all-normal dispersion Si_3N_4 waveguides," Opt. Express **30**(6), 8641–8651 (2022).
29. M. W. Puckett, K. Liu, N. Chauhan, Q. Zhao, N. Jin, H. Cheng, J. Wu, R. O. Behunin, P. T. Rakich, K. D. Nelson, and D. J. Blumenthal, "422 Million intrinsic quality factor planar integrated all-waveguide resonator with sub-MHz linewidth," Nat. Commun. **12**(1), 934 (2021).
30. J. Liu, G. Huang, R. N. Wang, J. He, A. S. Raja, T. Liu, N. J. Engelsen, and T. J. Kippenberg, "High-yield, wafer-scale fabrication of ultralow-loss, dispersion-engineered silicon nitride photonic circuits," Nat. Commun. **12**(1), 1–9 (2021).
31. C. R. Pollock and M. Lipson, *Integrated Photonics* (Springer, 2003).
32. D. Melati, A. Melloni, and F. Morichetti, "Real photonic waveguides: guiding light through imperfections," Adv. Opt. Photonics **6**(2), 156 (2014).
33. S. Roberts, X. Ji, J. Cardenas, M. Corato-Zanarella, and M. Lipson, "Measurements and Modeling of Atomic-Scale Sidewall Roughness and Losses in Integrated Photonic Devices," Adv. Opt. Mater. **10**, 2102073 (2022).
34. M. Girardi, V. Torres-Company, and A. Larsson, "Performance tradeoffs in low-loss Si_3N_4 waveguides for linear and nonlinear applications," in *23rd European Conference on Integrated Optics* (2022).

Optics EXPRESS

35. D. T. Spencer, T. Drake, and T. C. Briles, *et al.*, "An optical-frequency synthesizer using integrated photonics," Nature **557**(7703), 81–85 (2018).
36. W. Bogaerts, D. Pérez, J. Capmany, D. A. Miller, J. Poon, D. Englund, F. Morichetti, and A. Melloni, "Programmable photonic circuits," Nature **586**(7828), 207–216 (2020).
37. D. Pérez-López, A. Gutiérrez, and J. Capmany, "Silicon nitride programmable photonic processor with folded heaters," Opt. Express **29**(6), 9043–9059 (2021).
38. J. M. Arrazola, V. Bergholm, and K. Brádler, *et al.*, "Quantum circuits with many photons on a programmable nanophotonic chip," Nature **591**(7848), 54–60 (2021).
39. V. Torres-Company, J. Schröder, A. Fülöp, M. Mazur, L. Lundberg, Ò. B. Helgason, M. Karlsson, and P. A. Andrekson, "Laser frequency combs for coherent optical communications," J. Lightwave Technol. **37**(7), 1663–1670 (2019).
40. M. Soltani, A. Matsko, and L. Maleki, "Enabling arbitrary wavelength frequency combs on chip," Laser Photonics Rev. **10**(1), 158–162 (2016).
41. S. Kim, K. Han, C. Wang, J. A. Jaramillo-Villegas, X. Xue, C. Bao, Y. Xuan, D. E. Leaird, A. M. Weiner, and M. Qi, "Dispersion engineering and frequency comb generation in thin silicon nitride concentric microresonators," Nat. Commun. **8**(1), 372 (2017).
42. Z. Yuan, M. Gao, Y. Yu, H. Wang, W. Jin, Q.-X. Ji, A. Feshali, M. Paniccia, J. Bowers, and K. Vahala, "Soliton pulse pairs at multiple colors in normal dispersion microresonators," arXiv, arXiv:2301.10976 (2023).
43. X. Hu, M. Girardi, Z. Ye, P. Mu noz, A. Larsson, and V. Torres-Company, "Si_3N_4 photonic integration platform at 1 μm for optical interconnects," Opt. Express **28**(9), 13019–13031 (2020).
44. K. Twayana, Z. Ye, Ó. B. Helgason, K. Vijayan, M. Karlsson, and V. Torres-Company, "Frequency-comb-calibrated swept-wavelength interferometry," Opt. Express **29**(15), 24363–24372 (2021).
45. W. D. Sacher, Y. Huang, G. Q. Lo, and J. K. S. Poon, "Multilayer silicon nitride-on-silicon integrated photonic platforms and devices," J. Lightwave Technol. **33**(4), 901–910 (2015).
46. C. Xiang, J. Liu, J. Guo, L. Chang, R. N. Wang, W. Weng, J. Peters, W. Xie, Z. Zhang, J. Riemensberger, J. Selvidge, T. J. Kippenberg, and J. E. Bowers, "Laser soliton microcombs heterogeneously integrated on silicon," Science **373**(6550), 99–103 (2021).
47. C. Xiang, W. Jin, O. Terra, B. Dong, H. Wang, L. Wu, J. Guo, T. J. Morin, E. Hughes, J. Peters, Q.-X. Ji, A. Feshali, M. Paniccia, K. J. Vahala, and J. E. Bowers, "Three-dimensional integration enables ultra-low-noise, isolator-free Si photonics," arXiv, arXiv:2301.09989 (2023).
48. J. Mu, M. Dijkstra, Y.-S. Yong, M. de Goede, L. Chang, and S. M. García-Blanco, "Monolithic Integration of Al_2O_3 and Si_3N_4 Toward Double-Layer Active–Passive Platform," IEEE J. Sel. Top. Quantum Electron. **25**(5), 1–11 (2019).
49. W. D. Sacher, J. C. Mikkelsen, P. Dumais, J. Jiang, D. Goodwill, X. Luo, Y. Huang, Y. Yang, A. Bois, P. G.-Q. Lo, E. Bernier, and J. K. S. Poon, "Tri-layer silicon nitride-on-silicon photonic platform for ultra-low-loss crossings and interlayer transitions," Opt. Express **25**(25), 30862–30875 (2017).
50. A. Rao, G. Moille, X. Lu, D. A. Westly, D. Sacchetto, M. Geiselmann, M. Zervas, S. B. Papp, J. Bowers, and K. Srinivasan, "Towards integrated photonic interposers for processing octave-spanning microresonator frequency combs," Light: Sci. Appl. **10**(1), 109 (2021).
51. Y. Huang, J. Song, X. Luo, T.-Y. Liow, and G.-Q. Lo, "CMOS compatible monolithic multi-layer Si_3N_4-on-SOI platform for low-loss high performance silicon photonics dense integration," Opt. Express **22**(18), 21859–21865 (2014).
52. K. Luke, A. Dutt, C. B. Poitras, and M. Lipson, "Overcoming Si_3N_4 film stress limitations for high quality factor ring resonators," Opt. Express **21**(19), 22829–22833 (2013).
53. R. K. Willardson, E. R. Weber, S. M. H. Li, and R. M. Miller, *Chemical Mechanical Polishing in Silicon Processing* (Academic Press, 1999).
54. B. G. Ko, H. C. Yoo, and J. G. Park, "Effects of Pattern Density on CMP Removal Rate and Uniformity," J. Korean Phys. Soc. **39**, 318–321 (2001).
55. J. Seo, "Chemical Mechanical Planarization-Related to Contaminants: Their Sources and Characteristics," Emerg. Contam. (2020).
56. Ó. B. Helgason, M. Girardi, Z. Ye, F. Lei, J. Schröder, and V. Torres-Company, "Power-efficient soliton microcombs," arXiv, arXiv:2202.09410 (2022).
57. P. Marin-Palomo, J. N. Kemal, M. Karpov, A. Kordts, J. Pfeifle, M. H. P. Pfeiffer, P. Trocha, S. Wolf, V. Brasch, M. H. Anderson, R. Rosenberger, K. Vijayan, W. Freude, T. J. Kippenberg, and C. Koos, "Microresonator-based solitons for massively parallel coherent optical communications," Nature **16**, 798–802 (2022).
58. R. S. Tummidi and M. Webster, "Multilayer silicon nitride-based coupler integrated into a silicon photonics platform with <1 db coupling loss to a standard smf over o, s, c and l optical bands," in *Optical Fiber Communications Conference and Exhibition* (2020).
59. A. S. Alam, M. Girardi, A. Caut, A. Larsson, V. Torres-Company, M. Galili, Y. Ding, and K. Yvind, "$LiNbO_3/Si_3N_4$-Bilayer Vertical Coupler for Integrated Photonics," in *Conference on Lasers and Electro-Optics* (IEEE, 2020).
60. M. Girardi, Ó. B. Helgason, A. Caut, M. Karlsson, A. Larsson, and V. Torres-Company, "Data: Multilayer integration in silicon nitride: decoupling linear and nonlinear functionalities for ultralow loss photonic integrated systems," Zenodo (2023), https://doi.org/10.5281/zenodo.8308503.