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Abstract—The switching losses occurring between full soft-switching and hard-switching are described inadequately, and previous attempts of quantifying incomplete zero-voltage switching losses are topology specific and not applicable for any general half-bridge circuit. The ability to quantify these losses is crucial to optimize the converter efficiency across a wide operating range. This paper proposes a general method for accurately estimating the incomplete zero-voltage switching dynamics and losses in half-bridge converters, including the non-linear output capacitance of the semiconductors. The charge balance during the switching transition period is solved to determine the depth of incomplete zero-voltage switching, which can be used to predict the switching losses. The method is verified experimentally, and is shown to be able to predict the depth of incomplete zero-voltage switching accurately, which can be used to calculate the related losses.

I. Introduction

Wide band-gap (WBG) devices such as silicon carbide (SiC) MOSFETs are extending their application range to various high power industries, such as e.g. electric transportation, due to their favorable properties [1]–[4]. Electric drive trains implementing WBG devices are both lighter and less voluminous due to their superior isolation properties and higher switching frequencies. As e-mobility advances towards larger, high voltage batteries to cover heavy-duty vehicles allowing for goods transportation, the demand for high efficient charging stations covering a wide range of battery voltages increases [5]–[8]. Charging standards such as HPC-350 and upcoming megawatt charging system (MCS) cover a large variety of voltage and current operating points [6], [9]. In order to achieve high-efficiency with fast-switching WBG devices, zero voltage switching (ZVS) topologies are an attractive choice for the power converter [6], [10]–[12]. However, ZVS converters typically need to be operated in a application-specific ZVS area. This can cause limitations in the feasible operating area, which poses design challenges for the demands of wide operating range application [13]. Furthermore, the methods to determine the ZVS area are usually subject to topology-specific assumptions, and often do not account for the non-linearity of the semiconductors [13]–[15]. In [14], the output capacitance of the semiconductor is linearized, which leads to inaccurate results at the initial and final stage of the switching transition. Although Incomplete zero-voltage switching (iZVS) was considered, the assumption that the inductor current would decrease linearly to zero during the dead time period required a variable dead time dependent on the inductor current. This is topology-specific and rarely the case in common converter topologies. In [15], the non-linearity of the output capacitance is considered, but the method presented is topology-specific for series resonant converters and does not consider iZVS.

This paper proposes a generally applicable method for determining the border between soft and hard-switching of any half-bridge by predicting the voltage remaining across the device under test (DUT) after the switching transition, including the non-linear output capacitance of the semiconductors, as well as the LC resonant interaction in the circuit. This can be used to quantifies the losses of operating a half-bridge with iZVS and increase the feasible operating area. The proposed method is experimentally verified, allowing to determine the remaining voltage during iZVS at any given operating point from only a handful of known circuit and datasheet parameters.

II. Quantification of Depth of Incomplete Zero-Voltage Switching

In the circuit in Figure 1, the energy stored in the magnetic field of the inductor can be used to achieve soft-switching thus reducing the switching losses in the transistor. However, if the charge provided by the inductor is insufficient to complete the switching transition, iZVS will occur. To quantify the losses during iZVS, the remaining voltage across the DUT after the switching transition period must be determined.

A. Proposed Model

To quantify the magnitude of the remaining voltage across the DUT, the charge balance during the switching transition is solved using four key parameters: The voltages on each side of the inductor v_0 and V_n, the initial current in the inductor at the start of the switching transition i_{L0}, and the non-linear output capacitance of the transistor as a function of voltage $C_{oss}(v_{ds})$. Curve-fitting or a look-up table can be used to obtain the output-capacitance function. Depending on whether Q_H or
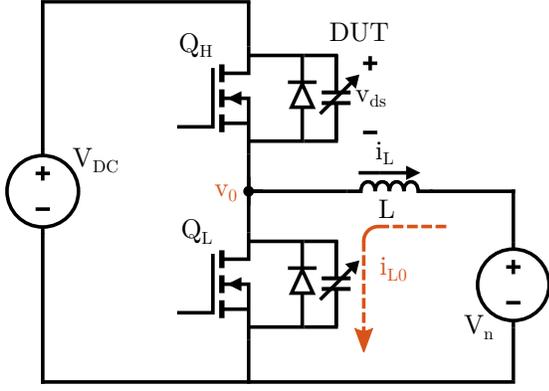
Fig. 1: Half-bridge circuit at the beginning of the switching transition, where Q_L was initially conducting the current i_{L0}, and is to be turned off, while Q_H (DUT) is about to turn on.

Fig. 2: Drain-source voltage of ZVS, iZVS, and hard-switching. The remaining voltage occurring at T_d must be determined to quantify the iZVS losses.

Q_L is considered, the parameters v_0 and initial current i_0 have to be adjusted accordingly.

$$v_0 = \begin{cases} 0 \text{ if DUT} = Q_H \\ V_{DC} \text{ if DUT} = Q_L \end{cases} \quad i_0 = \begin{cases} i_{L0} \text{ if DUT} = Q_H \\ -i_{L0} \text{ if DUT} = Q_L \end{cases}$$ (1)

At the beginning of the dead time period, the voltage across the DUT is equal to the DC voltage, and starts decreasing towards zero as the output capacitance is discharged while the output capacitance of the opposite transistor is charged to the DC voltage. During this period, the circuit shown in Figure 1 can be approximated by replacing the transistors with linearized charge-equivalent capacitors to predict the inductor current.

The output capacitance of a MOSFET is a non-linear function of the V_{ds}, and changes substantially at low voltages [16]. The charge-equivalent capacitance $C_{q,eq}(v_{ds})$ can be calculated by integrating the curve-fitted output capacitance as a function of drain-source voltage from zero to the desired drain-source voltage to get the charge stored at this voltage [14].

$$C_{q,eq}(v_{ds}) = \frac{Q_{oss}(v_{ds})}{v_{ds}}$$ (2)

$Q_{oss}(v_{ds})$ is obtained by integrating $C_{oss}(v_{ds})$ with respect to voltage. By solving the differential equation of the resulting linearized LC-resonant circuit, the time-dependent expression of the inductor current available to discharge the output capacitance of the DUT and charge the opposite transistor can be obtained.

$$i_L(t, v_{ds}) = i_0 \cdot \cos(\omega_0 t) - \frac{v_0 - V_n}{\sqrt{\frac{L}{2C_{q,eq}(v_{ds})}}} \cdot \sin(\omega_0 t)$$ (3)

Where ω_0 denotes the natural frequency of the LC circuit and is given by

$$\omega_0 = \frac{1}{\sqrt{2C_{q,eq}L}}$$ (4)

The charge provided by the inductor during the transition period is expressed as the time-integral of the inductor current from zero to the dead time.

$$\begin{aligned} Q_L &= \int_{t_0}^{T_d} i_L(t)dt \\ &= -\frac{i_0}{\omega_0} \cdot \sin(\omega_0 T_d) + \frac{v_0 - V_n}{\omega_0 \sqrt{\frac{L}{2C_{q,eq}}}} \cdot \left(\cos(\omega_0 T_d) - 1\right) \end{aligned}$$ (5)

In order to ensure ZVS, the charge provided by the inductor has to be larger than the charge stored in the output capacitance of the DUT, and the charge required to turn Q_L off, i.e. raise its voltage to the DC voltage. This relation can be used to calculate the remaining voltage across the DUT.

For ZVS to be achieved, the transistor turning off will require a larger amount of charge in the beginning of the switching transition to increase the voltage due to the non-linearity of the output capacitance. Likewise, the opposing transistor will need to lose additional charge to completely discharge by the end of the dead time period. Integrating the output capacitance from zero to the DC voltage yields the charge stored in the output capacitance at a given voltage. The charge required to change the voltage across the DUT by some voltage v can be quantified as

$$Q_{HB}(v) = \int_0^v C_{oss}(v) + C_{oss}(V_{DC} - v) \, dv$$ (6)

Where $Q_{HB}(v)$ is the charge required to change the voltage across the DUT by the voltage v, and V_{DC} is the initial voltage before turn on. The voltage remaining across the DUT can then be calculated by inserting (5) into (6), and solving for V_{rem}. If the remaining voltage is between zero and the DC voltage, iZVS will occur.

$$Q_L = \int_0^{V_{rem}} C_{oss}(v) + C_{oss}(V_{DC} - v) \, dv$$ (7)

Fig. 3: Example of charge balance in half-bridge during iZVS. The transistors used are C2M0080120D from Wolfspeed [16]. The initial current is 1 A with an inductance of 120 μH. The dead-time is 110 ns and the DC voltage is set to 650 V.

Figure 3 shows an example of the required charge to change the voltage across the DUT by v, and how the remaining voltage across the DUT can be determined by applying (5) and (7). From Figure 3, it can be observed that the charge required to achieve ZVS during the switching transition is equal to 210 nC, which is twice the output charge of the applied transistor with a DC voltage of 600 V. Thus, the initial current to achieve ZVS can be calculated by rearranging (5).

$$i_{zvs}(v_{ds}) = -\frac{\omega_0}{\sin(\omega_0 T_d)} \cdot$$
$$\left(2Q_{oss}(V_{DC}) + \frac{V_n - v_0}{\sqrt{\frac{L}{2C_{q,eq}} \cdot \omega_0}} \cdot (\cos(\omega_0 T_d) - 1) \right) \quad (8)$$

B. Incomplete Zero-Voltage Switching Losses

The losses that occur during iZVS are approximated by calculating the hard-switching losses that would occur if the DUT was hard-switched with the calculated remaining voltage across it. In [17], a method is presented to accurately calculate the hard-switching losses of SiC MOSFETs based on experimental waveforms and device parameters, taking the internal and external circuit parasitics and non-linearities into account. This method is applied to estimate the turn on losses during iZVS.

$$E_{on,iZVS} = \int_0^{t_f} v_{ds}(t) i_{ds}(t) dt - \frac{1}{2} L_{ds} I_0^2 + \frac{1}{2} C_{er}(V_{rem}) V_{rem}^2 \quad (9)$$

Where t_f is the fall time, defined from the end of the dead time period until the voltage across the DUT reaches zero, L_{ds} is the sum of the parasitic drain and source lead inductances,
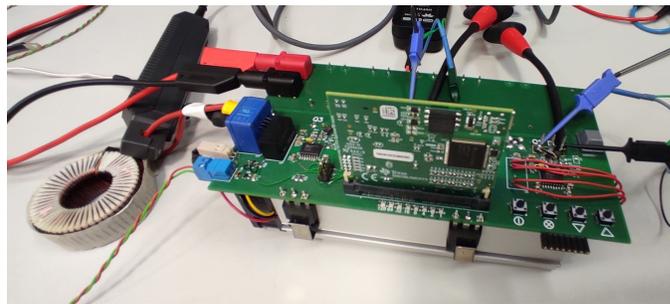
Fig. 4: Full-bridge converter to verify the proposed method.

I_0 is the current at the end of the dead time, and $C_{er}(V_{rem})$ is the energy related capacitance of the output capacitance of the transistor evaluated from 0 V to the remaining voltage, calculated as

$$C_{er}(v) = \frac{2}{V_{rem}^2} \cdot E_{oss}(V_{rem}) = \frac{2}{V_{rem}^2} \cdot \int_0^{V_{rem}} Q_{oss}(v) dv \quad (10)$$

The drain-source voltage in (9) is approximated as linearly decreasing from the remaining voltage towards zero during the fall time. The drain-source current is calculated using (3).

III. EXPERIMENTAL VERIFICATION

A full-bridge circuit with an inductive load is used to verify the proposed method of determining the remaining voltage and iZVS losses at different operating currents. The drain-source and gate-source voltage of the DUT are observed, while the current in the inductor at the start of the switching transition period is adjusted by modulating the transistors as described in [18]. The experimental setup can be seen in Figure 4.

TABLE I: The following parameters are used in the experiment to verify the remaining voltage across the DUT.

DUT Device	Drain-Source Voltage [V]	Dead Time [ns]	Inductor [μH]
Wolfspeed C2M0080120D (SiC)	600	110	170
Infineon IPB65R125C7 (Si)	50	400	170
Infineon IPB65R125C7 (Si)	75	400	170

Both a Si and a SiC MOSFET are tested to verify the model for different types of transistors and output capacitances. The Si MOSFET is tested at low voltages, as the non-linearity will be most significant in these areas. Waveforms for hard-switching, iZVS, and ZVS for the Si MOSFET at 50 V can be seen in Figure 5. The magnitude of the voltage at the turn-on of the DUT shows the converter is hard-switching (a), iZVS (b & c) and ZVS (d) at different switching currents.

Moreover, the drain-source voltage oscillations are of larger magnitude at increased turn-on voltages, due to the increase in dv/dt when the device is turned on. Apart from increased switching losses at higher turn-on voltages, the resulting switching oscillations can cause undesired EMI,

(a) Hard-switching at 50 V and 200 mA.

(b) iZVS at 23 V and −470 mA

(c) iZVS at 5 V and −800 mA

(d) ZVS at −1.3 A
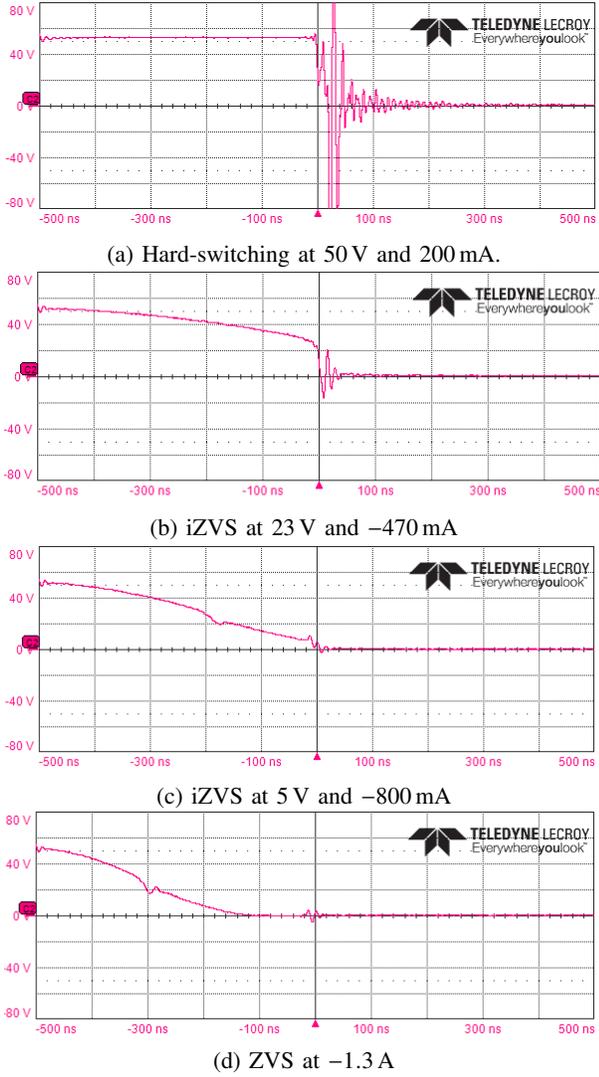
Fig. 5: Experimentally measured drain-source voltage of DUT (Si MOSFET) at different switching currents. The DUT is turned-on at 0 s.

voltage overshoot, additional power losses, and even shoot-through failures, thus severely compromising the performance of the converter [19]. Figure 6 shows the drain-source and gate-source voltages during the switching transition of a SiC MOSFET operating at a DC voltage of 600 V. The remaining voltage after the switching transition at different inductor currents is used to predict the switching modes of the DUT. It can be observed that the transistor enters iZVS when the inductor current is not sufficiently large to provide the required charge to achieve ZVS during the dead time period. The experimentally measured drain-source voltages at turn-on of the DUT are used to evaluate the proposed model.

A. Evaluation of Proposed Model

The obtained values for the remaining voltage at various switching currents are normalized with respect to the DC voltages and compared to the analytical model in Figure 7. It
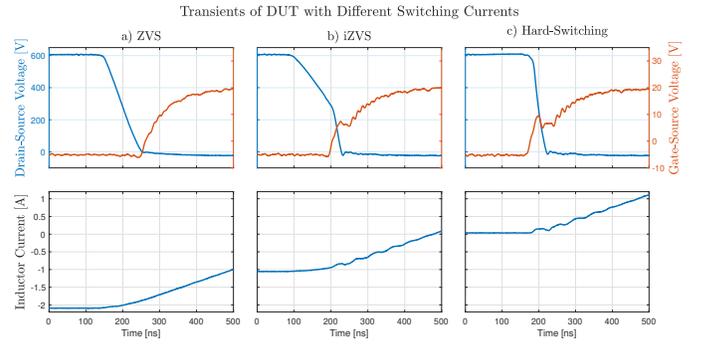
Fig. 6: Experimentally measured switching transients with (a) ZVS at −2.08 A, (b) iZVS at −1.05 A, and (c) hard-switching at 0 A.
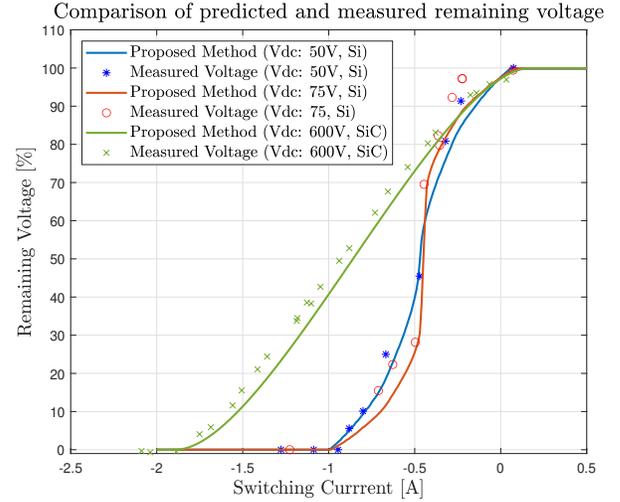
Fig. 7: Comparison of remaining voltage predicted by model and measured experimentally as percentage of the DC voltage of the experiments described in Table I.

can be observed that the non-linearity is most obvious with a Si DUT, which can be attested to the low voltages at which the experiments are conducted. The change in output capacitance is largest at low voltages, which can be observed both at the beginning of the switching transition, when the turn-off transistor is charged from 0 V, as well as at the end of the transition, when the DUT approaches 0 V, as shown in (7). At higher voltages, the linear region of the output charge is reached, which is reflected by the remaining voltage of the SiC device switched at 600 V. To evaluate the accuracy of the proposed model, the root-mean-square deviation (RMSD) from the predicted voltages to the measurements is calculated.

$$\text{RMSD} = \sqrt{\frac{1}{N} \sum_{i=1}^{N} (x_i - \hat{x}_i)^2} \qquad (11)$$

Applied to the normalized data seen in Figure 7, the RMSD of the model with respect to the experimental data is 4.7 %. The model does not account for measurement errors or the influence of parasitics. Furthermore, the function used to
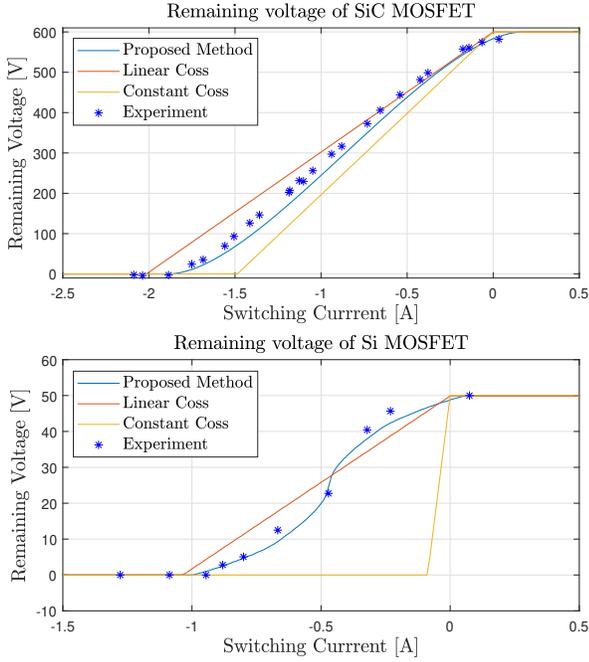
Fig. 8: Comparison of different methods for determining the ZVS current, using Wolfspeed C2M0080120D SiC MOSFET at 600 V.

TABLE II: ZVS current estimation using different methods, compared to experimentally measured

Experiment:	Constant:	Linear:	Proposed:	Measured:
SiC at 600 V	$-1.49\,\text{A}$	$-2.02\,\text{A}$	$-1.90\,\text{A}$	$-1.89\,\text{A}$
Si at 50 V	$-0.09\,\text{A}$	$-1.04\,\text{A}$	$-1.00\,\text{A}$	$0.95\,\text{A}$

calculate the output charge is a numeric integration of a curve-fit of the output capacitance extracted from the SPICE model provided by the manufacturer, which can also cause deviation of the model from experimentally observed results. Figure 8 shows how the proposed model compares with other common methods for predicting the ZVS current. The constant output capacitance method is widely used to determine the ZVS current and uses the value of the output capacitance listed in the datasheet of the device, usually at the rated voltage of the device [13], [20]. This method entirely disregards the effects of the non-linearity of the output capacitance and is therefore the least precise. The linear output capacitance method uses the charge equivalent capacitance as described in [14]. It provides a more accurate estimation, as the charge contribution from the non-linear part is considered. In the areas dominated by the non-linearity however, the method loses accuracy. The RMSD for the linear method is 10 % compared to the experimental results, which is more than twice the RMSD of the proposed method. The predicted ZVS currents of the different methods are presented in Table II. It can be seen that both the linear output capacitance method

Fig. 9: Calculated turn-on energy based on remaining voltage. iZVS between -1.89 and 0 A.

and the proposed model can predict the ZVS current with high accuracy, while the constant output capacitance method fails to make a precise prediction at low DC voltages, as the significant non-linear part is not considered.

B. Calculation of Turn-on Energy

Finally, the remaining voltage is linked to the turn-on energy. The turn-on energy is calculated for the SiC device as described in Section II-B using (9) as a function of the remaining voltage calculated by the proposed method. The dissipated turn-on energy increases non-linearly between complete ZVS and hard-switching in accordance with the remaining voltage. However, the applied turn-on loss estimation method requires many circuit parameters to be known in order to estimate the fall-time and the drain-source parasitic inductance and can be inaccurate if the parameters are not known precisely. Therefore, further research is required to develop a simplified model tying the remaining voltage to turn-on losses, verifying it with a calorimetric test setup to eliminate deviations caused by inaccuracies of the electrical measurements.

IV. CONCLUSION

The proposed method can be used to accurately determine iZVS losses in any half-bridge configuration with only a handful of circuit and datasheet parameters, allowing the circuit design to be optimized accordingly. Despite many possible sources of error, such as parasitic coupling, measurement errors, and potential inaccuracies during curve-fitting of the output capacitance as a function of drain-source voltage, the proposed resonant charge balance method has a low RMSD below 5 %, outperforming other methods for predicting the remaining voltage after the switching transition, as well as the ZVS current. A qualitative significance of the proposed method can clearly be observed when operating with low DC voltages, where the non-linearity of the output capacitance is dominating.

The analytical results determining the depth of iZVS in a half-bridge correlates well with experimental results, and the predicted turn-on energy corresponds to the turn-on energy based on experimental waveforms. The latter should be experimentally verified using a calorimetric test setup, removing the sources of error from electrical measurements. Furthermore, the iZVS losses can be tied to hard-switching losses at a lower DC voltage. To simplify the quantification of switching losses, further research is required to separate and measure turn-on, conduction, and turn-off losses.

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