Temperature distribution of 10 kV and 15 kV SiC-MOSFETs with large edge area

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***Index Terms*—Finite-element method, Thermal behavior, Medium voltage, SiC MOSFET, Modeling.**

***Abstract*—Thermal simulations evaluated temperature distribution of 10kV and 15kV SiC-MOSFETs with larger die edge areas. Experimental temperature measurements of the die surface confirmed thermal modeling. The results revealed that larger edges amplified die surface temperature variation compared to 1.2kV SiC-MOSFET. Simulation results also mentioned temperature variation of bond wires and solder during power cycle testing.**

The superior material properties of Silicon Carbide (SiC) enable power devices such as metal-oxide-semiconductor field-effect transistors (MOSFET) with high performance at high voltage to 10-15 kV and high frequency compared to conventional Silicon insulated gate bipolar transistor (Si-IGBT) [1]. Therefore, they are leading candidates for medium voltage power modules for new high power applications [2], [3]. Some new medium voltage power modules with SiC-MOSFETs were demonstrated [4], [5]. Nevertheless, challenges due to the material properties of SiC are also evident. In SiC power devices, the power cycle (PC) capability, that is a major reliability characteristic, is lower than the Si power devices [6]. This is because their high thermal conductivity and hardness make the thermal stress of solder under the chip higher during PC tests. Thus, package structure optimization to improve PC capability is a major issue in SiC-MOSFET power module design.

Conventional PC design involves the production of PC capability curves based on actual measurements using more than a few dozen samples [7], [8]. On the other hand, only few samples of 10 or 15 kV SiC-MOSFETs dies are available in the market for module design engineers because they are currently still under research and development phase. This causes difficulties of testing enough samples for designing PC capability curves.

Digital design method is attractive for next generation design process to save costs compared with actual prototyping [9]. This can be achieved by utilizing structural optimization and property prediction by 3D simulation in the design phase, thereby reducing the actual number of tests and the minimum samples used in tests. PC design of 10/15 kV SiC-MOSFET power modules is a good case study to apply the digital design.

In the study of failure phenomena occurring in PC testing, thermo-mechanical stress analysis including material degradation are required for accurate lifetime calculations [10]. Therefore, a more practical approach in product design phase is to evaluate the temperature and thermal stress of prototypes to optimize the structure for improving the power cycle performance [11]. It is an approach that attempts to predict PC capability using only simple thermal simulations in order to easily assess the reliability of module product samples. However, simple thermal modeling such as heating at the entire volume of the die is not sufficient to reproduce the actual

heat generation phenomena of power devices. Thermal modeling must reproduce the actual heating area and non-heating area in the device [12]. Therefore, it is necessary to make the thermal modeling of 10/15 kV SiC-MOSFET which has unique properties with small active area and large edge area [13].

The objective of this paper is to verify the thermal characteristics of 10/15 kV SiC-MOSFETs incorporated on power modules by 3D thermal modeling. The thermal simulation results were compared with actual measurement results, and a thermal modeling method that correctly represents the actual heat generation aspect is proposed. Subsequently, the temperature distribution of the bond wires to chip surface junction, and the solder under the chip, which is difficult to evaluate by actual measurement, was compared with the simulation results of a conventional 1.2 kV SiC-MOSFET to identify the difference, thermal distribution of 10 and 15 kV SiC MOSFET power modules.

I. Methodology

Thermal simulation was performed by finite element method (FEM) using ANSYS Mechanical (Workbench 2021 R1). At first, thermal modeling of the SiC-MOSFET chip was investigated. In previous research, thermal modeling of SiC-MOSFETs has been successfully performed with electrothermal modeling [14]. In this study, we demonstrate 3D temperature simulation to simplify, compared with electrothermal modeling. Therefore, it was tried to achieve high simulation accuracy with a simple model by simply dividing the device model into heating and non-heating components. The device heat generation is due to Joule heat generated by the resistance R_{on}, and the dominant components of the resistance is considered as the device heat generation area. Fig. 1 shows the schematic illustration of a typical MOSFET structure on the scale of a single MOSFET cell [15] and one die.

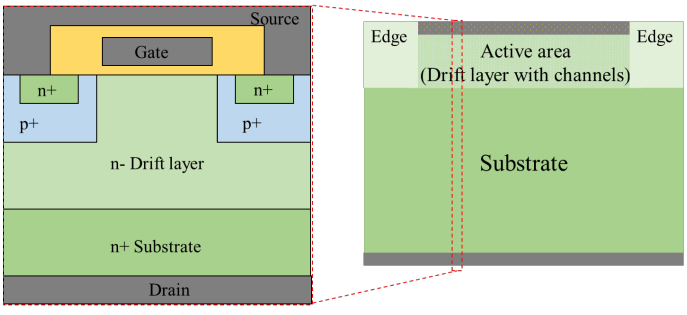


Fig. 1. Schematic illustration of MOSFETs from a single cell [15] to one die scale.

In a one cell unit, the device resistance R_{on} is dominated by the resistance of the drift layer, and channel (n+ for npn MOSFET) and p+ regions around the channel. In conventional 600 V Si-MOSFETs, the resistance of them accounts for 99 percent of the R_{on} [15]. Therefore, it is the region with these resistances that in the one die model is divided into an active area where the volume is heated by Joule heating. Other areas are defined as heat conductive components with no power generation. They are containing edge area of dies. The die size and the edge width are 8.1 mm square, 0.94mm edge width of 10 kV SiC-MOSFET at 20 A/die, and 8 mm square, 1.12mm edge width of 15 kV SiC-MOSFET at 10 A/die [13]. Each die thickness is 500 μm based on measurement results.

Fig. 2 below shows the 3D model of the SiC-MOSFET used in this thermal calculation using the above components.

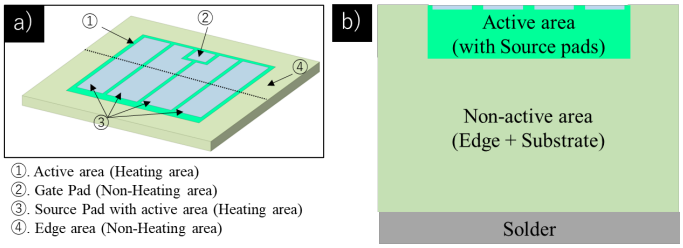


Fig. 2. (a). 3D model of 10kV SiC-MOSFET for thermal simulation, (b). Cross sectional image.

The SiC-MOSFET is modeled as these parts: Active area (n- drift layer, p+ and n+ region), source pad, gate pad, Non-active area (n+ substrate and edge area). As shown in Fig. (2b), the source pad was treated as the active area with the heat generation. The purpose of this paper is to clarify how the temperature distribution during heat generation in the above model affects high-voltage devices with large edge area, which are non-heat generating regions.

As parameters for comparison in the thermal modeling method, simulated temperatures were compared using the following models with different heat generation size in SiC-MOSFETs.

- 1. Entire volume of the die has power dissipation
- 2. Heating at the active area only

the active area thickness is varied from

2-1. 10 μm (thinner than actual drift layer)

2-2. 100/150 μm (actual drift layer depth [13])

2-3. until the die bottom (thicker than actual drift layer)

The sample is a half-bridge power module incorporating 10/15 kV SiC-MOSFETs which is built in-house. The detail of the package is shown in [16]. For this test module model has no casing, terminals or gel.

The picture of power modules and its material structure are shown in Fig. 3, and material properties are shown in Table I [12], [17]–[20].

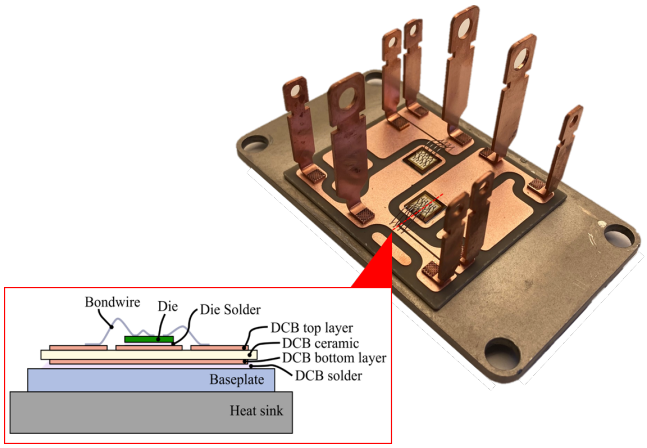


Fig. 3. Power module picture and material structure.

In these models, it was checked whether the thermal simulation results can be correctly reproduced by comparing with the actual measurements. Thermal simulations were performed for each model under the same operating conditions. Thus, the optimal thermal modeling method with suitable heat generating condition was selected.

The operating conditions of the simulation is chosen in such a way, that it is possible to perform the same type of test in a real experiment. A single DC constant power profile was adopted for the power cycle test (on / off = 2 / 3 sec., T_0 = 22 °C).

The applied power value was determined so that it corresponds with a maximum chip surface temperature ΔT_{csmax} = 100 K.

In the actual temperature measurement, the power modules without gels were used. They were mounted on an aluminium heat sink, and they were operated under the same conditions as thermal simulations.

The chip surface temperature was measured with an optical fiber (OTG-F type-10-62ST, from OpSens Solutions) as shown in [21].

II. Results and Discussion

A. Thermal simulation modeling

A 3D thermal model was defined to represent the heat generation aspect of the actual sample by comparing the results of thermal simulations with the actual measurements for 10 kV SiC-MOSFET. Fig. 4 below shows a photograph and 3D model of 10/15 kV SiC-MOSFETs incorporated in a module. The chip surface temperatures on these models were collected along the line profile through the center and each of the four corner points.

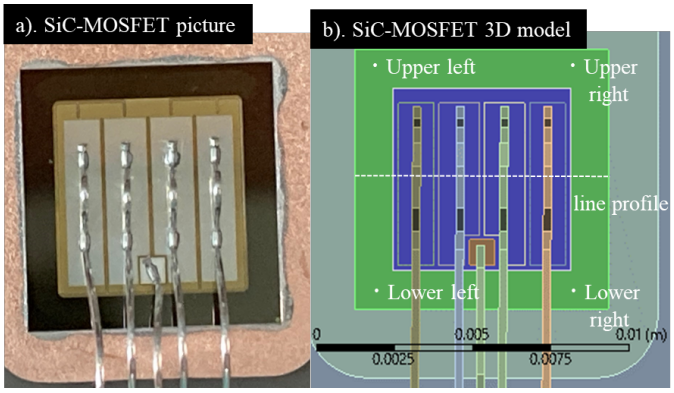


Fig. 4. (a) 10 kV SiC-MOSFET picture, (b) 3D model of 10 kV SiC-MOSFET with temperature measurement points.

A temperature comparison between the measurement and the simulation with different conditions of the die heating for a 10 kV SiC-MOSFET is shown in Fig. 5.

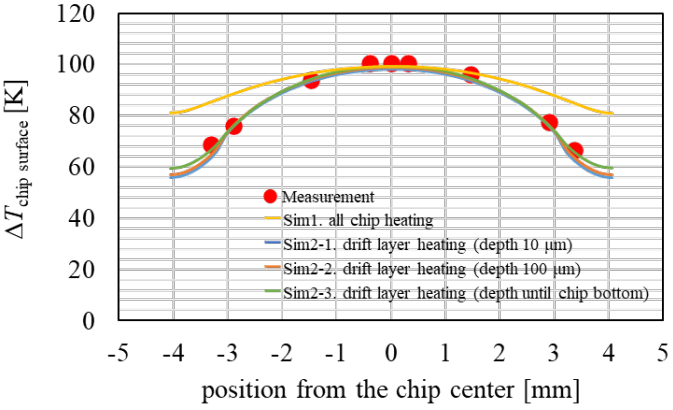


Fig. 5. The temperature line profile of 10kV SiC-MOSFET.

Fig. 5 shows that the model that heats only the drift layer part better represents the measurement temperature of the chip surface than the model that heats the entire volume of the chip. This trend was more evident at the chip edges, which were each more than 3 mm away from the chip center. On the other hand, the difference in temperature simulation results for different drift layer thicknesses was not clear in Fig. 5 for the same drift layer heat generation.

TABLE I
MATERIAL PROPERTIES [12], [17]–[20]

Structure	Material	Thickness	Density [kg/m^3]	Thermal conductivity [W/(m×K)]	Heat capacity [J/(kg×K)]	Reference
Bondwire	Al	250μm	2689	237.5	951	[17]
Die	4H-SiC	550μm	3240	353,3	551,8	[12]
Die solder	96.5Sn-3Ag-0.5Cu	50μm	7370	57	220	[12]
DCB top layer	Cu	300μm	8960	400	385	[18]
DCB ceramics	AlN	630μm	3300	150	710	[19]
DCB bottom layer	Cu	300μm	8960	400	385	[18]
DCB solder	96.5Sn-3Ag-0.5Cu	50μm	7370	57	220	[12]
Baseplate	AlSiC	1.5mm	3010	180	741	[20]
Heat sink	Al	10mm	2689	237.5	951	[17]

Therefore, the results of the 100 μm depth and the drift layer until the die bottom were compared with measurements at the surface temperature of die corners in Fig. 6.

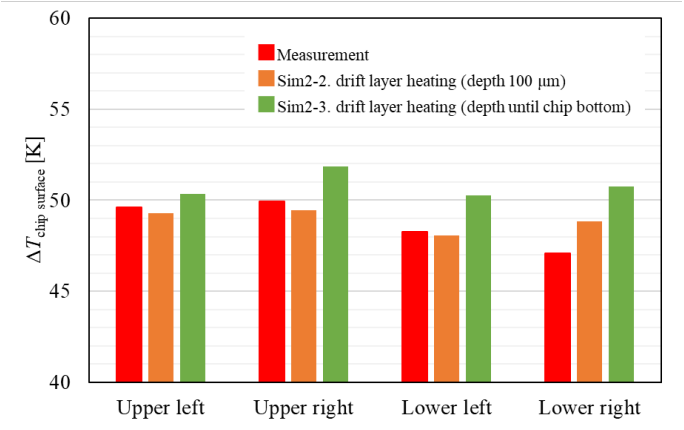


Fig. 6. 10 kV SiC-MOSFET temperature at the four corners.

Fig. 6 showed that the results with the 100 μm depth was the closest to the actual measurements.

The results indicate good agreement with the measurements for both the line profile and the four corners, when the active region with depth of 100 μm was set as the heat generation components of the die.

In order to verify that not only the surface temperature distribution on the die but also the heat path of the entire module was simulated correctly, the temperature of the base plate (i.e. case temperature T_c) for heat dissipation directly under the heat-generating die was also measured and compared with the simulation results. As a result, the maximum case temperature ΔT_{cmax} agreed well with the measured value of 37.8 °C and the simulated value of 40.0 °C. This confirms that both the surface temperature distribution of the heat-generating die and the case temperature up to the backside of the base were correctly calculated in the simulation with actual drift layer heating.

Next, the simulation results of a 15 kV SiC-MOSFET in the same module package are compared with the measured results. The purpose is to check whether the same 3D modeling method is valid for devices with different edge widths and drift layer thicknesses. Similar to the above, the line profiles of the surface temperatures in the 15 kV SiC-MOSFET are compared between measured and simulated results in Fig. 7, respectively.

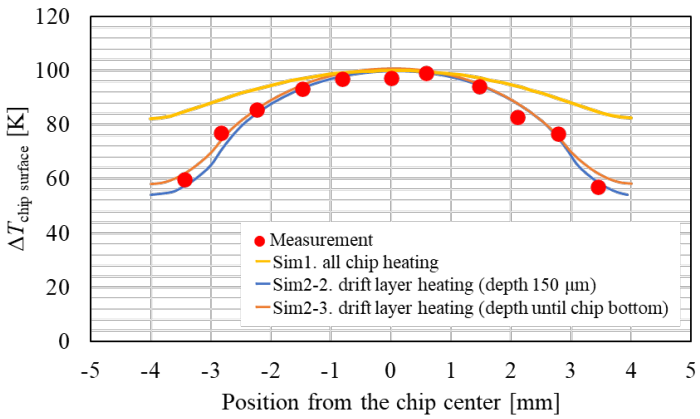


Fig. 7. The temperature line profile of 15 kV SiC-MOSFET.

In the case of 15 kV SiC-MOSFET, the above results show that the 3D model with the actual drift layer depth heating matches well with the actual die temperature distribution at 15 kV SiC-MOSFET. In other words, the actual device heating also occurs in the drift layer, and the 3D model reproduces the actual 3D thermal spread.

B. 10/15 kV temperature distribution investigation for the influence of PC performance

3D thermal modeling has demonstrated the accurate thermal distribution of power modules. This allows investigating the thermal characteristics of power modules

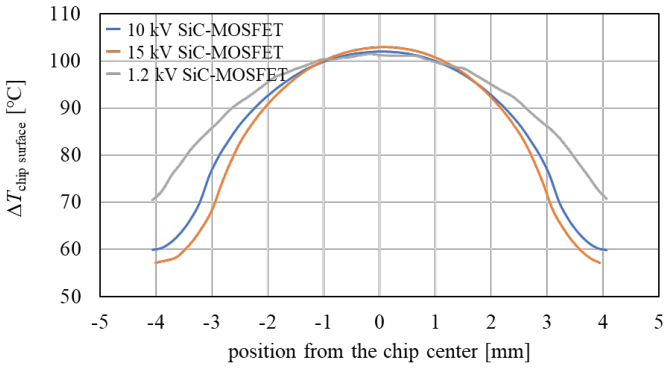


Fig. 8. Comparison of the chip surface temperature.

with 10 kV and 15 kV SiC-MOSFETs from the view of their PC performances. In general, PC capability is defined as the combination of different failure modes such as wire bond lift-off and solder fatigue [22]. It is known that the interfaces of some connection such as bond wires and solders are weak points against the thermal stress [23]. In this part, temperature distribution was evaluated from simulation results of 10 /15 kV SiC-MOSFETs at the two dominant locations in the PC breakdown: the wire on the chip and the solder under the chip, respectively. In order to clarify the thermal characteristics of them, a model assuming a 1.2 kV SiC-MOSFET which is a common low-voltage device with the same size and different device structure was also calculated as a comparison sample. The die size is the same with 8 mm square. The die of 1.2 kV SiC-MOSFET has the 0.17 mm width edge (it includes edge termination width 0.05mm, channel stop region 0.02mm, dicing lane 0.07mm with a margin 0.03mm [24]) , which has 185 μm thickness [25]. This comparison reveals the thermal distribution characteristics of the 10/15 kV SiC-MOSFET.

Fig. 8 shows the simulation results comparing of three SiC-MOSFETs with same die size and different breakdown voltage class (1.2 kV with 0.17 mm edge / 10 kV with 0.94 mm edge / 15 kV with 1.12 mm edge).

The profiles show that the temperature variation around the chip edge is smaller for SiC-MOSFETs with large edge area. This means that the difference between the maximum and minimum temperature of the die surface, i.e. the temperature variation, is greater for 10 kV / 15 kV SiC-MOSFETs than for 1.2 kV SiC-MOSFETs. This is due to the large edge and substrate thickness, which is the heat conductive area, relative to the active area, which is the heat generation area.

C. Thermal distribution of bonded wires

Wire crack which is the major power cycle failure mode was caused by thermal stress based on the aluminium heat expansion [26]. Thus, high temperature of bonding wires causes high thermal stress and decreases the PC capability by wire lift-off [27]. The location of bonding wires on the chip surface is a controllable parameter for wire temperature [28]. Therefore, the chip surface temperature distribution is an important factor in designing of wire placement to improve the PC capability. Accordingly, it was investigated that the temperature distribution during cycling on the wires and device surfaces of power modules with 10/15 kV SiC-MOSFETs.

As wires can reduce thermal stress if they are placed in lower temperature areas of the die surface [21], a larger temperature distribution on the die surface suggests that the wires can be bonded to areas with lower heat generation by moving the wire placement appropriately. On the other hand, large edge areas severely limit the area available for wire bonding. Fig. 9 shows the simulation results of active area surface temperature and wire bonding junction temperature.

10 kV and 15 kV SiC-MOSFETs have a smaller wire bonding area than 1.2 kV SiC-MOSFETs because the wire placement must be more centered on the die. As shown in Fig. 8, the temperature of the die center is higher than at the edge of the die, which leads to higher wire temperatures located on the chip center. However, due to large edge areas that behave as heat dissipation, the temperature gradient on the active area surface of high-voltage SiC-MOSFETs is larger than that of low-voltage one. As a result, the wire temperature of 10 kV and 15 kV SiC-MOSFET is comparable of 1.2 kV SiC-MOSFET as shown in Fig. 9. Larger temperature of bonded wires makes the PC capability of wire failure shorter [27]. This means that wire failure capability of 10 kV and 15 kV SiC-MOSFET is estimated to be the same as the 1.2 kV SiC-MOSFET.

D. Thermal distribution of the solder under the chip

According to the previous research [6], SiC has larger thermal conductivity and higher hardness than Si, it causes larger thermo-mechanical stress of solder layers under the dies. In this section, the influence of chip surface temperature distributions for the solder layer thermal distribution was compared with 10 / 15 kV SiC-MOSFET and 1.2 kV SiC-MOSFET at the same die and solder size. Fig. 10 shows the simulated temperature of the solder layer from the cross sectional view at the same test condition.

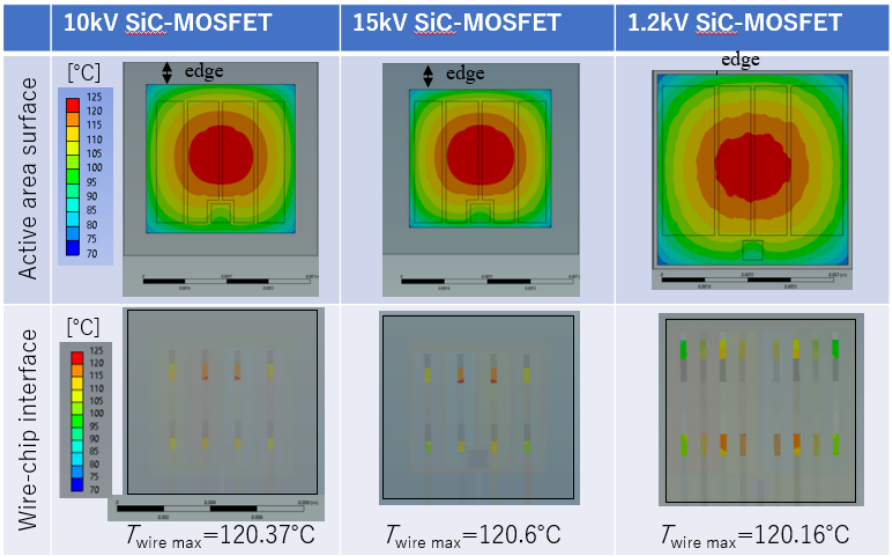
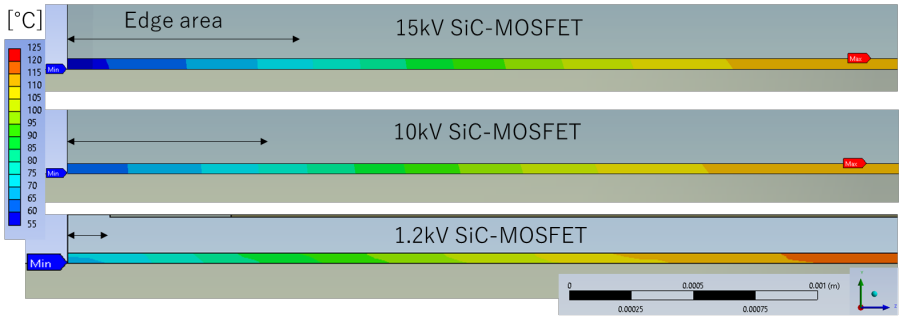


Fig. 9. Temperature distribution of each SiC-MOSFET and bonded wire area.



Sample (Devices)	$T_{solder\ max}$ [°C]	$T_{solder\ min}$ [°C]
1.2V SiC-MOSFET	120.8	65.8
10kV SiC-MOSFET	112.9	59.6
15kV SiC-MOSFET	113.5	57.7

Fig. 10. The temperature simulation results of solder layers.

The results showed that the solder temperature $T_{soldermax}$ and $T_{soldermin}$ of 1.2 kV SiC-MOSFET is higher than 10 kV and 15 kV SiC-MOSFET. This is thought to be due to the thicker die of the high-voltage device makes lower solder temperature.

The comparison between 10 kV and 15 kV shows that the $T_{soldermax}$ is larger at 15 kV while the $T_{soldermin}$ of 15 kV is lower than 10 kV. This can be attributed to the fact that the thickness of the heating layer is 50 μm larger at 15 kV. However, the larger edge area of 15 kV die makes the temperature at the edge of the solder lower. This is understood to be the same phenomenon seen in the chip surface temperature distribution, where the temperature at the chip edge decreases with increasing chip edge size. It was observed that SiC-MOSFETs with larger die thicknesses and edges (10 kV and 15 kV) tended to lower the temperature of the solder layer directly beneath them. This result suggests that the solder layer may be subjected to lower thermal stress during PC testing due to the lower temperature of the solder layer at the same device surface temperature, however further thermal stress analysis is needed to evaluate the details. This difference in solder layer temperature due to edge size and die thickness is not confirmed by conventional thermal modeling in which entire volume of the die is heated.

These results only clarify the thermal distribution. Future verification of thermal stress simulation analysis will enable a more rigorous discussion of the power cycle capability of 10 /15 kV SiC-MOSFETs.

III. Conclusion

Thermal modeling was discussed to analyze the temperature distribution of 10 kV and 15 kV SiC-MOSFET which are incorporated in the power modules.

In the thermal modeling method, an assessment was made by comparing measured results with simulation results using different heat generation regions. It was observed that defining the drift layer as the heat generation region yielded a temperature distribution that closely matched the actual samples. This finding was valid for both 10 kV and 15 kV SiC-MOSFETs, despite variations in device edge sizes and drift layer depths.

The 3D thermal simulations were utilized to investigate the influence of thermal distribution on the power cycling (PC) characteristics of the 10 kV and 15 kV SiC-MOSFETs.

Regarding wire heating, although the wire bonding area was small, the wide edge area resulted in a significant temperature gradient, enabling wire bonding to regions with lower temperatures. Consequently, when compared to a 1.2 kV SiC-MOSFET with a large bonding area but the same die area, the wire temperature remained comparable. Therefore, the expected thermal stress on wires in the 10/15 kV SiC-MOSFETs was similar to that of conventional low-voltage SiC-MOSFETs.

It was found that the temperature of the solder layer below the die was also affected by the temperature distribution of the die. The solder layer heating by conductive from the die heat generation area decreased with increasing die thickness. The solder edge temperature was also smaller with larger die edges. This indicates that the 10kV and 15kV SiC-MOSFETs generate less solder heat than the 1.2kV SiC-MOSFET.

In conclusion, a 3D thermal simulation method was proposed for the advanced devices, namely the 10/15 kV SiC-MOSFETs, which effectively replicated the actual heat generation of the samples. The temperature distribution characteristics obtained from the 3D thermal simulations were then discussed in relation to PC performance, in comparison to a 1.2 kV SiC-MOSFET.

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