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A Quadratic Boost Converter Suitable for Fuel Cell-Powered Electric Vehicles

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***Abstract*—This study presents a non-inverting transformer-less Boost converter with a higher voltage conversion ratio, resulting in quadratic growth of the output voltage with modest increments in the duty cycle rate. The continuous input current of this converter simplifies the input filter design and enhances fuel cells' lifetime and stability. Additionally, compared to existing architectures, this converter reduces the voltage and current stresses on semiconductor components, making it a promising alternative to other quadratic Boost converters. As a result, this topology appears to be a viable alternative for the remaining quadratic Boost converters. The inclusion of common-ground switches, which eliminate the need for additional components for gate driver isolation, is one of the main features that make this topology distinct. As a result, the converter fabrication cost and size are reduced. The proposed converter's steady-state analysis is thoroughly explained. Stresses placed on semiconductor devices. Then, a meaningful comparison between the proposed circuit and its counterparts is provided to understand this converter's unique attributes.**

***Index Terms*—DC-DC converters, Boost converters, quadratic converters, voltage stress, current stress, fuel cell**

I. Introduction

Over the past decades, the development of vehicles running on fossil fuels has caused these sources of energy on the cusp of depletion. It has also contributed to environmental upheavals. As a result of these issues, many researchers have resorted to fuel cell electric vehicles (FCEVs), as viable alternatives to traditional fuel vehicles, since the newly emerged cars do not emit any pollution [1], [2].

Fig 1. depicts the typical FCEV formation. In this architecture, the fuel cell output voltage level is generally lower than the value required to satisfy the inverter's nominal requirements. Having a "soft" output voltage characteristic, the fuel cell, additionally, suffers from instability of the output voltage when a slightly greater current is drawn from the output; that is, the output voltage plunges when the output current is a bit greater than the typical value [3]–[5]. Thus, in order to tackle these two issues, fuel cells need to be connected to inverters by high-gain step-up converters as shown in Fig 1. Isolated DC-DC converters, however, seem suitable since they provide higher voltage gains through the selection of a proper transformer turn ratio, these circuits might not perform efficiently due to the transformer leakage inductance. In addition to electromagnetic interference (EMI) issues, leakage inductance also brings about other problems such as component susceptibility to breaking down [6]. Given that isolated DC-DC converters are gigantic in size and expensive to build, transformer-less Boost converters show signs of being potential candidates [7].

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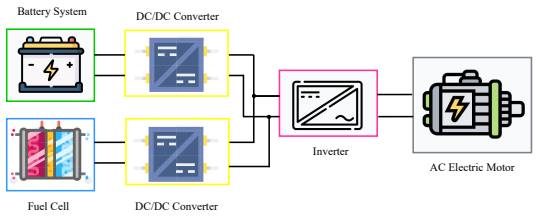

Fig. 1. Fuel cell-powered electric vehicle.

The traditional Boost converter, however, is theoretically expected to provide high voltage conversion ratios provided that extreme duty cycles are chosen. It is feasible to operate with a limited range of achievable voltage gain because of many inevitable rationales including parasitic effects, finite switching frequency, and power losses [8]. Cascaded Boost converters suggested in [9] are expected to solve the high input-to-output voltage gain problem; however, these complex configurations cause some obstacles, such as high voltage and current stresses and low efficiencies. The issues pertaining to the voltage and current stresses, however, are relieved by the three-level Boost converter presented in [10], this topology still has trouble with low voltage conversion gain. Investigated in [11]–[19], quadratic Boost converters appear plausible since they can raise the input voltage. Despite the fact that these configurations all demonstrate the same voltage conversion range, they all suffer from various problems that either increase the fabrication cost or decrease the reliability of the converters, all of which are discussed in the section related to the comparative analysis.

In this study, a transformer-less quadratic Boost converter with the following merits is introduced.

- The current flowing through the input is continuous, making the input filter's design procedure easier.

- Low voltage and current stresses on semiconductor devices.
- Simple control circuits and lower fabrication costs due in part to common-grounded switches.
- Not having instantaneous overvoltage and overcurrent on passive components.

The subject matter of this paper is structured as follows. In II, the proposed converter and its operating principle are explained in depth. The converter is simulated in section III to verify the validity of the theoretical analysis. Following that, the small signal model of the converter and the controller design is presented in section IV. Eventually, the conclusion is provided in section VII.

II. Circuit Description

As depicted in Fig. 2, the proposed converter consists of an input voltage source (V_{in}), two power switches (S_1 and S_2), two diodes (D_1 and D_1), two inductors (L_1 and L_2), and two capacitors known as (C_1 and C_o). It is of interest to mention that the inductor connected to the input voltage source plays a vital role in drawing continuous currents. This is deemed to be one of the main advantages of the presented converter. Furthermore, the common-grounded active switches are toggled simultaneously, which leads to a simplified design of the control circuit. In order to simplify the analysis of the introduced converter, the following assumptions need to be made:

- All components in this converter are perceived as ideal.
- Being large enough, capacitors experience nearly constant voltage during converter operation.
- The inductors used in this architecture are chosen sufficiently large, so the currents flowing through these inductors are ripple-free, and as a result, the converter operates in continuous conduction mode (CCM).

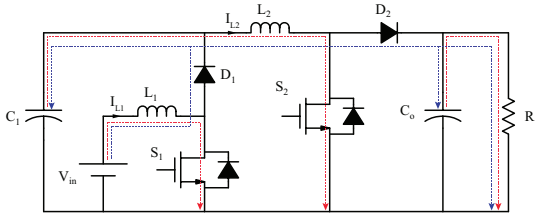

Fig. 2. Configuration of the proposed converter.

A. Steady state analysis

Based on the assumptions mentioned above, the key waveforms in the steady-state condition are depicted in Fig. 3, respectively.

Mode I: At the beginning of this time interval, both active switches are simultaneously turned on, whereas the diodes are reverse biased by V_{c1} and V_{co}. During this stage, the inductors L_1 and L_2 are magnetized by the input voltage source V_{in}, and the energy stored in the capacitor C_1, respectively. The capacitor C_o, similarly, is discharged and energy is transferred

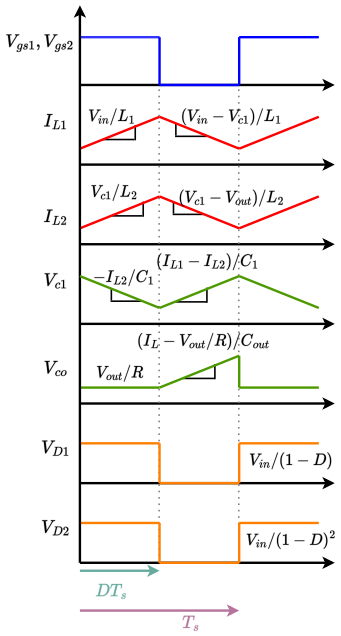

Fig. 3. Key waveforms.

to the output load. Therefore, the capacitor voltages decrease linearly and the inductors' currents, conversely, follow upward trends with diverse slopes. With regards to the current path shown in Fig. 2, the following equations could be induced.

$$\begin{aligned} V_{L1} &= L_1 dI_{L1}/dt = V_{in}, \\ V_{L2} &= L_2 dI_{L2}/dt = V_{c1}, \\ I_{c1} &= C_1 dV_{c1}/dt = -I_{L2}, \\ I_{co} &= C_o dV_{co}/dt = -V_{out}/R, \\ V_{co} &= V_{out}, \end{aligned} \tag{1}$$

where R represents the output load.

Mode II: Once the active switches are turned off, the diodes are forward-biased. Hence, the capacitor C_1 is charged by the magnetizing energy saved in the input inductor L_1. The output capacitor C_o is, similarly, charged by both the input voltage source and the energy stored in the inductor L_2. Hence, the voltage levels across all these two capacitors augment linearly, whereas the inductors' currents follow opposite trends, falling from their peaks. The mathematical equations obtained in this period are as follows:

$$\begin{aligned} V_{L1} &= L_1 dI_{L1}/dt = V_{in} - V_{c1}, \\ V_{L2} &= L_2 dI_{L2}/dt = V_{c1} - V_{out}, \\ I_{c1} &= C_1 dV_{c1}/dt = I_{L1} - I_{L2}, \\ I_{co} &= C_o dV_{co}/dt = I_{L2} - V_{out}/R, \\ V_{co} &= V_{out}. \end{aligned} \tag{2}$$

By applying the volt-second balance principle to the inductors L_1 and L_2 and using (1) and (2), the average voltages across the capacitors C_1 and C_o are written as follows:

$$\begin{aligned} V_{c1} &= V_{in}/1-D \\ V_{co} &= (1-D)V_{out} \end{aligned} \tag{3}$$

By combining the equations given in the (3), the ideal voltage conversion ratio is obtained as:

$$M = V_{out}/V_{in} = 1/(1-D)^2, \tag{4}$$

which means that the input voltage is quadratically boosted as the duty cycle increases.

B. Design procedure of the semiconductor equipment

Voltage stresses placed on switching equipment have profound impacts on the selection of proper components. Based on what has been expressed in the steady state condition, the drain-source voltages on the switches S_1 and S_2, which are, respectively, clamped by the capacitors C_1 and C_o, are obtained as follows:

$$\begin{aligned} V_{s1} &= V_{in}/1-D, \\ V_{s2} &= V_{in}/(1-D)^2. \end{aligned} \tag{5}$$

Comparably, the maximum reverse voltages which diodes D_1 and D_2 should endure are achieved as:

$$\begin{aligned} V_{D1} &= V_{in}/1-D, \\ V_{D2} &= V_{in}/(1-D)^2. \end{aligned} \tag{6}$$

By applying the ampere-second balance principle to the capacitors C_1 and C_o and using (1) and (2), the following equations could be achieved.

$$\begin{aligned} I_{L1} &= V_{in}/(1-D)^4 R, \\ I_{L2} &= V_{in}/(1-D)^3 R. \end{aligned} \tag{7}$$

Also, the current which passes into the switches $S_1$and S_1 are as follows:

$$\begin{aligned} I_{S1} &= DI_{L1}, \\ I_{S2} &= DI_{L2}. \end{aligned} \tag{8}$$

By substituting (7) into 8, the maximum current stresses passing through the power switching equipment are written as:

$$\begin{aligned} I_{S1} &= DV_{in}/(1-D)^4 R, \\ I_{S1} &= DV_{in}/(1-D)^3 R. \end{aligned} \tag{9}$$

Likewise, the forward-biased currents of the diodes are as:

$$\begin{aligned} I_{D1} &= V_{in}/(1-D)^3 R, \\ I_{D2} &= V_{in}/(1-D)^2 R \end{aligned} \tag{10}$$

As a result, the specifications of the required switching devices are obtained.

C. Design Guidance of Passive Components

To select appropriate inductors with certain specifications, the current ripple is the key factor that must be deemed. In this case, as the converter is supposed to operate under CCM, the minimum values of the currents flowing through the inductors L_1 and L_2 should be positive as shown in (11). By substituting the inductors' energy-saving equation presented in (7) into the inductors' current ripple equations given in (11), the minimum selectable values for the inductors are obtained. In these mathematical equations, ΔI_{L1} and ΔI_{L2} are the maximum allowable current deviations that could be considered concerning the converter's load requirements.

TABLE I
PARAMETER SPECIFICATIONS

Parameters	***Values***
Input Voltage (V_{in})	100-300
Output Voltage (V_{out})	800V
Output Power (P_{out})	100 KW
Inductor (L_1)	$450\mu H$
Inductor (L_2)	$500\mu H$
Capacitor (C_1)	$25\mu F$
Capacitor (C_o)	$10\mu F$
Switching Frequency (f_s)	$100KHz$

$$\begin{aligned} I_{L1,min} &= I_{L1} - \Delta I_{L1}/2 > 0, \\ I_{L2,min} &= I_{L2} - \Delta I_{L2}/2 > 0, \end{aligned} \tag{11}$$

$$\begin{aligned} \Delta I_{L1} &= D(1-D)^2 V_{out}/L_1 f_s, \\ \Delta I_{L2} &= D(1-D) V_{out}/L_2 f_s. \end{aligned} \tag{12}$$

It is worth mentioning that the inductors' currents are ensured to be non-pulsating if the inequalities given in (12) are met. Otherwise, the continuity of these currents is not ascertained and difficulties alongside the pulsating currents consequently arise.

$$\begin{aligned} L_1 &> D(1-D)^4 R/2f_s, \\ L_2 &> D(1-D)^2 R/2f_s. \end{aligned} \tag{13}$$

The maximum voltage ripples happening in the capacitors C_1 and C_o are the main parameters through which proper capacitors are chosen. For this purpose, (1) and (1) should be taken into account and merged, which culminates in (14).

$$\begin{aligned} \Delta V_{c1} &= V_{out} D/RC_1 f_s(1-D), \\ \Delta V_{co} &= V_{out} D/RC_o f_s. \end{aligned} \tag{14}$$

Thus, the voltage deviation on each capacitor could be easily designed based on the requirements of the application.

III. SIMULATION RESULTS

In order to verify the theoretical concepts, the converter with the specifications provided in Table I is simulated by Simulink/MATLAB software. Fig 4. shows the time-domain waveforms of the converter. According to the inductors' currents, the CCM operation of the converter is ascertained. In addition to this, the average currents of the inductors L_1 and L_2 are, respectively, 902A and 318A, both of which are in accordance with the values obtained by (7). Besides, given the input voltage and the duty cycle are selected to be 100 V and %64.64, the average output voltage and the average voltage placed across the capacitor C_1 are equal to 800 V and 283 V which are consistent with the theoretically calculated values by (3).

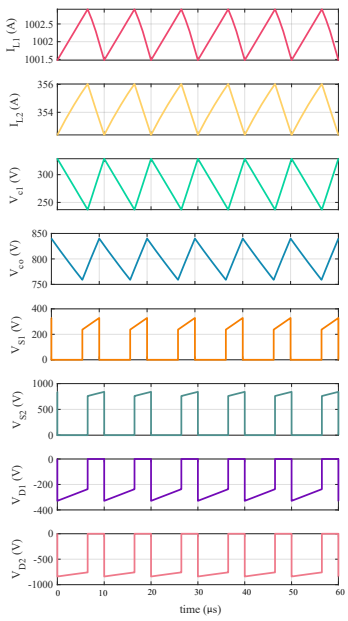

Fig. 4. Time domain-based key waveforms of the simulated converter.

IV. Small Signal Modeling and Controller Design

Since small signal modeling is a promising approach by which the dynamic behaviors of various power converters can be observed, it is applied to the envisioned converter. As can be seen from (15), it is noteworthy that $\langle I_{L1}\rangle$, $\langle I_{L2}\rangle$, $\langle V_{c1}\rangle$, and $\langle V_{co}\rangle$ are, respectively, the average values of I_{L1}, I_{L2}, V_{c1}, and V_{co}. With regards to these equations, the average input voltage, the average voltages placed across the capacitors, the average currents passing into the inductors, and the average duty cycle are the summation of the DC value of each parameter, being the corresponding capital letters, and their ac perturbations, shown by characters with hat and being far less than their own DC values.

$$\begin{aligned}
\langle V_{in}\rangle &= V_{in} + \hat{V}_{in} \qquad V_{in} \gg \hat{V}_{in},\\
\langle V_{co}\rangle &= V_{co} + \hat{V}_{co} \qquad V_{co} \gg \hat{V}_{co},\\
\langle V_{c1}\rangle &= V_{c1} + \hat{V}_{c1} \qquad V_{c1} \gg \hat{V}_{c1},\\
\langle I_{L1}\rangle &= I_{L1} + \hat{I}_{L1} \qquad I_{L1} \gg \hat{I}_{L1},\\
\langle I_{L2}\rangle &= I_{L2} + \hat{I}_{L2} \qquad I_{L2} \gg \hat{I}_{L2},\\
d &= D + \delta d \qquad D \gg \delta d.
\end{aligned} \tag{15}$$

After substituting the equations given in (15) into the differential equations given in (1) and (2) and neglecting higher order terms, the state space model given in (16) could be derived. By applying the Laplace transform to (16), the output-to-control transfer function defined as $G_{\delta d\to\delta y}$ could be calculated, given in (18).

$$d/dt \begin{bmatrix} \hat{I}_{L1}\\ \hat{I}_{L2}\\ \hat{V}_{c1}\\ \hat{V}_{co}\end{bmatrix} = A \begin{bmatrix} \hat{I}_{L1}\\ \hat{I}_{L2}\\ \hat{V}_{c1}\\ \hat{V}_{co}\end{bmatrix} + B \begin{bmatrix} \delta d\\ \hat{V}_{in}\end{bmatrix}, \tag{16}$$

where matrices A and B are defined as follows:

$$A = \begin{bmatrix} 0 & 0 & \frac{-(1-D)}{L_1} & 0\\ 0 & 0 & \frac{1}{L_2} & \frac{-(1-D)}{L_2}\\ \frac{(1-D)}{C_1} & \frac{-1}{C_1} & 0 & 0\\ 0 & \frac{1-D}{C_o} & 0 & \frac{-1}{RC_o}\end{bmatrix}, B = \begin{bmatrix} \frac{V_{c1}}{L_1} & \frac{1}{L_1}\\ \frac{V_{Co}}{L_2} & 0\\ \frac{-I_{L1}}{C_1} & 0\\ \frac{-I_{L2}}{C_o} & 0\end{bmatrix} \tag{17}$$

As a result, the behavior of the circuit both in transient and steady-state conditions could be investigated, which is crucial from a control point of view. $G_{Controller}$ indicates the transfer function by which the performance requirements for the proposed converter in the closed-loop control are held. Regarding the components' specifications in Table I, the bode diagram of the open-loop system and the closed-loop one compensated by a lead-lag controller are illustrated in Fig. 5 (a). As can be seen in this figure, the loop gain system is unstable which should be stabilized by the controller. To ensure stability, it is crucial to shape the loop gain curve to achieve a stable system response through the designed controller. The proposed controller alters the magnitude and phase characteristics of the loop gain curve to maintain stability margins, such as gain and phase margins, that ensure robust and stable system behavior.

$$\begin{aligned}
G_{\delta d\to\delta y} &= \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0},\\
b_3 &= -C_1 L_1 L_2 I_{L2} R,\\
b_2 &= C_1 L_1 L_2 R V_{co}(1-D),\\
b_1 &= -R I_{L2} L_2 (1-D)^2 - R I_{L1} L_1 (1-D) + L_1 I_{L2},\\
b_0 &= R L_2 V_{co}(1-D)^3 + R(V_{in} + V_{c1})(1-D)^2,\\
a_4 &= C_1 C_o L_1 L_2 R,\\
a_3 &= C_1 L_1 L_2,\\
a_2 &= (C_1 L_1 + C_o L_2) R (1-D)^2 + C_o L_1 R,\\
a_1 &= L_2 (1-D)^2 + L_1,\\
a_0 &= R(1-D)^4.
\end{aligned} \tag{18}$$

Moreover, the bandwidth of the closed-loop system is determined such that the input voltage variation, as a disturbance, is suppressed by % 90 at the output for all variations with frequencies less than the lower-left highlighted zone shown in Fig. 5(a). Additionally, another highlighted zone that ascertains the measurement noise suppression is demonstrated in the upper-right demonstrated in Fig. 5(a). Besides, the system frequency response exhibits a peak response at $f = 10$ KHz, which might cause instability in the presence of system-unknown uncertainties. To address this issue, a pole at $f = 30$ Hz is added to ensure the resonant peak is always below 0 dB. Given the following considerations, the proposed controller $G_{Controller}(s)$ is designed as:

$$G_{Controller(s)} = \frac{1.8}{6}\frac{s+100}{s^2+500s}, \tag{19}$$

Shown in Fig. 5(a), the bode diagram of the closed-loop system does not cross the forbidden zone and provides enough

TABLE II
COMPARISON WITH THE OTHER EXISTING TOPOLOGIES

Ref.	No. of Components (S-D-L-C-T)	Voltage Gain	Voltage Stresses on the Switches	Voltage Stresses on the Diodes	Current Stresses on the Switches	Current Stresses on the Diodes	Common-Grounded Switches	Control Circuit
[15]	1-3-2-2-8	$\frac{1}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	D_1 $\frac{V_{in}}{(1-D)^2}$ D_2 $\frac{V_{in}}{1-D}$ D_3 $\frac{DV_{in}}{(1-D)^2}$	$\frac{(2-D)DV_{in}}{R(1-D)^4}$	D_1 $\frac{V_{in}}{R(1-D)^2}$ D_2 $\frac{DV_{in}}{R(1-D)^3}$ D_3 $\frac{V_{in}}{R(1-D)^4}$	–	Simple
[16]	1-3-2-2-8	$\frac{1}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	D_1 $\frac{V_{in}}{(1-D)^2}$ D_2 $\frac{DV_{in}}{(1-D)^2}$ D_3 $\frac{V_{in}}{1-D}$	$\frac{(2-D)DV_{in}}{R(1-D)^4}$	D_1 $\frac{V_{in}}{R(1-D)^2}$ D_2 $\frac{DV_{in}}{R(1-D)^4}$ D_3 $\frac{V_{in}}{R(1-D)^3}$	–	Complex
[17]	2-2-2-2-8	$\frac{1}{(1-D)^2}$	S_1 $\frac{V_{in}}{1-D}$ S_2 $\frac{V_{in}}{(1-D)^2}$	D_1 $\frac{(2-D)V_{in}}{(1-D)^2}$ D_2 $\frac{V_{in}}{1-D}$	S_1 $\frac{DV_{in}}{R(1-D)^3}$ S_2 $\frac{DV_{in}}{R(1-D)^4}$	D_1 $\frac{V_{in}}{R(1-D)^2}$ D_2 $\frac{DV_{in}}{R(1-D)^3}$	No	Complex
[18]	2-2-2-2-8	$\frac{1}{(1-D)^2}$	S_1 $\frac{V_{in}}{1-D}$ S_2 $\frac{V_{in}}{(1-D)^2}$	D_1 $\frac{V_{in}}{1-D}$ D_2 $\frac{V_{in}}{(1-D)^2}$	S_1 $\frac{DV_{in}}{R(1-D)^3}$ S_2 $\frac{DV_{in}}{R(1-D)^3}$	D_1 $\frac{DV_{in}}{R(1-D)^4}$ D_2 $\frac{DV_{in}}{R(1-D)^2}$	Yes	Complex
Proposed Converter	2-2-2-2-8	$\frac{1}{(1-D)^2}$	S_1 $\frac{V_{in}}{1-D}$ S_2 $\frac{V_{in}}{(1-D)^2}$	D_1 $\frac{V_{in}}{1-D}$ D_2 $\frac{V_{in}}{(1-D)^2}$	S_1 $\frac{DV_{in}}{R(1-D)^4}$ S_2 $\frac{DV_{in}}{R(1-D)^3}$	D_1 $\frac{V_{in}}{R(1-D)^3}$ D_2 $\frac{V_{in}}{R(1-D)^2}$	Yes	Simple

margin for the resonant point not to enter the unstable area when uncertainties exist. To verify the effectiveness of the designed controller, the closed-loop system is simulated while the input voltage is disturbed by %10 of the input voltage. As can be seen from Fig. 5(b), even though the input voltage is disturbed, the output voltage of the introduced circuit maintains constant.

V. COMPARITIVE ANALYSIS

In this section, a meaningful comparison between the proposed converter and other related structures as shown in Table II is performed to corroborate the merits of the introduced structure. In terms of the voltage gain, it is obvious from Fig. 6(a) that the proposed converter witnesses the capability of lifting up the input voltage either the same or even higher than the other counterparts which have more components [11]. Moreover, compared to [17] which suffers from having floating switches, the converter introduced in this paper possesses common-grounded switches and as a result, the control circuit of this converter is both simple and cheap to implement. What also makes the proposed converter distinct in contrast with the topology presented in [19] is the simple control circuit; that is, the switching devices used in the presented architecture operate simultaneously, whereas its counterpart does not have this feature. Additionally, unlike the converter suggested in [16], the proposed converter has continuous input current which is a must for FCEV applications. Fig. 6(b) shows

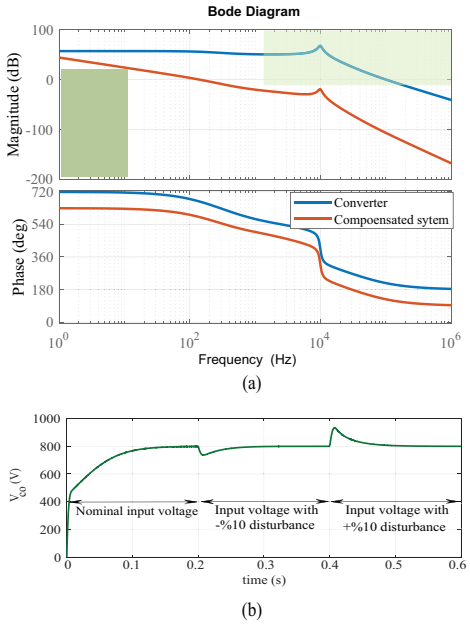

Fig. 5. (a) Bode diagram of the system, and (b) Output voltage and current while the input voltage of the compensated system varies.

a precise comparison between the average standing voltage obtained by the proposed converter and that of those derived from other topologies with the same voltage conversion ratio.

As can be seen in Fig. 6(b), compared to the other circuits, the proposed converter has the lowest voltage stress when the duty cycle is nearly higher than % 45, however, the configurations suggested in [15], [16] show the lowest standing voltage for lower duty cycles. With regards to the average current stress shown in Fig. 6(c), the proposed converter competes with the one demonstrated by the converter in [18].

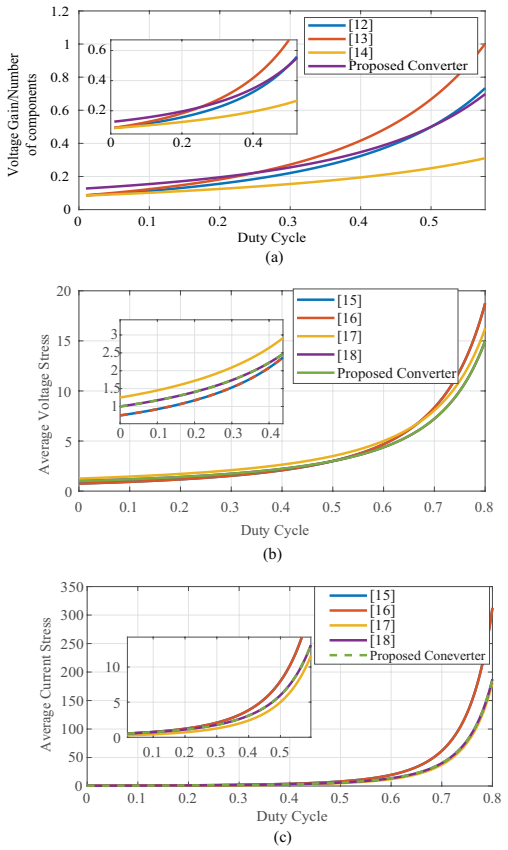

Fig. 6. (a)Voltage gain, (b) Average Voltage stress placed on semiconductor devices, and (c) Average current stress placed on semiconductor devices.

VI. Conclusion

In this paper, a quadratic boost converter is proposed. Compared to other existing topologies, this is the first quadratic boost converter whose switches do not need any extra equipment for gate isolation as the active switches are commonly grounded. At the same time, the polarity of the input and output is the same, causing less EMI radiation. Added to that, the input current drawn from the FC is continuous, which is beneficial for the FC's lifetime and stability. The theoretical analysis and design procedure are thoroughly explained, and a controller is designed to maintain the output voltage constant. Eventually, both the converter and the controlled converter are simulated by Simulink/Matlab to verify the validity of the analysis.

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