FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
DEGREE PROGRAMME IN ELECTRONICS AND COMMUNICATIONS ENGINEERING

PARASITIC EXTRACTION OF A POWER MANAGEMENT INTEGRATED CIRCUIT PCB

Author	Niko Alatalo
Supervisor	Jan Nissinen
Second Examiner	Timo Rahkonen
Technical Advisor	Jari Niemelä

August 2023

Alatalo N. (2023) Parasitic extraction of a power management integrated circuit PCB. University of Oulu, Faculty of Information Technology and Electrical Engineering, Degree Programme in Electronics and Communications Engineering. Master's Thesis, 81 p.

ABSTRACT

In this master's thesis parasitic extraction of a power management integrated circuit was established and evaluated using Ansys Q3D. From PCB the S_{21} parameter was extracted between two nodes from output and input to efficiently show the parasitic properties of the PCB. Extraction was done over frequencies from 100 kHz to 100 MHz. This was done using multiple different settings for the extraction to find out the optimal settings in terms of accuracy and time to solution.

An evaluation module PCB was designed for the power management integrated circuit using Altium. In this design the best practices for PCB layout design were utilized to get the performance as good as possible. Some of the PCB design choices were evaluated with Ansys Q3D to make an informed decision of the better design choice.

A measurement setup was established and validated by using a known component to ensure the setup is working as expected. The PCB was measured without components except the ones needed for the experiment. Measurements were taken with S_{21} shunt-through method with spectrum analyser with built-in network option, external vector signal generator and external pre-amplifier to get more dynamic range.

The output and input were evaluated with and without a capacitor to get a broader understanding of the modelling accuracy. A case with two capacitors was tested. These models were compared with a measurement result to evaluate the accuracy of the tools and methods. It was noticed that with simple geometries the different extraction options do not significantly affect the extraction accuracy. At the same time, the time to solution varies greatly which leads to the use of the simpler extraction settings to save time. When comparing the simulation with measurement the best average error was 3.3 % and the worst 34.3 %. The simulations matched the measurements best when a capacitor was placed and worst with open termination with no components. The model accuracies obtained in this thesis reflect what has been seen in previous studies in terms of frequency range and deviation from measured results.

Key words: Parasitic extraction, power management, printed circuit board, impedance

Alatalo N. (2023) Parasiittisten ominaisuuksien ekstraktointi tehonhallinta piirilevyltä. Oulun yliopisto, tieto- ja sähkötekniikan tiedekunta, elektroniikan ja tietoliikennetekniikan tutkinto-ohjelma. Diplomityö, 81 p.

TIIVISTELMÄ

Tässä diplomityössä parasiittisten ominaisuuksien ekstraktointityövaihe luotiin, sekä sen suorituskyky arvioitiin käyttäen Ansys Q3D ohjelmaa. Piirilevyltä ekstraktoitiin S_{21} parametri kahden solmun väliltä tulo- ja lähtöpuolelta käyttäen 100 kHz – 100 MHz taajuusaluetta. Tällä tavoin saatiin tehokkaasti esitettyä piirilevyn parasiittisten ominaisuuksien muodostama impedanssi. Tämä tehtiin käyttäen useita eri asetuksia, joita on saatavilla ohjelmistossa. Nämä asetukset vaikuttavat eri tavoilla ekstraktoinnin tarkkuuteen. Näitä tuloksia vertailemalla löydettiin tarkkuuden ja simulointiajan suhteen optimaaliset asetukset, joilla tehdä ekstraktointi.

Työtä varten suunniteltiin piirilevy tehonhallinta integroidulle piirille käyttäen Altium ohjelmaa. Tässä suunnittelussa käytettiin hyviä käytänteitä, jotta piirilevyn suorituskyvystä saataisiin mahdollisimman hyvä. Jotkin suunnitteluvalinnoista perustuvat Q3D:llä saatuihin tuloksiin, jotta voitiin valita useista vaihtoehdoista paras.

Mittauksia varten suunniteltiin ja toteutettiin mittausjärjestelmä, jonka toiminta varmennettiin mittaamalla tunnetun komponentin impedanssi ja vertaamalla sitä valmistajan antamaan dataan. Valmistetulta piirilevyltä mitattiin käyttäen vain niitä komponentteja, jotka olivat merkittäviä tutkimukselle. Mittaukset tehtiin käyttäen S_{21} shunt-through menetelmää käyttämällä spektrianalysaattoria, jossa on sisäänrakennettu verkkoanalysointioptio. Tämän kanssa käytettiin ulkoista vektorisignaaligeneraattoria ja ulkoista esivahvistinta, jotta saataisiin enemmän dynaamista aluetta.

Vertailuun valittiin piirin ulos- ja sisääntuloverkot kondensaattorilla ja ilman, jotta saataisiin laajempi käsitys mallinnuksen tarkkuudesta. Myös kahden kondensaattorin tapaus käsiteltiin. Näitä mallinnuksella saatuja tuloksia verrattiin mittaamalla saatuihin tuloksiin. Työssä huomattiin, että tässä sovelluksessa, jossa on yksinkertaisia geometrioita, eri ekstraktointi vaihtoehdot eivät vaikuttaneet tarkkuuteen huomattavasti. Ekstraktointiin kulunut aika vaihteli huomattavasti joidenkin vaihtoehtojen välillä, jonka takia valittiin yksinkertaisempi mallinnustapa, jotta säästettäisiin aikaa. Verrattaessa simuloituja ja mitattuja tuloksia, huomattiin että paras keskiarvoinen virhe oli 3,3 % ja huonoin 34,3 %. Simuloinnit vastasivat mittauksia parhaiten, kun tarkasteltiin tapauksia, joissa oli käytössä yksi kondensaattori ja huonoin, kun käytettiin avointa terminointia. Tässä työssä saadut tulokset vastaavat hyvin aikaisemmissa tutkimuksissa saatuja tuloksia sekä taajuusalueen puolesta, että eron mittauksen ja simuloinnin välillä.

Avainsanat: Parasiittiset ominaisuudet, ekstraktointi, tehonhallinta, piirilevy, impedanssi

TABLE OF CONTENTS

FOREWORD

This master's thesis was done for Texas Instruments in Oulu to establish and study parasitic extraction and how it should be conducted in the most efficient way. Thesis examiners from university of Oulu were Jan Nissinen and Timo Rahkonen. I would like to thank them for guiding me through the thesis process and giving me advice on how to write the thesis.

This thesis was done on an area that has been utilised, but not thoroughly studied, on PMIC PCB design at Texas Instruments. This created problems and many hours were spent on determining how all the different phases should be done both on simulation and measurement sides. This area also being relatively new to me has taught me a lot of new things about PCB layout design, parasitic extraction, and measurements.

From Texas Instruments my supervisor was Jari Niemelä and I got a lot of help from Samuli Piispanen and Jussi Särkkä. I would like to thank them for the weekly meetings and all the extra advice and support they have given me these past six months on Ansys, PCB design, thesis feedback and all the help on the details of the thesis. I would also like to thank Sini Pesonen for helping me with my written English.

Last but certainly not least, I would like to thank my girlfriend for bearing with my days of studying and writing this thesis. Many weekends and holidays were spent working on the thesis one way or another, but she always stood by me even during the not-so-good parts of the process.

Oulu, August 12th, 2023

Niko Alatalo

LIST OF ABBREVIATIONS AND SYMBOLS

3D	3- dimensional
3D-PEEC	3- dimensional partial element equivalent circuit
AC	alternating current
AEDT	Ansys electronics desktop
CG	capacitance and conductance solver in electromagnetic solvers
CPU	central processing unit
DC	direct current
DUT	device under test
ECM	embedded capacitance material
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ESL	equivalent series inductance
EVC	early voltage compensation
EVM	evaluation module
FEM	finite element method
GM	gain margin
GPIB	general purpose interface bus
HF	high frequency
IC	integrated circuit
LC	circuit consisting of inductor and capacitor
LDO	low dropout (regulator)
LF	low frequency
LSF	load sharing facility
LVDS	low voltage differential signalling
MLCC	multilayer ceramic capacitor
MoM	method of moments
MOSFET	metal-oxide-semiconductor field-effect transistor
PC	personal computer
PCB	printed circuit board
PDN	power delivery network
PM	phase margin
PMIC	power management integrated circuit
POL	point of load
RF	radio frequencies
RL	resistance and inductance solver in electromagnetic solvers
RLCG	circuit with resistance, inductance, capacitance, and conductance
SMT	surface-mount technology
SMPS	switching mode power supply
SRF	series resonance frequency
TLM	transmission line model
TTL	transistor-transistor logic
VCCA	positive supply voltage

A	cross-sectional area of a conductor
$\boldsymbol{a}$	waves flowing into a port in S-parameter measurement
A_{ol}	overlapping area of conductors

$\boldsymbol{B}$	magnetic flux density
$\boldsymbol{b}$	waves flowing from a port in S-parameter measurement
C	capacitance
C_0	capacitance between conductors with air as insulator
d	length of a trace
f	frequency
f_{RF}	resonance frequency
$\boldsymbol{H}$	magnetic field intensity
h	separation between conductors
I	current
i	imaginary number
I_1	current in conductor 1
$\boldsymbol{J}$	current density
L	inductance
L_1	inductance of a signal path
L_2	inductance of a return path
L_{Loop}	loop inductance
M_{12}	mutual inductance between traces 1 and 2
M_{21}	mutual inductance between traces 2 and 1
n	number of squares in a trace
Q	charge between conductors
R	resistance
R_{AC}	resistance at AC
R_{DC}	resistance at DC
R_{L}	resistance per length
R_{sq}	sheet resistance
$\boldsymbol{S}$	S-parameter matrix
S_{11}	reflection coefficient
S_{12}	forward transmission coefficient
S_{21}	reverse transmission coefficient
$S_{21,ser}$	S_{21} obtained by series-through measurement
$S_{21,shunt}$	S_{21} obtained by shunt-through measurement
S_{22}	output reflection coefficient
S_1	area of an inductance loop
t	thickness of a trace
V	voltage
w	width of a trace
x	x-axis of a coordinate system
y	y-axis of a coordinate system
$\boldsymbol{Z}$	Z-parameter matrix
z	z-axis of a coordinate system
Z_0	reference impedance
Z_{11}	self-impedance of port 1
Z_{12}	transimpedance from port 2 to port 1
Z_{21}	transimpedance from port 1 to port 2
Z_{22}	self-impedance of port 2
Z_{C}	impedance of capacitor
Z_{DUT}	impedance of a device under test

$Z_{DUT,ser\text{-}thru}$	impedance of DUT obtained by series-through method
$Z_{DUT,shunt\text{-}thru}$	impedance of DUT obtained by shunt-through method
Z_{ind}	impedance of inductor
Z_L	impedance of port two in series-through or shunt-through measurement
Z_S	impedance of port one in series-through or shunt-through measurement

∇	nabla operator
δ	skin depth
δ_{copper}	skin depth of copper
ε_0	permittivity of free space
ε_r	relative dielectric constant
μ	permeability
μ_0	permeability of free space
ρ	bulk resistivity
σ	conductivity
Φ	flux of magnetic field
Φ_2	magnetic flux around conductor 2
ω	angular frequency

1 INTRODUCTION

A PCB (Printed Circuit Board) has a significant effect on the performance of an entire system. This is why the layout designer must know how to design a well performing PCB. Due to the ever-increasing complexity of electronic systems, it can be an overwhelming task to design a PCB by only utilising the key layout design rules. This is why a computer software should be used in the design process to evaluate the performance. Software like Ansys Q3D and Siemens HyperLynx have been developed to help the designer evaluate properties such as signal integrity, power integrity and parasitic properties. Signal integrity and power integrity problems arise from the parasitic properties, and this is why by examining only the parasitic properties of the PCB, the designer can tell if the design needs improvements.

Extracting the parasitic properties is not a simple task to do properly, and the user must know which software to use and how to use it properly for the use case. The user must know the correct extraction frequencies, which properties are extracted, how many cells the equivalent circuit must contain and the accuracy of used mesh. Some software is dedicated to lower frequencies and some to higher frequencies, some are optimized for speed and some for accuracy. The user cannot increase the accuracy blindly because the time to solution increases fast and can reach calculation times up to several days.

Ansys Q3D is a part of Ansys Electronics Desktop software which specialises in fast low frequency parasitic extraction. It reduces the calculation times by not calculating full Maxwells equations but by approximating for example that the magnetic and electric fields do not change over the problem area. From the calculated results an equivalent circuit can be exported which can be used in further simulations.

In this study Ansys Q3D is used to extract parasitic properties of a power management integrated circuit evaluation module PCB, which are then compared with measurement results. From the PCB the chosen points of interest are output and input loops due to their high importance in this kind of system. Inductance in the output loop can make the device unstable and in the input loop it can cause voltage fluctuations due to the switching operation. The comparison between different extraction options is done to evaluate different extraction options and their effect on accuracy and time to solution. Comparing the simulation results with measured values shows the accuracy of the simulations.

Chapter 2 covers the basics of parasitic properties in a PCB and their effects on performance. This includes how inductance causes ground bounce and rail-collapse, capacitance causes cross talk, and resistance causes voltage drop and how it is related to frequency. It also covers how these properties contribute to the impedance profile and how these unwanted effects can be mitigated. Also, brief introduction to signal integrity is given. Chapter 3 focuses on two different extraction programs by Ansys and how they can be utilised. In chapter 4 the designed PCB is introduced and some of the design decisions are explained. Chapter 5 introduces the used simulation and measurement setups and how they were used. Chapter 6 shows the simulated results compared with the measurements after which is the chapter 7 where a broader look is given to this work and the accomplishments of this study. Finally in chapter 8 a summary of the thesis is given.

2 PARASITIC PROPERTIES OF PRINTED CIRCUIT BOARD

In modern systems design designer does not only need to worry about the qualities of all the components but also take the printed circuit board into consideration as it was a component in the system. The PCB can be thought to consist of resistance, capacitance, and inductance. Good power plane design can be the difference between device achieving and not achieving the specification [1].

The only reason for signal and power integrity problems are the three basic properties of any conductor which are resistance, capacitance, and inductance. If a conductor was ideal, none of these signal and power integrity problems would exist. Ability to optimize PCB design comes down to understanding these electrical properties and their effects, as well as how to mitigate them. [2]

If a sensitive chip and its accompanying system is designed considering only signal integrity, the signals themselves might be clean. However, when there are problems in for example the power rail, this will affect the signal one way or another. Also, if there is a disturbance in the reference voltage, the chip might get false readings. [2]

2.1 Resistance in conductors

Resistance is the conductor's ability to resist the flow of current at DC (Direct Current) as well as to dissipate excess energy as heat. Resistance depends on the physical geometry of the trace as well as its material property named bulk resistivity. Bulk resistivity is the materials intrinsic property to resist current flow, which means it is only dependent on the material itself and not on the amount of it. Copper is used in conductors, since it has low bulk resistivity of 1.58 μΩ·cm. [2]

The resistance of a conductor can be manipulated by changing its geometry. Current flows more freely in a wide and thick conductor, hence resistance can be defined by resistance per length and sheet resistance if the conductor's cross section is uniform in the trace. Both are dependent on the bulk resistivity of the material used. Resistance per length R_{L} is directly proportional to the length of the trace by

$$R_{\mathrm{L}} = \frac{R}{d} = \frac{\rho}{A}, \tag{1}$$

where R is resistance, d is conductor length, ρ is bulk resistivity and A is the cross-section area of the trace. [2]

Sheet resistance is determined by the thickness of the conductor and the material used. Resistance is directly proportional to the length of the conductor and inversely proportional to the width of the conductor. If both dimensions are changed the same amount, the resistance will not change. Thus, every square of the same conductor having uniform cross section will have the same resistance R_{sq} of

$$R_{\mathrm{sq}} = \frac{\rho}{t}, \tag{2}$$

where *t* is the thickness of the trace. In the case of sheet resistance, it is assumed that the current flows uniformly from one side to the opposite side of the trace. For typical thickness of 1-ounce copper sheet, or about 35 microns, the sheet resistance is 0.5 mΩ per square. [2]

Every trace can be made of squares and since every square in a uniform trace have the same resistance, the resistance at DC R_{DC}, where the entire trace has uniform cross-sectional area, can be given by

$$R_{\mathrm{DC}} = \frac{\rho}{t} \cdot \frac{d}{w} = R_{\mathrm{sq}} \cdot n, \tag{3}$$

where *w* is width of the trace and *n* is number of squares in the trace. From equation (3) it can be concluded that if the length and width of a trace are the same, the resistance of the trace is the same as sheet resistance. Thus, the only parameters affecting the resistance are the bulk resistivity and thickness of the trace. If the length is twice as large as the width, the resistance of the trace is two times the sheet resistance. [2]

At higher frequencies the current starts to flow closer to the surface of the conductor thus not utilizing the whole cross-sectional area of the conductor [3]. This is called the skin effect. Because of this effect, the resistance of a conductor is frequency dependent [3]. Skin depth is the maximum depth at which the current flows and therefore determines the cross-sectional area which is used by the current. Skin depth δ can be approximated with

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}, \tag{4}$$

where ω is angular frequency, μ is the conductor's permeability and σ is the conductor's conductivity [3]. With the skin depth the AC (Alternating Current) resistance R_{AC} for a rectangular conductor can be calculated by using equation

$$R_{\mathrm{AC}} = \frac{\rho}{2(w + t)\delta} \tag{5}$$

where the skin depth for copper can be calculated by using equation

$$\delta_{\mathrm{copper}} = \frac{66 \cdot 10^{-6}}{\sqrt{f}}, \tag{6}$$

where *f* is the frequency in megahertz [4].

These principles can be used to estimate and optimize the resistance of the trace. It must be taken into consideration that these equations assume that the current is distributed equally in the trace. If the source or sink point of the trace is narrower than the trace, the current will not flow uniformly and the resistance the current sees is higher than expected.

2.2 Capacitance of a trace

Capacitance is a measure of how efficiently two conductors can store charge between them at the cost of voltage [5]. Capacitance is only dependent on the geometric attributes of the two conductors and the dielectric material between them [2]. Ideally capacitance does not change

with extrinsic properties such as voltage [2]. The Higher the charge stored for fixed voltage, the higher the capacitance. Thus, capacitance C can be expressed as

$$C = \frac{Q}{V}, \tag{7}$$

where Q is the stored charge and V is voltage between the conductors. Equation (7) shows that if a lower voltage is applied to a capacitor its capacitance does not change but the charge stored decreases [2]. The capacitance of a capacitor ideally cannot be changed by applying different voltage across it [2]. The exception to voltage dependency are high dielectric constant capacitors which are highly susceptible to the so-called DC bias effect [6]. With these capacitors having dielectric constant over 200, their capacitance decreases with higher DC bias [6]. Since the commonly used FR4 in PCBs has dielectric constant of around four, it is not susceptible to this effect in a meaningful manner. Capacitance can also be expressed with the overlapping area of the plates, separation between plates and dielectric constant by

$$C = \varepsilon_0 \varepsilon_\mathrm{r} \frac{A_\mathrm{ol}}{h}, \tag{8}$$

where ε_0 is the permittivity of free space, ε_r is the permittivity of medium between plates, A_ol is the overlapping area of the conductors and h is separation between the plates [2]. This is more useful when optimizing PCB layout.

Dielectric constant is intrinsic property of the insulator in a capacitor. Relative dielectric constant ε_r is defined as the relation between capacitance with some dielectric and capacitance with air as the dielectric between the plates with

$$\varepsilon_r = \frac{C}{C_0}, \tag{9}$$

where C_0 is capacitance when the insulator between two plates is air. The dielectric constant is a property which tells how well insulating material holds an electric field. The dielectric constant can change up to 10 % with frequency. Some change can also be seen with change in temperature as with water it can change from about 90 to about 55 when temperature rises from 20 degrees to 100 degrees [7]. For FR4 the effect of temperature is minor [8]. [2]

Effective dielectric constant is the dielectric constant seen by the electric fields. If a conductor is placed on the top side of a printed circuit board, some of the electric field lines will be surrounded by the surrounding medium and some by the PCB dielectric material. This causes the dielectric constant in this capacitor to be somewhere between the dielectric constant of the surrounding material and the dielectric material. This leads to two traces having different capacitance between them depending on if one of the traces is in the inside layers of a multilayer PCB or at the surface, assuming the other trace stays in the same layer in both situations and the distance between the traces stays the same. [2]

Capacitance between two traces can cause cross talk which can be divided into common impedance and electromagnetic field coupling. Common impedance coupling is the cause of using a common return path for different signals. Electromagnetic field coupling occurs mainly at high frequencies and can be divided into capacitive and inductive coupling [9]. Two traces close together will have some capacitance between them but is mainly of concern when they

are on different layers and overlap. The capacitance between two traces can be calculated by equation (8). The closer they are together and the greater the overlap is, the higher capacitance between them. Capacitive coupling is more likely to occur at high frequencies due to impedance of a capacitor Z_C being lower according to

$$Z_C = \frac{1}{i\omega C}, \tag{10}$$

where i is the imaginary number, ω is the angular frequency and C is the capacitance. An example of switching noise is shown in Figure 1. [2]

Figure 1. Switching noise in quiet line coupling from switching line [2].

Eliminating cross talk is an impossible task but with careful design it can be mitigated. These design considerations include reducing the length of signal traces and keeping them as wide apart as possible, by reducing dielectric thickness between signal layer and reference plane and inserting a ground trace between signal lines. [9]

Capacitance between a switching node and a sensitive feedback trace can cause unwanted effects. In SMPS (Switching Mode Power Supply) circuit capacitance between the switching node and the input of the gate driver can cause false turn-off triggering of the power transistor [10]. Figure 2 shows the false turn off behaviour due to coupling between the output switching node and the gate driver input. This happens because a high enough voltage spike is coupled to gate driver input which causes the low side driver output to go low. Thus, the gate-source voltage goes low and turns off the low side power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) device as is shown in Figure 2 measurement type B and measurement type A would be the correct behaviour. This event is called a false turn-off event. This capacitance can be lowered for example by changing the layer stack up of the PCB by having the switching node of the transistor farther away from the control signal trace [10]. Capacitive coupling between a switching node and a feedback line in a power management integrated circuit weakens the performance due to false readings at the feedback input.

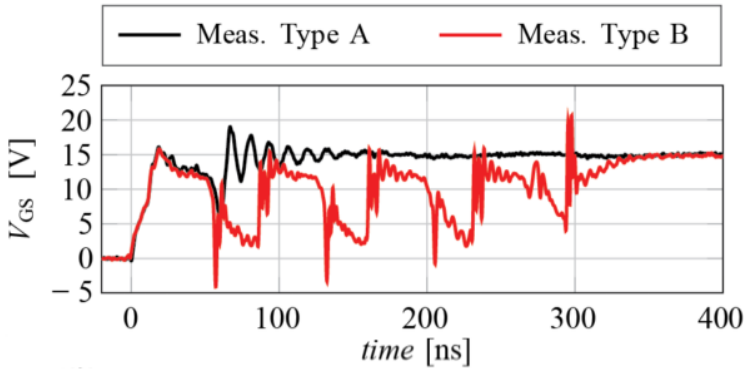


Figure 2. False turn-off triggering of power transistor due to parasitic capacitance [10].

Parasitic capacitance of a PCB can also be used to make capacitors for high frequency signals. The use of ECM (Embedded Capacitance Material) has been studied for use in power supplies and it was shown that capacitance of up to 10 nF/cm^2 can be created. According to equation (8) the capacitance is directly proportional to the dielectric constant of the dielectric material. FR4 has a dielectric constant of four and in the study the highest used dielectric constant was 2600 for ferroelectric Y5V. MC12TM, which was of interest in this study, has a dielectric constant of 10. These have capacitances per square centimetre of 6 pF and 9.5 nF respectively. The use case for ECM is for example filtering EMI (Electromagnetic Interference) or lowering the impedance of the PDN (Power Delivery Network) [11]. When comparing the use of FR4 and MC12TM ECM between the power and ground planes for minimizing the PDN impedance, it decreased the peak impedance from about 3 Ω to approximately 0.5 Ω in the frequency range from 300 MHz to 700 MHz. Also, the overall impedance over 300 MHz was lowered significantly [11]. This also reduced the simultaneous switching noise and jitter by 38.5 % and 53.9 % respectively [11]. The use of ECM can also lead to low profile converters, or the space saved can be used to populate other components. From the cost point of view embedded capacitance is no better than typical surface mount capacitors. [12]

2.3 Inductance in conductors

Inductance is conductor's efficiency to create magnetic field lines per amount of current. It is an intrinsic property of a conductor and is only affected by the geometry of the conductor. In simple terms inductance L can be defined as the number of magnetic field lines generated by one amp of current flowing in the conductor as

$$L = \frac{\Phi}{I}, \tag{11}$$

where Φ is the flux of magnetic field lines around the conductor in Webers and I is the current flowing through the conductor. While the current does not change the inductance of the conductor it does change the amount of field line rings around it and the ratio of those is the inductance. [5]

A current flowing through a conductor creates magnetic field lines around it which appear to have a direction of rotation determined by the right-hand rule. The number of magnetic field lines, also called the magnetic flux, can be counted at any point around the conductor as shown in Figure 3. [5]

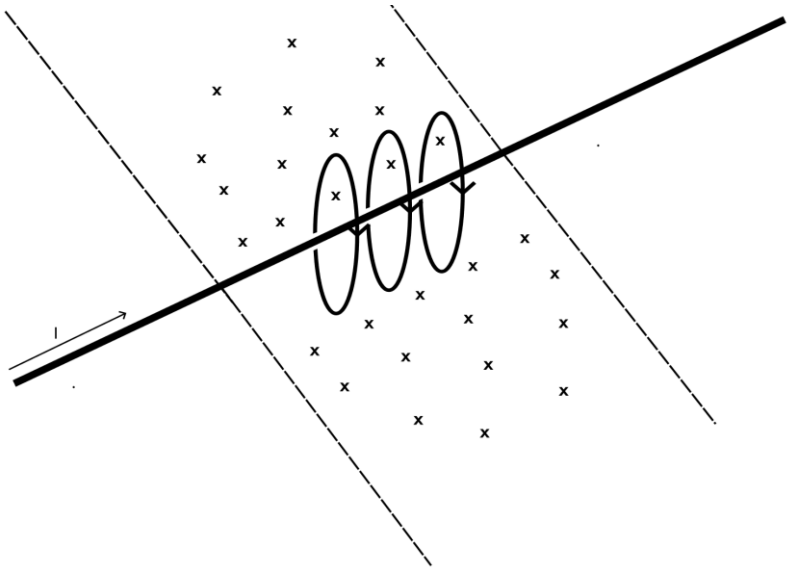


Figure 3. Magnetic flux of a conductor.

The Denser the magnetic field lines are, the higher the magnetic flux density and the higher the magnetic flux around the conductor. Magnetic flux density $\boldsymbol{B}$ can be written as

$$\boldsymbol{B} = \mu_0 \boldsymbol{H}, \tag{12}$$

where μ_0 is the permeability of free space and $\boldsymbol{H}$ is the density of magnetic field as a vector. Magnetic field density is measured in amperes per meter. The magnetic field density $\boldsymbol{H}$ is related to the current density $\boldsymbol{J}$ by

$$\boldsymbol{J} = \nabla \times \boldsymbol{H}, \tag{13}$$

where the ∇-operator is given by

$$\nabla = \left(\frac{\partial}{\partial x}, \frac{\partial}{\partial y}, \frac{\partial}{\partial z}\right), \tag{14}$$

where x, y and z are the axes of the system. Magnetic flux Φ can then be expressed as the line integral of the magnetic flux density by

$$\Phi = \int_s \boldsymbol{B} \cdot dS_l, \tag{15}$$

where $\boldsymbol{B}$ is the magnetic field intensity vector and S_l is the area that the loop surrounds. [13]

Inductance can be divided into partial and loop inductance. Loop inductance is what is always measured since measuring inductance must always include a closed loop where current can flow. Loop inductance consists of the self-inductance of that loop's sections and the mutual inductances between those sections. [5]

Partial inductance is defined like any other inductance as the efficiency to create magnetic field lines per one amp of current [5]. Loop inductance can be fully defined by only using the partial inductances of the loop's sections. Instead of focusing on the whole loop at once, which can be problematic for modelling the circuit, the magnetic field line rings produced by the current flowing in an isolated section are evaluated [14].

The partial inductances in a loop have self- and mutual inductance. Self-inductance is the inductance determined by field lines created by the current flowing in that specific section. To specify self-inductance even further, it can be divided into partial self-inductance and loop self-inductance. Partial self-inductance is the self-inductance in a section of a loop and loop self-inductance is the self-inductance of the entire current loop. [5]

Mutual inductance is the part of the inductance which is created by another section in that current loop [5]. Mutual inductance M_{12} is therefore defined as the number of field lines around a conductor created by one amp of current in another conductor by

$$M_{12} = \frac{\Phi_2}{I_1}, \tag{16}$$

where Φ_2 is the magnetic flux around the second conductor and I_1 is current through the first conductor [14]. Self- and mutual inductance is shown in Figure 4 by the black and red lines, respectively. The mutual inductance of two conductors is the same either way, which can be written as

$$M_{12} = M_{21}. \tag{17}$$

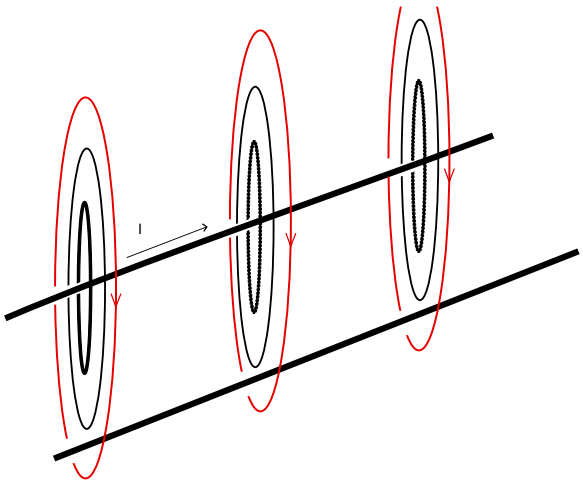


Figure 4. Self- and mutual inductance.

As with self-inductance, also mutual inductance can be divided into partial mutual inductance and loop mutual inductance. These describe how either sections of a loop or separate loops interact with each other. [5]

Mutual inductance is affected by the length of the two conductors and the distance between those conductors. Mutual inductance is directly proportional to the length of the conductors and the separation between them, so the closer the conductors are, the higher mutual inductance is. [5]

Loop inductance is determined by self-inductances and mutual inductances in that loop [5]. In Figure 4, if there was a current flowing in the lower conductor from right to left, the magnetic field lines would be in the opposite direction than the shown lines. This is often the situation with signal line and its return path. Because the field lines oppose each other, they are subtracted. We get the definition for loop inductance L_{Loop} as

$$L_{\mathrm{Loop}} = L_1 + L_2 - 2M_{12}, \tag{18}$$

where L_1 is the inductance of the signal path, L_2 is the inductance of the return path and M_{12} is the mutual inductance of these conductors. Mutual inductance is multiplied by two because it appears twice in the loop, first from conductor one to conductor two and then from conductor two to conductor one. In terms of PCB design, this means that the signal and return paths should be placed as close to each other as possible to get high mutual inductance and thus low loop inductance. [5]

The impedance of an inductor Z_{L} increases with frequency according to

$$Z_{ind} = i\omega L, \tag{19}$$

where i is the imaginary number, ω is angular frequency and L is inductance. According to equation (19), conductors attenuate higher frequency signals more than low frequency signals thus lowering the rise time of a signal. If the rise time exceeds the period of a bit, false triggering will occur. When comparing to signals, the length of the traces carrying these signals should be matched to avoid any skew between them. [2]

Rail collapse is another effect that arises from equation (19). Rail collapse occurs when the load increases rapidly and the transient interacts with the inductance in the power rail causing the voltage to drop. This voltage drop V can be calculated by

$$V = L\frac{dI}{dt}, \tag{20}$$

where dI/dt is the current change I in time t [2]. This is a problem in modern designs since the trend has been to lower supply voltage and to increase the current consumption with faster switching meaning the load transients are faster. This causes even the smallest of inductance to be a problem because higher currents are drawn with faster transient, but the voltage cannot drop much since even a small rail collapse is a big percentage of the supply voltage. Rail collapse can be prevented by lowering the inductance in the power rail, placing power and ground plane as close together as possible and as close to the surface as possible. Also using low inductance capacitors help. [2]

The effect of rail collapse can also be mitigated by careful design of the feedback for example of a PMIC (Power Management Integrated Circuit) or by increasing the supply voltage for the duration of the initial current transient. The feedback can be single ended or differential and both have their strengths. The strength of single ended feedback is the ability to maintain more solid power or ground plane where the negative feedback line would be routed. EVC (Early Voltage Compensation) can be used to anticipate the incoming current draw from the PMIC. This might be needed since the PMIC cannot increase the power output fast enough and the voltage will drop. This can be done by the microcontroller informing the PMIC of the incoming load increase so that the PMIC can increase the voltage for the initial current draw. The voltage

is adjusted back to the original value when the current transient has passed. By doing this when the rail collapses, it does not collapse under the specification but closer to the actual rail voltage. This can decrease the voltage drop at the load side. [15]

2.4 Impedance profile

Impedance profile is the impedance of a trace over some frequency span. Impedance of a trace can be depicted as RLCG (Resistance, Inductance, Capacitance, Conductance) circuit which has series resistance and inductance and parallel capacitance and conductance. [5]

Since impedance of inductor gets larger with frequency and impedance of capacitor gets smaller, there is a resonance frequency where they are equal. The resonant frequency f_{RF} is given by

$$f_{RF} = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}, \tag{21}$$

where L is inductance and C is capacitance. This frequency is the same for both the series and parallel LC (Inductance, Capacitance) circuit [2]. Figure 5 shows the series and parallel resonance for 1 nF capacitor and 1 nH inductor and their impedances in series configuration. It can be seen the parallel and series resonance frequencies are the same if the values are the same.

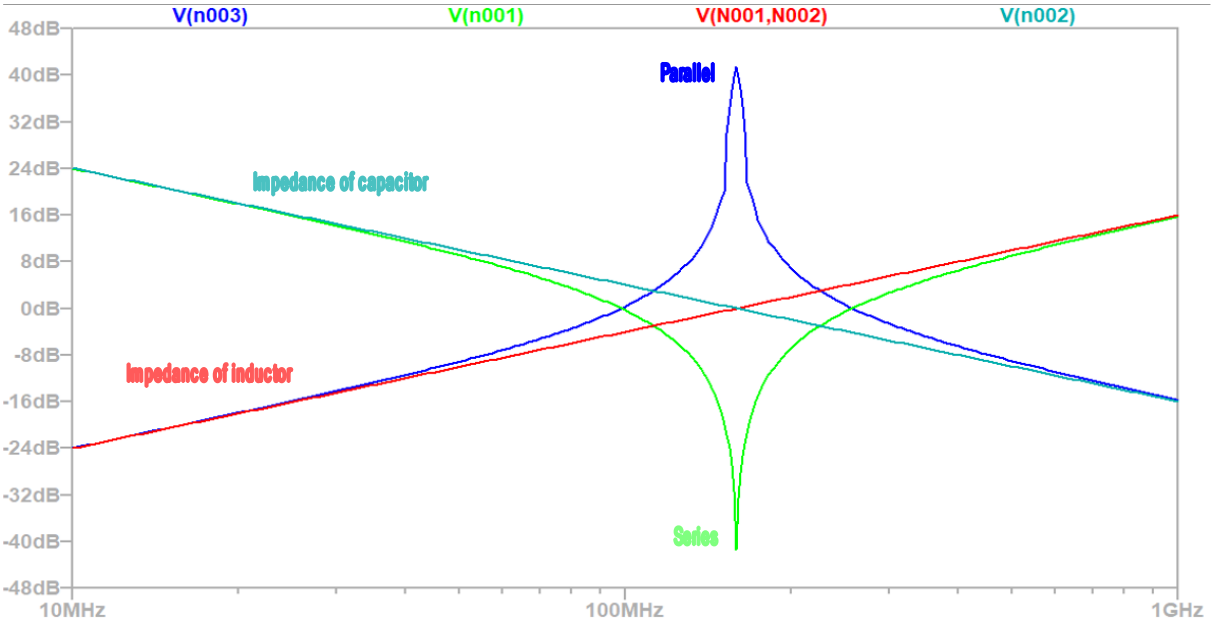


Figure 5. Series and parallel resonance spike of 1 nH inductor and 1 nF capacitor.

Signal plane and its return plane can interact as both series and parallel LC circuits depending on the entry and exit of the current. If the current is injected in a section with high inductance, the current interacts with inductance first and most of the capacitance is covered at the edge of plane pair. This acts as series LC circuit. If the current is injected at low inductance and high capacitance point of the plane pair and the current exits to high inductance point the structure acts as parallel LC circuit [5]. Impedance profile is formed by these interactions. As an example, an impedance profile of 1-inch-long transmission line with open termination is shown in Figure 6.

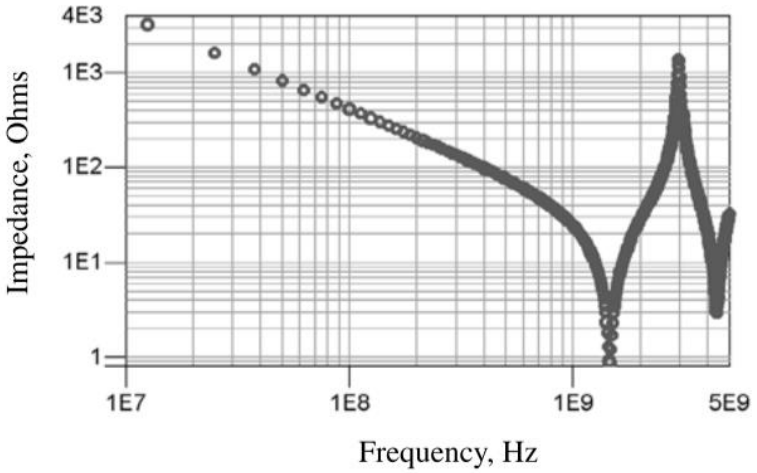


Figure 6. Measured impedance profile of 1-inch-long transmission line with open termination [2].

The understanding of impedance profile is important for designing great performing PCBs and thus better products. It should be understood what components the impedance includes and how they can be manipulated through different design choices.

2.5 Signal integrity

Signal integrity considers many different effects and new ones are found all the time. Knowing all of these would be almost an impossible task. These problems can be divided into four categories which simplifies the problem. Understanding all four categories allows us to deal with any signal integrity problem without having to memorize all singular problems. These categories are signal quality of a net, cross talk between multiple nets, rail collapse in power delivery network, and electromagnetic interference from the entire system.[2]

A net consists of all of the copper that is in direct contact with each other and the signal return path. Any impedance discontinuities in this net will distort a signal, and with high enough distortion false triggering may occur. These discontinuities include for example trace cross section changes, layer change through via and connectors. The most common impedance discontinuity is at the end of the net when impedance changes from the impedance of the net to open circuit or the load impedance. When rise time of the signal decreases, or the frequency increases, the distortions caused by impedance discontinuities increase since the impedance of the inductor increases with frequency. Reflections cause under and overshoot and ringing and these can cause damage, reduce noise margin, and increase settling time which affects stability [9]. [2]

EMI is generated from all three types of noise mentioned earlier, so every design aspect lowering noise will lower EMI. Although, even if every other noise has been pushed to low enough levels, EMI can still be a problem causing the design not to pass regulations. For radiated electromagnetic interference to occur, it needs a source, a radiator, and a receiver. Often this can be high-speed data line near PCB border where there is a connector to another device. This type of EMI can be decreased using a ferrite choke around cables leaving the printed circuit board. Since modern telecommunication bands are in the gigahertz territory, the high-speed signals that reach these frequencies are a big problem. EMI is a bigger problem when higher frequencies are reached in new designs. [2]

Eliminating EMI is difficult when the design is already finalized, and it does not pass regulations. The only solutions are to try some workaround to reduce EMI or to redesign and test the whole device. Neither of these solutions is cheap, fast, or easy, so the device should be designed from the beginning with EMI in mind. A bypass capacitor can be used at DC input to reduce noise from the power line and a transient-voltage-suppression diode can be used to suppress transients in the power line. Power cables should be shielded twisted pairs. EMI filters can be enclosed in metallic enclosures to minimize radiating EMI and LC filters can be used to reduce switching noise. [16]

Electromagnetic interference, common-mode voltage bounce and crosstalk can be improved with LVDS (Low Voltage Differential Signalling). LVDS uses low-voltage swing of around 300 mV to minimize power dissipation [17]. Differential transmission mode helps with common-mode voltage bounce and crosstalk since if the same disturbance happens in both lines it is cancelled in the differential receiver [17]. Current mode transmission reduces noise in the communication [17]. LVDS has become one of the best solutions for chip-to-chip transmission and controlling optical communication [18], [19].

2.6 PCB layout guidelines

These principles shown below can be used in PCB layout design using only a few simple rules. There are more guidelines and good practices but listing them all would be overwhelming. However, the following rules are a great starting point for layout design.

- Use as short as possible trace lengths to minimize inductance and resistance [2].
- Use wide traces to get larger cross-sectional area to minimize inductance and resistance [2].
- Keep distance between signal and return traces as small as possible to reduce loop inductance [2].
- Traces carrying current in the same direction should be kept as far away from each other as possible to minimize loop inductance [5].
- Capacitive coupling can be minimized by keeping traces as far from each other as possible [2].
- Power plane capacitance can be increased by bringing power and ground planes closer together. Effect of capacitance is negligible compared to inductance [5].

PCB design can be further improved by some more advanced design techniques such as making the PCB layer stack up symmetrical around the core, routing signals orthogonally on adjacent layers and interleaving the signal and return paths.

The impedance profile of a PCB can be influenced by considering the layer stack up order [20]. One scheme that can improve the performance of the PCB is making the stack up symmetrical respective to the core. An example of this can be seen in Table 1 where the core would be between SIG1 and SIG2 layers. This ensures that components on top and bottom layer can have similar current loops and thus similar loop inductances [21]. In this design the ground layers 2 and 5 are close to the surface which reduces inductance from vias. Also, by bringing power and ground layers closer together, the loop inductance can be minimized.

Table 1. Symmetric layer stack up in PCB layout

Layer number	Domain
1 (Top Layer)	POWER
2	GND
3	SIG1
4	SIG2
5	GND
6 (Bottom)	POWER

Interleaved signal and return paths are another more advanced design technique to improve the loop inductance. A cross section of a PCB design with interleaved signal and return traces is shown in Figure 7 where layers one and three are for signal and layers two and four are return paths. The inductance L in the schematic is the parasitic inductance of the PCB. Interleaving these paths reduce the inductance by having more volume for the current to flow in, but more importantly by reducing the magnetic flux density. In a normal design with signal on one layer and return path on the next, the magnetic flux density is high in this smaller area. By using four layers instead of two and interleaving the traces as shown in Figure 7, the flux density is much lower which reduces inductance according to

$$L = \oint \boldsymbol{H} \cdot \boldsymbol{B}\, dV / I^2, \tag{22}$$

where $\boldsymbol{H}$ is the magnetic field intensity and $\boldsymbol{B}$ the magnetic flux density. [22]

This method of interleaving the signal and return paths reduces the inductance by up to 35 %. This also provides a significant reduction in sensitivity to the geometry of the loop with 13 % and 36 % reduction in total PCB height and distance between the devices, respectively. A 34 % improvement in overshoot was achieved, though it should be mentioned that the original overshoot was already only 3.2 %. [22]

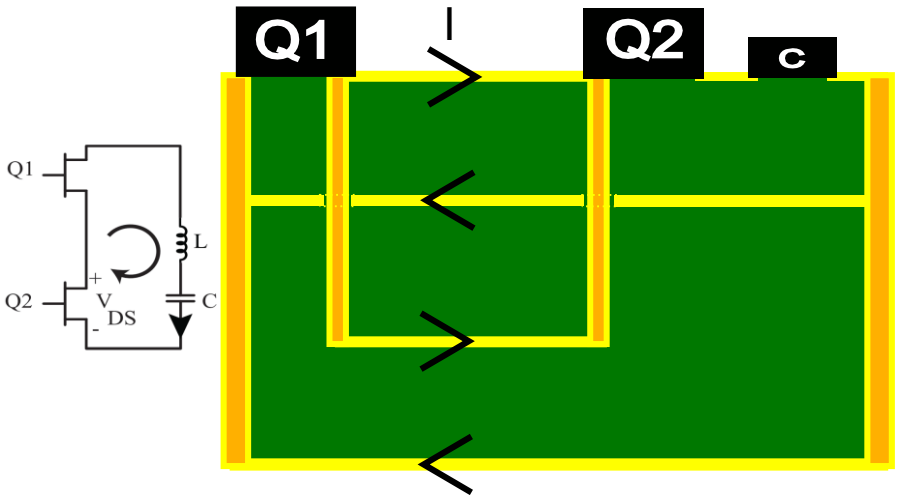


Figure 7. Cross section of interleaved signal and return paths redrawn from [22]. Inductance L in schematic is the parasitic inductance of the PCB.

Localized reference planes can be used to improve EMC (Electromagnetic Compatibility). Localized plane is a reference plane, usually ground, used under a high frequency and thus high RF (Radio Frequency) energy emitting components such as oscillators and buffers. This plane is connected to the main reference plane by at least two vias. If ground reference is used for the localized plane, it is recommended to place the component near ground stitching so that it is surrounded by stitching vias. [23]

The main reason for using localized planes is the RF emissions created by frequency generating components due to common mode currents from the circuitry. Metal chassis of the component receives some RF components created by the circuitry and if it is connected to the ground pin of the device, the pin must conduct both DC and RF components. Due to the high inductance of the ground pin and bonding wire, the RF component might be excessive for this pin to conduct. RF emissions can occur if there is no localized reference plane, and the nearest reference plane is far away. The localized reference plane captures some of the emissions thus lowering EMI. [23]

Using SMT (Surface-Mount Technology) packages is worse for EMC since they are usually made of plastic and thus do not capture any RF signals. This way the RF currents will radiate into free space and possibly to close by components or conductors. This is why the use of localized plane is important for SMT devices with plastic enclosures. [23]

3 TOOLS FOR PARASITIC EXTRACTION

There are commercial tools available for extracting parasitic properties of a printed circuit board in two- and three-dimensional geometries. Although parasitic properties can be estimated by hand with simple equations, the higher accuracy of these 3D (3- Dimensional) field solvers make them a valuable tool and for even moderately complex designs mandatory to get reasonable results [5]. 3D field solvers utilize Maxwell's equations and boundary conditions to calculate the results which can be exported for example as S-parameters or RLCG circuit which can further be used in circuit simulation [5].

These field solvers can be divided into full-wave and quasi-static field solvers. Quasi-static solvers like Ansys Q3D use quasi-static approximation which assumes that the phase of the fields does not vary over the problem area. This approximation can further be classified into electro-quasi-static and magneto-quasi-static [24] which include capacitive but not inductive effects and inductive but not capacitive effects, respectively [25]. The condition for a valid quasi-static condition is that the size of the problem area is much smaller than the smallest wavelength [26]. This approximation reduces the complexity of Maxwell's equations. When using full-wave solver like Ansys HFSS there are no restrictions to the problem but the time to solution increases. [5]

3.1 S-parameters and RLCG model

The parasitic model can be constructed using scattering parameters, also called S-parameters, or lumped model. S-parameters are widely used with high frequency signals since it is easier to depict a circuit in terms of waves rather than voltages or currents. For practical reasons a port model is used which has signal and its return path in each port rather than modelling with every node independently. This means that a model consisting of 2n nodes is modelled with a n port model. A 2-port model for shunt-through and series-through setup is shown in Figure 8. [27]

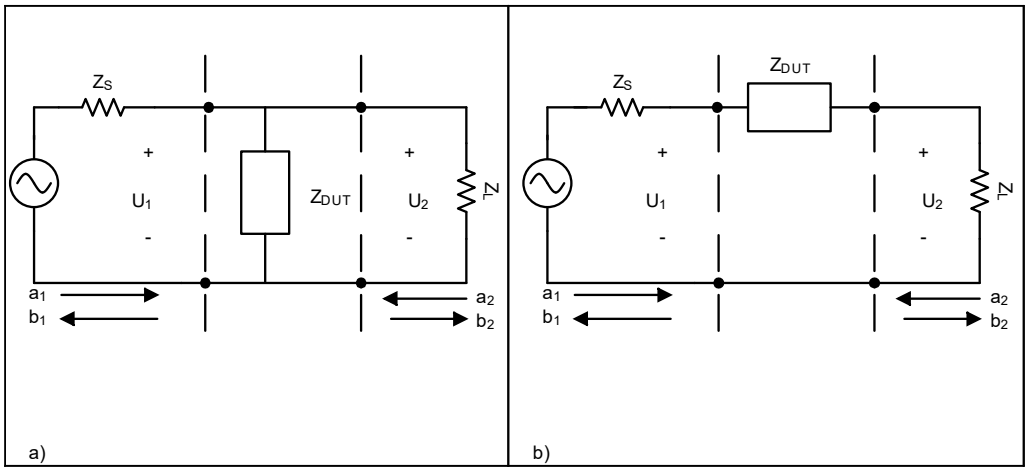


Figure 8. a) Shunt-through and b) series-through methods for determining S-parameters.

The waves flowing into the port are marked by vector a, and waves flowing from the port are marked by vector b. Now the relation between a and b can be written with S-parameters as

$$\boldsymbol{b} = \boldsymbol{S}\boldsymbol{a}, \tag{23}$$

where $\boldsymbol{b}$ is the vector containing waves coming from the port, $\boldsymbol{a}$ is the vector containing waves going into the port and $\boldsymbol{S}$ is the S-parameter matrix. The S-parameter matrix $\boldsymbol{S}$ for a two-port system is

$$\boldsymbol{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}, \tag{24}$$

where S_{11} is the input reflection coefficient when $a_2 = 0$, S_{21} the forward transmission coefficient from port one to port two, S_{12} the reverse transmission coefficient from port two to port one and S_{22} the output reflection coefficient. [27]

The impedances of this system can be defined by the impedance matrix $\boldsymbol{Z}$ consisting of Z-parameters which relates voltages to currents as

$$\boldsymbol{Z} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}, \tag{25}$$

where Z_{11} and Z_{22} are the self-impedances of the ports one and two, respectively. Z_{12} and Z_{21} are the transimpedances which define the voltage generated in one port when current is only applied in some other port. [5]

S-parameters and Z-parameters are related by

$$\boldsymbol{S} = \begin{bmatrix} \dfrac{(Z_{11} - Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} & \dfrac{2Z_{12}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} \\ \dfrac{2Z_{21}Z_0}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} & \dfrac{(Z_{11} + Z_0)(Z_{22} - Z_0) - Z_{12}Z_{21}}{(Z_{11} + Z_0)(Z_{22} + Z_0) - Z_{12}Z_{21}} \end{bmatrix}, \tag{26}$$

where Z_0 is the reference impedance which usually is the characteristic impedance of the line. [28]

Both shunt-through method and series-through method have their advantages in obtaining impedance of the DUT (Device Under Test). Series-through method is good for capturing high impedance values with the minimum impedance being about 30 Ω. This is due to the equation of impedance as the function of S21, when measuring with series-through method which is

$$Z_{\mathrm{DUT,ser-thru}} = \frac{2Z_{\mathrm{L}}}{S_{21,\mathrm{ser}}} - Z_S - Z_L, \tag{27}$$

where Z_{S} is the impedance of port one, Z_{L} is the impedance of port two and $S_{21,\,\mathrm{ser}}$ is obtained by the series-through method. These can be seen in Figure 8 b). In equation (27) $S_{21,\,\mathrm{ser}}$ is given by

$$S_{21,\mathrm{ser}} = \frac{2Z_{\mathrm{L}}}{Z_{\mathrm{L}} + Z_{\mathrm{S}} + Z_{\mathrm{DUT}}}, \tag{28}$$

where Z_{DUT} is given by equation (27). The equation (28) shows that when Z_{DUT} goes too low, the term $Z_{\mathrm{L}} + Z_{\mathrm{S}}$ starts to dominate the denominator. From this it follows that it is harder to differentiate the values of $S_{21,\,\mathrm{ser}}$ from each other. When Z_{DUT} approaches zero, given that $Z_{\mathrm{L}} = Z_{\mathrm{S}}$ which is usually the case, $S_{21,\,\mathrm{ser}}$ approaches one. [29]

Shunt-through method is good for low impedances and thus for PDN impedance measurements. The upper limit for impedance is about 30 Ω. Z_{DUT} as a function of S_{21} in this case is given by

$$Z_{\mathrm{DUT,shunt-thru}} = \frac{-S_{21}Z_{\mathrm{S}}Z_{\mathrm{L}}}{S_{21}Z_{\mathrm{S}} + S_{21}Z_{\mathrm{L}} - 2Z_{\mathrm{L}}}, \tag{29}$$

where S_{21} is obtained by the shunt-through method and is given by

$$S_{21,\mathrm{shunt}} = \frac{\frac{2Z_{\mathrm{L}}Z_{\mathrm{DUT}}}{Z_{\mathrm{L}} + Z_{\mathrm{DUT}}}}{Z_{\mathrm{S}} + \frac{Z_{\mathrm{L}}Z_{\mathrm{DUT}}}{Z_{\mathrm{L}} + Z_{\mathrm{DUT}}}}, \tag{30}$$

where Z_{DUT} is given by equation (29). If Z_{DUT} goes too high the S_{21} approaches one, therefore with higher impedances it is difficult to differentiate the values from each other. This is the opposite behaviour when compared to the series-through method. [29]

PCB properties can be modelled also by RLCG model which is a lumped model where R is the resistance of the trace, L is the inductance of the trace, C is the capacitance between signal and reference plane and G is the conductance between signal and reference plane as shown in Figure 9 [30]. These components are per unit length so multiple sections may be needed to model the whole trace [30]. Lumped models are valid only if the physical dimensions of the circuit are much smaller than the smallest wavelength. [14]

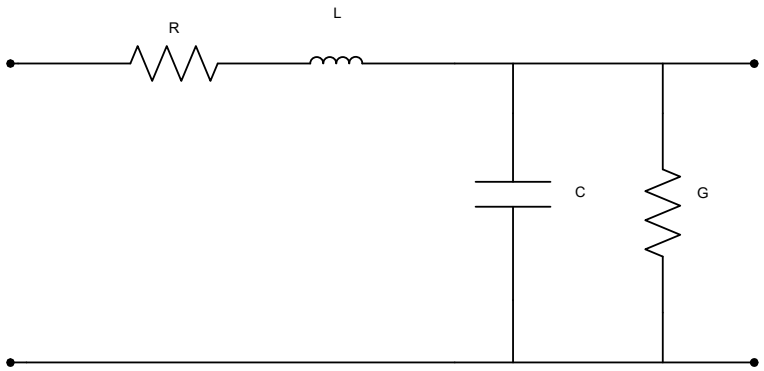


Figure 9. RLCG model.

3.2 Ansys HFSS and Q3D

Two widely used field solvers are HFSS and Q3D by Ansys. The major difference between the two is that HFSS uses full-wave calculations and Q3D uses quasi-static approximations. Since full-wave simulation does not have size limits for the problem area, HFSS is used to calculate properties for structures used in high frequency signalling [31]. Q3D can be used to calculate properties of structures carrying lower frequency signals [31].

3.2.1 HFSS and Q3D differences

There are three common ways to model parasitic effects; FEM (Finite Element Method), 3D-PEEC (3- Dimensional Partial Element Equivalent Circuit) method and RLCG equivalent

circuit method. From these the 3D-PEEC and RLCG methods are a form of equivalent circuit modelling which employ the PEEC method although they offer different advantages. [32]

FEM usually does not use any approximations on the Maxwell's equations and uses a mesh created from the 3D model, thus very accurate broadband parasitic models can be extracted using solvers built on this method. It is challenging to model the HF (High Frequency) and LF (Low Frequency) components with the same accuracy and thus FEM based solvers usually focus more only on one of these. In FEM-based modelling a boundary condition must be used to calculate the electromagnetic effects. In addition, in solvers utilizing FEM only closed current paths can be defined as in solvers using the PEEC method non-closed current paths can be defined by the placement of ports [31]. [32]

PEEC-based solvers' biggest advantage is being usually significantly faster than FEM-based solvers while still being accurate up to some hundreds of MHz although not as accurate as FEM-based. 3D-PEEC method uses modified nodal analysis to calculate the equivalent circuit which couples the electric and magnetic field effects which are calculated based on the mesh created from the 3D model. 3D-PEEC method can calculate the effects by full-wave and quasi-static calculations. The magnetic materials can also be included in the calculation [33]. [32]

RLCG solvers are a special case of a PEEC solver. RLCG solvers calculate the resistance and inductance by solving the PEEC calculations without considering the capacitive effect using a RL (Resistance and Inductance) solver. The capacitive effects are calculated by solving the PEEC equations without considering the magnetic effects using a CG (Capacitance and Conductance) solver. RL and CG solvers use different meshes to calculate the fields and by combining these a RLCG equivalent circuit can be formed. The mesh formed in RLCG method divides the cells of the 3D PEEC method further for these calculations. Typically, 3D RLCG method is faster to solve than 3D PEEC due to much smaller matrices in the equations used. However, it can become as complex as 3D PEEC when the number of ports in RLCG method is increased. [32]

Ansys Q3D is a specialised software used for extracting parasitic properties and models from three-dimensional structures such as printed circuit boards. It uses 3D RLCG method, FEM and MoM (Method of Moments) to calculate the electromagnetic fields and their effects. A LF optimized FEM solver is used to calculate the DC solution for resistance and inductance while the MoM solver is used to calculate the AC solution of R and L with the approximation that the skin effect is fully developed. Q3D can calculate both the RLCG models and the S-parameter models, both of which can further be exported to various circuit simulators in the form of netlist [31]. In Q3D the RLCG circuit can be represented as a TLM (Transmission Line Model) which distributes the R, L, C and G components uniformly, making the model in some cases more accurate [32].

Q3D calculates the inductances with the help of ports, or excitations, at the points of interest. Capacitive coupling is calculated between nets and self-capacitance between the signal path and ground but the distributed capacitance inside a net is not modelled. The ports are modelled as equipotential surfaces so current path is defined between two ports called source and sink. Being equipotential means that the surface defined as port is at the same potential. This can cause some issues since it is not how voltage behaves in the real world. [34]

Ansys HFSS uses full-wave FEM to calculate the S-parameters of the ports using the full physics of the 3D-structure. Since HFSS uses full-wave FEM calculations to extract the S-parameters, a boundary condition is needed to limit the problem area. This calculation is computationally heavy and thus it is recommended to use the interpolating sweep. Interpolating sweep calculates the FEM solution at predefined frequency points and calculates the remaining frequencies accordingly. [31]

HFSS supports differential lumped ports as well as single-ended ports. The lumped port is defined as a port between two nets with one being a reference node. If this node happens to be a global reference node i.e., ground, it is referenced as a single-ended port. The length of these ports should be as short as possible for them not to affect the inductance extraction. [35]

3.2.2 HFSS and Q3D accuracy

HFSS is mostly used to model structures involved with HF signalling due to its high accuracy and Q3D is mostly used with LF signals or when fast time to solution is valued. Both solvers come with their downsides. HFSS is significantly more performance demanding since it is up to seven times more CPU (Central Processing Unit) demanding than Q3D [36]. Q3D is not so accurate in higher frequencies. [31]

With HFSS the simulation results can be close to measurement data when simulation frequencies are over 10 MHz, but when the frequency gets below 1 MHz some mismatch occurs [31], [36]. Q3D can simulate up to 10 GHz but due to the restriction that the DUT must be much smaller than the shortest wavelength to get accurate results, the DUT should be small. The most accurate range for Q3D is up to 100 MHz but with correct settings it can be extended up to 1 GHz without significant deterioration. [36]

Q3D has settings to change the simulation frequency and number of cells used in the equivalent circuit export. The simulation frequency changes the frequency at which the model is simulated and from this the parasitic properties at that frequency are obtained. The model consisting of these single values can be exported and used in circuit simulator to get the impedance profile. The number of cells used to construct the equivalent circuit affects the performance of the model over 300 MHz. However, with the number of cells higher than five, the performance is improved only at frequencies over 1 GHz. To get accurate modelling for a 3000 mil (76.2 mm) DUT, a simulation frequency point of 100 MHz and equivalent circuit consisting of 5 cells can be used. This gives accurate results up to 300 MHz and with about 2 dB inaccuracy up to 1 GHz as shown in Figure 10. [36]

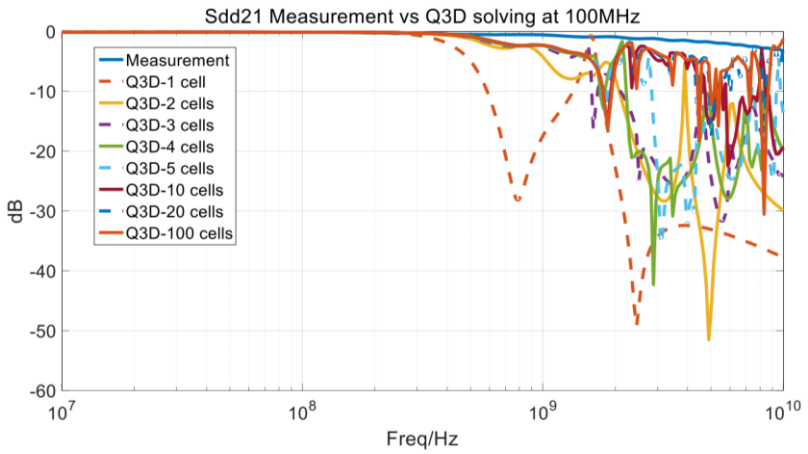


Figure 10. Sweep of number of cells with 100 MHz simulation frequency [36].

The accuracy of extractor tools when compared to measurements has been studied previously to validate these as a tool for estimating parasitic properties before broader manufacturing of the device [35], [37]–[39]. In study [38] it was shown that the difference between Ansys Q3D simulation and measurement can be up to 40 %. In another study this was challenged by a different way of measuring and simulating using Q3D and the results showed lower than 15 % deviation between simulation and measurement [39]. Impedance analysers

also tend to lose accuracy with low parasitic values which can affect the accuracy [39]. A maximum of 10 % deviation from measurements was shown in [37].

The accuracy and speed of simulation can be improved by segmenting the DUT and using Q3D as the simulator or by extracting the LF with Q3D and HF with HFSS [31], [36]. First method improves the accuracy by dividing the DUT into smaller sections so that the wavelength of the highest frequency would be greater than the physical dimensions of the segments. By doing this the single segments can be modelled accurately, and in post-processing these models can be joined in series to get the whole model of the DUT [36]. This also improves the time to solution since the need for HFSS is avoided. Since HFSS might not always be so accurate in the LF and Q3D not so accurate at HF, they can be used to extract the frequencies where they are accurate and then be combined in post-processing [31]. This leads to higher correlation with measured data than using just one solver [31].

The lower accuracy at HF of Q3D models when compared to HFSS models leads to high frequency oscillations which are not present in HFSS model [32]. This effect can be seen in Figure 11 a). The curve in Figure 11 b) shows HFSS model and Q3D model when using the TLM option. In this case it seems to mostly eliminate the high frequency ringing. This behaviour will slow down transient simulations which is problematic when these models are used to evaluate circuit behaviour with parasitic effects in long simulation sets.

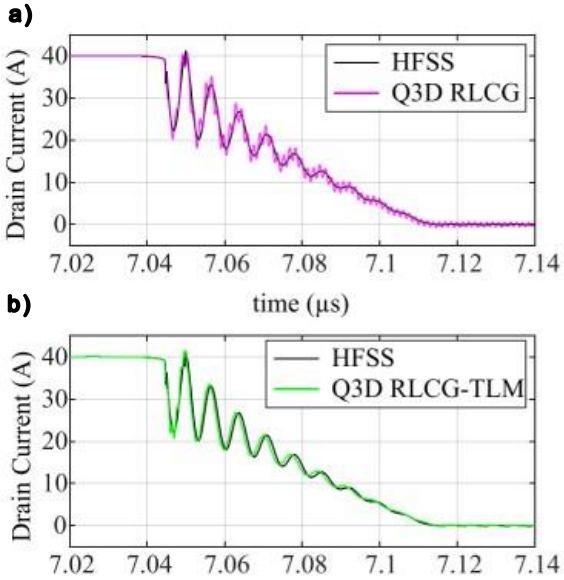


Figure 11. High frequency oscillations in Q3D model [32].

These studies show the strengths and weaknesses of both tools and the best use cases for both. It was also discussed how the accuracy could be improved for Q3D. From these previous studies it can be concluded that Ansys HFSS is not the right tool for the extraction in this study due to its more demanding calculations and thus longer time to solution.

4 PCB DESIGN

A PCB was designed for this study, which was for a PMIC that has three LDO (Low-Dropout) linear regulators and four buck converters from which two can be used in multiphase for higher output power. The specifications of buck outputs and LDO outputs are listed in Table 2 and Table 3, respectively. Due to the integrated circuit being evaluated with this board is a power management integrated circuit, closer attention is given to the power outputs and inputs of the device and their corresponding traces.

Table 2. Buck outputs

Output	Max. f_{SW}	Max. voltage	Max. current
BUCK1	4.4 MHz	3.3 V	5 A
BUCK2	4.4 MHz	3.3 V	5 A
BUCK3	4.4 MHz	3.3 V	2 A
BUCK4	4.4 MHz	3.3 V	2 A
BUCK1+BUCK2	4.4 MHz	1.2 V	10 A

Table 3. LDO regulator outputs

Output	Max. Voltage	Max. current
LDO1	3.3 V	300 mA
LDO2	3.3 V	400 mA
LDO3	3.3 V	400 mA

4.1 Evaluation module outputs

The output side schematic for the designed evaluation module is shown in Figure 12. There are more capacitors than in a typical design since this is used for evaluating the PMIC. Therefore, it is necessary to be able to configure the EVM (Evaluation Module) as needed. The output local capacitors closer to the PMIC are outlined in a solid line and the POL (Point Of Load) capacitors are outlined with a dashed line. Most of the current is assumed to go through capacitor C118. Placement for the buck1 capacitors is shown in Figure 13.

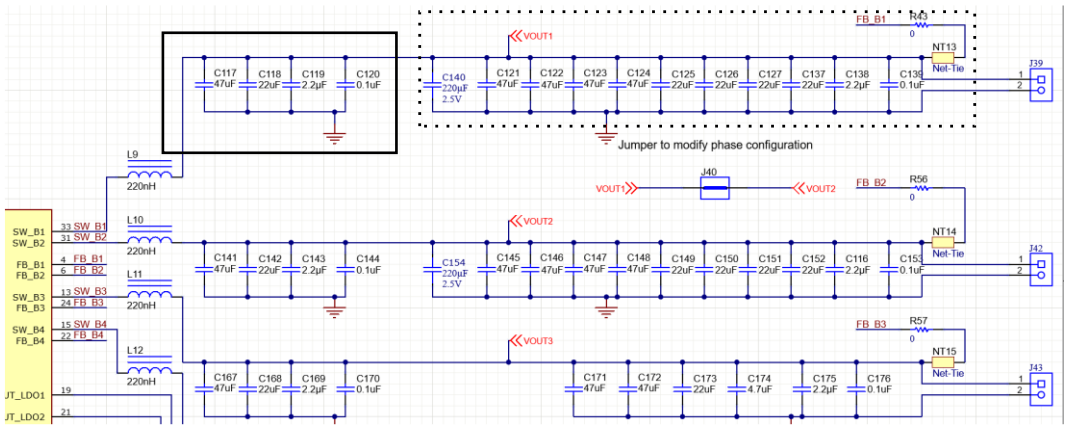


Figure 12. Part of the output side schematic showing bucks one, two and three.

Due to high current output and high switching frequencies, the buck outputs are prone to issues from the printed circuit board parasitic properties. Figure 13 shows the top (a) and bottom (b) layers for one of the buck outputs. The top layer is shown in a) with the output plane

highlighted in green, which is the biggest area in this figure. The area is maximized to minimize parasitic inductance and resistance. Switch node is outlined in blue on the bottom part of the figure a). This is kept as short and wide as possible. Inductor placement is outlined in black, showing the connection to the switch and output nodes, and the PMIC outlined in yellow dashed line. The capacitors are outlined in black in a) and in green in b). Loading connectors are outlined in a blue dashed line with the bigger one being high d*I*/d*t* connector. Because of fast transients on this connector, the top layer POL capacitors in a) are placed closer to this connector. There are in total four similar buck outputs and one of them is shown in Figure 13 as mirror image to the right of the discussed output.

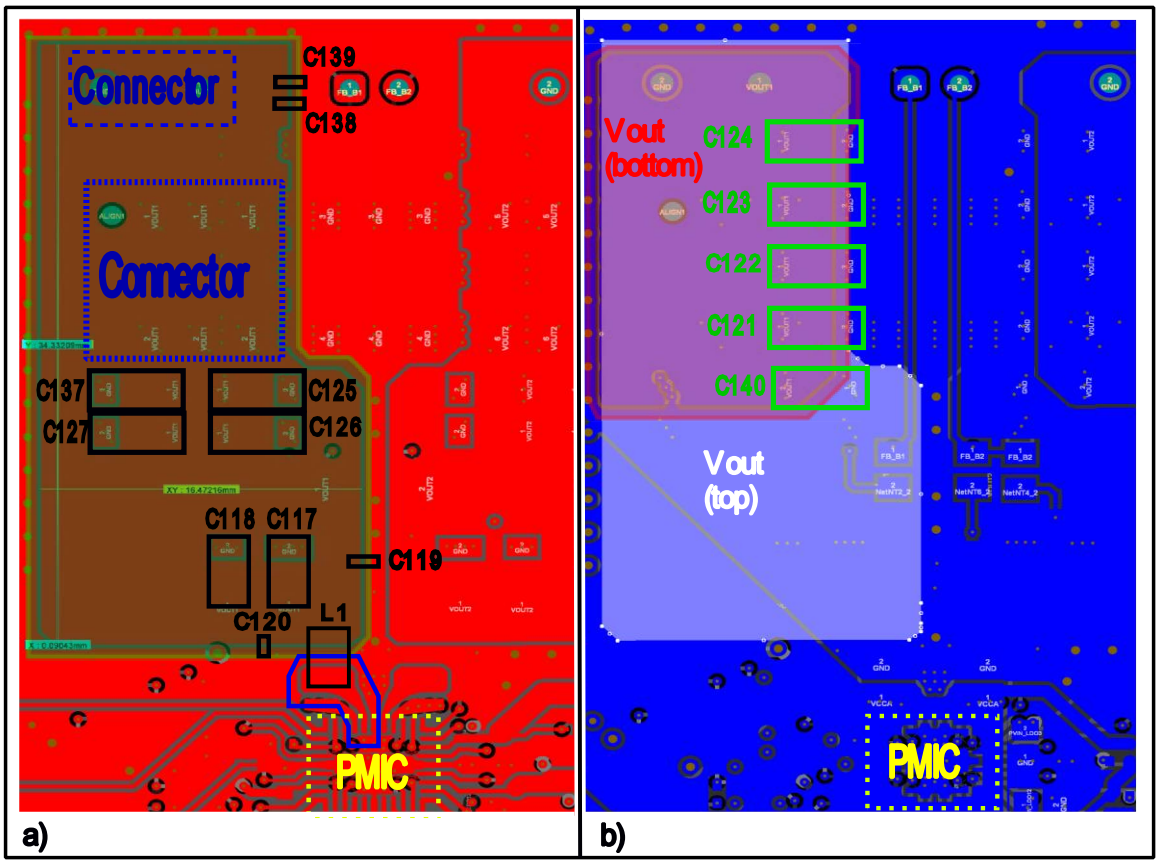


Figure 13. Buck output planes in a) top and b) bottom layers.

Trace to the inductor is kept as short as possible and made as wide as possible to minimize inductance and capacitance of that trace. Inductance of this trace is not as important since it is in series with the much higher inductance inductor, although it still contributes to the loop inductance. Capacitance between this trace and other traces should be kept low because of the fast switching. The parasitic loop inductance causes ringing and may cause overvoltage at the switching node [40]. This is highly important because of the high switching frequency and high dV/dt. In this PMIC the pins next to the switching node are the input voltage for the buck and the power ground. They all need to be as low inductance as possible, so compromises had to be made on all these trace sizes. The feedback of switching regulators is sensitive to noise since it must accurately measure the output voltage. This is why the feedback traces are kept away from any high noise traces.

Current loop in these buck outputs is designed to spread out as much as possible to lower the resistance and inductance. The current is directed to inner layers through vias. The

capacitors at the middle of the plane do not have direct contact to the top layer ground plane, thus many vias had to be used. In these capacitors as many vias were used as possible and they were placed as far away from each other as possible since this minimizes the mutual inductance between vias where current is flowing in the same direction [2].

Figure 13 b) shows V_{out} plane on the bottom highlighted in red and the bigger white highlighted area is the V_{out} plane on the top layer. This is done because there are more capacitors on the bottom layer which could not fit on the top. Because of this there must be some vias going from the top layer to bottom layer. These are mainly placed on the pads of the capacitors to minimize the current loop and thus the loop inductance.

The LDO regulator outputs are not designed to supply a lot of power, so the traces do not have to be as wide as the buck regulator output traces. In this layout the capacitor placement is designed so that the current can flow in the top layer as much as possible to avoid high inductance vias. This is why the current return path is tried to maintain as wide as possible while not having to sacrifice the width of the output traces. Vias are still used so the current can spread out. LDO regulators two and three could easily be designed to have the current flow mostly on the top layer but with the regulator one some vias had to be used to get the current to return to the wanted ground pin of the device. The final design for the LDO regulator outputs is shown in Figure 14 with capacitor placement marked with black rectangles. First millimetres of the output conductor are narrower due to space restrictions near the PMIC which somewhat increases the inductance.

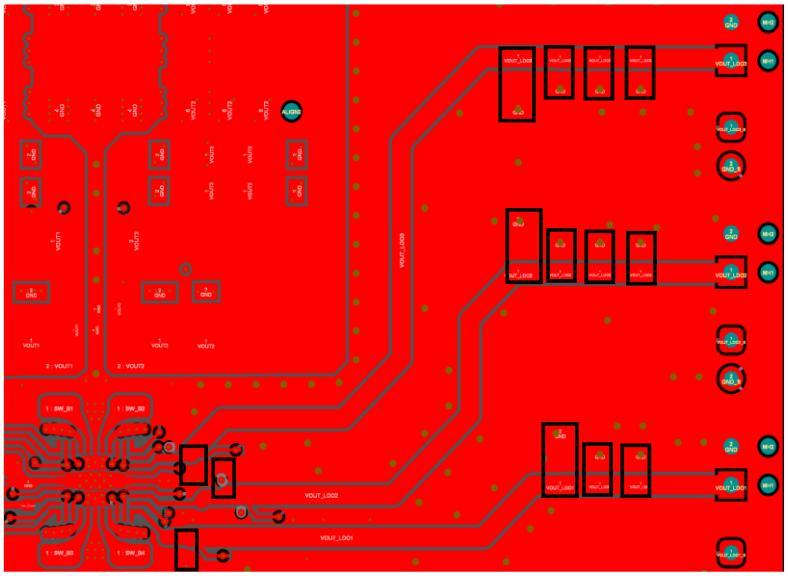


Figure 14. LDO regulator output traces and capacitor placements.

The LDO traces are not included in the further analyses because of their lower current capabilities. The LDO's were discussed since they are a part of the design and it had to be explained why those are not so much of interest in this study.

4.2 Evaluation module input and internal LDO

Since the device can output high currents, it must be supplied with high currents. This leads to high current transients and thus the input traces must have low resistance and loop-inductance to avoid rail collapse and to improve efficiency. The device also has an internal LDO, labelled

LDOVINT, which is used to supply the analog and digital functions of the PMIC. This supply needs an external capacitor for which there is an output pin.

The input side capacitors are shown in Figure 15. Capacitors C5, C8, C114 and C115 are placed on the bottom side under the PVIN pins and capacitors C158, C159, C160 and C161 are placed on the bottom side a bit further from the pin as shown in Figure 16.

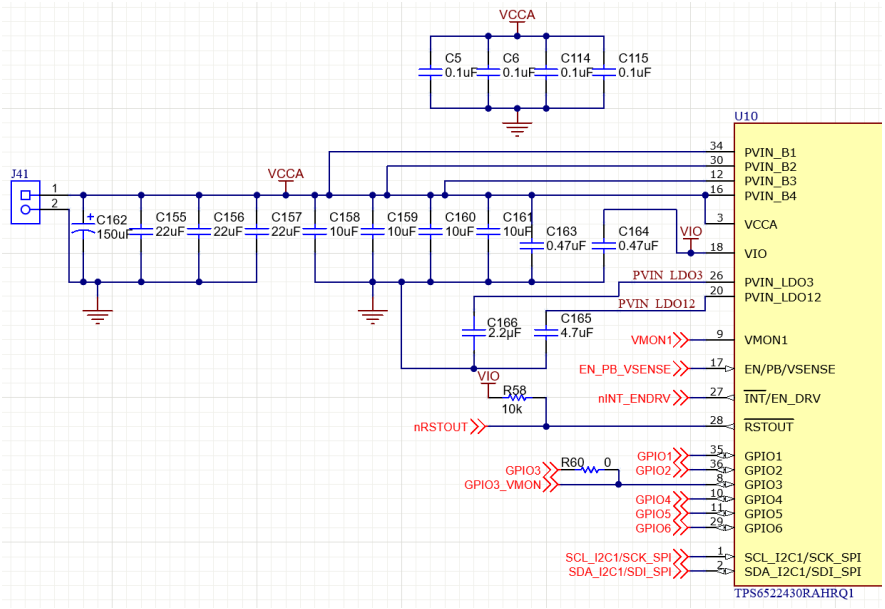


Figure 15. Input side schematic of the PMIC.

The Figure 16 shows the VCCA (positive power supply) plane on the bottom plane for the PMIC. The VCCA plane is highlighted in red and the PMIC is outlined with a dashed line. The VCCA plane runs on the bottom side of the PCB since there is more space for the plane and the input capacitors. These must be as close as possible to the PMIC so that the inductance between the input capacitor and PMIC is as small as possible. Capacitors closer to the PMIC are responsible for the fast transients due to low inductance between the capacitor and the pin and the bulk capacitors for the slower transients due to high inductance between the capacitors and the PMIC.

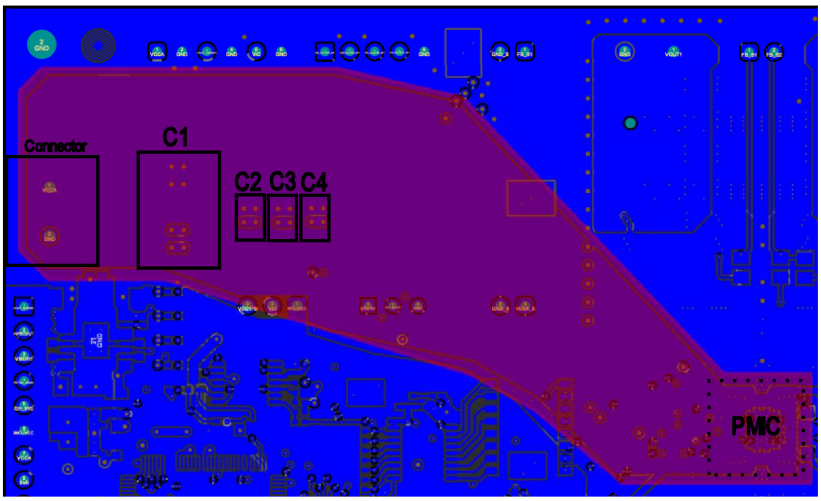


Figure 16. VCCA plane on bottom layer highlighted in red and PMIC location with dashed line.

The outlined connector on the left side of Figure 16 is the input voltage connector for the PMIC. Since this is far away from the device, the trace must be wide to avoid any rail collapse or voltage drop. The VCCA trace is tried to maintain uninterrupted to avoid any high impedance paths for the current. The four bulk capacitors are outlined in black and the local input capacitors for the PMIC are inside the dashed line.

In Figure 17 the four small capacitors outlined with red are the local input capacitors for the PMIC's buck input pins and the four larger capacitors next to them are also for the same node but little further away and with higher capacitance to help with transient loads. The two big capacitors to the right are input capacitors for the LDO regulators, and the small capacitor under the PMIC is for the IO voltage of the device. All these device inputs are prone to voltage variations and thus the capacitors are placed as close to the pins as possible to minimize the loop inductance associated with them. Some of the more important pins are the buck input pins because of their high current draw. Although some vias are needed to pass the current through the layers, this is still a lower inductance path than placing the capacitors on the top layer further away from the PMIC.

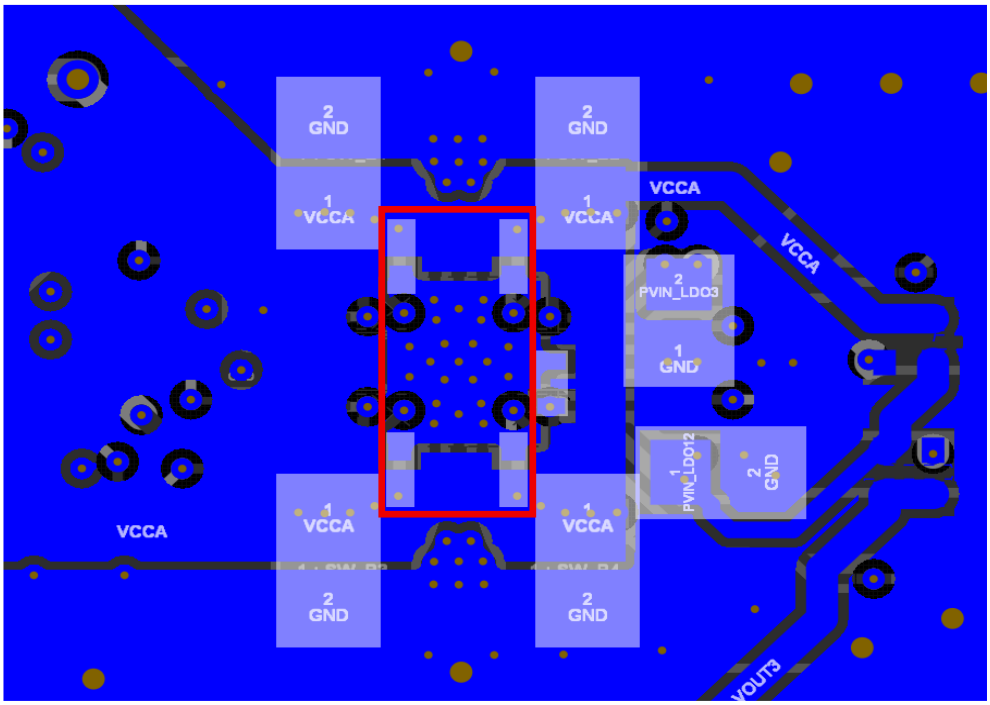


Figure 17. PMIC input capacitors on the bottom layer.

Two points of closer examination were the input pin for VCCA on the top layer and the output for the internal LDO regulator because of their high importance. These pins and their capacitors can be seen in Figure 18. The VCCA capacitor is C163 in Figure 15. Two options for the placement of these capacitors were considered which were to place them horizontally or vertically. In the vertical orientation one of the capacitors must be further away from the PMIC so the LDOVINT capacitor placement was prioritized.

The loop inductances were extracted by using Ansys Q3D software, and the loop used for both was from pin to capacitor positive terminal in series with capacitor negative terminal to ground pin of the PMIC. The extracted inductances are shown in Table 4.

Table 4. VCCA and LDOVINT loop inductance with different capacitor placements

Orientation	Current loop	Loop inductance
Vertical	LDOVINT	0.70 nH
	VCCA	1.17 nH
Horizontal	LDOVINT	0.98 nH
	VCCA	1.04 nH

Table 4 supports the theory that shorter loop should have less loop inductance since in the vertical layout the loop of VCCA came to be longer than in the horizontal orientation and LDOVINT loop inductance is smaller with vertical arrangement since it can be placed closer to the device. Based on these results it was decided that the LDOVINT capacitor is placed vertically and VCCA capacitor horizontally to minimize the loop inductance for both. This layout is shown in Figure 18 with the two capacitors highlighted.

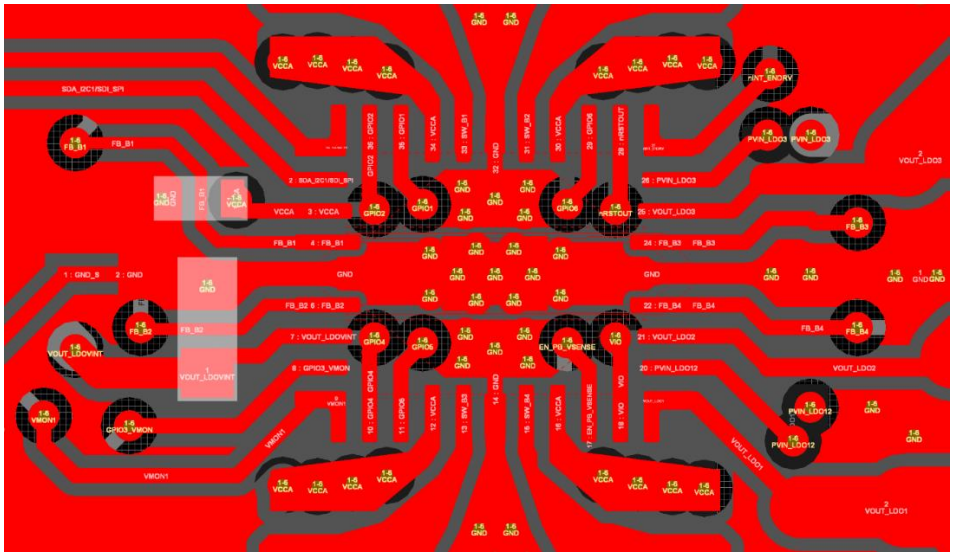


Figure 18. Final placement of VCCA (top) and LDOVINT (bottom) capacitors.

Although the LDOVINT layout is important, it is not further examined in this thesis. The analysis done on VCCA and LDOVINT capacitor placement could have been done on every capacitor in the design, but this would have taken a significant amount of time and since it was not in the scope of this thesis, it was not done on any other capacitor placements.

5 SIMULATION AND MEASUREMENT SETUPS

The parasitic properties of this EVM were extracted from two critical points which affect the performance of the PMIC. These points are the trace between switching regulator local and point of load capacitors, the return path associated with this and the input loop for the buck regulator.

5.1 Points of interest for extraction

The impedance, and more specifically the inductance, between the local and POL capacitors is of interest because of the phase shift it creates. This phase shift decreases the phase margin so if the inductance is too high at this point the device can become unstable. These conditions were simulated in SIMPLIS by SIMPLIS Technologies which is a specialized simulator for switching mode power supplies. The schematic used for these simulations is shown in Figure 19. These simulations were done to demonstrate why these points were chosen for the parasitic extraction.

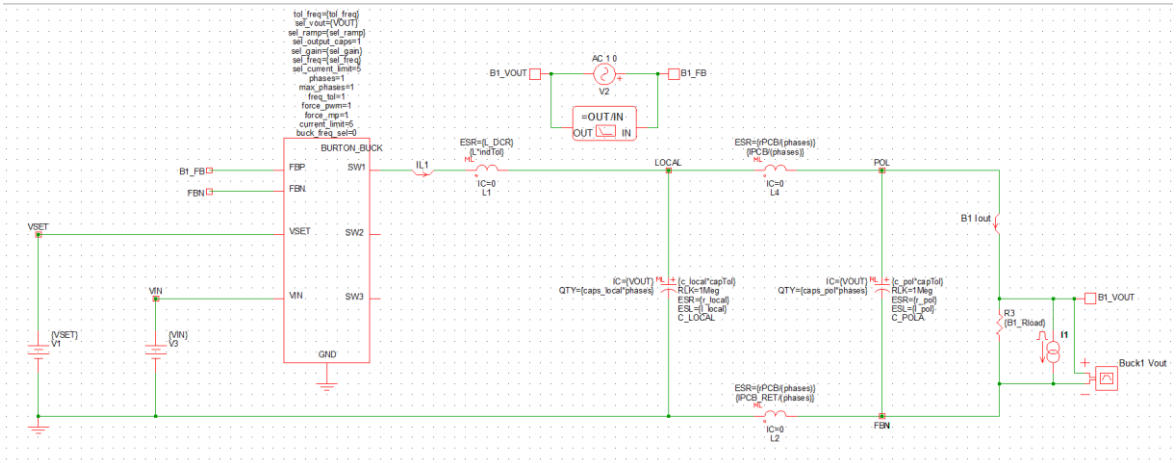


Figure 19. Schematic used in SIMPLIS simulations.

The effect of inductance in the signal path and the return path were evaluated separately. The inductance in signal path was simulated with no return path inductance so L2 in Figure 19 was shorted and the PCB inductance was simulated with a few different values. The effect of return path inductance was evaluated with signal path inductance of L1 set to 2 nH to show more prominent results and only the return path inductance L2 was swept. Local and POL capacitance was kept at a constant value and the used load transient was from 0 A to 1 A in 1 µs and the pulse duration was 100 µs.

The AC simulations show the loop gain and phase of the buck converter measured between feedback pin and output. The AC simulation plots for inductance in signal path can be seen in Figure 20 with phase plotted with black and gain in red. The plots differ slightly when the inductance increases but then considering that this is only from the PCB parasitic properties which can quite easily be mitigated, it is a noteworthy difference which has to be taken into consideration. Table 5 shows the full simulated values.

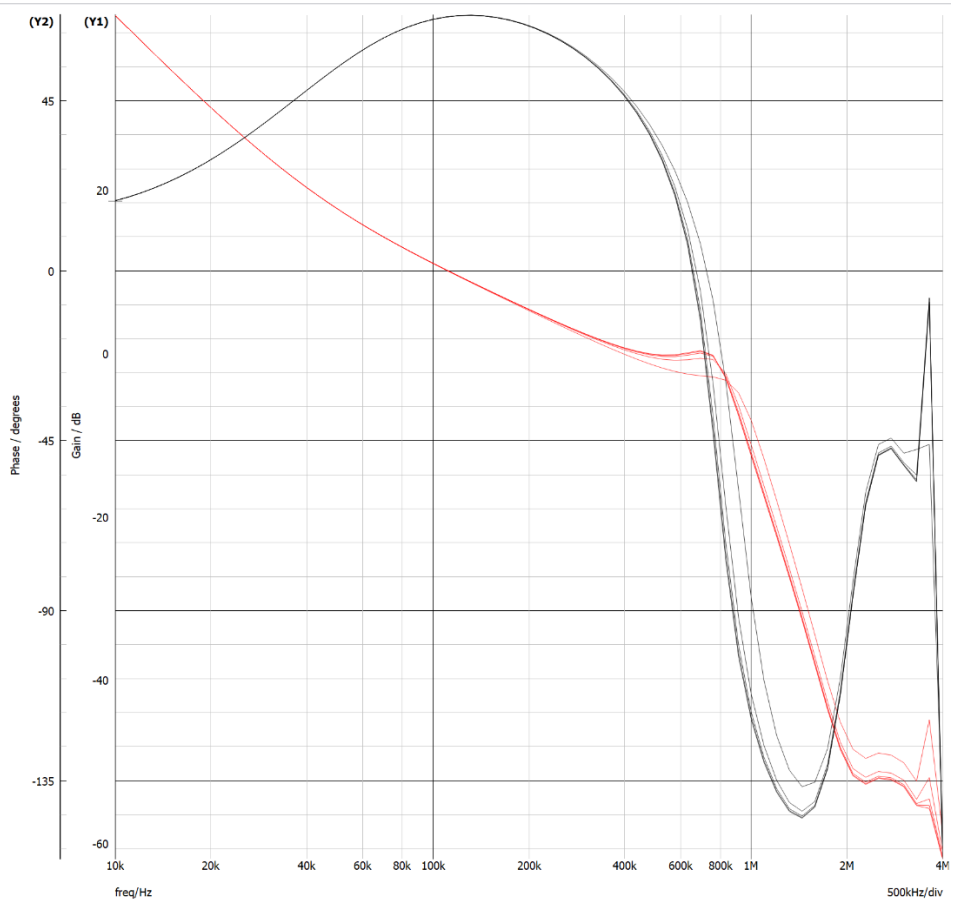


Figure 20. Loop gain and phase with inductance between local and POL capacitors. Measured between feedback and output. Red plot is gain and black is phase.

In Table 5 the simulated values are listed at different inductance values between local and POL capacitors. Gain crossover frequency, GM (Gain Margin) and PM (Phase Margin) are listed from the AC simulation and V_{out} maximum and minimum voltages as AC coupled measurement are listed from the transient simulation. These are the maximum and minimum deviations from DC level. It is seen that the phase margin is 48 degrees with 3 nH between local and POL capacitors and only 37 degrees with 4.45 nH which is the largest value simulated. This difference in phase margin is why the layout of the V_{out} trace should be well designed. Although the PM is well above the risk of instability the GM goes below zero when the inductance increases. This below-zero GM could make the regulator unstable at some point.

Table 5. Inductance between local and POL SIMPLIS results

Inductance/lPCB (nH)	Crossover (kHz)	GM (dB)	PM (degrees)	Max V_{out} deviation (mV)	Min V_{out} deviation (mV)
3	392.5	2.83	48.1	12.5	-12.7
4	431.8	0.68	42.8	12.6	-12.6
4.3	453.6	0.11	39.5	12.8	-12.7
4.4	464.0	-0.07	37.9	12.4	-12.8
4.45	470.5	-0.16	37.0	20.1	-20.3

The transient simulation for the same inductance sweep is shown in Figure 21. From the transient plot it is seen that when the max inductance is reached, the output starts to oscillate as

was predicted from the GM values. From Figure 21 it can be see that with smaller values the device is stable, but the ripple increases up to 2 mV with 4.4 nH. This is not seen in Table 5 values since the maximum and minimum values are the deviations from DC level which is 1.8 V.

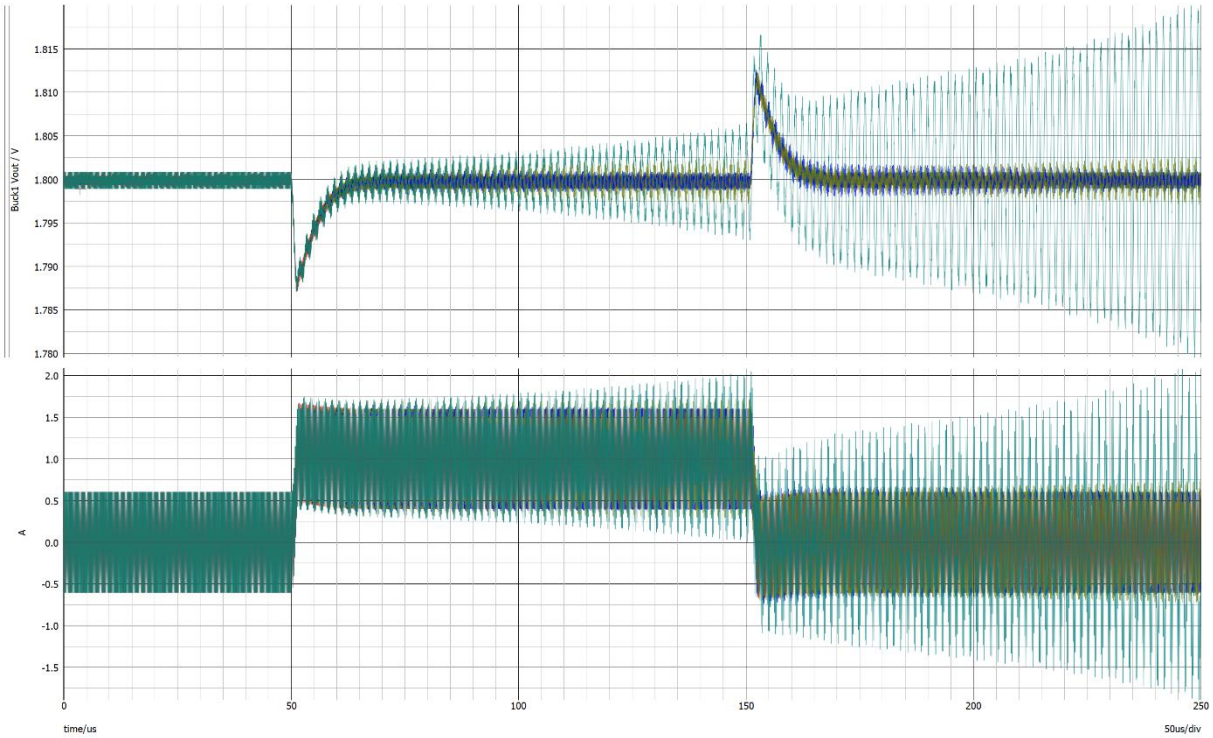


Figure 21. Transient simulation with inductance between local and POL capacitors.

The AC simulation results for the return path inductance sweep can be seen in Figure 22. Here the effect of inductance can be seen clearly in the black phase plot and quite well in the red gain plot. The maximum and minimum phase margin were 43 degrees and 2.2 degrees, respectively. These results were simulated with inductance values of 1 nH and 3 nH as can be seen in Table 6. In these results there is no crossover frequency or gain margin since the phase crosses zero degrees twice and thus the simulator does not know which value to use. From the plots the phase crossover would be between 800 kHz and about 1.5 MHz if it did not start from negative values. GM is positive for all the cases.

Table 6. Inductance in return path SIMPLIS results

Inductance/LPCB_RET (nH)	PM (degrees)	Max V_{out} deviation (mV)	Min V_{out} deviation (mV)
1	43.3	13.1	-13.4
1.5	41.4	13.0	-13.3
2	29.4	13.0	-13.3
2.5	14.8	13.0	-13.3
3	2.2	13.1	-13.4

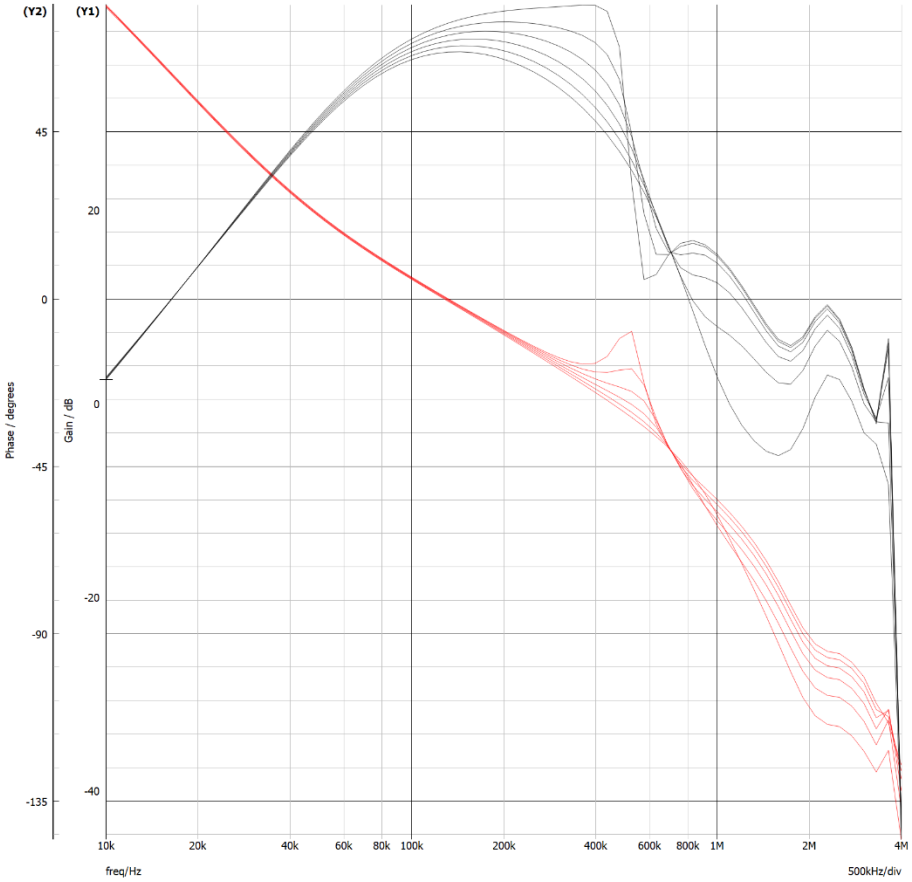


Figure 22. Loop gain and phase with inductance in return path. Measured between feedback and output. Red plot is gain and black is phase.

Although the phase margin minimum is low, the converter does not start to oscillate in a same way as in the previous case due to the positive gain margin. Since the regulator never starts to oscillate, the maximum and minimum values in Table 6 are all almost the same. In transient simulation the maximum voltage ripple can be seen to be around 2 mV peak-to-peak. The inductance in return path will introduce ground bounce in the load device since with fast transients the inductance of the inductor rises and the voltage drop over it increases.

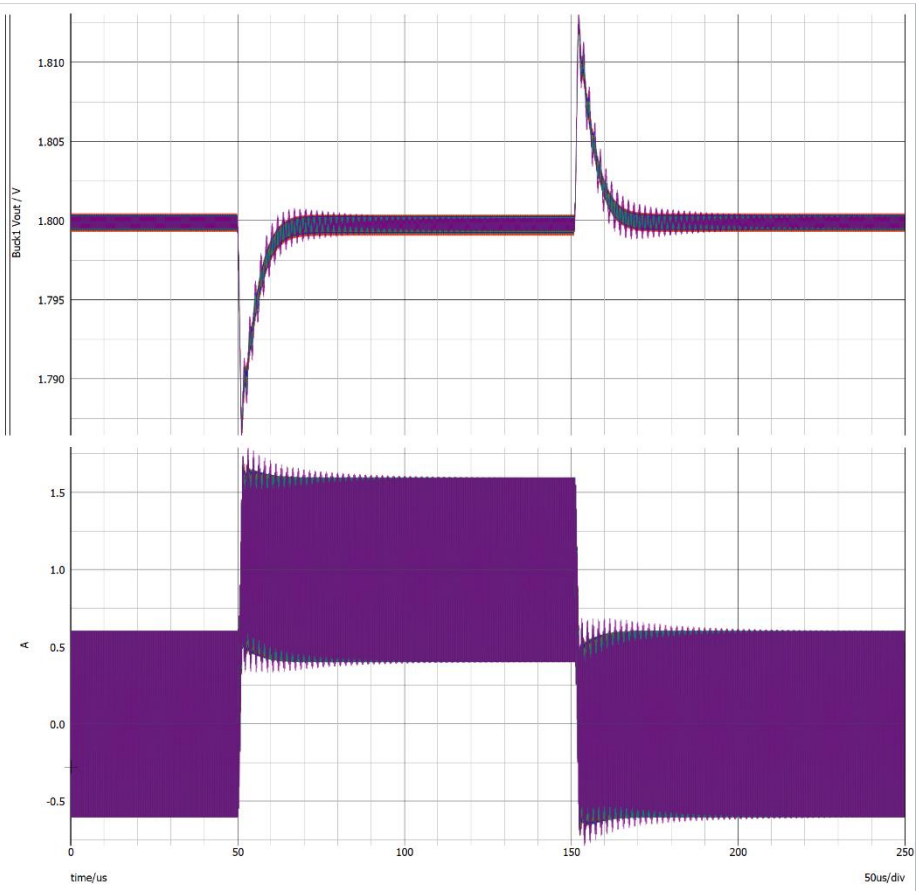


Figure 23. Transient simulation with inductance in return path.

The input loop is of interest due to high current changes between positive and negative switching cycle which is shown in Figure 24 as the difference path. Any inductance in this path will create voltage drops and rail collapse. This is why the input capacitor C_{in} should be placed as close to the IC (Integrated Circuit) as possible and on the same layer. If using multiple input capacitors, the one with the smallest value should be placed closer to the IC because it is providing the current path for the highest frequencies which are more prone to inductance. Frequencies up to and above 100 MHz are of interest in the input side since the rise and fall times of the switching are in the nanosecond region, thus the frequencies are higher in the input side than on the output side.

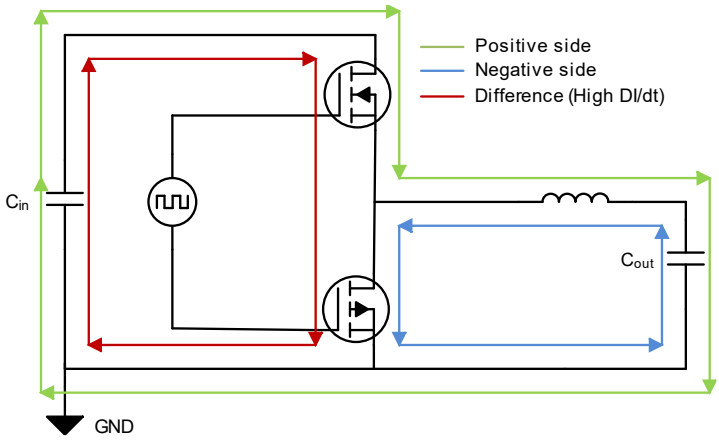


Figure 24. Currents in synchronous buck converter.

Since there are a lot of capacitors at the output, one had to be chosen to be the point of simulations and measurements. To get an idea how the currents flow through these capacitors at different frequencies, a current density simulation was run from 10 kHz to 100 MHz. Ansys SIwave uses magnetic field calculations to determine the current flow, and in the simulation results the magnetic field strength is shown. Magnetic field and current, and therefore current density, are related by equation (13). This is relative to the current flowing in the conductor. This simulation was run with two different conditions. First, the simulation was conducted with all the capacitors being similar with 22 µF capacitance and otherwise being ideal with no inductance or resistance. The second simulation was run with the correct values for capacitances and 500 pH ESL (Equivalent Series Inductance) with no resistance. This is done to determine whether the current path is more related to the resonance frequencies of the capacitors or the inductance of the PCB. The frequencies of 2 MHz and 100 MHz were chosen as the compared frequencies. The first simulation with all capacitors at the same value at 2 MHz and 100 MHz can be seen in Figure 25 a) and b), respectively. The capacitors on the top layer are highlighted with blue, inductor with dotted black and the voltage source placement with a circle as well as plus and minus signs. Voltage source was placed between the switch node and the ground.

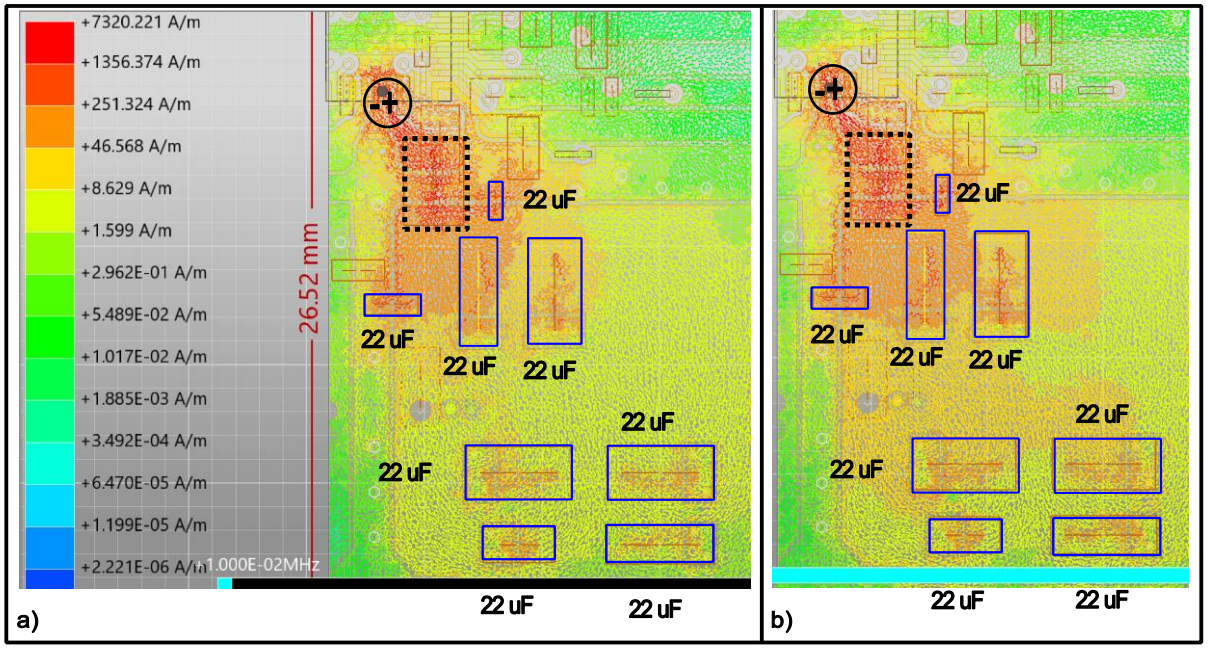


Figure 25. Current density with all the capacitors at the same value. Capacitors outlined in blue, inductor in dotted black and voltage source placement with a circle. a) 2 MHz and b) 100 MHz.

From Figure 25 it can be seen the current flows nearly the same way at 2 MHz and 100 MHz with only slight differences. This indicates that the differences in current path originate only from the properties of the PCB since the capacitors have the same impedance profile. If the capacitors would have different capacitances and thus different impedance profiles, the current would flow through the capacitor with the smallest impedance at that frequency. This behaviour can be seen in Figure 26. It can be seen that at 2 MHz the current flows more through the 22 µF and 47 µF which are placed closer to the inductor. According to equation (21) these have a lower resonance frequency and lower impedance at low frequencies. The reason the current is not flowing as much through the big capacitors further from the inductor is the inductance of

the PCB. At 100 MHz the current flows more through the 0.1 µF and 2.2 µF capacitors close to the inductor which have smaller impedance than bigger capacitors at higher frequencies. The decrease in current density can be seen clearest in the four capacitors furthest away from the inductor. The decrease in current density in these capacitors is because of the additional inductance of the PCB when compared to the upper capacitors in addition to the lower resonance frequency.

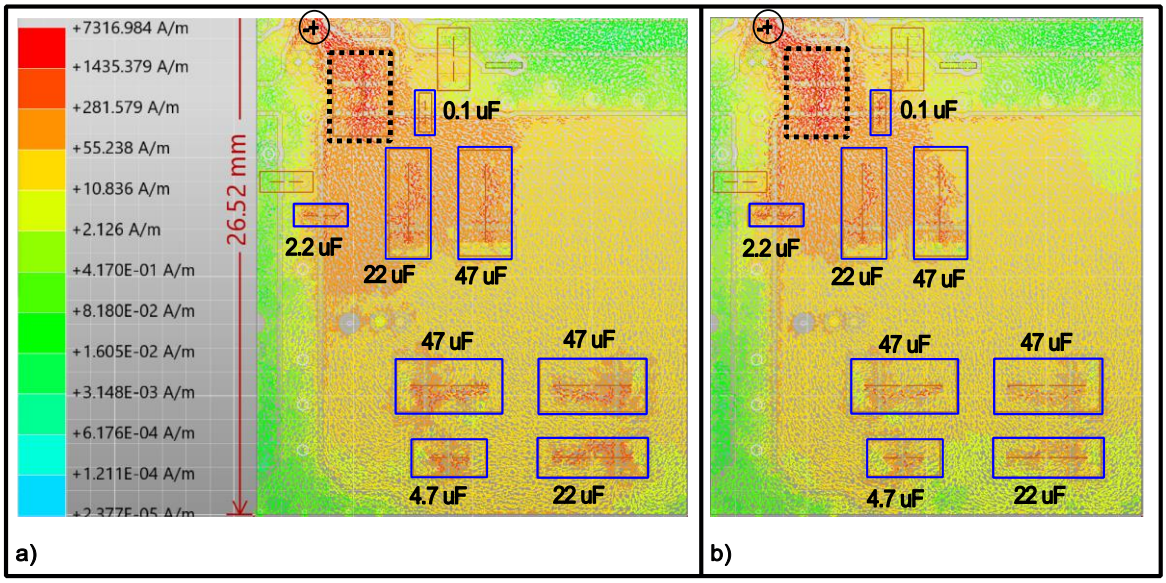


Figure 26. Current density with different capacitor values. Capacitors outlined in blue, inductor in dotted black and voltage source placement with circle. a) 2 MHz and b) 100 MHz.

Furthermore, from Figure 27 the SRF (Series Resonance Frequency) of a 4.7 µF capacitor can be seen at 3 MHz. With the equation (21) and using the 500 pH ESL, the theoretical SRF can be calculated to be about 3.28 MHz which matches the simulations well. There is some difference since the inductance of the PCB is in series with the ESL of the capacitor. This confirms that the current flow is mainly through the capacitors offering the lowest impedance and is not so dependent on the parasitic properties of the PCB.

From these simulations it is concluded that the current flow is related to the capacitor values and the inductance of PCB has only some effect on this. Because of this, the loop inductance can be simulated and measured through one capacitor and simulating and measuring multiple loop inductances through different capacitors is of minimal interest.

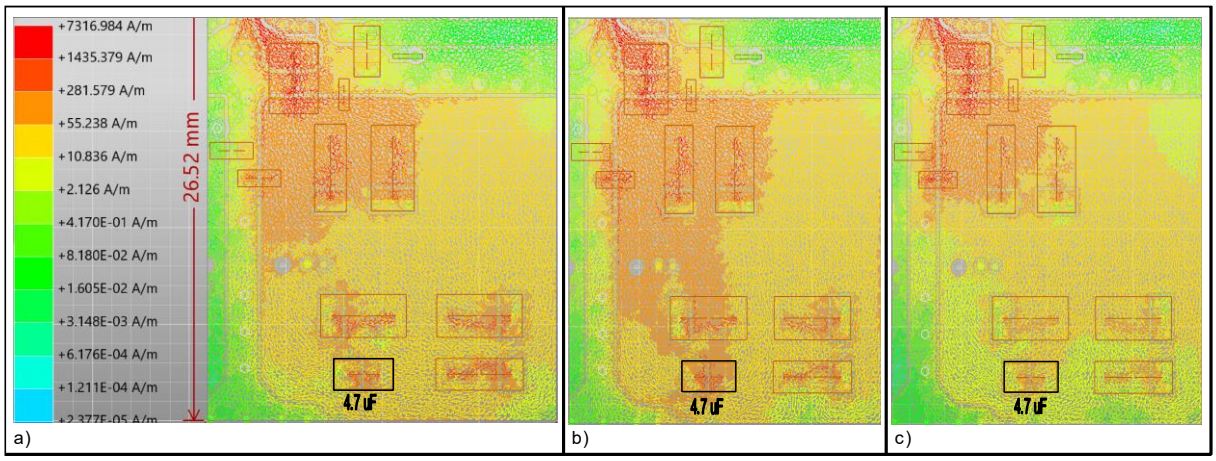


Figure 27. Current through a 4.7 µF capacitor at SRF. a) 2 MHz, b) 3 MHz and c) 4 MHz.

With these simulations the points of interest were determined and the reason why those were chosen for the final parasitic extraction were explained.

5.2 Measurement setup

For each simulation a corresponding measurement was taken to see how accurate the extracted model is. The measurements were taken on a bare PCB with no components and only two short coaxial cables soldered to the measurement point. The cables were soldered to get the best possible contact and to minimize contact resistance and inductance, which could be a problem with such low impedances. The S_{21} parameter was measured using a shunt-through method due to its ability to measure impedances down to mΩ region.

The setup consisted of Rohde & Schwarz FSU26 spectrum analyzer with network analyzer option added, Rohde & Schwarz SMJ100A vector signal generator, and Aaronia UBBV 0910 pre-amplifier. The setup is shown in Figure 28.

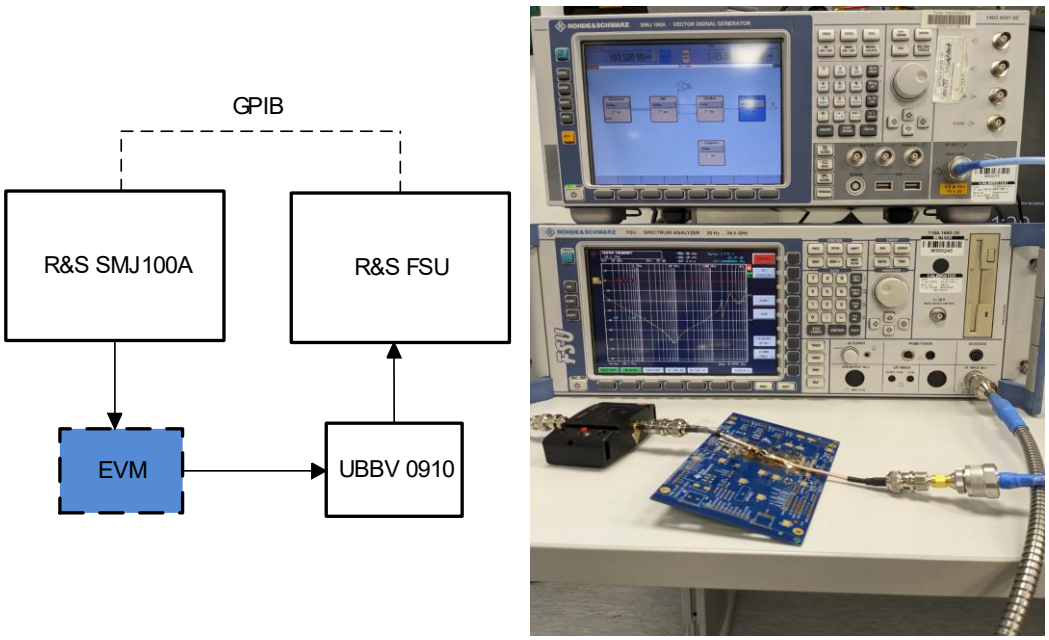


Figure 28. Measurement setup and block diagram.

The Rohde & Schwarz FSU is a spectrum analyzer with bandwidth from 20 Hz to 26.5 GHz. This unit is equipped with network analyzer add-on which makes it possible to connect a suitable signal generator to the FSU through GPIB (General Purpose Interface Bus) or TTL (Transistor-Transistor Logic). This way the generator can be controlled from the FSU and the parameters of the test signal can be accounted for already in the measurement. Thus, no post processing is needed to eliminate the qualities of the test signal.

The Rohde & Schwarz SMJ100A is a vector signal generator that is suitable for connecting to the FSU through TTL or GPIB, with the latter used in this setup. The bandwidth of the signal generator is from 100 kHz to 6 GHz. The SMJ100A limits the measurement range from the low frequencies but not from the high frequencies.

The Aaronia UBBV 0910 pre-amplifier is a battery powered low noise amplifier with typical gain of 22 dB. Maximum input power is +10 dBm and maximum output power +8 dBm and it is terminated to 50 Ω. The frequency range of the UBBV 0910 is from 9 kHz to 6 GHz thus not limiting the lower frequencies.

The DUT was connected using as short as possible coaxial cables. The cables were soldered directly to the DUT point of interest and taped down to the EVM to avoid stress and possible breaking as is shown in Figure 29. This way eliminating contact resistance and inductance as much as possible. Some adapters had to be used to connect all the different cables and device connectors but the use of them was minimized where possible.

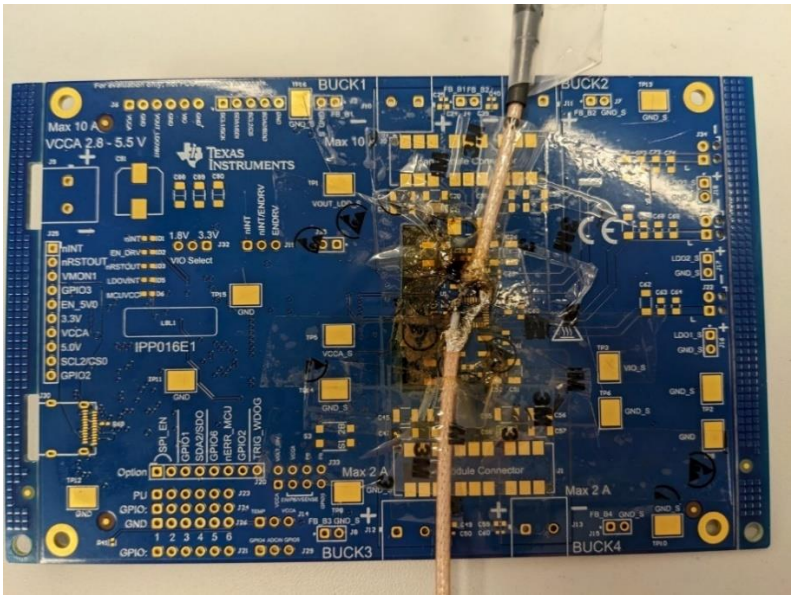


Figure 29. EVM with soldered coaxial cables and tape to limit stress on solder contact.

The measurements were all taken with shunt-through method with soldered cables. The parameters used are shown in Table 7. Before the measurement the reference plane was calibrated to be at the end of the coaxial cables which were soldered down. This was done by directly soldering the coaxial cable signal lines together and ground braids together. Then a calibration measurement was taken. By doing this the effect cables, interconnects and any other functional blocks in the measurement path was measured. Then this measurement was normalized to be the 0 dB line. Now if a measurement was taken again, the spectrum analyser would draw a straight line on 0 dB, thus also the pre-amplifier gain was normalized out and no data manipulation had to be done to account for this. Calibration was performed after even the slightest change in the setup. All the measurements were taken with logarithmic frequency

sweep and exported to a PC (Personal Computer) via Rohde & Schwarz RSCommander software.

Table 7. Measurement parameters

Parameter	Value
Start frequency	100 kHz
Stop frequency	1 GHz
Input signal magnitude	-15 dBm
Resolution bandwidth	30 kHz
Video bandwidth	10 kHz
Sweep time	3.4 s
Reference level	10 dbm
Attenuation	35 dB

The measurement setup was validated by measuring a known capacitor which in this case was LLL21R71E104MA01 from Murata. This validation had to be done since there was no existing impedance measurement setup or information on how it should be done with the available instruments. The comparison between data from Murata SimSurfing tool [41] and the measurement taken with the established setup can be seen in Figure 30.

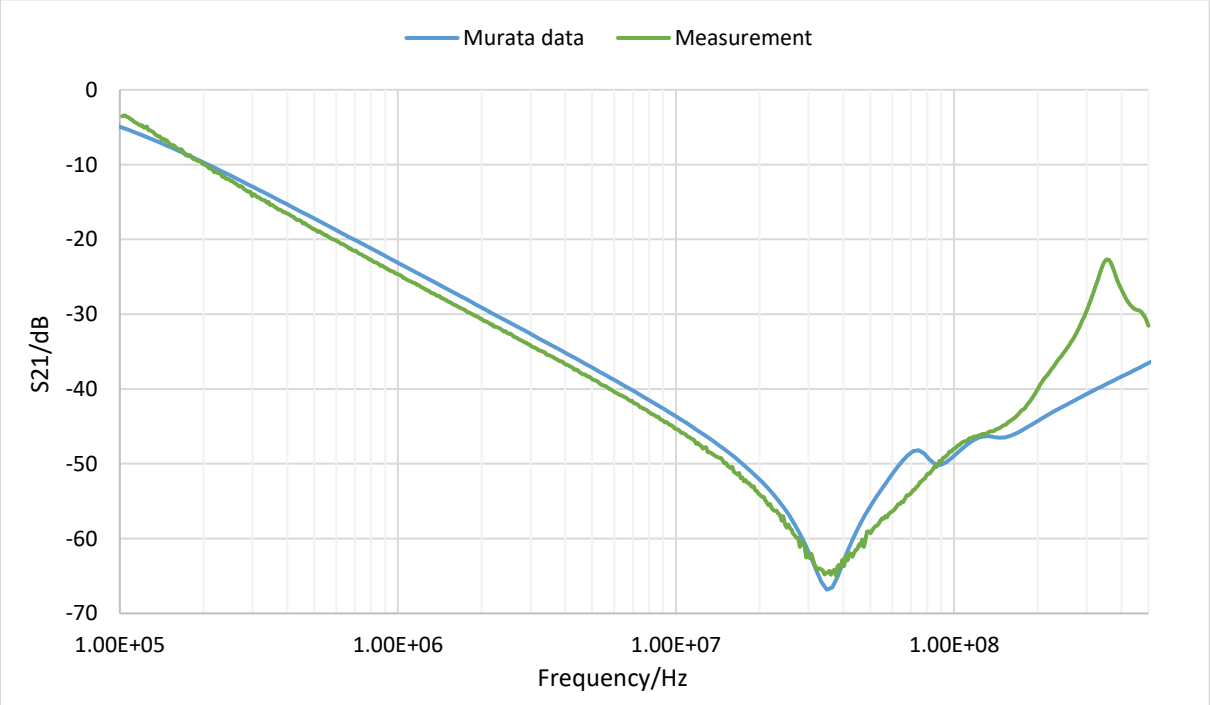


Figure 30. Measurement setup validation comparison.

The validation measurement shows a good match with the reference data across the entire frequency span. There is a small difference from 200 kHz to 2 MHz and above this all the nuances of the Murata's curve could not be replicated precisely. Other than these relatively small differences, some of which could come down to the unit measured, the overall shape is close to the reference data. The biggest difference is the parallel resonant frequency at about 350 MHz but since this is out of the range of interest it is not considered a major factor.

5.3 Simulation setup

The simulations were done using Q3D in AEDT (Ansys Electronics Desktop). The simulations had some common settings which were not changed during the simulation variations. The design settings window can be seen in Figure 31 and the full static settings in Q3D Design Settings window in Table 8. S Parameters setting is not shown here since it is varied in simulations between TLM and RLCG options.

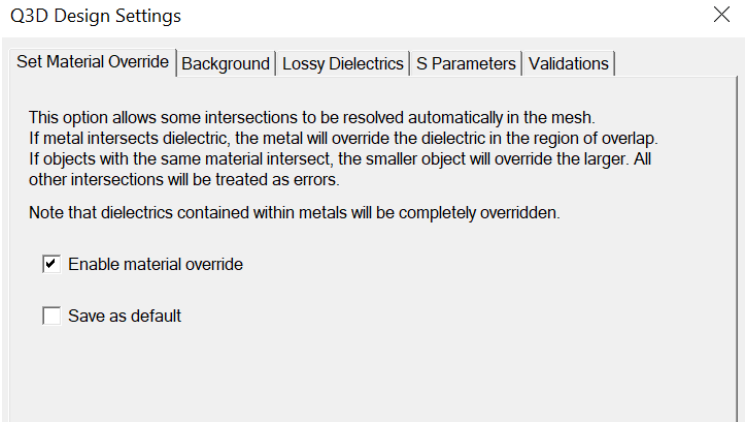


Figure 31. Q3D design settings window.

Table 8. Q3D static design settings

Setting	Set value
Enable material override	ENABLED
Background material	air
Automatically use causal materials	ENABLED
Ignore Unclassified Objects	DISABLED
Skip Intersection Checks	ENABLED
Perform full validations	ENABLED

The materials used and their parameters in Q3D can be seen in
Table 9 which are the default values with nothing changed. FR4 is used as the surrounding material for the layers as in real PCB, copper is used for all the conductive layers, solder is used for all the solder balls and solder resist is a thin layer on top of the top layer.

Table 9. Material parameters

Material	Parameter	Value
FR4	Relative permittivity	4.2
FR4	Relative permeability	1
FR4	Bulk conductivity	0
FR4	Dielectric loss tangent	0
FR4	Thermal modifier	None
Copper	Relative permittivity	1
Copper	Relative permeability	0.999991
Copper	Bulk conductivity	58 MS/m
Copper	Dielectric loss tangent	0
Copper	Thermal modifier	None

Solder	Relative permittivity	1
Solder	Relative permeability	1
Solder	Bulk conductivity	7 MS/m
Solder	Dielectric loss tangent	0
Solder	Thermal modifier	None
Solder resist	Relative permittivity	3.5
Solder resist	Relative permeability	1
Solder resist	Bulk conductivity	0
Solder resist	Dielectric loss tangent	0
Solder resist	Thermal modifier	None

All the extractions were done with 100 MHz simulation frequency and the selected solutions are capacitance/conductance, DC resistance/inductance and AC resistance/inductance. All the other options were left as default as shown in the window in Figure 32. The 100 MHz solution frequency is based upon the findings of previous studies discussed earlier such as [36] since it should give accurate results in the frequency range of interest.

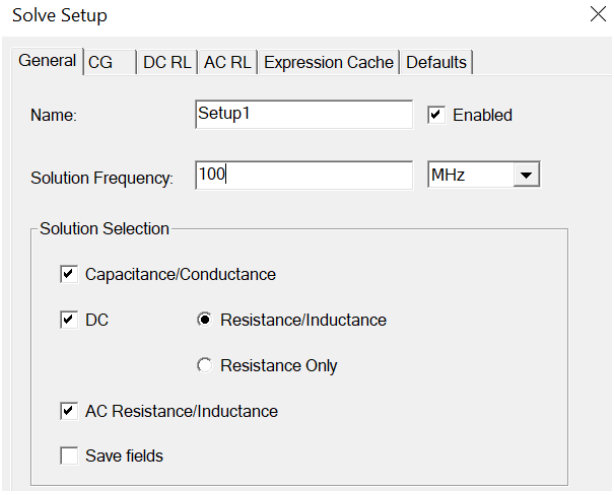


Figure 32. Q3D solution setup window.

The single frequency equivalent circuits were exported with the original matrix and by using capacitance, conductance, DC resistance and AC inductance with the number of cells being five were used as is shown in Figure 33. In some cases, AC resistance was used instead of DC, but this is mentioned in these cases. The export options for the frequency sweep are a bit different and can be seen in Figure 34. The number of cells was determined from studies discussed previously. Setting number of cells to five is a good middle ground for accuracy and performance in any possible post simulation run using the exported circuit. For higher frequencies more cells might prove to be more beneficial but below 100 MHz five cells should be enough. The format used for extraction was '*.cir'.

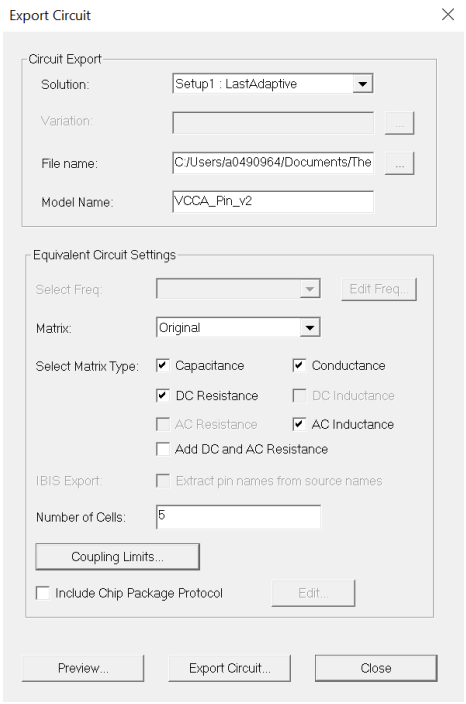


Figure 33. Q3D single frequency export settings.

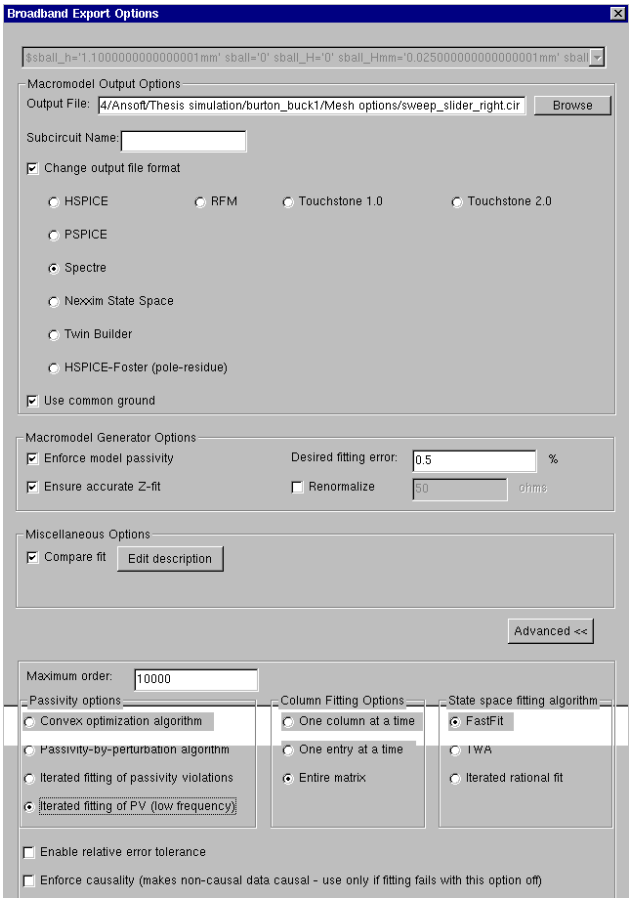


Figure 34. Frequency sweep export options.

The equivalent circuits were imported to Ansys Circuit spice simulator which is included in electronics desktop software. In Circuit two ports were placed on the same port to simulate the shunt-through measurements and ideal ground was placed on the port where the ground braids were in the measurements. The two ports were referenced to this ground. The solution setup used was linear network analysis with decade count sweep using frequencies from 100 kHz to 1 GHz with 50 counts in each decade. Although the highest frequency of interest was 100 MHz, the simulations were done up to 1 GHz to get more data just in case. The linear network analysis setup can be seen in Figure 35.

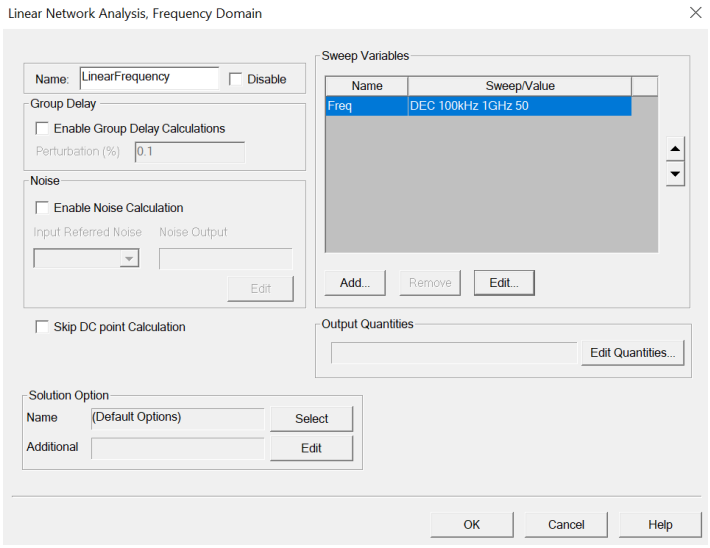


Figure 35. Linear network analysis setup in Circuit.

5.4 Simulation variations

There are a lot of different options in Q3D for changing the calculated solutions. There are options to change how the mesh is created, the simulation frequency or frequencies, the accuracy of each independent solver and the complexity of geometries just to name some. On the extraction side user can choose which solutions are accounted for in the circuit, how many cells are used and the exported format. Also, the way the model is created and where all the excitations are placed also affects the modelling accuracy. All these options change the solution accuracy, which affects the simulation time so user can choose the right balance for the current need. These models and solutions can also take a lot of disk space so that also must be taken into consideration. Since testing the effect of all these different options would take a lot of time only some were considered in this study.

On the modelling side the effect of solder ball modelling was tested to see how well the actual component soldering can be modelled. The models for solder balls in Q3D can be created in two ways. Easier method is to assign solder balls to the pads in SIwave which creates the solder ball from the determined options as shown in Figure 36. The user does not necessarily have to modify the pre-set values which speeds up the process even more. There are multiple options for the solder ball type but only the simple options were tested.

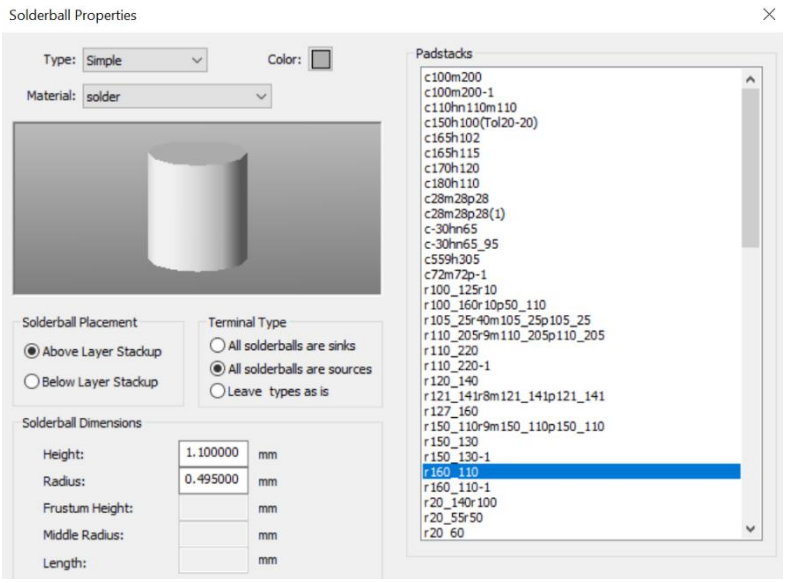


Figure 36. Example of default solder ball parameters.

The other way to create solder balls in Q3D is by drawing them manually. This takes a significant amount of time since every different solder ball must be created separately. These can be copied and pasted on other pads which speeds the process somewhat. The upside of creating the solder balls manually is that they can possibly be modelled more accurately than with the automatic creation.

The effect of solder ball dimensions to the extracted circuit was evaluated by changing the width and height of the solder balls. This was done by creating them in Q3D manually and assigning a variable to the height and width. These variables were swept using the Optimetrics solution option in Q3D. These sweeps were separate so that the other variable was kept constant while the other was swept across some values. Solder ball height was swept from 0.0025 mm to 0.25 mm with steps of 0.025 mm. The solder ball width and length were 1.6 mm and 1.0 mm or 1.1 mm depending on the solder ball. Also, the default solder ball created in SIwave was tested with the exact pre-determined values.

The mesh options in Q3D were tested to see if the mesh quality affects the simulation accuracy or time in a meaningful way. The available mesh options can be seen in Figure 37. These are the settings from which Q3D starts to refine the mesh when analysed.

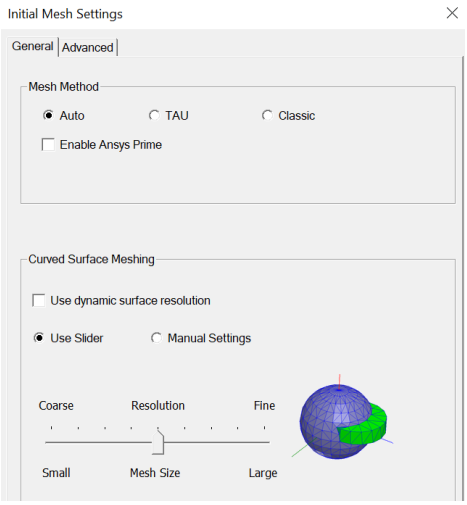


Figure 37. Initial mesh settings in Q3D.

From the mesh method section in these settings “Auto” is the default setting where the solver automatically selects the mesher. “TAU” mesher remeshes only some specific curve faces. “Classic” option is the standard mesher used in Q3D. When Enabling “Ansys Prime”, the solver tries to remesh existing meshes to improve the accuracy of the CG solutions. If a mesh has been remeshed it will show up in solution profile. In the curved surface meshing section, the “use dynamic surface resolution” option applies best practices to geometric models to try to create the best possible mesh for each geometry. This may or may not overwrite the user defined attributes. By using the slider or manual settings the curved surface mesh can be optimised for resolution or mesh size. [42]

From the initial mesh settings Auto, Classic and Auto with Ansys prime were tested. Also, the effect of curved surface mesh accuracy was tested by using auto mesh method and changing the curve mesh resolution from coarse to fine.

A configuration that would be as accurate as possible with no significant increase on simulation time was chosen based on the solder ball simulations and mesh variations simulations. These settings were then used to simulate two more cases to see if the chosen settings would provide similarly accurate solutions for these cases. All the simulation cases are listed in Table 10. The simulations were done on a LSF (Load Sharing Facility) server with 14 cores and 6 GB of memory per core. The simulations were divided into six tasks for faster solution time.

Table 10. Simulation cases

Trace	Termination	Mesh (method, slider)	Solder ball
V_{out}	Open/1 µF	Auto, middle	Default
			Height sweep: 0.0025mm-0.25mm
			Width sweep: 0.1mm-1.7mm
		Auto with prime, middle	Height 0.025 mm Width 1.6 mm
		Auto, left	Height 0.025 mm Width 1.6 mm
		Auto, right	Height 0.025 mm Width 1.6 mm
		Auto TLM, middle	Height 0.025 mm Width 1.6 mm
		Auto RLCG, middle	Height 0.025 mm Width 1.6 mm
		Classic, middle	Height 0.025 mm Width 1.6 mm
V_{out}	1 µF + 22 µF	Auto, middle	Height 0.025 mm Width 1.6 mm
VCCA	Open/0.47 µF	Auto, middle	Custom for each pad

The first V_{out} comparison was measured and simulated between one local capacitor and one POL capacitor. In the simulation this was done by placing the sources and sinks as in Figure 38 with the green solder balls (N) being sources and red (P) being sinks. The blue area is the V_{out} plane and the brown rectangles inside of it are ground. The measurement was taken by placing

the positive probe leads to the positive pad (P) of the capacitor C117 and negative leads to the negative pad (N) of the same capacitor.

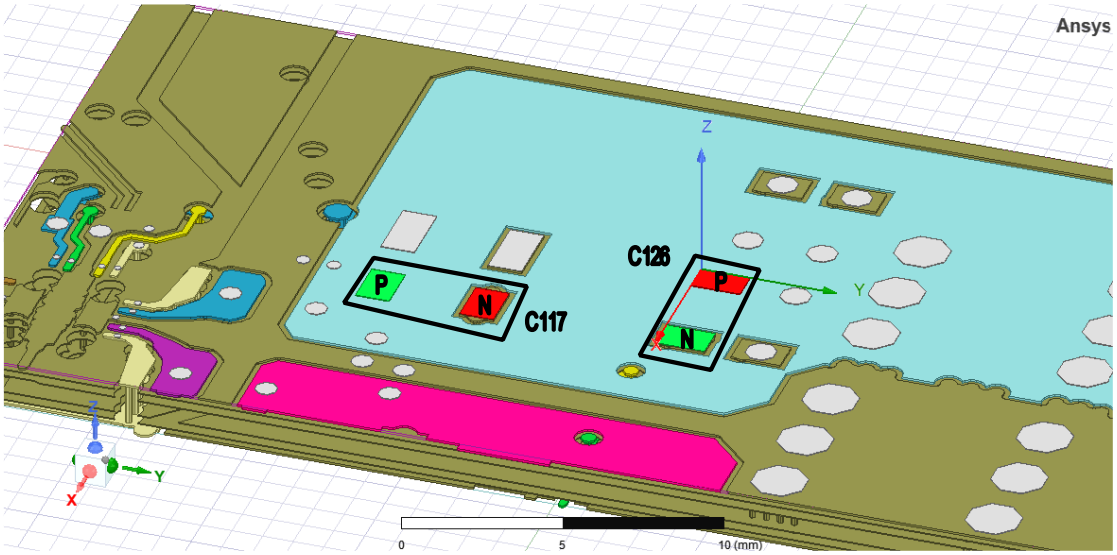


Figure 38. V_{out} with one capacitor extraction setup. Sources are in green (N), and sinks are in red (P).

The same V_{out} plane was used to evaluate the accuracy of the simulation when using two capacitors. In simulations the capacitors were first placed on the same port, which was the local port. In the second case the capacitors were placed as in the EVM which is one in local and one in POL. This also shows how big of an impact it makes to model the capacitor placement as it is in the EVM or if the capacitors could be placed at the same port. This comparison was measured and simulated by placing the positive lead to pad P of C118 and negative lead to pad N of C118 in Figure 39. Q3D can only handle one sink in each net. Since there are more than two excitations on each plane, there had to be two sources and one sink. Although this does not seem to be the exact flow of the current, placing the excitations in this manner does not affect the results. This setup was used because with this the accuracy of the model with two capacitors was tested and placing the probes over one capacitor would make that too dominant.

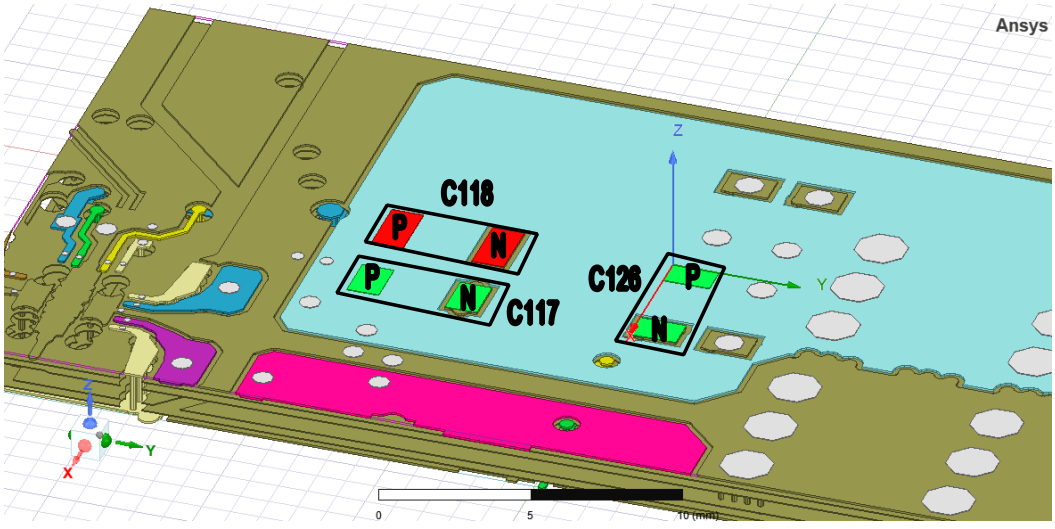


Figure 39. V_{out} with two capacitors extraction setup. Sources are in green, and sinks are in red.

In the VCCA comparison the excitations were placed as in Figure 40. From these the probes were placed on the narrower green solder ball labelled VCCA which is the VCCA pin of the PMIC and larger red solder ball labelled GND which is the ground pad of the PMIC. The pink area is the ground, and the green is the VCCA plane. The VCCA plane extents much further to above this figure. It continues all the way to the edge of the PCB and is not shown due to the sources and sinks being much smaller and thus they would not show properly.

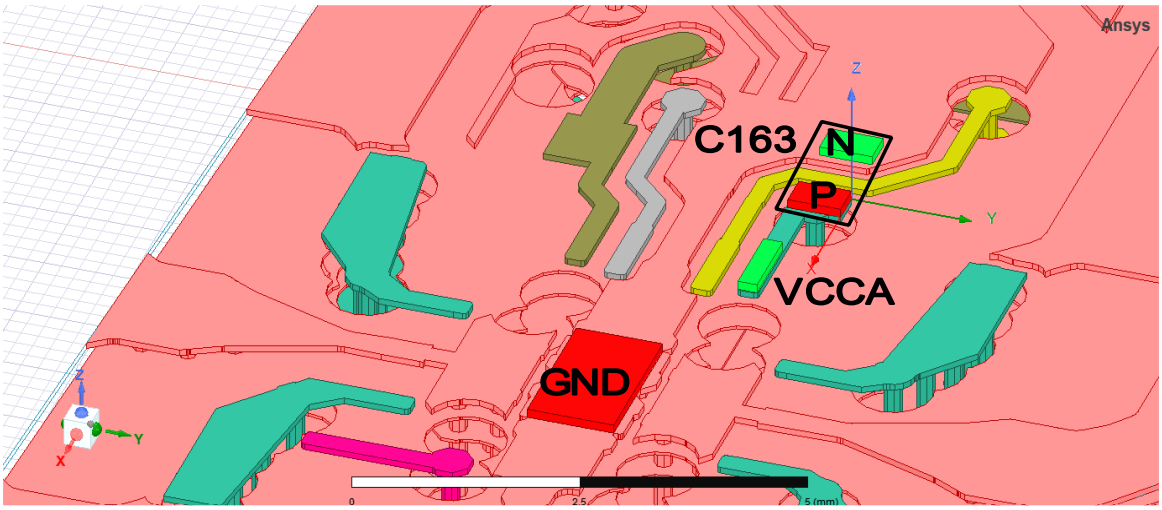


Figure 40. VCCA extraction setup. Sources are in green and sinks in red.

The V_{out} extractions could have been done on any of the four buck output planes since they are geometrically the same. The only differences are that in two outputs there are more capacitors due to the higher output power, but this would have been insignificant since at maximum two of these were populated for these simulations and measurements.

6 RESULTS

The results for impedance simulations and measurements are shown in this section in the form of S_{21} parameters. The placement of the probes for the following comparisons are shown in Figure 38, Figure 39 and Figure 40 with descriptions preceding each figure. The schematics for output and input are shown in Figure 12 and Figure 15, respectively.

6.1 Solder balls and mesh options

All the measurements and simulations in this section were done using the setup shown in Figure 38 which shows the V_{out} plane of one of the buck regulator outputs. The probe leads were soldered to the pads of C117 as well as with and without C126 being populated. There was a solder ball on each capacitor pad in all simulation cases.

Figure 41 shows the effect of solder ball height to the loop inductance from local capacitor to POL capacitor, C117 and C126, respectively. Here it can be seen that the inductance increases quite linearly as a function of solder ball height if the spur around 25 µm is ignored. This could be due to some modelling error in the simulation. The difference between highest and lowest inductance is about 7 % which is not significant in this model, but in a model with more solder balls in the loop the result will be more noticeable.

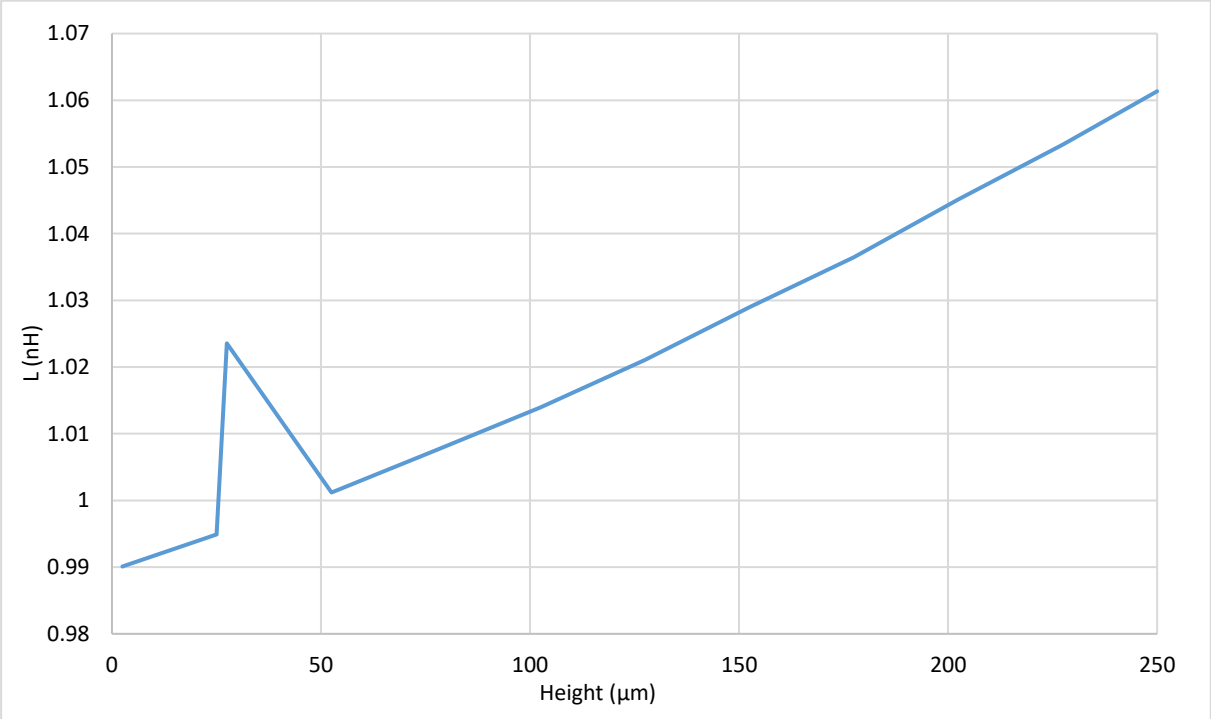


Figure 41. Loop inductance from local to POL capacitor as a function of solder ball height.

In Figure 42 one can see the effect of the solder ball height to the impedance with a measurement result as a reference. In this case the capacitor was not populated. Up to about 1 MHz the S_{21}, which can be interpreted as gain, is 0 dB. When the capacitance between the V_{out} and the ground plane start to be significant, the signal reaching the probe decreases thus lowering the gain and therefore impedance.

The solder ball height does not contribute much to the frequency response. Only the default solder ball simulation shows some variation to the results, and this is probably due to being

significantly higher than the manually created at 1.1 mm vs maximum of 0.25 mm, respectively. The simulations are accurate to about 20 MHz while the expectation was that the simulation should be accurate to about 100 MHz. Even the default solder ball simulation, which is the most accurate, is not significantly better than any other simulation. However, the accuracy is good for the application since very few frequency components should be above 20 MHz.

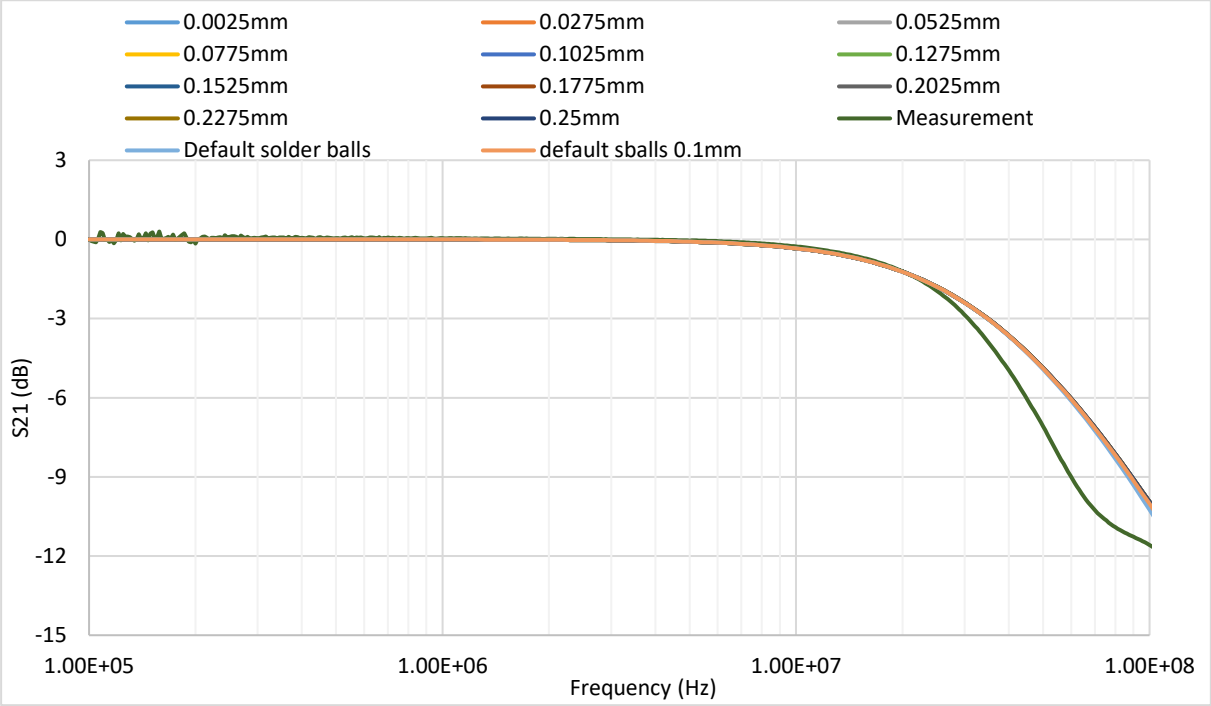


Figure 42. The effect of solder ball height to the impedance profile.

Figure 43 shows the loop inductance dependency on the solder ball widths. The width was swept from 0.1 mm to 1.7 mm with 0.4 mm steps. Solder ball height was kept at 0.025 mm. The trend is as expected with inductance decreasing with increasing solder ball width since there is more volume for current to flow in. The results at 0.9 mm and 1.7 mm widths are a bit off from this hypothesis but that could be because of modelling accuracy. It could also be that the 0.5 mm result is not accurate. The important outcome from this is that the width does contribute to the inductance significantly with difference of about 40 % between highest and lowest value. This change in inductance could be significant in post simulations using this model but in Figure 44 this does not affect the impedance profile significantly.

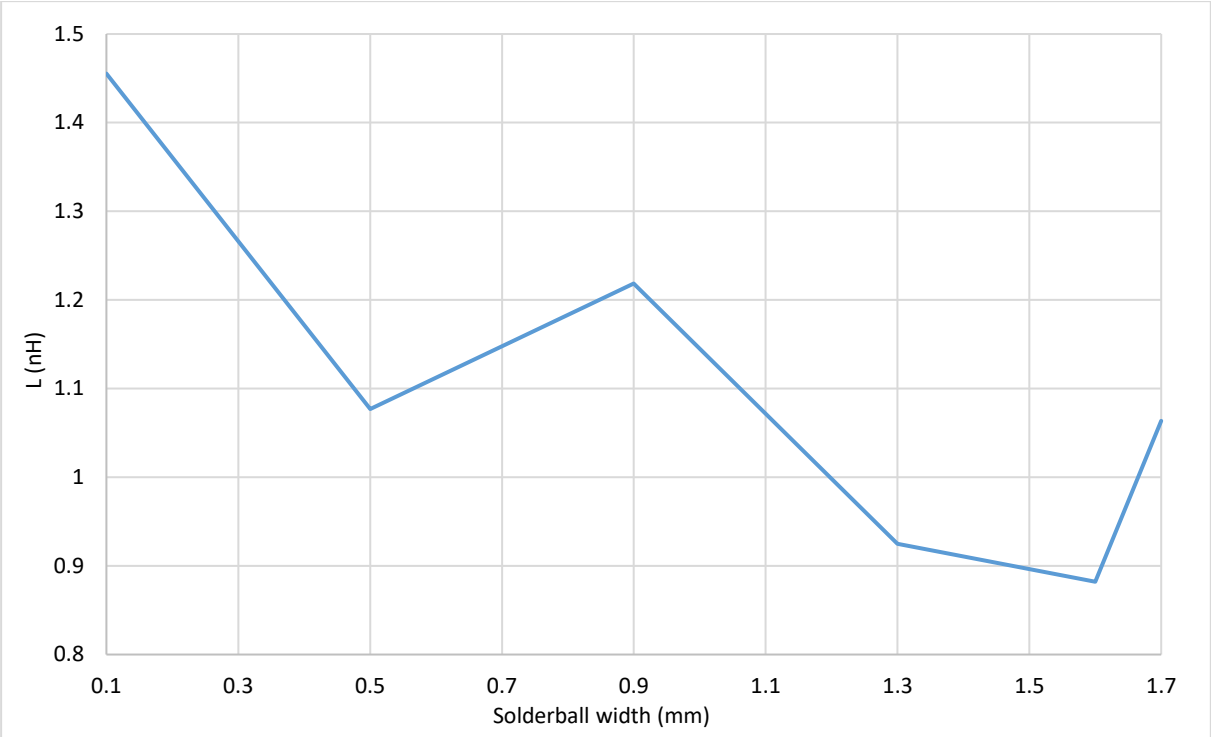


Figure 43. Loop inductance from local to POL capacitor as a function of solder ball width.

The effect of solder ball width was evaluated in the same way as height and the result can be seen in Figure 44. Even though the effect of solder ball width to inductance is high, it does not affect the impedance profile significantly. All the variations are accurate to about 20 MHz. The model is not as accurate between 20 MHz and 100 MHz, but still the trend is correct so the model can be concluded to be quite accurate in this scenario.

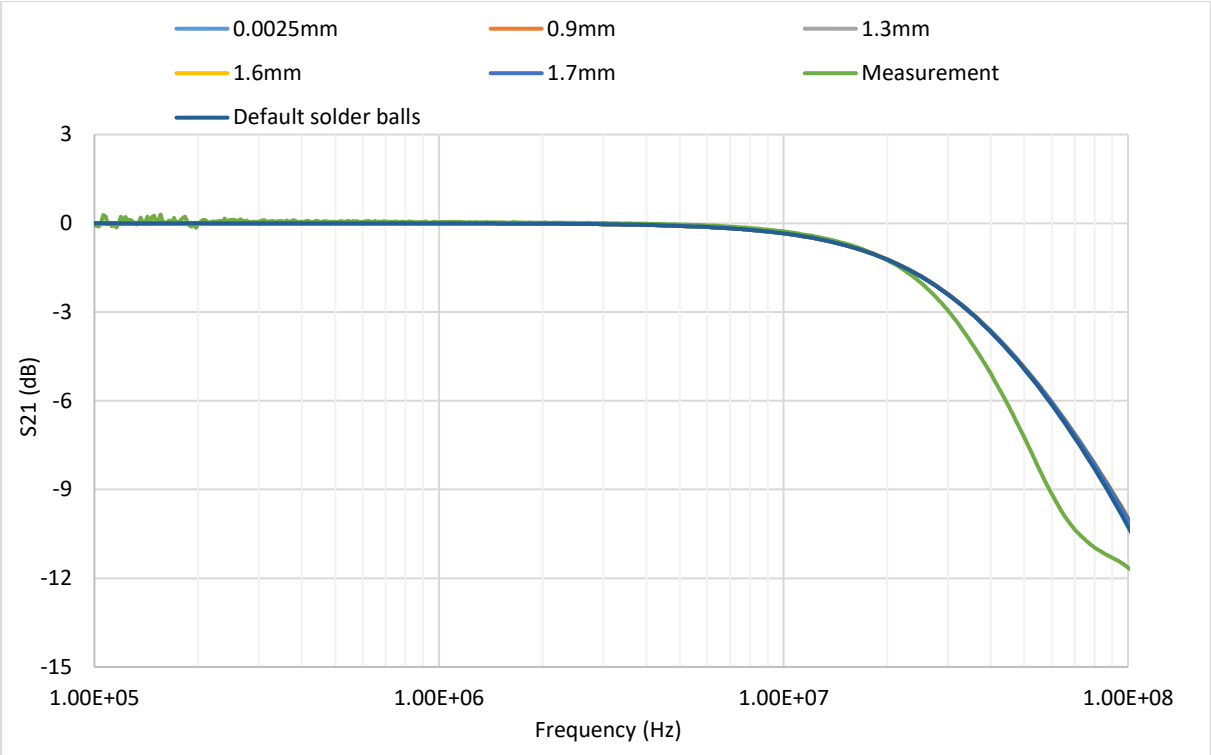


Figure 44. The effect of solder ball width to the impedance profile.

It should be noted that there are more differences in the higher frequencies in the solder ball variations and mesh variations. As an example, the frequency range from 100 MHz to 1 GHz is shown in Figure 45. Within these results more variation can be seen between the different values but since these frequencies were considered unnecessarily high for this use case they are not evaluated further. Also, the Accuracy of Q3D drops at these higher frequencies so much that none of the options are even close to the measurement as can be seen in Figure 45. From this figure the inductance first starts to increase the impedance at around 200 MHz with another increase in impedance due to inductance at 700 MHz.

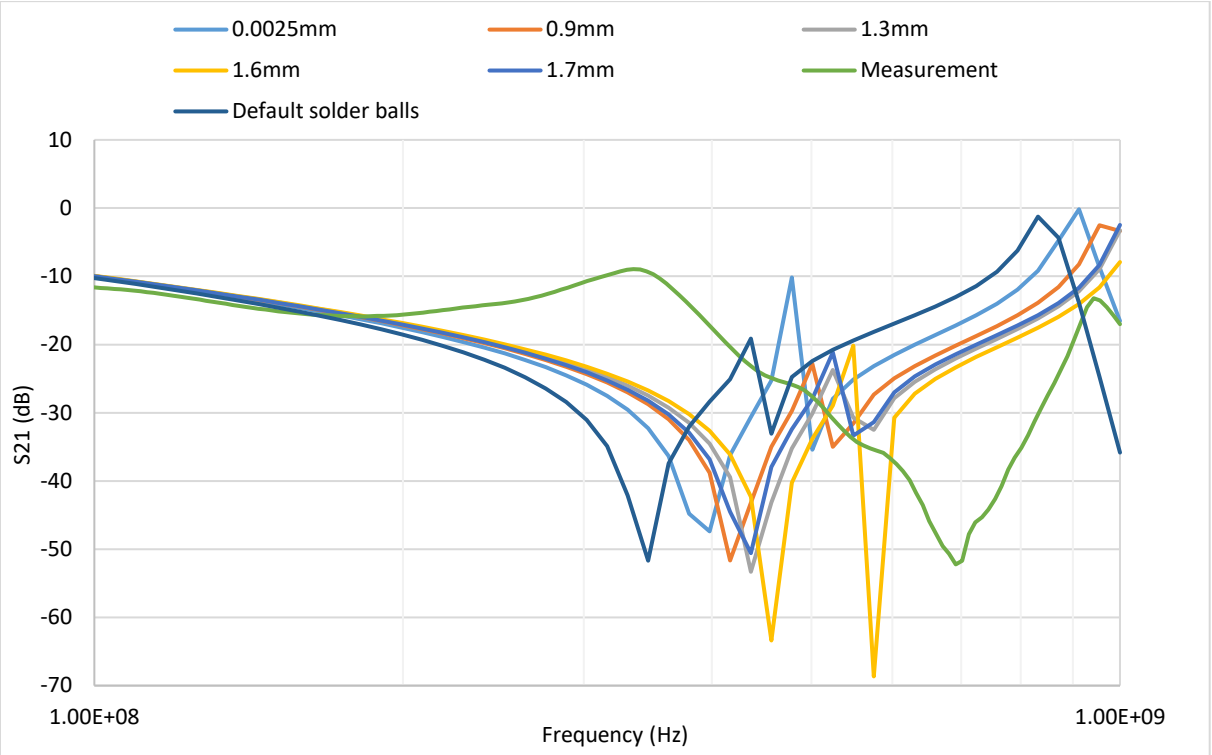


Figure 45. Higher frequencies of solder ball width sweep.

The effect of solder ball height and width was also evaluated when capacitor C126 is populated at the POL. This was done to determine the accuracy of the actual soldering modelling. The same solder ball width and height sweeps were used as previously but now in Circuit there was an ideal capacitor connected between the POL positive and negative nodes. The capacitance of the capacitor used was 1 µF and for the measurements a 1 µF MLCC (Multilayer Ceramic Capacitor) with a size of 1206 was used.

In Figure 46 the frequency response with a capacitor with different solder ball heights is shown. The capacitance decreases the impedance up to about 5 MHz after which the inductance in the traces and solder balls start to increase the impedance. The conclusion is similar to the one without the capacitor, but here the default solder ball is the furthest away from the measured curve though the magnitude at the resonant frequency is closer to the measured value than with the custom solder balls. The large difference between the custom solder balls and the default solder ball can be attributed to the fact that the default solder ball is much higher than the custom solder balls at 1.1 mm vs 0.25 mm as the highest custom solder ball. This is confirmed with another simulation with the default solder ball shape but with a height of 0.1 mm. This gives results closer to the custom solder ball results. Even though the height increases by factor of 100 between lowest and highest custom solder ball, the difference is not that significant. From these results it can be concluded that the solder ball height starts to matter when it gets closer to 1 mm. If the height is around 0.1 mm the results are always quite close to each other and differing from the measurement only at the resonant frequency magnitude.

With equation (21) the inductance in series with the capacitor can be estimated to be around 1 nH when considering the SRF to be 5 MHz. When considering the SIMPLIS PM and GM results in Table 5 and Table 6 with different inductances, 1 nH is low enough inductance to help keep the converter stable.

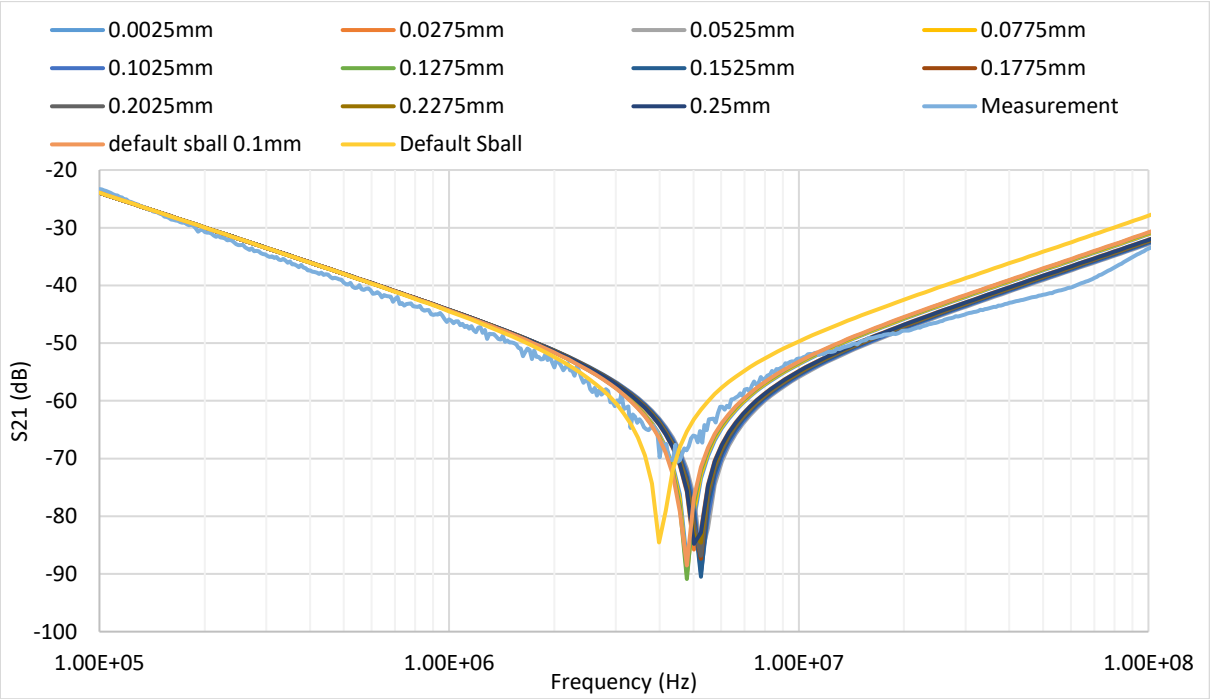


Figure 46. Solder ball height sweep with 1 µF MLCC connected.

Figure 47 shows the comparison between measurement and the solder ball width at different values. Again, the width does not play a significant role in the accuracy of the extraction. It should be noted that the width or the height does not have any pattern in the way they affect the simulation result. The two extreme cases of 0.5 mm and 1.7 mm have the resonant frequency lower than any other simulations. Thus, there does not seem to be any clear dependence between the resonant frequency and width or height of the solder balls. The explanation for this is not clear but it might be due to the proportionally small change in the geometry, which is difficult to model precisely, therefore not following any clear rule. Due to this fact, it is difficult to draw any clear conclusion about the solder ball dimensions other than to use a height of around 0.1 mm and width about the size of the pad.

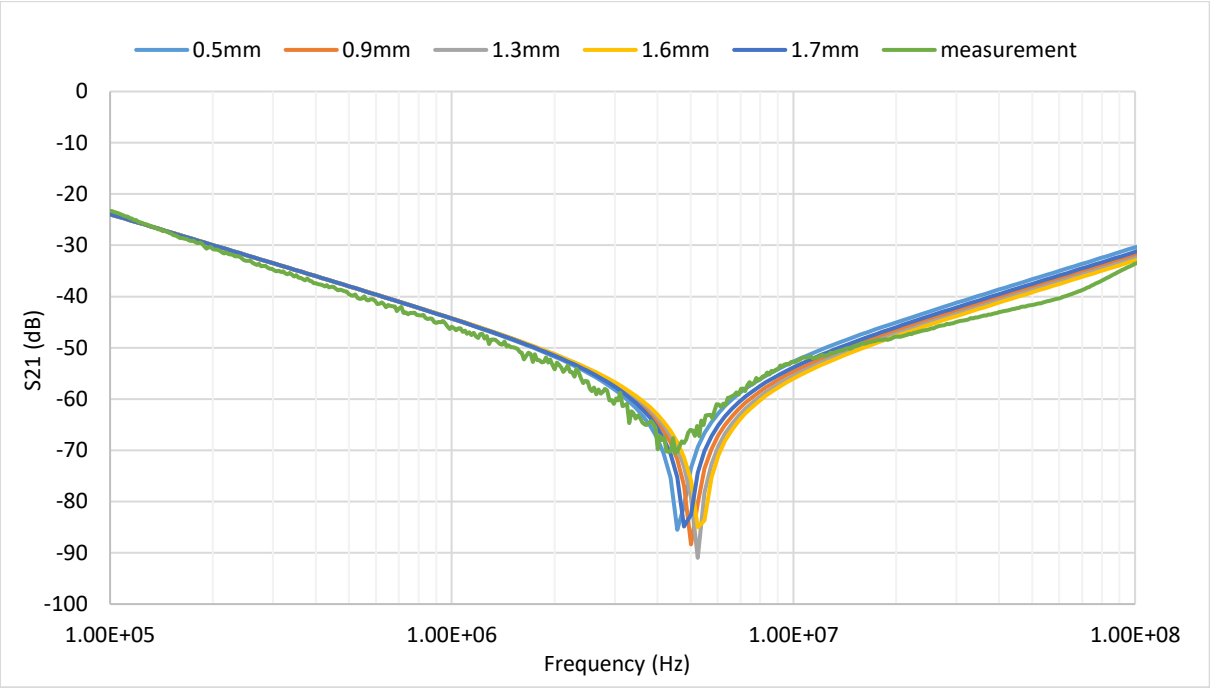


Figure 47. Solder ball height sweep with 1 µF MLCC connected.

The different meshing options and frequency sweep were tested in the same setup as the solder ball properties and the results without a capacitor are shown in Figure 48 and with a 1 µF MLCC in Figure 49. The results without a capacitor show similar trend in comparison with the solder ball properties. There is no practical difference in this frequency range between meshing options. The only option that shows slight variation is the frequency sweep extraction, but the difference is insignificant.

Bigger difference can be seen when using AC resistance in place of DC resistance when exporting the equivalent circuit. The lower frequencies magnitude is a bit lower than with the DC resistance options. This might be due to the AC resistance being lower than the DC resistance in these frequencies. After 3 MHz the AC resistance simulation is a bit more accurate, but not significantly.

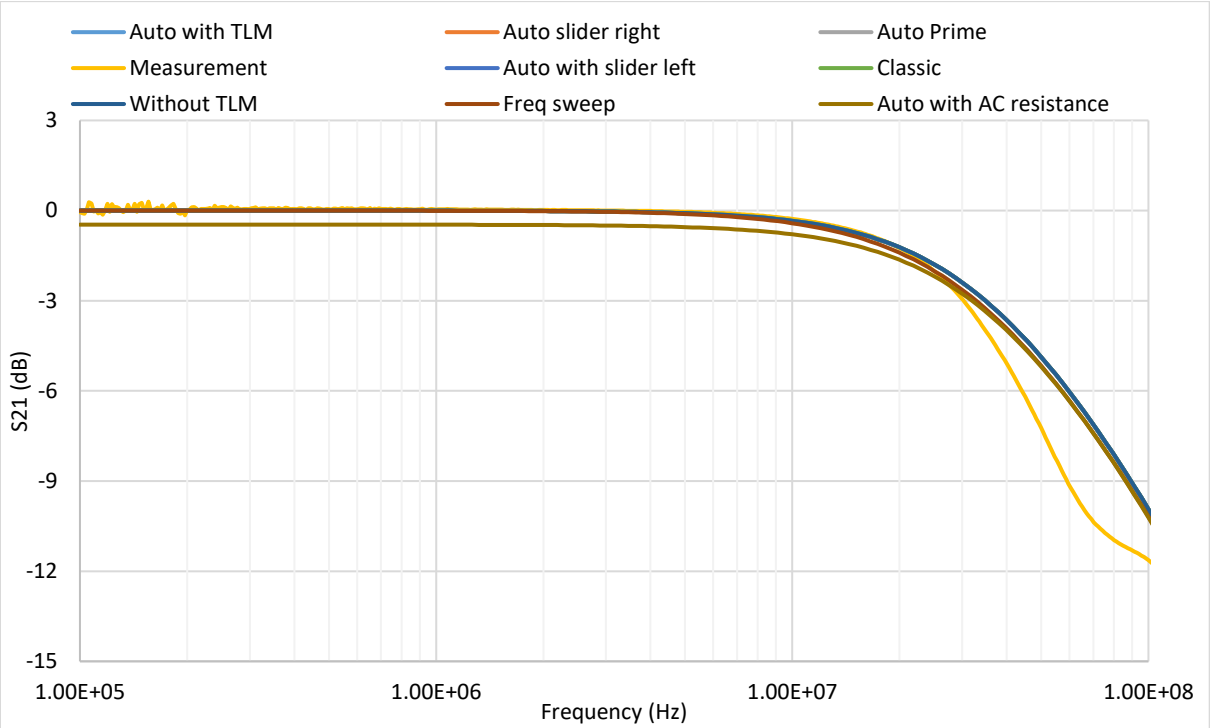


Figure 48. Mesh options and frequency sweep comparison.

The results of the different meshing options when a capacitor C126 was placed in the POL are shown in Figure 49. The only settings showing a significant difference in accuracy were the frequency sweep and AC resistance option. The frequency sweep is either more accurate or as accurate as the others except for the range from about 15 MHz to 40 MHz. The frequency sweep simulation modelled the resonant frequency more accurately, but this might not be true for different cases.

Here the AC resistance option is more accurate at least in terms of magnitude than the DC resistance simulations. The shape of the impedance curve resembles the measurement well except that the resonant frequency is a bit off. It can still be considered to be more accurate if the accuracy of the resonant frequency is not of importance. The accuracy of capacitors also must be considered with capacitors having tolerances up to +/- 20 %. The measurement resonant frequency is around 4.5 MHz, and the simulation is 5.5 MHz so the difference is within 20 % thus at least some of the difference can be attributed to the tolerance.

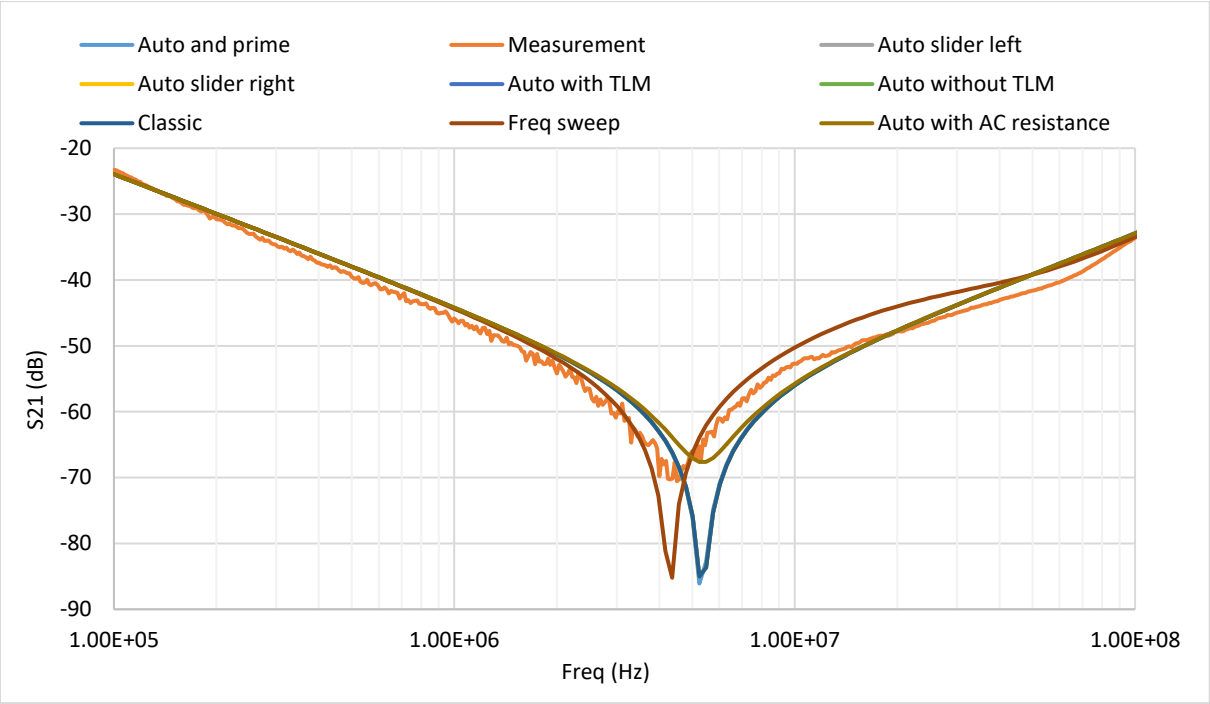


Figure 49. Mesh options and frequency sweep comparison with 1 µF MLCC.

The calculation times for the different extraction setup configurations were saved and are shown in Table 11. This solution time is the time for the Ansys Q3D simulation which is the time to calculate a solution from which the equivalent circuit model can be exported. The time to solution was captured to see how much more time it takes to get more accurate results and this way hopefully to determine a good middle ground between accuracy and solution time. The solution time for each different solder ball size was not captured since the solder ball sizes should not have a significant impact on the solution time.

Looking at the impedance results shown previously, it can be estimated that the only option that had different results is the frequency sweep. The frequency sweep took 51 minutes to get a solution which is significantly higher than the below 20 minutes of all the other options without prime meshing. Using the prime mesh option did not have a large impact in this use case but the time to solution was by far the highest at 1 hour and 26 minutes. This is why it cannot even be considered as a viable option for these extractions.

There is a benefit in using the frequency sweep solution since it is more accurate than the one frequency solution through almost the entire frequency range used. Since it is significantly slower to calculate it must be determined if this increase in accuracy is needed for the use case. For these simulations it was not considered to be enough of an improvement in accuracy and thus is not used. The configuration used in further simulations is highlighted in Table 11. In addition to these settings the exporting of the equivalent circuit is done with options shown in Table 12.

Table 11. Simulation time with different setup configurations using 6 cores

Solution frequency	Mesh	Solder balls	TLM	Prime mesh	Slider	Time
100 MHz	Auto	Custom	Yes	No	Middle	19 min
					Right	18 min
					Left	13 min
				Yes	Middle	1h 26 min
			No	No	Middle	14 min
		Default	Yes	No	Middle	13 min
	Classic	Custom	Yes	No	Middle	14 min
Sweep	Auto	Custom	Yes	No	Middle	51 min

Table 12. Equivalent circuit export options

Capacitance
Conductance
AC inductance
AC resistance
5 cells

6.2 V_{out} with two capacitors and VCCA loop

In this section the results of V_{out} case with two capacitors and the VCCA loop are shown. The setups for these can be seen in Figure 39 and Figure 40, respectively. In the two-capacitor case, the capacitors C117 and C127 were populated and the VCCA comparison was done with and without capacitor C163. The probe leads in two-capacitor comparison were connected to the positive and negative pads of capacitor C118. The probe leads in VCCA loop measurement were placed on the VCCA and the ground pins of the device.

In Figure 50 is shown the comparison between simulations and measurement when using two capacitors, C117 and C126 in the V_{out} plane. In the simulation where two capacitors are placed in the same port resistance and inductance must be placed between the capacitor ports or the larger capacitor will dominate the impedance. In this case, the resistance was 10 mΩ and inductance 0.1 nH which were placed in series between both the positive and negative legs. This was also simulated with exaggerated values which were 100 mΩ and 1 nH. In the other simulations no added impedance was used.

Up to 4 MHz the simulation with exaggerated added impedance is the most accurate and frequencies above this are the furthest away from the measurement. Overall, the most accurate simulation is the one where capacitors were placed on their actual ports and AC resistance was used. It does not accurately model the two resonant frequencies at 4.5 MHz and 7 MHz in the measurement. It does have these same spikes, but they are shifted in the frequency while still having about the correct magnitude for both spikes. The spikes are at the same frequencies in the simulation using DC resistance as with AC resistance, but the magnitude is off by a considerable margin. As with the previous results it can be concluded that the use of AC resistance is more accurate than using DC resistance by a significant amount. Although the modelling could be done using one port where all capacitors are connected and inserting some parasitic impedance between them manually, it is an educated guess how much should be used. It is much simpler to model at least the local and POL capacitor placement individually which also gives more accurate results.

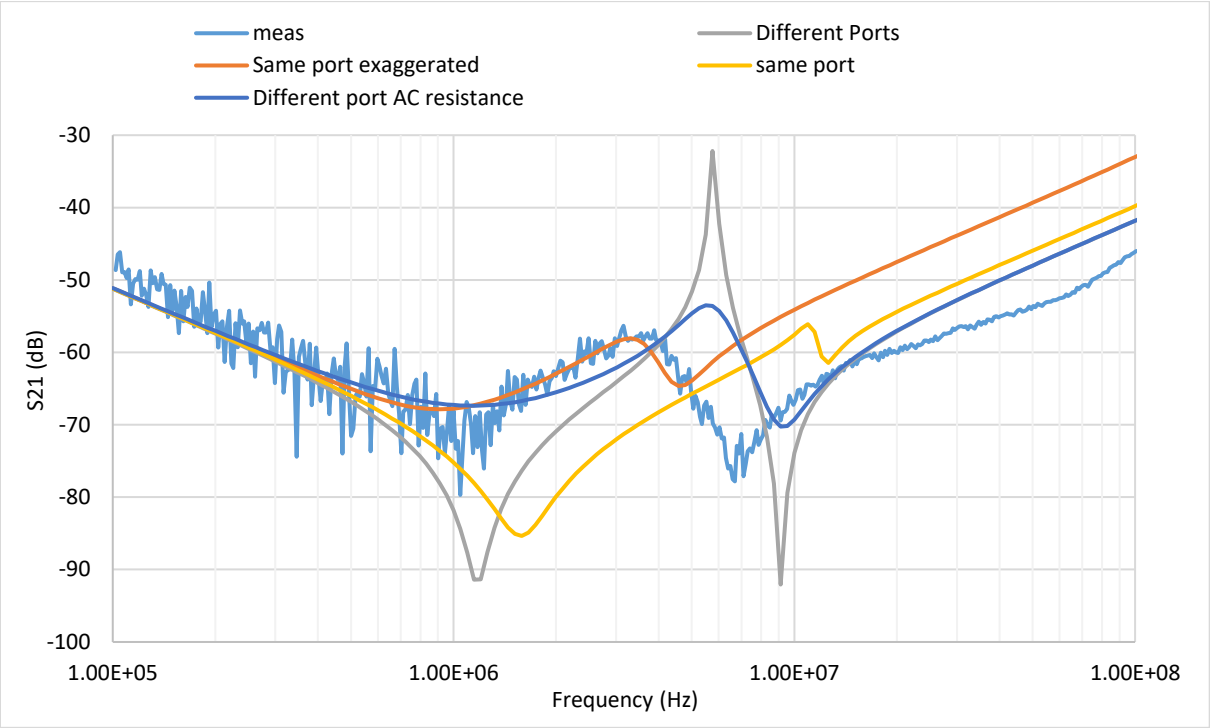


Figure 50. Comparison of different placements of a 1 µF and 22 µF MLCC.

The measurement and simulation comparison for the case without the capacitor C163 can be seen in Figure 51. The result is like the V_{out} with open termination, but the simulation matches the measurement up to about 5 MHz when with the V_{out} they matched up to 30 MHz. After this the simulation magnitude starts to decrease just like the measurement but not as fast due to the capacitance between the VCCA and ground planes.

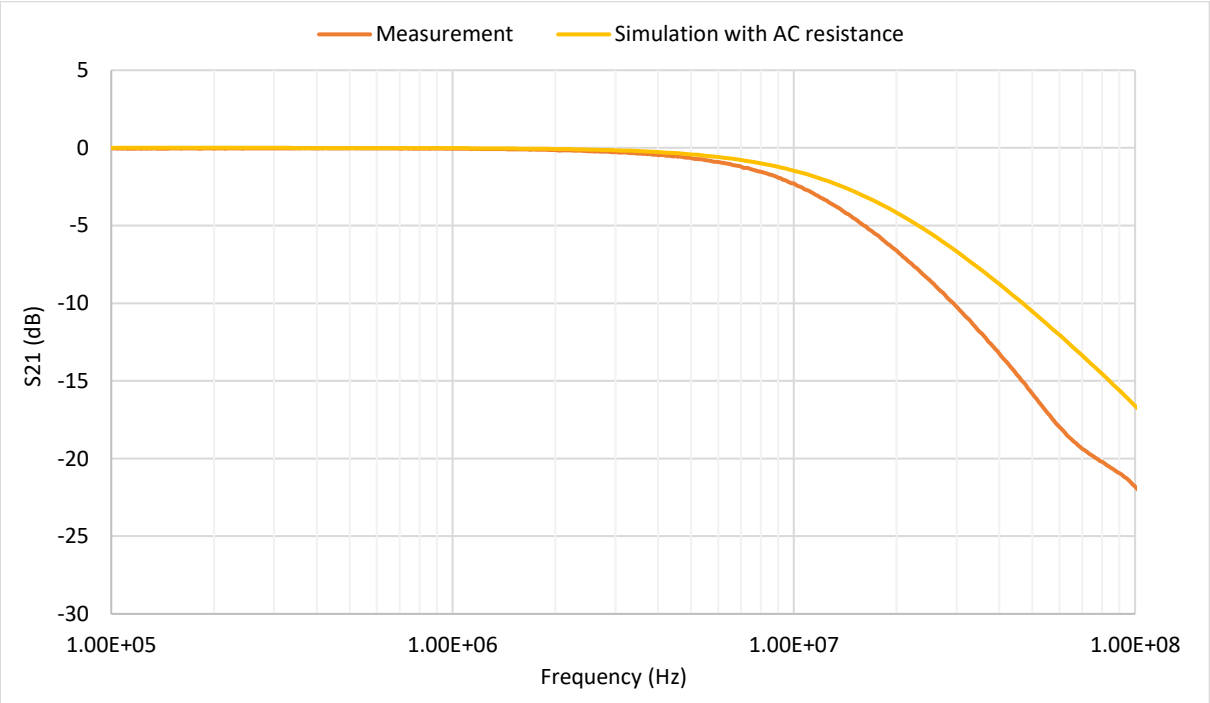


Figure 51. VCCA measurement vs. simulation taken between VCCA and ground pins with open termination.

The VCCA plane measurement and simulation comparison is shown in Figure 52 when 0.47 µF capacitor was populated at C163. The capacitance of the capacitor decreases the impedance up to about 10 MHz after which the trace and solder inductance start to increase the impedance. The simulation matches the measurement well with only a slight difference at 100 kHz, the resonant frequency at 8 MHz and above 30 MHz. This simulation result is the most accurate when comparing to the measurement of the cases simulated in this study. Reason for the better accuracy is not known since all the simulations were conducted with the same methodology and measurement setup did not change other than for the inspected trace. The different accuracy might come down to the different geometry of the traces and pads when compared to the V_{out} plane. These geometries are shown in Figure 40 and Figure 38, respectively.

From the SRF seen in Figure 52 at around 8 MHz the inductance can be calculated with equation (21) using the capacitance of 470 nF to be about 0.84 nH. This is close to the extracted value of 1.04 nH in Table 4. The behaviour of the device was not evaluated with different input inductances so it cannot be precisely evaluated how good of a performance this layout gives. The inductance is quite low so it probably is sufficient.

Since this result is accurate up to 100 MHz, which is the highest frequency of interest for this study, the frequencies up to 1 GHz are also evaluated. Also, frequencies in the input reach higher values than in the output due to the fast switching of the device. This is to understand possibly the best-case accuracy at the higher frequencies. Since the switching action of the device has rise and fall times in the nanosecond region, the higher frequencies are more of interest with the input than with the output. The accuracy is good up to about 350 MHz if not considering the spurs around 200 MHz. After 350 MHz the shape of the curve resembles the measurement but is highly exaggerated. This is on par with the previous studies suggesting that Q3D is accurate up to about 300 MHz.

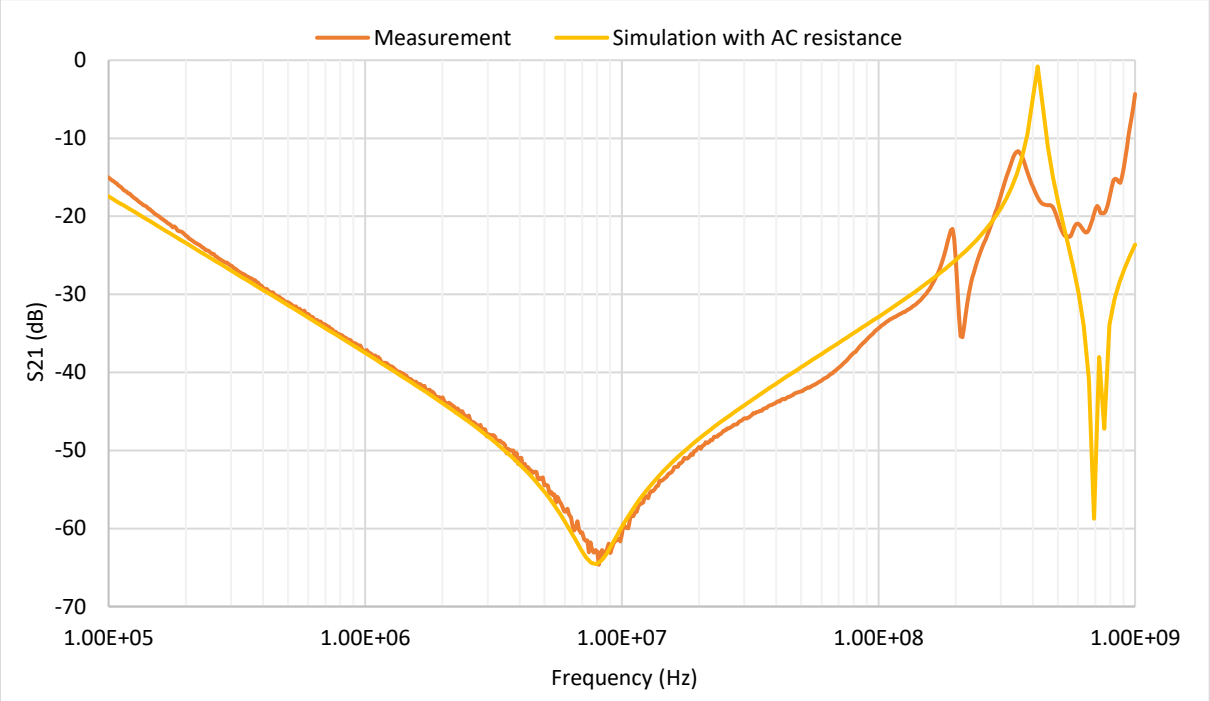


Figure 52. VCCA measurement vs. simulation with 0.47 µF MLCC.

The relative difference between the most accurate simulation and the measurement for each case can be seen in Table 13. These were calculated using a Python script with a condition that

S_{21} must be greater than one to eliminate the inaccuracies of the measurement. With S_{21} being smaller than one, the percentual difference between measurement and simulation could be very large but would not matter since the difference could be insignificant to the actual use case.

The worst performing simulation was the VCCA simulation with no capacitor with an average error of 34.3 % while the best performing simulation was the VCCA with capacitor with average error of only 3.3 %. The average minimum error was 2.9 %, average maximum error 27.3 % and average of the average error was 13.5 %.

Table 13. Relative differences between measurement and the most accurate simulation

Simulation	Min error (%)	Max error (%)	Average error (%)	Min error frequency (MHz)	Max error frequency (MHz)
Sball height	0.38	33.7	20.9	18.3	57.9
Sball height cap	0.13	29.1	4.8	0.13	4.8
Sball width	0.6	33.6	20.7	19.1	20.7
Sball width cap	0.04	21.7	4.9	10.0	4.6
Mesh	0.21	34.6	21.7	18.3	57.9
Mesh cap	0.1	11.7	4.0	0.13	4.0
Two caps	0.2	26.1	6.5	13.8	6.6
VCCA	23.8	38.8	34.3	100.0	12.7
VCCA cap	0.39	16.1	3.3	1.9	0.1

The maximum error between simulation and measurement was very high in some simulations with the maximum being 38.8 %. However, in many cases the average was much lower, with the highest average error being 34.3 % and rest below 22 %. The error was greatest in simulations without the capacitor probably due to the small values being simulated and measured. The simulations with capacitors were much closer to the measurement, possibly because the capacitors' capacitances were much higher than the capacitance of the PCB and they would this way dominate the measurements and simulations.

The resonant frequencies in the simulations were always close to the measured frequencies. Since there was no added inductance or resistance in the circuit simulations, this indicates that the dominating inductance comes from the PCB and the solder junction of the component and the PCB. This would show that the inductance values simulated are close to the actual inductances in the PCB.

The average of the average errors of 13.5 % is close to what have been seen in previous studies ([37]–[39]) bringing even more reliability to these results. The average results in this study are on the more accurate side, when comparing with the previous studies. This is likely due to the simpler geometries used in this study.

7 DISCUSSION

The extraction models and the simulations performed as anticipated based on previous studies, and in some cases even better. The simulations correctly capture the main frequency response of the PCB, but finer details of the measurements are not present in the simulations. It was expected that more variation would be seen between different extraction options and PCB geometries, but this was not the case. The differences between the different extraction options were not as large as was initially thought. This study manages to highlight the main methods on how the extraction should be conducted to get the best results.

One of the biggest takeaways from this study is that the use of AC resistance greatly increases the accuracy of the models compared to any other setting tested. Using frequency sweep instead of a single point extraction also increases the accuracy but at the cost of increased extraction time which might be a reason not to use this option. The different meshing options did not provide any significant differences in the simulation accuracies. This is probably because the model only included the copper traces with no external components, which can be difficult to model. Also, the studied traces were large and quite simple so even the simplest mesh provided good enough representation of the actual geometry.

When comparing with previous studies, the results seen in this thesis follow the findings. Q3D is most accurate up to 100 MHz after which the accuracy starts to decrease. In some cases, the accuracy was good up to about 350 MHz which was the upper limit shown in some studies. The average accuracy of the modelling in previous studies was from about 10 % to 40 % which is also the case in this study. This study shows that the average error varied between 3.3 % and 34.3 %.

In this study there was no time to evaluate the accuracy of the extracted resistance, capacitance, and inductance individually, thus only the impedance frequency response was considered. This could have shown better the differences between each extraction option and whether some of these parameters would be closer to measurement than others. Studying this was also limited by the measurement equipment which was not sophisticated enough to directly capture these parameters. Extracting these parameters would have been possible but there was no time to study how to do this and execute these measurements. This could be an interesting topic for further research.

When estimating the inductance between local and POL capacitors using SRF, the inductance was around 1 nH. This inductance is low enough to help keep the device stable. The VCCA inductance was simulated to be 1.04 nH and calculated to be about 0.84 nH, therefore probably achieving good performance for this device. Though more thorough study and evaluation should be conducted to draw final conclusions of the performance.

The measurement setup was established from the ground up for this study so it might be possible that there is a way to get better measurements with the same setup. Although there was prior knowledge of the spectrum analyser, it had not been used for impedance measurements previously, so it took time to figure out how to setup the measurement properly and get reasonable results. The measurements and simulations showed similar results meaning that the measurements were conducted correctly but there could still be room for improvement. This would be important if the impedance or the parasitic values would be investigated more closely.

When it comes to the investigation of accuracy of Ansys Q3D parasitic models, this study does not necessarily provide any new information, but it still manages to further confirm the results of previous studies. The main goal of this study was to investigate the different options of Ansys Q3D for conducting parasitic extraction that had not been identified in any of the previous papers studied for this process and this study succeeds in providing such insights.

During this study it was discovered that the extraction process includes a lot of manual work which can in some cases be as much as the calculation times itself. The nature of this manual work includes tasks like cutting out the region of interest, placing solder balls and assigning the ports. These could be automated with PyAnsys which is a Python based project aiming to automate different workflows inside of Ansys products, including Electronics Desktop, which includes Q3D.

8 SUMMARY

PCBs have parasitic properties in the form of resistance, capacitance and inductance which decrease the performance of the PCB and ultimately the entire system. Usually, the inductance is the single most important parasitic property that must be considered when designing a PCB. Parasitic properties cause different problems such as voltage drop, rail collapse, ground bounce, cross talk and EMI. With few simple rules these problems can be mitigated.

The parasitic properties of a PCB can be extracted using specialised software or through measurements. From the extraction a parasitic model can be created in the form of S-parameters or RLCG equivalent circuit. Extracting these properties with software in the design phase is more time efficient and saves money by not having to create multiple prototypes of the same design. Design changes can be made according to the simulations.

An evaluation module PCB for a PMIC was designed for this thesis. In this design the best practices for PCB design were utilized as much as possible to get a well performing EVM. This PCB was used for the measurements and the model was used for the parasitic extraction.

Ansys Q3D was used for the extraction and different options that could affect the accuracy were studied. Based on these options, multiple configurations were picked for the simulations. A measurement setup was established to get measurement data which was used as the reference for the simulations.

The simulations were done in a way which would resemble the real use case the most. The extraction was done in Q3D from where the equivalent circuit model was extracted as .cir file which is used in actual simulations using these models. The equivalent circuit model was imported to Ansys Circuit and a frequency sweep was performed. Two ports were placed as in a regular shunt-through measurement to get comparable results with the measurements. Another method would have been to extract the numerical values for resistance, capacitance and inductance and compare these values to the measured values. This could possibly show more variation between different extraction options. This could also show if different options affect some properties more than others.

The results of this study show that the different extraction options do not offer significant difference in the simulations for this use case. The biggest contributors to the more accurate extractions were the use of AC resistance and frequency sweep. Frequency sweep was discarded due to considerably higher time to solution. The final extraction setup consisted of 100 MHz single point extraction frequency, auto meshing option, custom solder balls and the use of transmission line model for the S-parameter calculation. The equivalent circuit exported consisted of five cells with capacitance, conductance, AC resistance and AC inductance.

The simulation with the highest correlation with measurement was the VCCA simulation with capacitor installed. This offered average error of 3.3 % when the highest average error was 34.3 % which was the VCCA trace with no capacitor. These findings reflect well the results shown in previous studies.

9 REFERENCES

[1] X. Lecoq, A. Lipani, S. Stemmer, and A. Chimeno, “Power integrity Flow for mixed-signal NVM flash IP,” in *2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI)*, 2019, pp. 1–3. doi: 10.1109/SaPIW.2019.8781668.

[2] E. Bogatin, *Signal and power integrity : simplified*, 2nd ed. in Prentice Hall modern semiconductor design series. Upper Saddle River, NJ: Prentice Hall, 2010.

[3] J. R. González-Teodoro, V. Kindl, E. Romero-Cadaval, and R. Asensi, “Analysis of Skin Effect in Single Wire Resistance by Finite Element Methods,” in *2020 IEEE 14th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2020, pp. 19–23. doi: 10.1109/CPE-POWERENG48600.2020.9161540.

[4] H. W. Ott, “Passive Components,” in *Electromagnetic Compatibility Engineering*, 2009, pp. 194–237. doi: https://doi.org/10.1002/9780470508510.ch5.

[5] E. Bogatin and L. D. Smith, *Principles of Power Integrity for PDN Design: Robust and Cost Effective Design for High Speed Digital Products*, 1st ed. Mark Taub, 2017.

[6] I. Novak, K. B. Williams, J. R. Miller, G. Blando, and N. Shannon, “DesignCon East 2011 DC and AC Bias Dependence of Capacitors Including Temperature Dependence.”

[7] S. C. Moldoveanu and V. David, “Mobile Phases and Their Properties,” *Essentials in Modern HPLC Separations*, pp. 363–447, 2013, doi: 10.1016/B978-0-12-385013-3.00007-0.

[8] Y. T. Chen, S. F. Liu, M. H. Chen, and C. H. Hung, “Temperature effects on electrical characterization of high dielectric constant substrates,” *IMPACT Conference 2009 International 3D IC Conference - Proceedings*, pp. 697–700, 2009, doi: 10.1109/IMPACT.2009.5382283.

[9] J. Liu, M. Zhang, and G. Hu, “Analysis of Power Supply And Signal Integrity of High Speed PCB Board,” in *2019 IEEE 8th Joint International Information Technology and Artificial Intelligence Conference (ITAIC)*, 2019, pp. 412–416. doi: 10.1109/ITAIC.2019.8785842.

[10] M. Nagel, S. Race, I. Kovacevic-Badstuebner, T. Ziemann, and U. Grossner, “Virtual PCB Layout Prototyping: Importance of Modeling Gate Driver and Parasitic Capacitances,” in *2022 IEEE Design Methodologies Conference (DMC)*, 2022, pp. 1–5. doi: 10.1109/DMC55175.2022.9906542.

[11] C. F. Yee, “Achieving Minimal PDN Impedance, SSN and Jitter on PCB with Embedded Capacitance Material,” in *2018 IEEE International RF and Microwave Conference (RFM)*, 2018, pp. 155–158. doi: 10.1109/RFM.2018.8846556.

[12] J. A. Ferreira, E. Waffenschmidt, J. Strydom, and J. D. van Wyk, “Embedded capacitance in the PCB of switchmode converters,” in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 2002, pp. 119–123 vol.1. doi: 10.1109/PSEC.2002.1023856.

[13] W. H. Hayt and J. A. Buck, *Engineering electromagnetics*, 8th ed. New York, NY: McGraw-Hill, 2012.

[14] C. Paul, *Inductance Loop and Partial*. 2010. doi: 10.1002/9780470561232.

[15] N. Chen, “Designs of power distribution network for octa-core mobile application processor,” in *2015 IEEE 19th Workshop on Signal and Power Integrity (SPI)*, 2015, pp. 1–4. doi: 10.1109/SaPIW.2015.7237388.

[16] Devender, K. N. Rao, K. Suryanarayana, S. Sarvade, and D. Ramesh, “Electromagnetic interference (EMI) suppression techniques - a case study,” in *Proceedings of the International Conference on Electromagnetic Interference and Compatibility (IEEE Cat. No.02TH8620)*, 2002, pp. 221–225. doi: 10.1109/ICEMIC.2002.1006494.

[17] H. Hui, L. Jia, S. Lingling, and C. Keming, “Design of 2Gb/s LVDS transmitter and 3Gb/s LVDS receiver for optical communication in 0.18μm CMOS technology,” in *2011 China-Japan Joint Microwave Conference*, 2011, pp. 1–3.

[18] J. Lee, J.-W. Lim, S.-J. Song, S.-S. Song, W. Lee, and H.-J. Yoo, “Design and implementation of CMOS LVDS 2.5 Gb/s transmitter and 1.3 Gb/s receiver for optical interconnections,” in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*, 2001, pp. 702–705 vol. 4. doi: 10.1109/ISCAS.2001.922334.

[19] R. G. Bozomitu, V. Cehan, and C. Barabaşa, “A VLSI implementation of a 3Gb/s LVDS transceiver in CMOS technology,” in *2009 15th International Symposium for Design and Technology of Electronics Packages (SIITME)*, 2009, pp. 69–74. doi: 10.1109/SIITME.2009.5407400.

[20] C. Hwang, “Power Integrity Concepts for High-Speed Design on Multi-Layer PCBs,” in *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI)*, 2018, p. PI-1-PI-41. doi: 10.1109/EMCSI.2018.8495312.

[21] S. Park and V. A. Huddar, “Design and Analysis of Power Integrity of DDR5 Dual In-Line Memory Modules,” in *2022 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, 2022, pp. 1–3. doi: 10.1109/EDAPS56906.2022.9995596.

[22] J. Hammer, I. G. Zurbriggen, M. A. Saket, and M. Ordonez, “Low Inductance PCB Layout for GaN Devices: Interleaving Scheme,” in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1537–1542. doi: 10.1109/APEC42165.2021.9487045.

[23] M. I. Montrose, “Additional Design Techniques,” in *Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers*, IEEE, 2000, pp. 211–246. doi: 10.1109/9780470545676.ch8.

[24] T. Steinmetz, M. Helias, G. Wimmer, L. O. Fichte, and M. Clemens, “Electro-quasistatic field simulations based on a discrete electromagnetism formulation,” *IEEE Trans Magn*, vol. 42, no. 4, pp. 755–758, 2006, doi: 10.1109/TMAG.2006.872488.

[25] M. J. Beck, D. L. Parker, and J. R. Hadley, “Quasistatic Solutions versus Full-Wave Solutions of Single-Channel Circular RF Receive Coils on Phantoms of Varying Conductivities at 3 Tesla,” *Concepts Magn Reson Part B Magn Reson Eng*, vol. 2021, p. 6638576, 2021, doi: 10.1155/2021/6638576.

[26] K. H. Dirks, “Quasistationary fields for microelectronic applications,” *Electr. Eng.*, vol. 79, pp. 145–155, 1996.

[27] F. Caspers, “RF engineering basic concepts: S-parameters,” Jan. 2012.

[28] W. A. Davis and K. K. Agarwal, “Appendix D: Two-Port Parameter Conversion,” *Radio Frequency Circuit Design*, pp. 292–295, Apr. 2003, doi: 10.1002/0471200689.APP4.

[29] S. M. Sandler, *Power Integrity: Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems*. McGraw-Hill Education, 2014. [Online]. Available: https://books.google.fi/books?id=FhPHngEACAAJ

[30] D. Hernandez, “Modeling of microwave transmission lines considering frequency-dependent current distribution effects,” 2017.

[31] I. Kovacevic-Badstuebner, U. Grossner, and D. Popescu, *Tools for Broadband Electromagnetic Modeling of Power Semiconductor Packages and External Circuit Layouts*. 2020. doi: 10.1109/ISPSD46842.2020.9170161.

[32] I. Kovacevic-Badstuebner *et al.*, “Broadband Circuit-Oriented Electromagnetic Modeling for Power Electronics: 3-D PEEC Solver vs. RLCG-Solver Rights / license: Creative Commons Attribution 4.0 International Broadband Circuit-Oriented Electromagnetic Modeling for Power Electronics: 3-D PEEC Solver vs. RLCG-Solver,” 2021, doi: 10.3929/ethz-b-000488428.

[33] I. Kovacevic-Badstuebner, D. Romano, G. Antonini, L. Lombardi, and U. Grossner, “Full-Wave Computation of the Electric Field in the Partial Element Equivalent Circuit Method Using Taylor Series Expansion of the Retarded Green’s Function,” *IEEE Trans Microw Theory Tech*, vol. 68, no. 8, pp. 3242–3254, 2020, doi: 10.1109/TMTT.2020.3002812.

[34] I. Kovacevic-Badstuebner, R. Stark, U. Grossner, M. Guacci, and J. W. Kolar, “Parasitic Extraction Procedures for SiC Power Modules,” in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–6.

[35] W. Sun, “Accurate EM simulation of SMT components in RF designs,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 140–143. doi: 10.1109/RFIC.2017.7969037.

[36] C. Che, H. Zhao, Y. Guo, J. Hu, and H. Kim, “Investigation of Segmentation Method for Enhancing High Frequency Simulation Accuracy of Q3D Extractor,” in *IEEE International Conference on Computational Electromagnetics (ICCEM)*, Mar. 2019, pp. 1–3. doi: 10.1109/COMPEM.2019.8779105.

[37] K. Zhang, M. Cai, M. Yun, L. Song, and D. Yang, “Comparison experiment of Parasitic Inductance Extraction of power module based on ANSYS Q3D software,” in *2021 18th China International Forum on Solid State Lighting & 2021 7th International Forum on Wide Bandgap Semiconductors (SSLChina: IFWS)*, 2021, pp. 58–60. doi: 10.1109/SSLChinaIFWS54608.2021.9675224.

[38] P. D. Reigosa, F. Iannuzzo, S. Munk-Nielsen, and F. Blaabjerg, “New layout concepts in MW-scale IGBT modules for higher robustness during normal and abnormal operations,” in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 288–294. doi: 10.1109/APEC.2016.7467886.

[39] F. Sawallich and H. Eckel, “Quantification of ANSYS Q3D Extractor for inductive extraction of power modules,” in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1–4.

[40] W. Teulings, J. L. Schanen, and J. Roudet, “MOSFET switching behaviour under influence of PCB stray inductance,” in *IAS ’96. Conference Record of the 1996*

IEEE Industry Applications Conference Thirty-First IAS Annual Meeting, 1996, pp. 1449–1453 vol.3. doi: 10.1109/IAS.1996.559257.

[41] "Murata SimSurfing." https://ds.murata.co.jp/simsurfing/index.html?lcid=en-us (accessed Aug. 30, 2023).

[42] "Ansys Help." https://ansyshelp.ansys.com (accessed Jul. 03, 2023).

10 APPENDICES

Appendix 1 EVM PMIC side of the schematic

Appendix 2 EVM microcontroller side of the schematic

Appendix 3 PCB top layer (layer 1)

Appendix 4 PCB first ground layer (layer 2)

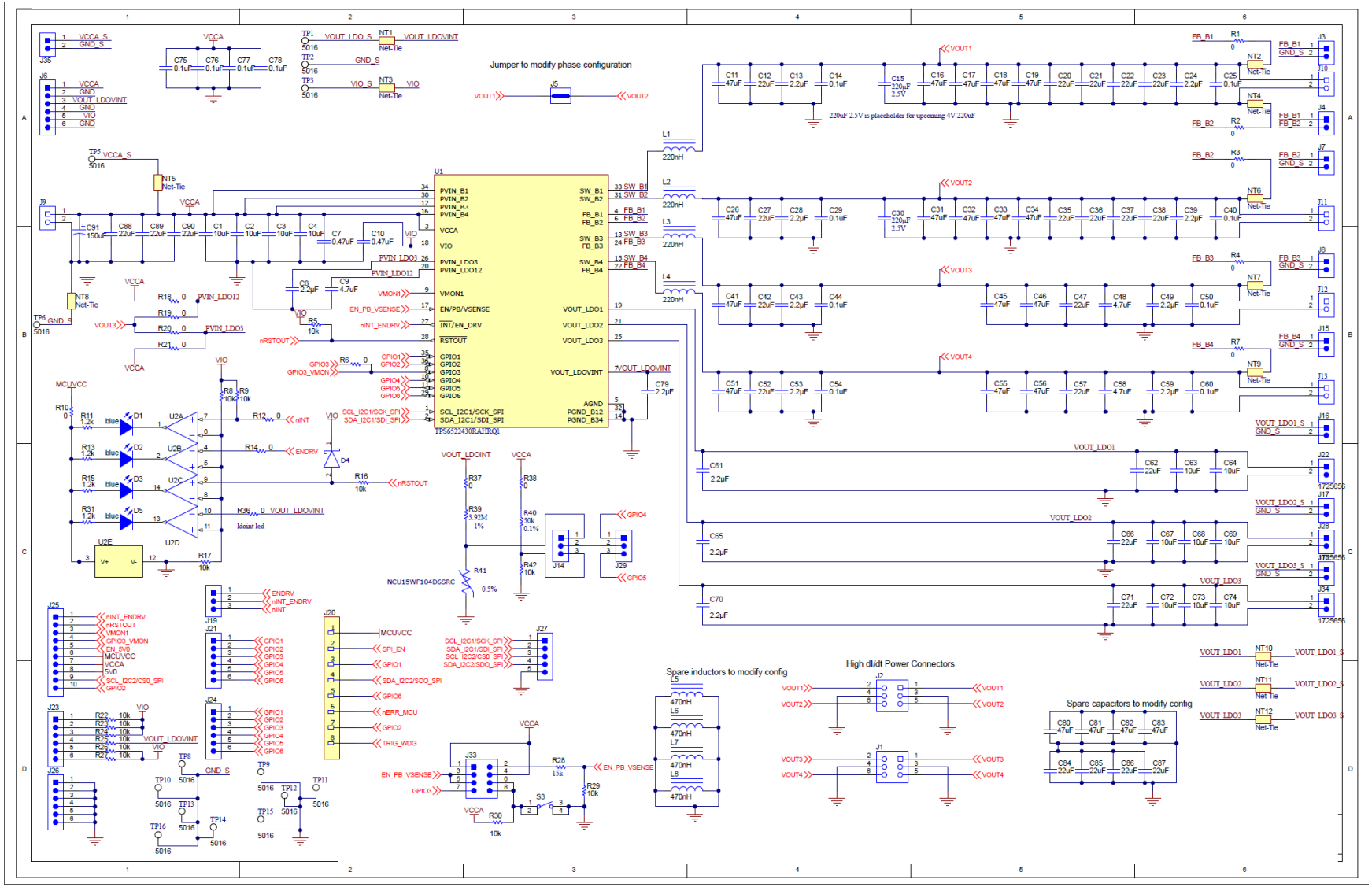
Appendix 5 PCB first signal layer (layer 3)

Appendix 6 PCB second signal layer (layer 4)

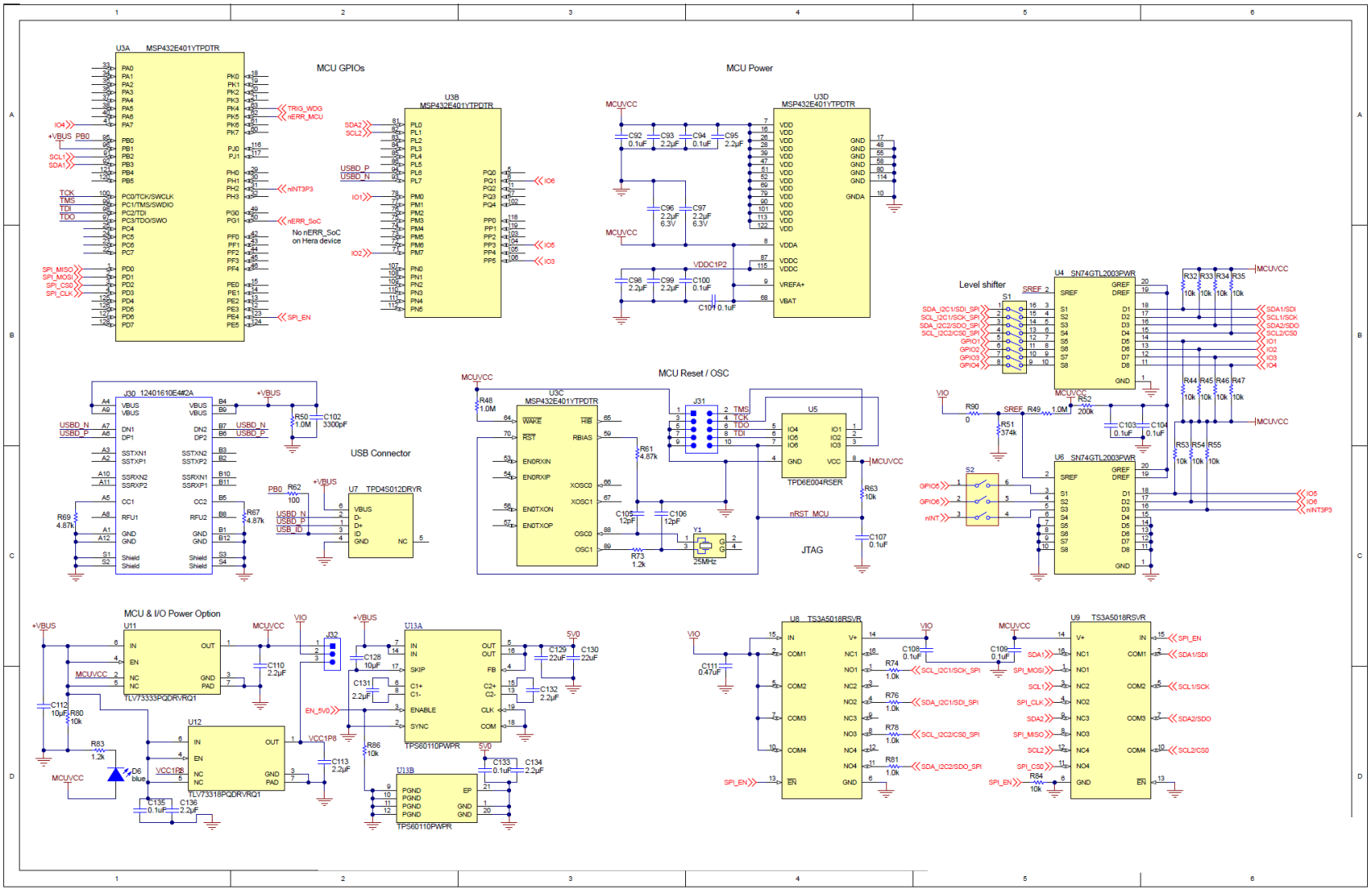
Appendix 7 PCB second ground layer (layer 5)

Appendix 8 PCB bottom layer (layer 6)

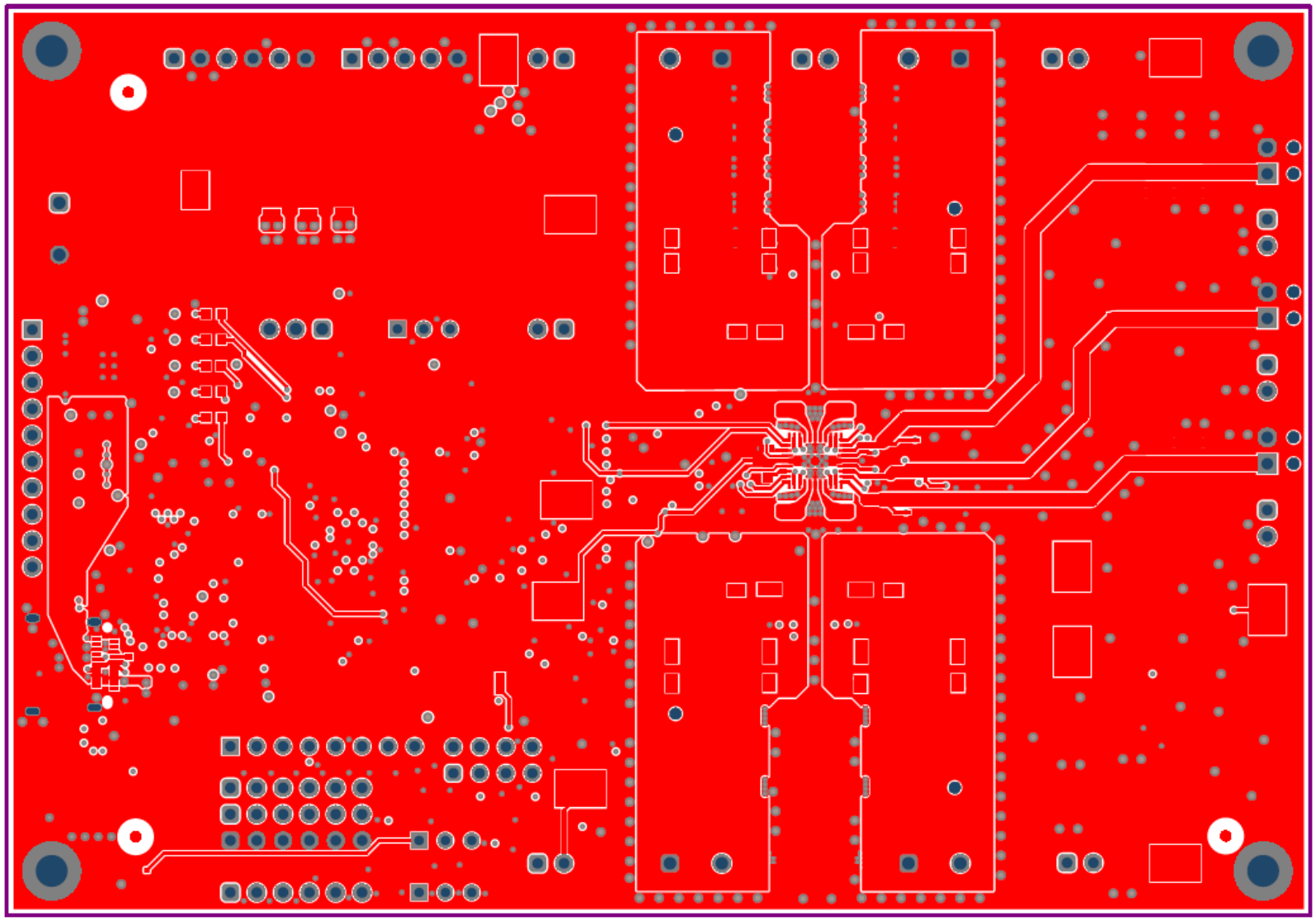
Appendix 1 EVM PMIC side of the schematic



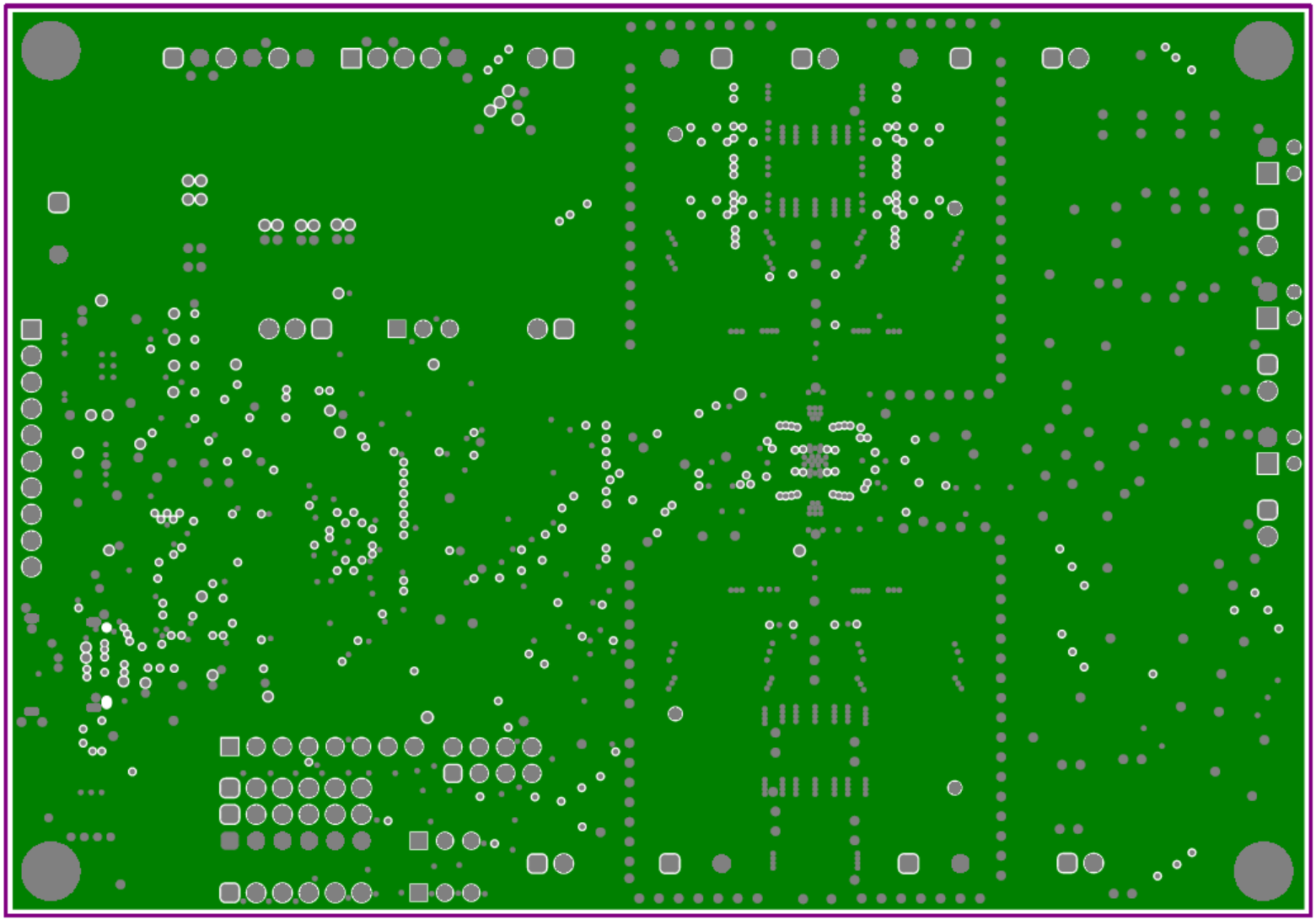
Appendix 2 EVM microcontroller side of the schematic



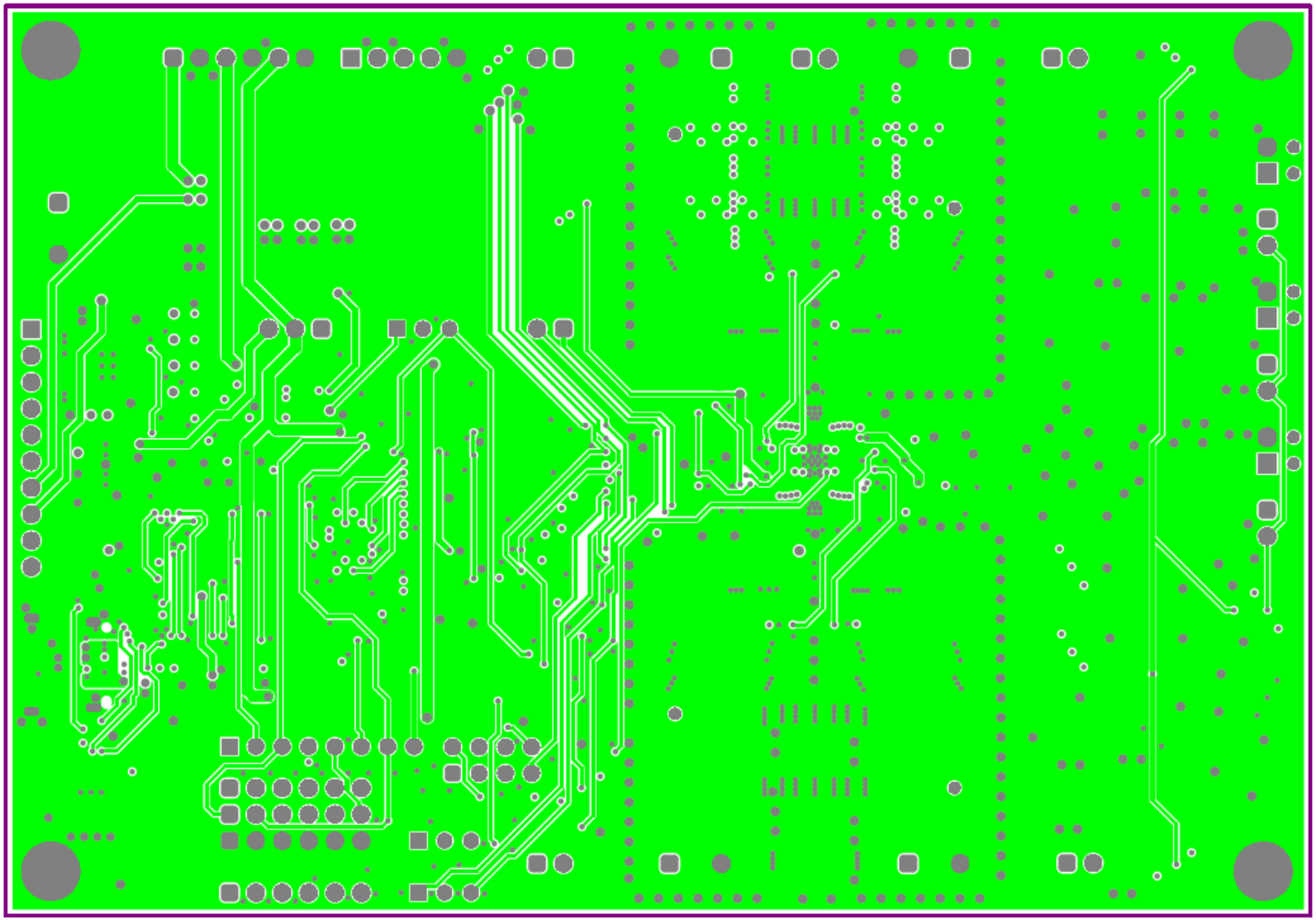
Appendix 3 PCB top layer (layer 1)



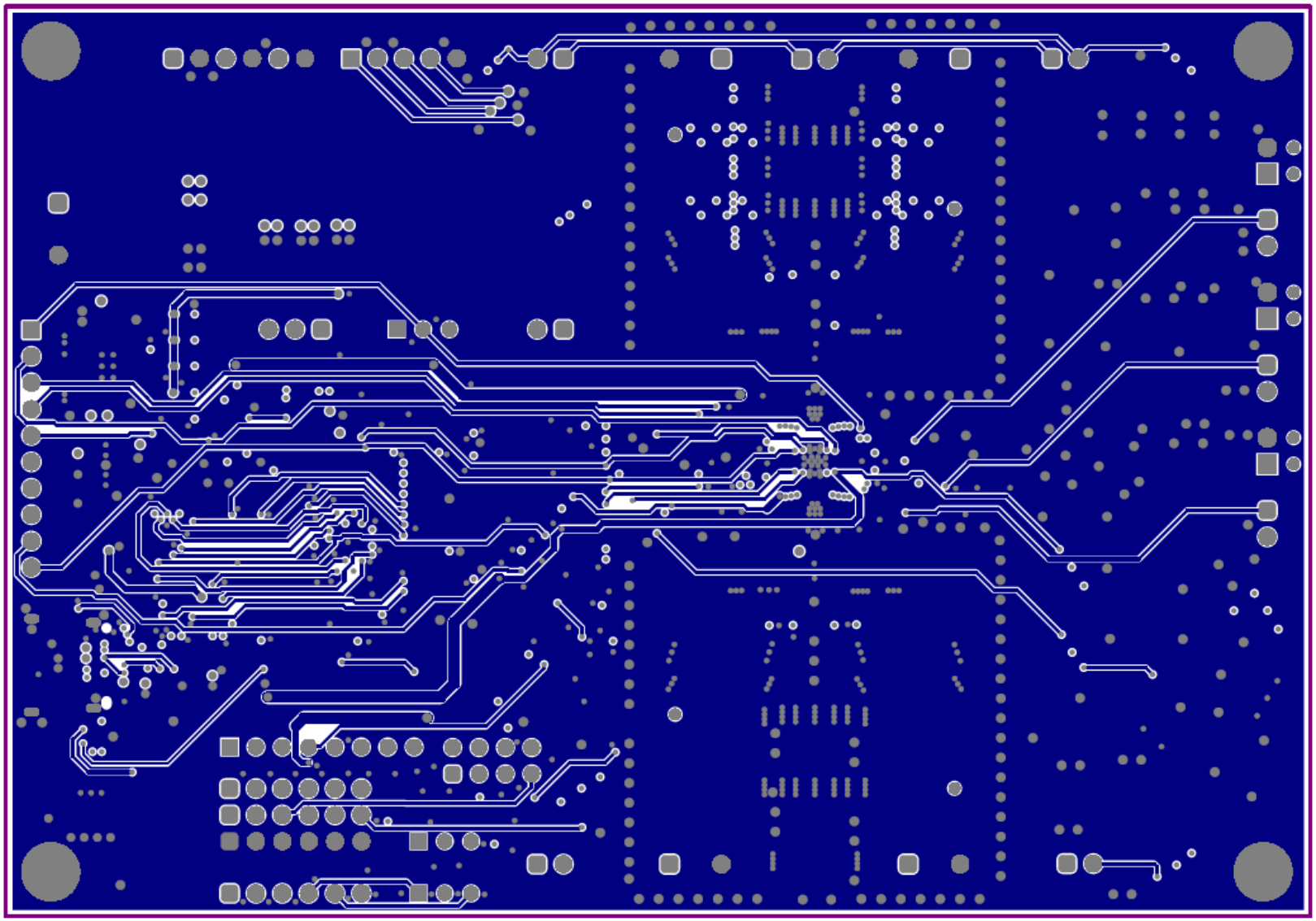
Appendix 4 PCB first ground layer (layer 2)



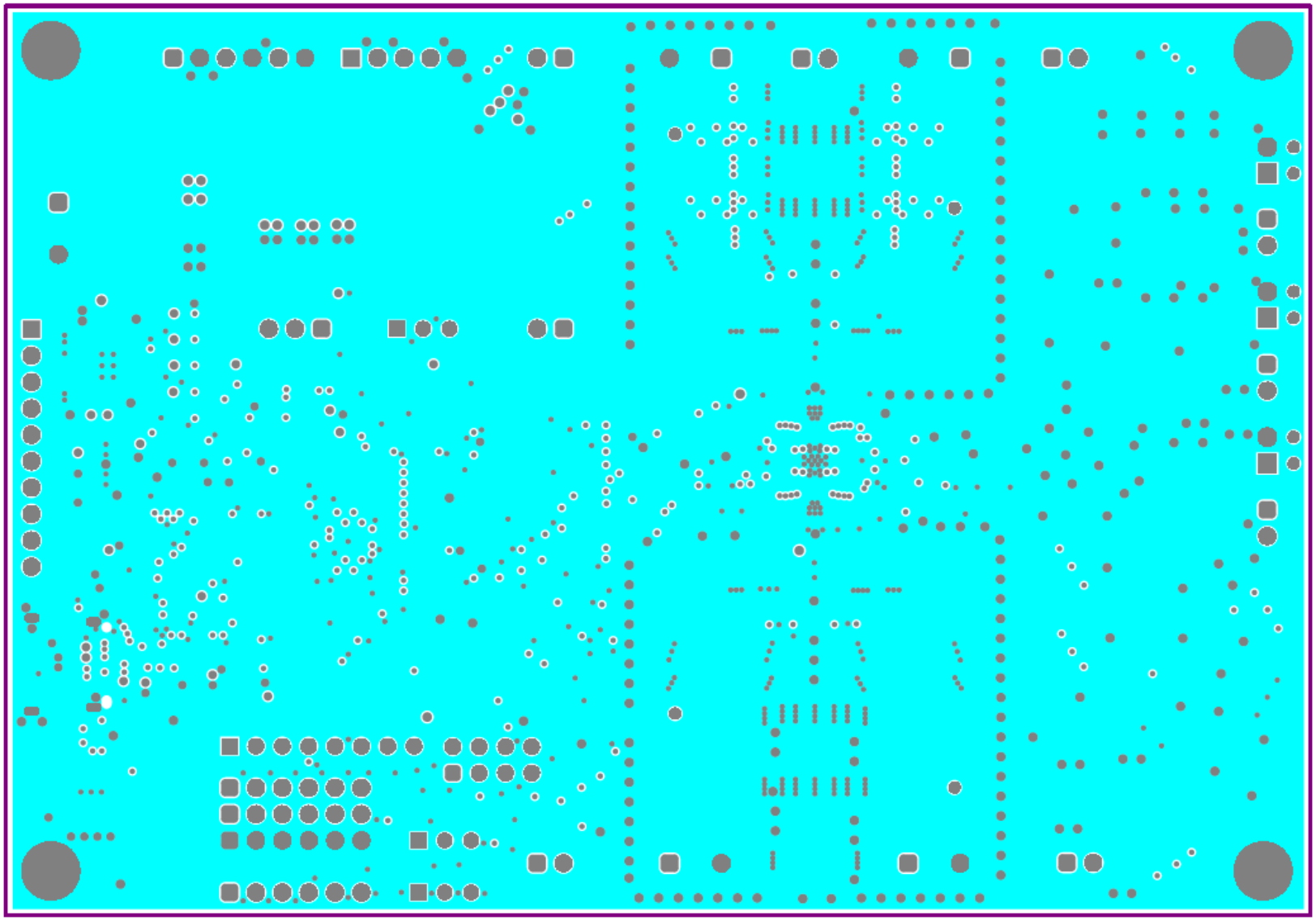
Appendix 5 PCB first signal layer (layer 3)



Appendix 6 PCB second signal layer (layer 4)



Appendix 7 PCB second ground layer (layer 5)



Appendix 8 PCB bottom layer (layer 6)