Converter Topology for Megawatt Scale Applications with Reduced Filtering Requirements, formed of IGBT Bridge operating in the 1000 Hz Region with Parallel Part-Rated High-Frequency SiC MOSFET Bridge

Converter Topology for Megawatt Scale Applications with Reduced Filtering Requirements, formed of IGBT Bridge operating in the 1000 Hz Region with Parallel Part-Rated High-Frequency SiC MOSFET Bridge

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***Abstract*—This article investigates the design and control of the Parallel Hybrid Converter (PHC), which consists of parallel connection of a Silicon (Si) IGBT bridge and a partially rated Silicon Carbide (SiC) MOSFETs bridge with a shared DC bus. The IGBT bridge processes the bulk of the power, while switching at a low frequency to maximise efficiency, while the SiC MOSFETs bridge's lower relative switching loss is exploited to filter low-order harmonics from the IGBT bridge. A Finite-Set Model Predictive Controller is detailed that allows IGBT switching frequencies down to 1 kHz to be achieved while also tightly controlling the magnitude of current in the SiC bridge. A Genetic Algorithm is utilised to automatically tune the control and investigate the design of the output filter as well as the influence of the controller time-step and horizon length on performance. Power loss estimates of a 1.5 MW application case are made showing potential for significant power-loss reductions. Experimental tests validate an FPGA implementation of the controller and topologies performance, with IGBT bridge frequencies below 1.2 kHz and grid-current THD below 3% achieved. The ability of converter to switch operation between a high-current and a low-current mode and dynamic performance is also verified.**

***Index Terms*—Power Electronic Converter, Partial Load Efficiency, Silicon Carbide MOSFETs, Model Predictive Control, Active Filtering, Depth-First Search, Field-Programmable Gate Array**

I. Introduction

The Silicon IGBT based two-level converter is one of the most commonly used DC-AC converter topologies in medium to high power applications. Passive LCL output filters are typically required in grid-connected applications to meet grid voltage and current requirements for harmonic emissions and total harmonic distortion. Such LCL filters can have significant drawbacks, including additional power losses resulting from damping resistor requirements [1], [2], reduced control bandwidth, additional reactive power generation, and susceptibility to oscillation [3]. In addition, the switching frequency of Si IGBTs in high-power applications is typically limited to 2-3 kHz, due to their relatively high switching losses, increasing filtering requirements. Wide-bandgap power semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), have made significant advances in performance and rated power in recent years. The vastly reduced switching losses of such devices offer the ability to design more efficient power converters with significant improvement in stability and power quality afforded by a reduction in required filter sizes [4], [5], [6]. SiC MOSFETs converters have demonstrated significant improvement gains over previous Si IGBT based converter topologies, particularly in kilowatt scale power applications [7], [8], [9]. SiC MOSFETs with voltage ratings in the 650-1700 V are now commercially available from multiple manufacturers, with single die devices with current ratings up to 120 A available. Recent multi-die SiC MOSFETs modules with current ratings of up to 700 A are just now becoming available, enabling converters with power ratings in the hundreds of kilowatts up to the megawatt scale. However, SiC Modules with current ratings in the 1-3 kA region, which would provide replacement of existing high current Si IGBT modules as typically used in multi-megawatt applications (such as wind turbines, solar PV, and energy storage systems) are not yet available commercially, though they are being experimentally demonstrated in the literature [10], [11], [12]. In addition, the cost of Wide-bandgap power-semiconductors is also generally still 3 to 8 times higher than their Si modules [13].

This paper presents an investigation into the design and control of the Parallel Hybrid Converter (PHC), with a focus on its use in grid-connected multi-megawatt scale applications. The PHC is shown in Fig. 1 and is formed by combining a Low-Frequency (LF) high-current Si IGBT two-level three-phase bridge with a partially rated High-Frequency (HF) SiC MOSFETs two-level three-phase bridge. This allows lower current (and so lower cost) SiC MOSFETs modules with low switching losses to be operated at high frequencies, gaining benefits in terms of reduced filtering requirement and

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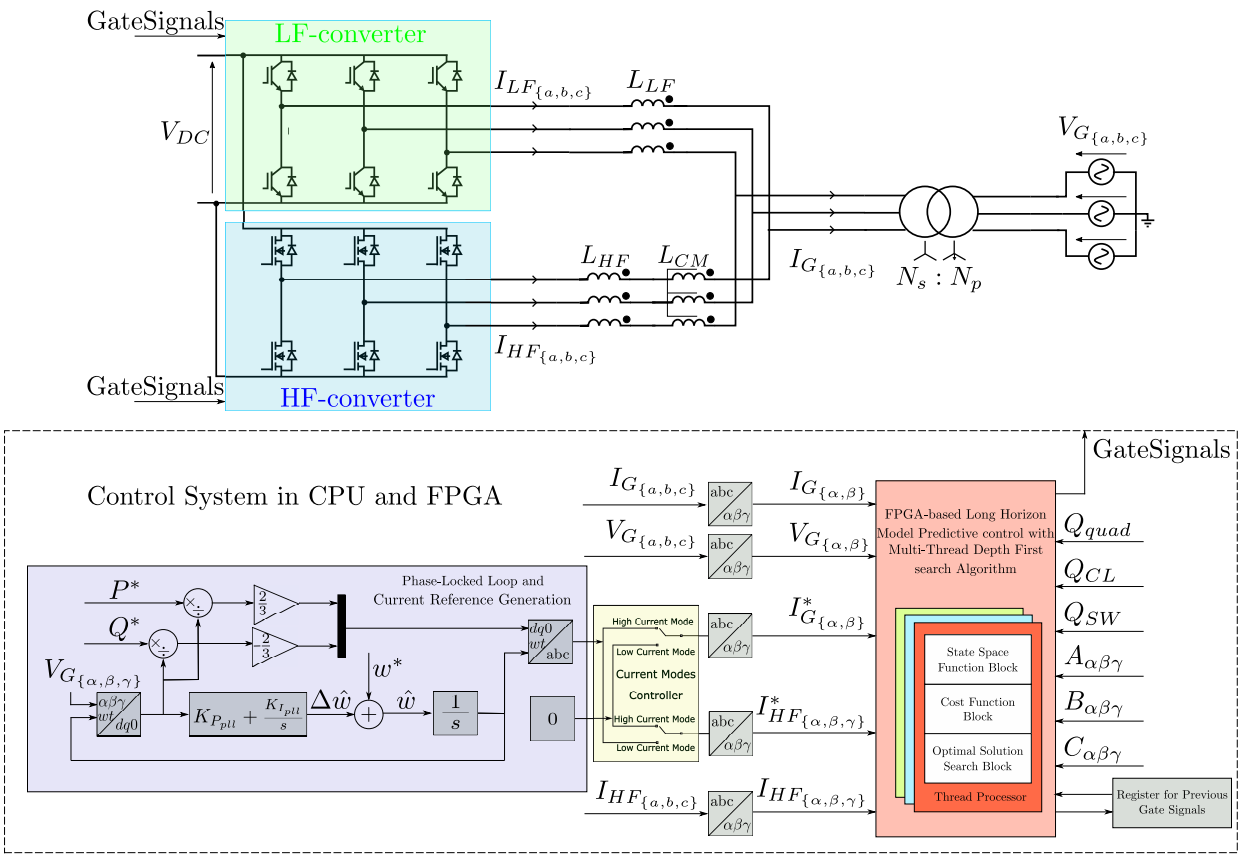


Fig. 1: Si/SiC Parallel Hybrid Converter Topology comprised of Low-Frequency (LF) Si IGBT bridge and High-Frequency (HF) partially-rated SiC MOSFETs bridge. The general control system consists of the reference generation implemented on a CPU and a Long-Horizon Finite-Set Model Predictive Control algorithm implemented on an FPGA.

increased control bandwidth, while taking advantage of lower-cost conduction loss optimised high current devices (such as Si IGBTs) to process the majority of the power. In comparison to alternative converter arrangements such as the parallel connection of multiple lower-rated two-level converters in parallel or interleaved, the PHC offers the advantage of the reduced number of current sensors and auxiliary circuits, the ability to use comparatively low-cost conduction optimised high-current IGBTs at low frequency, high control bandwidth, and the ability to achieve effective SiC MOSFETs switching frequencies while only using SiC MOSFETs with a partial power rating. This comes at the cost of a relatively complicated control structure and the necessity of a common-mode impedance to enable the circulating current between the LF and HF bridges to be controlled.

This general concept of implementing converter topology that utilise both Si IGBTs and partially-rated SiC MOSFETs has received some interest in the literature. A Si/SiC transistor-clamped multilevel H-Bridge inverter (TCHB) is proposed in [14]. An Active Neutral Point Clamped (ANPC) converter is proposed to use SiC MOSFETs to solve the unbalance switching problem and thermal stress in conventional neutral point clamped (NPC) converters [15], [16]. A converter topology consisting of an ANPC with Si IGBT module and H-bridge with SiC MOSFETs circuits is proposed in [17]. A Modular multilevel converter (MMC) with hybrid Si/SiC devices has been proposed for use in high-voltage DC transmission applications [18], [19]. In [20], a hybrid half-bridge (HHB) converter topology (400 V, 3000 W) is proposed and controlled by a proportional-integral regulator and PWM module with Si converter (20 kHz) and SiC converter (160 kHz) switching frequency, THD is about 4%, indicating the topology can achieve a 20%–50% device cost reduction compared to all SiC design. A Wide-bandgap Fractional Power Processing (WFPP) three-phase two-level voltage source inverter (VSI) is simulated and experimented with 100 V DC input, where a Si converter (2 kHz) and SiC converter (10 kHz) are individually SPWM controlled using PI controllers, showing the THD can be reduced to about 6% [13]. An optimisation strategy of WFPP control selects an optimal power-sharing factor between the PID controlled 2 kHz Si IGBT and 10 kHz SiC MOSFETs converter, which improves the THD performance down to 3.8% and reduces the circulating current [21]. In [22], a PI and PWM combined control method is demonstrated for the parallel converter. This control method is divided into three main current control blocks, including grid-side, main converter and active filter energy control, with the aim of reducing the SiC current load and frequency.

In the majority of these previous articles, conventional control methods have been applied, such as PWM or hysteresis band control, which result in relatively high and/or fixed switching frequencies in both converters. The high switching loss will decrease the overall efficiency of the system, particularly in multi-megawatt applications. In addition, in

such control methods is difficult to implement strict current limit constraints to limit the peak turn-off current of the partially rated devices within the converter. The authors have demonstrated that single-step direct Model Predictive Control techniques are very applicable to the PHC, and allow sub 2 kHz switching to be achieved in the LF converter [23], [24].

Motivated by the research above, this paper gives a comprehensive system and control design of the parallel hybrid converter topology with a focus on multi-megawatt applications, including experimental verification of the proposed control scheme and filter design. The main contributions of this article are summarised as follows:

1) A Long-Horizon Finite Control Set Model Predictive Control (FCS-MPC) for the PHC is implemented, allowing the switching frequency of the LF converter to be driven down to the region of 900-1300 Hz, substantially lower than other conventional control methods. This is achieved while also also achieving high-quality grid-side current waveforms, and strictly limiting the magnitude of current in the partially rated HF bridge to within a defined limit.
2) The impact of the converter output filter design as well as various FCS-MPC parameters such as controller time-step, look-ahead horizon, and tuning weights, on the achievable converter performance is analysed.
3) A real-time FPGA implementation of the proposed FCS-MPC controller is developed using a Multi-Thread Depth-First search algorithm, allowing controller frequencies of 100 kHz to be achievable on medium-cost hardware.
4) Experimental validation of the proposed FCS-MPC controller and the filter design on a 16.9 kW prototype converter in steady and dynamic conditions.
5) Efficiency estimates for a 1.5 MW scale converter are presented, showing the potential for significant efficiency improvements in comparison to a conventional fixed-frequency Si IGBT converter.

II. Parallel Hybrid Converter Topology

The Parallel Hybrid Converter topology considered in this paper is illustrated in Fig. 1. The PHC consists of two parallel connected three-phase bridge circuits, with an imbalance in current rating between the two bridges, here termed the Low Frequency (LF) bridge and High Frequency (HF) bridge. Nominally the LF bridge is shown as being formed of Si IGBTs, while the HF bridge is shown as being formed of SiC MOSFETs, though fully SiC MOSFETs or Si IGBTs implementations could also be considered. An example of the voltage and current waveforms in the PHC is given in Fig. 2. The LF bridge's primary purpose is to process the bulk of the power, while switching at a low frequency in order to maximise the efficiency, while the HF converter's lower relative switching loss is exploited to filter the low-order harmonics from the HF bridge. There is a trade-off in the converter design between the ratio of the current rating between the HF bridge and the LF bridge, and the achievable switching frequency reduction in the LF bridge. The HF bridge converter may be considered as an active power filter, though the shared DC bus means there is no strict requirement for it to only process reactive harmonic current. The shared DC bus also provides a path for common-mode current to circulate through the AC side of both converters, as shown in Fig. 2. To handle the circulating current between two bridges, some common-mode impedance must be present between the converter, with the magnitude of common-mode current limited by control action [25].

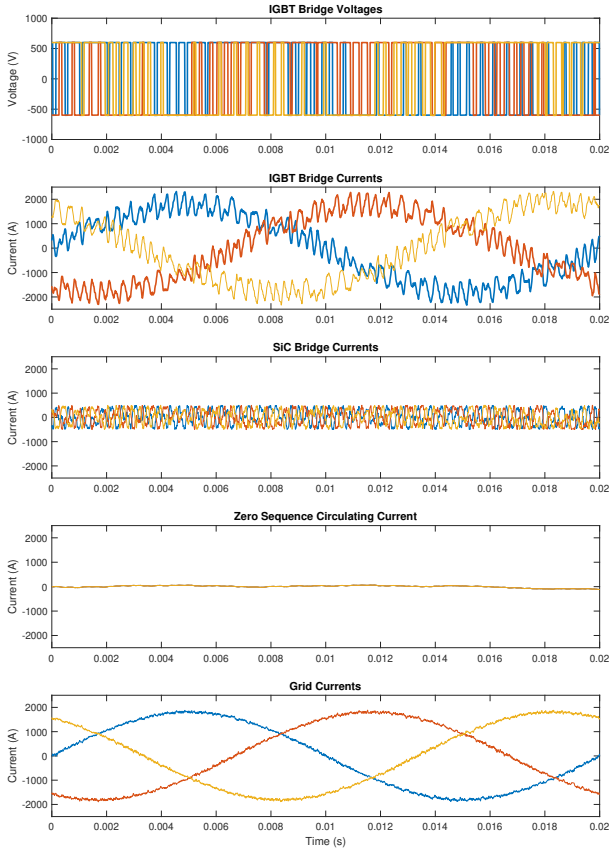


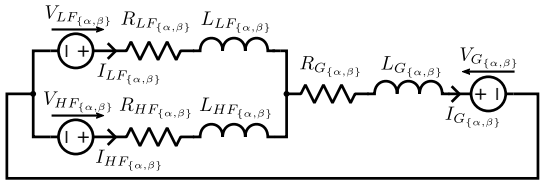
Fig. 2: Example voltage and current waveforms of the PHC showing the IGBT bridge voltages, IGBT bridge currents, SiC MOSFETs bridge currents, zero sequence circulating current and the grid currents.

The PHC topology was initially proposed in [25], for the purpose of reducing the switching cost of the inverter and the output filter in lower power applications. The achieved switching frequencies of the Si IGBT and SiC MOSFETs converters in [25] was 4 kHz and 25 kHz respectively, significantly higher than those desirable for high-current applications. A direct hysteresis control band method was used for regulating the grid-current, with the circulating current in the HF bridge being controlled using zero-sequence switching vector control, resulting in the HF bridge current magnitude not being strictly controlled to below a defined current limit. Previous work by the authors has demonstrated that single-step direct Model Predictive Control techniques are very applicable to the PHC, and allow sub 2 kHz switching to be achieved in the LF converter, while strictly controlling the HF bridge-current to within a defined current limit [23], [24].

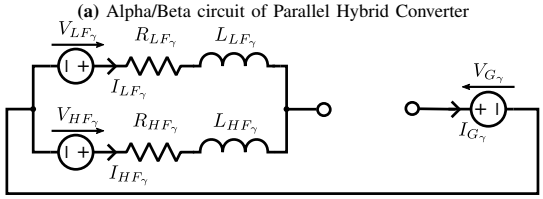
III. Parallel Hybrid Converter Current Controller and Model Design

This section describes the design of a Finite-Set Model Predictive Control implementation for the PHC that has been found to allow switching frequencies in the LF converter of around 1000 Hz, while also limiting the peak current in the HF bridge to within a strict current limit and achieving low THD grid current waveforms. Compared to traditional PID, PWM or linear-quadratic regulator (LQR) control, FS-MPC can more easily handle multi-objective control problems with constraints. This method has been found to be particularly applicable for the PHC, as it enables a strict regulation of the current magnitudes flowing through the partially-rated SiC bridge, tight regulation of the output currents, while also achieving low-switching frequencies in the LF bridge. Short horizon FS-MPC has previously been applied to the PHC in [23], [24]. The disadvantage of short horizon control is that it cannot consider the influence of the next optimal decision, and can lead to some inefficient switches decisions. As shown in [26], [27], [28], long prediction horizons have a positive influence on control and system performances.

A. System Description and State-Space Equation



(a) Alpha/Beta circuit of Parallel Hybrid Converter



(b) Gamma circuit of Parallel Hybrid Converter

Fig. 3: Circuit diagram of the of Parallel Hybrid Converter in the Alpha-beta-gamma coordinate frame.

The equivalent circuits of the PHC in the $\alpha\beta\gamma$ reference frame are given in Fig. 3. The equivalent inductances can be calculated by (1), where L_s is the winding self-inductance and k is the coupling factor. For a three-phase differential inductor with ideal coupling ($k = -0.5$) the value $L_{\alpha/\beta}$ is equal $\frac{3}{2}L_s$ with L_γ equal to 0, and for an ideal three-phase common-mode inductor with ideal coupling ($k = 1$) the value of L_γ is equal to $3L_s$ with $L_{\alpha/\beta}$ equal to 0.

$$L_{\alpha\beta\gamma} = L_s \begin{bmatrix} -k+1 & 0 & 0 \\ 0 & -k+1 & 0 \\ 0 & 0 & 2k+1 \end{bmatrix} \tag{1}$$

The state vectors are shown in (2) and the controllable and uncontrollable input vectors are given in (3) and (4). The state-space equations describing the dynamics of the system are given in (5) and (6). The matrices $A_{\alpha\beta\gamma}$, $B_{\alpha\beta\gamma}$ and $E_{\alpha\beta\gamma}$ of the state-space equations are given in (7), (8) and (9).

$$x_{\alpha\beta\gamma} = \begin{bmatrix} I_{G_\alpha} & I_{HF_\alpha} & I_{G_\beta} & I_{HF_\beta} & I_{HF_\gamma} \end{bmatrix}^T \tag{2}$$

$$u_{\alpha\beta\gamma} = \begin{bmatrix} V_{LF_\alpha} & V_{LF_\beta} & V_{LF_\gamma} & V_{HF_\alpha} & V_{HF_\beta} & V_{HF_\gamma} \end{bmatrix}^T \tag{3}$$

$$v_{\alpha\beta\gamma} = \begin{bmatrix} V_{G_\alpha} & V_{G_\beta} \end{bmatrix}^T \tag{4}$$

$$\dot{x_{\alpha\beta\gamma}} = A_{\alpha\beta\gamma} x_{\alpha\beta\gamma} + B_{\alpha\beta\gamma} u_{\alpha\beta\gamma} + E_{\alpha\beta\gamma} v_{\alpha\beta\gamma} \tag{5}$$

$$y_{\alpha\beta\gamma} = C_{\alpha\beta\gamma} \dot{x_{\alpha\beta\gamma}} + D_{\alpha\beta\gamma} u_{\alpha\beta\gamma} \tag{6}$$

B. Finite-Set Model Predictive Controller Description

A diagram of the proposed overall control scheme for the PHC is given in Fig. 1. A standard current reference calculation method can be implemented (shown here as a DQ implementation of P/Q control with a PLL), with this current reference passed to the FS-MPC current controller which then directly outputs the gate signals for both bridges. The tuning of the FS-MPC cost function coefficients determines the relative importance of the tracking of these set-points, with the weighing on the grid-side currents typically much higher than those applied to the HF bridge currents. Under high current mode, the current references for the grid-side currents are directly passed as references for the LF bridge, while the current reference for the HF bridge currents (including the circulating current component between the LF and HF bridge (i_{HF_γ})) are set to zero. As discussed in [23], during low power set-points it is possible to block the LF bridge and use just the HF bridge to process the power. This is achieved through the use of a switch which swaps current references between the HF and LF bridges, with the LF bridge gates blocked.

The general long-horizon FS-MPC cost function (10), (11), (12) consists of two terms. These two terms both are a sum of each $N_{horizon}$ step's value, where $N_{horizon}$ is the length of the FS-MPC look-ahead horizon, N_p is prediction horizon time steps. The first term is the predicted state error, which is the difference between the reference vector y^* and the state space function's output vector y. The second term is the converter switching penalty, comparing the difference between the current switching state and the previous switching state. When we set the C matrix to be an identity matrix and the D matrix to be a zero matrix, the output vector $y_{\alpha\beta\gamma}$ will be equal to $\dot{x_{\alpha\beta\gamma}}$, depending on (5) and (6).

$$J = \sum_{l=k}^{k+N_p-1} \|y^*(l+1) - y(l+1)\|^2_{Q_{quad}} + \|\Delta u(l)\|^2_{Q_{sw}} \tag{10}$$

Each term's representation is a Euclidean norm in matrix form. The penalty matrices Q_{quad} and Q_{sw} are used to tune the converter's performance by placing weight on minimising errors in the current references (11) and switching actions in the LF and HF bridges (12).

$$A_{\alpha\beta\gamma} = \begin{pmatrix} -\frac{L_{HF_\alpha}R_{LF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*R_{G_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & -\frac{L_{LF_\alpha}*R_{HF_\alpha}-L_{HF_\alpha}*R_{LF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 \\ 0 & -\frac{L_{HF_\beta}*R_{LF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*R_{G_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 & -\frac{L_{LF_\beta}*R_{HF_\beta}-L_{HF_\beta}*R_{LF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 \\ -\frac{L_{LF_\alpha}*R_{G_\alpha}-L_{G_\alpha}*R_{LF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & -\frac{L_{LF_\alpha}*R_{HF_\alpha}+(R_{LF_\alpha}+R_{HF_\alpha})*L_{G_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 \\ 0 & -\frac{L_{LF_\beta}*R_{G_\beta}-L_{G_\beta}*R_{LF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 & -\frac{L_{LF_\beta}*R_{HF_\beta}+(R_{LF_\beta}+R_{HF_\beta})*L_{G_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_{HF_\gamma}}{Lcm} \end{pmatrix} \tag{7}$$

$$B_{\alpha\beta\gamma} = \begin{pmatrix} \frac{L_{HF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 & -\frac{L_{LF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 \\ 0 & \frac{L_{HF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 & 0 & -\frac{L_{LF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 \\ -\frac{L_{G_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 & \frac{(L_{LF_\alpha}+L_{G_\alpha})}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 & 0 \\ 0 & -\frac{L_{G_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 & 0 & \frac{(L_{LF_\beta}+L_{G_\beta})}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} & 0 \\ 0 & 0 & -\frac{1}{Lcm} & 0 & 0 & \frac{1}{Lcm} \end{pmatrix} \tag{8}$$

$$E_{\alpha\beta\gamma} = \begin{pmatrix} -\frac{L_{LF_\alpha}+L_{HF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 \\ 0 & -\frac{L_{LF_\beta}+L_{HF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} \\ -\frac{L_{LF_\alpha}}{L_{LF_\alpha}*L_{HF_\alpha}+(L_{LF_\alpha}+L_{HF_\alpha})*L_{G_\alpha}} & 0 \\ 0 & -\frac{L_{LF_\beta}}{L_{LF_\beta}*L_{HF_\beta}+(L_{LF_\beta}+L_{HF_\beta})*L_{G_\beta}} \\ 0 & 0 \end{pmatrix} \tag{9}$$

$$\|y^* - y\|^2_{Q_{quad}} = (y^* - y)^T Q_{quad}(y^* - y) \tag{11}$$

$$\Delta u(k) = u(k) - u(k-1) \tag{12}$$

To simplify the function (10), the system outputs and switching states can be represented in matrix form (13) and (14).

$$Y(k) = [y^T(k+1)\ y^T(k+2)\ ...\ y^T(k+N_p)]^T \tag{13}$$

$$U(k) = [u^T(k+1)\ u^T(k+2)\ ...\ u^T(k+N_p)]^T \tag{14}$$

With the functions above, the original function (10) can be reformed into function (15).

$$J = \|Y^*(k) - Y(k)\|^2_{Q_{quad}} + \|\Delta U(k)\|^2_{Q_{sw}} \tag{15}$$

C. Circulating Current Control and HF Bridge Current Limit

The classical cost function typically applied to FS-MPC controlled power converters is an unconstrained function (15). In the case of the PHC, considering substantial differences in current rating between the LF and HF bridges, it is desirable to be able to strictly limit the peak value of the HF converter currents. This is achieved by the addition of a further constraint in the cost function, as given by (16), where i_{bnd} is a specified constant current limit value, i_{HF_x} is the HF converter output phase current, and Q_{CL} is the tuning weight matrix placed on the current limit term. This constraint adds a large penalty cost to any switching state that would result in the currents in the HF bridge exceeding the specified current limit. The inclusion of the current limit also further limits the magnitude of i_{HF_γ}, even if the $Q_{quad_{HF_\gamma}}$ term that is applied is set to zero.

$$J_{CL} = \sum_{l=k}^{k+N_p-1} \begin{cases} Q_{CL}, & \text{if } |i_{HF_x}(l+1)| \geq i_{bnd} \\ 0, & \text{if } |i_{HF_x}(l+1)| < i_{bnd} \end{cases} \tag{16}$$

The final long-horizon cost function with current limit constraint added is shown in (17), which will be implemented into the simulation and FPGA algorithm later.

$$J = \|Y^*(k) - Y(k)\|^2_{Q_{quad}} + \|\Delta U(k)\|^2_{Q_{sw}} + J_{CL} \tag{17}$$

IV. PHC Controller Parameter Selection and Filter Design

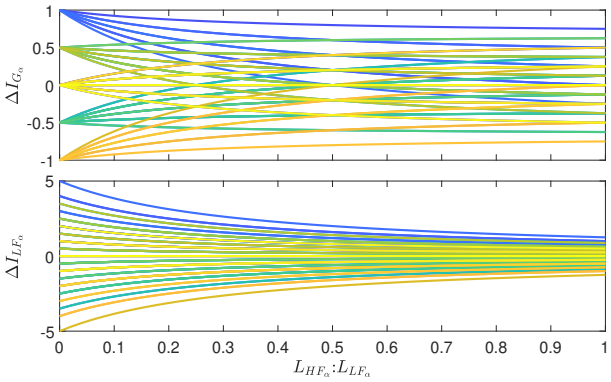
In grid-connected megawatt-scale applications, the grid-interfacing transformer forms a significant part of the converter output filter. Typical transformer impedance ($L_{G_{\alpha/\beta}}$) of 0.05-0.08 pu can be expected for megawatt-scale converters [29]. Unless otherwise stated, the converter parameters in Table I are used in the following sections. The main inductance sizes in the $\alpha\beta\gamma$ reference that can be adjusted through design in the PHC are therefore the LF bridge output inductance ($L_{LF_{\alpha/\beta}}$), the HF bridge output differential impedance ($L_{HF_{\alpha/\beta}}$) and the HF bridge common-mode impedance (L_{HF_γ}).

TABLE I: PHC filter and control parameters

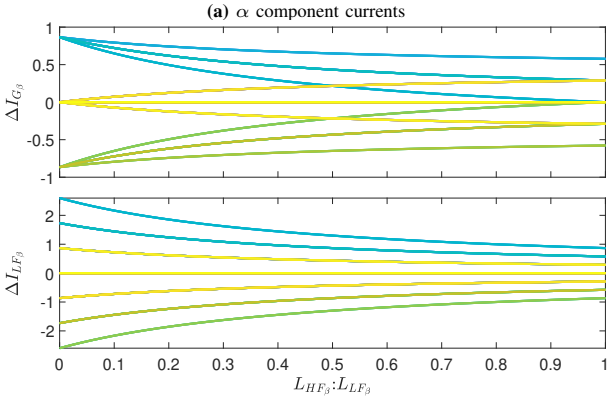
PHC Converter Parameters	Value
S	1.52 MVA
V_{DC}	1200 V
V_{line}	690 V
Z_{base}	0.313 Ω
L_{base}	996 μH
Grid Frequency	50 Hz
Current Limit	500 A
Look-Ahead Horizon ($N_{horizon}$)	1-4

In general the sizing of $L_{LF_{\alpha/\beta}}$ is similar to the sizing of the output inductor of a high-power fixed frequency converter. The

increased size results in reduced ripple current magnitudes, enabling lower switching frequencies, with corresponding design trade-offs of increased inductor size/cost and the inductive voltage rises/drops across the inductor. For design purposes it is convenient to consider the size of the HF bridge differential inductance $L_{HF_{\alpha/\beta}}$ as a ratio of $L_{LF_{\alpha/\beta}}$. Fig. 4 shows the normalised discrete-time grid side and LF converter current vectors that can be achieved by the 64 switching states of the PHC, with variation in the ratio of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$. With a ratio of 0 the voltage across the $L_{G_{\alpha/\beta}}$ is set purely by the output of the HF converter, and so the number of unique vectors in the α and β current components equals that of a two-level converter. As $L_{HF_{\alpha/\beta}} : L_{LF_{\alpha/\beta}}$ increases the number of discrete current vectors that can be achieved increases. Crossover points where several switching states result in the same current vectors can be seen at ratios of 0.5 and 1. For maximal potential current vectors ratios of either 0.4 or 0.6 appear to be good choices, providing 25 effective levels in the α component grid-side current and 9 in the β component of the grid-side current.



(a) α component currents



(b) β component currents

Fig. 4: Discrete time α and β current differentials for the grid side and LF converter currents with variation in the ratio of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$, $L_{LF_{\alpha/\beta}}$=$L_{G_{\alpha/\beta}}$= 0.075 pu. Currents normalised by the maximum grid-side current differential value.

Examples of the grid-current vectors in the α/β plane that can be achieved by each switching state for several example ratios of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$ are shown in Fig. 5.

A. System design by Non-Denominated Set Genetic Algorithm

The performance of the PHC in terms of achieved switching frequency reduction in the LF bridge and grid-current's THD

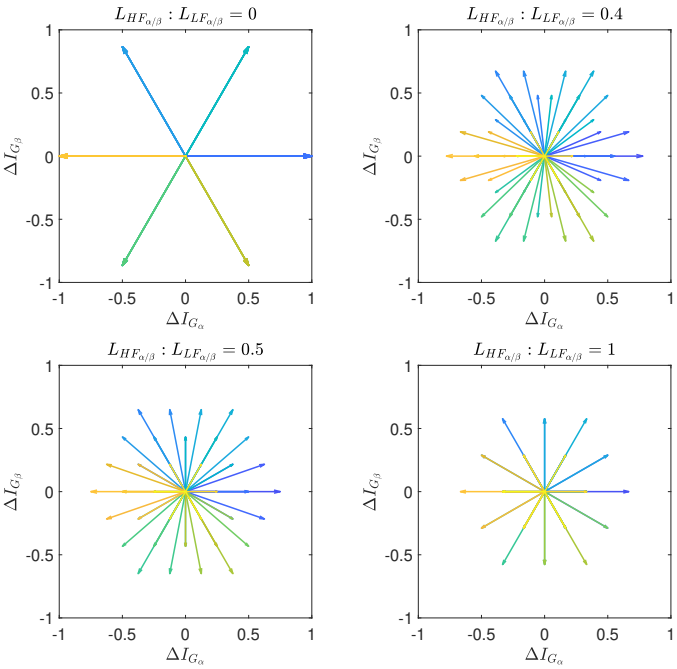


Fig. 5: Normalised discrete time α and β current vectors for the grid side current with variation in the ratio of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$, $L_{LF_{\alpha/\beta}}$=$L_{G_{\alpha/\beta}}$= 0.075 pu. Currents normalised by the maximum grid-side current differential value.

depends on the control system's parameters, including the FS-MPC controller's tuning weights, control time-step and look-ahead horizons. To further evaluate and make a fair comparison among different control system's parameters, a Non-Denominated Set Genetic Algorithm (NSGA) [30] is utilised to automatically tune the weights of the FS-MPC penalty matrices. As the switching losses within the LF converter are likely to be an order of magnitude higher than the HF converter, a two-objective NSGA has been implemented in most cases with the average switching frequency of the LF bridge and the THD of the grid side current set as the objectives. A constraint on the peak magnitude of the currents within the HF converter was also implemented to ensure these stay within the specified current limit.

The NSGA manipulates the quadratic costs applied to currents in the HF bridge ($Q_{quad_{HF}}$), the switching costs applied to both the LF and HF bridges ($Q_{SW_{LF}}$, $Q_{SW_{HF}}$) and the costs applied to any currents in the HF bridge exceeding the current limit (Q_{CL}). The cost applied to the grid current (Q_{quad_G}) is left as a constant. The parameters used in NSGA are given in Table II. A model of the PHC was implemented in Matlab/Simulink and configured so that the tuning weights were configured by the NSGA.

B. Influence of Output Filter on Performance

The first step of designing the system components is to optimise the HF and LF bridge inductances. Unless otherwise stated, the converter parameters in Table I are used in the following sections. The value of the common-mode impedance L_{HF_γ} was set to 1 pu within these tests to minimise its influence on the performance, along with a current limit in the HF bridge 0.27 times the peak current reached in the

LF bridge. This current limit was chosen to align with the indicative realistic ratio between currently available IGBT (e.g 1800 A) and SiC MOSFETs modules (e.g 500 A). The impact of varying current limits on performance will be investigated in Section VII.

Fig. 6 shows the NSGA-derived Pareto fronts as the ratio of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$ when the objectives are the LF bridge switching frequency and the grid-current THD. A significant increase in achievable performance at the Pareto fronts can be seen as the ratio of $L_{HF_{\alpha/\beta}}$ to $L_{LF_{\alpha/\beta}}$ is increased from 0 to 0.4, with a subsequent reduction as the ratio approaches 1. LF bridge frequencies of approximately 1 kHz are achieved at the knee point of the Pareto fronts.

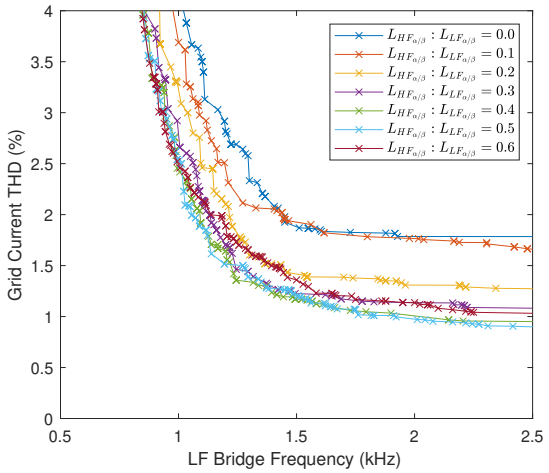


Fig. 6: Pareto fronts of LF switching frequency and grid-current THD performance with variation in HF converter differential mode impedance. L_{HF_γ} = 1.0 pu, $L_{LF_{\alpha/\beta}}$ = 0.075 pu, $L_{G_{\alpha/\beta}}$ = 0.075 pu, f_{MPC} = 100 kHz, $N_{horizon}$ = 1.

Fig. 7 shows the NSGA-derived Pareto fronts when the objectives are the LF bridge switching frequency and the grid-current THD, with variation in the magnitude of $L_{LF_{\alpha/\beta}}$. The value of $L_{HF_{\alpha/\beta}}$ was set to a fixed ratio of 0.4 times the LF bridge inductance, following the results from previous tests. Results show that in order to achieve switching frequencies in the region of 1 kHz in the LF bridge requires values of $L_{LF_{\alpha/\beta}}$ in the region of 0.07-0.1 pu. These values are in the range typically considered for a fixed-frequency two-level converter with switching frequencies in the 2-3 kHz range [31], [32]. Inductance values below these could be considered options for lower power applications where higher switching frequencies in the LF bridge can be tolerated.

Fig. 8 shows the Pareto fronts with variation in the HF common-mode inductance L_{HF_γ}. It should also be noted

TABLE II: Main configuration of the Genetic Algorithm

Genetic Algorithm Parameters	Value
Population Size	400
Elite Count	1
Crossover Fraction	0.5
Max Generations	20
Lower Bounds	[0, 0, 0, 0]
Upper Bounds	[1, 30000, 1000, 100000]
Initial Values	[0.05, 1000, 100, 35000]
Manipulated Values	$Q_{quad_{HF}}, Q_{SW_{LF}}, Q_{SW_{HF}}, Q_{CL}$

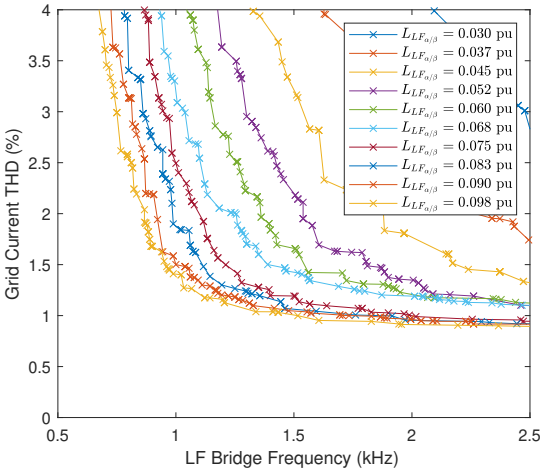


Fig. 7: Pareto fronts of LF switching frequency and grid-current THD performance with variation in LF converter differential mode impedance. L_{HF_γ} = 1.0 pu, $L_{HF_{\alpha/\beta}} = 0.4 \cdot L_{LF_{\alpha/\beta}}$, $L_{G_{\alpha/\beta}}$ = 0.075 pu, f_{MPC} = 100 kHz, $N_{horizon}$ = 1.

that the per-unit impedance shown in Fig. 8 is done on the overall converter base power, and this common-mode inductance would only be rated to conduct the partial current of the HF bridge. With the value of L_{HF_γ} set to 0 the FS-MPC algorithm is still able to function, using switching states that result in zero inter-converter common-mode voltage being generated. This comes at a significant penalty however in terms of the achievable switching frequency in the LF bridge and the grid-current THD. Significant improvements in achievable performance at the Pareto fronts can be seen as impedance is increased from 0 pu to 0.225 pu, with the common-mode impedance enabling the use of the full set of switching states, with diminishing returns past this point in terms of increased performance.

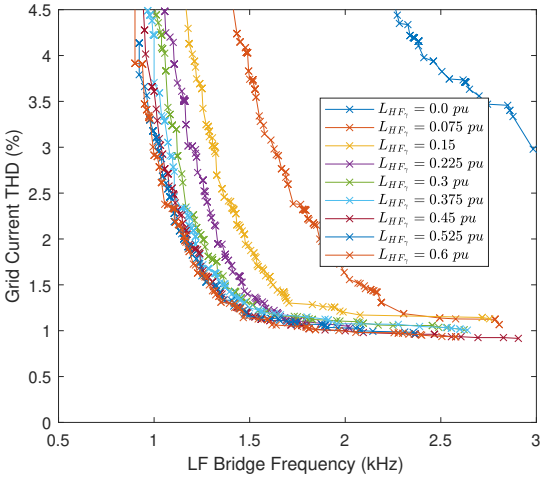


Fig. 8: Pareto fronts of LF switching frequency and grid-current THD performance with variation in HF converter common-mode impedance. $L_{LF_{\alpha/\beta}}$ = 0.075 pu, $L_{HF_{\alpha/\beta}}$ = 0.03 pu, $L_{G_{\alpha/\beta}}$ = 0.075 pu, f_{MPC} = 100 kHz, $N_{horizon}$ = 1.

C. Influence of MPC Look-Ahead Horizon And Controller Time-step on Performance

Fig. 9 shows the Pareto fronts of three different controller time-steps and look-ahead horizons. In each controller frequency case, a notable improvement in achievable performance can be observed when moving from a look-ahead horizon of 1 to 2, with diminishing returns as look-ahead horizons of 3 and 4 are used. Another benefit is the consistency of performance, with small incremental adjustments in either grid-current THD or average switching frequency of the HF converter (f_{HF}) possible horizon values of 2 or greater, whereas the single time-step horizons tend. For the f_{MPC} = 200 kHz case the f_{HF} is approximately 27.5 kHz, decreasing to 14 kHz at f_{MPC} = 100 kHz and 8 kHz at f_{MPC} = 50 kHz. A small decrease in f_{LF} is also observed when moving from a single time-step look-ahead horizon to 2 or 3 steps horizons.

For designs where the achievable grid-current THD is below a desired upper limit, there is scope to reduce f_{LF} by adjusting the cost associated with its switching action. This indicates that there is little to no benefit in considering look-ahead horizons greater than 2 in the PHC. Practically achievable controller frequencies and look-ahead horizon values will be discussed in Section. V.

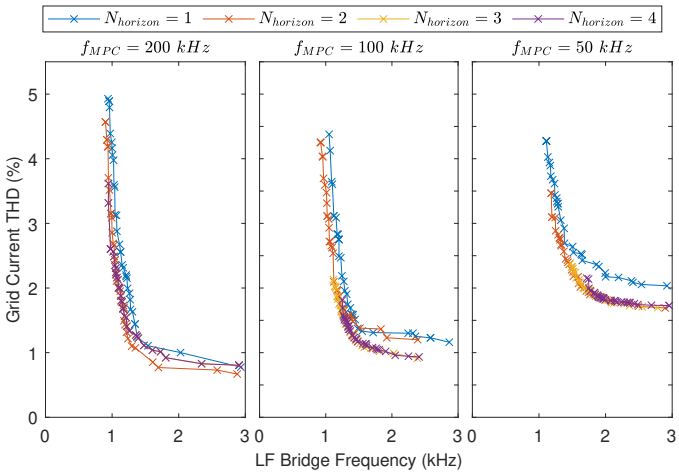


Fig. 9: Pareto fronts of PHC showing impact of controller frequency (f_{MPC}) and look-ahead horizon length ($N_{horizon}$) on PHC switching frequency and THD performance. L_{HF_γ} = 0.3 pu, $L_{LF_{\alpha/\beta}}$ = 0.075 pu, $L_{HF_{\alpha/\beta}}$ = 0.03 pu , $L_{G_{\alpha/\beta}}$ = 0.075 pu.

D. Comparison Against other Control Schemes

The performance of the FS-MPC algorithm was compared against two alternative control schemes applicable to the PHC: direct space vector control [25] and fixed frequency PWM fractional power control [13]. This comparison is given in Fig. 10, and was made using PHC implementations with identical component parameters and with NSGA tuned control parameters. The FS-MPC control can be seen to substantially outperform the other two control methods, achieving substantially lower THD and achievable LF bridge frequencies, while also maintaining a fixed peak current limit in the HF bridge. The direct space vector control method, which uses direct space vector modulation with hysteresis bands, is only suitable at relatively high LF bridge switching frequencies, making it unsuitable for megawatt scale applications. In addition, it also requires a relatively high HF bridge peak current rating. The fractional power control method, which does not have inherent constraints imposed on the HF bridge's currents, outperforms the direct space vector method, but has higher THD and HF bridge peak currents at frequencies below 5 kHz.

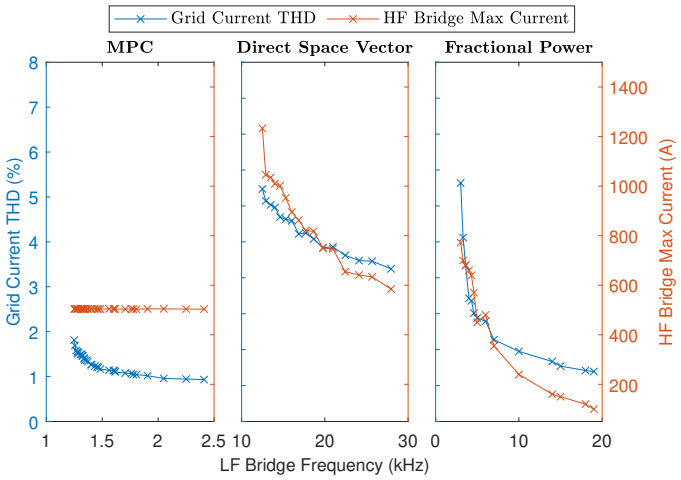


Fig. 10: Comparison of three different control methods on achievable Pareto front of LF bridge switching frequency and THD. L_{HF_γ} = 0.3 pu, $L_{LF_{\alpha/\beta}}$ = 0.075 pu, $L_{HF_{\alpha/\beta}}$ = 0.03 pu , $L_{G_{\alpha/\beta}}$ = 0.075 pu. For MPC control, f_{MPC} = 100 kHz, $N_{horizon}$ = 1, $\hat{i}_{bnd}$=500 A.

V. Real-Time FPGA Implementation of MPC Controller

Results in the previous section have demonstrated that there are notable performance benefits that can be achieved by moving to a long-horizon MPC algorithm. The primary challenge in implementing longer horizons MPC for the PHC is that there are 64 potential switching states that must be considered, in comparison to 8 in the case of a standard two-level converter. The solution space therefore becomes extremely large at even small horizon numbers and the controller also requires a fast calculation and execution time. Methods such as sphere-decoding have been proposed for both drive and grid-connected applications, focusing on two and three-level converters [33], [34]. To solve the problem that the classic sphere-decoding algorithm cannot handle the constraints in cost function which in the case of the PHC is necessary to ensure the current limit of the HF converter is respected during normal operation. In [33], [35], a method to initialise constrained sphere radius by combining the constrained and unconstrained spheres is demonstrated. In [36], it demonstrates a method to reduce further the candidate-solution set by sorting the traverse sequence and verified by the FPGA-in-the-Loop simulation. However, the common feature of these methods is that they work in series, which limits the achievable controller frequency. In order to accelerate the execution time in the FPGA and utilise the FPGA hardware resource efficiently, this section presents a Multi-Thread Depth-First search algorithm that allows horizon steps of 2 to be achieved at controller frequencies of up to 100 kHz on medium-cost FPGA hardware.

A. Design of Multi-Threaded Depth-First Search Algorithm

Depth-First search (DFS) is a well-known algorithm used to efficiently solve tree traversal or mazes problems [37]. This algorithm traverses all potential switching possibilities on the tree and prunes useless branches by updating the global minimum cost value J_{min}. The basic concept of DFS in the thread is shown in Algorithm 1 pseudo code. After traversing, the branch with the minimum cost value J_{min} will be chosen to be the next optimal switching state for the converter.

Algorithm 1 DFS based algorithm pseudo code for single thread

```
1: function DFS(J, X, Horizon)
2:     if J ≥ J_min then
3:         return
4:     end if
5:     for U ← States 1 to States 64 do
6:         X_new = StateSpaceFunction(A, B, E, X, U, V)
7:         J_new = J + CostFunction(X_new, U)
8:         if J_new ≤ J_min then
9:             if Horizon = N_p then
10:                J_min = J_new
11:                return
12:            end if
13:            return DFS(J_new, X_new, Horizon + 1)
14:        else
15:            continue
16:        end if
17:    end for
18: end function
```

Algorithm 2 DFS based algorithm pseudo code for parallel threads

```
1: function DFS(Thread Updated Data)
2:     if J ≥ J_min then or At Boundary
3:         CALL Movement TYPE 3
4:         return
5:     end if
6:     X_new = StateSpaceFunction(A, B, E, X, U, V)
7:     J_new = J + CostFunction(X_new, U)
8:     if J_new ≤ J_min then
9:         if Horizon = N_p then
10:            J_min = J_new
11:            CALL Movement TYPE 2
12:            return
13:        end if
14:        CALL Movement TYPE 1
15:        return
16:    else
17:        CALL Movement TYPE 2
18:    end if
19: end function
```

The DFS pseudo code above also needs to transform into cascade instead of recursive functions in order to be synthesisable on FPGA hardware. In the proposed implementation, the search area is divided into several equal subtrees that are each searched by each independent thread. Each thread's working pattern is following the concept shown in Algorithm 2. It is not necessary for each thread to traverse all branches of its own tree, because the thread can prune the branch or node by the global updating J_{min} and also update this value if they find a better solution. Therefore, the thread processor will find different optimal solutions at different times. This global updating parameter accelerates the system's execution time.

B. Synthesis and Implementation of Algorithm based on FPGA

To illustrate the idea of the FPGA-based Multi-Thread Depth-First search algorithm, the control flow diagram example is shown in Fig. 12. Each block function will be explained as follows:

Movement Block: This block controls the movement of a thread to a new node, using three basic moving types. *TYPE 1*: Traverse down. This is the common case for the thread to search longer horizon switching cases, while the J_{new} is lower than the J_{min}. *TYPE 2*: Move to a different node in the same level. This moving operation happens while the J_{new} after the cost function is higher than the J_{min} or the thread is in the leaf node. *TYPE 3*: Backtrack to upper level. If the input J is higher than the J_{min} or the thread is on the boundary, the thread will backtrack to the upper level and explore a new different location. A search example is shown in Fig. 11.

Calculation Block: This block calculates the cost function at the current node, shown in Algorithm. 2 line 6, 7.

Global minimum cost and pruning: This block controls the pruning of nodes, as shown in Algorithm. 2 line 2. When the current J value is greater than the global J_{min}, this branch will be pruned and back to the upper level.

Thread Memory and Predefined Assignment block: Each thread processor has its own memory array to store the necessary parameters to enable a backtrack movement, including visited states, visited costs and locations. In this way, the thread can save time from duplicated computation. Splitting the subtree equally is achieved by defining the assignment and boundary nodes at a lower level than the root node. The boundary node is a node that indicates the finish point of the predefined assignment. After crossing the boundary node, the thread completes its own search, updates the globally optimal solution (if it exists) and then stops and waits for the end of the other parallel thread processors.

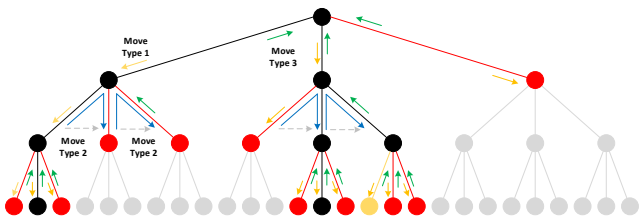


Fig. 11: Searching process illustration on a tree with 3 horizon levels. The thread begins searching from the left subtree and the arrows show the searching track. Black node indicates the valuable node, the red node indicates the pruned nodes, and the yellow node indicates the optimal solution.

The end condition and thread management block manages each thread's location and checks whether the search is complete. The results collector and sharing data block will update each thread's output information globally and prune branches in the search tree by updating the global minimum cost value J_{min}.

This algorithm was coded in C and converted into HDL code using Xilinx High-Level Synthesis (HLS) tools. Table

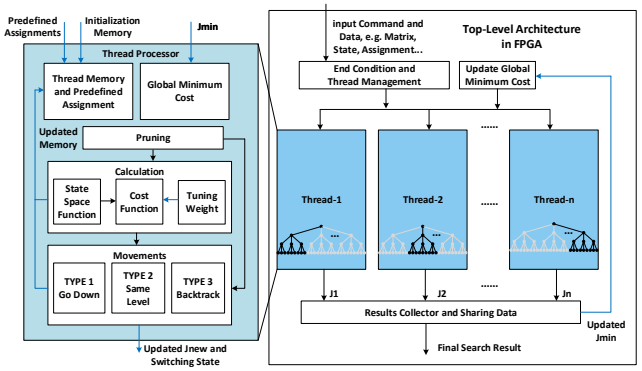


Fig. 12: Control flow diagram of the FPGA implemented Multi-Thread Depth-First search algorithm.

III compares the statistics of required FPGA resources and run-time with variation in threads number = [1, 8, 16, 32, 64] and $N_{horizon}$ = [1, 2, 3] using run-time data extracted from a Simulink simulation and implementation results from Xilinx HLS tools. Table IIIa shows the measured algorithm average calculation cycles for different horizon step and thread numbers, while Table IIIb shows the FPGA (Kintex-7 xc7k325t-1fbg900) synthesis resource utilisation for each control implementation. While the 1-64 thread implementations with $N_{horizon}$ = 3 are synthesizable, the average number of clock cycles required (given by the product of the calculation cycle and the number of clock steps per cycle) exceeds the maximum 1000 value required to achieve real-time performance with a 10 μs controller time-step and a 100 MHz FPGA based clock. After the particular optimisation for the $N_{horizon}$ = 2 case with 64 threads case, it is both synthesizable and achieves a max total clock cycle value of 845, which satisfies the 100 kHz control time. The results also indicate that a 200 kHz control time-step 2-step controller may be achievable on an unlocked version of the same FPGA, or a 2-step 100 kHz implementation using the 64 threads implementation.

VI. Experimental Results

To validate the design of the PHC and the performance of the developed real-time FS-MPC controller experimental testing of the topology was performed using the prototype converter shown in Fig. 13. A dSPACE real-time MicroLabBox rapid control prototyping platform was used as the controller, with the FS-MPC controller implemented on its onboard Xilinx Kintex-7 xc7k325t-1fbg900 FPGA. Supervisory control and reference generation were implemented on the CPU portion of the MicroLabBox. A six-pulse rectifier was used as the dc-supply and a 30 kVA ETPS four-quadrant power-supply was used as the AC supply. The cabinet was originally scaled for a 90 kVA power rating, but due to the unavailability of a DC supply with this power-rating the DC voltage and power-rating of the converter was scaled to maintain the per-unit impedance of the inductances. Measurements were performed using a combination of the MicroLabBox's internal data-logging system logging measurements from the converter's voltage and current sensors, and voltages/currents from a

TABLE III: Comparison of the impact of the number of threads and the MPC horizon step number on the execution time and resource requirements of the FPGA FCS-MPC implementation.

(a) FPGA calculation cycle performance

Horizon Step	Thread Number	Avg/Max Cycle	CLK Per Cycle	Avg/Max Total CLK
1 Horizon Step	1	64/64	13	832/832
	8	8/8	13	104/104
	16	4/4	13	52/52
	32	2/2	13	26/26
	64	1/1	13	13/13
2 Horizon Steps	1	754/4160	13	9802/54080
	8	177/520	13	2301/6760
	16	121/260	13	1573/3380
	32	89/130	13	1157/1690
	64	54/65	13	702/845
3 Horizon Steps	1	5108/266304	13	66404/3461952
	8	955/33288	13	12415/432744
	16	608/16644	13	7904/216372
	32	289/8322	13	3757/108186
	64	259/4160	13	3367/54080

(b) FPGA resource utilization (Kintex-7 xc7k325t-1fbg900)

Horizon Step	Thread Number	DSP/(%)	FF/(%)	LUT/(%)
1 Horizon Step	1	11 (1%)	2801 (1%)	1807 (1%)
	8	60 (7%)	32643 (8%)	12160 (6%)
	16	116 (14%)	64338 (16%)	25353 (12%)
	32	228 (27%)	127630 (31%)	54790 (27%)
	64	452 (54%)	253601 (62%)	120785 (59%)
2 Horizon Steps	1	11 (1%)	3223 (1%)	2983 (1%)
	8	60 (7%)	28613 (7%)	30298 (15%)
	16	116 (14%)	55754 (14%)	63178 (31%)
	32	228 (27%)	111141 (27%)	131381 (64%)
	64	452 (54%)	184401 (45%)	164765 (81%)
3 Horizon Steps	1	11 (1%)	3879 (1%)	3786 (2%)
	8	60 (7%)	35574 (9%)	38045 (19%)
	16	116 (14%)	70872 (17%)	77114 (38%)
	32	228 (27%)	141347 (35%)	157882 (77%)
	64	452 (54%)	278110 (68%)	331305 (163%)

single phase using a Tektronix MSO4104B 1 GHz oscilloscope and differential voltage probes with a 50 MHz bandwidth and current measurements with a 2.5 MHz bandwidth. Details of the converters parameters and output filter inductance values are given in Table IV. Commercial three-phase inductors were used for the LF bridge output inductor. The grid-interfacing transformer was measured to have a leakage inductance of approximately 1% pu, substantially below what would be expected in a multi-megawatt grid-scale transformer and so additional inductors were added to increase the effective value of the grid-side inductance. A custom common-mode choke was wound using FS-650060-2 cores from MicroMetals. The common-mode and differential mode inductance of this choke was measured using an impedance analyser, with the differential inductance being sufficiently large that no additional dedicated differential mode inductance was used for the HF bridge differential output inductance. The details of the common-mode choke are also given in Table IV.

A. Steady-State Tests

Fig. 14 shows the time-domain waveforms from single phase C of the converter while it is running at fully rated power. From the diagram, the HF bridge currents can be seen to be tightly contained within the defined 22 A current limit, while the LF bridge achieves an average switching frequency of 1120 Hz and the THD of grid side current is about 2.79%, below the recommended limit given by IEEE 519-2014 [38]. Also of note in this waveform is that the majority of the switching actions of the LF bridge occur around the zero-crossing of the current, with only a small number of switching instances when the current is at its peak magnitude.

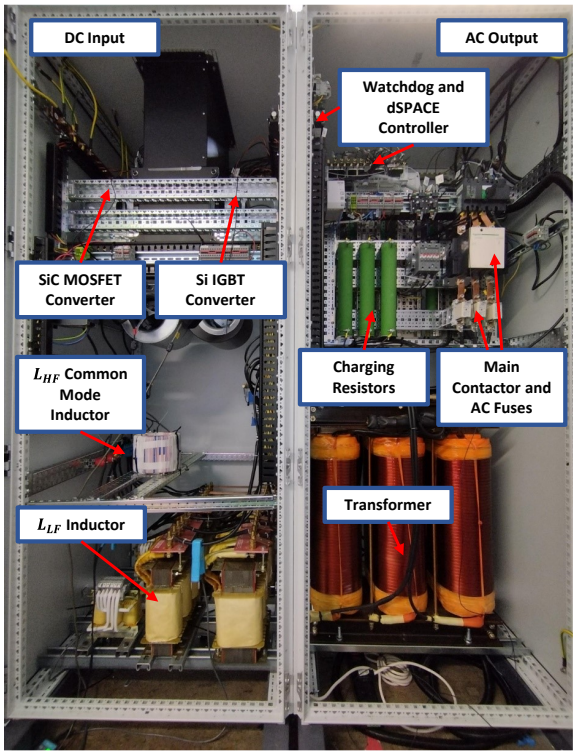


Fig. 13: Si/SiC Parallel Hybrid Converter in the power electronics lab.

TABLE IV: Experimental converter components and parameters

Experiment System Parameters	Value
S	16.9 kVA
V_{DC}	300 V
V_{line}	172.5 V
Z_{base}	1.76 Ω
L_{base}	5.6 mH
$L_{LF_{\alpha/\beta}}$	420 μH (0.075 pu)
$L_{G_{\alpha/\beta}}$	420 μH (0.075 pu)
$L_{HF_{\alpha/\beta}} : L_{LF_{\alpha/\beta}}$	0.3741
Grid Frequency	50 Hz
Look-ahead Horizon	2 Steps
Controller Time Step	100 kHz
Current Limit	22 A
Tuning Weight Information	
Q_{quad} ($Q_{quad_{G\alpha}}, Q_{quad_{HF\alpha}}, Q_{quad_{G\beta}}, Q_{quad_{HF\beta}}, Q_{quad_{HF\gamma}}$)	[1, 0.03225, 1, 0.03225, 0.03225]
Q_{SW} ($Q_{SW_{LF}}, Q_{SW_{LF}}, Q_{SW_{LF}}, Q_{SW_{HF}}, Q_{SW_{HF}}, Q_{SW_{HF}}$)	[28, 28, 28, 14.55, 14.55, 14.55]
Q_{CL}	80000
L_{HF} Common-Mode Inductor Information	
Core	Micrometals FS-650060-2
Num. of Turns	26
Wire Size in AWG	18
Num. of Wire Strands	2
Num. of Cores Stacked	4
Winding Self Inductance	606 μH
Coupling Factor	0.739
$L_{HF_{\alpha/\beta}}$	157.12 μH (0.028 pu)
$L_{HF_{\gamma}}$	1485 μH (0.265 pu)
Si and SiC Module Information	
Si IGBT Module	SEMITRANS SKM600GB126D
SiC MOSFET Module	Wolfspeed WAB300M12BM3

Fig. 15 shows the measured relationship between the output total harmonic distortion (THD) and the switching frequency of the LF bridge under different $i_{bnd} : \hat{i}_{phase}$ (defining the ratio between the HF bridge current limit and the peak phase current) conditions. These values of $i_{bnd} : \hat{i}_{phase}$ were selected to align with an efficiency estimate case study for a megawatt-scale converter using different SiC module choices for the HF bridge given in Section VII. It also compares three output waveforms at different specific switching frequencies. In the low-frequency region, the parameter $i_{bnd} : \hat{i}_{phase}$ significantly influences the starting point of the grid current's THD. In the high-frequency region, all three cases gradually converge towards the same output THD. It should be noted that the frequency of the LF bridge can be further reduced by adjusting the tuning weight of the cost function. However, increasing the tuning weight will also result in an increase in THD.

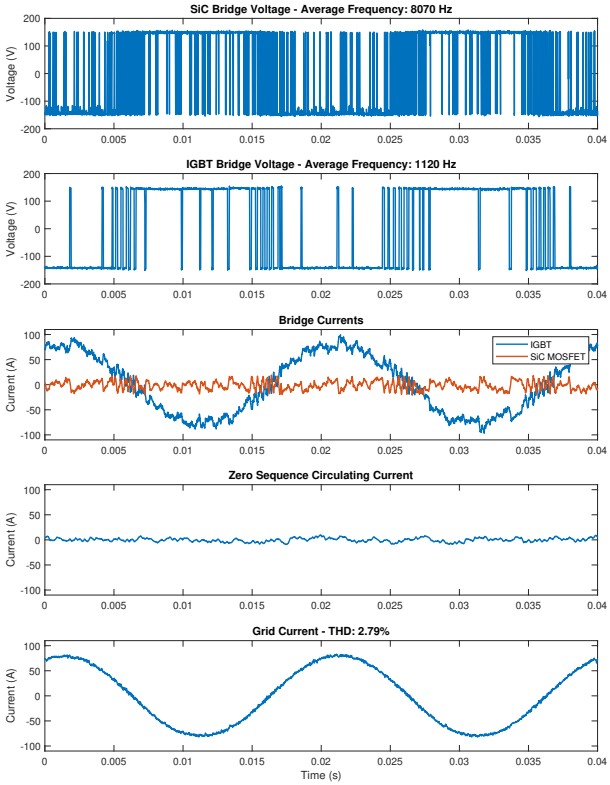
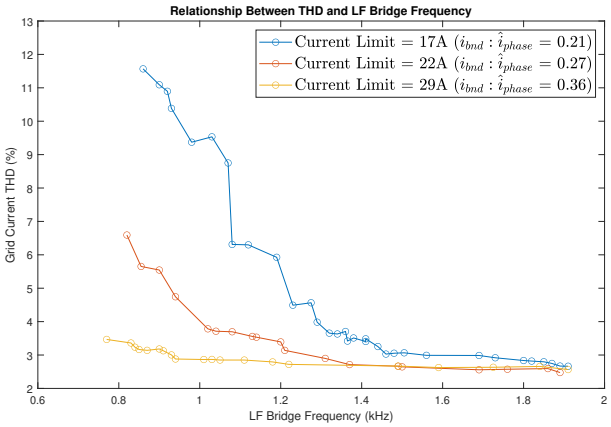


Fig. 14: Experimental voltage and current waveforms from a phase C of the PHC at a set-point of 1 pu P and 0 pu Q - measured using a Tektronix MSO4104B oscilloscope.

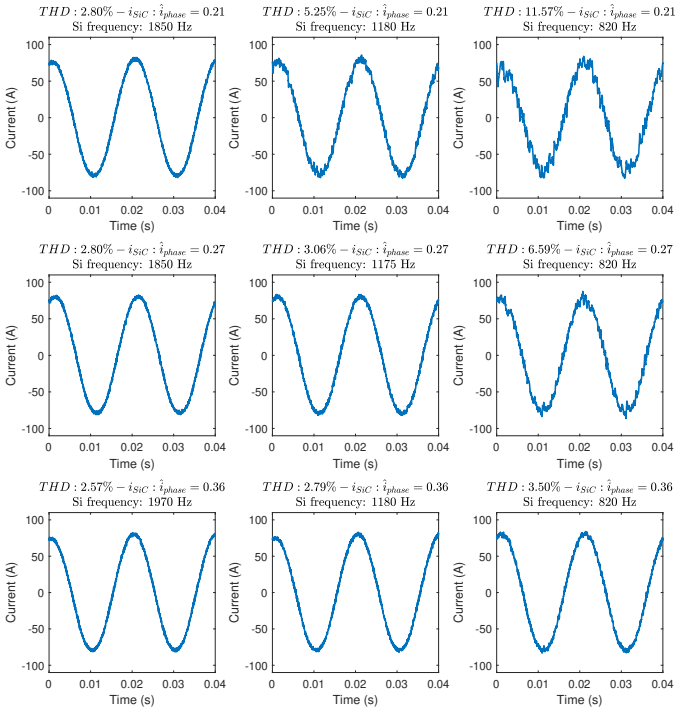
B. Dynamic Response Testing

The ability of the implemented controller and the PHC converter to switch operation modes between high-current mode, where the grid current is conducted by a combination of the LF bridge and the HF bridge, and low-current mode, where just the SiC MOSFETs bridge conducts the grid-current, was also tested in the experiment, with results of this test are shown in Fig. 16. This shows the converter ramping its power output downwards to a level where the IGBT bridge can be blocked and the grid-current conducted wholly by the SiC bridge. The power set-point is then ramped back upwards with the PHC switching back to its high-current operation mode. Minimal disturbance to the grid-side current can be observed as the PHC switches between the two-modes, with the current within the SiC bridge contained within the defined current limit.

The performance and robustness of the implemented controller under faulted scenarios was also tested, with Fig. 17a giving the results from a three-phase fault with the retained voltage at 0.3 pu. The obtained results indicate that the system is capable of dynamically responding to the reference signal during both the fault and recovery periods. The ability and robustness of the implemented control to reject harmonics present in the external grid-voltage was also tested, with



(a) Measured relationship between THD and LF Bridge frequency.



(b) Grid current waveforms at different frequencies, from top to bottom current limit = 17, 22, 29 A ($i_{bnd} : \hat{i}_{phase}$ = 0.21, 0.27, 0.36)

Fig. 15: Comparison of experimentally measured waveforms at different average switching frequencies of the LF bridge, with variation in the ratio of the HF bridge current limit to the peak phase current ($i_{bnd} : \hat{i}_{phase}$).

results given in Fig. 17b, where a combination of 5th and 7th harmonic is introduced to the grid voltage waveform for 100 ms. The results show good robustness of the control to this disturbance.

VII. Power-Loss Estimates

This section presents an estimation of the semiconductor power-losses within a PHC rated for 1.5 MW, considering the use of three of the most recent commercially available 1700 V Silicon Carbide MOSFETs modules from Wolfspeed within the HF bridge, shown in Table V, with data from a 1700 V, 1800 A IGBT used for the LF bridge. Conduction/switching characteristics at junction temperatures of 125^oC from the datasheets of the devices were used. Bench-mark power-losses

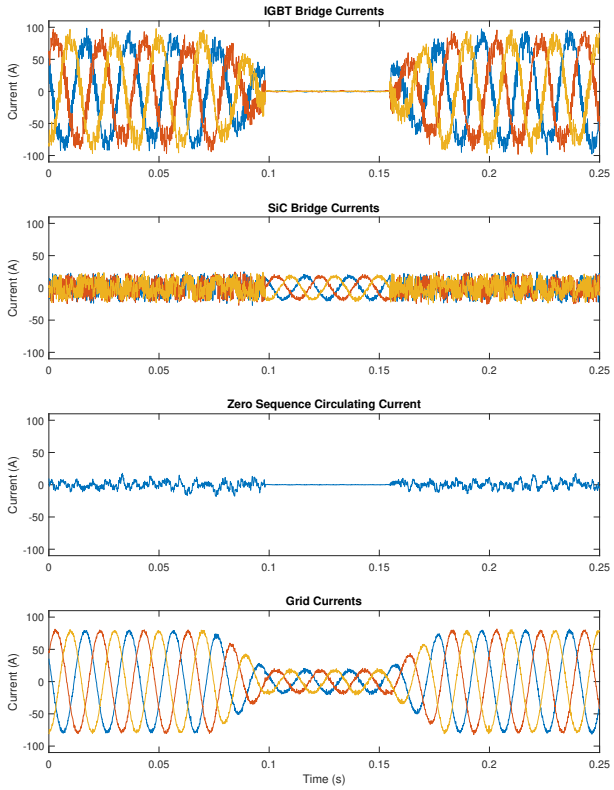


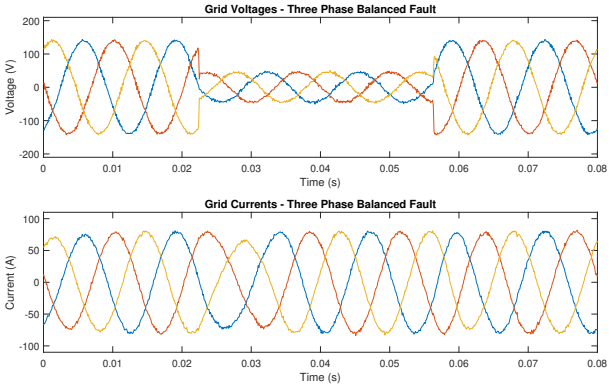
Fig. 16: Experimental PHC converter transitioning from high-current mode to low-current mode and then back to high-current mode - measurements logged using the dSPACE MicroLabBox data-logging system.

when considering a fixed-frequency converter of the same power-rating operating at 2.5 kHz (in the typical range for a two-level converter of this power-rating) were also made for comparison. Semiconductor power-losses are estimated using the method detailed in [39]. The current limit used with the FS-MPC controller is set to equal the current rating of the SiC MOSFETs module considered in each case. The use of the blocked IGBT operation once the grid-current falls below the rated current of the SiC MOSFETs module, as proposed in [23] is also considered to increase efficiency at low power set-points.

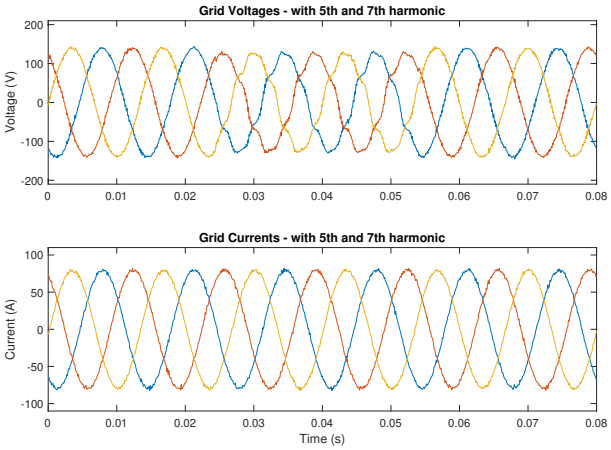
TABLE V: Power-Semiconductor device parameters used within power loss estimates.

Item	CM1800DY-34S	CAS380M17HM3	CAB500M17HM3	CAB650M17HM3
$i_{bnd} : \hat{i}_{phase}$	-	0.21	0.27	0.36
Blocking Voltage	1700 V	1700 V	1700 V	1700 V
Current Rating	1800 A	380 A	500 A	650 A
Forward Cond. Bias	0.75 V	0 V	0 V	0 V
Forward Cond. Slope	0.85 mΩ	5 mΩ	3.66 mΩ	2.38 mΩ
Rev. Cond. Bias	0.9 V	0 V	0 V	0 V
Rev. Cond. Slope	0.9 mΩ	3.2 mΩ	3.92 mΩ	2.58 mΩ
Turn On Bias	0 mJ	5 mJ	0 mJ	0 mJ
Turn On Slope	0.36 mJ/A	0.0257 mJ/A	0.082 mJ/A	0.1 mJ/A
Turn Off Bias	0 mJ	1 mJ	0 mJ	0 mJ
Turn Off Slope	0.324 mJ/A	0.02 mJ/A	0.05 mJ/A	0.069 mJ/A
Rev. Recovery Bias	0 mJ	2.5 mJ	0 mJ	0 mJ

The power-loss estimates and average switching frequencies for the three considered SiC MOSFETs Module choices are given in Fig. 18. It can be seen that the LF bridge switching frequency varies with the choice of SiC MOSFETs module, with the SiC modules with higher current ratings (allowing a higher current limit for the HF bridge to be set in the MPC control) achieving lower LF bridge switching frequencies. The

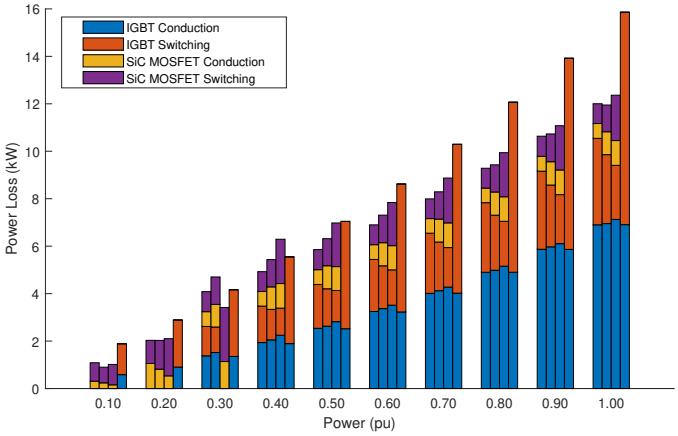


(a) Three-phase balanced fault test with a retained voltage of 0.3 pu.

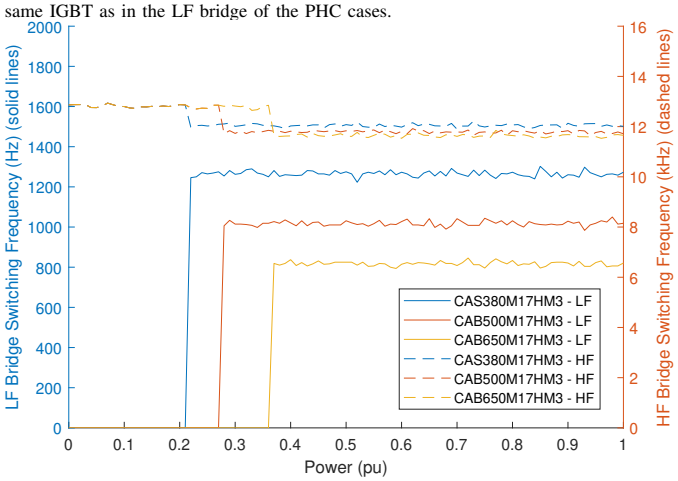


(b) Grid voltage harmonic injection in with 5^{th} harmonic (5%) and 7^{th} harmonic (5%). Grid current THD is 3.2% and LF bridge average frequency is 1610 Hz during the harmonic injection period.

Fig. 17: PHC grid voltage and grid currents under two dynamic test scenarios.



(a) Power-Semiconductor loss estimates. HF bridge semiconductor device in each group (left-to-right): CAS380M17HM3, CAB500M17HM3, CAB650M17HM3. Right-most bar in each group gives an estimate of the losses in a 2.5 kHz two-level converter using the same IGBT as in the LF bridge of the PHC cases.



(b) HF and LF bridge average switching frequencies. (HF bridge: dashed line; LF bridge: solid line)

Fig. 18: PHC power-semiconductor loss estimates and switching frequencies considering designs that use CAS380M17HM3, CAB500M17HM3 and CAB650M17HM3 modules for the HF bridge. $L_{LF_{\alpha/\beta}}$ = 0.075 pu, $L_{G_{\alpha/\beta}}$ = 0.075 pu, $L_{HF_{\gamma}}$ = 0.3 pu, $L_{HF_{\alpha/\beta}}$ = 0.03 pu, $N_{horizon} = 2$.

drop in the LF bridge frequency corresponds to a transition between high-current mode and low-current mode (where the LF bridge is blocked and the HF bridge conducts the entire grid current). When examining the power losses at 1 pu active power there is only a slight variation between the power losses in the three considered PHC cases, reduced IGBT switching losses achieved using the SiC MOSFETs module are mostly cancelled by higher conduction and switching losses in the SiC MOSFETs module itself. All three PHC cases achieve an approximate 25% overall power-semiconductor loss reduction at 1 pu power, with the difference reducing at partial power set-points. The case with the highest rated SiC MOSFET (and so highest current limit) being able to transition to low-current mode at the higher power set-point than the other two cases. The IGBT conduction loss is dominant at high power set-points. The flexibility of the PHC concept means further power-loss reductions could potentially be achieved by using an oversized or conduction loss optimised IGBT in the LF bridge.

VIII. Conclusion

This article investigated the design and control of the Parallel Hybrid Converter, focusing on its use in megawatt-scale converter applications. The impact of the converters output filter impedance on the achievable performance was investigated using a Non-Denominated Set Genetic Algorithm to automatically provide tuning weights for the Finite-Set MPC controller. The impact of the FS-MPC controller time-step and horizon length was also investigated, indicating the majority of performance gains can be achieved with a low horizon length. A 2-step Multi-Thread Depth-First search algorithm was proposed and used to implement the FS-MPC controller into the medium-cost FPGA hardware. The performance of the PHC and its real-time control was verified by experiment using a prototype converter, demonstrating that THD values 2.79% can be achieved while having an average switching frequency in the LF bridge of 1120 Hz, while also keeping current in the HF bridge tightly controlled within its defined current limit. This is achieved using a purely inductive output filter, eliminating any requirements for passive filter damping which can cause considerable additional losses in megawatt-scale converters. Additionally, the ability of the converter to switch operation between high-current mode, where both the LF bridge and HF bridge are operational with the LF bridge processing the majority of the grid-current,

and low-current mode, where the LF bridge is blocked was verified by experiment. The dynamic response performance of the converter is also verified by common system fault and harmonic injections in the experiments. Power-semiconductor power-loss estimates for a case-study 1.5 MW PHC with a 1200 V DC voltage were made considering three potential SiC MOSFETs. These losses were compared against the estimated losses in a 2.5 kHz fixed frequency two-level converter using the same IGBT as considered for the LF bridge in the PHC cases, indicating potential efficiency gains. The results also showed that while the selection of a SiC MOSFET with higher current ratings for use in the HF bridge enables a lower LF bridge switching frequencies, this does not necessarily result in significant efficiency gains versus the use of a lower current SiC MOSFET. This is a result of the decrease in switching losses in the LF bridge being mostly cancelled by increased switching losses in the HF bridge. The optimal current rating ratio between power semiconductors used in both bridges for any application would require a full techno-economic study and may vary based on the relative performance of the devices used in each bridge.

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