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Optocoupler Integration of LTCC-based Gate Driver in a SiC Power Module

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ABSTRACT

The growing demand for electrical energy in today's industrialized economy has driven the need for innovative approaches to meet diverse application requirements. Notably, advancements have been made in the field of power electronic systems, as reliable power electronic converters are essential for managing multiple power sources and loads. However, the development of these systems poses challenges related to power device switching speed, system weight and size, and power losses. The integration of a gate driver into a SiC power module offers a solution to many of these challenges, thereby driving the advancement of electrical power density expansion.

An LTCC-based gate driver with an LTCC-based optical isolator was developed and integrated into a fabricated 1.2kV SiC power module. This development was done specifically for high temperature applications as part of a wider research on the reliability of the integrated power module at higher temperatures. Therefore, this high temperature gate driver integrated SiC power module was tested from 25^{o}C to 200^{o}C. Double pulse testing of the fabricated integrated SiC power module was done to characterize the switching performance of the power module. The test results indicate a minimal voltage overshoot of approximately 3.5V during both the turn-on and turn-off periods. Additionally, the current overshoot ranges from ~5A to ~8A as the temperature increases from 25^{o}C to 200^{o}C. The results show good switching performance resulting in minimal losses over higher temperatures. Therefore, with these results, the integrated SiC power module can enhance better power density, and lower losses even in high temperature applications.

ACKNOWLEDGMENTS

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1.1 Research Background and Motivation

Present-day industry and society require large amounts of electrical energy for operating electrical circuits such as inverters, converters, motor drives, etc. This significant increase in demand for electrical energy has spurred the development of advanced ways to meet the requirements of various applications within the currently industrialized economy. A noticeable advancement is in the area of power electronic systems as reliable power electronic converters are necessary in operating multiple power sources and loads. The challenging development surrounding reliability of these systems involve switching speed of the power device, weight and size of the system, and power losses. Using a gate driver integrated SiC power module in the system solves a lot of these challenges, thus, advancing electrical power density expansion.

Power electronic module is a compact interconnection of multiple power semiconductor devices together with their control circuitries for use in powering electronic systems [1]. The use of multiple technologies in fabricating the power module is advancing rapidly. Technologies like semiconductor chip attachment, wire bonding and encapsulation are some of the technologies used among others [2]. A basic power semiconductor module consists of a stack of four main parts that are power semiconductor chips, insulating substrate with metallization, baseplate, and bonding material [2].

Integrated power modules are desired for various reasons that include their high-power density, small overall system size, and simplicity in performance [3]. Industry and academic efforts are focused on increasing power density of power converters by increasing power ratings and decreasing size [4]. Advanced and proper packaging of these power electronic modules are thus important as their level of performance and reliability is directly affected. Recent advances

in packaging technologies have tried to address the limitations of standard packaging techniques in both packaging elements and package structures [5]. With these advanced packaging techniques, power modules can be optimized for their high electric fields while reducing the challenges high-voltage and high temperature application poses [6].

1.2 Silicon Carbide Power Modules

1.2.1 Overview of (Wide Bandgap) WBG Devices

Among the various wide bandgap (WBG) materials, the 4H SiC (Silicon Carbide) and GaN (Gallium Nitride) are the relevant ones in today's semiconductor devices world amidst the silicon semiconductor industry dominance. These WBG semiconductor devices are universally seen as the future devices to dominate the power electronics field. The distinct properties of the WBG devices that give them an edge over Si devices are significant especially in regards to on-state resistance (R_{ON}) and breakdown voltage (V_{BR}) which results in a reduction of the power losses when compared to Si devices.

Table 1.1: Wide bandgap fundamental properties comparison [19].

WBG Fundamental Properties	Si CMOS	4H-SiC	GaN HEMT
Critical Electric Field (MV/cm)	0.3	3	3.5
Energy Bandgap (eV)	1.12	3.23	3.4
Electron Mobility (cm2/V-s)	500	35	1500
Electron Saturation Velocity (10^7 cm/s)	1	1.8	3.4
Thermal Conductivity (W/K-cm)	1.3	3.7	1.5

Table 1.1 shows the value of the properties associated with semiconductors. It can be seen that WBG semiconductor devices clearly have advantages over Si devices. Some of the properties that distinct WBG devices from Si devices are as follows:

Wider band gap- The figure below shows a pictorial view of the WBG materials as compared to Si semiconductor, and it is clear that WBG materials cover more space in the energy gap which means higher activation energies in the semiconductor materials [7].

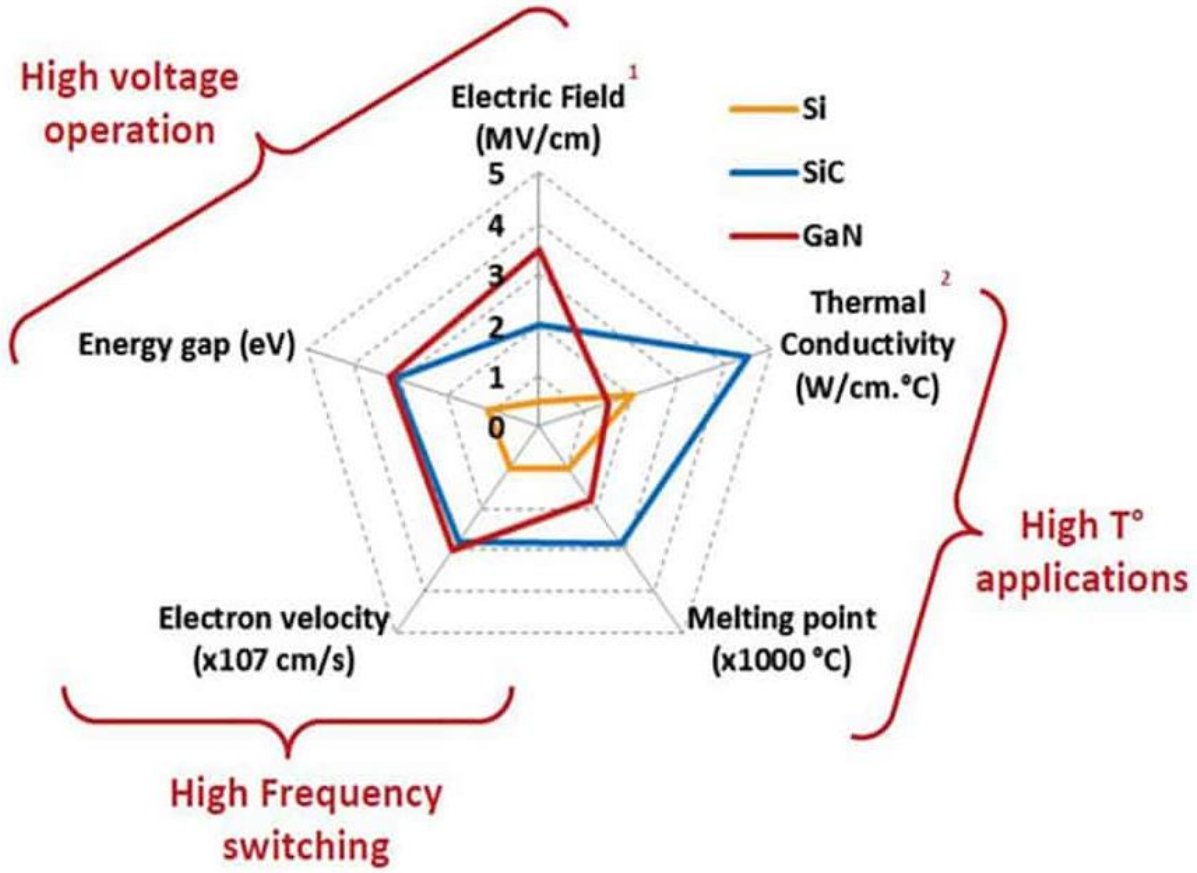


Fig. 1.1: GaN, SiC and Si Energy Band Gap Comparison [20].

Higher electric breakdown field- The wider energy gap of WBG devices typically above 3 eV translates to a higher electric breakdown field. This property is important in achieving large blocking voltage which in effect results in high voltage operation [19].

Higher thermal conductivity- The thermal properties of SiC and GaN are such that they can reach a high operating temperature which is important in extreme application conditions. Specifically, the SiC is at the forefront of this property as it has the potential to operate at temperatures in excess of 1,200 K [21]. Due to the packaging limitations of the device and technology as well as being bereft of information on safe operating temperatures, most commercialized SiC power MOSFETS operate at temperatures of up to 573 K [22].
Higher electron saturation velocity- This property directly relates to the device's ability to switch at higher frequencies. GaN is a more dominant device in this area as it has a significantly higher mobility and saturation velocity in the two-dimensional (2-D) channel FET (Field Effect Transistor) due to a very high density of 2-D electron gas at GaN/AlGaN interface [23].

WBG semiconductor devices, despite their overwhelming superiority as compared to Si, still have significant reliability issues which in effect restricts its industry wide adoption and application. Silicon semiconductors' dominance is due to the deep knowledge and matured technology available; hence it is widely adopted. SiC has made great strides over the years but its limited application is due to its low channel mobility issue [24]. Although SiC is currently dominant and competitive in applications requiring higher power density and operating temperature. These application areas typically feature the need for reduced device size and lower switching loss, hence better efficiency, which is within SiC capability. In the case of GaN devices, they can be considered the least technologically matured despite its wide market availability in optoelectronic applications and radio frequency [25]. GaN semiconductors still report reliability issues in terms of the low hole mobility and poor contacts. However, GaN devices have promising superior properties in high switching frequency application and it's

unique heterostructure nature which produces lateral devices suitable for monolithic integration [19], [25].

According to status of the power electronics industry report released by Yole's Group, the WBG power semiconductor market is expected to reach 3 billion by 2027 which is a growth of ~22 % from 2019 to 2027 [26].

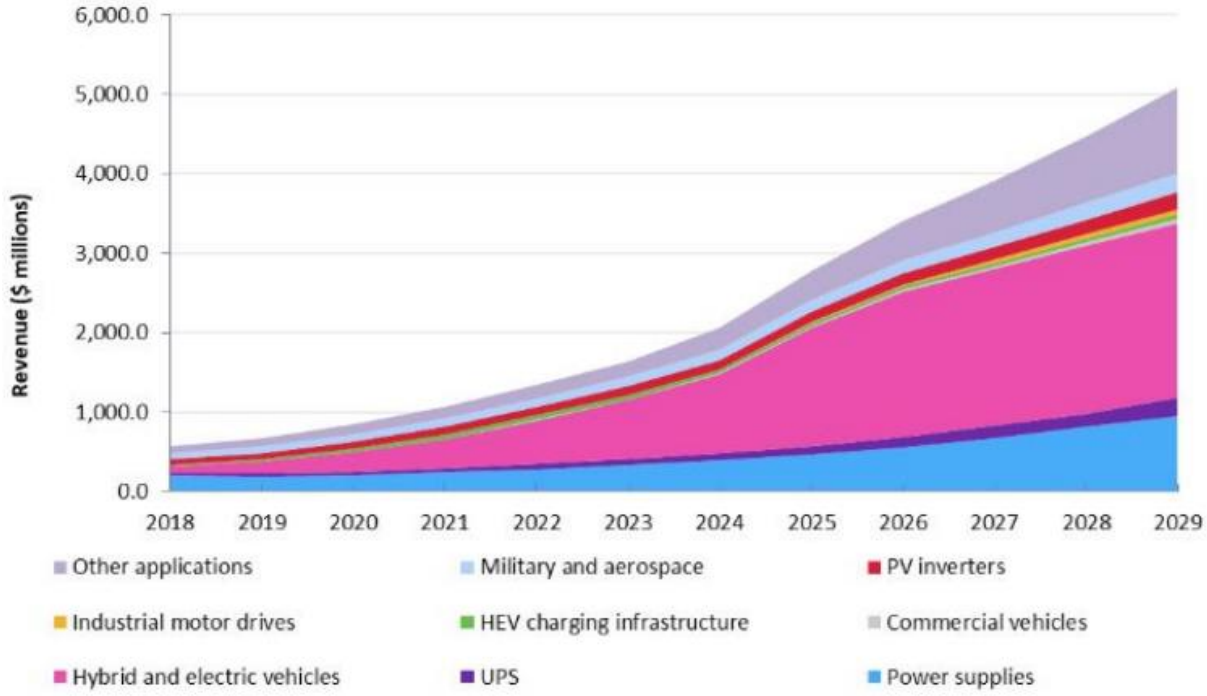


Fig. 1.2: Industry application of SiC and GaN Semiconductors [27].

The figure above shows the projected revenue generated from different industries using wide bandgap semiconductor devices. This immense growth is spurred by the electric vehicle market as major players in this industry like Tesla and BYD are adopting SiC-based modules.

1.2.2 Introduction to a Conventional SiC Power Module

Figure 1 shows a conventional power module layout. This layout represents a half-bridge, wire bonded, SiC power module which was designed using ANSYS Q3D software. There are basically two important layout design considerations to examine when designing a power module layout. First, it is important to understand that when the switching frequency is high, large voltage spikes results due to the high rate of current rise. So, by reducing the parasitic inductance, the magnitude of these voltage spikes can be reduced. Second, the parasitic inductance between paralleled devices for multi-die power modules needs to be balanced. This helps to achieve equal current distribution in parallel devices, consequently affecting the performance of the power module as a whole [9].

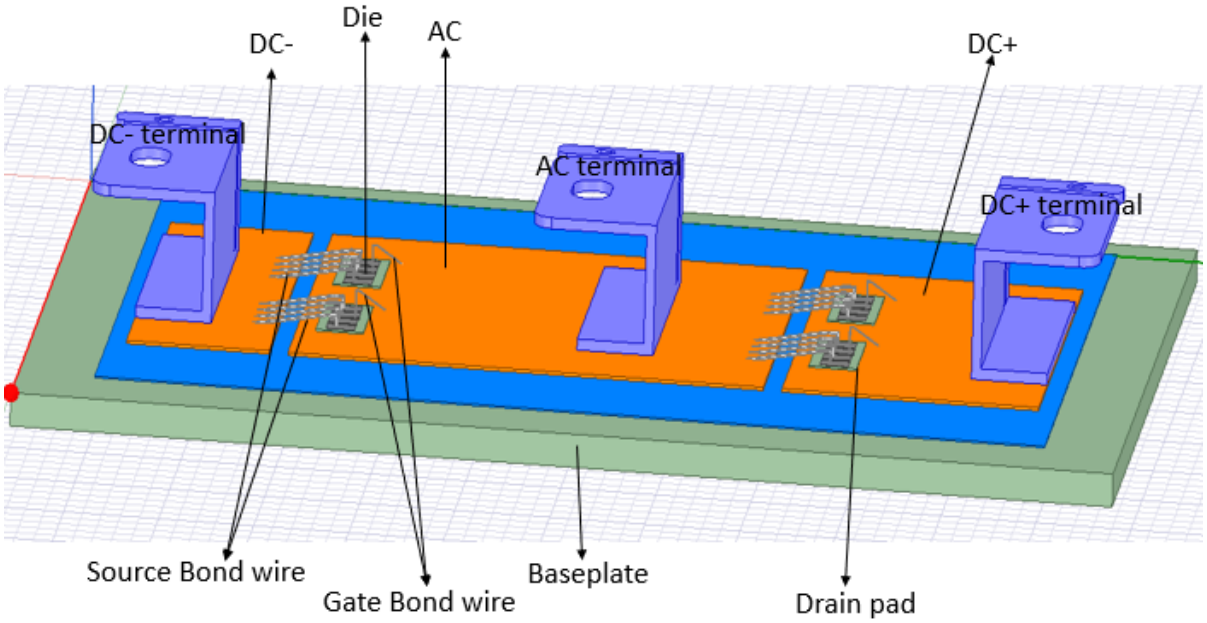


Fig. 1.3: A conventional half-bridge, wire bonded, SiC power module layout is designed using ANSYS Q3D software.

The electrical modeling of a power module, specifically the terminal and the bond wire interconnection is designed using ANSYS Q3D. ANSYS Q3D is a finite element analysis (FEA) software developed by ANSYS Corporation. It is used in conjunction with most computer-

aided-design software (like SolidWorks CAD) to complete the power module design and simulation. It also provides many functions to verify the reliability and performance of electronic devices [10]. In ANSYS 16.0 and subsequent releases, the ANSYS Electronics Desktop application combines electromagnetic fields, circuitry, and system analysis into a seamless working environment within a single, highly integrated interface [11]. ANSYS Q3D is adopted for the design and simulation of the power modules in this paper. The basic procedures for using this software include drawing a geometric model, modifying the model design parameters, setting up the simulation, running the simulation and then reviewing the results of the simulation [2], [11]. Figure 1.4 shows the packaging structure of a conventional wire bonded power module. This was the conventional packaging structure that existed for silicon devices and it has been adopted for silicon carbide devices.

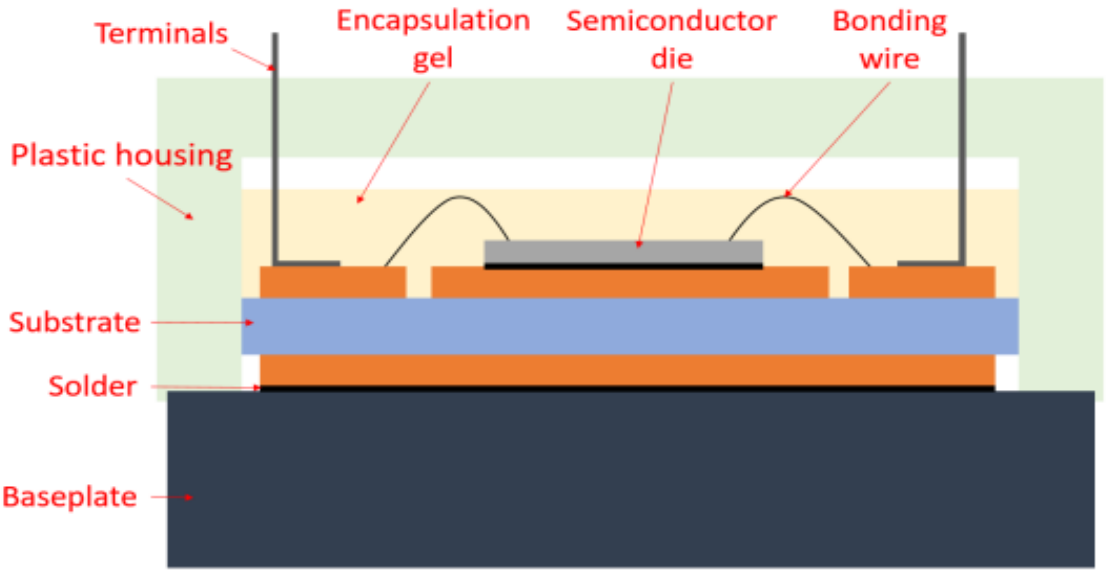


Fig. 1.4: Packaging structure of a conventional wire bonded power module [64].

1.3 Thesis Organization

In this thesis, the design of an opto-isolator gate driver integrated into a SiC power module is explained. The gate driver design process, design requirements for a SiC power module and circuit simulation results together with the board layout is presented. The power module design process is discussed at length. The need for parasitic inductance optimization and parasitic extraction process of the power module is also expounded on. Lastly, the various challenges experienced during the integration of other electronic components, especially the gate driver, to the power module is examined and tackled.

The organization of the optocoupler gate driver integration into a SiC power module explored in this paper is as follows:

Chapter 1 gives a brief introduction on the conventional SiC power module available and the need for parasitic inductance optimization. Chapter 2 discusses the motivation behind integration of the gate driver into a power module as well as an overview of the gate driver design and the challenges of integration. Chapter 3 walks through the design process used to bring about the optocoupler gate driver design integration into a SiC power module and extensively explores the need for an optocoupler. Chapter 4 discusses the fabrication process of a SiC power module, and finally chapter 5 investigates the characterization of the optocoupler gate driver integrated into a SiC power module.

Chapter 6 ends with the conclusions obtained from the design of the optocoupler gate driver integrated into a SiC power module and any future work that could be explored to improve this design.

Chapter 2: Integration of SiC MOSFET Half-Bridge Power Module and Isolated Gate Driver

2.1 Motivation for Integration of Power Module and Gate Driver

The more commercialized Silicon (Si) device has matured and been developed over the years to its limit. Despite the Si device dominance, there has been a clear need for a higher temperature operation, higher power density, higher switching capability and lower switching losses in power electronic systems. These needs have arisen from the varied power electronic application requirements and the hazardous conditions these applications are subjected to. Hence, there has been an increased interest in wide bandgap (WBG) devices such as gallium nitride (GaN) and silicon carbide (SiC) devices which show very promising material device characteristics. SiC mainly targets high-voltage, high-power density applications above 600 V/kW while GaN targets low voltage, low power applications below 600 V/kW [7]. These distinctly improved characteristics are highlighted in Table 2.1 in comparison to Si devices.

Table 2.1: Si and SiC device properties comparison [8].

Property	Silicon	4H-SiC
Band gap, E_g(eV)	1.12	3.26
Intrinsic Carrier concentration N_i (cm^{-3}) at room temperature	1.45×10^{10}	8.2×10^{-9}
Electric critical field, E_c (kV/cm)	300	2200
Electron mobility, μ_n (cm^2/Vs)	1500	1000
Thermal conductivity, K (W/cm K)	1.5	4.9
Saturated electron drift velocity, Vsat($\times 10^7$ cm/s)	1	2

With high breakdown electric field, WBG devices have higher voltage capability, lower losses, and smaller packages. With low specific on-resistance and fast switching speed, WBG devices have lower conduction and switching loss, and because of the high-temperature capability of WBG devices, the cooling requirements during power electronic applications can be reduced. With fast switching speed and low switching loss, high switching frequency can be realized. This increase in switching frequency can lead to better dynamics, and reduced filter and passive component needs in general [7].

The development of power modules over the years has been increasingly important as researchers and industry experts find ways to harness the impressive characteristics of WBG devices. Recently power modules are used in extreme applications in areas like hybrid electric vehicles, aerospace, marine vessels and space exploration, therefore, power converters that utilize the WBG characteristics are necessary. Power electronic modules in these applications are essential because of multiple power generation sources and multiple loads with different ratings.

With increasing demand in power density, there is a tendency for the volume and size of power converters to also increase which could have a negative effect in power electronic operation. In power converter applications, switching at high frequencies can help reduce the size of passive components which leads to a reduction in losses.

The high-density power modules based on the WBG semiconductor devices are operated in areas of rigorous applications such as automotive and traction, renewable energy, utility systems and aerospace. These applications mean that inventive ways need to be developed in the design and packaging of the power module and gate drive circuitry.

The gate driver is the most fundamental control circuitry for a power device. The gate driver circuit is capable of taking in a PWM signal from a microcontroller and amplifying the signal to an appropriate range to seamlessly switch the power device while offering protection features like signal isolation and, noise immunity, among others [61]. Since WBG devices like SiC can operate at high frequency and switching speed, it is important for the passive components in the gate drive circuit to be designed in a way that would harness the benefits of the WBG devices. Typically, a reduced parasitic effect is achieved with reduced passive components. This reduction in parasitic can drastically help in reducing power losses and improving the efficiency of the whole power electronic system. Integration of the gate driver into the power module can achieve similar effects for the power electronic system as it results in reduced parasitic effect, faster switching speeds and smaller system size. The proximity of the gate driver to the power module is of crucial importance as a close proximity of the gate driver ICs to the power devices would provide the lowest gate loop inductance and maximize the switching performance of the power devices [9].

2.2 Current State of Integration

There has been an immense development in the existing hardware in power electronics. With the increasing demand in energy conservation, renewable sources of energy and environmental pollution control, power electronics would continue to have breakthroughs and go through evolutionary changes. One main area these changes have been achieved is in the area of integration of individual electronic component [3]. Increased levels of integration could solve some of the challenges seen in power electronics like increasing power density and reliability.

The idea of integrating a power device with its dedicated driver and protection circuitry was first introduced in the late 1980's by Mitsubishi Electric based on a new invention [10]. The

integration was done on the Insulated Gate Bipolar Transistor (IGBT) module which displayed some inherent parasitic and performance limitations at the time. The resulting integrated IGBT module was named Intelligent Power Module or IPM [11]. SiC module integration has shown tremendous progress since then as there have been vast research and development into creating higher level of functional and structural integration trimmed for the new characteristics power device possesses [27], [28], [29].

(a) (b)

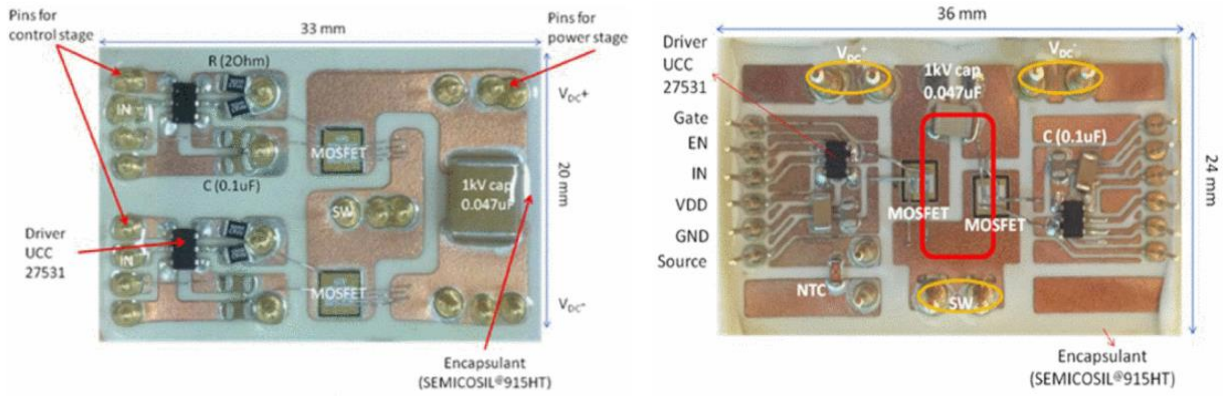


Fig. 2.1: Conventional gate driver integrated power module. (a) Gen-I and (b) Gen-II Integrated SiC Module [30].

2.2 Design of SiC Power Module with Gate Driver Integration

2.2.1 General Layout Design of a SiC Power Module

Proper design of the layout and packaging of a power module is specifically important for SiC devices. There are two major layout considerations when designing packaging layouts for a power module. The first consideration involves electrical parasitic optimization while the second involves thermal optimization of the power module. Depending on the specific application of the power module the layout is methodically designed to address either consideration or both.

Optimization of the power loop parasitic and the thermal stress in a power electronic module can be challenging especially in a multichip or multi-die module. From an electrical layout perspective, switching loss and dynamic behavior are negatively impacted by parasitic parameters within a power module [58]. From a thermal perspective, the heat distribution unbalance of the junction temperature is amplified by the higher switching frequency in SiC MOSFETS [59]. Current research focus is not only in the invention of new power module layouts but also in the development of innovative methods for optimizing existing layouts [60]. Seeing that increasing the size of the direct bonded copper (DBC) substrate can help relieve thermal stress, this could on the other hand result in an increased power loop inductance [15]. So, analyzing the tradeoffs between these two important considerations is vital for achieving proper optimization of the power module layout.

The conventional layout of the power module typically consists of a MOSFET and an anti-paralleled diode. This is referred to as a phase leg configuration as the MOSFET and diode form one switch. A sample half bridge configured power module like the one shown in figure 2.2 has 6 parallel SiC MOSFETS and 12 antiparallel SiC Schottky diodes. In the simplified half-bridge circuit diagram, there are body diodes within the SiC MOSFET and antiparallel diodes. The antiparallel diode is a SiC Schottky diode which serves as a freewheeling diode essentially bypassing the body diode of the SiC MOSFET [31].

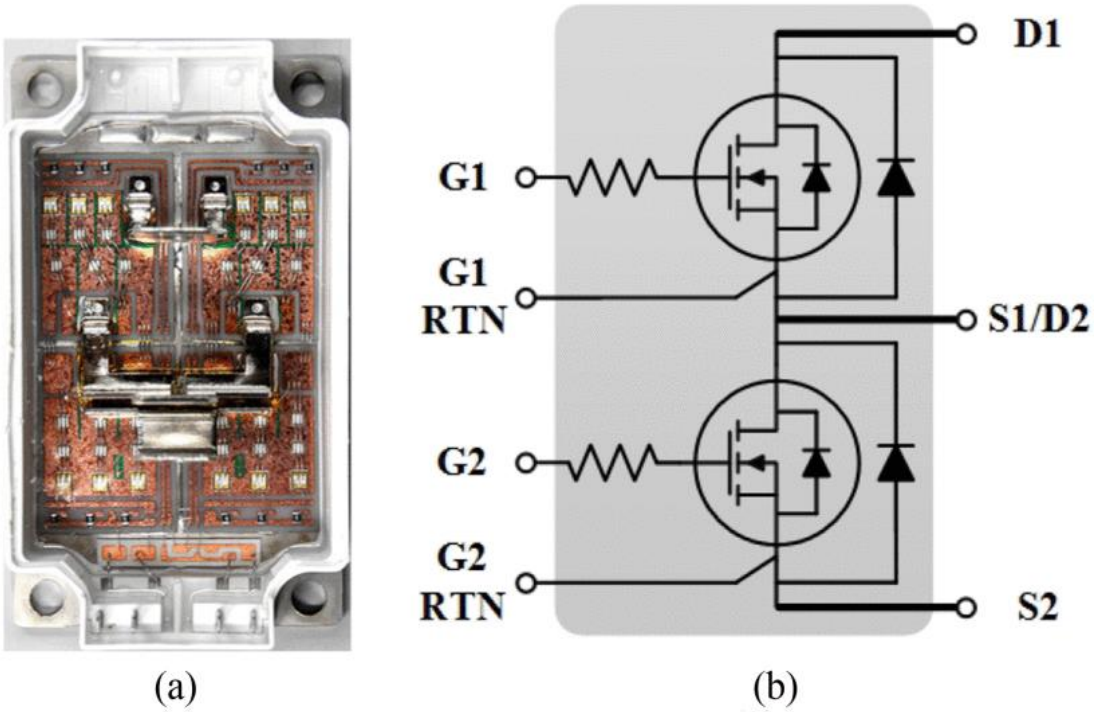


Fig. 2.2: Sample SiC half-bridge module CAS120M12BM2. (a) Open package and (b) circuit diagram [31].

2.2.2 Parasitic Extraction of a SiC Power Module using ANSYS Q3D

The simulation software used for the parasitic extraction of the SiC power module is known as ANSYS Q3D. This software is a finite element analysis (FEA) tool that is used to predict how a design will behave under certain operational conditions. An overview on how to extract the parasitic inductance of the wire bonds and terminals in a power module involves, first, drawing the module in ANSYS Q3D as presented in figure 1.3. Second, designing the parameters of the module so that adjustments can be made on it if needed. Third, setting up the simulation in ANSYS Q3D. Finally, executing the parasitic inductance extraction, and then reviewing the result of the extraction. The structure of the power module, as illustrated in figure 1.3, was designed with a half-bridge topology. Three nets were created for parasitic inductance extraction. The first net represents the drain-to-source path, the second net is the gate path, while

the third net is the DC+ to DC- terminal path. The result of the analyzed inductance extraction of the power module design in figure 1.3 is presented in the simulated graphs from figure 2.3 to figure 2.7. These figures show how changing the dimensions of interconnecting materials, like the terminal and bond wire, affects the parasitic inductance extracted from the power module. The material and dimensions of the terminal and bond wire must be well understood to optimize the design of these interconnections. The material used for the terminal is copper and the material used for the bond wire is aluminum. The design geometry of the terminal in the extraction process involves increasing the height of the terminal from 1mm to 8mm with a constant length of 5mm. The width and length dimension of the terminal is simulated from 1mm x 1mm to 8mm x 8mm for the area of terminal connection graph. In the bond wire parasitic extraction, the parasitic inductance is found for 1 to 8 bond wire interconnections with a fixed length of 0.25mm and a fixed diameter of 0.15mm. The length of the bond wire is simulated from 2.5mm to 5mm. The diameter of the bond wire simulation is also varied from 1mil to 15mil for the inductance extraction.

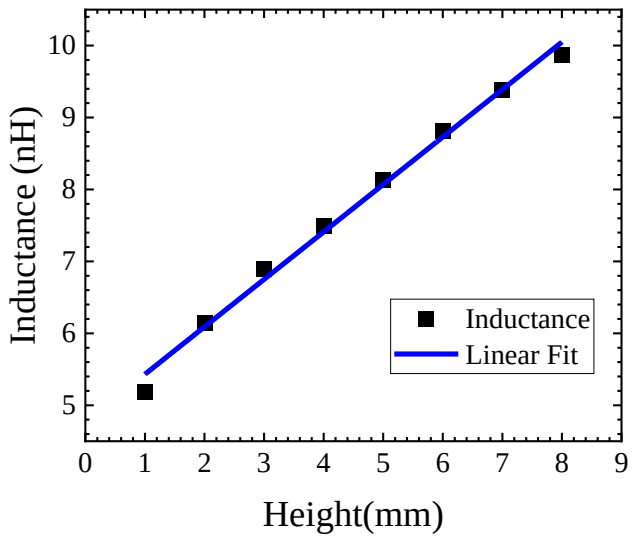


Fig. 2.3: The terminal height dimension is varied from 1mm to 8 mm.

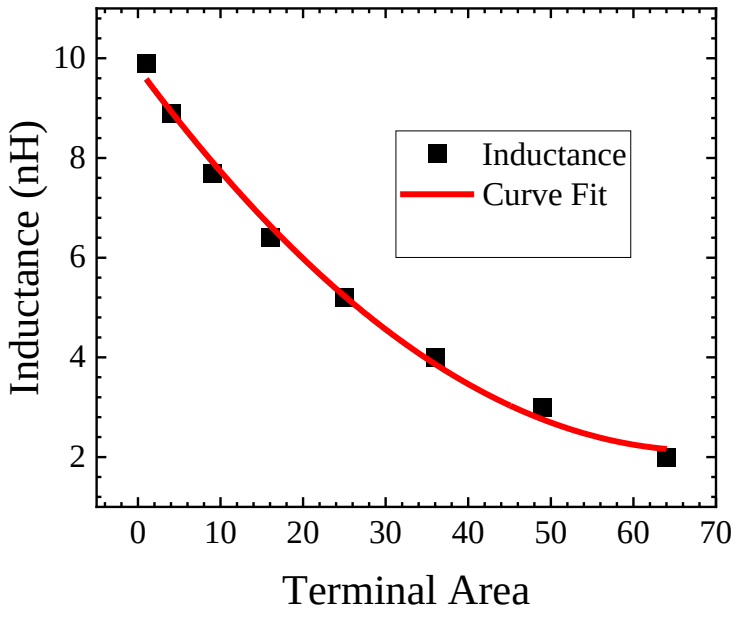


Fig. 2.4: The terminal area comprising the length and width is simulated from 1 mm^2 to 64 mm^2.

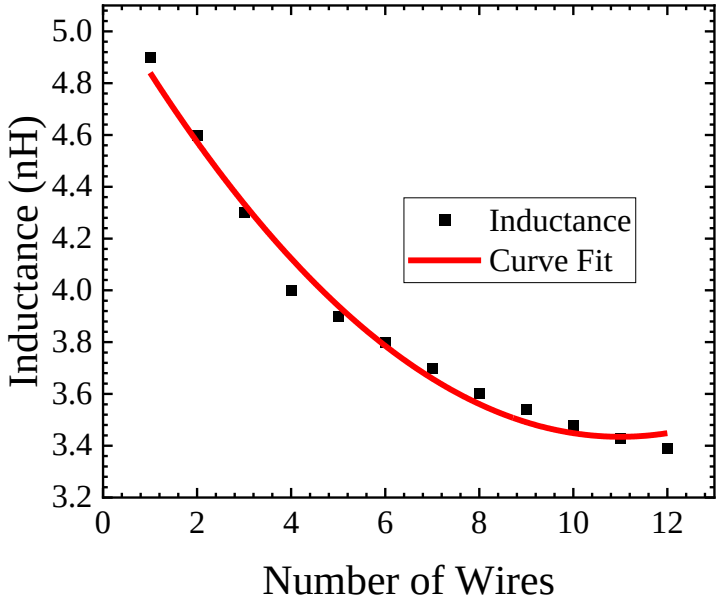


Fig. 2.5: The number of bond wires is varied from 1 to 12 in the power module.

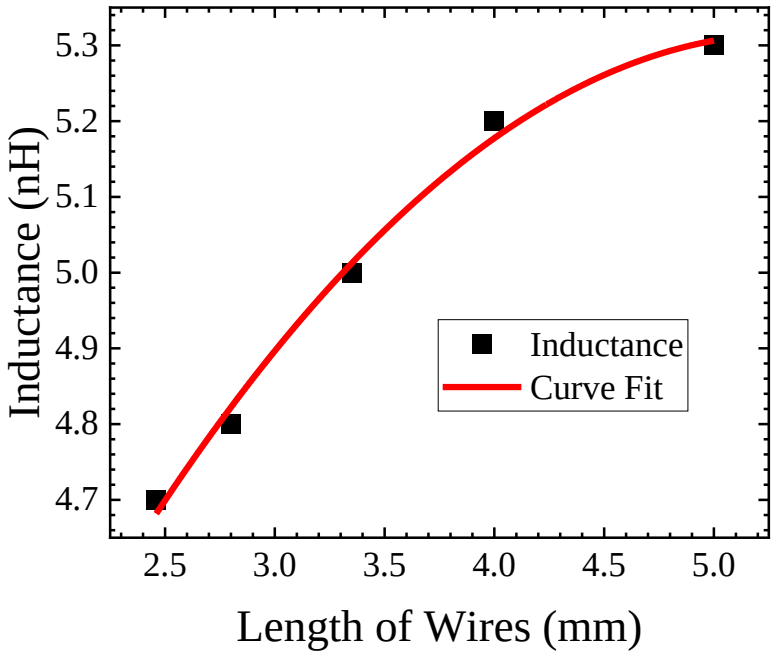


Fig. 2.6: The length of the bond wire is simulated from 2.5 mm to 5 mm with a fixed diameter of 0.15 mm.

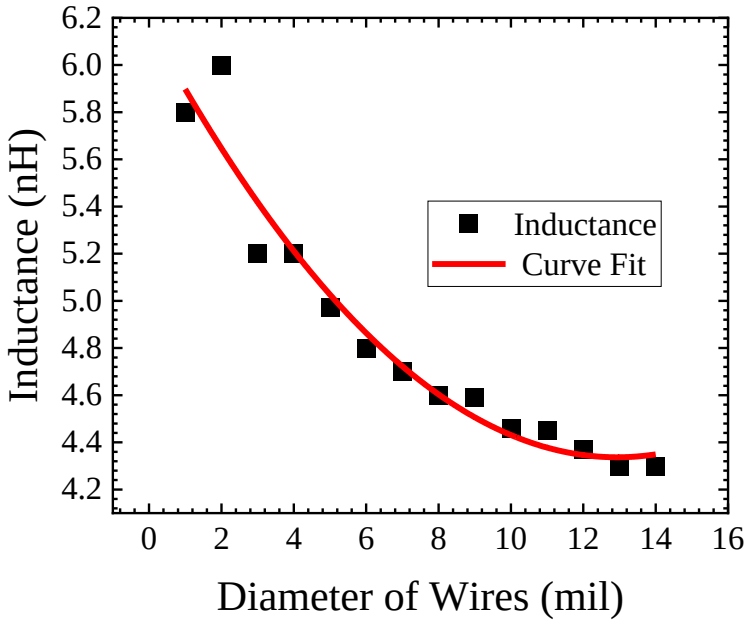


Fig. 2.7: The diameter of the bond wire is varied from 1 to 16 mil with a constant length of 9.8 mil.

The results found from the parasitic inductance extraction made in ANSYS Q3D is provided and graphed using a software called Origin for better visual analysis. Figure 2.3 describes the relationship between the height of the terminal and the inductance values that result from different height measurements from 1 mm to 8 mm. The linear relationship portrays an expected result as the height of the terminal increases with parasitic inductance. This is expected since the current path for the terminal is longer indicating more storage of energy as current flows through the longer terminal path. In figure 2.4, the relationship between the terminal area and the parasitic inductance is non-linear. Since a wider current path reduces the parasitic inductance value, the multiplication of the length by the width of the terminal results in the terminal area that is inversely proportional with the parasitic inductance. For the number of bond wires, there is a non-linear relationship with the parasitic inductance values as given in figure 2.5. Twelve bond wires are used to make this interconnection between the direct bonded copper (DBC) and the die. The length and the width of all the twelve bond wires are 0.25 mm and 0.15 mm respectively. The graph in figure 2.5 further illustrates that the parasitic inductance decreases rapidly from one to four bond wires. The parasitic inductance then reduces gradually until it begins to flatten out at nine bond wires where additional increase in the number of bond wires does not produce any significant effect on the parasitic inductance. The length of the bond wire is another parameter to consider as in this case, in figure 2.6, a non-linear relationship exists with the parasitic inductance. Maintaining the same parameters for the width and number of bond wires, the length of the bond wire was extracted from 2.5mm to 5mm. The parasitic inductance for the bond wire length extraction ranges from 4.7nH to 5.3nH. The diameter of the bond wire is also a factor that must be taken into consideration. Figure 2.7 indicates that the relationship between the parasitic inductance values and the diameter of the bond wire is non-

linear. Generally, the thickness of the bond wire is highly dependent on the amount of current that is supposed to flow through it. For instance, the drain-source bond wire tends to have a higher diameter than the gate bond wire interconnection because there is more current flow from the drain to source path connection to the DBC compared to the current flow in the gate bond wire connection to the DBC. The bond wire thickness (diameter) was extracted from 1mil to 15mil. The graph in figure 2.7 displays a sharp decrease in the inductance from 1mil to 5mil. The parasitic inductance reaches a critical value in the diameter at 11mil where any further increase in the bond wire diameter does not produce any significant change in the parasitic inductance. There is no specific limit to the diameter of the bond wire. It is mostly application dependent. Also, it is obvious from the graph that the relationship between the bond wire diameter and the parasitic inductance is non-linear.

Optimizing the terminal and bond wire design ensure that there are less parasitic effects like voltage overshoot during power module operation especially at high frequency and high-power operation. The reasoning behind optimizing the terminal and bond wire design parameters is because of the quest for an increase in switching frequency so that power density can be increased leading to a miniaturization of power electronic modules in power electronic applications. The DC+ and the DC- terminals are simulated in a power module to give the power loop inductance. This power loop inductance parameter can be considered to contribute about 75 percent of the total loop inductance that a power module is exposed to during power module operation [62]. It is crucial to understand that reduction of the power loop inductance is not just about optimization of the DC+ and DC- terminals. The power loop inductance also includes the DBC of the DC+, AC and DC- traces, and the bond wire that is also discussed in this chapter. As noted from the results in figures 2.3 - 2.7 above, the optimization of the terminals of the

power module is based on the concept of having a small current loop area that provides a short and wide current path. This approach in terminal optimization is also echoed in [32]. To better understand the results determined from the simulation graphs presented in this chapter, comparisons were made with the commercial power module presented in [62]. Notice that in reference [62], the extracted parasitic inductance value of the DC+ to DC- terminal generated from the commercial 1.2 kV SiC power module is 14.86nH. While that generated from the proposed module presented in the same paper is 2.09nH with both simulations done at a frequency of 10MHz. This reduction in inductance from the commercial module to the proposed module represents a 76% reduction which is huge in reducing the over voltage effects during module operation at 10MHz switching frequency. Also note that power module operation at a higher frequency would exhibit higher voltage oscillation across the drain to source path which could in effect damage the dies. Furthermore, the same terminal and bond wire design geometry from [32] is used in this paper for a more appropriate comparison. There are other methods that can be used to extract parasitic inductance in a power module in addition to the ANSYS Q3D simulation. In [34], an FEM (finite element model) is used and compared with the FEA method for validation. This FEM method is a frequency-domain impedance measurement method based on the two-port network technique. This power loop extraction method does not require detailed knowledge of the material properties of the terminals and bond wires to complete the extraction. A similar approach for the parasitic extraction process in this paper is discussed in [35]. Although the power module layout in [35] is different from what is presented in this chapter, the comparison of the Q3D method and the FEM method is analyzed for a wire bondless layout leading to similar results in the power loop parasitic inductance extraction.

2.3 Gate Driver Design Fundamentals

2.3.1 Introduction to Gate Drive in SiC Power Modules

The gate drive circuit is an important component of every power electronic system as it is capable of controlling power devices under static, dynamic and fault conditions in an efficient and reliable way. In order to understand the gate drive feature and its need in driving a SiC power module, it is crucial to explain the switching operation of a power MOSFET, specifically of its gate terminal. The MOSFET is a three-terminal device, having the gate, source and drain as the terminals. The gate terminal controls the conduction between the drain and source terminals.

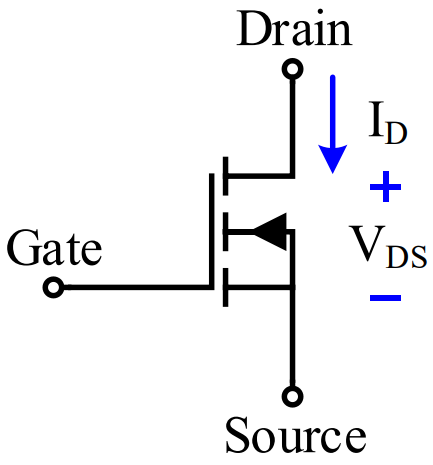


Fig. 2.8: MOSFET switching structure [12].

As seen in the MOSFET switching structure shown in figure 2.8, the gate is electrically isolated from the conductive path from the drain to the source which means the gate input resistance is very high. The gate forms a resemblance to MOS capacitor that has to be charged and discharged every time the MOSFET switches on and off. In power MOSFETS, this gate capacitance could range from hundreds of picofarads to tens of nano-farads [13]. The gate

threshold voltage is the voltage at which, upon charging the gate capacitance, the transistor starts to conduct. The figure below shows the relationship between gate charge and gate to source voltage.

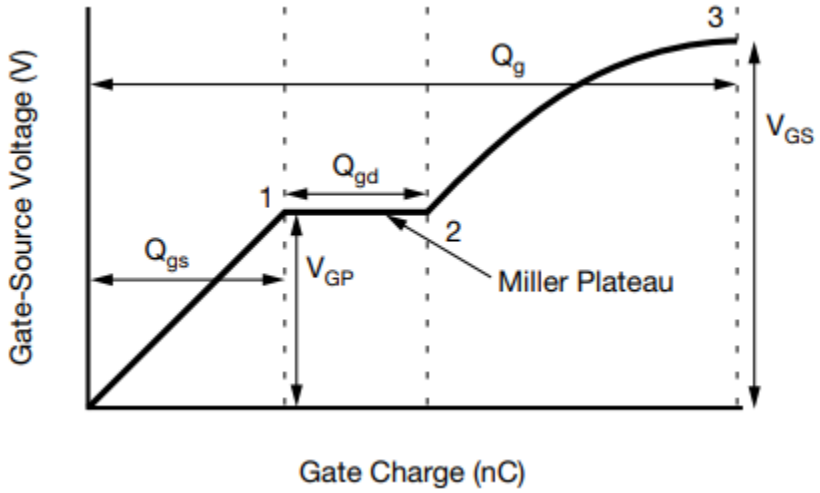


Fig. 2.9: Sketch showing breakdown of gate charge [13].

To operate the power MOSFET, a voltage signal is usually applied to the gate of the power device that charges the gate capacitor and as a result, turns the power device on. The device supplying this PWM signal typically emanates from a DSP, MCU or FPGA. The maximum voltage range of the PWM signal is usually 3.3-5 V with limited current generation. This is an issue when switching power devices of SiC semiconductor as the gate voltage requirement is much higher than the 5V range. For SiC MOSFETS, a positive gate drive voltage of around 20V is typically recommended to effectively drive the SiC MOSFET and to obtain sufficiently low ON resistance. Hence, there is a need for a gate driver to supply this positive voltage range to the gate of the MOSFET to effectively drive the SiC device. Also, a negative gate to source voltage is needed for active turn-off. The range of the negative bias voltage is -5V

and it is required to prevent any false or undesired turn on of the SiC MOSFET ensuring a quick and safe turn-off transient.

2.3.2 Need for Isolation in a Gate Driver for a SiC Power Module

The goal of isolation in a gate driver circuit is to provide an electrical separation between the circuit's signal controller stage and the power stage connected to the gate of the power device. In other words, this provides a galvanic isolation between the world of control and the world of power. These two worlds can be described as two stages in a gate driver circuit. Galvanic isolation of these two stages of the gate driver circuit ensures that there is no current flow in the functional sections between the two stages of the electrical system. This separation is very important, and it is often mandated in some industries. Safety of the end user of a power electronic system from high voltage surges and even protection of the very expensive equipment within the power electronic system are some of the reasons why it is critical to use galvanic isolation. Now, there are two forms of isolation needed in a gate driver circuit. Signal flow isolation and power flow isolation.

The signal isolation provides galvanic separation between the microcontroller ground and gate driver ground while safely transmitting control and fault signals from the input to the output of the gate driver. The voltage level of the signal (or logic stage) of the gate drive circuit is low while the voltage level of the gate drive (or power stage) of the gate drive circuit is high. For this reason, there is need for galvanic isolation within the signal flow of the gate drive circuit. The figure below illustrates this concept in a gate drive circuit.

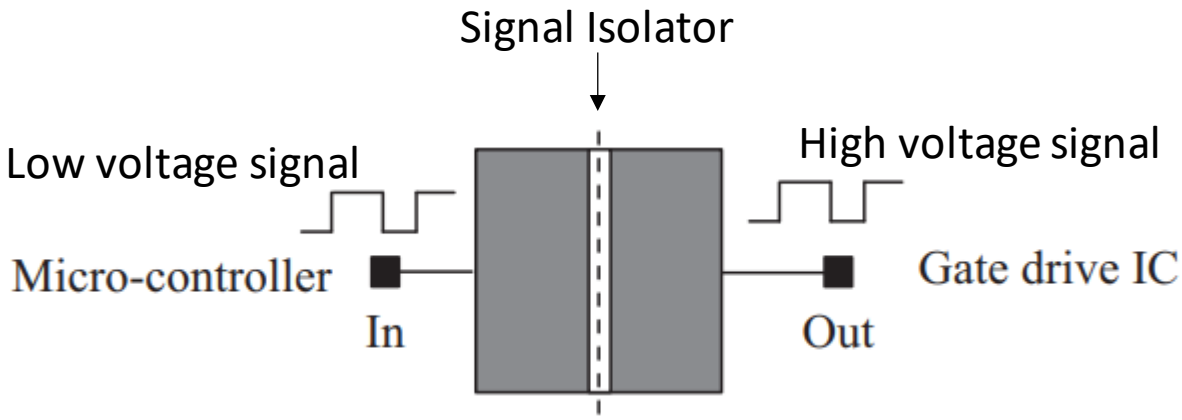


Fig. 2.10: Illustrating Signal isolation in a gate drive circuit [7].

Some of the technologies used for galvanic isolation are optically isolated and digitally isolated devices. Optical isolation involves a photodiode and a light emitting diode (LED) as major components. Meanwhile digital isolators provide isolation in the form of insulation with on-chip capacitors and off-chip capacitors, as well as with on-chip inductors. Galvanic isolation in this stage is typically integrated into the gate driver using different methods. These methods are based on an optocoupler, transformer, or a capacitor. It is important to note that each of these methods has its advantages and disadvantages, and the choice of any of these methods is application dependent. The next chapter further explores optical isolation as it contrasts other isolation methods. The main components involved in optical isolation and its application in a gate drive circuit is also examined.

Isolation with the aid of an optical fiber is a more modern isolation technique so it is not widely used. Even though it has the best protective isolation method in terms of isolation voltage capability and performance reliability, it is quite expensive to implement [36].

In the power flow stage of a gate drive circuit, there is also a need for galvanic isolation. Even though optical isolation can act as an insulator for the control signal side, there is a need for

isolation on the power side. Common methods used for galvanic isolation include high frequency DC-DC converters, isolated transformers, and bootstrap supplies.

2.3.2 Gate Driver Circuit Design and Simulation

This section presents various gate drive circuit designs and gate driver requirements to be able to drive a SiC MOSFET. Formulas and parameters are also given in calculating the gate current and power required to drive the SiC MOSFET into conduction.

Figure 2.11 shows a general schematic design of a gate driver. In this architecture, the transformer is acting as the power stage isolation while the optical fiber is acting as the signal control stage isolation.

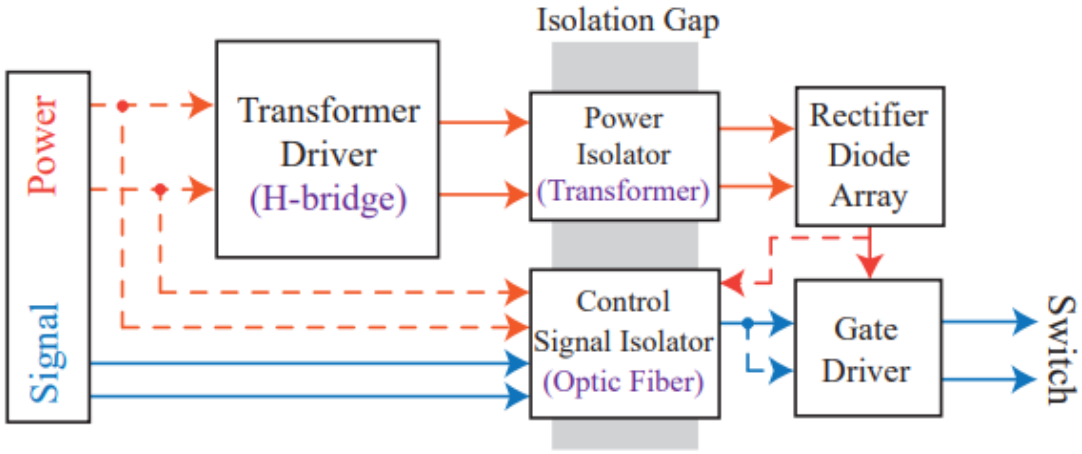


Fig. 2.11: General schematic of the architecture of a gate driver circuit [37].

It is difficult to develop the design of the power transmission stage of the gate driver due to the competing needs of high isolation, low coupling capacitance, and an efficient gate driver footprint. To accomplish this, a careful balance must be reached to fulfill all the requirements at the same time. So, the architecture for an optimized gate driver circuit is more complicated and detailed than this presented in the figure above.

Some of the gate driver circuit consideration for designing an optimized gate driver circuit include:

- The supply voltage range. Referencing the gate to source voltage value of the SiC MOSFET would help determine what the positive and negative range should be.
- The need for a negative drive voltage has previously been discussed. This is an important consideration to ensure quick and safe turn off transient and lower turn off switching loss.
- The Common Mode Transient Immunity (CMTI) is a measure of how well two isolated circuits can withstand a rapid change in the common mode voltage. This typically happens with faster switching speeds of SiC MOSFETs when voltage passes from the control side to the power side, and it can result in ringing and damage to the MOSFET. A 150 V/ns rate of rise/fall is usually recommended for preventing this kind of electrical error.
- Driving capabilities of the gate driver.

  The formula for determining the required gate drive current per channel is: (Ig) = $\frac{Q_G}{t_{on}}$; *where* Q_G *is the total gate charge and* t_{on} *is the desired turn on time of the power device.*
- Propagation delay time is the time it takes an input edge to propagate to the output. Because shoot through could happen during device operation hence, inserting a proper dead time prevents any damage to the transistor. Better delay matching of the device and gate drive means a lower dead time is required which in turn results in a smoother operation of the power switch.
- An external gate resistor is also an important consideration. The main reason for the external gate resistor is to limit the oscillations that might occur as a result of parasitics in

the gate loop. Reference [38] details how to find the appropriate gate resistor for an optimum gate driver design.

- Short circuit protection is important to ensure the surge current generated during short circuit conditions, especially in a SiC device is quickly detected and countered to prevent any false triggering of the devices or destruction of the system. Reference [39] proffers different protection methods and offers guidelines for a rugged short circuit design.

2.4 Challenges in Power Module Integration of a Gate Driver

2.4.1 From the Power Module Side

Developing and designing a gate driver integrated SiC power module offers significant advantages. These advantages manifest in the form of increased power density, reduced power loss, and overall improved efficiency of power electronic systems. This enhancement directly impacts energy consumption during the switching performance of the power device. However, this close integration offers major concerns from the gate driver and power module perspective during system integration.

Basically, any component like the gate driver, decoupling capacitors, temperature sensors, cooling sensors, protection circuits, and cooling equipment integrated into a power module reduces the dead space that could have been created between the power module and the components in a system-level design [40]. The figure below shows possible power module structures that could serve the function of a highly integrated power module.

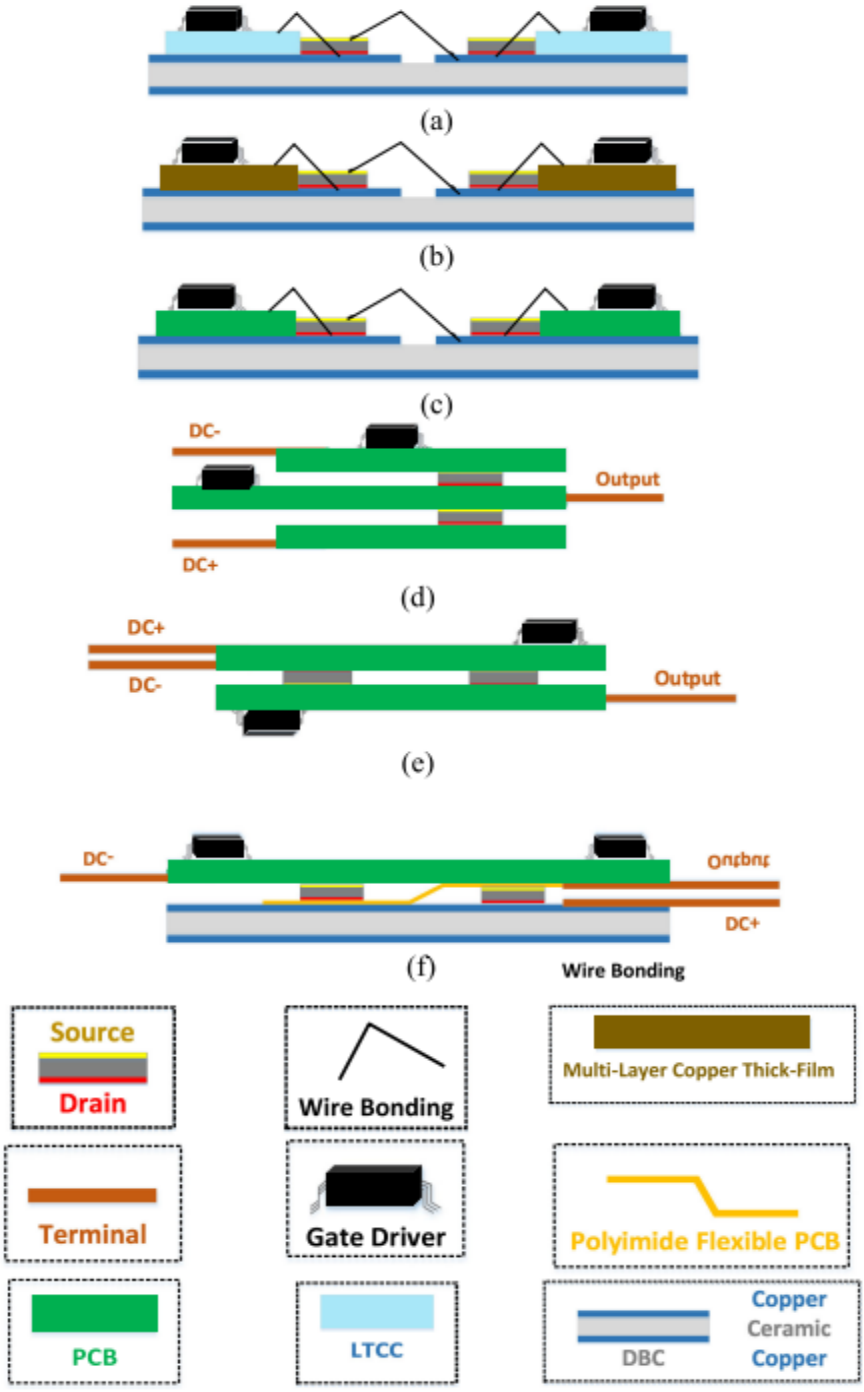


Fig. 2.12: Various architectures for power module integration [41].

Reference [41] discusses the challenges that could be encountered, and the benefits associated with various high levels of integration. Figure 2.12 reproduced from [41] shows several of these options. Figure 2.12 (a) shows the power module structure with a low temperature co-fired

ceramic (LTCC) gate driver integrated with a DBC substrate. The paper further reveals that the cooling mechanism in this type of integration may be one-sided, and soldering on the LTCC substrate would be difficult. The challenges in (b) have to do with the cost of the integration. (c) has the same challenges as (a) together with issues involving coefficient of thermal expansion (CTE) mismatch between the DBC and PCB. Additionally, (c) also presents the added issue of an increase in the overall size of the power module. The challenge (d) has relates to the high cost of fabrication and the difficulty in attaching components to the DBC. The architecture of (e) poses challenges related to the high fabrication cost and the limitation of the DC+ and DC- thickness to 0.8 mm. Finally, the challenges for the structure design of (f) entails CTE mismatch and a more complicated fabrication process for the structure design. In chapter 3, a more in-depth evaluation is presented for the integration architecture (a), which employs an LTCC integrated gate driver with the DBC power substrate.

Thermal management is another issue the integrated power module faces. Minimizing the gate loop by placing the gate driver as close as possible to the power device could lead to thermal coupling between the driver and the power device. In the case of a SiC MOSFET whose peak junction temperature is around 150^{o}C, the SiC MOSFET during operation could reach temperatures above 100^{o}C as strong thermal coupling could cause the self-heating of the MOSFET and the device temperature to rise [42]. This could essentially destroy both the power device and the packaging materials, especially if they are not suitable for these temperature levels. Consequently, the placement of the gate driver integrated circuit (IC) must be planned in such a way that thermal coupling with the SiC MOSFET is reduced to a minimum.

2.4.2 From the Gate Driver Side

As previously highlighted, the dead space between the gate driver and the power module in a conventional power electronic system is greatly reduced if the gate driver is integrated into

the power module system. This has many benefits which have previously been discussed but it also has a major challenge that has to do with the gate drive interference. Due to the close proximity of the gate driver IC to the power devices, which is essential to reduce parasitic inductance, the interaction between the gate driving loop and the power loop will be much more pronounced. Consequently, interference may occur in the driver ICs, with the signal input being particularly vulnerable and requiring heightened protection or isolation measures. Reference [42] gives more detailed analysis of this issue. Additionally, reference [43] provides experimental verification of this issue and its impact on the overall system. In analyzing the gate signal interference, a double pulse test setup is made, with the specifications of the integrated power module shown in table 2.2.

Table 2.2: Specification of the integrated power module [43].

Parameters	Value
Rated Voltage/Current	1200V/20A
SiC MOSFET	CPM2-1200-0080B
Bypassing Capacitors (on board)	1200V/15nF(×2)
Signal Isolation	Si8233
Gate Driver IC	UCC27531

An equivalent circuit of the test setup is also shown together with the waveform of the double pulse test result in figure 2.13.

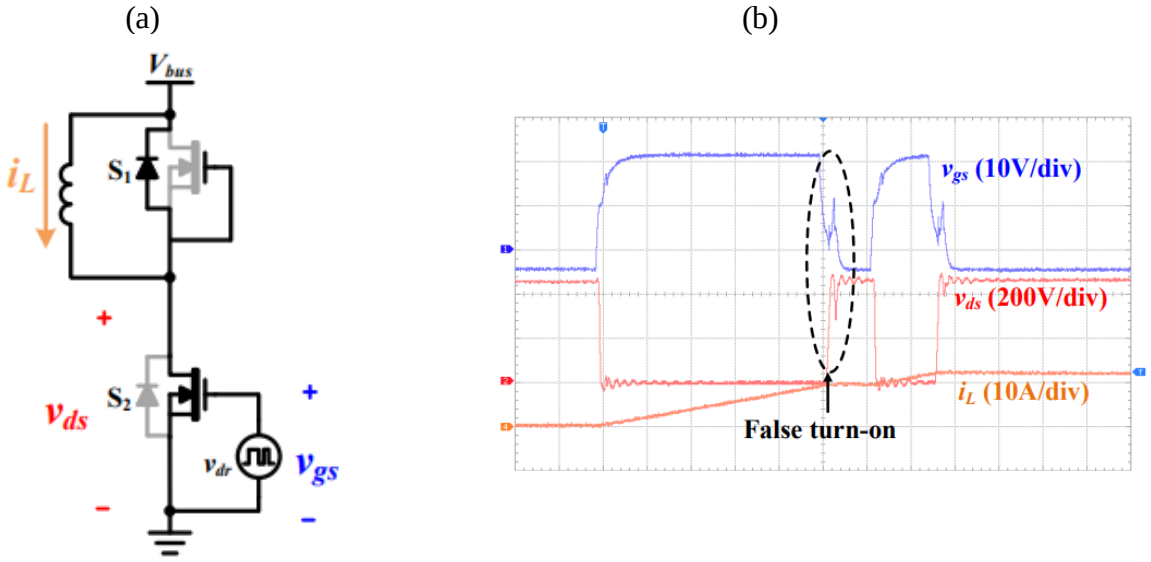


Fig. 2.13: Analysis of the gate signal interference: (a) Equivalent double pulse test (b) Waveforms of the double pulse test [43].

As shown in the waveform, as the gate to source voltage (blue trace) decreases, interference can be seen making the drain to source voltage (red trace) decrease unintentionally resulting in a false turn on of the power device. This interference impairs the dependability of the module and should be removed or mitigated as much as possible.

Chapter 3: Optocoupler Integration of a Gate Driver in a SiC Power Module

3.1 Integrated SiC Power Module Design- Optimized Layout and Parasitic Extraction

Implementing an integrated SiC power module design entails a number of considerations which have been previously discussed and they can be grouped into electrical and thermal considerations. Generally, electrical consideration relates to reducing the parasitic inductance of the overall integrated power module design. Parasitic mitigation in an integrated module design might entail the use of decoupling capacitors, high quality gate drive signals, and minimizing electromagnetic interference emissions [41]. Thermal consideration majorly relates to avoiding incidents of thermal coupling and its effects. Since passive components and gate drivers are closely attached to the devices, ensuring effective heat spreading and cooling, especially in hot spot areas like power devices, alleviates issues that could result in damaging the power module. This is where the careful selection of the attachment materials, proper interconnection methods, and the integration of passive components is required in order to address these challenges [44].

An optimized DBC layout was designed for the purpose of integration as shown in figure 3.1.

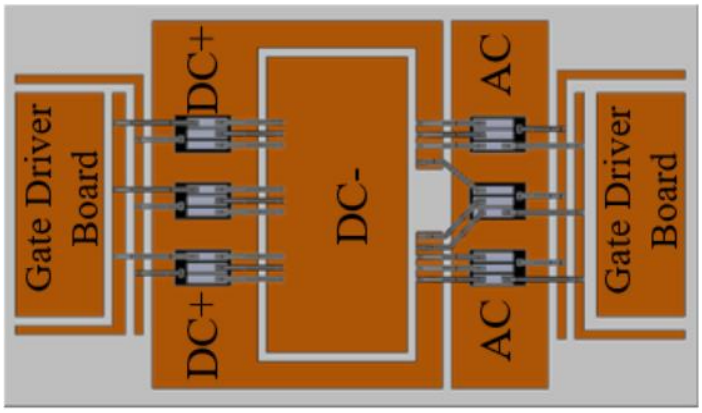
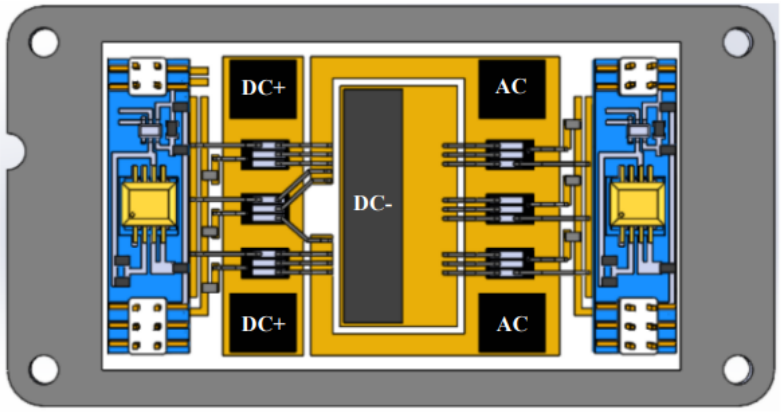


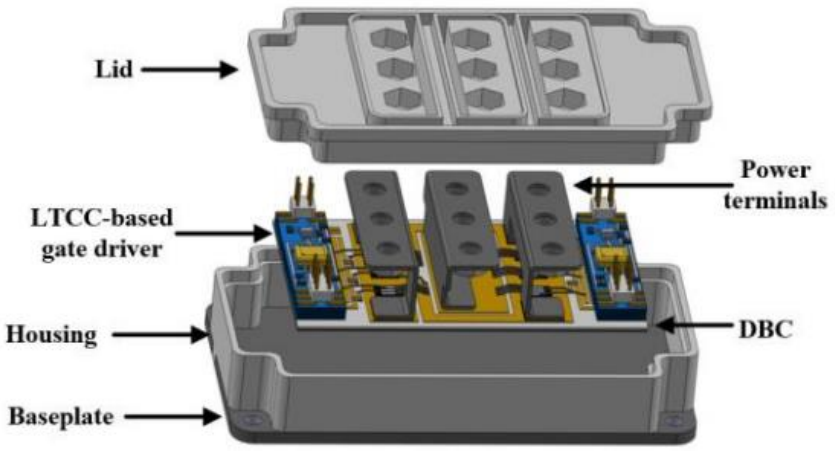
Fig. 3.1: Optimized DBC layout design.

The maximum dimension of the DBC substrate area is 80x45 mm. The maximum area for the gate driver board on the DBC substrate is 40x11 mm. With the aid of ANSYS Q3D, parasitic extraction was done to determine the power loop inductance of the layout which came out to be 7.5 nH. The optimization technique used in reducing the parasitic inductance was based on an improved design of the P-cell, N-cell phase leg module in [45]. A 1.2 kV, 149 A SiC MOSFET from CREE (CPM3-1200-0013A) was attached to the top of the DBC. The current balance and heat spread across the surface of the DBC is improved with a symmetrical layout as illustrated in figure 3.1. As shown in figure 3.2(a), two LTCC-based gate drivers are also attached to the top of the DBC. The LTCC-based gate driver has output pads located on the bottom layer. This is done in order to establish connections with the power devices through copper traces on the DBC and with the aid of aluminum bond wires.

(a)



(b)



(c)

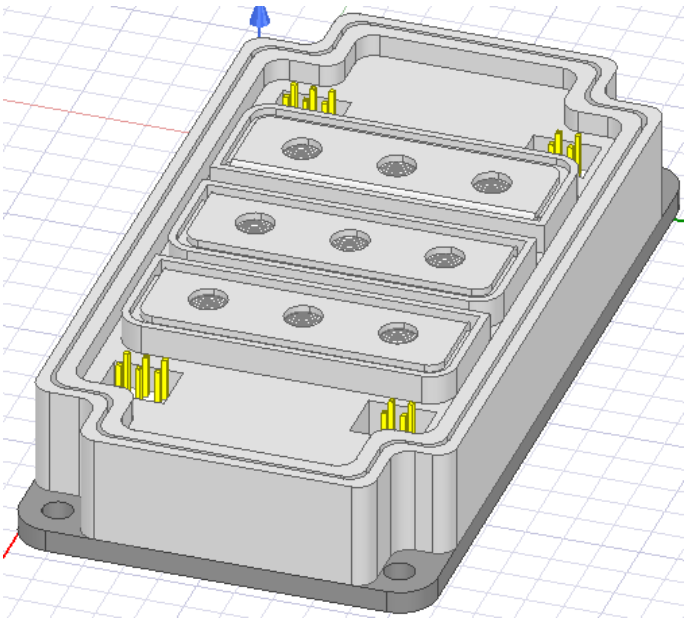


Fig. 3.2: (a) Layout, (b) 3D model and (c) 3D housing case of the gate driver integrated SiC power module.

As shown in figure 3.2(b), the power terminals of the power module were positioned strategically to help reduce the power loop parasitic inductance. Also, the close proximity between the SiC MOSFET die and the gate driver ensures that the parasitic inductance is effectively minimized.

Simulation and parasitic extraction were done on the designed power module shown in figure 3.2 using ANSYS Q3D. The results are shown in figure 3.3. In the power loop simulation,

the DC+ terminal served as the source, while the DC- terminal served as the sink. In the gate loop simulation, the source was set as the output pad of the LTCC-based gate driver, and the sink was set as the gate pad of the power device. Note that 3 extractions were done for the gate loop inductance representing the three parallel gate pads (set as the sink) of the power devices on both the high side and the low side. The average value of the three gate loop inductances was plotted for both sides. Figure 3.3 further illustrates that the power loop inductance at 1MHz is approximately 7nH, and the gate loop inductance at 1MHz is approximately 9nH and 10nH for both high side and low side respectively. These inductance values are comparable to other commercially available SiC power modules [30], [46], [47].

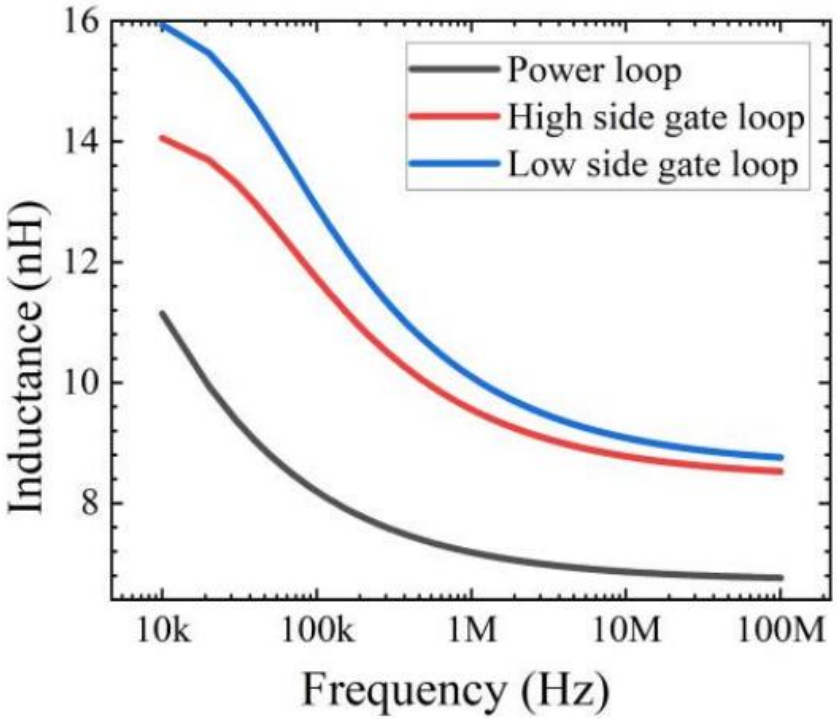


Fig. 3.3: Graph showing the parasitic inductance versus frequency.

3.2 Overview of Optocoupler's Basic Structure and Isolation Applications

This thesis has briefly discussed some electrical signal isolation methods in a system. As previously highlighted, transformers, optical isolators and capacitors are commonly used to separate signals from the control side to the power side. During system operation, fault currents may arise from the power side which might destroy low voltage electronics within the system. Therefore, electrical separation ensures there is no direct conduction path between the varying power levels, which then ensures safety of the electronic equipment and the operator. Optical isolation with the use of optocouplers is discussed extensively in this chapter because it offers some unique advantages in comparison to other isolation methods.

Simply put, an optocoupler is a device that combines two diodes: one that emits light when current travels through it, and the other that absorbs light and generates a proportional current [14]. Optical isolators also referred to as optocouplers generally use an LED lighting fixture as the transmitter which sends light waves to a receiver (photo-diode or photo-transistor) which is light sensitive. Optical isolators come in two types. The first type is isolation IC, which provide complete galvanic isolation by emitting and receiving light. They are employed in lower voltage applications like medical and industrial communication. The second type is optical fibers which are preferred in high voltage applications. The isolation ICs type is the focus of this paper. For effective optocoupler integration into a gate driver, it is important that the packaging of the optocoupler is not only compact but also comes in less weight and low cost. These reasons make the isolation ICs preferable as it consumes less power and has high switching frequency due to short switch-on and switch-off times.

The figure below shows the basic structure of the optocoupler as it transmits sensed signal information from the control circuitry to the power circuitry by light. As can be seen in the

figure, there is a separation between the output signal and the input signal. This ensures that there is no electrical coupling between the input and output. In terms of options available for commercial use, there are numerous companies that provide optocouplers in isolation IC packages to enhance gate driver integration. They range from Avago, now a part of Broadcom, to TI and Onsemi. The SiC MOSFET gate drive optocoupler options from these companies have good maximum voltage isolation (8 kV - ~10 kV), and good integration and reliability level.

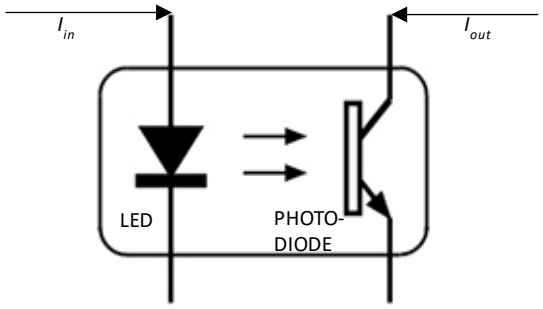


Fig. 3.4: Basic structure of optocoupler.

For this specific application, a low temperature co-fired ceramic (LTCC) packaged optocoupler was developed as an optical signal isolation method. This LTCC optocoupler design is developed for high temperature applications up to 250°C. LTCC technology has been used for over 20 years and has gained significant popularity in the production of sensors and electronics [48]. Its exceptional electrical and mechanical properties render it suitable for applications in high temperatures and harsh environment conditions. Figure 3.5 shows the fabrication process of the LTCC-based optical isolator. High temperature optoelectronic materials and devices were used for the emitter and detector of the optocoupler. This high temperature optocoupler incorporates LEDs as emitters and photodiodes as detectors. The LED material used is Aluminum gallium indium phosphide (AlGaInP) (with LED type known as Red for Display

(RD)) while the photodiode material used is Aluminum gallium arsenide (AlGaAs) (with LED type known as OPC-6900-21(OPC)).

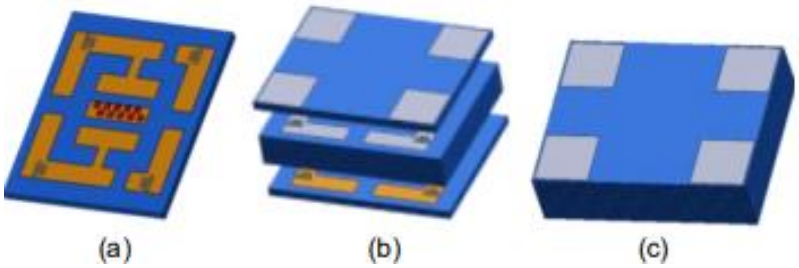


Fig. 3.5: Fabrication flow of LTCC-based optical isolator. (a) Chip carrier with LED attached. (b) Exploded view of LTCC-based optocoupler. (c) 3D representation of LTCC-based optocoupler [36].

References [36] and [49] offer more details into the design and fabrication of LTCC based optical isolation package together with the characterization of the coupling efficiency and output current of various configurations of the emitters and detectors in the optocoupler package.

3.3 Optocoupler Integration in a Gate Drive Circuit

Applications that require signal isolation from electronic devices and components often use optocouplers as current signals are used to drive these devices [15]. Most power devices are voltage controlled like the power MOSFETs and IGBT [16]. Therefore, optocouplers generally do not operate independently. They are operated and employed for specific application circuits. One of these circuits is the TIA (Trans-Impedance Amplifier). The function of the TIA in a gate drive circuit is fundamentally to take an input from an optocoupler (in the form of current pulse signal) and modify it to a useable gate drive signal (in the form of voltage pulse signal) in preparation for its amplification by the gate driver IC [17].

Since optocouplers are preferred to other isolation methods, like the pulse transformer, for their simplicity in design, smaller size, and ease of implementing into an existing design, the figure below shows an optocoupler-TIA integrated gate driver circuit.

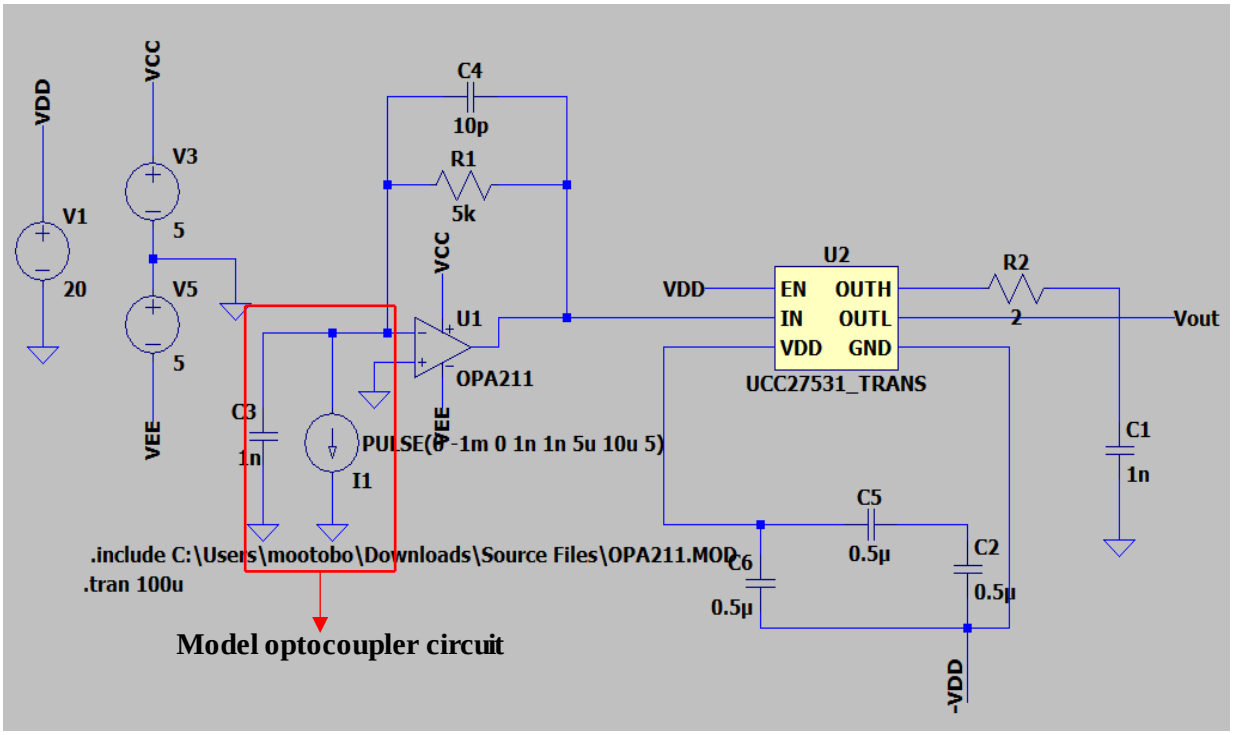


Fig. 3.6: Optocoupler-TIA integrated gate driver circuit.

The optocoupler-TIA stage features an input capacitor, a feedback capacitor and resistor, a current source and an OPA211 operational amplifier from TI. The OPA211 op-amp is ideal for this application considering its size, which helps in gate driver board integration. The optocoupler model utilized the characterization behavior of an optocoupler, where it was replaced with a current source in parallel to a 1nF capacitor. In determining the input current source value, the value of the feedback resistor and the output voltage desired have to be considered. For this particular circuit a pulse voltage signal of -5 - 0V is needed as the output of the optocoupler-TIA circuit. The negative voltage requirement is to ensure there is no incidence of false turn-on of the SiC device as the turn-on threshold of the SiC device is low. In a typical

transimpedance circuit, the value of the output voltage can be determined using its formula as shown in figure 3.7, where I_s is the source current and R_f is the feedback resistor. Since -5V is desired for the output of the Optocoupler-TIA stage in figure 3.4, and with a feedback resistor of 5 $k\Omega$, the result of the source current can be calculated.

$$V_{out} = -I_s \times R_f$$
$$-5\ V = -I_s \times 5\ k\Omega$$
$$\therefore I_s = -1\ mA$$

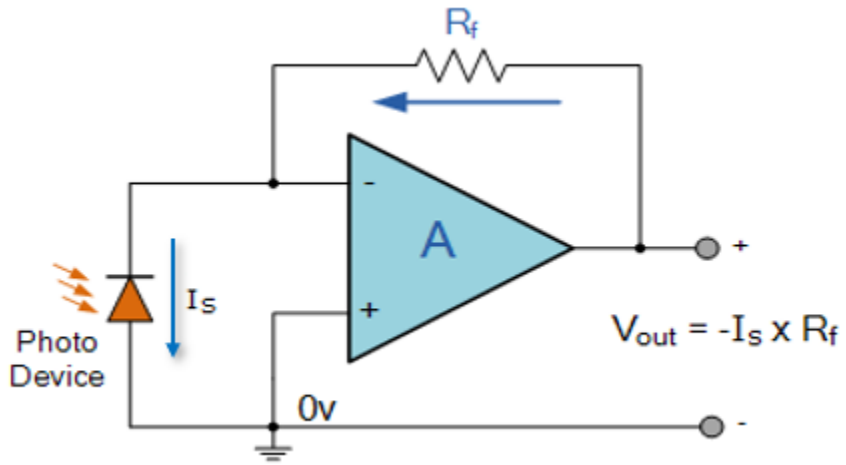


Fig. 3.7: Figure showing a light activated transimpedance circuit.

The operating voltage point at the inverting input and the output level are controlled by the feedback resistor R_f. Also, the 1nF input capacitance is associated with the photodiode of the optocoupler. The feedback capacitor of 10 pF is necessary in reducing the oscillation of the on and off transient time. A range of 1 – 10pF is ideal. Note that increasing the value of the feedback capacitor too high, like in the nano-range, could have a negative effect on the switching waveform as the rise time would be too high.

The second stage features the UCC27531 gate driver from TI. This gate driver integrated circuit (IC) has fast propagation delay, and rise and fall times. It is able to source up to 2.5A and sink 5A (peak) [50]. The size of this IC is small which is ideal for system integration. It also features some protective circuitry to effectively prevent against parasitic miller turn-on events,

which is crucial for SiC device switches. The input requirement of the gate driver IC is compatible with the output of the optocoupler-TIA stage. In the gate driver circuit, the load capacitor of 1nF is chosen based on the input capacitance of the SiC device being driven. The output resistor of 2Ω (R2) represents the external gate resistor corresponding to the gate of the SiC MOSFET device.

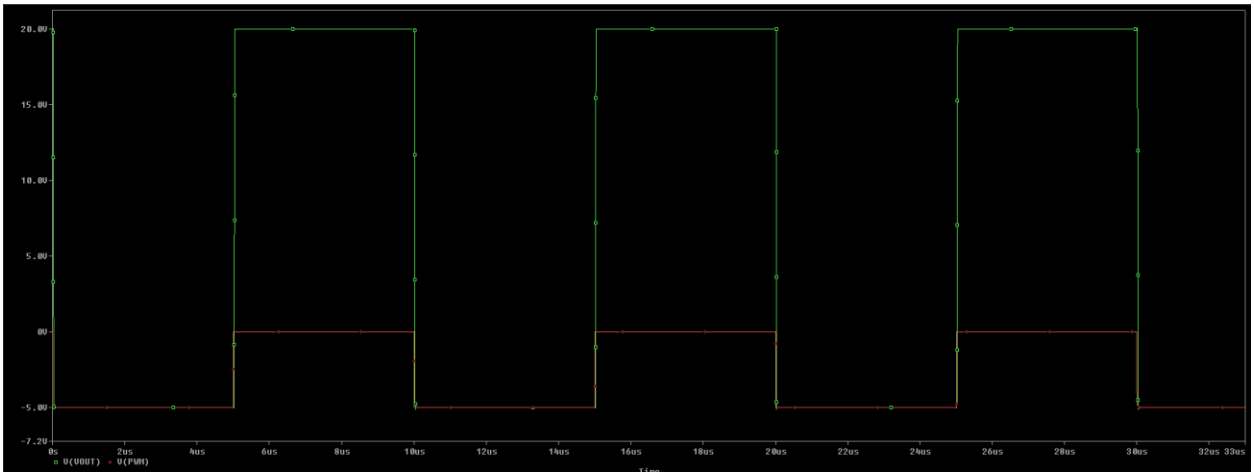


Fig. 3.8: Simulated output graphs of the Optocoupler-TIA integrated gate driver circuit.

The simulated output shows the trace (red) from the optocoupler-TIA stage and the trace (green) from the gate driver stage. The simulation details 3 periods with a rise and fall time of around 1ns each. The output of both stages has limited oscillations which is attributed to the feedback capacitor. For the purpose of driving the CPM3-1200-0013A SiC MOSFET, this is the expected output from both stages.

3.4 Design Parameters for an Optocoupler Gate driver Integration in SiC Power Module

The project involving the integration of an optocoupler-isolated gate driver into a SiC power module was undertaken as a subproject within a larger research group. This particular project was specifically tailored to address high temperature applications, reaching temperatures

of up to 200°C. So, the design parameters for this integrated power module design would be investigated from a high temperature standpoint together with further analyses of the fabrication process and characterization of the integrated SiC power module in the coming chapters.

The optocoupler-isolated gate driver circuit features an LTCC-based high-temperature optocoupler and an LTCC-based gate driver. In their study, P. Lai et al [36] describes the advancement of a high temperature optocoupler based on LTCC technology. This optocoupler demonstrates remarkable signal and minimal leakage current even at temperatures as high as 250°C. The fabrication flow of this LTCC-based high temperature optocoupler is shown in figure 3.5 and a 3-D package of the LTCC-based optocoupler is shown in figure 3.9.

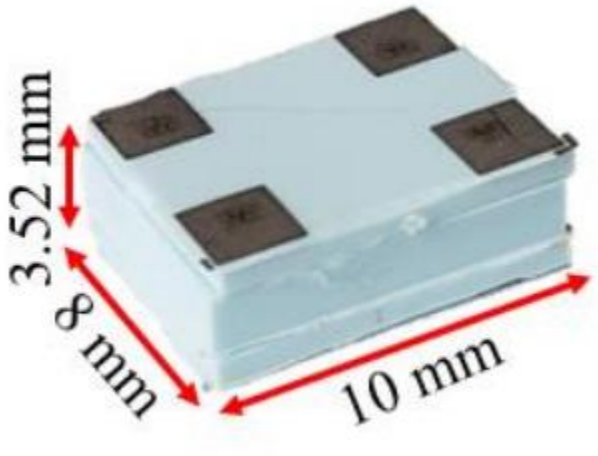


Fig. 3.9: 3-D design package of the LTCC-based optocoupler.

In addition, according to P. Lai et al [36], the current transfer ratio (CTR) studied for this developed LTCC-based optocoupler proved that at 250°C, even though CTR drops dramatically, the output current was still higher than 5μA for some sample optocoupler configurations. This current level is sufficient for the designed gate drive circuit and indicates the LTCC-based optocoupler can operate in high temperature environments.

Ensuring high protection voltage is a major concern for the packaging design of the LTCC-based high-temperature optocoupler, as it is intended to serve as a galvanic isolation device for gate driver circuitry. Reference [49] designed an optocoupler test circuit to test for the isolation voltage of the LTCC-packaged optocoupler and it was seen that the optocoupler can withstand an isolation voltage of around 1000 V which is very good for this gate driver circuit.

The TIA is also adapted for high temperature. The TIA used for the gate driver circuit is the OPA211HT amplifier from TI. According to the datasheet of the OPA211HT amplifier, the maximum junction temperature is 200°C. The propagation delay and maximum operating frequency of the gate driver circuit are determined by the rise and fall time of the TIA. Since these parameters are important, tests were carried out in [36] to ascertain the transient characterization of the OPA211HT amplifier for varying temperatures from 25°C to 250°C. The optocoupler samples tested with the TIA showed rise and fall times to be greater than 100ns which is good for the gate driver design.

For the LTCC-based gate driver in a tightly integrated power module, the proximity of this gate driver to the power device is very important in reducing parasitic elements and improving switching transients. Hence, the temperature capability of the gate driver needs to be close to that of the power device. LTCC substrates are designed specifically for this gate driver circuit because of its high operating temperature of around 400°C. Therefore, in order to ensure proper integration, slots were created on both sides of the LTCC substrate for the close integration of the LTCC-based optocoupler (detector and emitter substrate) and other components like the resistors, high temperature signal pins, the OPA211HT TIA and the UCC27531 IC are attached to the top layer of the LTCC substrate. The figure below gives an

illustration of the exact position of all these components confirming close proximity to realize proper integration. The gate driver board dimensions measure 40mmx11mmx11mm.

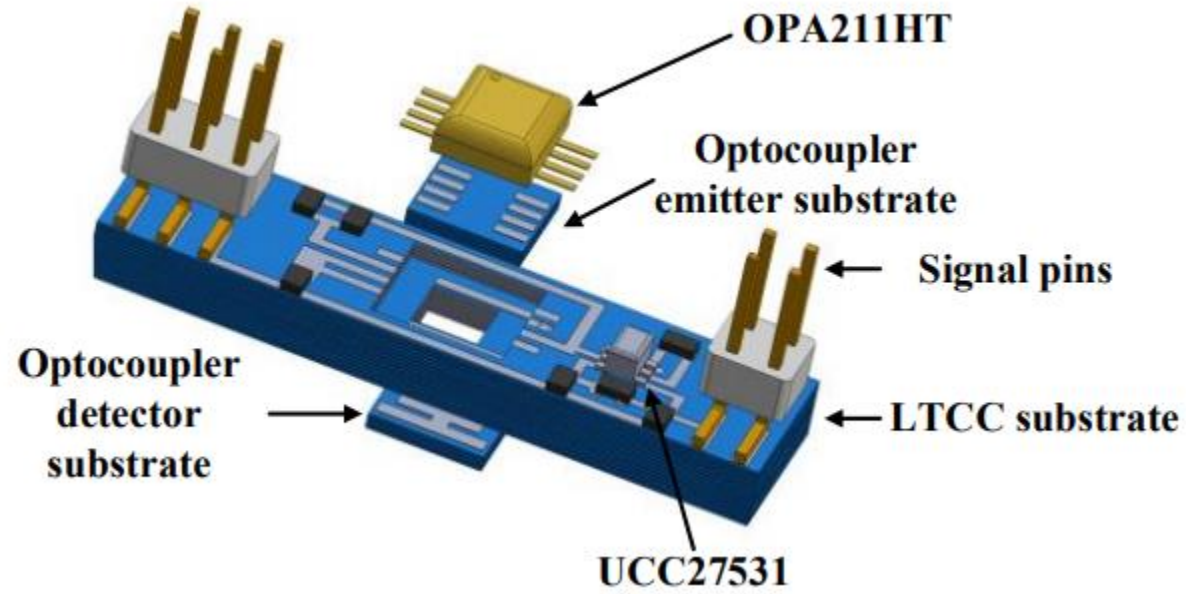


Fig. 3.10: 3-D model of the integrated LTCC-based gate driver board.

As stated in previous sections, in order to achieve close system integration of gate driver circuitries with high-density devices like SiC power modules, it is crucial to enhance the temperature limitations of the controlling components, including optocoupler, amplifiers and gate drivers [51]. Even though this is the case, reliability of the system integration would be restricted if the power module packaging isn't adapted for this level of system integration. The packaging materials, attachment and interconnection processes, and thermal management of the power module must be optimized for this level of integration. Taking all these into consideration ensures an increased power density and a higher temperature operation can be realized.

Chapter 4: Development of a Gate Driver Integrated SiC MOSFET Power Module

4.1 Packaging Materials in the Power Module Fabrication Process

Wide band gap semiconductor devices are setting the pace for the modern power electronics module. Generally, these WBG devices have lower intrinsic carrier concentration, higher electric breakdown field, higher thermal conductivity, and larger saturated electron drift velocity [63]. These characteristics that WBG devices possess give rise to operation with significantly higher voltage handling, higher switching speed and lower power losses. Even with the immense benefits of the WBG devices, major limitations exist in the packaging that would ensure optimal utilization of the power module. The module fabrication explained in this chapter is for SiC devices. The materials and fabrication process used is also detailed.

There are factors that must be considered when selecting materials for use in a power electronic module. These factors play a key role in not only preventing the device from damage but also ensuring optimal performance, that is, in taking advantage of the WBG benefits. The coefficient of thermal expansion (CTE), electrical parasitics, cost, and reliability of the materials must be considered during the material selection process. Also, the specific operational conditions of the power module in a system play a key role in the nature and type of material to be chosen. The figure below shows the major steps involved in the power module fabrication process.

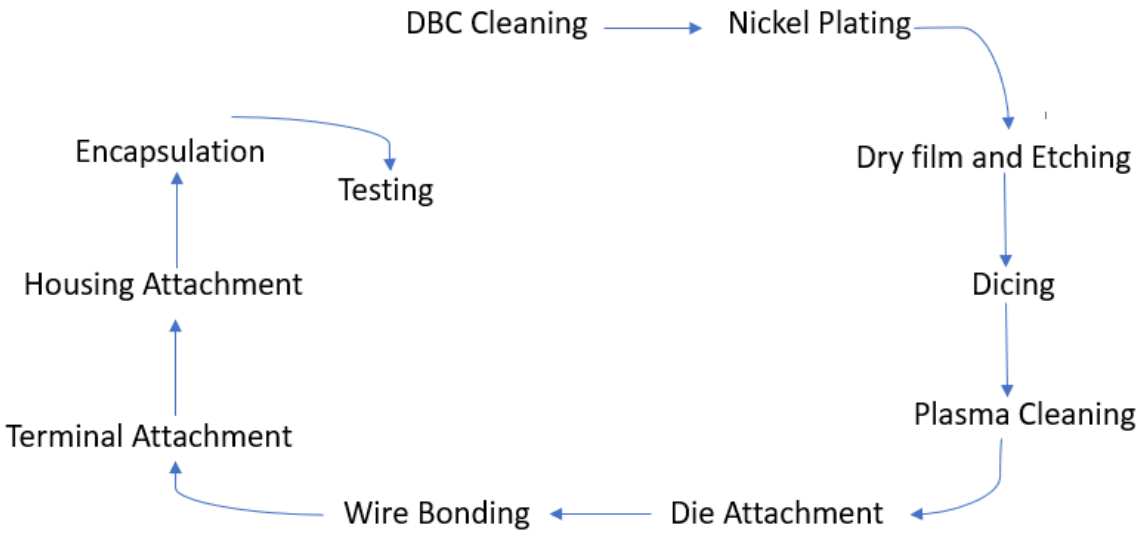


Fig. 4.1: Steps involved in power module fabrication process.

The first five steps DBC (Direct Bonded Copper) cleaning, nickel plating, dry film and etching, dicing, and plasma cleaning are useful in preparing for the die attachment step where the SiC device (in the form of a die) is attached to the surface of the DBC. The terminal attachment has to be done before wire bonding because of the heat the module is exposed to when attaching the power connectors which could have an adverse effect on the bond wire connection from the die to the DBC.

Figure 4.2 shows the cross-section of a conventional wire-bonded power module. This power module can be grouped into 3 sections. The lowest section comprises of the baseplate (in addition to a cooling system, not shown in the figure), the mid-section is the DBC together with the encapsulant, and the topmost section is the terminal and the casing (or housing). In selecting materials for the baseplate, it is worth noting that the baseplate serves as a cooling interface between the insulating substrate and the heat sink of the system during power transient. As such, the material to be used as a baseplate must have high thermal conductivity and its CTE must be

compatible with the insulating substrate. For power devices that operate at high power levels, the need for a highly suitable baseplate is heightened as these levels of power operation tend to generate heat, which has to be effectively removed from the system.

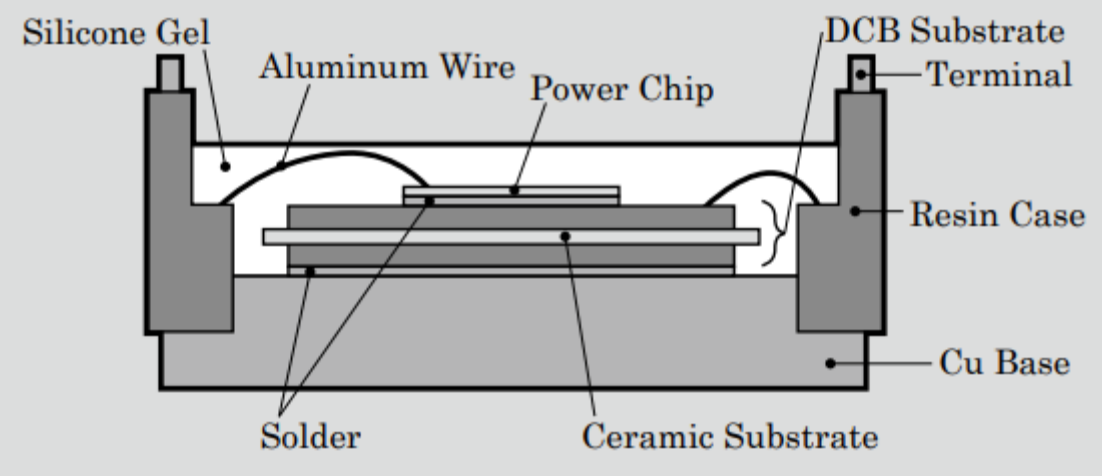


Fig 4.2: Cross-section of an aluminum wire-bond power module [52].

Some of the popular baseplate materials used in high power level applications are copper and aluminum. They may require gold plating for ease during soldering and to protect them from corrosion.

The materials for the DBC substrate are typically an insulator with high thermal conductivity. This is important as the conductive paths on the DBC surface have to be isolated from the bottom DBC and the baseplate. Some of the popular substrates used in high power density applications are AlN, AL_2O_3, and Si_3N_4 [15].

CTE compatibility of the DBC and baseplate is an important consideration. Table 4.1 details insulating substrates with their corresponding CTE and compatible base plate options.

Table 4.1: Table showing the compatible baseplate and substrate.

Insulating Substrate	CTE	Base Plate
Al_2O_3 (96%)	6	$Cu/Mo, AlSiC, Cu$
Al_2O_3 (99%)	7.2	$Cu/Mo, AlSiC, Cu$
AlN	4.6	$Cu/Mo, AlSiC, Cu$
Si_3N_4 (Hot pressed)	3.3	Not required

In selecting materials for the terminal attachment process, the nature of the connection to the outer electronic system has to be considered since the terminal structure can come in different shapes like a low profile (cube shaped with a circular threaded screw hole) or a C-shaped terminal with a hole at the top of the metal bend for fastening. Aluminum and copper are popular materials used as terminal connectors. Some of the properties required for the power terminal connector are; high mechanical strength, high electrical conductivity, high wear resistance and high corrosion resistance. Usually, the metals used for the power connectors tend to be coated to ensure corrosion from the environment is minimal. Silver, gold, and nickel are some of the materials used for plating the aluminum or copper terminal connector. Even though silver has the highest conductivity of ordinary metals, it tarnishes when exposed to the atmosphere because of its softness, hence, it is not durable. Gold and nickel are more durable. They both have excellent corrosion resistance and are also excellent conductors.

4.2 Fabrication of the Integrated SiC Power Module

In the fabrication of a power module, it is important to identify the various necessary fabrication steps at an early stage. Some of the key considerations are the careful selection of materials like the power module substrates for both the baseplate and the DBC, and also the attachment materials and methods.

Table 4.2: Components used in the integrated SiC power module.

Component	Material	Specification
Base plate	Cu	Au plated
DBC	Cu-AlN-Cu	Au plated 0.2 mm Cu 0.6 mm AlN
Switch	SiC	1.2 kV 149 A
Bond wire	Al	5 mil for gate loop 12 mil for power loop
Terminal	Cu	Au plated
Encapsulant	Silicone	Nusil R-2188 250 °C

Table 4.3: Solder and adhesive materials used.

Parts	Materials	Maximum temperature	Fabrication process
H9890-6A	Ag	260 °C	DBC & die attachment
SAC305	Sn/Ag/Cu	218 °C	Terminal attachment
CW2400	Conductive epoxy	343 °C	Gate driver attachment
RTV106	Epoxy	260 °C	Housing attachment

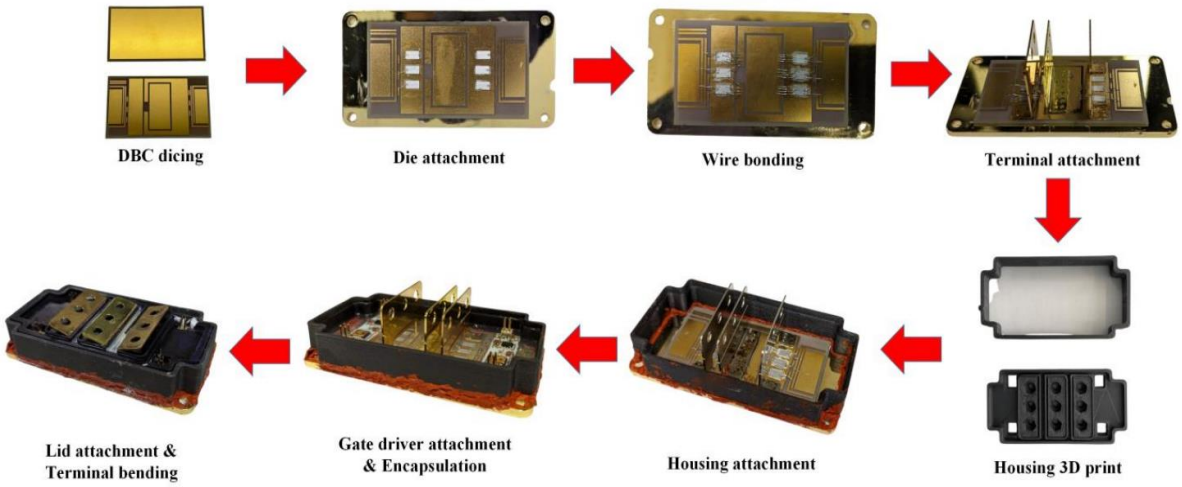


Fig. 4.3: Fabrication flow of the gate driver integrated SiC power module.

Figure 4.3 indicates each step of the process flow in fabricating the gate driver integrated SiC power module. The first step in the process is obtaining the module substrates. The material for the DBC is the copper-aluminum-copper (Cu-Al-Cu) with gold plating on the top and bottom

copper. The thickness of the copper bonding measures 0.2mm while the thickness of the aluminum nitride (AlN) substrate is 0.6mm. The DBC needs to be diced into desired sizes with a dicing saw according to the layout chosen. The next step is die attachment, which entails selection of the power die and attaching it to the surface of the DBC in its specified position. The die selected is the 1.2kV, 149A SiC MOSFET from CREE. The attachment process was carried out using silver sintering which is a method for high temperature attachment since this power module is for high temperature application. Silver paste (H9890-6A from NAMICS) was used for the die attachment process. The next process step is wire bonding and an aluminum (Al) wire was chosen as the bonding material. In this step, a connection is made between the DBC substrate and the power device. Two forms of connections are made here. One is for the power loop and the other is for the gate loop. The power loop connection uses a 12 mil Al bond wire since more current is anticipated to flow through this path while a 5 mil Al bond wire is used for the gate loop. The next step is attaching the DC+, DC- and AC terminals. Positioning of this terminal is an important consideration for mutual inductance cancellation which could effectively reduce the power loop inductance. The material used for the terminal is copper and it is gold plated to prevent corrosion since it tends to be exposed to air and to improve attachment quality to the DBC substrate. The attachment material is a SAC305 lead free high temperature solder alloy. This solder is an alloy of 96.5% tin, 3% silver and 0.5% copper. The adhesiveness of this solder alloy is good up to a maximum temperature of 218^{o}C. The next step entails printing a housing wall to encase the power module. A 3D printer is needed for this step and the measurements of the baseplate is used to make this 3D housing case. This 3D printed housing case is then attached to the baseplate. The material used for the attachment is a high temperature epoxy called RTV106 with a maximum operating temperature of 260^{o}C. It is important the

epoxy is used to completely seal around the baseplate of the power module to prevent leaks from the liquid encapsulant which is used later in the fabrication process. Now, two fabricated LTCC gate driver boards shown in figure 4.4 are integrated into the power module for the high side and low side MOSFET. The LTCC fabricated gate driver board has components such as optocouplers, resistors, capacitors, and the gate driver IC attached to the LTCC board. Figure 4.5 shows the fabrication flow of LTCC-based gate drivers. The attachment material used for attaching the LTCC gate driver board to the power module is the CW2400 conductive epoxy, which has a maximum operating temperature of 343°C.

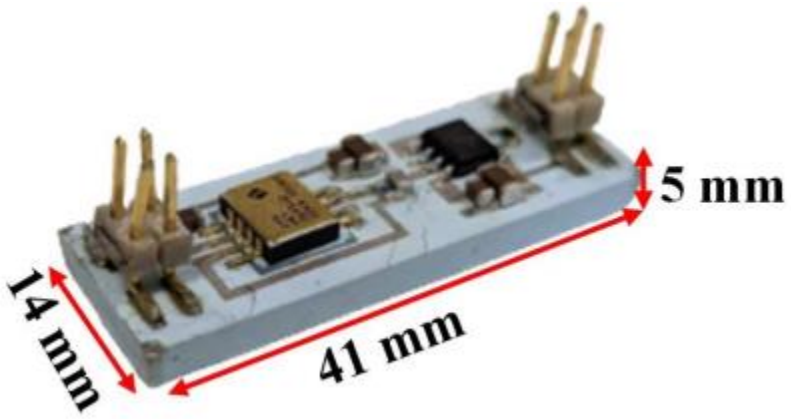


Fig. 4.4: Fabricated LTCC-based gate driver.

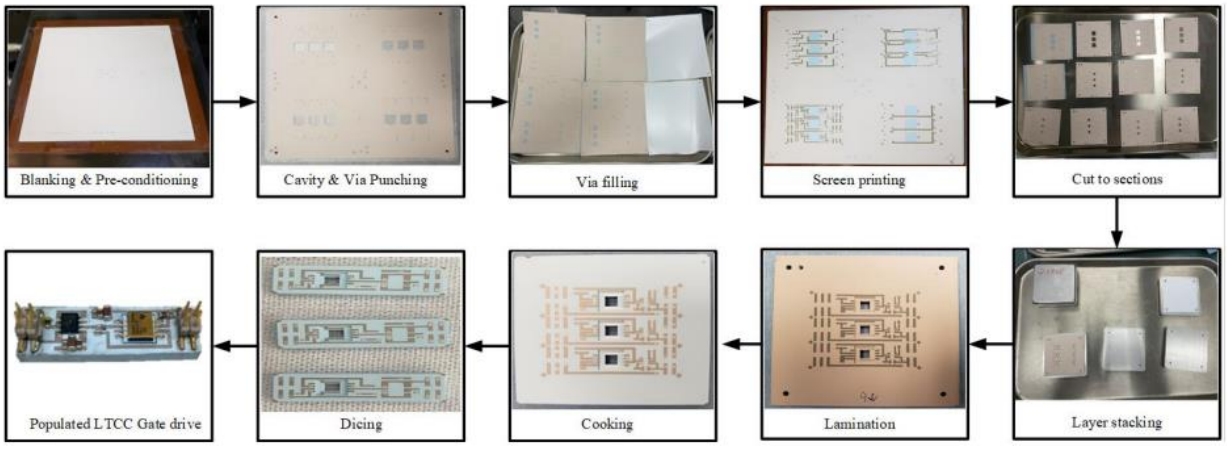


Fig. 4.5: Fabrication flow of LTCC-based gate drivers.

The subsequent step in the fabrication process involves the encapsulation process, which is essential for effectively sealing the power devices and protecting them from environmental contaminants. The encapsulant material is a Nusil R-2188 silicone plotting and encapsulating elastomer. It comes with two compounds with a 1 to 1 mix ratio of the two compounds. This encapsulant, after properly mixing the compounds, is poured on the encased top of the power module covering the gate driver board, power devices and wire bonds. Typically, a total of 15 g of encapsulant is needed for a power module dimension of 105mm, 55mm and 18mm which are the length, width and height respectively. The encapsulant can be cured at room temperature or at 150^{o}C for 30 mins [53]. In this process, both curing methods were used as the encapsulant in the power module was left for 24 hours at room temperature to remove any remaining air bubbles, then cured for 1.5 hours at 150^{o}C. The final step in the fabrication process entails bending the three power terminals to form a C-shape as seen in figure 4.3, then attaching the lid to complete the housing of the fabricated power module.

Chapter 5: Characterization of Optocoupler Gate Driver Integrated SiC MOSFET Power Module

5.1 Double Pulse Test Set-up

For the experimental phase of this paper, a double-pulse test (DPT) is performed to acquire and examine the switching characteristics of the device under test (DUT), which is a gate driver integrated SiC power module.

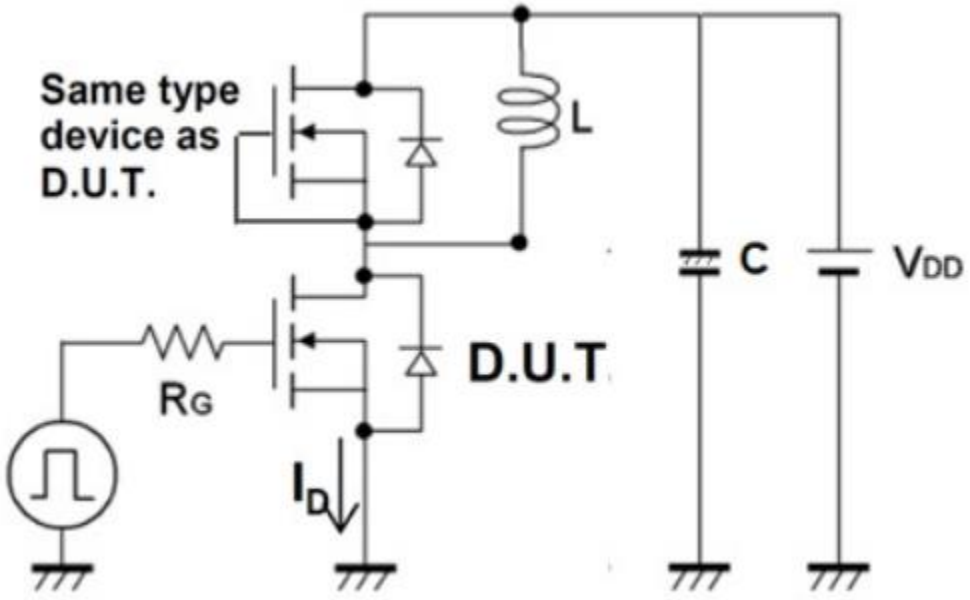


Fig. 5.1: Setup of a double pulse test circuit [54].

Carrying out the test entails, first, charging the capacitor bank to the desired voltage using a power supply. The duration of the pulse sequence has to be determined and used to calculate the inductive load using this formula;

$$V_{load} = L_{load}.\frac{di_{load}}{dt}$$

Provided the load voltage, which is the desired test voltage from the power supply, is known. This test is normally done with a purely inductive load. The first pulse turns on the lower transistor, which is the DUT, in figure 5.1. This results in a current flow in the inductor that charges it. The width of the first pulse is typically wide enough to a magnitude that is good for analysis [9]. Since this initial pulse initiates the flow of current through the inductor, the pulse is adjusted accordingly to reach the intended test current as shown in figure 5.2.

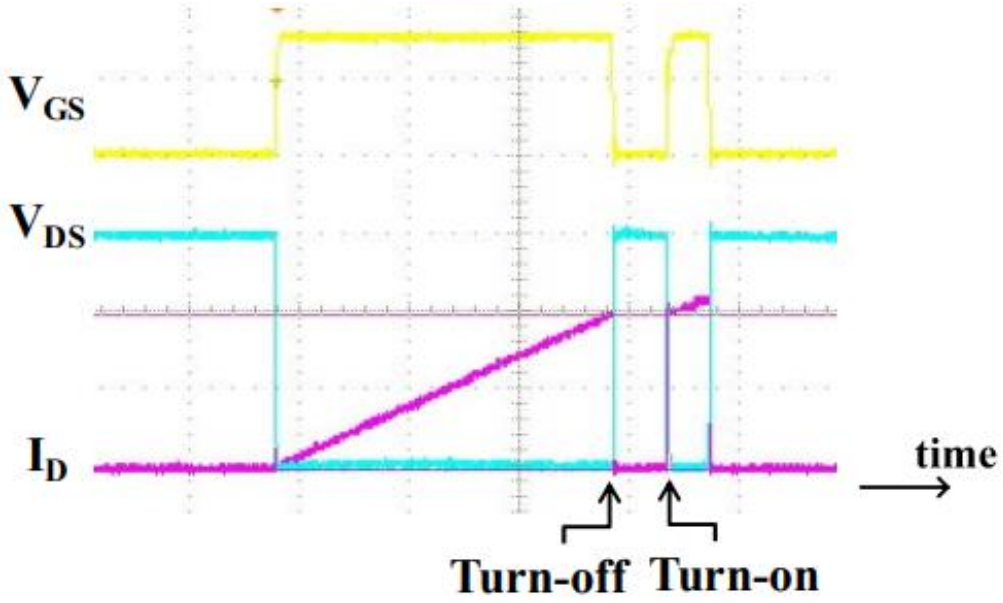


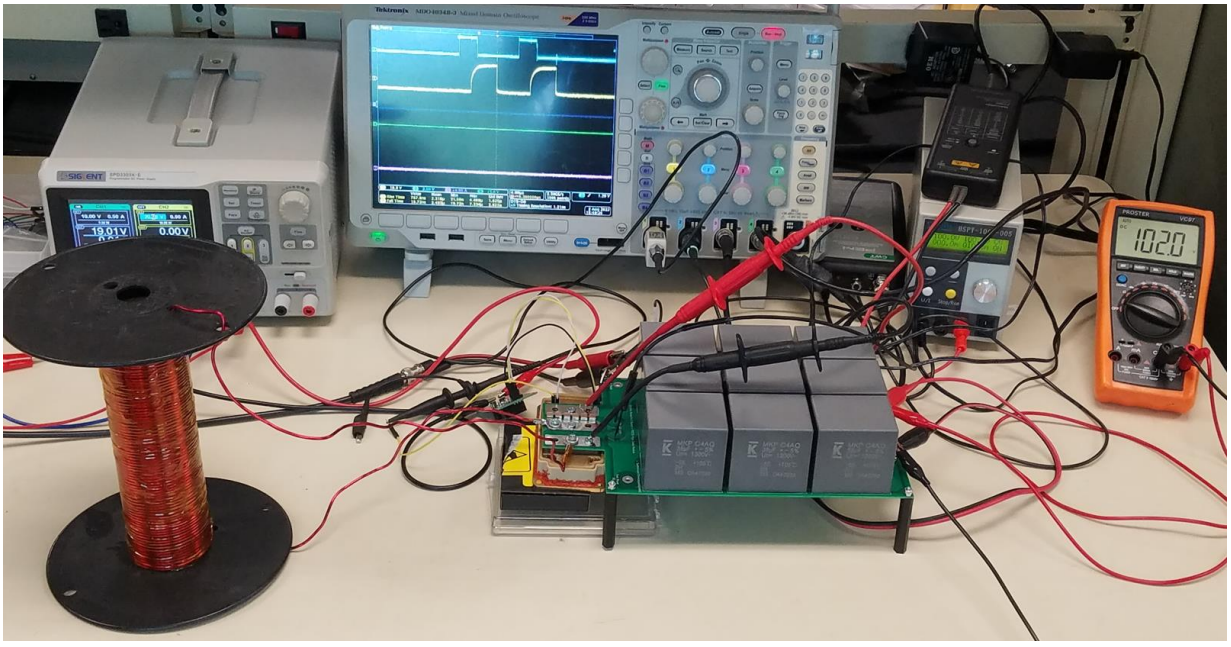
Fig. 5.2: Typical switching waveform of the double pulse test [65].

The turn off period in the switching waveform is short. This is intended to limit changes in the value of the inductor current. Notice the drain current of the DUT diminishes to nearly zero, despite the continued flow of current through the inductor (load). As a result, current is induced in the free-wheeling diode of the high side MOSFET. The second pulse turns the DUT on again as a result there is a voltage drop and drain current continues to rise as seen in the red marker of figure 5.2. The width of the second pulse needs to be carefully selected to prevent the current through the DUT from exceeding an unacceptable level [55].

5.2 Switching characterization of the SiC MOSFET power module with integrated LTCC-based gate driver.

The characterization is done to ascertain the switching performance of the DUT. The DUT is a fabricated SiC power module with integrated LTCC-based gate driver board, which was attached with a high temperature conductive epoxy (CW2400). The power device is a 1.2kV, 149A SiC MOSFET (CPM3-1200-0013A) from CREE. Switching evaluation of the DUT is performed at high temperatures to see the reliability of its switching performance from 25^{o}C to 200^{o}C. A hotplate (PC-600D by Corning) as seen in figure 5.3(b) is used to heat the DUT to perform this high temperature test. Other equipment used for the DPT setup are power supplies, function generator, inductive load which in this case was 115µH, capacitor bank (or busbar) and a 4-channel Tektronix oscilloscope to view the switching waveforms.

(a)



(b)

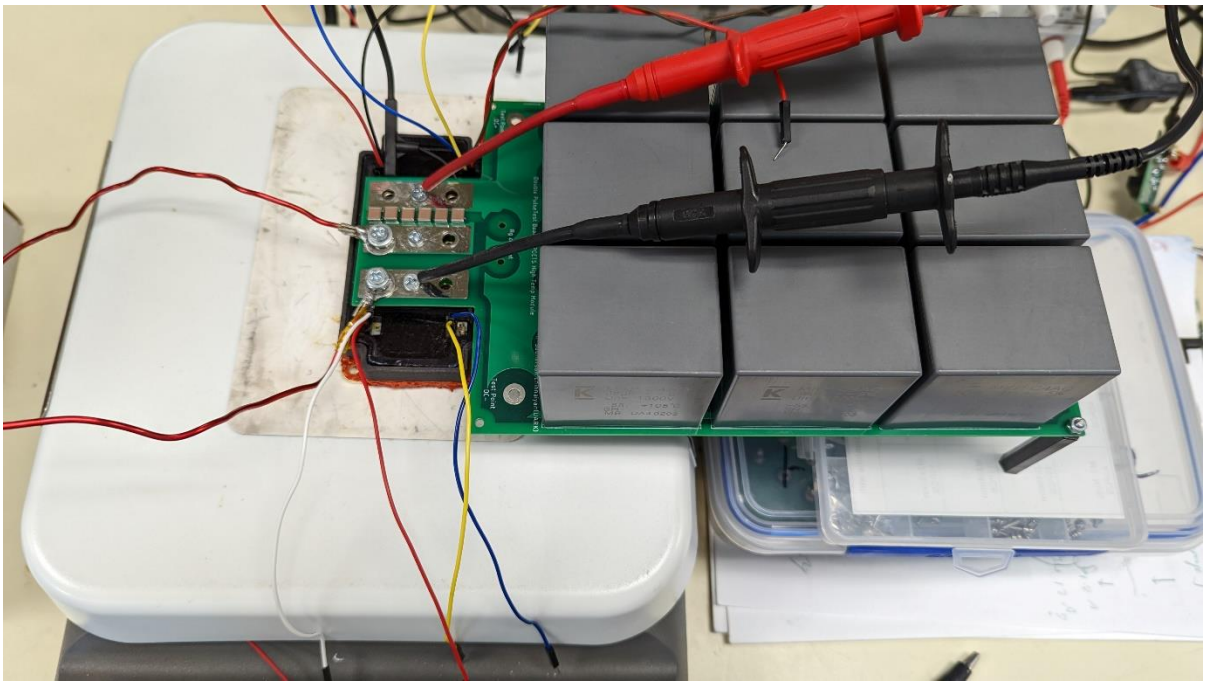
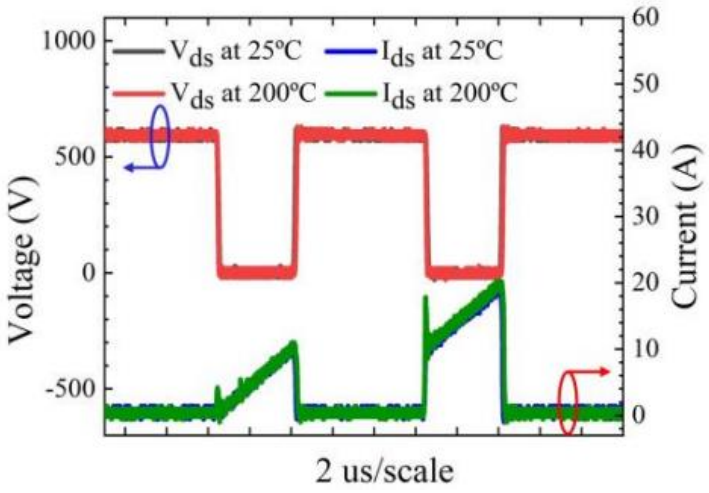


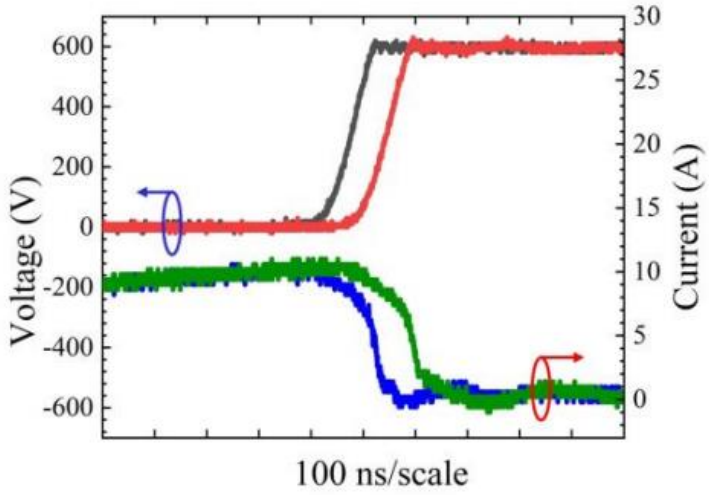
Fig. 5.3: Characterization setup for the gate driver integrated power module. (a) Testing done at room temperature (b) Testing done at elevated temperature of 200°C.

The DUT was subjected to testing with a drain-to-source voltage of 600 V and a drain current of 50 A. For this half bridge configured power module, the high side MOSFET was used for the switching and the low side MOSFET acted as the freewheeling diode. Figure 5.4 illustrates that the switching performance exhibits minimal variation across the temperature range of 25°C to 200°C.

(a)


1000
500
0
-500
Voltage (V)
60
50
40
30
20
10
0
Current (A)
V_{ds} at 25°C
I_{ds} at 25°C
V_{ds} at 200°C
I_{ds} at 200°C
2 us/scale

(b)


600
400
200
0
-200
-400
-600
Voltage (V)
30
25
20
15
10
5
0
Current (A)
100 ns/scale

(c)

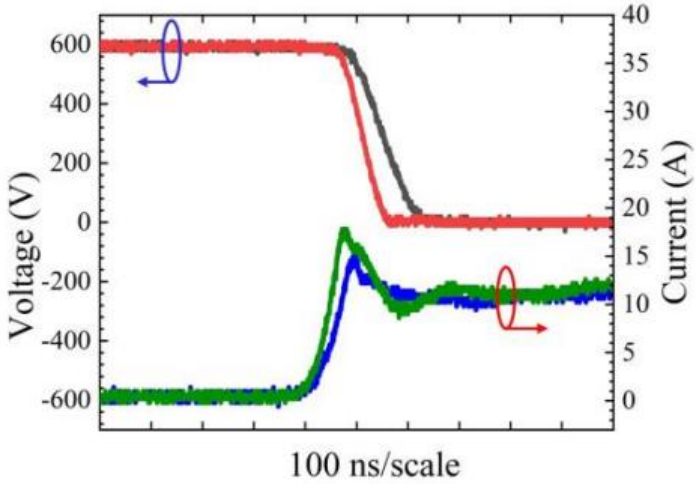


Fig. 5.4: DPT results of the integrated SiC power module at 25°C and 200°C (a) V_{ds} and I_d switching waveform, (b) turn-off measurements, (c) turn-on measurements.

A function generator was used to generate a pulse width of 4µs for both pulses, with a current rise and fall time recorded as approximately 100ns. The turn-off measurements were taken at the end of the first pulse while the turn-on measurements were taken at the start of the second pulse as shown in figure 5.2. Few oscillations and overshoots were noticed in the switching waveforms. Figure 5.4(a) shows a peak current overshoot at the beginning of the second pulse. This can be attributed to the reverse recovery of the stored charges in the freewheeling diode (low side MOSFET). As shown in figure 5.4(b), during the turn-off period, the combined duration of the current fall time and voltage rise time, which contributes to the generation of switching loss, rises from approximately 160 ns to around 170 ns as the temperature ranges from 25°C to 200°C. There is no peak overshoot in the turnoff transient but some oscillations exist in the V_{ds} and I_d waveforms, which could be attributed to the power loop inductance. Based on voltage overshoot calculation, the overvoltage was determined to be ~3.5V at 50A of current, considering a power loop parasitic inductance of ~7nH at 1MHz frequency, as shown in figure 3.3. The turn-on waveform in figure 5.4(c) illustrates a peak current overshoot from ~5A to ~8A as the temperature varies from 25°C to 200°C. This current overshoot can be

attributed to the charging and reverse recovery current of the device's body diode [56]. Furthermore, in figure 5.4(c), during the turn-on period, the combined duration of the current rise and voltage fall time, which contributes to the generation of switching loss, transitions from approximately 200 ns to around 180 ns.

Overall, the half bridge configured integrated power module shows reliable switching performance even when tested at high temperatures. The peak voltage overshoot and current overshoot as reported is minimal compared to DPT done on commercially available power modules.

Chapter 6 Conclusion and Future Work

6.1 Conclusion

The integration of an LTCC-based gate driver into a SiC power module has been analyzed in this thesis. The aim of this research is to address the challenges and benefits associated with this integration, particularly in terms of its electrical performance, thermal management, and overall system efficiency.

The motivation behind the integration of SiC power module and LTCC-based gate driver is to aid in increasing power density and switching performance because of the proximity of the gate driver to the power die. Also, reduction in the overall system size can be achieved which is of vital importance to various industries.

The LTCC-based optocoupler was studied in depth as it functions as a form of electrical isolation that ensures there is no direct conduction path between the low signal power levels and high signal power levels. In order to ensure proper integration of the LTCC-based optocoupler in the LTCC-based gate driver board, slots were created on both sides of the LTCC substrate. The LTCC-based gate driver with the integrated LTCC-based optocoupler was then integrated into a SiC power module using high temperature conductive epoxy (CW2400).

Double pulse test of the integrated power module was performed for varying temperatures from 25^{o}C to 200^{o}C. The results from this test show minimal voltage overshoot of ~3.5V for the turn-on and turn-off period and a current overshoot from ~5A to ~8A for temperature levels of 25^{o}C to 200^{o}C respectively.

In summary, this thesis emphasizes the significance and viability of integrating a gate driver into a SiC power module, thereby unlocking new opportunities for advanced power electronic applications.

6.2 Future Work

Since close integration of the gate driver and SiC power module has been achieved, more work needs to be conducted in improving the performance of this integration. The double pulse tests need to be done at a higher test voltage level close to 1kV. Moreover, it is necessary to conduct more rigorous testing at higher voltage levels to ensure the switching reliability of not only higher temperature power modules but also higher power density power modules. Finally, life expectancy and reliability tests need to be carried out on the integrated power modules to evaluate its performance over time. Lastly, a higher temperature gate driver IC needs to be developed with higher temperature ratings above 200^{o}C instead of the UCC27531 commercial gate driver IC used in the LTCC-based gate driver board.

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