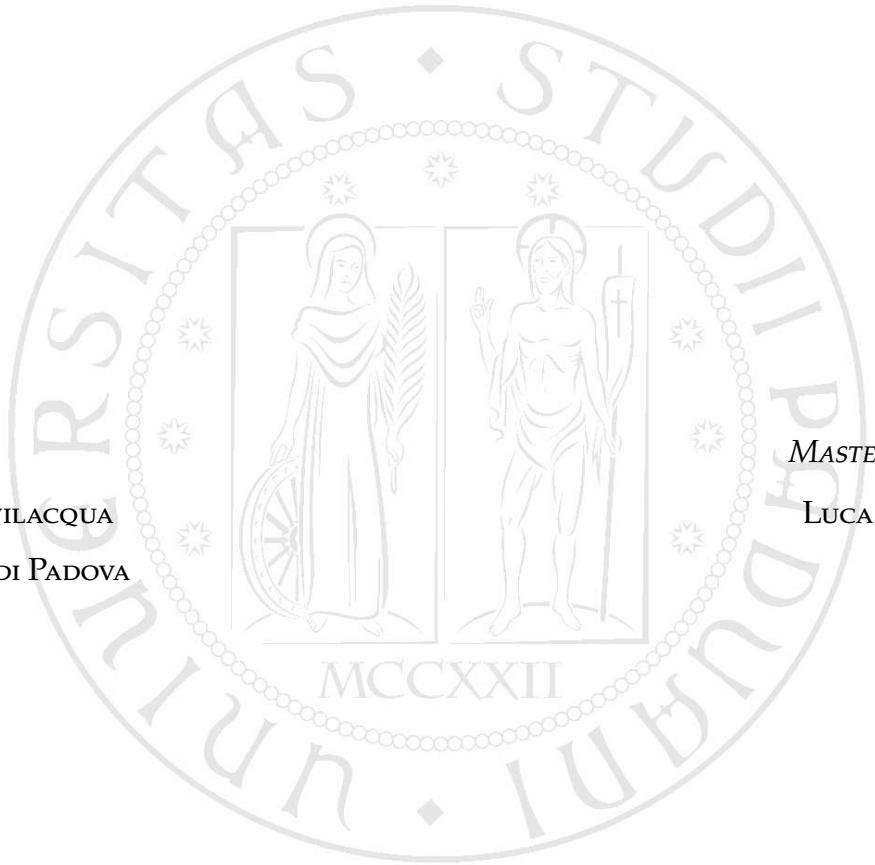
Università degli Studi di Padova

Dipartimento di Ingegneria dell'Informazione

Master Thesis in Electronic Engineering

Co-design of a Class-D Oscillator and Dedicated DC-DC Power Converter



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Abstract

This thesis analyses the design problems behind the realization of an integrated oscillator directly powered by a switching voltage regulator. Additionally, the possibility of using the oscillator itself to provide the switching frequency for the converter is explored. The building blocks constituting the circuit are analysed focusing on the different design challenges of each component, on how they interact with each other and if it is possible to obtain a fully integrated design. Some possible design solutions are then provided at the end of the thesis including simulation results for the presented circuits.

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Acronyms

SoC System-on-Chip

VLSI Very Large Scale Integration

VR Voltage Regulators

RF Radio Frequency

IF Intermediate Frequency

LO Local Oscillator

LDO Low-Dropout Regulator

SC Switched-Capacitor

LTI Linear Time Invariant

LTV Linear Time Variant

FSL Fast Switching Limit

SSL Slow Switching Limit

PSK Phase Shift Keying

QAM Quadrature Amplitude Modulation

PFM Pulse-frequency Modulation

SWM Switch Width Modulation

DCM Digital Capacitance Modulation

PN Phase Noise

ISF Impulse Sensitivity Function

FoM Figure of Merit

NOC Non-Overlapping Clock

VCO Voltage Controlled Oscillator

Introduction

In order to maximize the utilization of chip area and lower power consumption, the concept of System-on-Chip (SoC) has been introduced. The basic idea behind SoC is to integrate all the electronic components into a single chip. However, as different on-chip components require different voltages to operate, the role of voltage regulation becomes more important than ever in Very Large Scale Integration (VLSI). By tailoring the level of the supply voltage for the specific needs of each component we are in fact able to significantly diminish power dissipation in the system.

Although Voltage Regulators (VR) were traditionally realized as off-chip devices the requirements of nowadays complex integrated circuits, require the use of on-chip VR to be able to quickly adjust voltage during the operation of the circuit. Two different types of VR are mostly encountered in the recent literature: Switching VR and linear VR. Switching VR offer the highest efficiency, while linear VR are free from any switching noise, possesses ripple rejection capacity, low voltage noise, fast response time and smaller area overhead, but their efficiency is lower compared to that of switching VR.

In this work we focus on the power management of a particular Radio Frequency (RF) building block: the Local Oscillator (LO). We note however that most of the components present in a RF system are supply-sensitive blocks and the LO is no exception. This means that the LO may show an unwanted behaviour if there are disturbances in the power supply. Generally speaking, a cascade of switching and linear regulators is commonly used to drive an oscillator. In this scheme, showed in Figure 1, the switching VR initially converts the supply voltage in an efficient way and then, in order to guarantee the best performance for the LO, linear VR are often used, in the form of a low-noise Low-Dropout Regulator (LDO), to generate a "clean" supply for the oscillator.

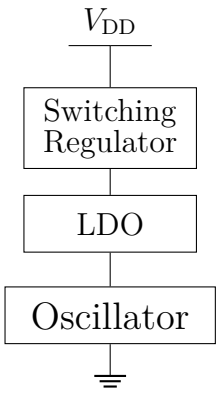


Figure 1: Power supply scheme for a conventional oscillator

Low noise LDOs however come at the cost of an additional quiescent current, which impacts the system power efficiency significantly. To improve the efficiency of the circuit one idea is to try and remove the low-noise LDO and to power the LO directly with a switching voltage regulator.[1, 12]

In this thesis we are therefore going to analyse the problem of realizing an oscillator directly powered by a switching voltage regulator. The switching regulator has to be designed in a way that doesn't interfere with the performance of the oscillator. Moreover, to save chip area, the regulator may use as its clock signal the output of the oscillator divided by an appropriate frequency divider. The equivalent block scheme of this circuit is shown in Figure 2. The final aim of this thesis is to understand if it is possible to realize such a circuit and whether or not it is possible to integrate all of its components. The oscillator topology that is going to be used in this thesis is that of a Class-D oscillator, which requires low supply voltage values in order to perform at its best. A Switched-Capacitor DC-DC converter is therefore employed to step down the supply voltage and directly power the oscillator.

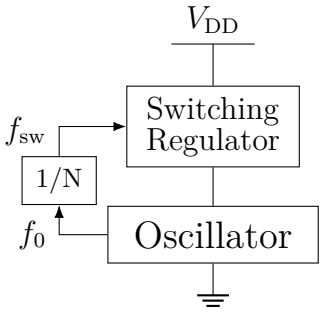


Figure 2: Power supply scheme for the oscillator in our thesis

The thesis is organized as follows. In chapter one the working principles of an RF oscillator and the design challenges that it involves are presented. In chapter two the Class-D oscillator is analysed in order to understand why this particular topology is so attractive. In chapter three a deep review of the design of Switched-Capacitor (SC) converters is carried out with specific considerations stemming from our particular design case. In chapter four a design prototype, first employing an off-chip capacitor for filtering the supply disturbances, is designed and its simulated performance is presented. Finally in the same chapter a second prototype is developed, this time using an on-chip capacitor, and the results that have been obtained are showed as well.

CHAPTER 1

LC Harmonic Oscillators Theory

In this chapter an introductory summary of the working principles of LC harmonic oscillators is made. We start from theoretical notes on how oscillation is achieved, first from a feedback theory standpoint and then in a more qualitative way. We proceed by analysing the building blocks that are necessary to realize an oscillator. Additionally, design problems such as phase noise and frequency pushing are analysed in this chapter in order to get a better insight on how oscillator design works.

1.1 Feedback Theory Analysis

An oscillator is an autonomous system capable of continuously generating a periodic output signal at a frequency of oscillation ω_0. Oscillators in electronics are divided into 2 types: harmonic oscillators, which produce a sinusoidal (or mostly sinusoidal) output signal, and relaxation oscillators which produce a non-sinusoidal input. For RF applications, relaxation oscillators are rarely used in high-performance transceivers because they generate signals of inadequate spectral purity[8], that is why in this work we are going to focus only on harmonic oscillators.

Oscillators in order to function must have a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal[13]. This behaviour can be studied by means of feedback theory by representing the oscillator as in Figure 1.1, where $V_{\text{in}} = 0$ being the oscillator an autonomous system. Note however that V_{in} could also be viewed as the noise of the oscillator itself.

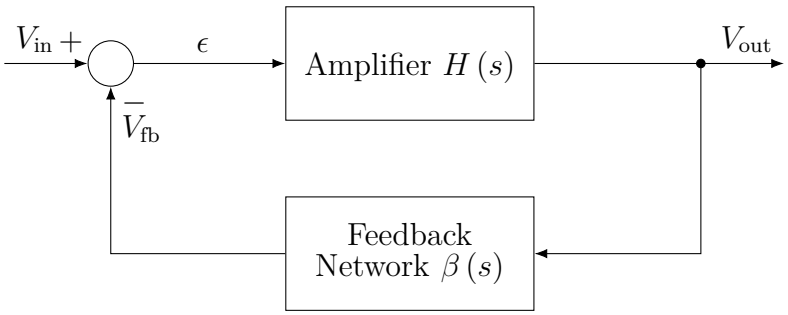


Figure 1.1: General model of a feedback system

For simplicity we can represent the transfer function of the system in Figure 1.1 as:

$$\frac{Y(s)}{X(s)} = \frac{H(t)}{1+\beta(s)H(s)} = \frac{K}{(s-p_1)(s-p_2)} \tag{1.1}$$

Then since the oscillator is an autonomous system and $V_{\text{in}} = 0$ we have that the natural response of the system is:

$$v_{\text{out}}(t) = a_1 e^{p_1 t} + a_1 e^{p_2 t} \tag{1.2}$$

where a_1 and a_2 are the initial condition of the system. In order to observe oscillation at the frequency ω_0, the system must have in its root locus conjugate imaginary poles positioned at $p_{1,2} = \sigma \pm j\omega_0$, with $\sigma \geqslant 0$. If these conditions are realized the natural response of the system, assuming $a_1 = a_2^*$, can be rewritten as:

$$v_{\text{out}}(t) = 2|a_1|e^{\sigma t} cos\left(\omega_0 t + \underline{/a_1}\right) \tag{1.3}$$

The time evolution of $v_{\text{out}}(t)$ has been plotted in Figure 1.2 and we can clearly see how the amplitude of oscillation exponentially increases, while oscillating at ω_0. Note however that in real circuits, due to various non-linear effects, the amplitude of oscillation eventually reaches a steady state value and ceases to increase.

Alternatively, the requirements for a system to oscillate at ω_0, can also be formulated mathematically in the form of the "Barkhausen Criteria". Assuming that in Figure 1.1 the feedback network is such that $\beta(s) = 1$, then the Barkhausen Criteria are as follows:

$$|H(j\omega_0)| = 1 \tag{1.4}$$

$$\underline{/H(j\omega_0)} = 180^\circ \tag{1.5}$$

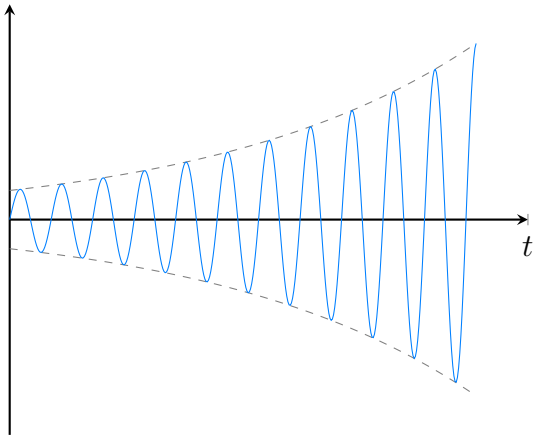
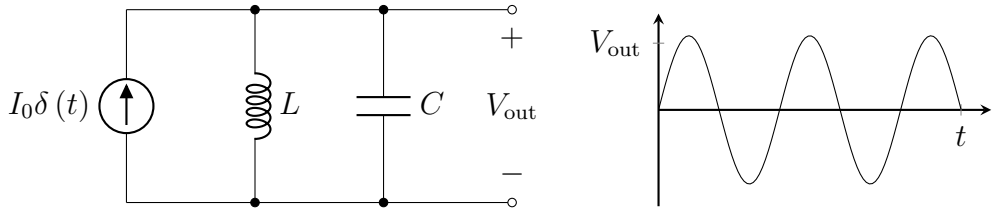


Figure 1.2: Response of an unstable system oscillating at ω_0

When referring to Figure 1.1, the conditions described by Equation 1.4 and Equation 1.5 mean that any noise signal V_{n} at ω_0 present on V_{in} will generate a signal $V_{\text{fb}} = -V_{\text{n}}$ which will the add up with $V_{\text{in}} = V_{\text{n}}$, causing ϵ to increase and creating a positive feedback loop that eventually will build into an oscillation at ω_0.

1.2 Negative Resistance Method

Another more intuitive way to understand the behaviour of a harmonic oscillator comes from modelling it as a combination of a lossy resonator (a circuit having resonant behaviour) and an active circuit that cancels the loss. Resonators can be realized by using quarter-wave pieces of transmission line or even quartz crystals, but the most common way to realize a resonator is by the means of a RLC tank, which is the implementation used by the oscillators presented in this work. To better understand this concept, an equivalent model of an ideal lossless LC tank is first shown in Figure 1.3.



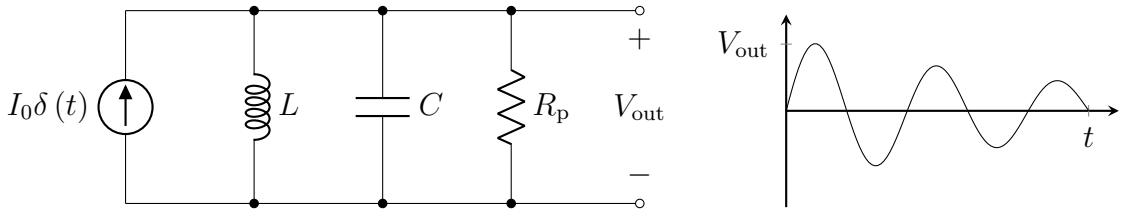
(a) Equivalent circuit scheme (b) Plot of V_{out}

Figure 1.3: Lossless LC tank

If we apply a current impulse, $I_0\delta(t)$, to the lossless tank of Figure 1.3 the impulse is entirely absorbed by C, generating a voltage of I_0/C. The charge on C then begins to flow through L, and the output voltage falls. When V_{out} reaches zero, C carries no energy, but L has a current equal to $L\frac{dV_{\text{out}}}{dt}$, which charges C in the opposite direction,

driving V_{out} toward its negative peak. This periodic exchange of energy between C and L continues indefinitely, with an amplitude given by the strength of the initial impulse.

Considering now the model of a real lossy RLC tank, shown in Figure 1.4, we have that such a circuit behaves similarly, except that the resistance R_{p} consumes some of the capacitor energy in every cycle, causing an exponential decay in the amplitude.



(a) Equivalent circuit scheme

(b) Plot of decaying V_{out}

Figure 1.4: Lossy RLC tank

As anticipated, by combining a lossy RLC tank with an active element that realizes a "negative resistance" $-R$ we are capable of restoring the loss caused by R_{p} and have the circuit continuously oscillate as in Figure 1.3b. The equivalent model of a harmonic oscillator realized in this way is shown in Figure 1.5.

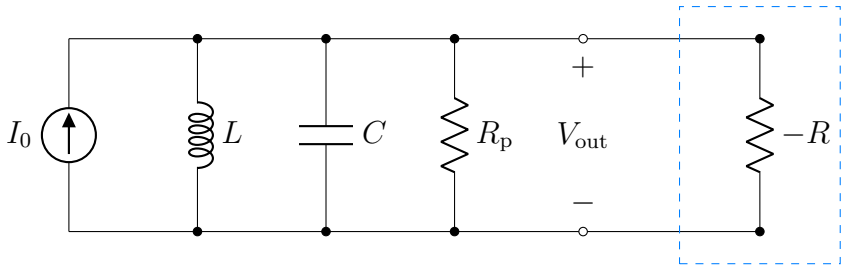


Figure 1.5: Harmonic RLC oscillator

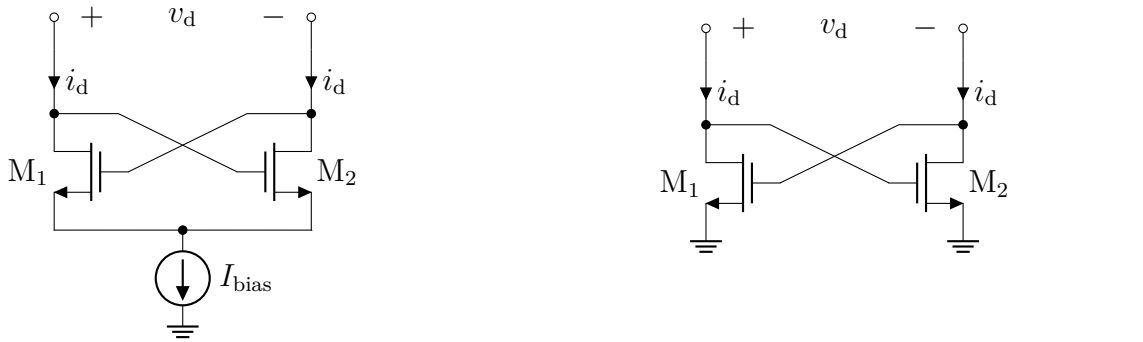
By writing the transfer function of the system from the input current I_0 to the output voltage V_{out}, which corresponds to the impedance of the equivalent circuit, we get the following expression:

$$Z_0 = \frac{V_{\text{out}}}{I_0} = \left(\frac{1}{sL} + sC + \frac{1}{R_{\text{p}}} - \frac{1}{R}\right)^{-1} = \frac{sLR_{\text{p}}R}{s^2LCR_{\text{p}}R + sL\left(R - R_{\text{p}}\right) + RR_{\text{p}}} \tag{1.6}$$

If we impose in Equation 1.6 the condition $R \geqslant R_{\text{p}}$ we have that the transfer function becomes that of an unstable system having conjugate imaginary poles placed at $p_{1,2} = \sigma \pm j\omega_0$ with $\sigma \geqslant 0$. This means that the equivalent circuit of Figure 1.5 correctly realizes a harmonic oscillator of oscillating frequency $\omega_0 = 1/\sqrt{LC}$.

1.3 The Cross-Coupled Pair

Now that we have understood the basic principles behind the behaviour of LC harmonic oscillators, we are going to briefly touch on how to realize the active circuit that allow us to implement a negative resistance. The most popular solution to implement a negative resistance is by the means of the so called "cross-coupled pair" which is depicted in Figure 1.6.



(a) Cross-coupled pair with current tail generator (b) Cross-coupled pair with no current tail generator

Figure 1.6: Cross-coupled pair

This topology owes its name to the particular way in which the two mosfets M_1 and M_2 are connected. Note that the current source I_bias, shown in Figure 1.6a, is inserted to correctly bias the pair. Cross-coupled oscillators realized in this way take the name of "tail-biased oscillators". However, as we will see later, there exist other oscillator topologies, such as Class-D oscillators, which don't make use of this biasing current and have the cross-coupled pair realized as in Figure 1.6b.

We focus now on the equivalent small signal scheme of the cross-coupled pair of Figure 1.6a which is shown in Figure 1.7.

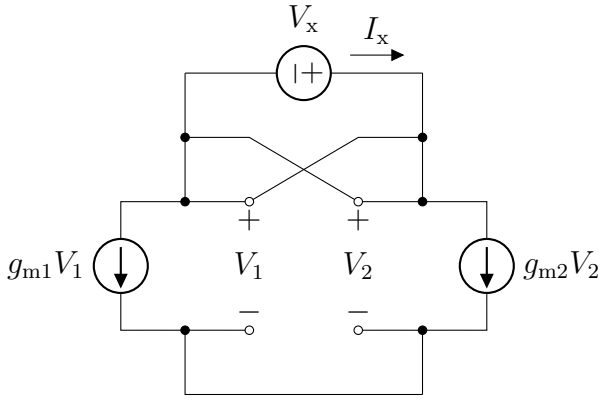


Figure 1.7: Equivalent small signal scheme of a cross-coupled pair

We want to prove that by looking inside the terminals of the crossed-coupled pair we see a negative resistance. Note that in order to simplify the calculations we assume that the small-signal resistance r_0 can be neglected ($r_0 \gg 1/g_\mathrm{m}$) and we don't take into account the parasitic capacitances of the transistors. We have that:

$$I_\mathrm{x} = -g_\mathrm{m1}V_1 = -g_\mathrm{m2}V_2 \tag{1.7}$$

and since $V_\mathrm{x} = V_1 - V_2$ we can write:

$$\frac{V_\mathrm{x}}{I_\mathrm{x}} = -\left(\frac{1}{g_\mathrm{m1}} + \frac{1}{g_\mathrm{m2}}\right) \tag{1.8}$$

which, by imposing $g_\mathrm{m} = g_\mathrm{m1} = g_\mathrm{m2}$ can be reduced to:

$$\frac{V_\mathrm{x}}{I_\mathrm{x}} = -\frac{2}{g_\mathrm{m}} \tag{1.9}$$

which clearly shows that the resistance of the crossed-coupled pair is negative.

1.4 Class-B Oscillators

We now have all the elements to understand the working principles behind the behaviour of LC harmonic oscillators. If we combine the cross-coupled pair of Figure 1.6a with a RLC resonator, such as the one in Figure 1.4, we end up with the very popular topology of a Class-B oscillator, which is depicted in Figure 1.8:

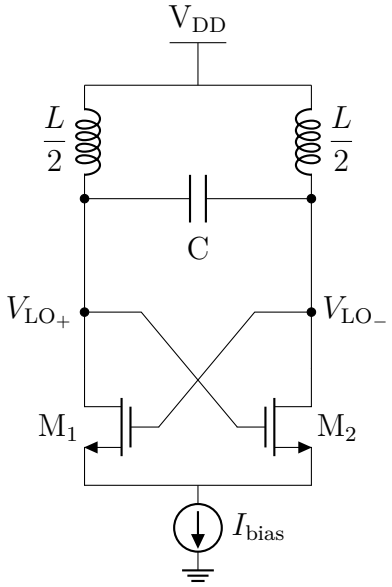


Figure 1.8: Class-B oscillator

If the negative resistance, provided by the cross-coupled pair as in Equation 1.9, is sufficient to cancel the loss due to the resistance of the tank we have that oscillation in the Class-B oscillator starts up. The oscillation frequency for a Class-B oscillator is of:

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \tag{1.10}$$

The amplitude of oscillation $\hat{V}_{\mathrm{LO}}$ of the differential signal between nodes V_{LO_+} and V_{LO_-} called $V_{\mathrm{LO}}(t)$ increases as in Figure 1.2 and eventually reaches a steady state value instead of continuously growing. This is because as $\hat{V}_{\mathrm{LO}}$ increases the switches of the cross-coupled pair start to operate in hard switching. As a result M_1 and M_2 continuously alternate between an OFF state, where they are not conducting, and an ON state, where they work in the triode region, causing a decrease in g_{m} that leads $\hat{V}_{\mathrm{LO}}$ to stop growing and reach steady state. An intrinsic consequence of hard switching is that when, for example, M_1 is in the ON state, M_2 is in the OFF state and vice versa.
This aids our analysis aimed at understanding what is the steady state value of $\hat{V}_{LO}$.
By considering only one of the transistors of the pair during a period of oscillation it's easy to see that the current I_{M} absorbed by the transistor is square-wave like. Therefore, since we know the Fourier expansion for a square wave, we have that:

$$I_{\mathrm{M}} = \frac{I_{\mathrm{bias}}}{2} + \sum_{n=1,3,5,\ldots}^{\infty} \frac{2I_{\mathrm{bias}}}{n\pi} sin\left(2\pi f_0 \cdot n \cdot t\right) \tag{1.11}$$

Note how by summing I_{M1} and I_{M2} we get back the current I_{bias}.
We now take a look at the equivalent AC model of the oscillator shown in Figure 1.9.

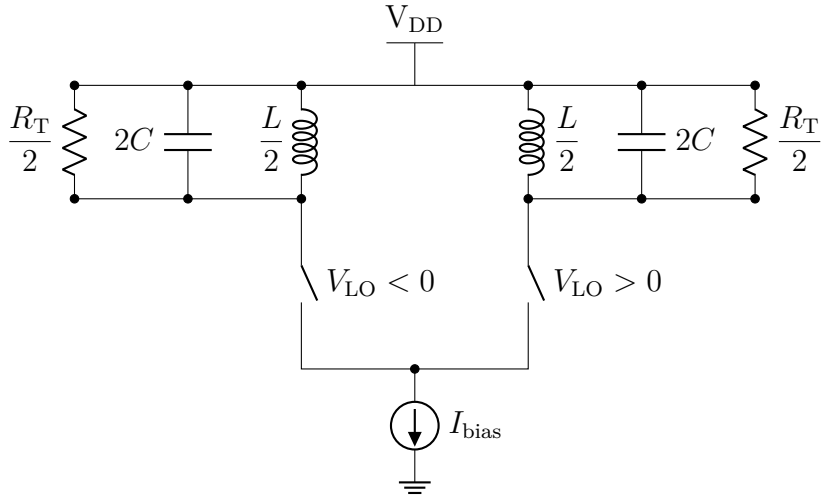


Figure 1.9: Equivalent circuit of a Class-B oscillator

We have that the tank has been divided into 2 separate portions where R_{T} is the equivalent parallel resistance of the inductor parasitic resistance and it's equal to:

$$R_{\mathrm{T}} \simeq Q_{\mathrm{L}}^2 * R_{\mathrm{L}} \simeq Q_{\mathrm{L}} \omega_0 L_{\mathrm{T}} \tag{1.12}$$

The impedance of one of the portions of the tank at the resonance frequency is:

$$Z_{\mathrm{T}}(\omega_0) = 2C /\!\!/ \frac{L}{2} /\!\!/ \frac{R_{\mathrm{T}}}{2} = \frac{R_{\mathrm{T}}}{2} \tag{1.13}$$

while for other frequencies multiple of ω_0 we have that $Z_{\mathrm{T}}(\omega) \simeq 0$.
From Equation 1.11 we can then calculate the current in the tank for ω_0:

$$I_1 = \frac{2}{\pi} I_{\mathrm{bias}} \tag{1.14}$$

Putting all equations together, the voltage on nodes V_{LO_+} and V_{LO_-} is given by:

$$V_{\mathrm{LO}_+}(t) = V_{\mathrm{DD}} + \frac{R_{\mathrm{T}}}{2} I_1 sin(\omega_0 t) = V_{\mathrm{DD}} + \frac{2}{\pi} I_{\mathrm{bias}} \frac{R_{\mathrm{T}}}{2} sin(\omega_0 t) \tag{1.15}$$

$$V_{\mathrm{LO}_-}(t) = V_{\mathrm{DD}} - \frac{R_{\mathrm{T}}}{2} I_1 sin(\omega_0 t) = V_{\mathrm{DD}} - \frac{2}{\pi} I_{\mathrm{bias}} \frac{R_{\mathrm{T}}}{2} sin(\omega_0 t) \tag{1.16}$$

Therefore we have a formula for the oscillation amplitude of the Class-D oscillator:

$$\hat{V}_{\mathrm{LO}} = \frac{2}{\pi} R_{\mathrm{T}} I_{\mathrm{bias}} \tag{1.17}$$

1.4.1 Voltage and Current Limited Regime

As a result of Equation 1.17 the oscillation amplitude of the Class-B oscillator $\hat{V}_{\mathrm{LO}}$ depends on the value of I_{bias}. This means that if we are interested in increasing $\hat{V}_{\mathrm{LO}}$ we can do so by raising the value of I_{bias} at the obvious cost of more power consumption. However there comes a point in the operation of the Class-B oscillator where $\hat{V}_{\mathrm{LO}}$ saturates to $\hat{V}_{\mathrm{LO}} = V_{\mathrm{DD}} - V_{\mathrm{S}}$, with V_{S} the voltage on the source terminal of the switches, and no longer increases as I_{bias} does. The only way to increase $\hat{V}_{\mathrm{LO}}$ then is by raising V_{DD}. The oscillator therefore based on the values of I_{bias} and V_{DD} moves between two different regimes. In the "current limited regime" $\hat{V}_{\mathrm{LO}}$ is proportional to I_{bias} as we have come to expect. On the other hand, in the "voltage limited regime" $\hat{V}_{\mathrm{LO}}$ is proportional to V_{DD} and increasing I_{bias} has no effect on $\hat{V}_{\mathrm{LO}}$. This behaviour is shown in Figure 1.10.

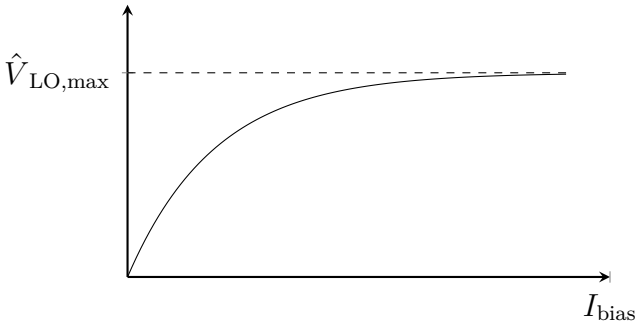


Figure 1.10: $\hat{V}_{\mathrm{LO}}$ as a function of I_{bias}

Note that, as we have anticipated, Class-D oscillators don't include a tail generator in their cross-coupled pair that limits the absorbed current to a value I_{bias}. Therefore we can expect the Class-D oscillator to operate in the "voltage limited regime" and have their oscillation amplitude depend only on V_{DD}.

1.5 Phase Noise

An ideal oscillator, as explained in Section 1.1, is capable of continuously generating a periodic output signal at a frequency of oscillation ω_0. This signal, in the ideal case, can be written as $x(t) = cos(\omega_0 t)$ and is such that its zero crossing occurs at exact integer multiples of $T = 2\pi/\omega_0$. In reality however the noise of the oscillator randomly perturbs the zero crossing. To model this behaviour we rewrite $x(t)$ as:

$$x(t) = cos(\omega_0 t + \phi_{\mathrm{n}}(t)) \tag{1.18}$$

where the term $\phi_{\mathrm{n}}(t)$ is a small random phase quantity that deviates the zero crossing from the integer multiples of T and it's what we call Phase Noise (PN). An example of this effect in the time domain, although greatly exaggerated, is shown in Figure 1.11.

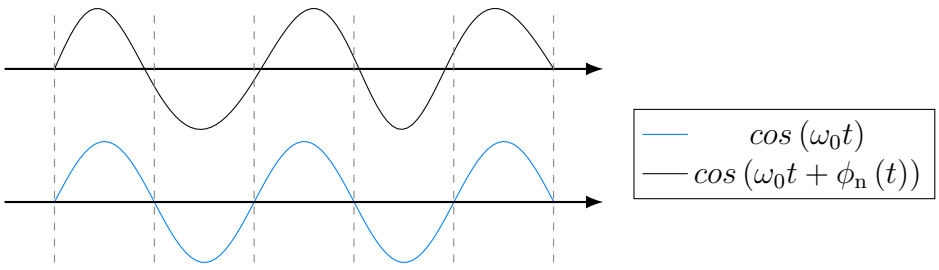
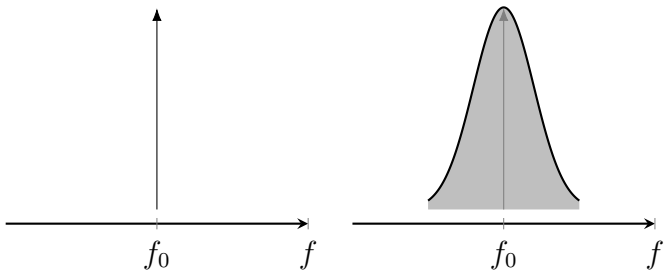


Figure 1.11: Output waveforms for an ideal and a noisy oscillator

The perturbations of the zero crossing of the waveform, given by phase noise, have another effect that can be appreciated by looking at the waveform in the frequency domain. We know that frequency can be expressed as $f_0 = 1/T$. However by considering a noisy oscillator the value of T is no longer fixed, as now T randomly fluctuates due to ϕ_{n}. This leads the frequency of the waveform to fluctuate as well. By looking at the spectrum of the output waveform of a noisy oscillator, instead of observing a pure impulse centered at f_0, as we would expect from a sinusoidal source, we will see that the spectrum has "broadened". The difference between these spectra is illustrated in Figure 1.12.



(a) Ideal output spectra (b) Noisy output spectra

Figure 1.12: Comparison between ideal and noisy spectra of an oscillator

This behaviour can be formulated mathematically by rewriting the time-domain expression in the following way:

$$x(t) = Acos(\omega_0 \cdot t + \phi_{\mathrm{n}}(t)) \tag{1.19}$$

$$\simeq Acos(\omega_0 \cdot t) - Asin(\omega_0 t)\, sin(\phi_{\mathrm{n}}(t)) \tag{1.20}$$

$$\simeq Acos(\omega_0 \cdot t) - A\phi_{\mathrm{n}}(t)\, sin(\omega_0 t) \tag{1.21}$$

Then since $X(\omega) \coloneqq \mathcal{F}[x(t)]$ and $\Phi_{\mathrm{n}}(\omega) \coloneqq \mathcal{F}[\phi_{\mathrm{n}}(t)]$, by applying some simple signals theory for $\omega > 0$ we get the following spectrum:

$$X(\omega) = \frac{A}{2} \cdot (\delta(\omega + \omega_0) + \Phi_{\mathrm{n}}(\omega + \omega_0)) \tag{1.22}$$

We have that Equation 1.22, as expected, shows that the spectrum of $x(t)$ is composed of an impulse centered in ω_0 and of the spectrum of $\phi_{\mathrm{n}}(t)$ translated to the center frequency ω_0. The composition of $\Phi_{\mathrm{n}}(\omega)$ is going to be analysed later, but for now it's important to note that $\Phi_{\mathrm{n}}(\omega)$ decreases as we move away from ω_0.

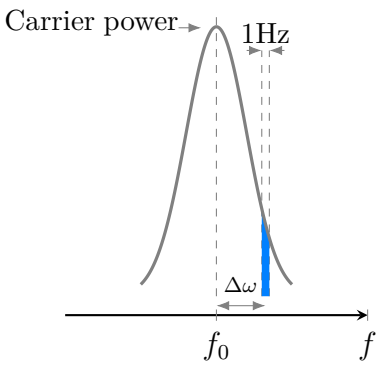


Figure 1.13: Specification of phase noise

Phase noise is thus measured with respect to a certain "frequency offset" $\Delta\omega$ from the carrier. Referencing Figure 1.13, we have that PN is defined by first considering a 1Hz bandwidth of the noise spectrum at an offset $\Delta\omega$ from the carrier, then measuring the power in this bandwidth and finally normalizing the result to the "carrier power" which can be viewed as the peak of the spectrum. The unit used to measure PN is called dBc/Hz which stands for "dB with respect to the carrier" reflecting on this procedure.

1.5.1 Phase Noise in Oscillators - LTI Approach

Let's consider the equivalent RLC model of a harmonic oscillator under Linear Time Invariant (LTI) conditions, as the one depicted in Figure 1.4. We model the noise current in the tank as a white thermal source $S_{\text{i}R_\text{T}}(f)$ given by the tank resistance R_T, with mean squared spectral density of:

$$S_{\text{i}R_\text{T}}(f) = \frac{\overline{i_\text{n}^2}}{\Delta f} = \frac{4k_\text{B}T}{R_\text{T}} \tag{1.23}$$

with k_B the Boltzmann constant and T the temperature. In order to carry out our analysis, we assume that the negative resistance $-R$, perfectly compensates, at steady state, the losses given by the tank resistance R_T, but not its noise as seen in Figure 1.14

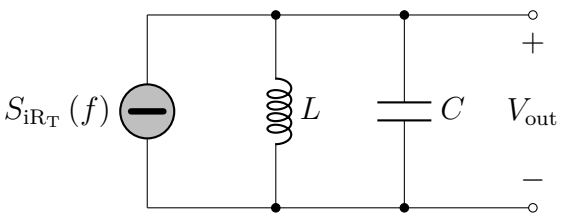


Figure 1.14: Equivalent circuit of a noisy harmonic RLC oscillator

For $\Delta\omega \ll \omega_0$ the impedance of the LC tank of Figure 1.14 may be approximated as:

$$Z\left(\omega_{\mathrm{o}}+\Delta\omega\right) \simeq -j \cdot \frac{\omega_{\mathrm{o}} L}{2\dfrac{\Delta\omega}{\omega_0}} \tag{1.24}$$

which can be rewritten, by considering $L = R_{\mathrm{T}}/\left(\omega_0 Q\right)$ where Q is the quality factor of the unloaded tank, as follows:

$$\left|Z\left(\omega_{\mathrm{o}}+\Delta\omega\right)\right| \simeq \frac{\omega_0 R_{\mathrm{T}}}{2Q\Delta_{\omega}} \tag{1.25}$$

In this way we emphasize the dependence of $\left|Z\left(\omega_{\mathrm{o}}+\Delta\omega\right)\right|$ from Q and R_{T} as opposed to L. Next, we calculate the spectral density of the mean square noise voltage:

$$S_{\mathrm{v_n}}(f) = \frac{\overline{v_{\mathrm{n}}^2}}{\Delta f} = |Z|^2 \cdot \frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} = 4k_{\mathrm{B}} T R_{\mathrm{T}} \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{1.26}$$

We note that $S_{\mathrm{v_n}}(f) \propto^{-1} \Delta\omega^2$ due to the filtering action of the tank. This $1/f^2$ behaviour simply reflects the fact that the voltage frequency response of an RLC tank rolls off as $1/f$ to either side of the center frequency and power is proportional to the square of voltage. Moreover we notice that by increasing Q the value of $S_{\mathrm{v_n}}(f)$ decreases while keeping all the other parameters constant, underlining the importance of employing a good resonator to realize an oscillator.

To proceed with our analysis we have to consider that $S_{\mathrm{v_n}}(f)$ introduces both amplitude noise and PN, however we have seen that the amplitude of oscillation $\hat{V}_{\mathrm{LO}}$ has a self-limiting effect and eventually reaches a steady state value. This leads us to consider that only half of $S_{\mathrm{v_n}}(f)$ contributes to PN. Referencing the previous notation we therefore have that $\Phi_{\mathrm{n}}(f) = S_{\mathrm{v_n}}(f)/2$. We can then derive the expression of PN as seen in Section 1.5. By normalizing $S_{\mathrm{v_n}}(f)/2$ to the mean square carrier voltage $P_{\mathrm{LO}} = \hat{V}_{\mathrm{LO}}^2/2$ and report the ratio in decibels, obtaining the normalized single-sideband noise spectral density, which is what we call PN and is expressed in $\mathrm{dBc/Hz}$:

$$\begin{aligned}\mathcal{L}(\Delta\omega) =& 10log_{10}\left[\frac{4k_{\mathrm{B}}TR_{\mathrm{T}}}{2}\cdot\frac{1}{P_{\mathrm{LO}}}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] = 10log_{10}\left[\frac{4k_{\mathrm{B}}TR_{\mathrm{T}}}{\hat{V}_{\mathrm{LO}}^2}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \\ =& 10log_{10}\left[\frac{k_{\mathrm{B}}T}{\hat{V}_{\mathrm{LO}}^2}\cdot\frac{R_{\mathrm{T}}}{Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right]\end{aligned} \tag{1.27}$$

From this expression we immediately notice how PN improves as both P_{LO} and Q increase. This result is consistent with what we expect, increasing P_{LO} improves PN because the thermal noise is fixed, while increasing Q improves PN quadratically because the tank's impedance falls off as $1/(Q\Delta\omega)$.

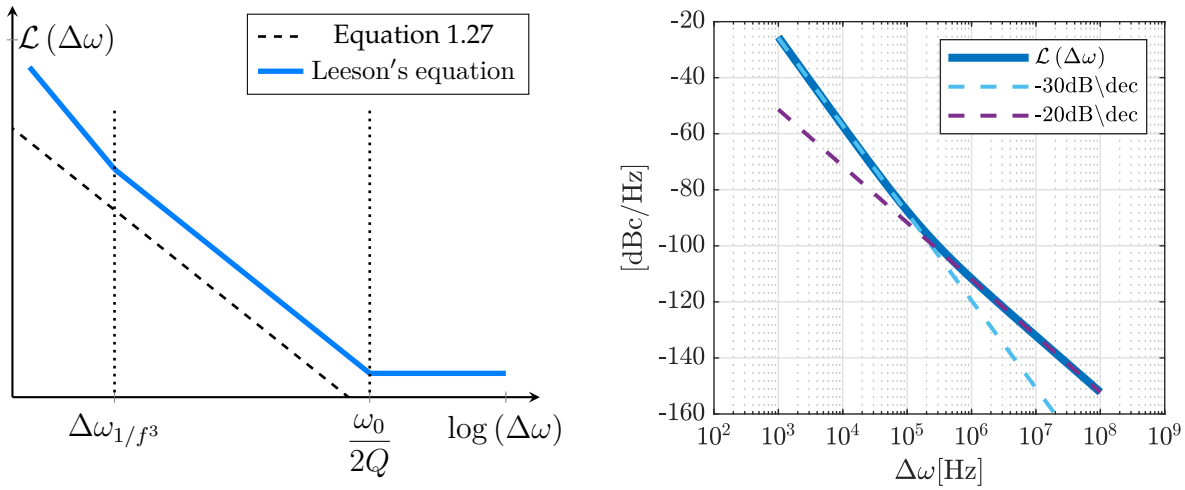
However due to the many simplifying assumptions that we have made in order to obtain Equation 1.27, the accuracy of the formula that we have found, unsurprisingly, shows some discrepancies when compared with a real oscillator spectra.

First, while in real spectra there exist a region where the spectral density is proportional to $1/(\Delta\omega)^2$ the magnitudes are typically quite a bit larger than predicted. This is because there are additional noise sources besides the tank's losses, such as the transistors that realize the cross coupled pair, which contribute to PN. Moreover a real measured spectra eventually stops decreasing as it flattens out hitting what it's called a "noise floor". Finally there is almost always a $1/(\Delta\omega)^3$ region for small values of $\Delta\omega$. This region is given by another noise source, that we have neglected until now, called "flicker noise". Contrary to thermal noise which has its PSD constant over the entire frequency range, the PSD of flicker noise is such that $S_{\mathrm{i,flicker}} \propto^{-1} \omega$. Therefore since noise gets "multiplied" by a factor $1/f^2$ when becoming phase noise, flicker noise originates a $1/f^3$ region in the phase noise.

In order to take into account these effects we have to modify Equation 1.27 obtaining what is generally referred to as "Leeson's equation":

$$\mathcal{L}(\Delta\omega) = 10log_{10}\left[\frac{2Fk_{\mathrm{B}}T}{P_{\mathrm{LO}}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left\{1+\frac{\Delta\omega_{1/\mathrm{f}^3}}{|\Delta\omega|}\right\}\right] \tag{1.28}$$

The modification of Equation 1.27 made by Leeson, consist in the addition of a factor F to account for the increased noise in the $1/(\Delta\omega)^2$ region, an addictive factor of 1 (inside the braces) to model the noise floor and finally a multiplicative factor (inside the second set of braces) to provide a $1/(\Delta\omega)^3$ behaviour at small offset frequencies. In Figure 1.15a we plot the PN given by Equation 1.28 and compare it with the model given by Equation 1.27, while in Figure 1.15b the phase noise of a simulated Class-B oscillator is shown, as an example, to better understand the phase noise behaviour in the $1/f^3$ region.



(a) Comparison of Leeson's equation with simplified model

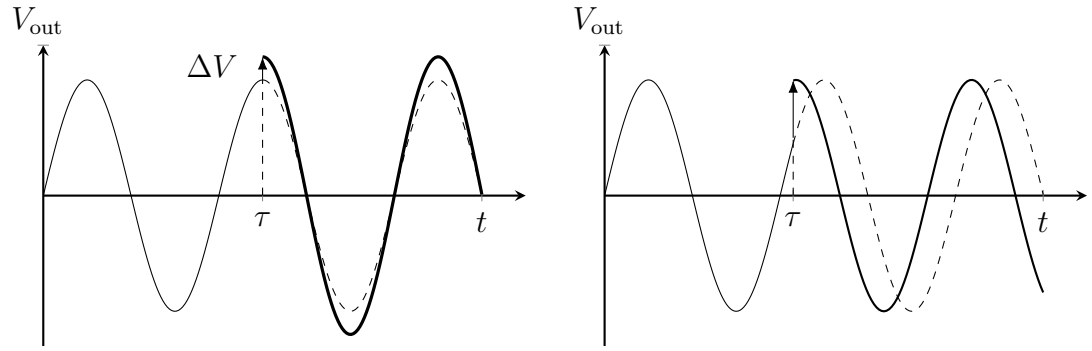
(b) Phase noise of a simulated Class-B oscillator

Figure 1.15: Phase noise behaviour of a real oscillator

We note however how the parameter F is an empirical fitting parameter and the same could be said for $1/(\Delta\omega)^3$ meaning that they must be obtained from measurements, diminishing the predictive power of Equation 1.28. The model also predicts that the frequency at which the $1/f^2$ and $1/f^3$ regions in the phase noise meet, called the "$1/f^3$ corner frequency", is the same at which the thermal and flicker noise PSD are equal, which is respectively called the "$1/f$ corner frequency" This behaviour however is generally hardly observed in practical measurements. The frequency at which the noise floor should start is also not always well predicted by the model. In order to solve these issues a new model has to been developed and it's going to be explained in the next subsection.

1.5.2 Phase Noise in Oscillators - LTV Approach

To improve upon the evident limits of the Leeson model, Hajmiri and Lee [8] formulated a new theory regarding phase noise by modelling the oscillator as a Linear Time Variant (LTV) system. In order to show that an oscillator is indeed a time variant system we take, as an example, the same ideal LC tank of Figure 1.3a, which has been oscillating with a constant amplitude just like Figure 1.3b for an indefinite amount of time, given the lack of a resistance R_T that consumes the energy of the tank. If we apply an impulse at different time instants, we are able to see that the system reacts differently based on when the impulse was applied.



(a) Impulse doesn't perturb zero crossing (b) Impulse perturbs the zero crossing

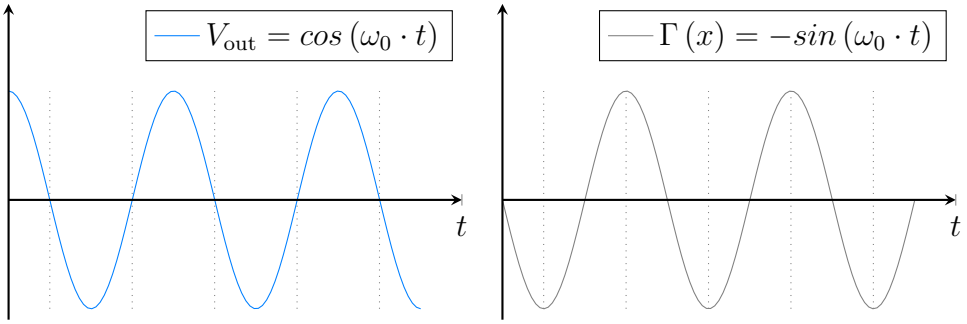
Figure 1.16: Impulse response of a LC tank

With respect to the waveform shown in Figure 1.16a, we consider the case where the time instant, in which the impulse is injected into the oscillator, coincides with a voltage maximum of the oscillator output waveform. This leads to a temporary increase in the oscillation amplitude by an amount ΔV, but because the response to the impulse superimposes exactly in phase with the pre-existing oscillation the timing of the zero crossing does not change. In contrast an impulse injected at some other time as shown in Figure 1.16b generally effects the timing of the zero crossing. Since, as already discussed, we can consider the timing of the zero crossing as a measure of phase, we clearly see that the effect of the impulse changes based on when the injection occurs in time. The principle of time-invariance for oscillators therefore fails to hold and we have to treat them as LTV systems.

The impulse response of the oscillator, going forward, has to be formulated in its LTV form, which is given by:

$$h_{\phi}\left(t,\tau\right)=\frac{\Gamma\left(\omega_{0}\tau\right)}{q_{\max}}u\left(t-\tau\right) \tag{1.29}$$

where $u\left(t\right)$ is the unit step function. The function $\Gamma\left(x\right)$ is normalized by $q_{\max}$ which corresponds to the maximum charge displacement in the capacitors. $\Gamma\left(x\right)$ is called the Impulse Sensitivity Function (ISF), which is a dimensionless, frequency and amplitude independent function periodic in 2π. The ISF encodes information about the sensitivity of the oscillator to an impulse injected at phase $\omega_{0}t$. An example of the ISF for a LC harmonic oscillator is shown in Figure 1.17 where we can appreciate how $\Gamma\left(x\right)=0$ for the time instants where V_{out} is at its maximum, meaning that no phase perturbation can be applied to the system, which is consistent with the example of Figure 1.16.



(a) LC oscillator output waveform (b) LC oscillator ISF

Figure 1.17: Comparison between ISF and output waveform of an oscillator

While its most practical to determine the ISF through simulation, there are also analytical methods that apply in certain scenarios. In any case once the ISF has been determined, we can compute the excess phase due to an arbitrary noise signal, through use of the superposition integral, as follows:

$$\phi\,(t) = \int_{-\infty}^{\infty} h_\phi\,(t,\tau)\,i\,(\tau)\;d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma\,(\omega_0\tau)\,i\,(\tau)\;d\tau \tag{1.30}$$

where ϕ is the phase noise term seen in Equation 1.18. We can rewrite Equation 1.30, by rewriting the ISF as its Fourier series:

$$\Gamma\,(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_{\text{n}} cos\,(n\omega_0\tau + \theta_{\text{n}}) \tag{1.31}$$

where the c_{n} coefficients are real and θ_{n} is the phase of the n-th harmonic of the ISF. Note however that we assume the noise components as uncorrelated so their relative phase θ_{n} in irrelevant. Putting Equation 1.30 and Equation 1.31 together we get:

$$\phi\,(t) = \frac{1}{q_{\text{maz}}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i\,(\tau)\;d\tau + \sum_{n=1}^{\infty} c_{\text{n}} \int_{-\infty}^{t} i\,(\tau)\,cos\,(n\omega_0\tau)\;d\tau \right] \tag{1.32}$$

The physical meaning of Equation 1.32 can be understood by considering to inject in the system a sinusoidal current whose frequency is near an integer multiple m of the oscillation frequency, being:

$$i\,(t) = I_{\text{m}} cos\,[(m\omega_0 + \Delta\omega)\,t] \tag{1.33}$$

Assuming $\Delta\omega \ll \omega_0$, we can then plug Equation 1.33 into Equation 1.32 and obtain Equation 1.35.

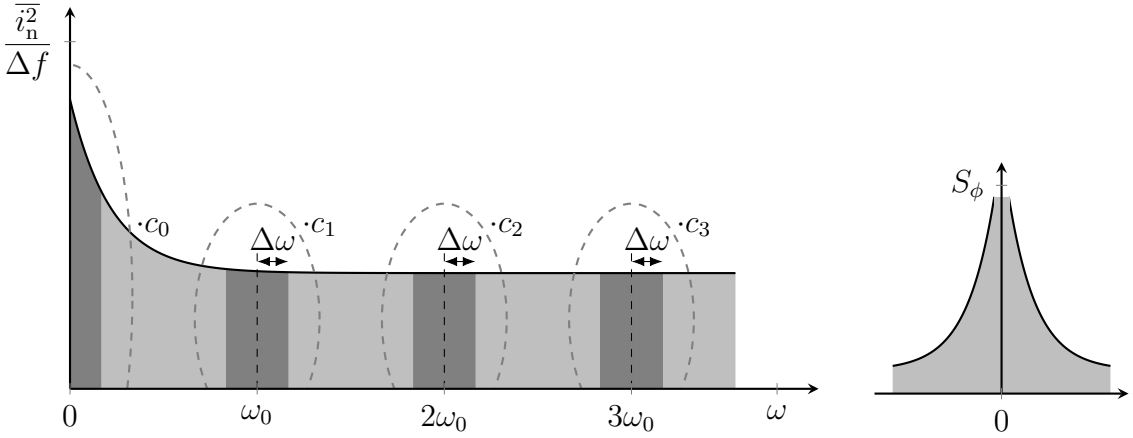
$$\phi(t) = \frac{1}{q_{\max}} \left[\begin{array}{l} \frac{c_0}{2} \int_{-\infty}^{t} I_{\mathrm{m}} cos\left[(m\omega_0 + \Delta\omega)\,\tau \right]\, d\tau \\ \quad + \sum_{n=1}^{\infty} c_{\mathrm{n}} \int_{-\infty}^{t} I_{\mathrm{m}} cos\left[(m\omega_0 + \Delta\omega)\,\tau \right] cos\left(n\omega_0 \tau \right)\, d\tau \end{array} \right] \tag{1.34}$$

$$\phi(t) = \frac{1}{q_{\max}} \left[\begin{array}{l} \frac{c_0}{2} \int_{-\infty}^{t} I_{\mathrm{m}} cos\left[(m\omega_0 + \Delta\omega)\,\tau \right]\, d\tau \\ \quad + \sum_{n=1}^{\infty} \frac{c_{\mathrm{n}}}{2} \int_{-\infty}^{t} I_{\mathrm{m}} cos\left[((n-m)\,\omega_0 + \Delta\omega)\,\tau \right]\, d\tau \\ \quad + \sum_{n=1}^{\infty} \frac{c_{\mathrm{n}}}{2} \int_{-\infty}^{t} I_{\mathrm{m}} cos\left[((n+m)\,\omega_0 + \Delta\omega)\,\tau \right]\, d\tau \end{array} \right] \tag{1.35}$$

The only term of Equation 1.35 that provides a non negligible contribution is the one associate with $n = m$, therefore we can get the approximation:

$$\phi(t) \simeq \frac{I_{\mathrm{m}} c_{\mathrm{m}} sin\left(\Delta\omega t\right)}{2 q_{\max} \Delta\omega} \tag{1.36}$$

In a more general case however the spectrum of the noise is not given by a single sinusoidal tone, but it's a continuous spectra. Therefore what happens in reality is that $\phi(t)$ is given by the summation of all the noise contributions located at distance $\Delta\omega$ from the multiples of the oscillation frequency ω_0. Note that the $1/f$ noise near DC gets upconverted, with relative weight given by the coefficient c_0, into $1/f^3$ noise, while white noise near the higher carrier multiples, weighted by the coefficients $c_{\mathrm{k}\neq 0}$, undergoes downconversion turning into $1/f^2$ noise. This process is shown in Figure 1.18 where the weighted noise contributions shown in Figure 1.18a all sum up following Equation 1.36 into $\phi(t)$ which is shown in Figure 1.18b. Finally the summation of the various noise contributions all "fold" into noise near the carrier itself, following Equation 1.22.



(a) Noise contributions to phase noise

(b) Summation of noise contributions

Figure 1.18: Noise folding principle

Following these reasonings, in order to calculate the phase noise we start by considering that the value of $\phi(t)$, that we have calculated in Equation 1.36, translates following the mechanism of Equation 1.21 into two tones of the output spectrum of the oscillator symmetrically disposed from the carrier at distance $\Delta\omega$ having power:

$$P_{\mathrm{SBC}}(\Delta\omega) \simeq 10log\left[\frac{I_{\mathrm{k}}c_{\mathrm{k}}}{4q_{\max}\Delta\omega}\right]^2 \tag{1.37}$$

Extending this formula for the case of a white source noise we get:

$$P_{\mathrm{SBC}}(\Delta\omega) \simeq 10log\left[\frac{1}{4q_{\max}^2\Delta\omega^2}\cdot\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f}\cdot\sum_{k=0}^{\infty}c_{\mathrm{k}}^2\right] \tag{1.38}$$

which can used to derive the general expression of phase noise in the $1/f^2$ region:

$$\mathcal{L}(\Delta\omega) \simeq 10log\left[\frac{1}{2q_{\max}^2\Delta\omega^2}\cdot\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f}\cdot\Gamma_{rms}^2\right] \tag{1.39}$$

where Parseval's Theorem has been used to rewrite $\sum_{k=0}^{\infty}c_{\mathrm{k}}^2 = 2\Gamma_{rms}^2$.
Finally by considering the ISF of a LC oscillator being $\Gamma(x) = -sin(x)$, that $q_{\max} = C_{\mathrm{T}}\hat{V}_{\mathrm{LO}}$ with $C_{\mathrm{T}} = Q_{\mathrm{T}}/(\omega_0 R_{\mathrm{T}})$ and using Equation 1.23 we get:

$$\mathcal{L}(\Delta\omega) \simeq 10log\left[\frac{1}{2q_{\max}^2\Delta\omega^2}\cdot\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f}\cdot\Gamma_{rms}^2\right] \tag{1.40}$$

$$= 10log\left[\frac{1}{2C_{\mathrm{T}}^2\hat{V}_{\mathrm{LO}}^2\Delta\omega^2}\cdot\frac{4k_{\mathrm{B}}T}{R_{\mathrm{T}}}\cdot\frac{1}{2}\right] \tag{1.41}$$

$$= 10log\left[\frac{1}{2\hat{V}_{\mathrm{LO}}^2\Delta\omega^2}\cdot\frac{\omega_0^2R_{\mathrm{T}}^2}{Q_{\mathrm{T}}^2}\cdot\frac{4k_{\mathrm{B}}T}{R_{\mathrm{T}}}\cdot\frac{1}{2}\right] \tag{1.42}$$

$$= 10log\left[\frac{k_{\mathrm{B}}T}{\hat{V}_{\mathrm{LO}}^2}\cdot\frac{R_{\mathrm{T}}}{Q_{\mathrm{T}}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{1.43}$$

which gives us back Equation 1.27. Moreover the "$1/f^3$ corner frequency" can be estimated using:

$$\Delta\omega_{1/f^3} = \omega_{1/f}\cdot\frac{c_0^2}{4\Gamma_{\mathrm{rms}}^2} = \omega_{1/\mathrm{f}}\cdot\left(\frac{\Gamma_{\mathrm{dc}}}{\Gamma_{\mathrm{rms}}}\right)^2 \tag{1.44}$$

where the term $\omega_{1/\mathrm{f}}$ is the "$1/f$ corner frequency". While in this thesis we are not interested in operation near the $1/f^3$ corner frequency this once again proves the power of the LTV phase noise model.

1.5.3 The Figure of Merit

Looking at the formula for phase noise derived in Equation 1.43 we notice how:

$$\mathcal{L}\left(\Delta\omega\right) \propto \left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{1.45}$$

Moreover we have that:

$$\mathcal{L}\left(\Delta\omega\right) \propto^{-1} \hat{V}_{\mathrm{LO}}^2 \propto I_{\mathrm{bias}}^2 \tag{1.46}$$

when we assume operation in the current limited regime. In order to compare different oscillator topologies, working at different oscillation frequencies and absorbing a different amount of power the Figure of Merit (FoM) is used and its defined as:

$$FOM = \mathcal{L}\left(\Delta\omega\right) - 20log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) + 10log_{10}\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) \ \ \mathrm{dBc/Hz} \tag{1.47}$$

where P_{DC} is the DC power consumption of the oscillator.

1.5.4 Effects of Phase Noise

We wish now to investigate what effects PN has on the correct operation of electronic circuits that include a noisy oscillator.

Phase Noise in Receivers

One effect of low phase noise can be observed in a receiver, where its equivalent scheme is shown in Figure 1.19.

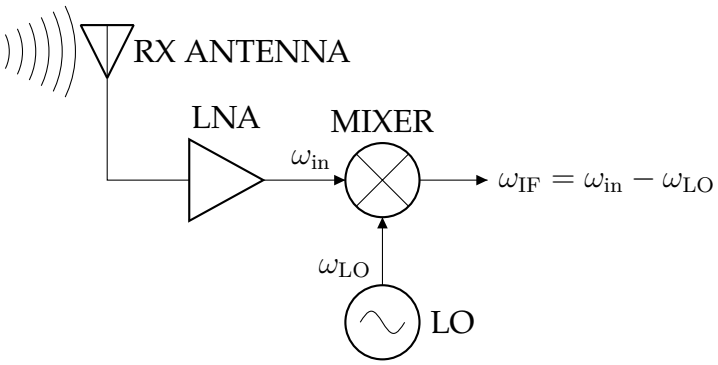


Figure 1.19: Receiver scheme

In the ideal case the signal produced by the LO is an impulse at ω_{LO} which when convolved through the mixer with the desired channel at ω_{in} yields an Intermediate Frequency (IF) signal at $\omega_{\mathrm{IF}} = \omega_{\mathrm{in}} - \omega_{\mathrm{LO}}$ as shown in Figure 1.20.

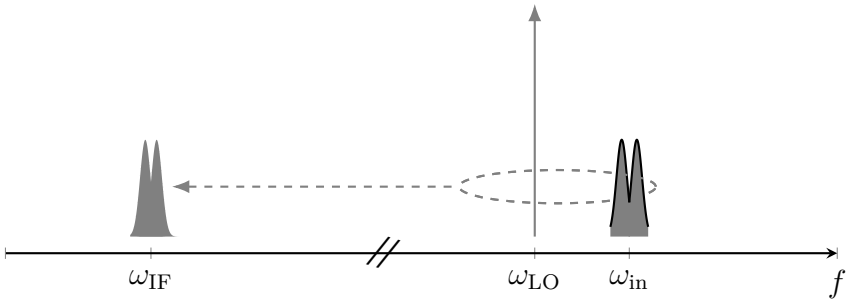


Figure 1.20: Downconversion with an ideal LO

However if a noisy LO is used and the desired signal is accompanied by a large interferer at ω_{int}. The convolution of the desired signal and the interferer with the noisy LO spectrum results in a broadened downconverted interferer which overwhelms the desired IF signal corrupting it, as shown in Figure 1.21. This phenomenon is called "reciprocal mixing".

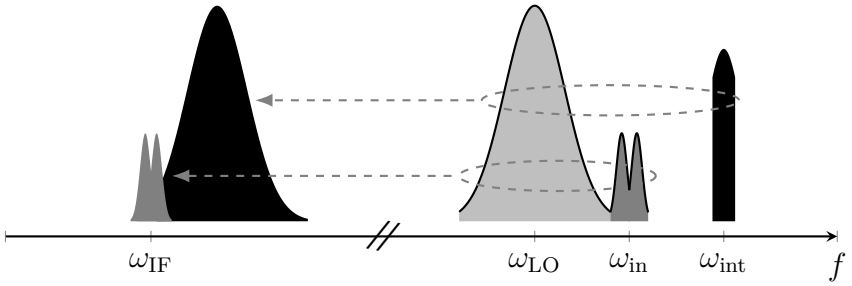


Figure 1.21: Downconversion with a noisy LO

Phase Noise in Digital Modulation

There is however another more important effect that involves telecommunications systems employing digital modulations such as Phase Shift Keying (PSK), which in order to be understood requires a brief theoretical introduction regarding the problem of transmitting information and being able to correctly receive it.

Without loss of generality then we consider the problem of the transmission of a single isolated pulse associated to a symbol a_0.

With reference to the system scheme shown in Figure 1.22 the transmission system aims to transfer the value of a_0 to the receiver through the channel.

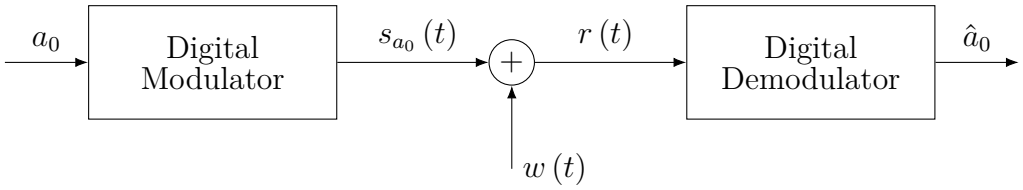


Figure 1.22: System model for digital transmission of an isolated pulse

In particular the digital modulator, defined by a given set of M real-valued waveforms $s_{\mathrm{n}}(t), n = 1, ..., M$, selects the waveform to transmit in accordance with the value of a_0. This means that if the selected symbol value is $a_0 = n$, then the transmitted signal is $s_{a0}(t) = s_{\mathrm{n}}(t)$. The selected signal $s_n(t)$ is then transmitted through the channel, which for simplicity is assumed to have an ideal impulse response. Assuming that the waveform with index n is transmitted, which represents the symbol $a_0 = n$, the received, or observed, signal is given by:

$$r(t) = s_{\mathrm{n}}(t) + w(t) \tag{1.48}$$

where $w(t)$ models the noise introduced by the channel.

The receiver now, based on $r(t)$, must decide which among the M hypothesis

$$H_{\mathrm{n}} : r(t) = s_{\mathrm{n}}(t) + w(t), \qquad n = 1, 2, ..., M \tag{1.49}$$

is the most likely, and correspondingly must select the detected value $\hat{a}_0$.

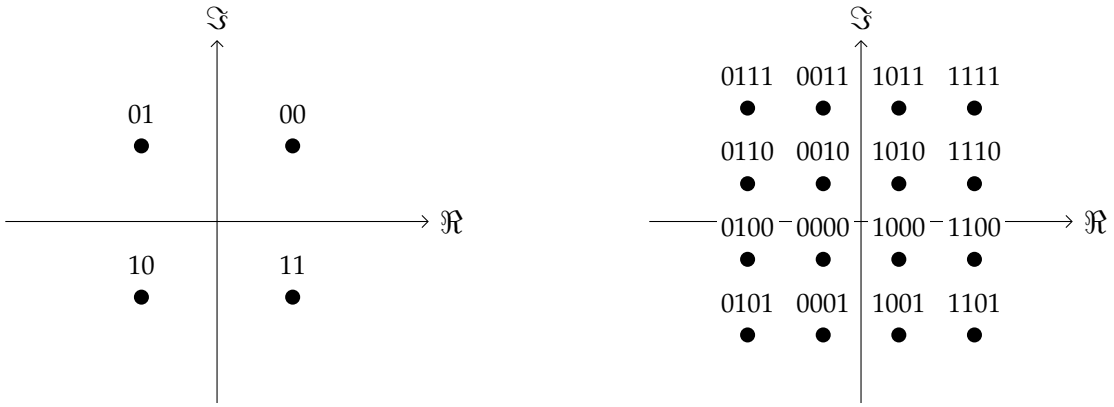
In order to proceed, it is convenient to represent the signals using vector notation. The received signal $r(t)$ is therefore associated to a vector r of dimension I. Symbol detection is made by subdividing the space $\mathbb{R}^I$ into M non overlapping regions R_{n} each one associated to one of the possible outcomes of a_0. The hypothesis H_{m} (and so $\hat{a}_0 = n$) is chosen if the received vector belongs to R_{m}, that is:

$$if\ r \in R_{\mathrm{m}}\ then\ choose\ H_{\mathrm{m}}\ and\ \hat{a}_0 = m \tag{1.50}$$

This decision rule is realized by a block called "detector" which is part of the digital demodulator.

It is clear that the presence of a noise component $w(t)$ could lead to errors in detection if the noise is so high that it moves a symbol $a_0 = n$ associated to the region R_{n} to another region R_{k} with $k \neq n$.

An example of a decision region for a Quadrature Amplitude Modulation (QAM) with $M = 4$ and $M = 16$ is shown in Figure 1.23. As can be appreciated, the detection of the symbol region in the $M = 4$ case can be implemented by checking the sign of the coordinates of r, while for the $M = 16$ case extra information regarding the modulus of the received vector is needed.



(a) 4-QAM Constellation

(b) 16-QAM Constellation

Figure 1.23: Examples of QAM constellations

We can now focus our attention on the PSK modulation in order to understand how also PN can lead to errors in symbol detection. We have that in PSK a generic signal waveform is given by:

$$s_{\mathrm{n}}(t) = h_{\mathrm{tx}}(t)\, cos\,(2\pi f_0 + \varphi_{\mathrm{n}}) \tag{1.51}$$

$$\varphi_{\mathrm{n}} = \frac{\pi}{M}(2n-1) + \varphi_0 \qquad n = 1, 2, ..., M \tag{1.52}$$

where $h_{\mathrm{tx}}(t)$ is a real-valued finite-energy baseband pulse. This means that signals are obtained by choosing M possible values of the phase of a sinusoidal signal with frequency f_0 modulated by h_{tx}.
An alternative way to write $s_{\mathrm{n}}(t)$ is given by:

$$s_{\mathrm{n}}(t) = cos\,(\varphi_{\mathrm{n}})\, h_{\mathrm{tx}}(t) cos\,(2\pi f_0) - sin\,(\varphi_{\mathrm{n}})\, h_{\mathrm{tx}}(t) sin\,(2\pi f_0) \tag{1.53}$$

It can be easily proved that $s_{\mathrm{n}}(t)$ can be written as the linear combination of the following two vectors:

$$\phi_1(t) = +\sqrt{\frac{2}{E_{\mathrm{h}}}} h_{\mathrm{tx}}(t) cos(2\pi f_0) \tag{1.54}$$

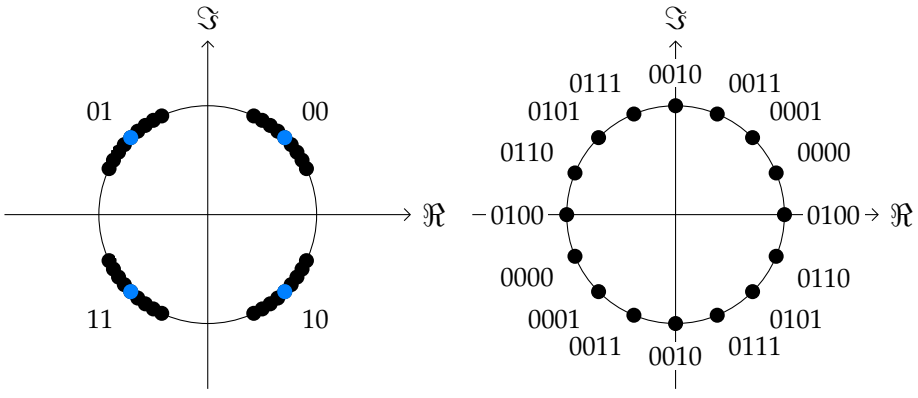
$$\phi_2(t) = -\sqrt{\frac{2}{E_{\mathrm{h}}}} h_{\mathrm{tx}}(t) sin(2\pi f_0) \tag{1.55}$$

which, with E_{h} the energy of $h_{\mathrm{tx}}(t)$, constitute an orthonormal basis for $I = 2$.
The vector coordinates of $s_{\mathrm{n}}(t)$ are finally given by:

$$s_{\mathrm{n}} = \sqrt{\frac{2}{E_{\mathrm{h}}}} \left[cos(\varphi_{\mathrm{n}}), sin(\varphi_{\mathrm{n}})\right] \tag{1.56}$$

To obtain the vector coordinates in Equation 1.56 an oscillator provides a reference sinusoidal signal $x(t)$ of frequency f_0 plus a cosinusoidal signal realized by phase shifting by $90°$ the original signal $x(t)$. In this way we are capable of realizing the basis of Equation 1.54 and Equation 1.55 and obtain s_{n}. However due to the oscillator PN, the coordinates of s_{n} are going to be affected by the noise.

Figure 1.24a show the decision region for a PSK modulation with $M = 4$ where PN is present, causing a "drift" of the received symbols along the constellation circumference. Therefore as PN increases, it's easy to see how it can lead to errors in detection by pushing the received symbols in the wrong region. This problem becomes even bigger if we increase the value of M, in order to be able to transmit more data, as shown in Figure 1.24b. This is the reason why over the years specification on PN have become more stringent to accommodate for modulations employing higher values of M. [2]



(a) Constellation of a noisy 4-PSK (b) Constellation of a 16-PSK

Figure 1.24: Examples of PSK constellations

1.6 Frequency Pushing

Thus far we have assumed, for simplicity, the value of the supply voltage to be constant. In practical implementations however the power supply will contain noise and, in some cases, even sinusoidal contributions at certain frequencies. The oscillating frequency of the oscillator is generally dependent from the value of the power supply, meaning that small changes in the value of V_{DD} will modulate the value of ω_0 changing it too. This behaviour is called "frequency pushing" and it can be quantified by the "supply pushing factor" K_{V}, which is specific for each different type of oscillator. K_{V} is normally measured in $\mathrm{Hz/V}$, meaning that a variation of ΔV on the power supply corresponds to a variation of the output frequency of $\Delta\omega = 2\pi K_V \cdot \Delta V$.

Sinusoidal ripple, present in the power supply, gets translated to spurious tones in the output spectrum of the oscillator, due to supply pushing. In order to prove this, we consider that the frequency modulation given by a ripple $\Delta V_{\mathrm{m}} = V_{\mathrm{m}} cos\left(\omega_{\mathrm{m}} t\right)$ will be:

$$\Delta\omega = 2\pi K_{\mathrm{V}} \cdot V_{\mathrm{m}} cos(\omega_{\mathrm{m}} t) \tag{1.57}$$

Then since phase is the integral of the angular frequency we get;

$$\phi\left(t\right) = \phi\left(0\right) + \int_0^t \omega\left(\tau\right)\, d\tau \tag{1.58}$$

$$\phi\left(t\right) = \frac{2\pi K_{\mathrm{V}}}{\omega_{\mathrm{m}}} V_{\mathrm{m}} sin\left(\omega_{\mathrm{m}} t\right) \tag{1.59}$$

where we have assumed $\phi\left(0\right) = 0$.
By plugging Equation 1.59 into the usual Equation 1.21 we obtain the formula:

$$x\left(t\right) \simeq Acos\left(\omega_0 t\right) - Asin\left(\omega_0 t\right) \left(\frac{2\pi K_{\mathrm{V}}}{\omega_{\mathrm{m}}}\right) V_{\mathrm{m}} sin\left(\omega_{\mathrm{m}} t\right) \tag{1.60}$$

By computing the Fourier transform of the second term for $\omega > 0$ we get:

$$X_{\mathrm{n}}\left(\omega\right) = \frac{A}{4} \left(\frac{2\pi K_{\mathrm{V}}}{\omega_{\mathrm{m}}}\right) V_{\mathrm{m}} \left[\delta\left(\omega_0 + \omega_{\mathrm{m}}\right) + \delta\left(\omega_0 - \omega_{\mathrm{m}}\right)\right] \tag{1.61}$$

Which shows how as a result of frequency pushing two spurs at frequencies $\omega_0 \pm \omega_{\mathrm{m}}$ make an appearance in the output spectrum of the oscillator. These spurs have to kept under a certain level with respect to the carrier to avoid reciprocal mixing.

A spectrum example is shown in Figure 1.25:

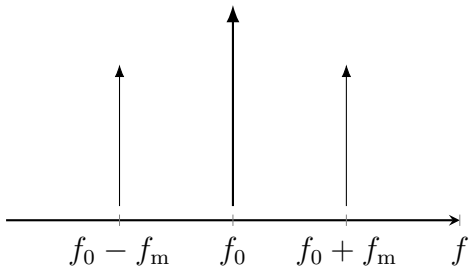


Figure 1.25: Output spectrum of an oscillator with ripple on the power supply

The power of the spurs represented in dBc is given as:

$$S_{\mathrm{spur}} = 10log_{10}\left(\frac{2\pi K_{\mathrm{V}} V_{\mathrm{m}}}{2\omega_{\mathrm{m}}}\right)^2 \mathrm{dBc} \tag{1.62}$$

Given the desired spur level the maximum ripple tolerated by the oscillator can be calculated by:

$$V_{\mathrm{m}} < \frac{2\omega_{\mathrm{m}}}{2\pi K_{\mathrm{V}}} 10^{(S_{\mathrm{spur}}/20)} \tag{1.63}$$

which is going to be one of the most critical specifications in the design of the SC converter of Chapter 3. We note in fact that K_{V} for Class-D oscillator can be as high as $600\mathrm{MHz/V}$ [4].

As a result of frequency pushing, noise present in the supply voltage gets also picked up by the oscillator, and randomly modulates the oscillation frequency, through the same mechanism explained before. This leads to the conversion of noise in the power supply into phase noise. We can quantify how much supply noise gets converted into phase noise by looking at the following formula:

$$\mathcal{L}_{\mathrm{supply}}(\Delta\omega) = 10log_{10}\left(\frac{(2\pi K_{\mathrm{V}})^2}{\Delta\omega^2} V^2_{\mathrm{n,supply}}(\Delta\omega)\right) \tag{1.64}$$

where $V^2_{\mathrm{n,supply}}$ is the power spectral density of the supply noise. To preserve the inherit phase noise of the oscillator we have to satisfy the condition:

$$\mathcal{L}_{\mathrm{supply}}(\Delta\omega) \ll \mathcal{L}(\Delta\omega) \tag{1.65}$$

This leads to:

$$V_{\mathrm{n,supply}}^2 < \frac{10^{\frac{-FOM}{10}}}{10^3 \mathrm{P_{DC}}} \left(\frac{\omega_{osc}}{2\pi K_{\mathrm{V}}} \right)^2 \tag{1.66}$$

which tells us the maximum value that the supply noise can assume, before deteriorating the phase noise of the oscillator. Note that even though Equation 1.66 seems to suggest that by increasing the frequency of the oscillation ω_0 the oscillator is able to tolerate more supply noise, we have to consider that K_{v} is also weakly dependent from frequency. This effect is due to how the capacitance of the tank is realized. C_{TOT} is generally composed of a fixed capacitor C_{fix}, a variable capacitor C_{tune} needed to tune the oscillation frequency, as we will see in Section 2.2, and the parasitic capacitances C_{par} of the switches. The expression for C_{TOT} is therefore the following:

$$C_{\mathrm{TOT}} = C_{\mathrm{fix}} + C_{\mathrm{tune}} + C_{\mathrm{par}} \tag{1.67}$$

The effective value C_{par} however can be modulated by the supply voltage, contributing to K_{V}. In order to increase ω_0, following Equation 1.10, we have to decrease C_{tune}. This in turn makes C_{par}, in proportion, a bigger component of C_{TOT} leading to an increase in K_{V}. As a result the ratio $\omega_0 / (2\pi K_{\mathrm{V}})$ remains almost constant across the operating frequency range.

CHAPTER 2

Class-D Oscillators

In this chapter an analysis of the Class-D oscillator and its advantages over other oscillator topologies is presented. An analysis on the time-variant nature of the Class-D tank is made, in order to outline how critical design parameters such as oscillation frequency, current consumption and even phase noise are influenced by the nature of the Class-D tank. This analysis is naturally instrumental in order to understand how to approach the design of Class-D VCOs which is also touched upon in this chapter.

2.1 Topology Overview

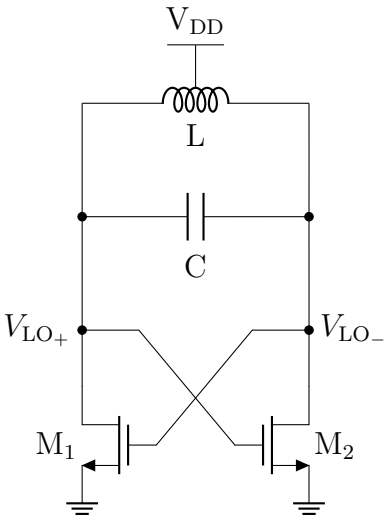


Figure 2.1: Class-D oscillator scheme

By removing the tail generator from a Class-B oscillator we push, as anticipated, the oscillator in its voltage limited region obtaining the topology of a Class-D oscillator, shown in Figure 2.1.

Additionally it has to be noted that to guarantee good Class-D operation, switches M_1 and M_2 have to be sized so that their equivalent resistance is negligible with respect to the tank equivalent resistance.

One of Class-D main characteristics is that it oscillates at an amplitude of $\hat{V}_{\mathrm{LO,ClassD}} \simeq 3V_{\mathrm{DD}}$. This makes the Class-D oscillator incredibly attractive for operation at low V_{DD} since it is able to guarantee an excellent level of phase noise even when the supply voltage is limited. We have in fact seen in Equation 1.43 how the phase noise is dependent on the oscillation amplitude $\hat{V}_{LO}$ and compared to a Class-B Oscillator that, as we have seen in in Section 1.4.1, reaches a maximum value of $\hat{V}_{\mathrm{LO,ClassB}} = V_{\mathrm{DD}} - V_{\mathrm{S}}$, it's easy to see why the Class-D topology excels for very low power supply applications.

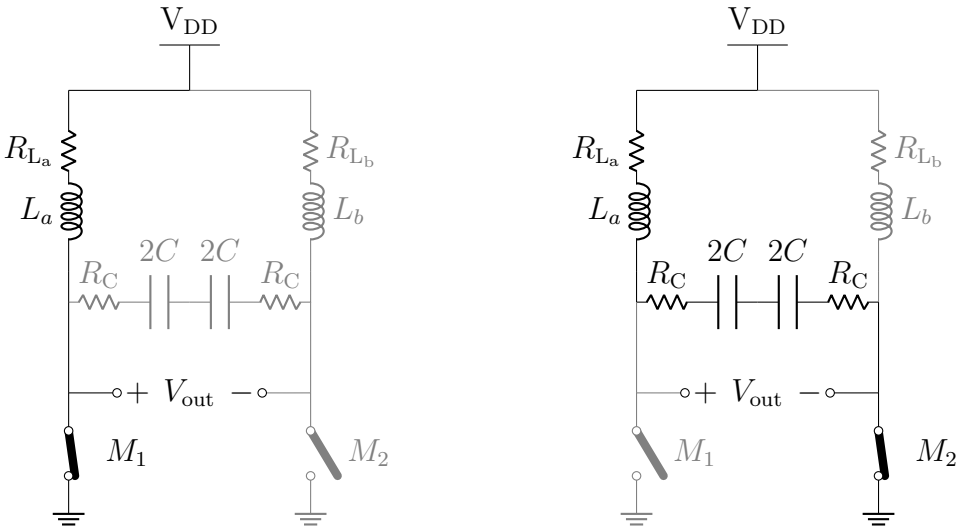
On the other hand, even though the Class-D oscillator is capable of producing less phase noise than a Class-B Oscillator, for the same power consumption, this comes at the cost of a higher power supply pushing which can be as high as $600\mathrm{MHz/V}$ and needs to be kept in high consideration during the design process.

The key difference between Class-D and Class-B oscillators, besides the tail generator, is that the Class-D LC tank displays a time-variant nature, meaning that the properties of the tank change during the oscillation period. Not only that, but the behaviour of the Class-D oscillator changes based on the nature of the tank capacitance: floating or single-ended. In reality, since the tank can't be purely floating or single-ended, the behaviour of the oscillator is going to be confined between two different working extremes. In the following sections we are going to show the expressions of the behaviour of a Class-D oscillator, based on these particular properties, as showed in [4].

2.1.1 Oscillation Frequency

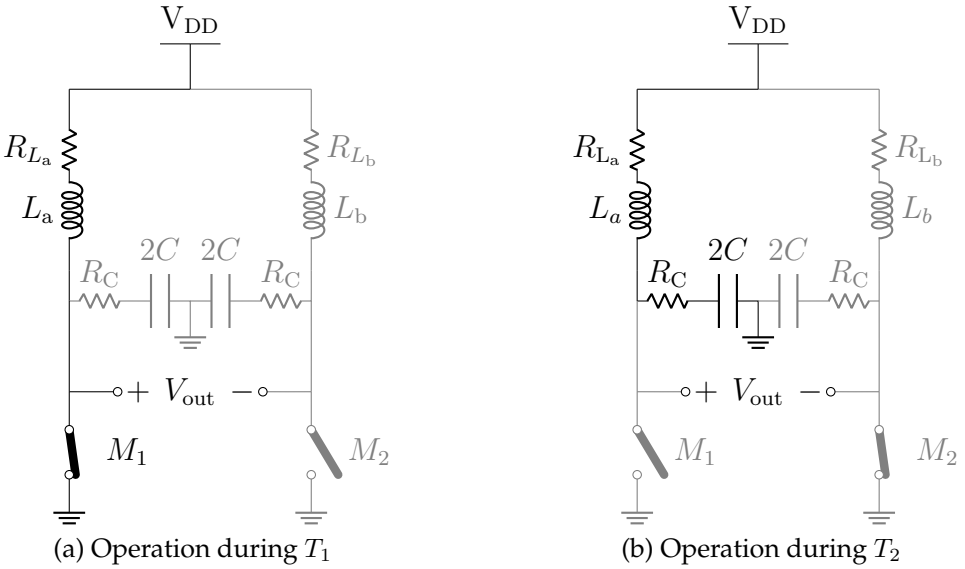
As anticipated, due to the time-variant nature of the tank, the Class-D oscillator changes its properties based on the nature of the capacitance present in the tank. The aforementioned property extends even to its oscillation frequency which has the peculiarity of varying between two extremes $\omega_{0,\mathrm{float}}$ for a completely floating tank capacitance and $\omega_{0,\mathrm{se}}$ for a completely single-ended tank capacitance. This is in sharp contrast with the fixed ω_0 value of Class-B oscillators, as seen in Equation 1.10.

In order to derive expressions for $\omega_{0,\mathrm{se}}$ and $\omega_{0,\mathrm{float}}$ it is necessary to study how the current flowing into the inductor $L_\mathrm{a} = L_\mathrm{b} = L/2$ evolves during an oscillation period. We take, as a reference, the equivalent scheme of the Class-D oscillator shown in Figure 2.2 for the case where the oscillator is loaded with a floating capacitor and the one showed in Figure 2.3 for when in turn a single-ended capacitor is used.



(a) Operation during T_1 (b) Operation during T_2

Figure 2.2: Equivalent scheme of a Class-D oscillator with floating capacitance



(a) Operation during T_1 (b) Operation during T_2

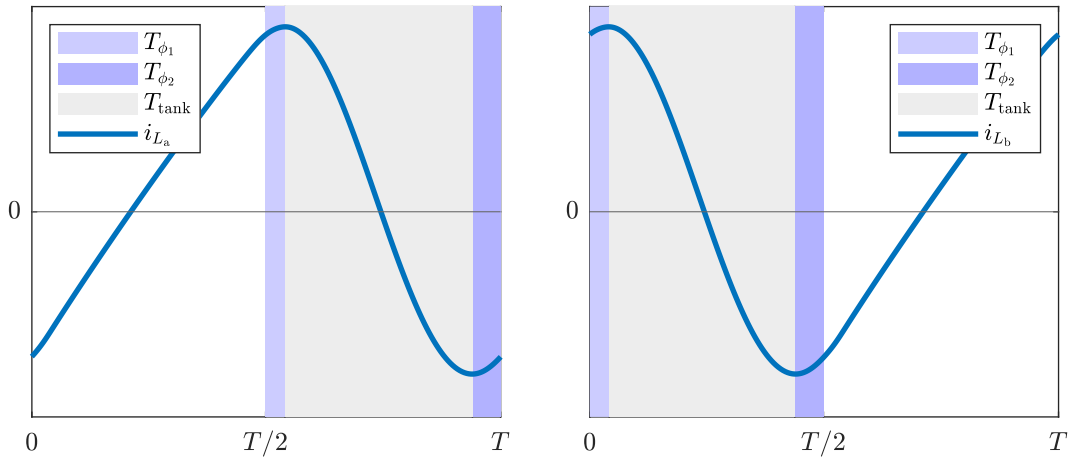
Figure 2.3: Equivalent scheme of a Class-D oscillator with single-ended capacitance

The operation of the oscillator during an oscillation period T_osc is divided into 2 phases. During T_1 (i.e. for $0 < t < T_\mathrm{osc}/2$), M_1 shorts L_a to ground and $i_{\mathrm{L_a}}(t)$ results from the exponential charge of L_a. During T_2 (i.e. for $T_\mathrm{osc}/2 < t < T_\mathrm{osc}$), on the other hand, M_1 is off and L_a resonates with the equivalent tank capacitance C_eq.

In this last case $i_{\mathrm{L_a}}(t)$ is a sinusoidal current wave with oscillation frequency ω_{tank} of:

$$\omega_{\mathrm{tank}} = \sqrt{\frac{1}{L_{\mathrm{a}} C_{\mathrm{eq}}}} \tag{2.1}$$

where $C_{\mathrm{eq}} = C$ in the case of Figure 2.2 and $C_{\mathrm{eq}} = 2C$ in the case of Figure 2.3.
The same behaviour can be observed by looking at the operation of transistor M_2 and the inductor current $i_{L_{\mathrm{b}}}(t)$ since their operation is complementary with respect to M_1 and $i_{L_{\mathrm{a}}}(t)$. In Figure 2.4 the time evolution of $i_{L_{\mathrm{a}}}$ and $i_{L_{\mathrm{b}}}$ is plotted showing this aspect and highlighting the period T_{tank} of ω_{tank}.



(a) Behaviour of current $i_{L_{\mathrm{a}}}(t)$ (b) Behaviour of current $i_{L_{\mathrm{b}}}(t)$

Figure 2.4: Currents on the inductors L_{a} and L_{b}

Note from Figure 2.4 how the oscillation period of T_{tank} is smaller than T_2 so we have to take this into account by writing:

$$T_2 = T_{\phi 1} + \frac{T_{\mathrm{tank}}}{2} + T_{\phi 2} \tag{2.2}$$

During T_1 the expression of $i_{L\mathrm{a}}(t)$ is:

$$i_{L_{\mathrm{a}},T_1}(t) = i_1 + \frac{V_{\mathrm{DD}}}{R_{L_{\mathrm{a}}}}\left(1 - e^{-(R_{L_{\mathrm{a}}}/L_a)t}\right) \tag{2.3}$$

where $i_1 = i_{L_{\mathrm{a}}}(0) = i_{L_{\mathrm{a}}}(T_{\mathrm{osc}})$ and $R_{L_{\mathrm{a}}} = R_{L_{\mathrm{b}}} = R_L/2$ is the series resistance of L_{a}.
The derivative of $i_{L_{\mathrm{a}},T_1}(t)$ is:

$$\dot{i}_{L_{\mathrm{a}},T_1}(t) = \frac{V_{\mathrm{DD}}}{L_{\mathrm{a}}} e^{-(R_{L_{\mathrm{a}}}/L_{\mathrm{a}})t} \tag{2.4}$$

We can then proceed by calculating the values of $i_{L_{\mathrm{a}},T_1}(t)$ and $\dot{i}_{L_{\mathrm{a}},T_1}(t)$ at the transition time $t = T_{\mathrm{osc}}/2$ between T_1 and T_2:

$$i_{L_{\mathrm{a}},T_1}\left(\frac{T_{\mathrm{osc}}}{2}\right) = i_1 + \frac{V_{\mathrm{DD}}}{R_{L_{\mathrm{a}}}}\left(1 - e^{\pi/Q_{L_{\mathrm{a}}}}\right) = i_0 \tag{2.5}$$

$$\dot{i}_{L_{\mathrm{a}},T_1}\left(\frac{T_{\mathrm{osc}}}{2}\right) = \frac{V_{\mathrm{DD}}}{R_{L_{\mathrm{a}}}} e^{-\pi/Q_{L_{\mathrm{a}}}} = i_0' \tag{2.6}$$

where $Q_{L_{\mathrm{a}}} = \omega_{\mathrm{osc}} L_{\mathrm{a}}/R_{L_{\mathrm{a}}}$, with $\omega_{osc} = 2\pi/T_{\mathrm{osc}}$
Assuming the tank losses to be negligible we can rewrite i_0 as:

$$i_0 = i_1 + \frac{V_{DD}}{L_{\mathrm{a}}}\frac{T_{\mathrm{osc}}}{2} \tag{2.7}$$

and the same applies for i_0':

$$i_0' = \frac{V_{DD}}{L_{\mathrm{a}}} \tag{2.8}$$

Moreover, since there are no losses, the current on the inductor L_{a} at time $t = 0$ and $t = T_{\mathrm{osc}}/2$ is the same in modulus, therefore:

$$-i_{L\mathrm{a}}(0) = i_{L\mathrm{a}}(T_{\mathrm{osc}}/2) \tag{2.9}$$

Combing Equation 2.9 and Equation 2.7 we get:

$$-i_1 = i_0 = i_1 + \frac{V_{DD}}{L_{\mathrm{a}}}\frac{T_{\mathrm{osc}}}{2} \tag{2.10}$$

which allow us to immediately write:

$$i_0 = \frac{1}{2}\left(\frac{V_{DD}}{L_{\mathrm{a}}}\frac{T_{\mathrm{osc}}}{2}\right) = \frac{\pi V_{DD}}{2L_{\mathrm{a}}\omega_{\mathrm{osc}}} \tag{2.11}$$

During T_2 we treat, as already mentioned, $i_{L_{\mathrm{a}}}(t)$ as a portion of sinusoid of angular frequency ω_{tank}. This sinewave is however damped by the combined losses of L_{a} and C_{eq}. Knowing the values of $i_{L_{\mathrm{a}}}(t)$ and of $\dot{i}_{L_{\mathrm{a}}}(t)$ at $t = T_{\mathrm{osc}}/2$, due to the continuity of the current, the expression of $i_{L_{\mathrm{a}},T_1}(t)$ during T_2 can be written as:

$$i_{L_{\mathrm{a}},T_2}(t) = \left\{\left(\frac{i_0'}{\omega_{\mathrm{tank}}} + \frac{i_0}{2Q_{\mathrm{tank}}}\right) sin\left(\omega_{\mathrm{tank}}t'\right) + i_0 cos\left(\omega_{\mathrm{tank}}t'\right)\right\} e^{-\left(\left(R_{L_{\mathrm{a}}}+R_{C_{\mathrm{eq}}}\right)/(2L_{\mathrm{a}})\right)t'} \tag{2.12}$$

where $t' = t - T_{\mathrm{osc}}/2$.

Furthermore by substituting $Q_{\text{tank}} = \omega_{\text{tank}} L_{\text{a}} / \left(R_{L_{\text{a}}} + R_{C_{\text{eq}}} \right)$ we get:

$$i_{L_{\text{a}},T_2}(t) = I_{\text{pk}} cos\left(\omega_{\text{tank}} t' - \phi_0\right) e^{-\left(\left(R_{L_{\text{a}}}+R_{C_{\text{eq}}}\right)/(2L_{\text{a}})\right)t'} \tag{2.13}$$

$$I_{\text{pk}} = \sqrt{\left(\frac{i'_0}{\omega_{\text{tank}}} + \frac{i_0}{2Q_{\text{tank}}}\right)^2 + i_0^2} \simeq \sqrt{\left(\frac{i'_0}{\omega_{\text{tank}}}\right)^2 + i_0^2} \tag{2.14}$$

$$\phi_0 = arctan\left(\frac{i'_0}{i_0 \omega_{\text{tank}}} + \frac{1}{2Q_{\text{tank}}}\right) \simeq \left(\frac{i'_0}{i_0 \omega_{\text{tank}}}\right) \tag{2.15}$$

The term ϕ_0 can be further rewritten as:

$$\phi_0 = arctan\left(\frac{2}{\pi}\frac{\omega_{\text{osc}}}{\omega_{\text{tank}}}\right) \simeq \frac{2}{\pi}\frac{\omega_{\text{osc}}}{\omega_{\text{tank}}} = \frac{2}{\pi}\frac{T_{\text{tank}}}{T_{\text{osc}}} \tag{2.16}$$

By noticing that due to the symmetry of $i_{L_{\text{a}}}(t)$ we have that $T_{\phi 1} = T_{\phi 2} = T_{\phi}$.
T_{ϕ} is given by:

$$T_{\phi} = \frac{\phi_0}{2\pi} T_{\text{tank}} \tag{2.17}$$

We have now all the elements to derive the oscillation frequency as follows:

$$T_2 = \frac{T_{\text{osc}}}{2} \tag{2.18}$$

$$= \frac{T_{\text{tank}}}{2} + 2T_{\phi} \tag{2.19}$$

$$= \frac{T_{\text{tank}}}{2} + 2\frac{\phi_0}{2\pi} T_{\text{tank}} \tag{2.20}$$

$$= \frac{T_{\text{tank}}}{2} + \frac{2}{\pi^2}\frac{T_{\text{tank}}^2}{T_{\text{osc}}} \tag{2.21}$$

which results in

$$T_{\text{osc}} = \alpha T_{\text{tank}} \implies \omega_{\text{osc}} = \frac{\omega_{\text{tank}}}{\alpha} = \frac{1}{\alpha}\sqrt{\frac{1}{L_{\text{a}} C_{\text{eq}}}} \tag{2.22}$$

with

$$\alpha = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{4}{\pi^2}} \simeq 1.3 \tag{2.23}$$

Since C_{eq} changes if the tank capacitance is floating or single-ended ω_{tank} changes as well and we have two separate oscillation frequencies.

The formulas for the oscillation frequency of a Class-D oscillator are therefore given by:

$$\omega_{0,\text{float}} = \frac{\sqrt{2}}{\alpha}\sqrt{\frac{1}{LC}} \tag{2.24}$$

$$\omega_{0,\text{se}} = \frac{1}{\alpha}\sqrt{\frac{1}{LC}} \tag{2.25}$$

We immediately notice how operating the oscillator with a floating capacitance allows for higher oscillation frequency than a Class-B oscillator, for the same values of L and C. On the other hand, operation with a completely single-ended capacitance leads to a frequency of oscillation lower than Class-B.

2.1.2 Voltage Waveforms

The expression for the voltage waveform for the Class-D oscillator can be obtained by integrating Equation 2.12. Keeping the assumption that losses in the tank are negligible, we obtain:

$$V_{\text{LO}_+}(t) = V_{\text{DD}} + \left(V_{\text{DD}}\sqrt{\frac{\alpha^2\pi^2}{4}+1}\right) sin\left(\omega_{\text{tank}}t' - \phi\right) \tag{2.26}$$

with peak amplitude:

$$V_{\text{peak}} = V_{\text{DD}}\left(1+\sqrt{\frac{\alpha^2\pi^2}{4}+1}\right) \simeq 3.27V_{\text{DD}} \tag{2.27}$$

Note however that due to losses in the tank the actual peak oscillation amplitude is, as anticipated, $V_{\text{peak}} \simeq 3V_{\text{DD}}$. We show in Figure 2.5 the behaviour of output voltage of the oscillator corresponding to the drain voltage of transistors M_1 and M_2.

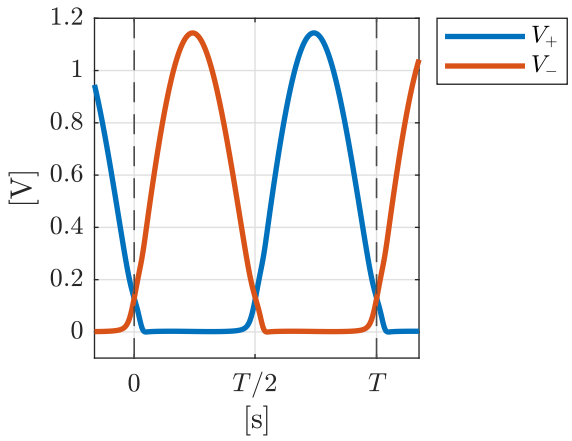


Figure 2.5: Output voltage waveforms for a Class-D oscillator

2.1.3 Current Consumption

The current consumption equations can be also obtained from Equation 2.12 [4]. The equations, that again depend on the nature of the tank capacitance, are the following:

$$I_{\mathrm{DC,float}} = (7.1 - 2.0\kappa)\,\frac{(R_{\mathrm{C}} + R_{\mathrm{L}})\,V_{\mathrm{DD}}}{\omega_{0,\mathrm{float}}^2 L^2} \tag{2.28}$$

$$I_{\mathrm{DC,se}} = (3.6 + 1.6\kappa)\,\frac{(R_{\mathrm{C}} + R_{\mathrm{L}})\,V_{\mathrm{DD}}}{\omega_{0,\mathrm{se}}^2 L^2} \tag{2.29}$$

with $\kappa = R_{\mathrm{L}}/\left(R_{\mathrm{L}} + R_{\mathrm{C}}\right)$.
We note how the values of $I_{\mathrm{DC,se}}$ and $I_{\mathrm{DC,float}}$ depend separately by the loss caused by the inductor parasitic resistance R_{L} and by the capacitance parasitic resistance R_{C}. We have therefore four corners of current consumption, dependently on whether the tank capacitance is floating or single-ended, and whether losses are capacitive or inductive.

In practical implementations however losses in the tank are generally largely given by the inductor resistance, meaning that $\kappa \simeq 1$. By inspecting Equation 2.29 and Equation 2.28 this means that, in order to reduce current consumption, it is advisable to operate the oscillator with a floating tank capacitance whenever possible.

2.1.4 Phase Noise of a Class-D Oscillator

The phase noise performance of the Class-D oscillator is, unsurprisingly, very strongly dependent on whether the tank capacitance is dominated by a floating capacitance or by a single-ended capacitance. Moreover similarly to what we have seen in Equation 2.29 and Equation 2.28 the values R_{L} and R_{C} contribute with different weights to the phase noise. We report below the $1/f^2$ phase noise expression for a floating tank and for a single-ended tank, which have been derived in [4] following the LTV theory of [8].

$$\mathcal{L}_{\mathrm{float}}(\Delta\omega) = 10log_{10}\left[\frac{\omega_{0,\mathrm{float}}^2}{\Delta\omega^2}\frac{k_{\mathrm{B}}\,T}{V_{\mathrm{DD}}^2}\left(0.104R_{\mathrm{L}} + 0.141R_{\mathrm{C}}\right)\left(1 + n_{\mathrm{MOS}}\right)\right] \tag{2.30}$$

$$\mathcal{L}_{\mathrm{se}}(\Delta\omega) = 10log_{10}\left[\frac{\omega_{0,\mathrm{se}}^2}{\Delta\omega^2}\frac{k_{\mathrm{B}}\,T}{V_{\mathrm{DD}}^2}\left(0.104R_{\mathrm{L}} + \frac{0.141}{2}R_{\mathrm{C}}\right)\left(1 + n_{\mathrm{MOS}}\right)\right] \tag{2.31}$$

where n_{MOS} is the noise generated by both switches together normalized by the tank noise. We notice how, since the Class-D oscillator works in the voltage limited regime, PN is directly dependent from V_{DD}.

By inspecting Equation 2.30 and Equation 2.31 we can conclude that, similarly to the case of current consumption, it is highly advantageous to operate the Class-D oscillator with a floating tank capacitance and tank losses dominated by the tank inductance, if the best phase-noise performance is to be retained. We note that a reasonable contribute to phase noise for each switch is 20-25%, meaning that the noise produced by the switches can add up to almost 50% of the total phase noise of the oscillator (n_{MOS}=1).

Additionally, as reported in [4], employing wider switches result in lower phase noise if the tank capacitance is floating, while on the other hand the phase noise may even increase if the tank capacitance is single-ended. Moreover, for a given level of $1/f$ noise, the upconverted $1/f^3$ phase noise decreases when the switch on-resistance decreases. As a result in order to guarantee a good phase noise performance the switches M_1 and M_2 must be made as big as reasonably possible. This is in accordance with what has been anticipated, regarding how the sizing of the switches is crucial to guarantee good Class-D operation. Naturally, since real transistors include parasitic capacitance, there is a limit on how large the switches can be made.
We have in fact that:

$$\omega_{\mathrm{tank}} = \sqrt{\frac{1}{L\left(C + C_{\mathrm{par}}\right)}} \tag{2.32}$$

where C_{par} groups up all the parasitic capacitance contributions, showing how they can compromise the maximum switching frequency of the oscillator if $C \simeq C_{\mathrm{par}}$.
The sizing of the transistors therefore has to be made without compromising the ability of the oscillator to reach the target oscillation frequency ω_0.

2.2 Class-D VCO

In practical implementations, oscillators do not operate at a fixed frequency, but they are built in a way that allows them to change their oscillation frequency dynamically. The regulation of the oscillation frequency is usually achieved by means of a capacitor bank connected to the differential nodes of the oscillator. The bank contains a parallel combination of switchable capacitors that can be added or subtracted to the total tank capacitance to respectively decrease or increase ω_0.

Although the capacitances of the bank may be chosen to appear single-ended when active, a better choice in the case of Class-D oscillators, is to have them float. We have in fact seen how by loading the oscillator with a floating capacitance we are able to obtain a better value of phase noise, oscillation frequency and lower the power consumption. In Figure 2.6 an implementation of a floating $3bit$ capacitor bank is showed.

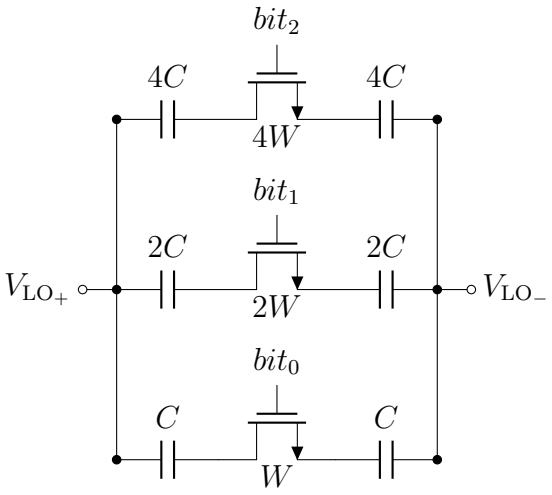


Figure 2.6: 3bit floating capacitor bank

where following the scheme of Figure 2.6 the mosfets have to be sized so that their equivalent resistance R_{on} doesn't degrade the quality factor of the tank. Their width is therefore scaled as the capacitors increase.

One additional note is that, while the capacitor bank allows us to rapidly increase the size of the tank capacitor, the resolution through which we can change ω_0 is discrete as such is the nature of the capacitance added by the bank. An additional voltage controlled capacitor has therefore to be added to the bank in order to continuously fine tune the frequency of the oscillator, by means of a tuning voltage V_{tune}, as show in Figure 2.7

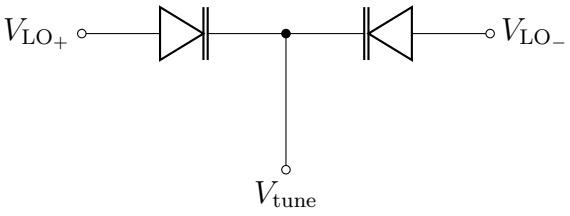


Figure 2.7: Circuit for fine tuning of the oscillation frequency

Since both the discrete and continuous tunings are made using voltage, an oscillator realized in this way is generally called a VCO. These oscillators are commonly compared based on their PN performance, power consumption and tuning range, which is defined as follows:

$$TR = \frac{\omega_{0,\max} - \omega_{0,\min}}{\frac{\omega_{0,\max} + \omega_{0,\min}}{2}} \tag{2.33}$$

where $\omega_{0,\max}$ is the maximum oscillation frequency achievable by the VCO and $\omega_{0,\min}$ the minimum. Additionally it is common practice to show the tuning range of the VCO by plotting the value of the oscillation frequency f_0 as a function of V_{tune} and of the combinations of the capacitor bank. An example is shown in Figure 2.8 were f_0 is plotted as a function of V_{tune} for two adjacent bank combinations.

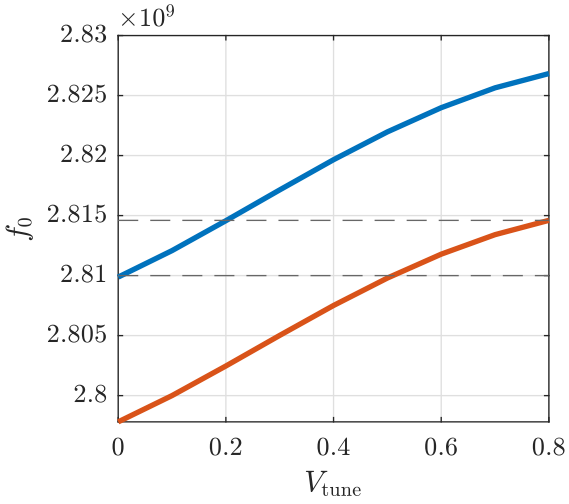


Figure 2.8: Example of tuning range behaviour for a VCO

Note from Figure 2.8 that, to guarantee a continuous tuning, the 2 adjacent curves must slightly overlap so that the VCO correctly covers all its tuning range. One final note, following the previous considerations, is that the Class-D VCO works under quite different conditions across its tuning range. When the capacitor bank is fully switched in the oscillator sees what is basically a completely floating capacitance. On the other hand, when the bank is switched out the tank capacitance is dominated by the parasitic capacitances of the switches which are single-ended. This behaviour has to be kept in consideration during the design process as it affects the performance of the VCO based on its current capacitor bank combination and in turn on its oscillation frequency f_0.

CHAPTER 3

Switched Capacitor Converters

In this chapter, an analysis of the SC converter is presented. First the working principle of this particular topology is explained. The model of the converter is then derived, focusing on the modelling of the output impedance. A loss model is presented in order to define which combination of parameters of the design space maximizes the efficiency. A control technique, chosen in order to fit our desired application, is presented and analysed. Finally, the main auxiliary circuits that are necessary for the correct behaviour of the circuit are illustrated.

3.1 Theoretical Analysis and Derivation of an Ideal Model

In this section the working principle of the SC converter is illustrated, and its ideal model is derived. The topology of a $1/2$ SC converter is showed in Figure 3.1.

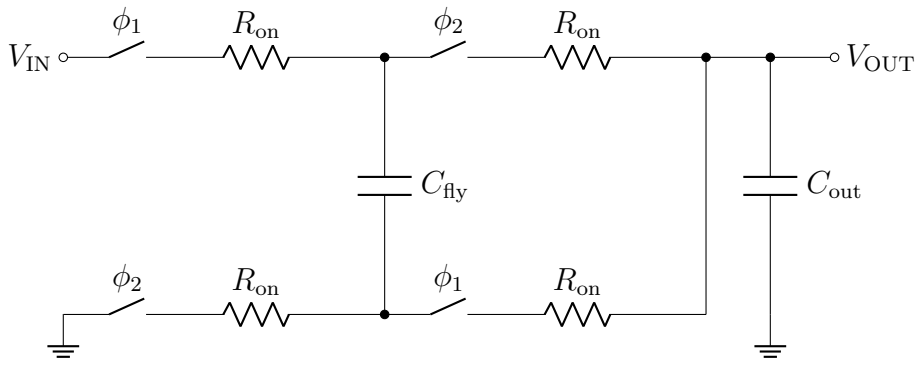
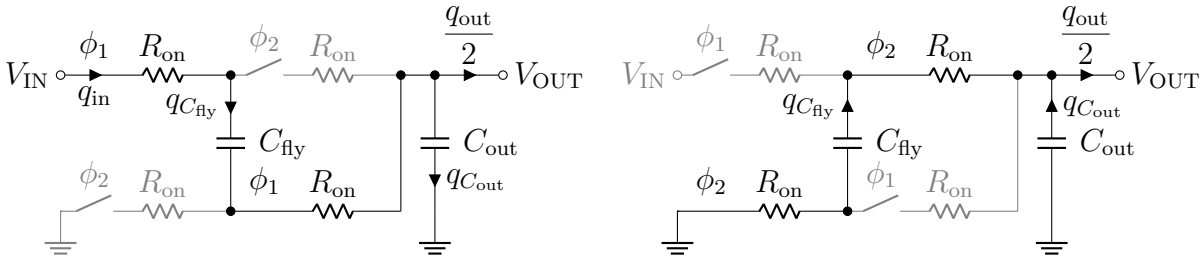


Figure 3.1: Simplified schematic of a $1/2$ SC converter

The converter is composed of a flying capacitor C_{fly} and 4 switches having equivalent resistance R_{on}, where $\phi_{1,2}$ are two clock signals complementary to each other with 50% duty cycle and switching frequency f_{sw}.

During phase ϕ_1, C_{fly} connects between the input voltage V_{IN} and the output voltage V_{OUT} and, during phase ϕ_2, C_{fly} connects between V_{OUT} and ground as shown in Figure 3.2 [9].



(a) Schematic during ϕ_1 (b) Schematic during ϕ_2

Figure 3.2: Change of the SC converter topology based on $\phi_{1,2}$

The capacitor C_{fly} therefore acts as a "bucket" absorbing charge during ϕ_1 and releasing it during ϕ_2 towards the output node V_{OUT}. The filtering capacitor C_{out}, on the other hand, is needed to store the charge drawn through C_{fly} from the power supply V_{IN}.
It is easy to show that this topology indeed realizes a step down converter with conversion ratio CR equal to $1/2$. Assuming that V_{OUT} is kept constant, due to charge conservation we have that when a transition between phases $\phi_{1,2}$ occurs the following equation must be true:

$$(V_{\text{IN}} - V_{\text{OUT}}) \cdot C_{\text{fly}} = V_{\text{OUT}} \cdot C_{\text{fly}} \tag{3.1}$$

which can easily be rewritten to show that indeed:

$$CR = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1}{2} \tag{3.2}$$

However, it has to be noted that these calculations were made by neglecting the finite resistance R_{on} of the switches and the influence of the charge/discharge time of capacitor C_{fly}. In reality the equation $V_{\text{OUT}} = CR \cdot V_{\text{IN}}$ has to be viewed as the maximum ideal limit to the value of V_{OUT}, hence $V_{\text{MAX}} = CR \cdot V_{\text{IN}}$, while the real value of V_{OUT} is going to be smaller than V_{MAX} due to the losses that are present in the real circuit. These losses can be modelled by the means of a resistance R_{OUT} put in series to the ideal voltage source V_{MAX}. The SC converter can therefore be modelled as an ideal transformer, as seen in Figure 3.3.

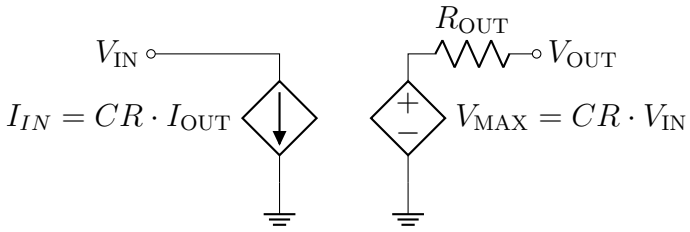


Figure 3.3: Ideal transformer model

As a result, the value of the output voltage can be expressed as:

$$V_{\text{OUT}} = \frac{V_{\text{IN}}}{2} - R_{\text{OUT}} \cdot I_{\text{OUT}} \tag{3.3}$$

It has to be noted that, for the same value of R_{OUT}, as the load current I_{OUT} increases, the value of V_{OUT} decreases. Meaning that only for very light loads we have $V_{\text{OUT}} \simeq V_{\text{MAX}}$.

3.1.1 Modelling of the Output Resistance

The value of R_{OUT} in a SC converter however is not fixed, but it's frequency dependent meaning that it depends on the switching frequency f_{sw} of the converter and has two limits referred to as the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL). These limits are related to the time constants of the capacitive networks in the system. In SSL, f_{sw} is low compared to these time constants. This means that the capacitors voltages tend to settle to their final values and current flow is limited by the capacitance. Therefore, from the perspective of the load, the converter appears capacitive. On the other hand, in FSL, f_{sw} is high with respect to the time constants. The capacitors are therefore unable to charge to their final value and the on-resistances of the switches is responsible for limiting the current flow. From the perspective of the load the converter this time appears resistive. An example of this behaviour is illustrated in Figure 3.4.

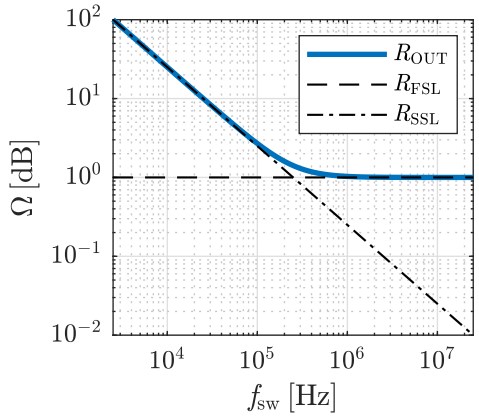


Figure 3.4: Frequency behaviour of resistance R_{OUT}

As we can see from Figure 3.4 the behaviour of R_{OUT} has, as already mentioned, two extremes given by the SSL and the FSL with a zone in the middle where the f_{sw} is comparable to the time-constants of the circuit meaning that R_{OUT} is both "resistive and capacitive".

The behaviour of R_{OUT} that is shown in Figure 3.4 is derived from a model of the output resistance which is the following:

$$R_{\mathrm{OUT}} = \sqrt{R_{\mathrm{SSL}}^2 + R_{\mathrm{FSL}}^2} \tag{3.4}$$

This model proves to be accurate if we assume that C_{out} is huge compared to C_{fly} [18]. The resistances R_{SSL} and R_{FSL} which model respectively the SSL impedance and the FSL impedance of the converter can be calculated using the following generalized formulas, which are applicable for many different families of switched capacitor converters.

$$R_{\mathrm{SSL}} = \sum_{i \in caps} \frac{a_{\mathrm{c,i}}^2}{C_{\mathrm{i}} \cdot f_{\mathrm{sw}}} \tag{3.5}$$

$$R_{\mathrm{FSL}} = \sum_{i \in switches} a_{\mathrm{r,i}}^2 \cdot 2R_{\mathrm{on,i}} \tag{3.6}$$

where $R_{\mathrm{on,i}}$ and C_{i} represent respectively the value of equivalent resistance of the i-th transistor and of capacitance of the i-th capacitor. The variables $a_{\mathrm{c,i}}$ and $a_{\mathrm{r,i}}$ on the other hand are called charge multiplier vectors. $a_{\mathrm{c,i}}$ in particular is the capacitor charge multiplier vector and it represents the charge that flows in and out of each capacitor in each switching state. Similarly, $a_{\mathrm{r,i}}$ is called a transistor charge multiplier vector and it represent the charges flowing through each switch.

The derivation of these vectors generally is not trivial for complex converters but given the simplicity of our $1/2$ SC converter the results are in this case easily derived. In order to do so we have to understand how charge moves during the operation of the SC converter.

As shown in [10], referencing Figure 3.2 we first notice that since the converter operates at 50% duty cycle, then the current drawn by the load, namely $q_{\mathrm{out}}/2$, is going to be equal in both phases. We can then proceed by writing the KCL equations of the circuit in Figure 3.2 for the states corresponding to ϕ_1 and ϕ_2.

In the first state we have:

$$q_{C_{fly}} = q_{in,\phi_1} = q_{C_{\text{out}}} + \frac{q_{\text{out}}}{2} \tag{3.7}$$

while in the second state we have:

$$q_{C_{\text{fly}}} + q_{C_{\text{out}}} = \frac{q_{\text{out}}}{2}, \qquad q_{\text{in},\phi_2} = 0 \tag{3.8}$$

Summing Equation 3.7 and Equation 3.8 together we get:

$$q_{C_{\text{fly}}} = \frac{q_{\text{out}}}{2}, \qquad q_{C,\text{out}} = 0 \tag{3.9}$$

The charge vectors for the capacitors can therefore be derived as:

$$a_{\text{c},\phi_1} = \begin{bmatrix} q_{C_{\text{out}},\phi_1} & q_{\text{out},\phi_1} & q_{C_{\text{fly}},\phi_1} & q_{\text{in},\phi_1} \end{bmatrix} / q_{\text{out}} = [0.5 \quad 0 \quad 0.5 \quad 0.5] \tag{3.10}$$

$$a_{\text{c},\phi_2} = \begin{bmatrix} q_{C_{\text{out}},\phi_2} & q_{\text{out},\phi_2} & q_{C_{\text{fly}},\phi_2} & q_{\text{in},\phi_2} \end{bmatrix} / q_{\text{out}} = [0.5 \quad 0 \quad -0.5 \quad 0] \tag{3.11}$$

For the switches, on the other hand, we have that when a switch is OFF its charge is zero, while when its ON it has the same charge of capacitor C_{fly}, i.e. $q_{C_{\text{fly}}}$. Therefore the charge vector for the switches is:

$$a_{\text{r},\phi_1} = [q_{SW1,\phi_1} \quad q_{SW2,\phi_1} \quad q_{SW3,\phi_1} \quad q_{SW4,\phi_1}] / q_{\text{out}} = [0.5 \quad 0 \quad 0.5 \quad 0] \tag{3.12}$$

$$a_{\text{r},\phi_2} = [q_{SW1,\phi_2} \quad q_{SW2,\phi_2} \quad q_{SW3,\phi_2} \quad q_{SW4,\phi_2}] / q_{\text{out}} = [0 \quad 0.5 \quad 0 \quad 0.5] \tag{3.13}$$

By putting the values that we have obtained, for the charge vectors, inside of Equation 3.5 and Equation 3.6 we finally get:

$$R_{\text{SSL}} = \frac{1}{4 C_{\text{fly}} f_{\text{sw}}} \tag{3.14}$$

$$R_{\text{FSL}} = 2 R_{\text{on}} \tag{3.15}$$

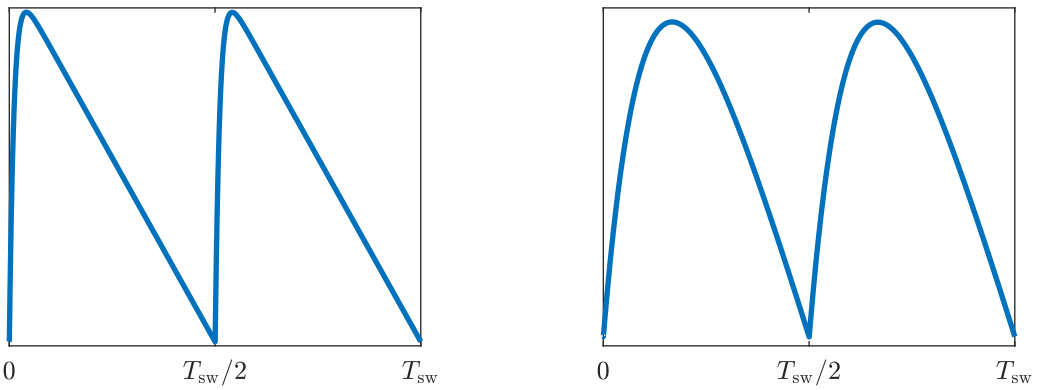
With these equations finally derived we immediately notice how, for the same target R_{SSL}, it is possible to reduce the dimension of capacitor C_{fly} simply by increasing the value of the switching frequency f_{sw}. Naturally, as we will see during the analysis of the SC converter efficiency, by increasing f_{sw} we will have also an increase in dissipated power, so a trade off has to be made on the sizing of C_{fly}.

3.1.2 Output Voltage Ripple

Up until now we have simplified our analysis by considering that V_{OUT} is kept constant and that $C_{\mathrm{out}} \gg C_{\mathrm{fly}}$. In reality we have that V_{out} shows some ripple given by the operation of the converter. At the very start of each phase we have that C_{out} either charges together with C_{fly}, as in ϕ_1, or is charged by the charge stored by C_{fly} which happens in ϕ_2. This charging process makes the voltage at the terminals of C_{out} increase. At the same time however the load absorbs a current I_{OUT} that, in first approximation, we can assume as constant which discharges the capacitor C_{out} making V_{OUT} decrease. The charging/discharging of C_{out} originates a ripple on the node V_{out}.

Before making any consideration on how to estimate this ripple it has to be noted that the "shape" of the ripple itself changes based on how much the SSL resistance R_{SSL} prevails on the FSL one R_{FSL}. This is in turn related to the time constants of the SC converter itself. We have that the equivalent resistance of the switches R_{on} and the capacitor C_{fly} form a RC network that charges and discharges during a time $T_{\mathrm{sw}}/2$. The time constant of the network for a specific phase $\phi_{1,2}$ can be calculated as $\tau \simeq 2R_{\mathrm{on}}C_{\mathrm{fly}}$.

If $\tau \ll T_{\mathrm{sw}}/2$ we have that at the start of each phase $\phi_{1,2}$ the charge transfer towards C_{out} can be modelled as an impulse raising instantly the value of V_{out} which then slowly decreases linearly as I_{OUT} "consumes" the charge stored in C_{out}. In this case we have that the ripple has a sawtooth-behaviour as illustrated in Figure 3.5a. On the other hand if $\tau \simeq T_{\mathrm{sw}}/2$ the initial charge of C_{out} can no longer be approximated by an impulse and the ripple will have a more distinct exponential shape at the start of a phase $\phi_{1,2}$ as showed in Figure 3.5b.



(a) Ripple with "impulse" charging

(b) Ripple with finite charging

Figure 3.5: Ripple behaviour

To quantify the amplitude of ΔV_{ripple} one way is to consider that C_{fly} at the end of ϕ_1 is charged to $(V_{\text{in}} - V_{\text{out}})$ while it's shorted to C_{out} during ϕ_2. The value of V_{out} as a result, during a transition $\phi_1 \rightarrow \phi_2$, becomes $(V_{\text{out}} + \Delta V_{\text{ripple}})$. We can therefore calculate ΔV_{ripple} as: [7]

$$C_{\text{out}} V_{\text{out}} + C_{\text{fly}} (V_{\text{in}} - V_{\text{out}}) = (C_{\text{out}} + C_{\text{fly}}) (V_{\text{out}} + \Delta V_{\text{ripple}}) \tag{3.16}$$

$$\implies \Delta V_{\text{ripple}} = \frac{C_{\text{fly}}}{C_{\text{fly}} + C_{\text{out}}} (V_{\text{in}} - 2V_{\text{out}}) \simeq \frac{C_{\text{fly}}}{C_{\text{out}}} (V_{\text{in}} - 2V_{\text{out}}) \tag{3.17}$$

It has to be noted however that this formula works under the hypothesis that the charge transfer can be considered as an impulse, so it works well to estimate the ripple of Figure 3.5a, while it has to be considered as an upper-bound for the case in Figure 3.5b. Nevertheless from Equation 3.17 we get an important result as we notice that the ripple is proportional to the ratio of $C_{\text{fly}}/C_{\text{out}}$ and we can immediately see how by imposing $C_{\text{out}} \gg C_{\text{fly}}$ it is possible to directly reduce the ripple. This result is not completely surprising since for capacitors we have that $\Delta V_{\text{C}} = q/C$ and since the charge q, transferred to the capacitor during a switching cycle is fixed it's natural that by increasing C the variation of voltage at the extremes of the capacitor ΔV_{C} is reduced.

Another way of estimating ΔV_{ripple}, by making use of the "impulse" charging approximation, is considering the section of the ripple after the effect of the charge "impulse" where V_{out} starts to decrease linearly. We have that V_{out} decreases with a slope given by $I_{\text{OUT}}/(C_{\text{fly}} + C_{\text{out}})$ [17] which can either be deduced by inspecting the circuit or by computing the term directly by means of state space equations. Therefore knowing that a phase $\phi_{1,2}$ lasts for a time $T_{\text{sw}}/2$ we have:

$$\Delta V_{\text{ripple}} = \frac{T_{\text{sw}}}{2} \frac{I_{\text{OUT}}}{(C_{\text{fly}} + \text{out})} = \frac{I_{\text{OUT}}}{2 f_{\text{sw}} (C_{\text{fly}} + C_{\text{out}})} \tag{3.18}$$

For this formula the same reasonings, regarding the quality of the approximation, apply as in Equation 3.17. Moreover simulations results show that this method of estimating ripple leads to bigger errors compared to Equation 3.17 if $\tau \simeq T_{\text{sw}}/2$. The result however clearly shows us how ΔV_{ripple} is also tied to the switching frequency f_{sw} and the load current I_{OUT}.

3.1.3 Symmetric Charge-Discharge Topology

The analysis that we have carried out of the SC converter structure up to this moment has neglected the effect that the parasitic capacitances, of its various components, have on its behaviour. We are now going to analyse how these capacitances, especially the ones related to capacitor C_{fly}, impact ΔV_{ripple} as seen in [16]. Real capacitors often include a top and bottom plate parasitic capacitance as shown in Figure 3.6.

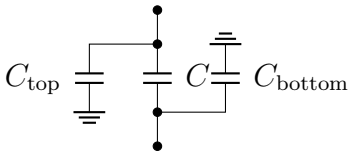
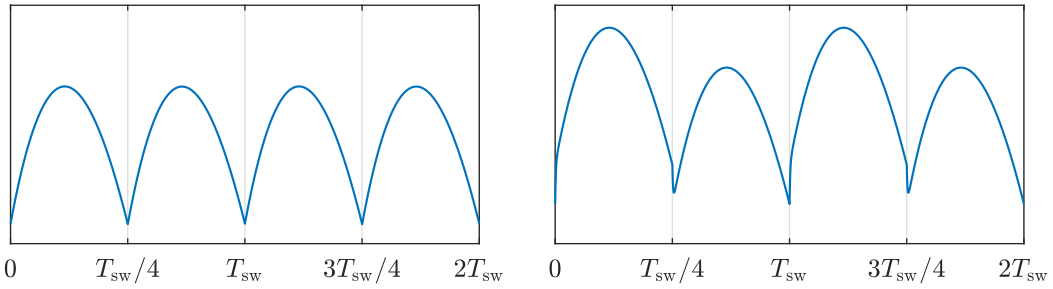


Figure 3.6: Top and bottom plate capacitance in a capacitor

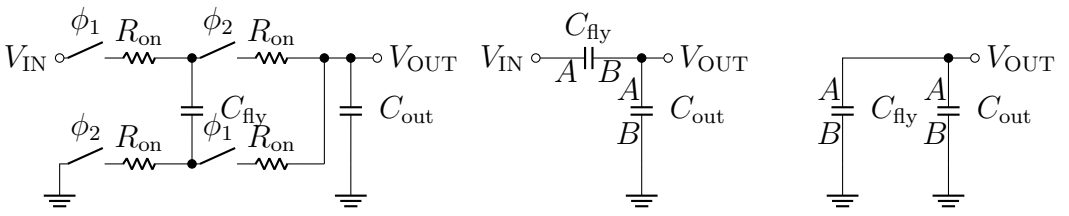
This non ideality manifests itself by making the ripple of the converter asymmetric with respect to phases ϕ_1 and ϕ_2. The effect can be appreciated in Figure 3.7 where an appropriate comparison is made between a converter without parasitic capacitances and one with 2% top and bottom plate parasitic capacitances.



(a) Ideal converter (b) 2% top/bottom plate capacitance

Figure 3.7: Comparison of voltage ripple between converters

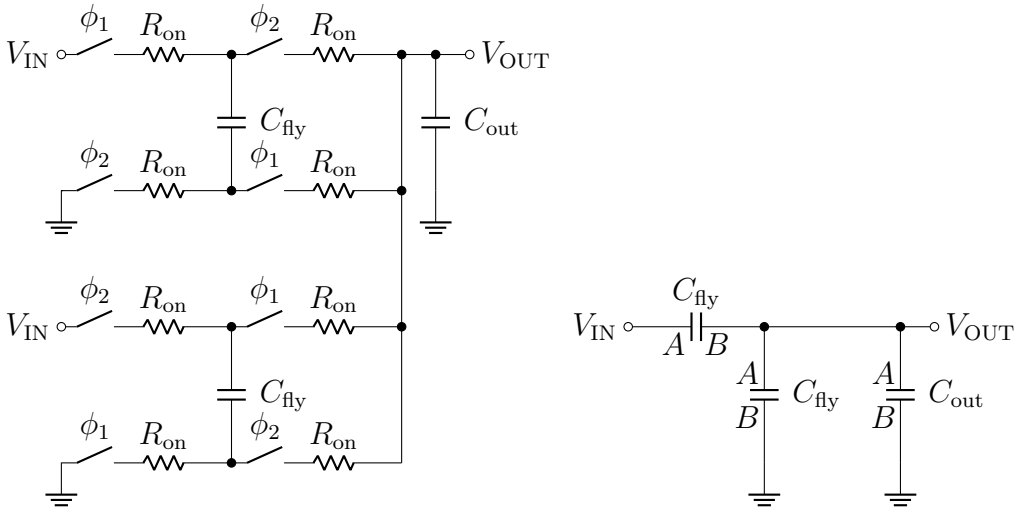
As shown in Figure 3.7b, the effect of the bottom plate capacitance modulates the voltage ripple. In order to understand why this happens we look at Figure 3.8:



(a) Asymmetric SC converter scheme (b) Capacitor scheme during ϕ_1 (c) Capacitor scheme during ϕ_2

Figure 3.8: Asymmetric converter topology

From Figure 3.8b we see that during ϕ_1 C_{fly} is charged with its bottom-plate (terminal B) connected to C_{out}. During ϕ_2 as shown in Figure 3.8c, on the other hand, the top-plate (terminal A) of C_{fly} is connected to C_{out}. We also have that during ϕ_2 C_{out} and C_{fly} are connected in parallel making the equivalent output capacitance bigger and decreasing ΔV_{ripple}. This problem can be solved by recurring to the converter topology of Figure 3.9.



(a) Symmetric SC converter scheme

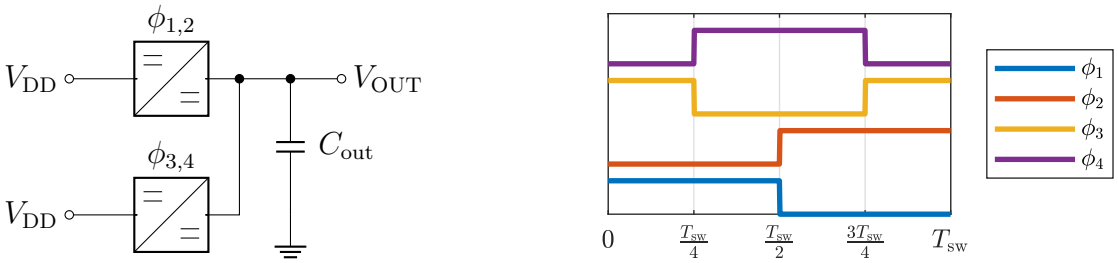
(b) Capacitor scheme during ϕ_1 and ϕ_2

Figure 3.9: Symmetric converter topology

By operating the converter as a combination of two converters "modules" working in opposition of phase as seen in Figure 3.9a we have that the capacitor scheme is the same in both phases as shown in Figure 3.9b, meaning that the asymmetric voltage ripple is eliminated. This solution can also be used to reduce the overall ripple of the converter [9] but to a smaller degree that what we will see in Section 3.1.4. Finally employing an asymmetric converter ever so slightly eases its design as now the output resistance R_{OUT} is given by the parallel of two smaller modules. This makes the value of R_{OUT} less subject to deviations of the components values or slight sizing errors, as the effect of the parallel evens out these differences, resulting in a more consistent value of R_{OUT}.

3.1.4 Phase Interleaving

We want now to analyse a technique that allows us to drastically decrease the ripple of our converter. The idea is very similar to the one shown in Section 3.1.3 since its realized by taking N different SC converter modules and operating them in parallel, but this time a phase shift, equal to $T_{sw}/2N$, is applied to the phases of each module i with respect to the module $i-1$. This technique takes the name of "Phase Interleaving" and in order to understand how it works we first take a look at Figure 3.10 where the operation of a $N = 2$ phases interleaved converter is depicted.

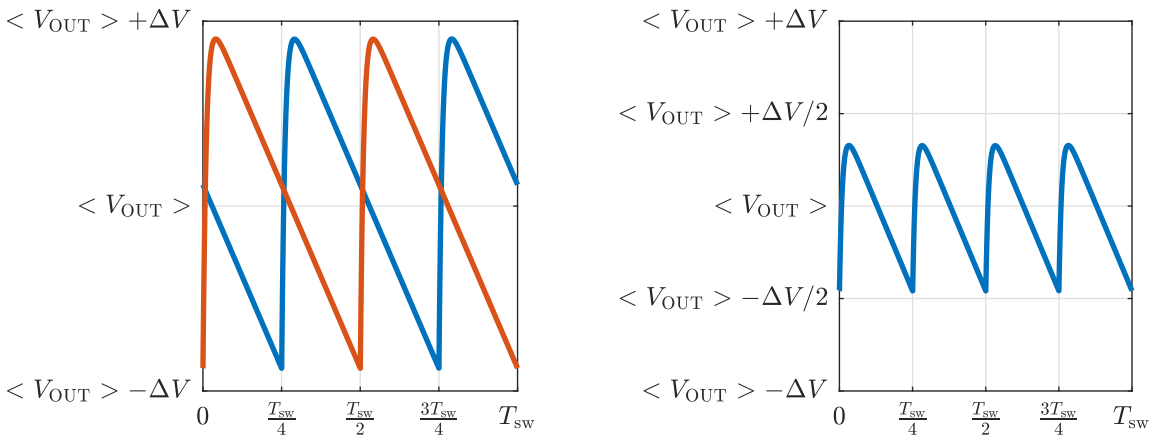


(a) Symmetric SC modules interleaved with $N = 2$

(b) Interleaved phases

Figure 3.10: Phase utilization and topology of a phase interleaved converter

We see from Figure 3.10a that in this interleaving scheme two symmetric converters are made to work in parallel with each other. The phases used to drive the modules are showed in Figure 3.10b where we can appreciate how ϕ_1 is in opposition of phase with respect to ϕ_2, and the same goes for ϕ_3 and ϕ_4. It's also quite clear how the pair $\phi_{3,4}$ has been obtained by phase shifting $\phi_{1,2}$ by $T_{sw}/4$. Finally in Figure 3.11 it's showed how phase interleaving effectively reduces the ripple of the converter.



(a) Symmetric non-interleaved converters V_{out}

(b) V_{out} after Interleaving of the symmetric converters

Figure 3.11: Comparison of voltage ripple between converters

In Figure 3.11b we show the output voltage V_{out} of the two symmetric converters working separately, while in Figure 3.11a we show V_{out} when the converters work in parallel with interleaved phases. We can easily notice how ΔV_{ripple} has decreased by a factor of $N \simeq 2$ in the interleaved case.

This is due to the fact that now charge is taken from the input and delivered to the output in smaller amounts, thanks to phase interleaving. In fact with the previous structure charge was delivered in larger amounts at a single time instant increasing ΔV_{ripple}. Therefore thanks to phase interleaving we can reduce by a factor of N the value of ΔV_{ripple}, with respect to non-interleaved SC converters.

3.2 Derivation of Efficiency Limits

We are now interested in realizing a mathematical model of the SC converter, in order to understand how to correctly size its components. More specifically, we want to see how its efficiency varies based on the combination of the design variables such as the switching frequency f_{sw}, dimension of flying capacitor C_{fly} and sizing of the switches $W_{\text{SW,i}}$. We proceed therefore by creating a loss model of the converter in order to understand how to maximize its efficiency.

We start by considering the losses due to the finite resistance of the converter R_{OUT} which are called conduction losses and are given as follows:

$$P_{\text{conduction}} = I_{\text{out}}^2 \cdot R_{\text{OUT}}/N/k_{\text{sym}} \tag{3.19}$$

where R_{OUT} is considered as the equivalent output resistance of a single asymmetric converter module. The factor k_{sym} takes into account if the converter is symmetric or not and it's equal to 2 or 1 respectively, while the term N accounts for phase interleaving. We notice how in order to reduce $P_{\text{conduction}}$ it is necessary to reduce R_{OUT}, which in turn implies that the terms $R_{\text{SSL}} \propto^{-1} (C_{\text{fly}} f_{\text{sw}})$ and $R_{\text{FSL}} \propto R_{\text{on}}$ must decrease as seen in Equation 3.14 and Equation 3.15. Note that since $R_{\text{on,i}} \propto^{-1} W_{\text{SW,i}}$, as we will see in Section 3.2.1, the last condition is equivalent to increasing the size of the switches $W_{\text{SW,i}}$.

We now direct our analysis to the subject of switching losses. These losses are given by the parasitic gate capacitance C_{gg} of the transistors, used to realize the switches. The capacitance C_{gg} in fact is charged and discharged every switching cycle dissipating power. The formula for these losses is:

$$P_{\mathrm{switching}} = C_{\mathrm{gg,TOT}} \cdot V_{\mathrm{IN}}^2 \cdot f_{\mathrm{sw}} \cdot N \cdot k_{\mathrm{sym}} \tag{3.20}$$

where $C_{\mathrm{gg,TOT}}$ groups together the parasitic capacitance $C_{\mathrm{gg,i}}$ of each of the four switches that realize a converter module. Note that $C_{\mathrm{gg,i}} \propto W_{\mathrm{SW,i}}$, but since we have seen that $R_{\mathrm{on,i}} \propto^{-1} W_{\mathrm{SW,i}}$ we immediately notice that there is a trade off between reducing R_{FSL} and $P_{\mathrm{switching}}$, while scaling the value of $W_{\mathrm{SW,i}}$. A similar trade off is made when trying to limit the value of C_{fly} used by increasing f_{sw} in R_{SSL} as it also means an increase in $P_{\mathrm{switching}}$.

Another loss present in the converter is given by the losses due to top and bottom plate parasitic capacitances that, as anticipated, are present in the capacitor C_{fly}. These losses share a very similar formulation to the switching losses, as seen below:

$$P_{\mathrm{top/bottom\ plate}} = C_{\mathrm{fly}} \cdot \frac{V_{\mathrm{out}}^2}{2} \cdot f_{\mathrm{sw}} \cdot k_{\mathrm{top/bottom}} \tag{3.21}$$

where C_{fly} refers to the total flying capacitance used in the converter, including all modules present due to symmetric design or phase interleaving, while $k_{\mathrm{top/bottom}}$ on the other hand is the percentage of parasitic top and bottom plate capacitance with respect to C_{fly}. The $1/2$ factor takes into account that, while referencing Figure 3.8 only the bottom capacitance (terminal B) contributes to losses as its charged at V_{out} during ϕ_1 and then discharged during ϕ_2 towards ground. To get a feeling on the importance of this loss we note that the product $(C_{\mathrm{fly}} \cdot k_{\mathrm{top/bottom}})$ often times is comparable to $C_{\mathrm{gg,TOT}}$. Finally the last loss present in the circuit is given by the parasitic resistance of the flying capacitor R_{ESR}. This loss component is often negligible, nevertheless we have decided to include it in the model. Its formula is given by:

$$P_{\mathrm{ESR}} = I_{\mathrm{OUT}}^2 \cdot R_{\mathrm{ESR}}/N/k_{\mathrm{sym}} \tag{3.22}$$

Now that we know all the power that is lost inside the converter, before calculating the efficiency, we have to calculate the amount of power delivered to the load.

This power is given by P_{out} which is expressed as:

$$P_{\text{out}} \simeq \left(V_{\text{out,min}} + \frac{\Delta V_{\text{ripple}}}{2}\right)\left(I_{\text{out,min}} + \frac{\Delta I}{2}\right) \simeq V_{\text{OUT}} \cdot I_{\text{OUT}} \tag{3.23}$$

where we have assumed negligible the effect of the output voltage ripple ΔV_{ripple} and of the output current ripple ΔI. Note also that the value of V_{OUT} has to be calculated, following Equation 3.3, by correctly considering the value of R_{OUT} based on the structure of the converter and the values N and k_{sym}. The expression of the output resistance therefore becomes:

$$R_{\text{OUT}_{\text{TOT}}} = R_{\text{OUT}}/N/k_{\text{sym}} \tag{3.24}$$

where, as anticipated, R_{OUT} now represents the resistance associated to a single converter module. By combining all the previous equations we can calculate the converter theoretical efficiency, which is given by:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{conduction}} + P_{\text{switching}} + P_{\text{top/bottom}} + P_{\text{ESR}}} \tag{3.25}$$

we have that η is dependent on the design variables: f_{sw}, C_{fly} and $W_{\text{SW,i}}$ so in order to arrive to a final design we have to impose some constraints on these design variables.

We can simplify our analysis by first considering instead of, 4 separate variables $W_{\text{SW,i}}$, controlling the size of the switches, the value of R_{FSL}. In this way we can focus on selecting an appropriate value of R_{SSL} while sizing the mosfets later following a procedure which will be explained in Section 3.2.1. We then impose the constrain that the time-constant of the converter during either phases $\phi_{1,2}$ must be such that: $4\tau = T_{\text{sw}}/2$ [9]. This choice will be better explained in Section 3.2.2 and it's easy to show that it's equivalent to imposing that $2R_{\text{SSL}} = R_{\text{FSL}}$.

$$4\tau = \frac{T_{\text{sw}}}{2} \tag{3.26}$$

$$4\left(2R_{\text{on}}C_{\text{fly}}\right) = \frac{1}{2f_{\text{sw}}} \tag{3.27}$$

$$2\left(2R_{\text{on}}\right) = \frac{1}{4C_{\text{fly}}f_{\text{sw}}} \tag{3.28}$$

$$2R_{\text{FSL}} = R_{\text{SSL}} \tag{3.29}$$

Following the constrain imposed by Equation 3.29 we have that by selecting a value of C_{fly} and f_{sw} we are also imposing the value of R_{FSL}, while $W_{\text{SW,i}}$ as anticipated can be derived by R_{SSL}. We therefore now have all the elements to plot the value of η as a function of only C_{fly} and f_{sw}. This will allow us to understand how to size C_{fly} when aiming to obtain a specific efficiency, for a given I_{OUT}. A plot of $\eta\left(C_{\text{fly}}, f_{\text{sw}}\right)$, for an ideal load current of $I_{\text{OUT}} = 12.4\text{mA}$, is showed in Figure 3.12.

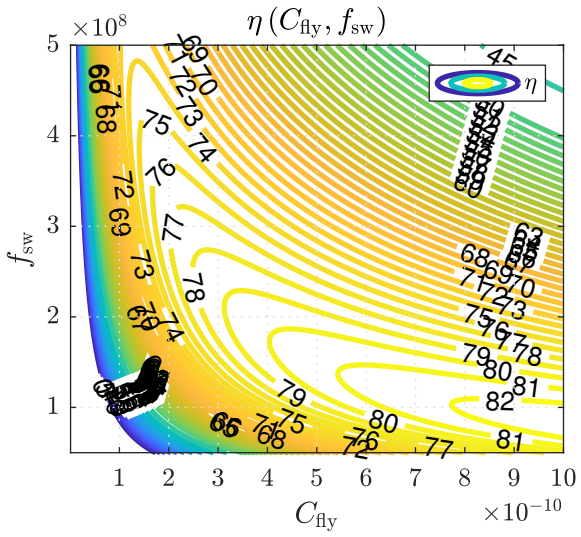


Figure 3.12: $\eta\left(C_{\text{fly}}, f_{\text{sw}}\right)$ using technology values

After having selected C_{fly} we can then relax the constrain imposed by Equation 3.29 and plot η as a function this time of f_{sw} and R_{FSL} to find a design point for our converter. A plot of $\eta\left(f_{\text{sw}}, R_{\text{FSL}}\right)$, where $C_{\text{fly}} = 500\text{pF}$ is showed in Figure 3.13. In both cases we have assumed $N = 1$ and $k_{\text{sym}} = 2$. Note that the value of R_{FSL} found refers to a single converter module.

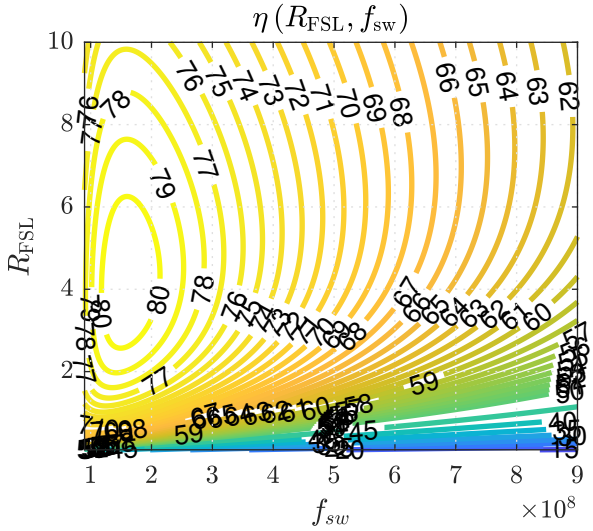


Figure 3.13: $\eta\left(R_{\text{FSL}}, f_{\text{sw}}\right)$ using technology values

3.2.1 Sizing of the Mosfets

Given a certain value of R_{FSL}, that we want to obtain, we have that the SC converter is going to be realized by employing mosfets as in Figure 3.14, where switches $SW_{1,2}$ have been implemented as p-mosfets, while switches $SW_{1,2}$ as n-mosfets.

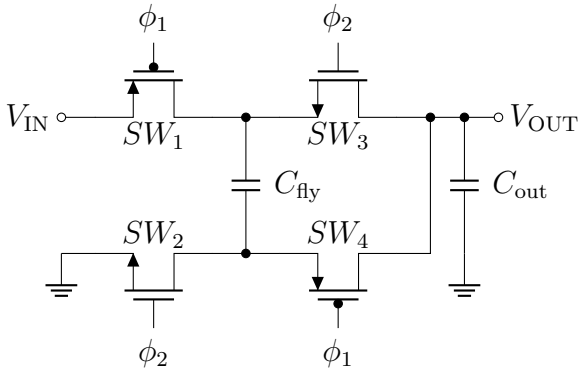


Figure 3.14: SC converter scheme with real mosfet switches

This means that phases $\phi_{1,2}$ have to be modified and can no longer be considered complementary, since p-mosfets work for negative values of V_{GS}, while n-mosfets for positive values of V_{GS}. Moreover the phases that will drive the mosfets will need to include a "dead-time" in the transition between phases $\phi_{1,2}$ to avoid the condition where all switches are turned on at the same time, due to the finite turn-on time of the mosfets. This problem is further explained in Section 3.4.1.

In any case, now that we know which type of mosfet we are using to realize each switch, we look at the formula for the equivalent resistance of a mosfet working in the triode region, (under the long-channel approximation) which is as follows:

$$R_{\mathrm{on}} = \frac{1}{(\mu_{\mathrm{m}} C_{\mathrm{ox}})\,(W/L)\,(V_{\mathrm{GS}} - V_{\mathrm{TH}})} \tag{3.30}$$

As anticipated, we have that $R_{\mathrm{on}} \propto^{-1} W$, but we also notice that $R_{\mathrm{on}} \propto^{-1} (V_{\mathrm{GS}} - V_{\mathrm{TH}}) \simeq V_{\mathrm{GS}}$. This last relation is important since as seen in Figure 3.14 when $\phi_1 = 0V$, we have that SW_1 and SW_4 are ON as intended, but while $V_{\mathrm{GS1}} = -V_{\mathrm{IN}}$ we have that $V_{\mathrm{GS4}} \simeq -V_{\mathrm{OUT}} \simeq -V_{\mathrm{IN}}/2$. The same applies for switches SW_2 and SW_3 where $V_{\mathrm{GS2}} = V_{\mathrm{IN}}$ and $V_{\mathrm{GS3}} \simeq V_{\mathrm{OUT}} \simeq V_{\mathrm{IN}}/2$. Another issue that we have to consider is that μ_m changes if the mosfet is type-n or type-p. This ultimately means that for a set value of W each of the four switches will have different values of R_{on}.

We therefore have to size each mosfet individually, finding the values of $W_{\mathrm{SW,i}}$ that realize the needed value of R_{FSL} for both phases $\phi_{1,2}$, while minimizing the total value of $C_{\mathrm{gg,TOT}} = \sum_{i=1}^{4} C_{\mathrm{gg,i}}$ in order to contain the switching losses.

This problem can be formulated mathematically for a single phase ϕ_{i} as:

$$R_{\mathrm{FSL}} = \frac{R_{\mathrm{on,V_{GS}=0.4V}}}{W_{\mathrm{V_{GS}=0.4V}}} + \frac{R_{\mathrm{on,V_{GS}=0.8V}}}{W_{\mathrm{V_{GS}=0.8V}}} \tag{3.31}$$

$$\min\left(C_{\mathrm{gg,V_{GS}=0.4V}} \cdot W_{\mathrm{V_{GS}=0.4V}} + C_{\mathrm{gg,V_{GS}=0.8V}} \cdot W_{\mathrm{V_{GS}=0.8V}}\right) \tag{3.32}$$

where the values of $R_{\mathrm{on,V_{GS}=0.8V}}$, $R_{\mathrm{on,V_{GS}=0.4V}}$, $C_{\mathrm{gg,V_{GS}=0.8V}}$ and $C_{\mathrm{gg,V_{GS}=0.4V}}$ are normalized with respect to a fixed value of W_{REF} and can be estimated with the aid of simulation tools for both type-n and type-p mosfets. Moreover the values of $W_{\mathrm{V_{GS}=0.4V}}$ and $W_{\mathrm{V_{GS}=0.8V}}$ have to be seen as a scaling factor for W_{REF}. Therefore, for example, for a given $W_{\mathrm{V_{GS}=0.4V}}$ the real mosfet width is given by $W = W_{\mathrm{V_{GS}=0.4V}} \cdot W_{\mathrm{REF}}$.
We can then rewrite Equation 3.31 as:

$$W_{\mathrm{V_{GS}=0.4V}} = \frac{R_{on,\mathrm{V_{GS}=0.4V}} \cdot W_{\mathrm{V_{GS}=0.8V}}}{R_{\mathrm{FSL}} \cdot W_{\mathrm{V_{GS}=0.8V}} - R_{on\mathrm{V_{GS}=0.8V}}} \tag{3.33}$$

Plugging Equation 3.33 into Equation 3.32 we are left with a minimization problem with only one variable $W_{\mathrm{V_{GS}=0.4V}}$, which can easily be resolved by using derivatives and gives our final result:

$$W_{\mathrm{V_{GS}=0.8V}} = \frac{R_{on,\mathrm{V_{GS}=0.8V}} + \sqrt{\frac{C_{gg,V_{\mathrm{GS}=0.4V}}}{C_{gg,V_{\mathrm{GS}=0.8V}}} \cdot R_{on,\mathrm{V_{GS}=0.8V}} \cdot R_{on,\mathrm{V_{GS}=0.4V}}}}{R_{\mathrm{FSL}}} \tag{3.34}$$

$$W_{\mathrm{V_{GS}=0.4V}} = \frac{R_{on,\mathrm{V_{GS}=0.4V}} + \sqrt{\frac{C_{gg,V_{\mathrm{GS}=0.8V}}}{C_{gg,V_{\mathrm{GS}=0.4V}}} \cdot R_{on,\mathrm{V_{GS}=0.8V}} \cdot R_{on,\mathrm{V_{GS}=0.4V}}}}{R_{\mathrm{FSL}}} \tag{3.35}$$

Following this procedure we are able to optimally size the switches for a given target value of R_{FSL}.

3.2.2 Partial Charging

We have seen how, in order to size the converter, the constrain $4\tau = T_{\text{sw}}/2$ has been imposed. This choice has been taken in virtue of an effect called "partial charging". As seen in Figure 3.5 by varying the number n of allowed time constants for a semi period of the circuit ($n \cdot \tau = T_{\text{sw}}/2$) the behaviour of the output voltage ripple of the converter changes. This is equivalent to varying the ratio between R_{SSL} and R_{FLS} as seen in Equation 3.29.

From a design standpoint we want to keep the value of R_{FSL} comparable to R_{SSL} in order to avoid oversizing the mosfets, leading to an unnecessary increase in the switching losses. Partial charging however limits how big we can make the value of R_{FSL} in relation to R_{SSL}. If we don't allow enough time for the RC network to fully charge, we will in fact see an increase in the value of R_{OUT} by a factor of $1/\gamma$.
We have that γ is generally given by:

$$\gamma = \frac{1 - e^{\frac{-1}{2R_{\text{eq}}C_{\text{fly}}f_{\text{sw}}}}}{1 + e^{\frac{-1}{2R_{\text{eq}}C_{\text{fly}}f_{\text{sw}}}}} \tag{3.36}$$

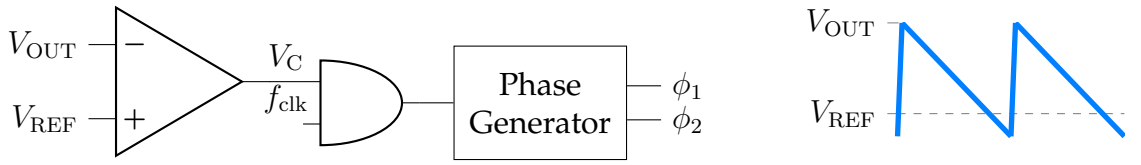
where $R_{\text{eq}} = 2R_{\text{on}} + R_{\text{ESR}}$. Under the condition of Equation 3.29 we have that Equation 3.36 gives $\gamma \simeq 1$, proving it to be a good compromise in the design of the converter[9]. In practical cases however we have that $\gamma \simeq 1$ if $f_{\text{sw}} < 1/\left(R_{\text{on}}C_{\text{fly}}\right)$ [5] and simulation data proves that even the condition $2\tau = T_{\text{sw}}/2$ doesn't see a meaningful deterioration of the value of R_{OUT}.

The effect of partial charging can be explained by considering that if the flying capacitor C_{fly} isn't fully charged, the converter effectively sees a smaller capacitor than the one that is actually present in the circuit. This causes an increase in R_{SSL} and in turn of R_{OUT} as explained above. At the same time however, since partial charging reduces the effective value of C_{fly} we have that the ratio $C_{\text{out}}/C_{\text{fly}}$ does too, leading to a decrease of ΔV_{ripple}. Partial charging therefore is beneficial in terms of decreasing the amount of ripple of the converter, however we can't allow R_{OUT} to increase too much as it will significantly impact the performance of the converter. This means that we have to pay close attention to the effect of γ during the sizing phase of the converter.

3.3 Output Voltage Control

Up to now we have considered the output current I_{OUT} required by the load as constant. In reality the current load can be considered, more generally, as a combination of a DC value I_{OUT} and an AC one $i_{\mathrm{out}}(t)$ giving $I_{\mathrm{out}} = I_{\mathrm{OUT}}(t) + i_{\mathrm{out}}(t)$. In our case the effect of $i_{\mathrm{out}}(t)$ can be seen as negligible. As the VCO changes its output frequency, during its operation, it leads however to a change in the value of I_{OUT}. This causes the value of V_{OUT} to change during the operation of the circuit. If I_{OUT} changes too much it may deteriorate the performance of the circuit, so a control technique has to be included in the converter. As we will see not all the control techniques are suitable for our application.

A popular control technique for switched capacitor converters is Pulse-frequency Modulation (PFM) where the output voltage is regulated by changing the switching frequency of the converter as the current changes, which can be implemented as showed in Figure 3.15 [9, 15].



(a) Single bound hysteretic control block diagram

(b) Voltage waveforms

Figure 3.15: Voltage control using PFM technique

In this technique we first compare the value of V_{OUT} with a reference value V_{REF} that we want the converter to track. When $V_{\mathrm{REF}} - V_{\mathrm{OUT}} > 0$ we have that the comparator output V_{C} goes high, enabling the AND port and letting the clock signal go to the converter. The flying capacitors are therefore able to bring charge to the output raising V_{OUT} over the reference. Once this happens and $V_{\mathrm{REF}} - V_{\mathrm{OUT}} < 0$ the clock signal is stopped and V_{OUT} slowly decreases as it gets consumed by I_{OUT} and then the cycle continues.

This technique has however a huge downside as it makes the output spectrum of the converter become of random nature since the switching frequency varies continuously without settling during the operation of the converter. This of course is a huge problem in RF systems, as seen in Section 1.6, therefore any kind of frequency modulation technique has to be avoided for our purposes.

A popular, fixed frequency, control technique is called Switch Width Modulation (SWM) where the width of the mosfets, and therefore their equivalent resistance R_{on}, is modulated allowing us to regulate R_{OUT} and V_{OUT}. In order to perform SWM we substitute every mosfet switch with a mosfet array realized by the parallel of b mosfets, where the size of each mosfet is binary weighted as shown in Figure 3.16.

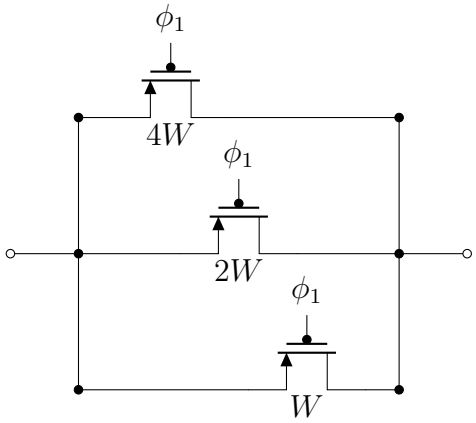


Figure 3.16: SWM principle

In this example we have an array of $b = 3$ mosfets, in parallel, of sizes W, $2W$ and $4W$. By turning ON or OFF the mosfets of the array, having different widths, we can achieve up to $2^b - 1$ equivalent resistance combinations, ranging from R_{on} to $R_{\text{on}}/\left(2^b - 1\right)$. This proves how by properly selecting the value of b we are able to finely regulate V_{OUT}. Note however that in the case where $R_{\text{SSL}} \simeq R_{\text{FSL}}$ we aren't able to fully modulate the value of R_{OUT} as it's held back by R_{SSL}. Nevertheless we have that with this implementation we are able to efficiently scale the switching losses when I_{OUT} changes. The width of the mosfets (and therefore the switching losses) are increased only when I_{OUT} increases, in order to keep V_{OUT} inside a certain range. On the other hand, for low loads we can use combinations with smaller widths reducing the switching losses. This however doesn't allow us to scale the top and bottom plate losses as we aren't changing the value of C_{fly} during operation and the flying capacitor remains the same for all values of I_{OUT}. Another problem lies in how the time constants of the converter τ change during operation as a result of the modulation of the switch width, leading to a deterioration of the behaviour of the ripple across different loads. SWM therefore seems like a promising technique for our application, but with some caveats that need to be solved if we want to preserve the efficiency of the circuit across a wider range of values of I_{OUT}.

3.3.1 Digital Capacitance Modulation

The technique that we are going to use to control the output voltage of the converter, is therefore an evolution of SWM and its called Digital Capacitance Modulation (DCM) [12]. In DCM as it could be guessed by our previous discussion, we also modulate the size of the capacitor C_{fly}, together with the switch width of the mosfets. This allows us to scale both the switching and top/bottom plate losses, while ensuring that the time constant of the circuit τ stays the same during operation. Of course DCM comes at the cost of a greater design complexity than solutions like PFM or SWM.

The switch and capacitance modulation of DCM is realized by making b converters modules, having their components scaled following binary weights, work in parallel. The combination of modules used are expressed by the vector $c = [c_0 c_1 ... c_b]$ where the coefficients c_i are either equal to 1 if the i-th module partecipates to the charge/discharge process or 0 if it doesn't. For instance for $b = 4$ the vector $c = [1111]$ corresponds to a converter using all of its modules, while for $c = [0001]$ it employs only its smallest module, corresponding to the least significant bit. A converter example for $b = 4$ is shown in Figure 3.17.

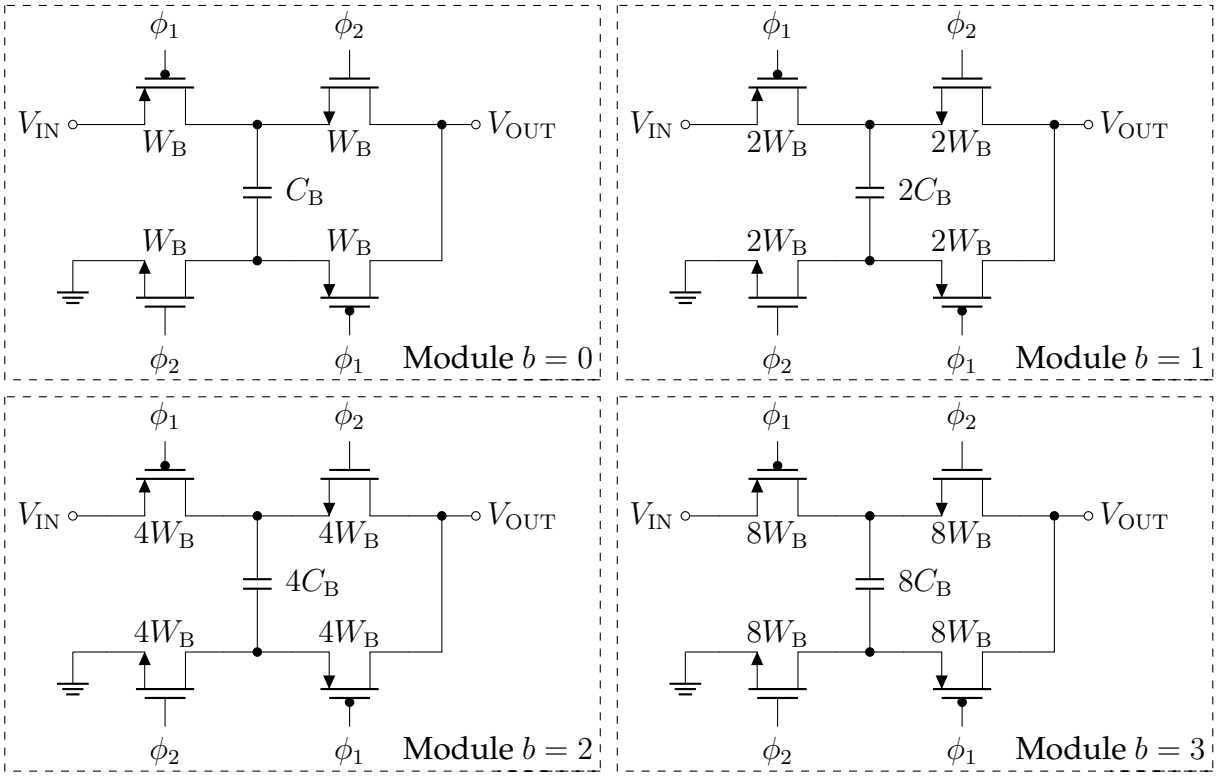


Figure 3.17: DCM converter scheme for $b = 4$

Note that each module is obtained by scaling up the smallest module having $C_{\mathrm{B}} = C_{\mathrm{fly}}/(2^b - 1)$ and $W_{\mathrm{B}} = W/(2^b - 1)$ by using powers of 2. The formula for the output resistance of the converter therefore becomes:

$$R_{\mathrm{OUT_{DCM}}} = \frac{R_{\mathrm{OUT}}}{2^b - 1} \sum_{n=0}^{b} c_{\mathrm{i}} \cdot 2^n \tag{3.37}$$

where R_{OUT} represents the output resistance of the converter before applying DCM. Equation 3.37 clearly shows how the output resistance of the converter can be scaled using this technique. The equivalent scheme of a converter employing DCM is shown in Figure 3.18.

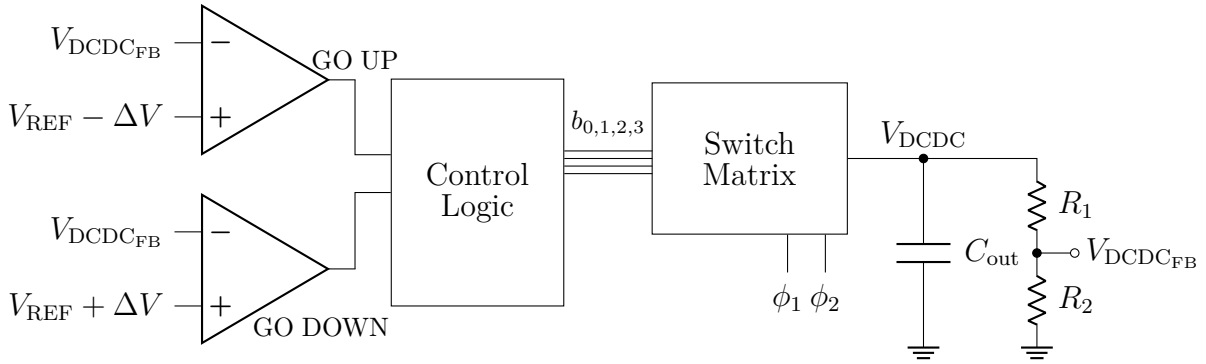


Figure 3.18: Equivalent scheme of a converter employing DCM

We see from Figure 3.18 how the output voltage of the SC converter is compared to two thresholds to understand if the number of active modules has to be adjusted. If the output voltage is inside the limits, then the structure of the converter stays the same. On the other hand, if one of the thresholds is crossed, the number of modules participating to charge/discharge is modified. The modules of the converter are progressively turn on or off following a digital counter. If the upper threshold is crossed the counter will begin counting down decreasing the number of modules used. In this case the converter may employ only the module associated to the least significant bit for very light loads. As suggested in [12] an additional logic may be included in this last case to allow PFM to regulate the converter if needed, since this condition usually means that the circuit is partially turned off and we can ignore the spurs produced by the PFM. On the other hand, if the lower threshold is crossed the counter will count up, increasing the number of modules. Note that in presence of high loads the converter, even employing all of its modules, might not be able to control the voltage inside of the boundaries.

3.4 Additional Circuits

In this section we are going to briefly analyse some additional circuits that are fundamental for the correct behaviour of the converter.

3.4.1 Non Overlapping Clock Generator

Due to the finite turn-on time of real mosfets phases ϕ_1 and ϕ_2 cannot be switched at the same time. Doing so will in fact create a time interval Δt, for which all of the switches of the converter are ON, creating a low resistance path from V_{DD} to V_{out}. This creates a surge of current called "Shoot-Through", which deteriorates the operation of our converter and can also lead to damage to the components. In order to avoid this problem, phases are generated by using a Non-Overlapping Clock (NOC) generator, which inserts a "dead-time" between the phases where all the switches of the circuit are OFF. The schematic of the circuit is showed in Figure 3.19 while the generated phases are showed in Figure 3.20.

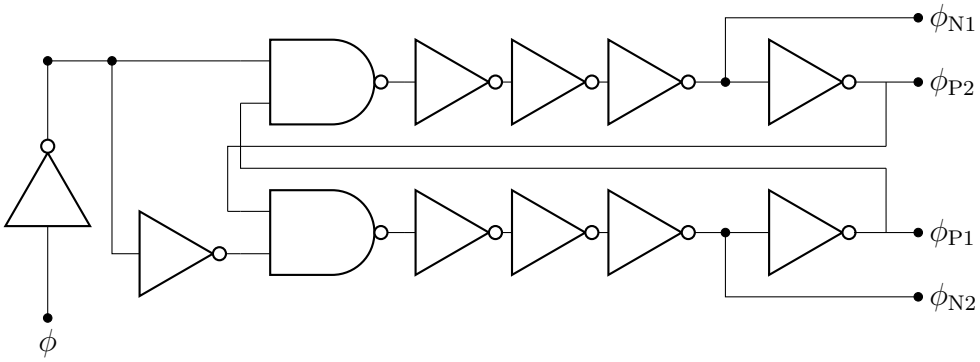
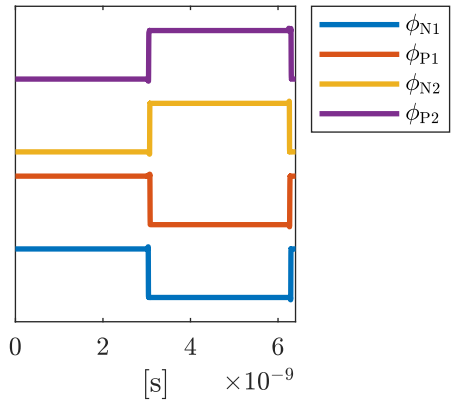
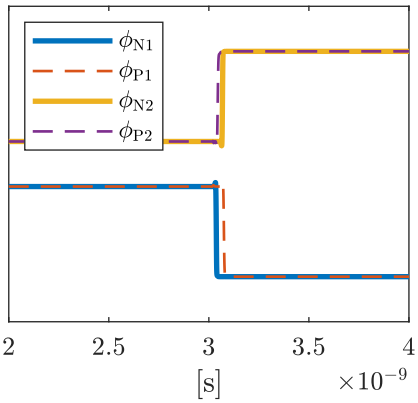


Figure 3.19: Circuit scheme of a NOC generator



(a) Phases generated by the NOC viewed separately



(b) Phases generated by the NOC grouped in pairs

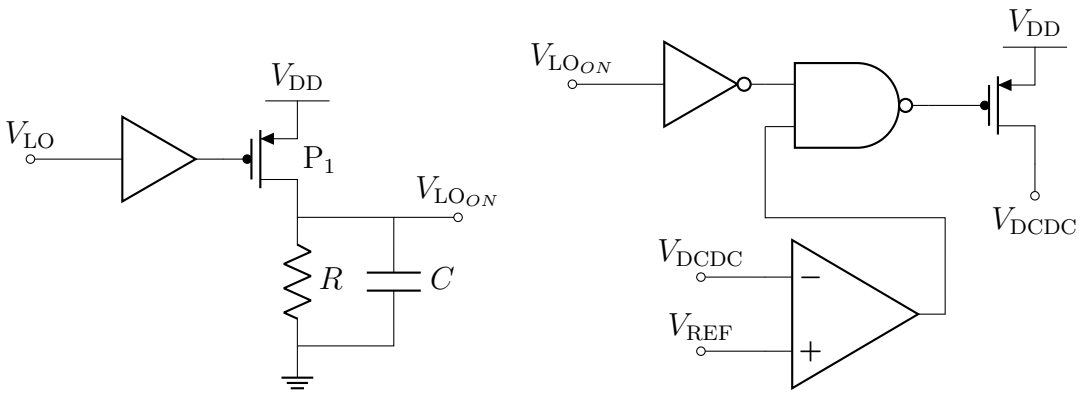
Figure 3.20: Phases generated by a NOC circuit

The reported NOC circuit can be fed with a periodic waveform at frequency f_{sw} and it will generate 2 pair of phases, $\phi_{1/2}$ and $\phi'_{1/2}$ where each pair of phases is in opposition of phase with the other. This makes the circuit useful for generating the driving signal for a symmetric converter. Note however that the phases $\phi_{1/2}$ and $\phi'_{1/2}$ cannot be directly fed to the gate of the mosfets, but a chain of inverters has to be used to drive the big gate capacitance of the switches.
By acting on the delay of the inverter chain of the NOC generator we are capable of adjusting the dead time of the phases, which can be observed in Figure 3.20. Note that while dead time has to be chosen in a way that avoids "Shoot-Through" it must not be excessively longer than needed. Leaving all the switches turned OFF, means in fact that the converter is not working as it should and this too can have an impact on the operation of the converter if the dead time starts to be comparable with the period of f_{sw}. This is also one of the reasons, besides the presence of switching losses, which makes power switching operation at high frequency such a difficult task as it becomes increasingly difficult to keep the dead time negligible with respect to the phases period.

3.4.2 Start-Up Circuit

In order to make the initial transient of the converter faster, most SC converters employ a start-up circuit that creates a temporary bypass path between V_{DD} and the output node of the converter [9]. In our case this operation is more crucial than ever. Since we want to use the output signal of the oscillator to generate the switching signal for our converter, we have than the initial transient of the circuit becomes quite tricky. The oscillator in fact needs a supply voltage to oscillate, but that same supply voltage in order to be delivered by the SC converter requires the oscillator to be working. This is because without the signal f_{sw} the converter can't transfer charge to its output terminal. In order to solve this dilemma a start-circuit has to be realized.

The circuit, as anticipated, creates a bypass path between V_{DD} and the output node of the converter V_{DCDC} until it reaches a certain value V_{REF} set to be lower than the steady state value of the output voltage. This allows the oscillator to start oscillating, feeding f_{sw} to the SC converter which can then start to transfer charge to its output node and bringing the circuit to steady state. The start-up circuit is showed in Figure 3.21.



(a) Detection of V_{LO} (b) Start-Up logic and bypass of the converter

Figure 3.21: Start-Up circuit scheme

As can be observed in Figure 3.21a the start-up circuit contains a block that resembles a peak detector. The output voltage V_{LO} of the oscillator is in fact used to drive a mosfet P_1 that charges an RC network, with a bigger time constant than the period of the oscillating frequency f_0. If the VCO is oscillating the value of $V_{\mathrm{LO}_{ON}}$ will therefore quickly set to a steady state value of $\simeq V_{DD}$, if we assume the voltage drop on P_1 to be negligible. $V_{\mathrm{LO}_{\mathrm{ON}}}$ can then be used as a logic value in the circuit showed in Figure 3.21b. The logic of the start-up circuit therefore will enable the bypass path only if the VCO is not oscillating and the value of the voltage V_{DCDC} is below a certain threshold, that in our case has been fixed to $V_{\mathrm{REF}} = 300\mathrm{mV}$.

CHAPTER 4

Circuit Design and Simulation

In this chapter some possible design solutions for a DC/DC powered Class-D VCO are presented. The design has been made with the aid of the simulation tools, provided by the software Cadence ®Virtuoso ®. The technology node used is that of 22nm FDSOI. The power supply voltage is of $V_{\mathrm{DD}} = 0.8\mathrm{V}$. The VCO therefore is going to be powered by a $2:1$ SC converter, providing a maximum voltage of $V_{\mathrm{MAX}} = 0.4\mathrm{V}$.

4.1 Design of a Class-D VCO

We start from the design of the VCO, in order to understand what its current consumption I_{DC} will be. This will allow us to later size the SC converter accordingly. We note that in this first phase, it's important to limit the value of I_{DC} as much as possible, to retain a good level of efficiency later in our design.

Note that in order to be able to compare, more effectively, the performance of our SC powered Class-D VCO with other designs, we are going to realize a VCO with similar specifications to the ones used in [3]. Our VCO therefore will have a frequency range between $2.5\mathrm{GHz}$ and $3.3\mathrm{GHz}$, corresponding to a tuning range of 27.5%, and will employ a $6\ bit$ capacitor bank.

For sizing the inductor, which is going to be used by the Class-D oscillator, we look at the formulas for current consumption of Equation 2.28 and Equation 2.29. We notice how $I_{\mathrm{DC}} \propto^{-1} L$ and $I_{\mathrm{DC}} \propto^{-1} f_0$. This means that, for a fixed value of L, the minimum current consumption of the VCO happens when its working near its maximum oscillation frequency $3.3\mathrm{GHz}$. On the other hand, the maximum current consumption

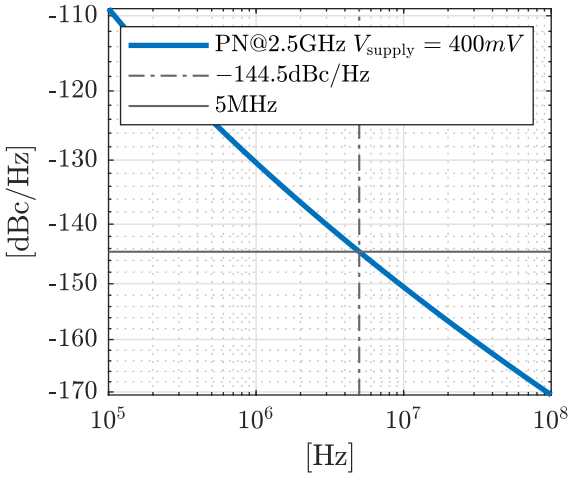
happens when it is operating close to its minimum oscillation frequency $2.5\mathrm{GHz}$. Moreover by increasing the size of L, if its quality factor Q_{L} doesn't vary too much across the VCO range, we are able to reduce the value of I_{DC}, across all the frequency range. We therefore purposely select a big value for the inductor of $L = 1.1\mathrm{nH}$, which is one of the biggest allowed by the technology.

Next, we move on to the sizing of transistors M_1 and M_2, which, as anticipated, have to made as big as possible. We note that, due to the Class-D high oscillation amplitude of $\simeq 3V_{\mathrm{DD}}$, the maximum voltage on the terminals of the switches is of $\simeq 1.2\mathrm{V}$. This means that to avoid damage to the components, the transistor length cannot be the minimum length allowed by the technology $L = 18\mathrm{nm}$, but instead have to be of $L = 70\mathrm{nm}$. The switches are implemented using super low V_{TH} devices. The total width of each device is of $W = 1.44\mathrm{mm}$, with a W/L ratio of $\simeq 20570$.

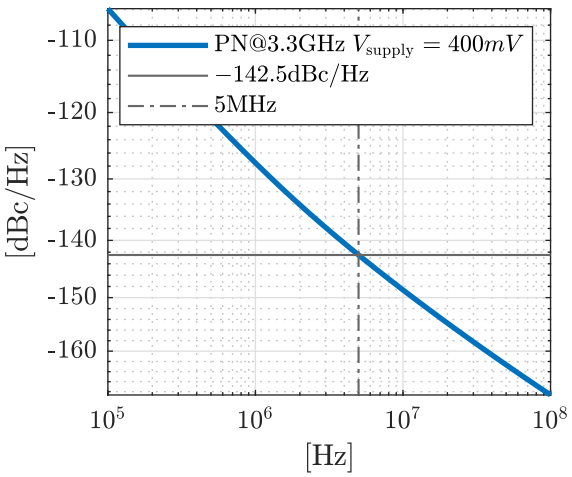
Finally we report the values used for the capacitor bank. A small floating capacitor of $C_{\mathrm{float,fixed}} \simeq 189\mathrm{fF}$ is employed in parallel to the bank. $C_{\mathrm{float,fixed}}$ guarantees a small amount of floating capacitance even at the highest oscillation frequency, where the capacitor bank is disconnected from the circuit. The bank on the other hand employs a total switchable floating capacitance of $\simeq 2.28\mathrm{pF}$. More specifically the switchable floating capacitance, of the least significant bit, is of $C_{bit0} = 37.5\mathrm{fF}$. The following capacitors are therefore scaled correspondingly, following a progression of powers of 2, however the bigger capacitors are slightly smaller than needed, to take into account the effect of the parasitic capacitance introduced by the switches. We have therefore:$C_{bit1} = 75\mathrm{fF}$, $C_{bit2} = 150\mathrm{fF}$, $C_{bit3} = 296\mathrm{fF}$, $C_{bit4} = 582\mathrm{fF}$, $C_{bit5} = 1.138\mathrm{pF}$. A small varactor is used to provide continuous capacitance tuning, between the values provided by the switchable capacitor bank. The size of each switch on the other hand doesn't follow a progression of powers of 2 for the bigger switches. This is to try to limit the effect of the parasitic capacitance of the switches. The reasoning behind this is that when capacitance is switched in, the oscillation frequency decreases leading to an increase in the quality factor of the capacitor bank. This allows us to contain the width of the switches, but in a way that doesn't affect the quality factor of the capacitor array. The following progression for the switches is therefore used: $W_{bit0} = 49\mu\mathrm{m}$, $W_{bit1} = 2W_{bit0}$, $W_{bit2} = 4W_{bit0}$, $W_{bit3} = 7W_{bit0}$, $W_{bit4} = 11W_{bit0}$, $W_{bit5} = 16W_{bit0}$.

4.1.1 Simulation of the VCO

The operation of the VCO is simulated at its frequency extremes first with a supply voltage of $V_{\text{supply}} = 0.4$ corresponding to the maximum supply voltage that the SC converter can deliver. A second simulation is made with $V_{\text{supply}} = 0.35$ corresponding to a more realistic value of V_{supply} due to the finite output resistance of the SC converter. The results are summarized and compared to [3] in Table 4.1, while the plots of phase noise for $\Delta\omega = 100\text{kHz} - 100\text{MHz}$ are reported in Figure 4.1 for $V_{\text{supply}} = 0.4$ and in Figure 4.2 for $V_{\text{supply}} = 0.35$.

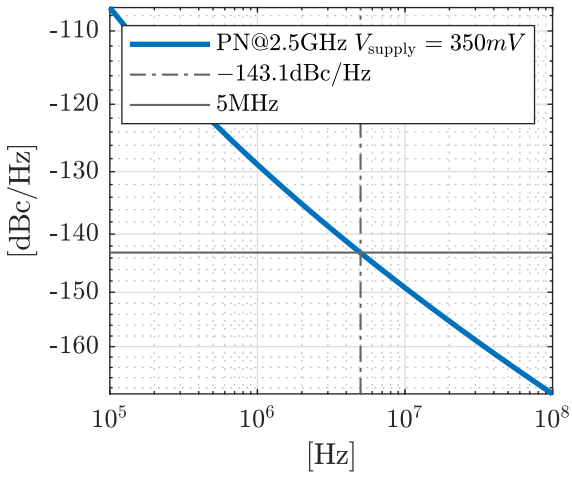


(a) PN of the VCO with $f_0 = 2.5\text{GHz}$ at $\Delta\omega = 5\text{MHz}$

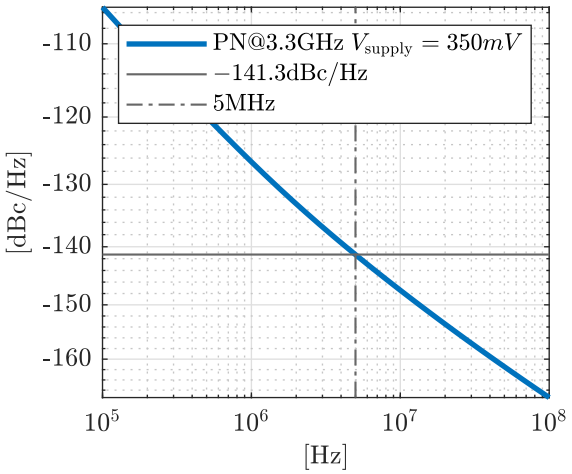


(b) PN of the VCO with $f_0 = 3.3\text{GHz}$ at $\Delta\omega = 5\text{MHz}$

Figure 4.1: PN of the VCO at its oscillation frequency extremes for V_{supply}= 400mV



(a) PN of the VCO with $f_0 = 2.5\text{GHz}$ at $\Delta\omega = 5\text{MHz}$



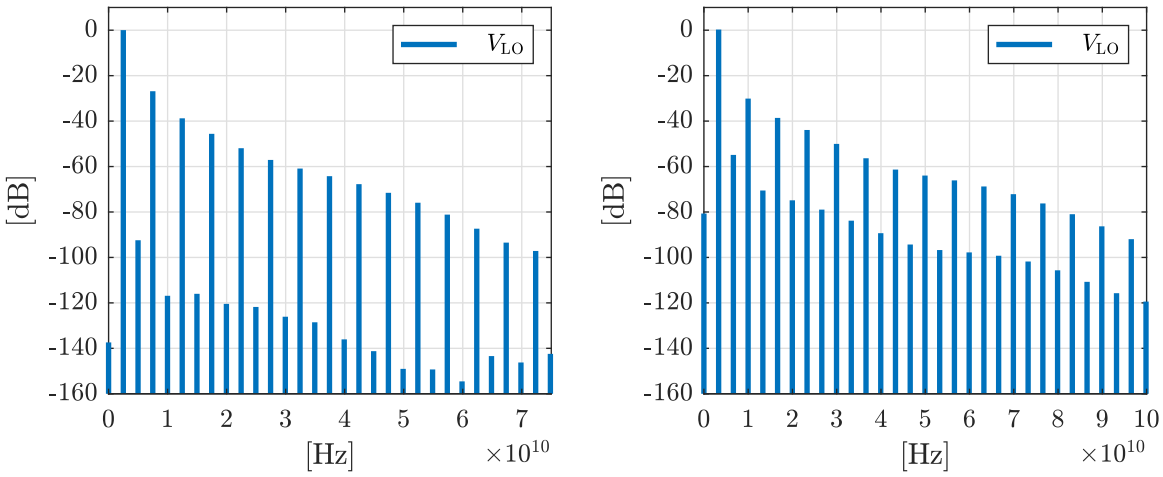
(b) PN of the VCO with $f_0 = 3.3\text{GHz}$ at $\Delta\omega = 5\text{MHz}$

Figure 4.2: PN of the VCO at its oscillation frequency extremes for V_{supply}= 350mV

	$\mathcal{L}(\Delta\omega)$	I_{DC}	FoM
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 2.5\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.4\mathrm{V}$	$-144.5\mathrm{dBc/Hz}$	$14.4\mathrm{mA}$	190.9
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 3.3\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.4\mathrm{V}$	$-142.5\mathrm{dBc/Hz}$	$8.4\mathrm{mA}$	193.6
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 2.5\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.35\mathrm{V}$	$-143.1\mathrm{dBc/Hz}$	$12.4\mathrm{mA}$	190.7
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 3.3\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.35\mathrm{V}$	$-141.3\mathrm{dBc/Hz}$	$7.2\mathrm{mA}$	193.6
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 2.5\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.4\mathrm{V}$ [3]	$-144\mathrm{dBc/Hz}$	X	189/190
$\Delta\omega = 5\mathrm{MHz}$ $f_0 = 3.3\mathrm{GHz}$ $V_{\mathrm{supply}} = 0.4\mathrm{V}$ [3]	$-140.5\mathrm{dBc/Hz}$	X	189/190

Table 4.1: Simulation results for PN and I_{DC} with ideal power supply

The spectrum of the VCO at $f_0 = 2.5\mathrm{GHz}$ and $f_0 = 3.3\mathrm{GHz}$ for $V_{\mathrm{supply}} = 0.35\mathrm{V}$ is reported in Figure 4.3. We notice how the even harmonics are less attenuated in Figure 4.3b, which might be due to some errors either in the simulation or in the VCO design. In any case the main results of this work aren't undermined by this issue.

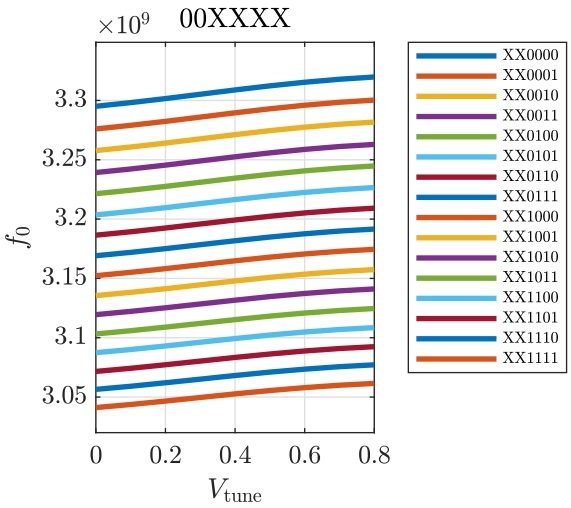


(a) Spectrum for $f_0 = 2.5\mathrm{GHz}$

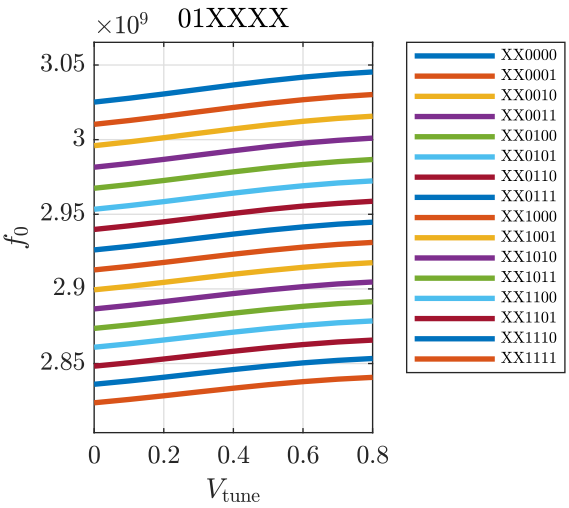
(b) Spectrum for $f_0 = 3.3\mathrm{GHz}$

Figure 4.3: Output spectrum of the VCO for ideal power supply

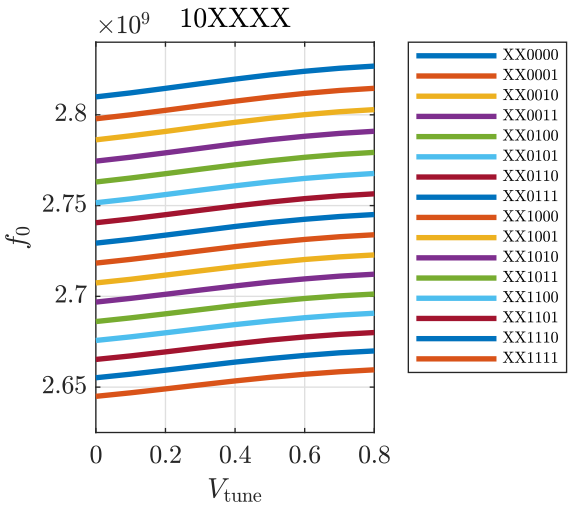
The tuning range is tested for every bank combination and plotted in Figure 4.4 where it has been divided based on the 2 most significant bits of the bank. In Figure 4.5, on the other hand, the whole tuning range has been plotted together. We note that as we switch in more capacitance to reduce the VCO oscillation frequency, we are making the tank capacitor approach more and more the behaviour of a floating capacitance, as intended to preserve PN. However since a floating capacitance allows for higher oscillation frequency this conflicting behaviour results in a deterioration of the tuning range for the VCO. This can be observed in Figure 4.5 where the curves related to the highest value of the capacitance bank, 11XXXX, are closer to each other and cover a smaller frequency range compared to the curves of 00XXXX.



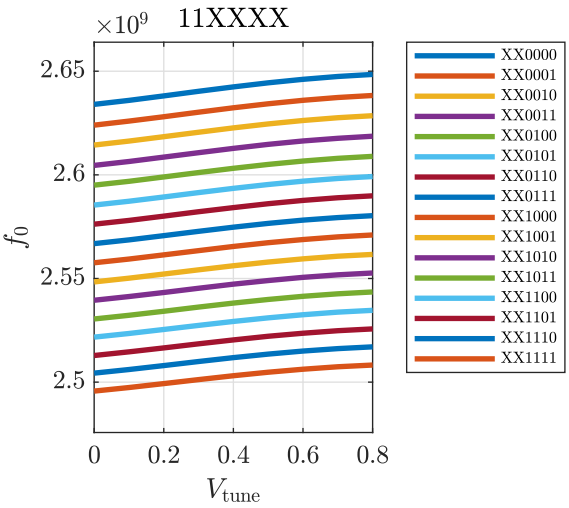
(a) Tuning range of the VCO for bank combinations: 00XXXX



(b) Tuning range of the VCO for bank combinations: 01XXXX



(c) Tuning range of the VCO for bank combinations: 10XXXX



(d) Tuning range of the VCO for bank combinations: 11XXXX

Figure 4.4: Tuning range of the VCO

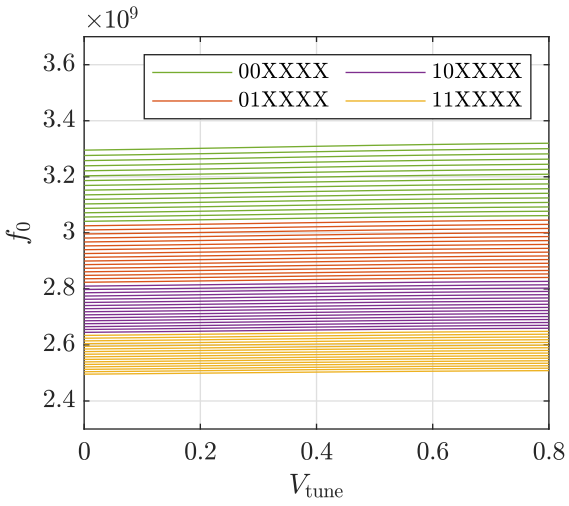
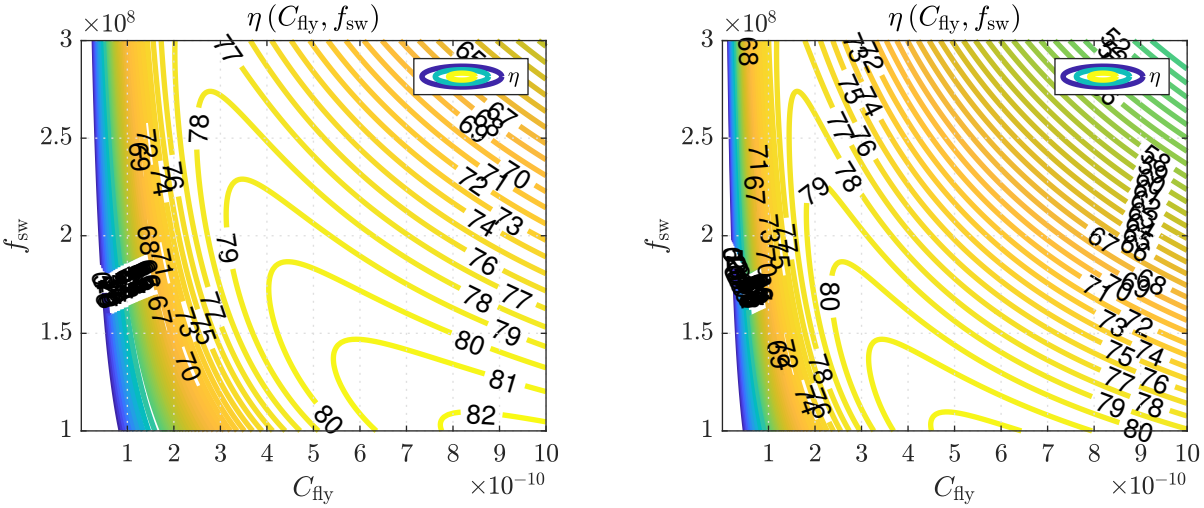


Figure 4.5: Tuning range of the VCO - All curves together

4.2 Design of the SC Converter

We now want to design a symmetric SC converter that is going to power our Class-D VCO. In order to do so we have to remember that the switching signal, needed to drive the SC converter, is going to be obtained by dividing the output of the VCO by a suitable number of frequency dividers. This means that $f_{\text{sw}} = f_0/2^N$, with N the number of dividers used. For our case $N = 4$ is a good trade off as it allows us to sufficiently scale C_{fly}, while preserving the efficiency. Considering the case when the VCO is at its lower oscillation frequency extreme, for $f_0 = 2.5\text{GHz}$, the switching frequency would then be $f_{\text{sw}} \simeq 156\text{MHz}$ with $N = 4$. On the other hand for the upper frequency extreme, $f_0 = 3.3\text{GHz}$, the switching frequency would be $f_{\text{sw}} \simeq 206\text{MHz}$ with $N = 4$.

Using the loss model developed in Chapter 3, and assuming to allow 4 time constants τ, for the design of a symmetric converter, we get the plots reported in Figure 4.6. Note that in Figure 4.6a we have assumed the case where the VCO operates at $f_0 = 2.5\text{GHz}$ providing a load current of $I_{\text{DC}} = 12.4\text{mA}$, while for Figure 4.6b we have assumed that it operates at $f_0 = 3.3\text{GHz}$ with a load current of $I_{\text{DC}} = 7.2\text{mA}$.



(a) $f_0 = 2.5\text{GHz}$, $I_{\text{DC}} = 12.4\text{mA}$

(b) $f_0 = 3.3\text{GHz}$, $I_{\text{DC}} = 7.2\text{mA}$

Figure 4.6: Efficiency as a function of f_{sw} and C_{fly} fixing 4 time constants τ

We select the value of $C_{\text{fly}} = 500\text{pF}$, which represent the total flying capacitance used by the converter. Since the converter is going to be symmetric, each module will use 250pF of flying capacitance. This choice of C_{fly} has been made since it allows for a maximum efficiency of approximately 80% for $f_{\text{sw}} \simeq 156\text{MHz}$, as seen in Figure 4.6a. Note that for the same value of C_{fly} in Figure 4.6b the efficiency is degraded if the VCO works

near its upper frequency extreme, $f_{\text{sw}} \simeq 206\text{MHz}$, with a load current $I_{\text{DC}} = 7.2\text{mA}$. This is because for lighter loads the power delivered to the load P_{OUT} decreases with I_{DC}. Furthermore, since $P_{\text{switching}}$ dominates the efficiency of the converter and is independent from the load current, if P_{out} decreases the ratio between $P_{\text{switching}}$ and P_{out} becomes larger causing the efficiency of the converter to decrease. However looking at Figure 4.6b we see how for $C_{\text{fly}} = 250\text{pF}$ efficiency is again near 80% for $f_{\text{sw}} \simeq 206\text{MHz}$. This demonstrates the importance that DCM will later have on the efficiency of the converter, as it will allow to dynamically scale $P_{\text{switching}}$ as the load changes.

Next, we can plot the efficiency, as a functions of R_{FSL} and f_{sw}, together with a function that tells us the number of time constants allowed by the RC network of the converter. Looking at Figure 4.7 we can try to understand what is a good design point for our converter. (Note that R_{FSL} refers to the target value of one single module.)

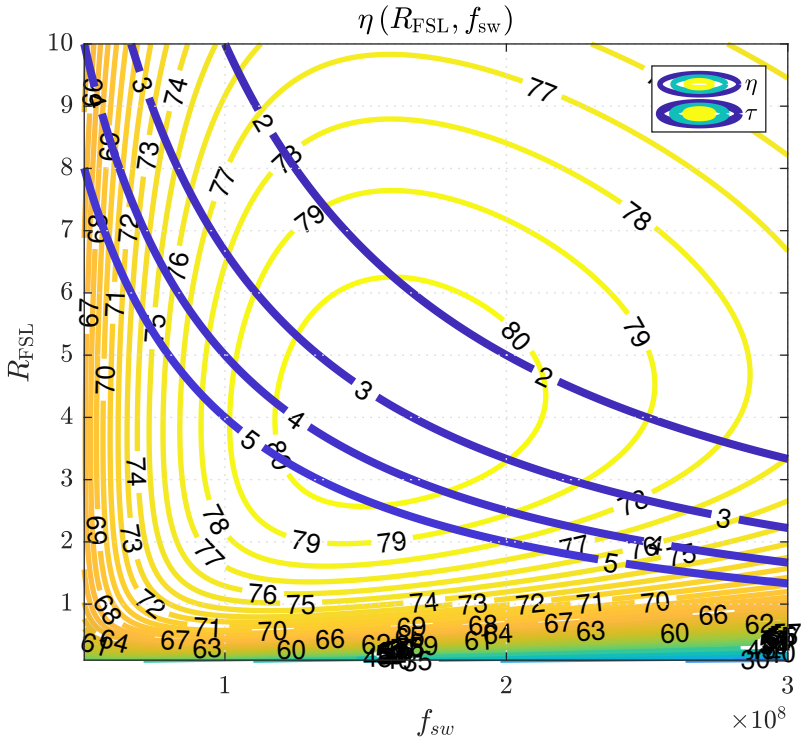


Figure 4.7: Efficiency as a function of f_{sw} and R_{FSL}

By allowing four time constants τ for $f_{\text{sw}} \simeq 156\text{MHz}$ we obtain $R_{\text{FSL}} \simeq 3.2$. Note that this means that the converter will allow $\tau \simeq 3$ for $f_{\text{sw}} \simeq 206\text{MHz}$. We can therefore proceed to size the mosfets and verify our design following the procedure of Section 3.2.1. Note that, contrary to the case of the VCO, the maximum voltage applied on the switches of the SC converter is $V_{\text{DD}} = 0.8V$. We can therefore use the minimum length allowed by the technology of $L = 18\text{nm}$.

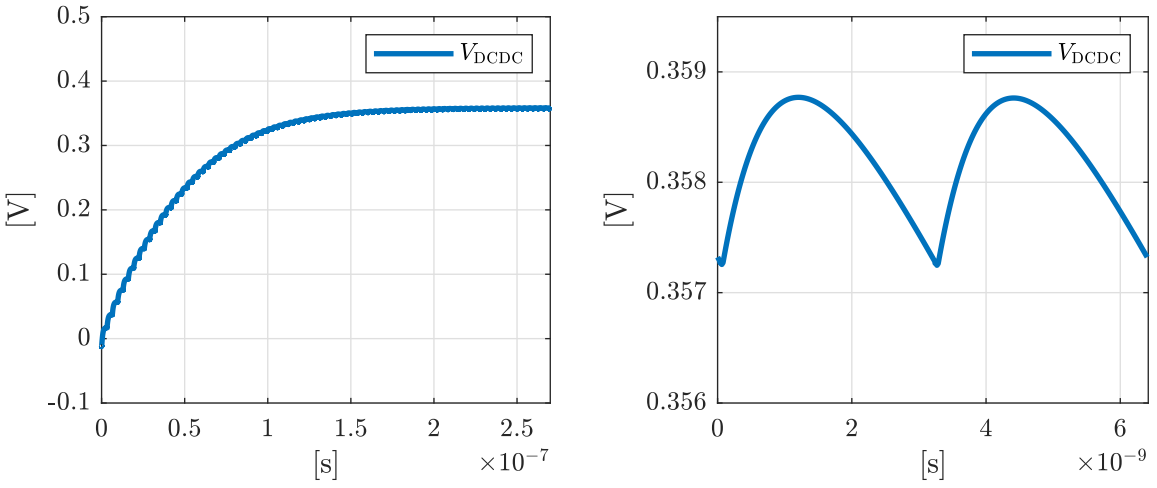
The mosfet widths obtained, for a module of a symmetric converter, are reported in Table 4.2

	$V_{GS} = 0.8$	$V_{GS} = 0.4$
NMOS	$218\mu m$	$365\mu m$
PMOS	$263\mu m$	$504\mu m$

Table 4.2: Mosfet Sizing

4.2.1 Simulation of the SC Converter

The SC converter is simulated, to verify its efficiency, using a large output capacitance $C_{\text{out}} = 10\text{nF}$. We first consider the case of a converter working with $f_{\text{sw}} = 156\text{MHz}$ and ideal current load of $I_{\text{DC}} = 12.4\text{mA}$. A plot of the initial transient of the SC converter is first shown in Figure 4.8a, together with the steady state waveform of the output voltage of the converter V_{DCDC} for one period T_{sw} in Figure 4.8b.



(a) Initial transient of the SC converter

(b) Steady state output voltage waveform of the SC converter

Figure 4.8: Simulation of the SC converter with $C_{\text{out}} = 10\text{nF}$, $f_{\text{sw}} = 156\text{MHz}$ and ideal load current $I_{\text{DC}} = 12.4\text{mA}$

The average value of V_{DCDC}, which can be obtained from Figure 4.8b, is of 357.7mV. This is in line with what we expect from the theory. The symmetric converter is in fact realised by 2 modules each one with $R_{\text{FSL}} = 3.2\Omega$ and $R_{\text{SSL}} = 6.4\Omega$, following Equation 3.29. The resistance of the parallel of the converters is therefore of $R_{\text{OUT}} \simeq 3.58\Omega$. By following Equation 3.3 we get a matching theoretical value of $V_{\text{DCDC}_{\text{TH}}} = 0.356\text{V}$. The ripple of V_{DCDC} on the other hand is $\Delta V_{\text{ripple}} = 1.5\text{mV}$, while Equation 3.17 gives $\Delta V_{\text{ripple}_{\text{TH1}}} \simeq 3.9\text{mV}$ and Equation 3.18 leads to $\Delta V_{\text{ripple}_{\text{TH2}}} = 2.1\text{mV}$. This further proves

that, since the converter is operating allowing only 4 time constants, the impulse charging approximation is no longer valid and the previously derived equations have to be considered as upper bounds.

The simulations results regarding the converter efficiency are listed in Table 4.3. Simulation has been carried out for values corresponding to the extremes of operation of the VCO showing a great correlation with the results predicted by our theoretical model. In particular the efficiency of the converter drops, as shown in Figure 4.6b, when the VCO oscillates at 3.3GHz, corresponding to operation of the converter for $f_{\text{sw}} = 206\text{MHz}$ and $I_{\text{DC}} = 7.2\text{mA}$. Note that if the load current is raised to $I_{\text{DC}} = 12.4\text{mA}$ the efficiency of the converter increases since the ratio $P_{\text{out}}/P_{\text{switching}}$ does too.

	η_{SIM}	η_{TH}
$f_{\text{sw}} = 156\text{MHz}$ $I_{\text{DC}} = 12.4\text{mA}$.	80.2%	80.6%.
$f_{\text{sw}} = 206\text{MHz}$ $I_{\text{DC}} = 12.4\text{mA}$.	79.4%	79.8%
$f_{\text{sw}} = 206\text{MHz}$ $I_{\text{DC}} = 7.2\text{mA}$.	75.35%	75.7%

Table 4.3: Efficiency Simulation

4.3 Simulation of the SC Powered Class-D VCO

We can therefore proceed to simulate the SC powered Class-D VCO, using the VCO and the SC converter that we have previously designed, with a value of $C_{\text{out}} = 10\text{nF}$. A block diagram of the simulated circuit is shown in Figure 4.9.

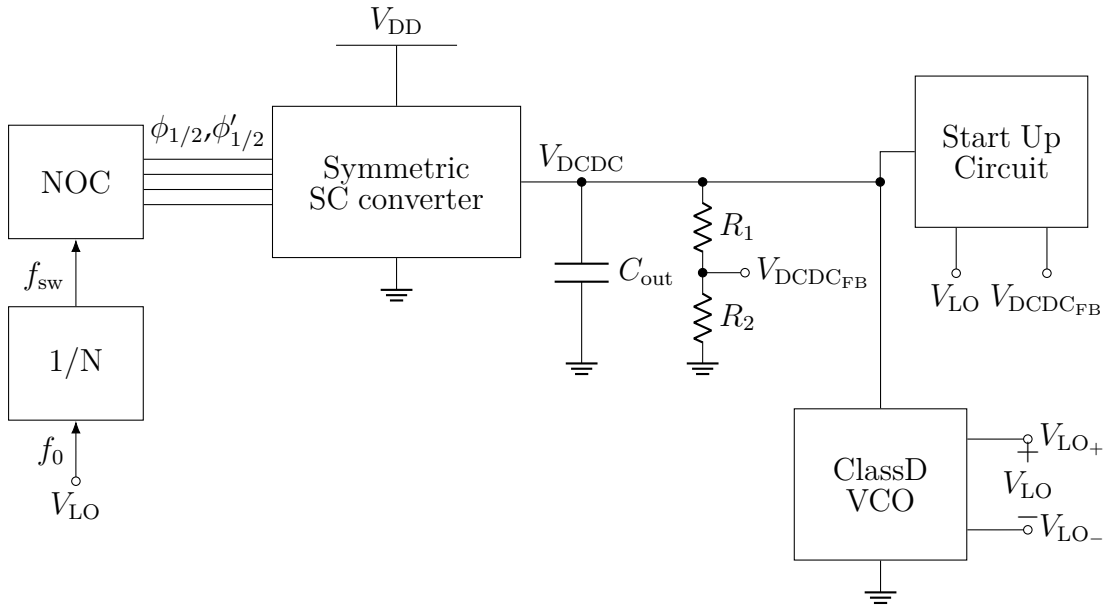
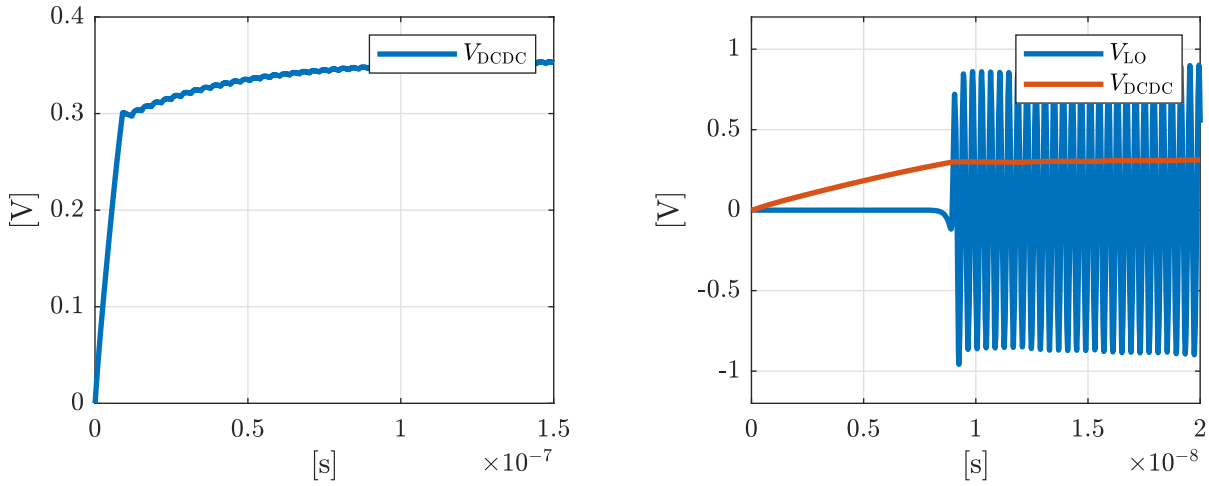


Figure 4.9: Block diagram of the SC powered Class-D VCO

As seen in Figure 4.9 the output of the SC converter is directly connected to the Class-D VCO, meaning that the voltage at the center tap of the Class-D inductor is the output voltage of the SC converter V_{DCDC}. Additionally the output voltage of the oscillator V_{LO} is used to feed a frequency divider, with divide ratio $N = 16$, that then feeds the NOC generator providing the phases for the converter. Finally the startup circuit is connected to V_{DCDC}, taking as an input V_{LO}, to check if the VCO is oscillating, and a scaled version of V_{DCDC} to verify its current value and eventually help to charge C_{out}.

In Figure 4.10 we report the transient simulation of the output of the SC V_{DCDC} converter and of V_{LO}, the differential output of the VCO. We see from Figure 4.10a how the startup circuit swiftly brings V_{DCDC} to the reference voltage of $V_{\mathrm{REF}} = 0.3\mathrm{V}$. At this point, since the threshold voltage has been reached, the bypass path between V_{DD} and V_{DCDC} is opened. However, the VCO hasn't started oscillating yet and can't feed f_{sw} to the converter. The value of V_{DCDC} therefore starts to decrease as C_{out} discharges. This leads V_{DCDC} to cross again $V_{\mathrm{REF}} = 0.3\mathrm{V}$ leading the bypass path to be closed once more. The charging and discharging of C_{out} leads to an unbalance at the nodes of the VCO, which causes the VCO to oscillate, as seen in Figure 4.10b.

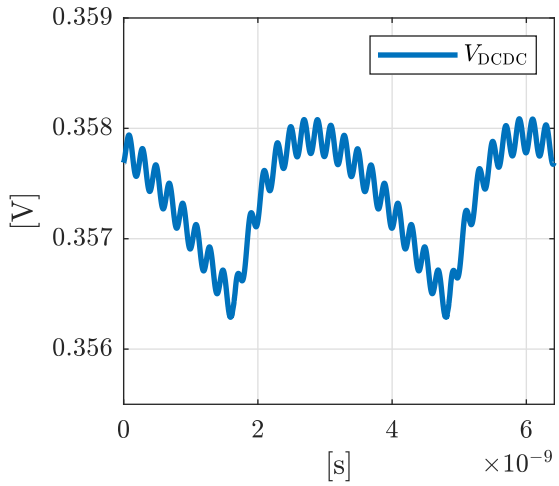


(a) Initial Start-Up transient for V_{DCDC}

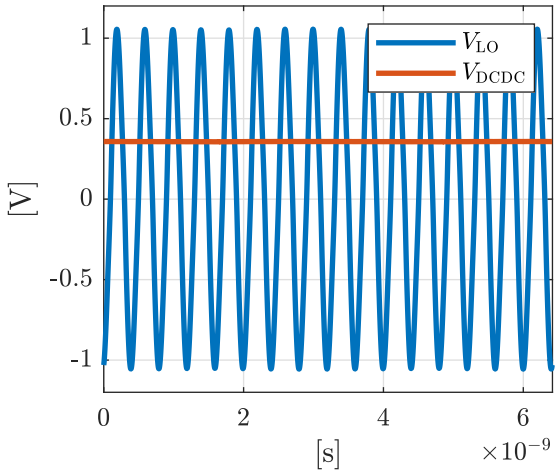
(b) Initial Start-Up transient for V_{DCDC} and V_{LO}

Figure 4.10: Transient simulation of V_{DCDC} and V_{LO}

Once the VCO starts oscillating, the SC converter begins to receive the phases from the NOC circuit and charge starts to be transferred from the supply to the node V_{DCDC} charging as a result C_{out}, until steady state is reached. The steady state voltage waveforms, of V_{DCDC} and V_{LO}, for a period of $f_{\mathrm{sw}} \simeq 156\mathrm{MHz}$, are reported in Figure 4.11.



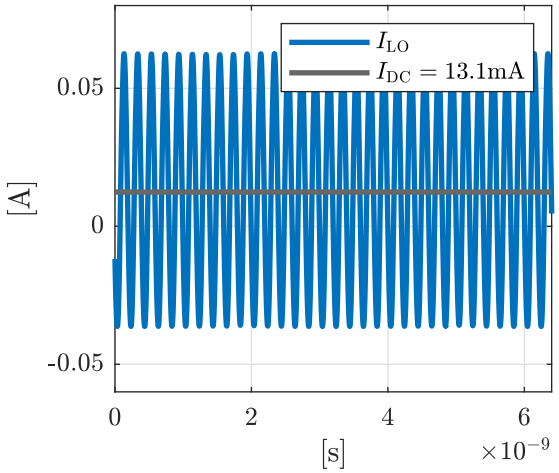
(a) Ripple of V_{DCDC}



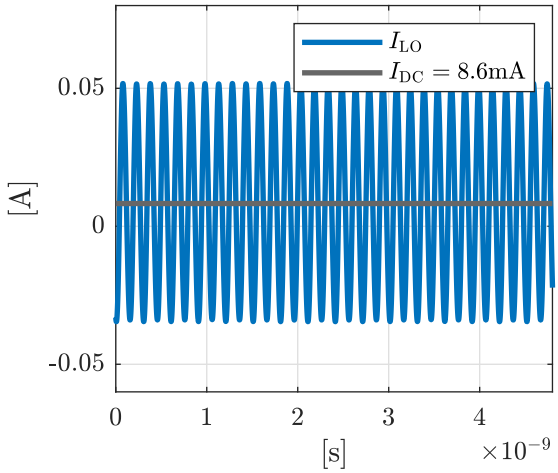
(b) V_{DCDC} compared to V_{LO}

Figure 4.11: V_{DCDC} and V_{LO} in a period for $f_0 = 2.5\mathrm{GHz}$

The simulated value of V_{DCDC} in Figure 4.11 has an average value of $V_{\mathrm{DCDC}} \simeq 0.3573V$ with a ripple of $\Delta V_{\mathrm{ripple}} = 1.8\mathrm{mV}$. These results are in line with previous simulations reported in Figure 4.8. Note however how the ripple seen in Figure 4.11 now shows a high frequency ripple component which is due to the current consumption of the VCO. The current feeding the VCO has in fact two components: one at DC, which is the one that we have considered so far, and one at AC at the frequencies $m \cdot 2f_0$ with $m = 1, 2, 3, ...$ The AC behaviour of the current can be observed in Figure 4.12.



(a) Current consumption of the VCO for $f_{\mathrm{sw}} = 2.5\mathrm{GHz}$

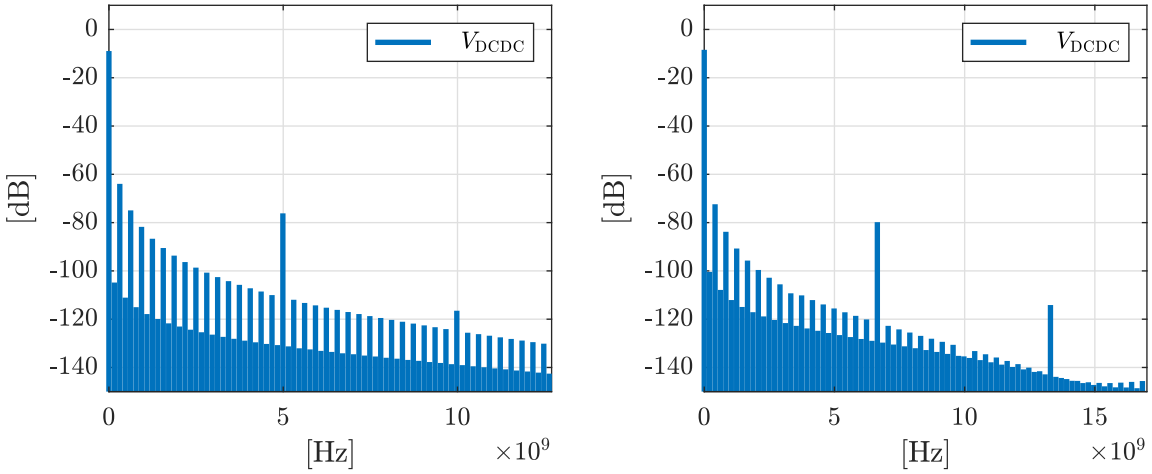


(b) Current consumption of the VCO for $f_{\mathrm{sw}} = 3.3\mathrm{GHz}$

Figure 4.12: Current consumption of the VCO for different f_0

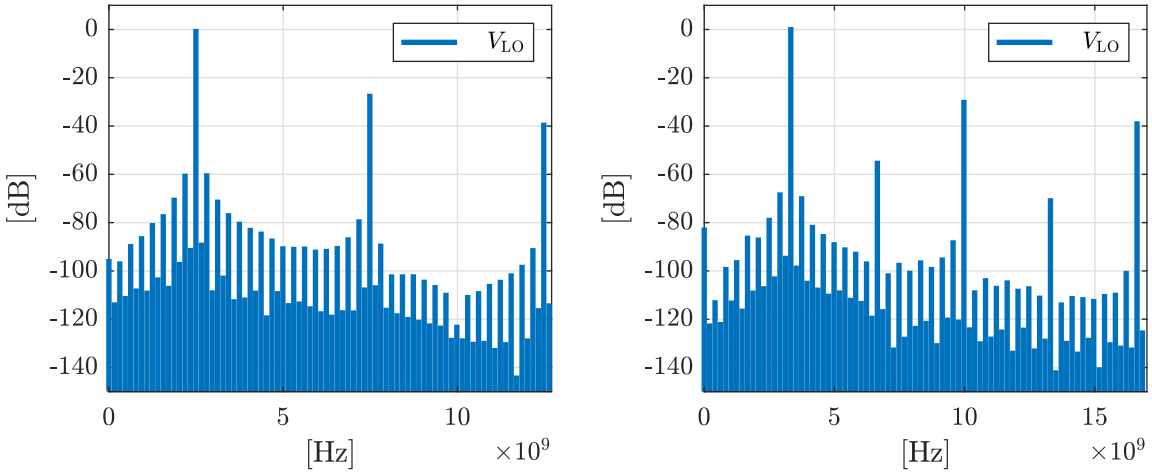
Continuing with our simulation the output spectrum of the VCO and SC converter are showed in Figure 4.13. Note from Figure 4.11a and Figure 4.13 that the ripple introduced on the supply voltage of the VCO, by the SC converter, is at a frequency of $2f_{\mathrm{sw}}$. Looking at the spectrum of V_{DCDC} we therefore clearly see a peak at DC, a series

of peaks at multiples of $2f_{\text{sw}}$ and then a series of peaks for the multiples of $2f_0$, due to the current consumption of the oscillator. A seen in Section 1.6 the ripple of V_{DCDC} generates frequency tones at the terms $f_{\text{m,n}} = m \cdot f_0 \pm n \cdot f_{\text{sw}}$, with $m, n = 1, 2, 3, ...$ This effect can be appreciated by looking at Figure 4.14 where this behaviour is clearly present, compared to the ideal spectrum of Figure 4.3.



(a) Spectrum of V_{DCDC} for $f_0 = 2.5\text{GHz}$ (b) Spectrum of V_{DCDC} for $f_0 = 3.3\text{GHz}$

Figure 4.13: Spectrum of V_{DCDC}



(a) Spectrum of V_{LO} for $f_0 = 2.5\text{GHz}$ (b) Spectrum of V_{LO} for $f_0 = 3.3\text{GHz}$

Figure 4.14: Spectrum of V_{LO}

We note that that the spur levels that we have obtained are coherent with what we expect. If we assume $V_{\text{m}} = 1\text{mV}$ and $K_{\text{V}} \simeq 600\text{MHz/V}$ we obtain for $f_{\text{m}} = 312\text{MHz}$ a spur level of -60.3dBc where the real simulated value is of -59.9dBc for $f_0 = 2.5\text{GHz}$. Moreover we can notice how the spurs of Figure 4.14b are attenuated as an effect of the higher frequency of operation of the VCO which raises f_{sw} reducing the ripple of the SC converter and the power of the spurs.

We can now proceed with the simulation of the phase noise of the SC powered Class-D VCO, which we plot in Figure 4.15. The results are consistent with what we have found in previous simulations where the VCO was powered by an ideal supply voltage. This proves that the SC converter doesn't deteriorate the performance of the VCO. Referring to the maximum noise allowed by Equation 1.66, simulation confirms that the noise produced by the SC converter is in fact well below that threshold, even assuming a high supply pushing of 600MHz/V.

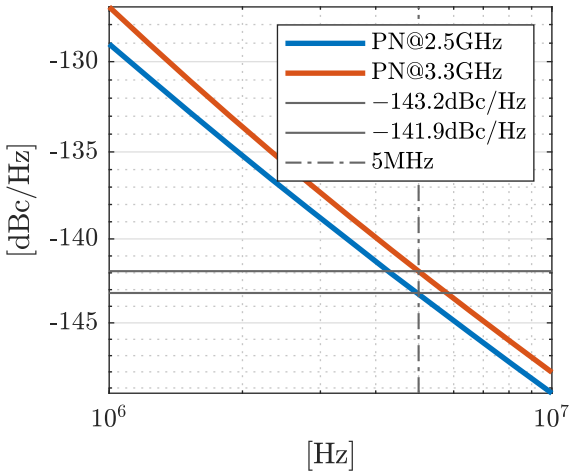


Figure 4.15: PN of the SC powered Class-D VCO for $f_{\text{sw}} = 2.5\text{GHz}$ and $f_{\text{sw}} = 3.3\text{GHz}$

Finally in Figure 4.16 we compare the behaviour of V_{DCDC} for $f_0 = 2.5\text{GHz}$ and $f_0 = 3.3\text{GHz}$. As we can clearly see since for $f_0 = 3.3\text{GHz}$ the load current I_{DC} decreases, V_{DCDC} increases compared to the case with $f_0 = 2.5\text{GHz}$. As we have already discussed however this, contrary to our intuition, doesn't aid the efficiency of the circuit so a technique like DCM has to be employed, to regulate V_{DCDC} while also improving efficiency.

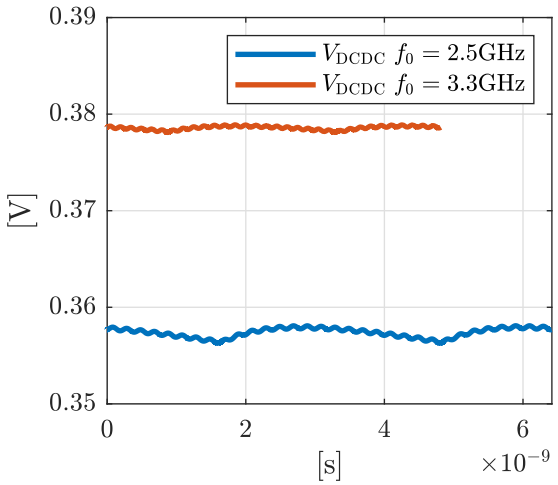


Figure 4.16: Comparison of V_{DCDC} for different f_0 of the VCO

Digital Capacitance Modulation

We therefore show briefly how DCM can be used to regulate the output voltage through some transient simulations. Supposing that we want to control the voltage inside of the interval $350\text{mV} - 360\text{mV}$, we implement DCM with $b = 4$ by dividing our converter in 4 binary weighted modules. We can verify if the number of modules used is sufficient by plotting the value of V_{DCDC}, as a function of I_{DC} and f_{sw} based on the combinations of modules used. To do this we use the data obtained from the previous simulations of the VCO. Since we know the power consumption of the VCO at its extremes we use a linear approximation to predict its behaviour for all its frequency range. Then by combining Equation 3.37 and Equation 3.3 we obtain the plot of Figure 4.17,

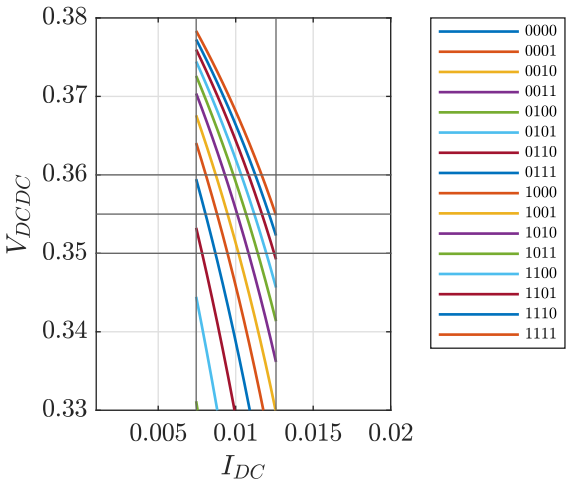
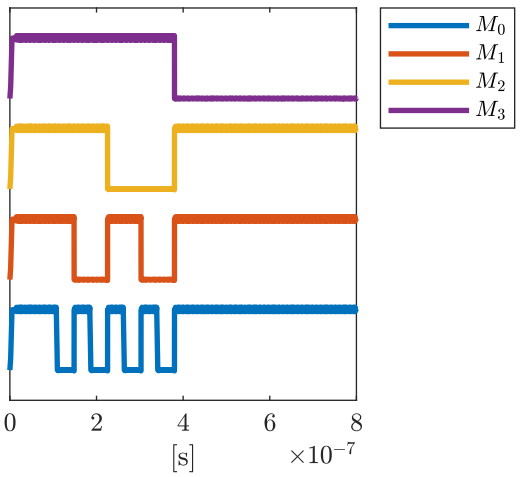


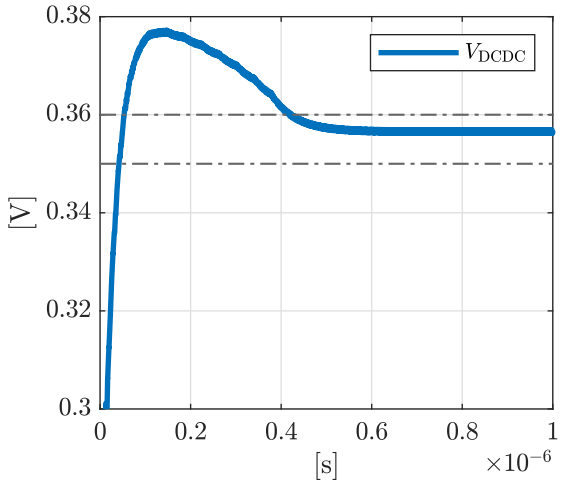
Figure 4.17: Model of V_{DCDC} based on the operating point of the VCO

It's important to note that, in order for DCM to work for every value of current load I_{DC} there must be a corresponding curve in Figure 4.17 inside of the bounds in order for the converter to be able to reach a steady state condition.

Simulations are made for a SC converter powering the VCO operating at $f_0 = 3.3\text{GHz}$. The resulting initial transient of the SC converter is shown in Figure 4.18b, while the digital signals controlling which modules contribute to the charge/discharge process are shown in Figure 4.18a . Note that the signal M_0, controls the module corresponding to the least significant bit, while M_3 controls the most significant bit. We see how initially the output voltage crosses the upper threshold, this causes the number of modules to consequently be decreased, by the control logic, until the voltage returns inside the boundaries. The value of V_{DCDC} finally then reaches steady-state. This same process happens during operation of the VCO for a load change.



(a) Signals controlling which modules contribute to conduction



(b) Transient of V_{DCDC} using DCM

Figure 4.18: Regulation of the output voltage with DCM

Note that the steady state value of V_{DCDC} is coherent with what predicted by the model, of Figure 4.17. The voltage waveform V_{DCDC} of a SC converter employing DCM with module combination 0111, for an ideal current load, is plotted below:

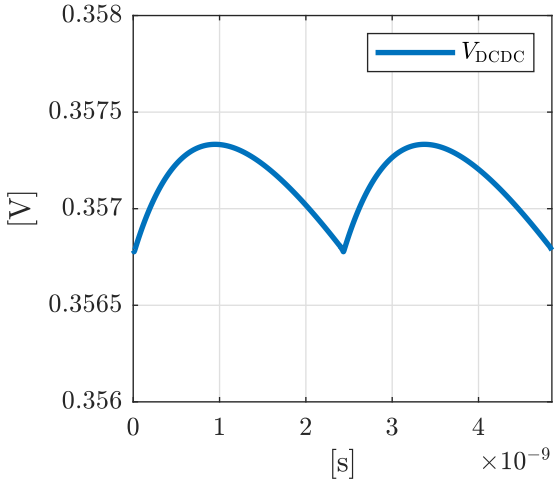


Figure 4.19: V_{DCDC} in a period T_{sw} for a simulated converter employing DCM

Finally we note how DCM can be used to regulate the output voltage of the SC converter, while aiding efficiency. The combination 1111 in fact, represents the design point of the converter in Table 4.2, so by employing different combinations we are effectively using a converter with mosfets that have a smaller W. This allows us to scale the switching losses as the load changes, for a fixed target steady state value of V_{DCDC}. For the case showed above, when the converter operates with the configuration 0111, the simulated efficiency, for an ideal load, is of $\eta \simeq 78\%$ which shows a slight improvement compared to the values obtained in Table 4.3.

4.3.1 Considerations on the use of External Capacitors

The simulations results that we have showed, up until now, were made with an output capacitor $C_{\text{out}} = 10\text{nF}$ which cannot be integrated in this technology, contrary to C_{fly}, due to the excessive area consumption necessary to physically realize it. The highest capacitance density achievable is in fact of $7.76\text{fF}/\mu\text{m}^2$, meaning that $C_{\text{out}} = 10\text{nF}$ will lead to an area occupation of $\simeq 1.29\text{mm}^2$, which is too expensive to be realised when compared to an off-chip solution. The flying capacitor, on the other hand, for a value $C_{\text{fly}} = 500\text{pF}$ occupies 0.0644mm^2 which doesn't pose the same problems and can be integrated. The capacitor C_{out} therefore has to be realized as an external component, allowing us to use higher values of capacitance compared to an on-chip solution. The final chip design however will be bulkier as a result of the use of off-chip components.

Note that in our design thanks to the use of a high switching frequency, we were able to reduce the size of capacitor C_{fly} and C_{out} compared to designs with a lower switching frequency. This can be seen by looking at Equation 3.14 where increasing the value of f_{sw} allows us to obtain the same value of R_{SSL} for smaller values of C_{fly}. Nevertheless since C_{out} is realized as an off-chip component it can easily be made far bigger than $C_{\text{out}} = 10\text{nF}$, with negligible additional cost and allowing us to decrease the power of the spurs in the circuit. We can therefore perform another simulation of the circuit employing this time an output capacitor of $C_{\text{out}} = 100\text{nF}$. The results for PN are the same so we show only the spectrum of the output signal of the VCO in Figure 4.20.

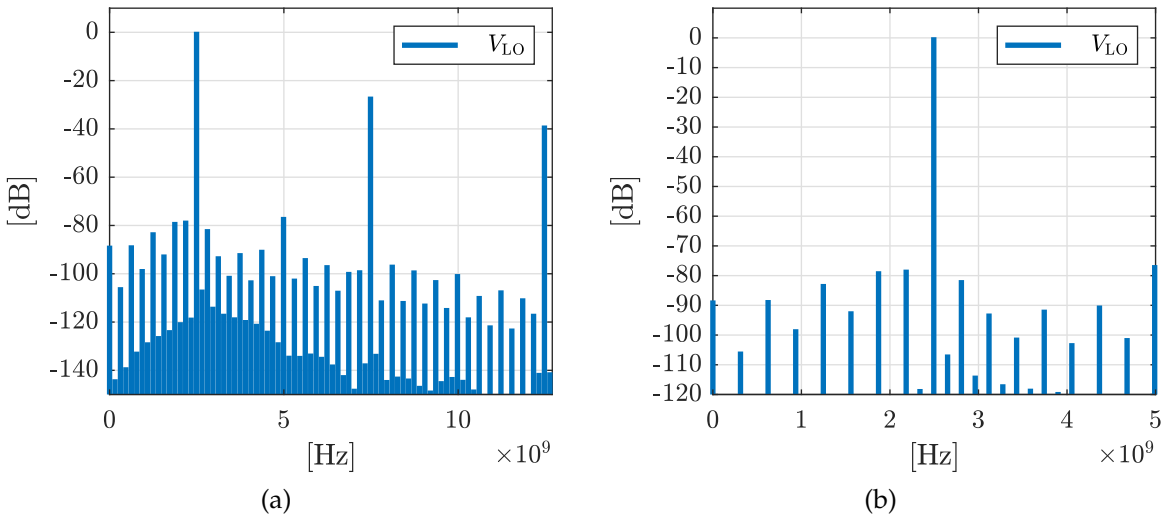


Figure 4.20: Spectrum of V_{LO} for $f_0 = 2.5\text{GHz}$ with $C_{\text{out}} = 100\text{nF}$

Having increased the value of C_{out}, by an order of magnitude the ripple has to decrease by an order of magnitude too, following Equation 3.17. Therefore as shown in Figure 4.20 the power of spurious tones decreases of 20dB, becoming comparable to the even spurs of the oscillator, with the largest spur having a power of -78dBc. Note that we could also be using an even bigger capacitor than $C_{\text{out}} = 100\text{nF}$ and further reduce the spurs, but a trade off has to ultimately be made as bigger values of capacitance tend to make the dynamic response of the converter slower in the case of quick load changes. As a comparison for the previous results, in [6] a SC powered Class-D VCO is realised, achieving a spur of -66dBc at $f = 6\text{MHz}$ which is the switching frequency of the converter and of the reference signal of the PLL. In [11] for a similar circuit, the spur of the converter is at $f = 500\text{kHz}$ with -73.7dBc. Finally in [14] a SC powered LC oscillator has its ripple induced spurs below -65dBc without using external components.

4.3.2 Simulation with Phase Interleaving

We now want to show how by applying phase interleaving we are able to reduce the size of the output capacitor C_{out} to a point where it can be integrated with the other components. In fact, since phase interleaving allows us to reduce the amount of ripple, we can take advantage of it to scale down the value of C_{out} while keeping fixed ΔV_{ripple}. We proceed by applying phase interleaving to our symmetric converter with $N = 4$ by realising our converter as a parallel combination of 4 converters were each one is phase shifted with respect to the next by a quantity $T_{\text{sw}}/8$, as show in Figure 4.21.

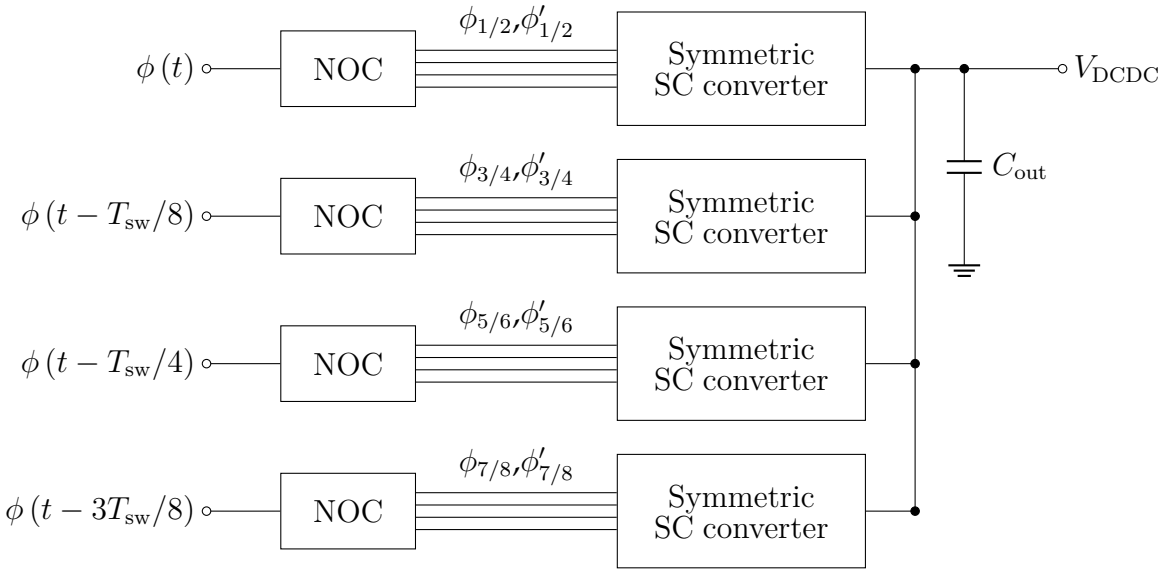


Figure 4.21: Block diagram of the interleaved converter with $N = 4$

Note that normally, for $N = 4$, phase interleaving allows us to reduce the voltage ripple by a factor of 4, however in our case we will obtain a reduction of 16. This is because, since we want to keep the same value of R_{OUT}, we have to scale each symmetric converter by a factor of 4. Considering that we have fixed a total flying capacitance of $C_{\mathrm{fly}} = 500\mathrm{pF}$, each module will then use a total of $125\mathrm{pF}$ and its switches will be 4 times smaller, leading to a 4 time increase in the R_{on} of each switch. Each symmetric module will have therefore 4 times the value of R_{OUT} of the converter sized in Table 4.2. The parallel combination of the 4 converters however compensates for this scaling and will give us back the original value of R_{OUT}. However since the voltage ripple depends on the ratio $C_{\mathrm{fly}}/C_{\mathrm{out}}$, and C_{fly} has been scaled down by a factor of 4, this means that for the same value of C_{out} the ripple is also decreased by 4. In light of this results, we can scale the output capacitance of C_{out}, by a factor of 16 while keeping the same ripple value. The new value of the filtering capacitor is therefore $C_{\mathrm{out}} = 625\mathrm{pF}$, which can be integrated. Simulation of the behaviour of the voltage ripple for an non-interleaved converter with $C_{\mathrm{out}} = 10\mathrm{nF}$ and a interleaved converter with $C_{\mathrm{out}} = 625\mathrm{pF}$, working at $f_{\mathrm{sw}} \simeq 156\mathrm{MHz}$ with an ideal load $I_{\mathrm{DC}} = 12.4\mathrm{mA}$, is shown in Figure 4.22.

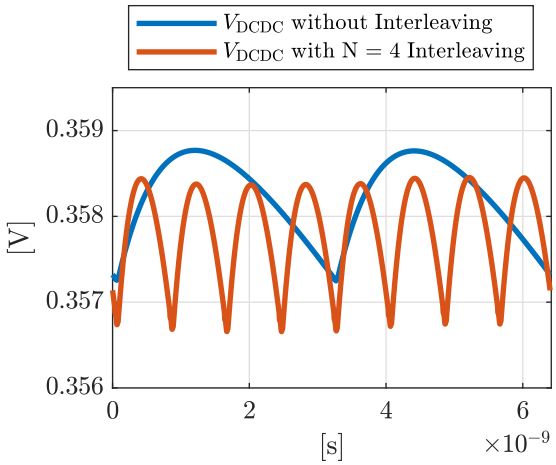
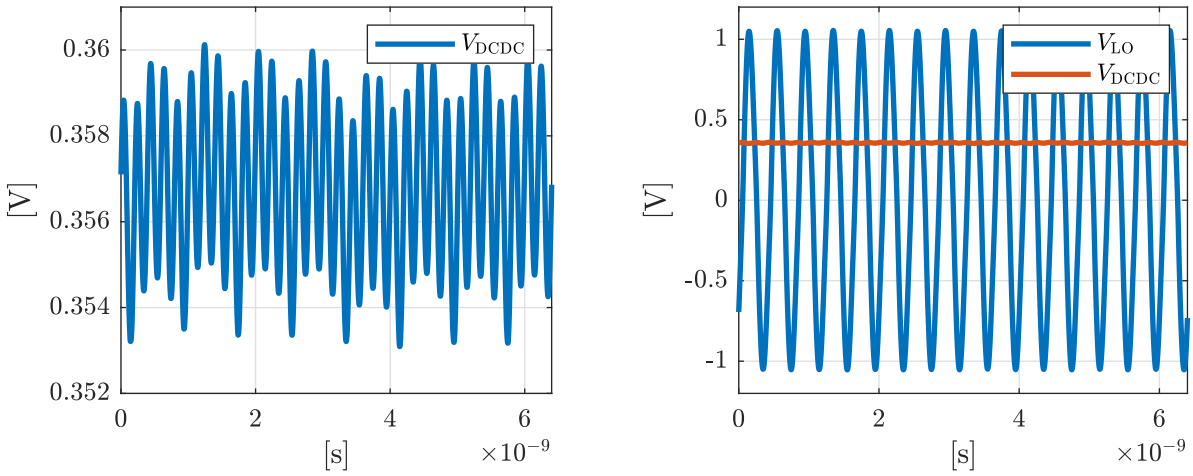


Figure 4.22: Comparison of V_{DCDC} between interleaved and non-interleaved designs

We can clearly see how, as anticipated, the ripple of the converter remains basically the same. A small negligible drift in the average value of V_{DCDC} is also observed, probably due to non-linearity effects of the components. Furthermore the waveform of the interleaved converter suffers from small "jumps" due to small timing errors in the generation of the phases that make the waveform slightly go up and down during T_{sw}. Finally we also notice how the frequency of the ripple has been multiplied by $N = 4$. Following this observation we can expect the largest spur of the VCO to be positioned at a distance of $8 f_{\mathrm{sw}} = 1.248\mathrm{GHz}$ from the carrier.

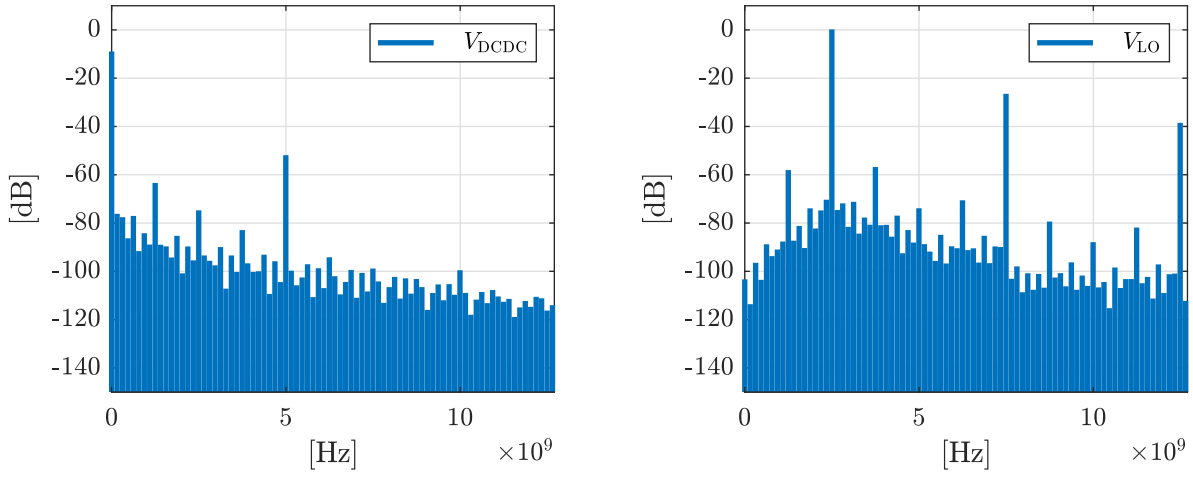
We proceed to simulate the circuit for the case where the VCO is working at $f_0 = 2.5\text{GHz}$, which is the more challenging working extreme from what pertains to the ripple amplitude, following Equation 3.18, since in this scenario the converter works with the lowest switching frequency $f_{\text{sw}} \simeq 156\text{MHz}$ and the highest ideal current load $I_{\text{DC}} = 12.4\text{mA}$. The voltage waveforms in a period T_{sw} for both the SC converter and the VCO, are therefore shown in Figure 4.23



(a) Ripple of V_{DCDC} (b) V_{LO} compared to V_{DCDC}

Figure 4.23: V_{DCDC} and V_{LO} in a period for $f_0 = 2.5\text{GHz}$ with $C_{\text{out}} = 625\text{pF}$ and $N = 4$

Their spectrum is then showed in Figure 4.24 where as expected the main ripple component of the spectrum of V_{DCDC} is at $f_0 = 1.248\text{GHz}$ which translates to the 2 largest spurs in the spectrum of the VCO, being at -57dBc and -58.2dBc, while the third biggest spur at $\Delta f = 156\text{MHz}$ is of -70.5dBc.



(a) Spectrum of V_{DCDC} (b) Spectrum of V_{LO}

Figure 4.24: Spectrum of V_{LO} and V_{DCDC} for $f_0 = 2.5\text{GHz}$ with $C_{\text{out}} = 625\text{pF}$ and $N = 4$

A zoomed version of Figure 4.24b is plotted in Figure 4.25 for extra reference.

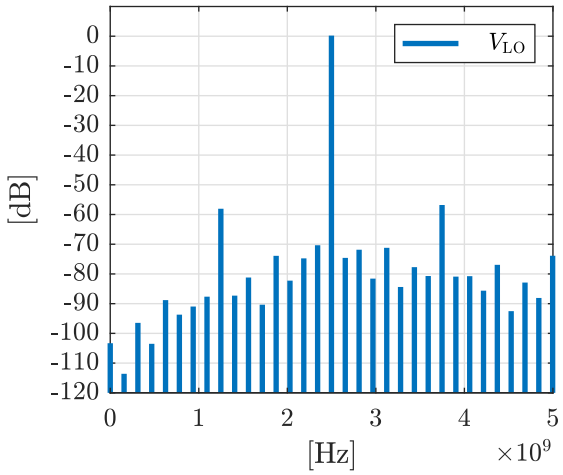


Figure 4.25: Spectrum of V_{LO} zoomed around the carrier

Finally the PN of the VCO is plotted in Figure 4.26, showing no deterioration from the operation with the interleaved converter.

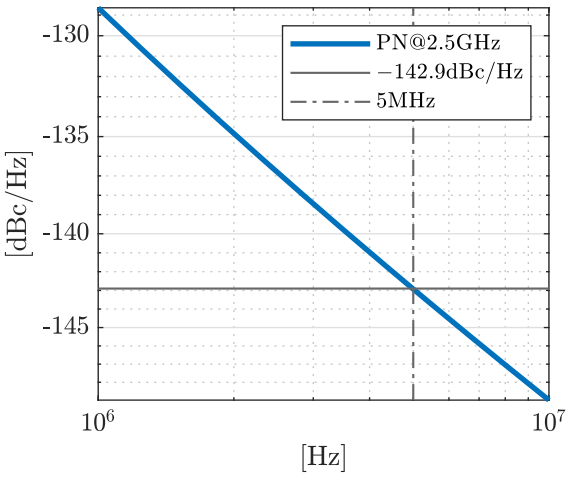


Figure 4.26: PN for $f_0 = 2.5\mathrm{GHz}$ with $C_{\mathrm{out}} = 625\mathrm{pF}$ and $N = 4$

Note that another possible design point can be found by employing phase interleaving and an external capacitor C_{out} in order to reduce even further the level of the spurs.

Conclusions

In this thesis the design challenges behind the realization of a Class-D oscillator directly powered by a switching regulator have been analysed. A possible design solution has been provided by powering a $2.5\text{GHz} - 3.3\text{GHz}$ Class-D VCO with a SC converter achieving a maximum efficiency of 80%. Additionally, the switching regulator takes advantage of the output signal of the VCO to generate its switching frequency through a frequency divider. The switching frequency of the converter therefore varies between 156MHz and 206MHz. Simulation results show that the phase noise of the VCO is preserved even when powered by the switching regulator. The very high frequency pushing of the Class-D topology however requires the use of an external capacitor in order to significantly reduce the spurs present in the output spectrum of the VCO. For a value of the output capacitor of $C_{\text{out}} = 100\text{nF}$ the highest simulated spur level is of -78dBc. An additional design employing phase interleaving on the switching regulator has also been analysed to improve the ripple of the converter. The output capacitor, in this way, has been reduced to $C_{\text{out}} = 625\text{pF}$, which is suitable for integration. The largest simulated spur in this case is positioned at 1.248GHz from the carrier with a level of -57dBc, while the spurs inside this frequency range remain below -70.5dBc.

Bibliography

[1] Farid Uddin Ahmed et al. "A Brief Overview of On-Chip Voltage Regulation in High-Performance and High-Density Integrated Circuits." In: *IEEE Access* 9 (2021), pp. 813–826. DOI: 10.1109/ACCESS.2020.3047347.

[2] Tomaso Erseghe. *Digital Modulation Systems*. John Wiley & Sons, Ltd, 2011. Chap. 5, pp. 259–371. ISBN: 9781119978589. DOI: https://doi.org/10.1002/9781119978589.ch5.

[3] Luca Fanori and Pietro Andreani. "A 2.5-to-3.3GHz CMOS Class-D VCO." In: *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. 2013, pp. 346–347. DOI: 10.1109/ISSCC.2013.6487763.

[4] Luca Fanori and Pietro Andreani. "Class-D CMOS Oscillators." In: *IEEE Journal of Solid-State Circuits* 48.12 (2013), pp. 3105–3119. DOI: 10.1109/JSSC.2013.2271531.

[5] Ramesh Harjani and Saurabh Chaubey. "A unified framework for capacitive series-parallel DC-DC converter design." In: *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*. 2014, pp. 1–8. DOI: 10.1109/CICC.2014.6946050.

[6] Hossein Rahmanian Kooshkaki and Patrick P. Mercier. "A 0.55mW Fractional-N PLL with a DC-DC Powered Class-D VCO Achieving Better than -66dBc Fractional and Reference Spurs for NB-IoT." In: *2020 IEEE Custom Integrated Circuits Conference (CICC)*. 2020, pp. 1–4. DOI: 10.1109/CICC48029.2020.9075944.

[7] Sudhir S. Kudva and Ramesh Harjani. "Fully Integrated Capacitive DC–DC Converter With All-Digital Ripple Mitigation Technique." In: *IEEE Journal of Solid-State Circuits* 48.8 (2013), pp. 1910–1920. DOI: 10.1109/JSSC.2013.2259044.

[8] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. 2nd ed. Cambridge University Press, 2003. DOI: 10.1017/CBO9780511817281.

[9] Ricardo Madeira, João Pedro Oliveira, and Nuno Paulino. *Fully Integrated Switched-Capacitor PMU for IoT Nodes: Analysis and Design*. English. Synthesis Lectures on Engineering, Science, and Technology. Netherlands: Springer, Nov. 2022. ISBN: 978-3-031-14700-5. DOI: 10.1007/978-3-031-14701-2.

[10] Timothy McRae and Aleksandar Prodić. "Design Oriented Analysis of Switched Capacitor DC-DC Converters." In: *IEEE Open Journal of Power Electronics* 1 (2020), pp. 2–13. DOI: 10.1109/OJPEL.2019.2959553.

[11] Ali Nikoofard and Patrick P. Mercier. "A 900MHz GFSK and 16-FSK TX Achieving Up to 63.9% TX Efficiency and 76.2% PA Efficiency via a DC-DC-Powered Class-D VCO and a Class-E PA." In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.9 (2022), pp. 3739–3743. DOI: 10.1109/TCSII.2022.3170537.

[12] Yogesh K. Ramadass, Ayman A. Fayed, and Anantha P. Chandrakasan. "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS." In: *IEEE Journal of Solid-State Circuits* 45.12 (2010), pp. 2557–2565. DOI: 10.1109/JSSC.2010.2076550.

[13] Behzad Razavi. *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. 2nd. USA: Prentice Hall Press, 2011. ISBN: 0137134738.

[14] Alessandro Urso et al. "A Switched-Capacitor DC-DC Converter Powering an LC Oscillator to Achieve 85% System Peak Power Efficiency and -65dBc Spurious Tones." In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.11 (2020), pp. 3764–3777. DOI: 10.1109/TCSI.2020.3012106.

[15] Tom M. Van Breussegem and Michiel S. J. Steyaert. "Monolithic Capacitive DC-DC Converter With Single Boundary–Multiphase Control and Voltage Domain Stacking in 90 nm CMOS." In: *IEEE Journal of Solid-State Circuits* 46.7 (2011), pp. 1715–1727. DOI: 10.1109/JSSC.2011.2144350.

[16] Anurag Veerabathini and Paul M. Furth. "A Low Output Voltage Ripple Fully-Integrated Switched-Capacitor DC-DC Converter." In: *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2019, pp. 937–940. DOI: 10.1109/MWSCAS.2019.8884904.

[17] Zhekai Xiao, Anh Khoa Bui, and Liter Siek. "A Hysteretic Switched-Capacitor DC–DC Converter With Optimal Output Ripple and Fast Transient Response." In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.11 (2017), pp. 2995–3005. DOI: 10.1109/TVLSI.2017.2728606.

[18] Dengke Zheng et al. "Medium Frequency Output Impedance Limits of Switched-Capacitor Circuits." In: *IEEE Transactions on Power Electronics* 38.2 (2023), pp. 2156–2168. DOI: 10.1109/TPEL.2022.3213647.

Run, rabbit, run
Dig that hole, forget the Sun
And when at last the work is done
Don't sit down, it's time to dig another one

— Pink Floyd

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