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A 1.8 V 25 Mbps CMOS single-phase, phase-locked loop-based BPSK, QPSK demodulator

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ABSTRACT

A single-phase binary/quadrature phase-shift keying (BPSK/QPSK) demodulator basing on a phase-locked loop (PLL) is described. The demodulator relies on a linear characteristic a rising-edge RESET/SET flip-flop (RSFF) employed as a phase detector. The phase controller takes the average output from the RSFF and performs a sub-ranging/re-scaling operation to provide an input signal to a voltage-controlled oscillator (VCO). The demodulator is truly modular which theoretically can be extended for a multiple-PSK (m-PSK) signal. Symbol-error rate analysis has also been extensively carried out. The proposed BPSK and QPSK demodulators have been fabricated in a 0.18 μm digital complementary metal–oxide–semiconductor (CMOS) process where they operate from a single supply of 1.8 V. At a carrier frequency of 60 MHz, the BPSK and QPSK demodulators achieved maximum symbol rates of 25 and 12.5 Msymb/s while consuming 0.68 and 0.79 mW, respectively. At these maximum symbol rates, the BPSK and QPSK demodulators deliver symbol-error rates less than 7.9×10^{-10} and 9.8×10^{-10}, respectively where their corresponding energy per bit figures were at 27.2 and 31.7 pJ.

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1. INTRODUCTION

In and on-human body communication (HBC) has been emerging as an essential development for modern healthcare monitoring and treatment. To achieve a practical implant communication distance and a reasonably high data rate, a 10 to 100 MHz frequency band can be utilized for in-body HBC applications owing to high penetration depth and low path loss [1]–[3]. Regarding a modulation scheme, binary and quadrature phase-shift keying (BPSK, QPSK) can offer a very low bit-error rate (BER) for a given signal-to-noise ratio [1]. BPSK and QPSK have been widely deployed in many communication systems for various applications such as HBC, biomedical data links, wireless radio, and optical data links [4]–[17]. One of the most widely-used BPSK demodulation technique in integrated circuits and systems relies on Costas loop [4], [18] which allows carrier frequency tracking and phase synchronization. With the use of a quadrature voltage-controlled oscillator (VCO) inside a phase-locked loop (PLL), the Costas loop has a deep impact on digital communications for many decades [19].

In research [9], [11], Costas loop has been employed for high data-rate BPSK demodulation in a high-speed wireless link. To improve the Costas loop's stability, a delay-locked loop (DLL) can be utilized to build a BPSK demodulator as demonstrated in [12], [14] for HBC. Linear multiplication and a quadrature VCO in these Costas loops pose a design challenge, especially at a high-frequency operation. A BPSK or QPSK

demodulator using a single-phase VCO without any linear multiplier would be truly attractive. The BPSK demodulator in [20] employs a DLL-based clock-data recovery technique (CDR) with a half-rate bang-bang phase detector (BBPD) that directly extracts a synchronized clock signal from the BPSK signal with a dedicated 0/90° signal generator. Extending this technique for higher-order PSK demodulation is possible but with a more complicate design on the CDR loop and the phase detector. A single-phase locked-loop-based BPSK demodulator in [8] is proposed for a biomedical data link. However, the structure still possesses two overlapping loops making the design rather complicate in controlling the loop stability. Another single-phase BPSK demodulator can be found in [15] which employs a phase-frequency detector (PFD) inside a single-loop structure. The demodulation principle practically relies on transition detection where it requires a dedicate data recovery block to obtain demodulated data from the transition detector. For both of these BPSK demodulators, it would be rather difficult to extend these demodulators for QPSK, 8-PSK or *m*-PSK demodulation.

The non-locked-loop BPSK demodulator in [21] utilizes an injection-locking oscillator together with signal addition and amplitude detection for extraction. Although it offers a fairly competitive performance in term of energy-per-bit (E_b), the technique is prone to adjacent channel interference with a rather high bit-error rate (BER) of about 10^{-3}. The all-digital non-locked-loop system in [22] delivers one of the best E_b-based BPSK demodulator's performance. Its principle is based on generating a data flipping signal whose rising edges indicate the instants when the recovered data should be flipped. The architecture is non-modular and not straightforward to be extended for demodulating high-order PSK signals.

The Costas loop can also be effectively extended for QPSK demodulation with additional circuitries to perform a specific phase-control function suitable for QPSK demodulation as in [23]–[26]. The modifications of these QPSK demodulator structures can be found in [9], [12] for high data-rate applications. These demodulators still employ a quadrature VCO where the accuracy of 0/90° phase difference is still eminent in the design. To the authors' knowledge there is still no 8-PSK demodulator developed from the Costas loop, so its modularity is limited to a certain extent. The QPSK demodulator of the receiver in [16] utilizes a carrier recovery loop (CRL), multiphase generator and *I*/*Q* demodulator where a single-phase VCO is only required for down conversion. However, a low data rate of this demodulator from 2.4 GHz carrier results in a rather high E_b value. The non-locked-loop 8-PSK demodulator in [27] implemented with an InP 250 nm DHBT process delivers a very high data rate of 15 Gbps. It employs a comparator and a frequency divider for carrier recovery. However, deployment of the off-chip active circuits such as an amplifier, a bandpass filter and a power detector makes it less attractive and hard to assess the overall power efficiency.

In this work, an alternative PLL based *m*-PSK demodulator employing a single-phase VCO inside a single loop structure is introduced for BPSK and QPSK demodulation. The structure is very simple and truly modular owing to the linear phase detector's characteristic over an entire 2π range of the phase difference. Without any linear multiplier, the phase control process is simple and power efficient. The demodulator concept has been fabricated in a standard 0.18 μm complementary metal–oxide–semiconductor (CMOS) process aiming for deep-implant HBC applications with a competitive E_b performance as compared to the prior arts, especially those with a locked-loop structure. The basic principle for PLL-based *m*-PSK demodulation is reviewed in section 2.1 which paves a way for proposing a single-phase/single-loop PLL-based *m*-PSK demodulator in section 2.2. Regarding to the proposed demodulation structure, the theoretical symbol-error-rate (SER) analysis based on phase comparison is extensively carried out in section 3. Design and analysis of the circuit building blocks for the BPSK, QPSK demodulators are described in section 4. Chip implementation and measurement in 0.18 mμm CMOS process is reported in section 5 including performance comparison. Future works are also discussed before the conclusion in section 6.

2. SINGLE-PHASE PLL-BASED *m*-PSK DEMODULATORS

2.1. A Basic Principle of PLL-Based *m*-PSK Demodulation

Simple mathematical description can be used to explain the *m*-PSK demodulation principle using Figure 1. By considering a general PLL-based circuit structure of Figure 1(a), where a phase detector (PD) is employed for phase comparison. The phase difference $\Delta\phi(t)$ generated from the phase detector can be written as (1),

$$\Delta\phi(t) = \phi_P(t) - \phi_V(t) = \overbrace{[\omega_c t + \theta_{dj}(t)]}^{\phi_P(t)} - \overbrace{[\omega_V t + \phi_{0V}(t)]}^{\phi_V(t)} = (\omega_c - \omega_V)t - \phi_{0V}(t) + \theta_{dj}(t) \quad (1)$$

where $\phi_P(t)$ and $\phi_V(t)$ are the *m*-PSK and the VCO's phases, $\phi_{0V}(t)$ is the initial VCO's phase considered at the first instance when a lock condition has been reached, ω_c and ω_V are the carrier and the VCO's frequencies, $\theta_{dt}(t)$ represents a data phase of the *m*-PSK signal, e.g., $\theta_{dt}(t)=\{0, \pi\}$ and $\theta_{dj}(t)=\{0, \pi/2, 2\pi/2, 3\pi/2\}$ for BPSK and QPSK, respectively; generally, $\theta_{dj}(t) = \{j(2\pi/m)\}$ with the symbol index j=0, 1, 2, …, (m-1).

When the loop is in a lock condition by the PLL mechanism, we have $\omega_V = \omega_c$ and the phase difference in (1) is reduced to (2).

$$\Delta\phi(t) = \theta_{dj}(t) - \phi_{0V}(t) \tag{2}$$

If the initial VCO's phase $\phi_{0V}(t)$ is constant and unchanged regardless of $\theta_{dj}(t)$ values, e.g., $\phi_{0V}(t) = \phi_{0VK}$ for a specific carrier frequency ω_c (=ω_V), this gives,

$$\Delta\phi(t) = \theta_{dj}(t) - \phi_{0VK} \tag{3}$$

which clearly suggests that the signals $\Delta\phi(t)$ and $\{v_y\}$ $(= f(\Delta\phi(t)) = f(\theta_{dj}(t) - \phi_{0VK}))$ in Figure 1(a) can uniquely represent the original data as long as $f(\cdot)$ is a one-to-one function. The digital data bits can thus be recovered from $\{v_y\}$ by various means.

Getting the VCO to maintain its phase at a constant value ϕ_{0VK} after the initial frequency lock, the VCO_{in} has to experience no significant change even if $\{v_y\}$ varies with $\theta_{dj}(t)$ over different symbol periods. This operation is essentially managed by the phase controller yielding,

$$VCO_{in} = g(\{v_y\}) = g\left(f(\Delta\phi(t))\right) = g(\Delta\phi(t)) = g(\theta_{dj}(t) - \phi_{0VK}) = g(\theta_{dj+1} - \phi_{0VK}) = g(\theta_{dj} - \phi_{0VK}) \tag{4}$$

for j=1, 2, …, (m-1). As shown in (4) simply suggests that different data phases render the same value of VCO_{in}. Therefore the function $g(\cdot)$ is a kind of many-to-one function. Noting that if the carrier frequency changes, the loop will adjust itself and re-lock to this new frequency with a new value of ϕ_{0VK}. This will basically move the voltage V_K along the VCO_{in} curves in Figure 1(b). In another word, this m-PSK demodulator loop is able to track with a carrier frequency and it basically possesses capturing and locking mechanisms similar to a typical PLL system.

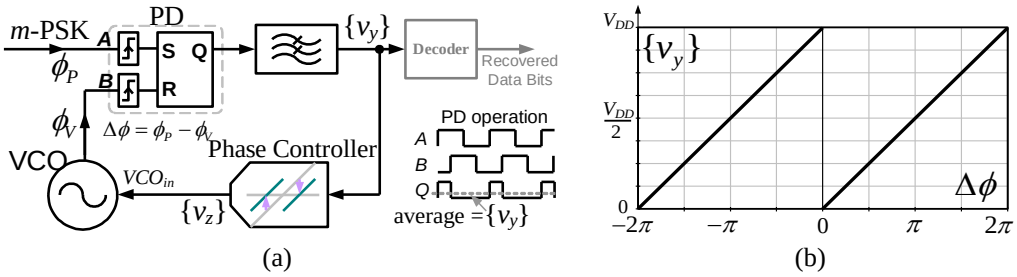


Figure 1. A conceptual PLL-based m-PSK demodulator with a phase controller: (a) basic structure and (b) rising-edge-triggered RSFF's characteristic

2.2. Proposed single-phase/single-loop PLL-based *m*-PSK demodulators

Practical realization of a locked-loop-based m-PSK demodulator will be addressed here where a single-phase VCO can be employed by exploiting a rising-edge-triggered RESET/SET flip-flop (RSFF) as a phase detector (symbolized in Figure 1(a)). Its average output voltage, $\{v_y\}$ against the phase difference, $\Delta\phi$ is characterized in Figure 1(b) indicating a repeating linear relation between $\{v_y\} = 0$ and V_{DD} over $\Delta\phi = 2n\pi$ to $2(n+1)\pi$ radians where $n = 0, \pm1, \pm2, \ldots$. The *linear* $\{v_y\}$–$\Delta\phi$ characteristic of the rising-edge RSFF helps relax designing a phase controller as explained below.

The phase controller operates differently on $\{v_y\}$ depending on a particular order of PSK signal as depicted in Figure 2. Figure 2(a) shows a phase-control step of the BPSK demodulation which can be achieved with a 1-bit phase-control circuit in Figure 2(b). Similarly, QPSK demodulation can be done with two steps of the same phase-control process as shown in Figure 2(c). On the first graph of Figures 2(a) and 2(c), the data symbols of the BPSK and QPSK signals are represented by the unique $\{v_y\}$ level. The phase controller has to operate on these $\{v_y\}$ positions such that all the different data symbol levels on the $\{v_y\}$–$\Delta\phi$ graph have to be mapped to the *same* level of $\{v_z\}$ and fed to VCO_{in} which in turn produces a specific output frequency identical to the incoming carrier frequency. Moreover, this essentially restricts VCO_{in} not to experience any significant

change for different data symbols; hence the VCO's phase remains undisturbed after the initial frequency lock. Consider the BPSK scenario in Figure 2(a), $\{v_y\}$ is mapped to $\{v_z\}$ by a "sub-ranging/shifting/re-scaling" process. The up/down voltage-shifting operation can be implemented with a circuit in Figure 2(b) where a comparator is employed to determine the range of $\{v_y\}$ relative to $V_{DD}/2$. If $\{v_y\}$ is lower (higher) than $V_{DD}/2$, it will be pulled up (down) using *UP* (*DN*) switches to guide a direct current I_{UPDN} to flow from right (left) to left (right) of the resistor R_P rendering a shifted voltage at gate of N_1, $\{v_{y\_sh}\}$ as described by (5a) and (5b).

$$\{v_{y\_sh}\} = \{v_y\} + R_P I_{UPDN}, \text{for } \{v_y\} \leq \frac{V_{DD}}{2}, \tag{5a}$$

$$\{v_{y\_sh}\} = \{v_y\} - R_P I_{UPDN}, \text{for } \{v_y\} > \frac{V_{DD}}{2} \tag{5b}$$

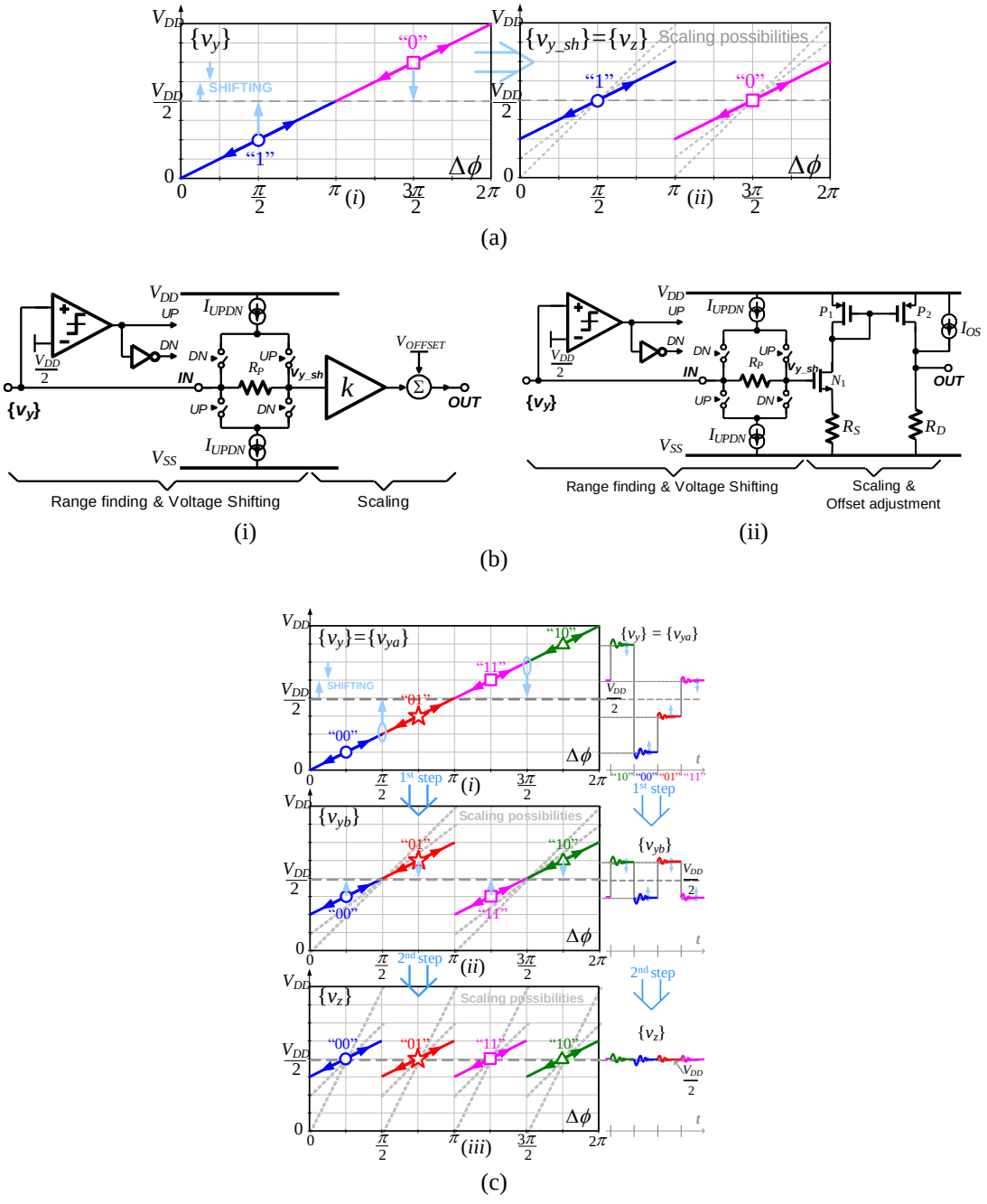


Figure 2. Voltage–$\Delta\phi$ graphs for phase-control steps in (a) BPSK, (b) a 1-bit shifting/re-scaling phase-control circuit-concept (*i*) and realization (*ii*), and (c) QPSK demodulation

The amplifier *k* and offset-voltage adjustment help rescale the output voltage back to a larger voltage range after shifting and this can simply be done with a source-degenerated N-channel metal-oxide-semiconductor (NMOS) amplifier and a P-channel metal-oxide-semiconductor (PMOS) current mirror as shown in Figure 2(b-*ii*) where the direct current (DC) offset current I_{OS} helps adjust the output DC voltage. It is fairly obvious that the *UP* and *DN* logic level from the comparator's output can be considered as a recovered data bit. This 1-bit sub-ranging/re-scaling process can be recursively employed for QPSK Figure 2(c), 8-PSK or *m*-PSK demodulation where 2, 3 or $\log_2(m)$ sub-ranging/re-scaling stages are needed. Moreover, because the phase controller still preserves the PLL's loop dynamic, if the carrier frequency changes, the phase controller would automatically set the voltage $\{v_z\}$ (and VCO_{in}) to the new value to attain frequency tracking as shown by the leaning arrows in Figures 2(a) and 2(c). In this way, the frequency tuning can be achieved for this *m*-PSK demodulator similar to the conventional PLL technique. Time-domain signaling of the phase control is also illustrated in Figure 2(c) for QPSK demodulation (in practice, there will be a high-frequency signal component embedded in $\{v_y\}$).

Following the above phase-control description, Figure 3 shows the proposed single-phase, single-loop BPSK and QPSK demodulators in Figures 3(a) and 3(b), respectively where one and two 1-bit phase-control circuits from Figure 2(b) are employed. The capacitors C_{PC} and C_{SP} have been connected across the resistors R_P and R_S for pole/zero compensation purpose as later explained in section 4. Inside these demodulator structures, the *R*/*C* networks [R_A, R_B, C_B] and [R_D, R_E, C_E] are utilized to serve as lag-lead loop filters for high-frequency component removal as well as loop stabilization as also described in section 4.

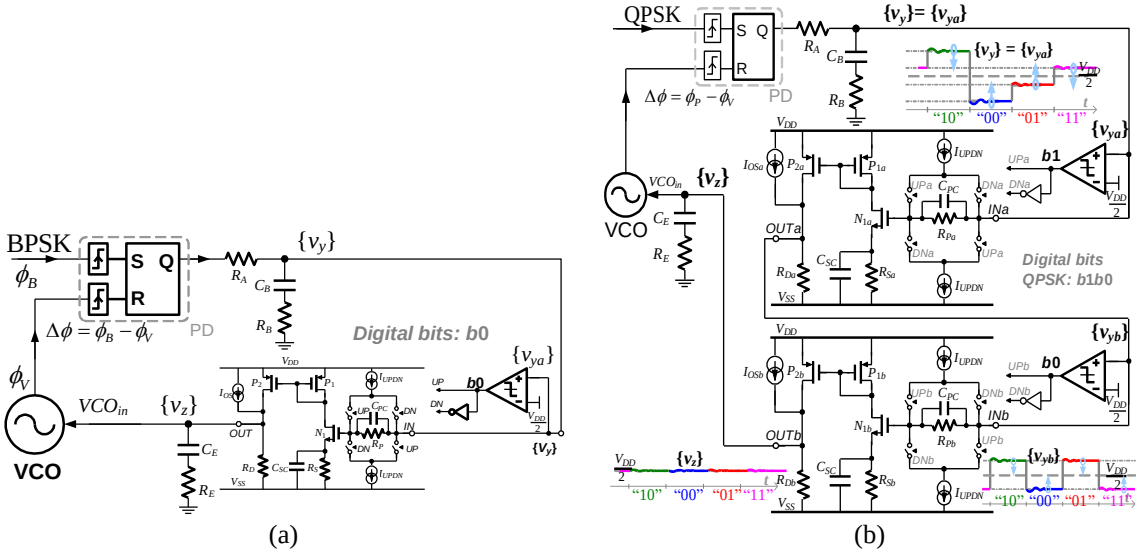


Figure 3. Proposed PLL-based BPSK, QPSK demodulators with a single-phase VCO: (a) BPSK and (b) QPSK

3. SYMBOL-ERROR-RATE ANALYSIS FOR THE SINGLE-PHASE PLL-BASED M-PSK DEMODULATORS

The aim of any error rate analysis is to understand how the error rate is related to the modulated signal-to-noise ratio (SNR). When the demodulator is under a locked condition, a constellation diagram of the BPSK and VCO signals entering an ideal phase detector (PD) of Figure 4(a) can be plotted in Figure 4(b). To simplify the symbol-error-rate (SER) analysis and without loss of generality, the VCO's phase (ϕ_{VCO}) is assumed to be at 0 rad while the two BPSK signals' phases (ϕ_{BPSK}) are at $+\pi/2$ and $-\pi/2$ for the symbols "1" and "0", respectively. The ideal PD is capable of measuring the phase difference between two signals accurately. The rising-edge-triggered RSFF employed in this work theoretically behaves closely to this ideal PD where its average output voltage is directly proportional to the phase difference over the range of 2π rads. All of the following data-error rate analysis will be carried out in a phase domain, only until the end where this phase-based data-error rate will be related back to a typical power-based *SNR*.

If the BPSK and VCO signals are disturbed by Gaussian noise plotted as clouds of signals shown in Figure 4(b), the probability density functions (*PDF*) of $\phi_{BPSK}, P_{\phi_{BPSK}}$ and of $\phi_{VCO}, P_{\phi_{VCO}}$ are assumed to be Gaussian, their corresponding *PDF* expressions can be written as (6a) and (6b).

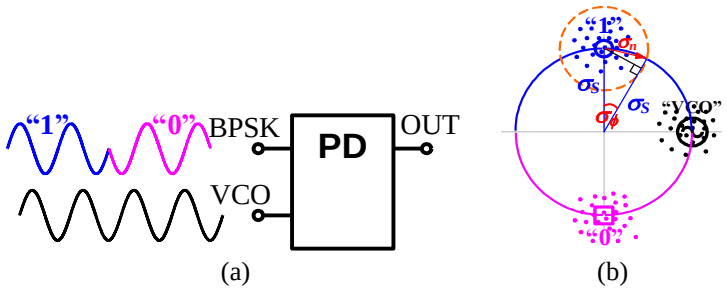


Figure 4. BPSK demodulation concept for symbol-error-rate calculation (a) ideal phase comparison and (b) constellation diagram

$$P_{\phi_{BPSK}@"1"}(x) = \frac{1}{2\sigma_{\phi bpsk}\sqrt{2\pi}} exp\left(\frac{-\left(x-\left(\frac{\pi}{2}\right)\right)^2}{2\sigma_{\phi bpsk}^2}\right), \quad (6a)$$

$$P_{\phi_{BPSK}@"0"}(x) = \frac{1}{2\sigma_{\phi bpsk}\sqrt{2\pi}} exp\left(\frac{-\left(x+\left(\frac{\pi}{2}\right)\right)^2}{2\sigma_{\phi bpsk}^2}\right) \quad (6b)$$

for symbols "1" and "0", respectively with $\sigma_{\phi_{bpsk}}$ being a standard deviation (*SD*) of ϕ_{BPSK} and

$$P_{\phi_{VCO}}(x) = \frac{1}{\sigma_{\phi vco}\sqrt{2\pi}} exp\left(\frac{-x^2}{2\sigma_{\phi vco}^2}\right) \quad (7)$$

where $\sigma_{\phi_{VCO}}$ being an *SD* of ϕ_{VCO}. These *PDF*'s are illustrated in Figure 5 where $P_{\phi_{BPSK}}$ and $P_{\phi_{VCO}}$ are in Figure 5(a). It is important to note that Gaussian noise or interference is usually assumed for disturbance in terms of amplitude [4]–[6]. However, in our case of the phase detection, this Gaussian distribution assumption of the phase distributions will be later justified for a large power SNR.

Let the phase difference $\Delta\phi$ between the BPSK signal and the VCO signal be $\Delta\phi_b = \phi_{BPSK} - \phi_{VCO}$, by following the proof and the conclusion developed in [28], [29], the *PDF* of this *phase difference* $P_{(\phi_{BPSK}-\phi_{VCO})} = P_{\Delta\phi b}$ can be expressed as (8a) and (8b),

$$P_{\Delta\phi_b@"1"}(\Delta\phi_b) = \frac{1}{2\sqrt{2\pi}\sigma_{\Delta\phi b}} exp\left(\frac{-\left(\Delta\phi_b-\left(\frac{\pi}{2}\right)\right)^2}{2\sigma_{\Delta\phi b}^2}\right), \quad (8a)$$

$$P_{\Delta\phi_b@"0"}(\Delta\phi_b) = \frac{1}{2\sqrt{2\pi}\sigma_{\Delta\phi b}} exp\left(\frac{-\left(\Delta\phi_b+\left(\frac{\pi}{2}\right)\right)^2}{2\sigma_{\Delta\phi b}^2}\right) \quad (8b)$$

when bit "1" or bit "0" is sent with the *SD* of $\Delta\phi_b$, $\sigma_{\Delta\phi b} = \sqrt{\sigma_{\phi bpsK}^2 + \sigma_{\phi vco}^2 - 2\rho_{\phi bv}\sigma_{\phi bpsk}\sigma_{\phi vco}}$, and $\rho_{\phi bv}$ being a correlation factor between ϕ_{bpks} and ϕ_{vco}. These $P_{\Delta\phi_{b@"1"}}(\Delta\phi_b)$and $P_{\Delta\phi_{b@"0"}}(\Delta\phi_b)$are also shown in Figure 5(b). The symbol-error rate by means of ideal phase comparison, SER_ϕ can be calculated by finding the shaded areas in Figure 5(b). This yields an *SER* of BPSK demodulation, $SER_{\phi,bpsk}$,

$$SER_{\phi,BPSK} = \int_{\frac{\frac{\pi}{2}}{\sigma_{\Delta\phi b}}}^{+\infty} \frac{2}{\sqrt{2\pi}} exp\left(\frac{-z^2}{2}\right) dz - \int_{\frac{\frac{3\pi}{2}}{\sigma_{\Delta\phi b}}}^{+\infty} \frac{2}{\sqrt{2\pi}} exp\left(\frac{-z^2}{2}\right) dz = 2Q\left(\frac{\frac{\pi}{2}}{\sigma_{\Delta\phi b}}\right) - 2Q\left(\frac{\frac{3\pi}{2}}{\sigma_{\Delta\phi b}}\right) \quad (9)$$

where $Q(x)$ is widely known as a Q function [30], [31]. The above expressions of $SER_{\phi,bpsk}$ and $\sigma_{\Delta\phi b} = \sqrt{\sigma_{\phi bpsk}^2 + \sigma_{\phi vco}^2 - 2\rho_{\phi bv}\sigma_{\phi bpsk}\sigma_{\phi vco}}$ clearly suggest that the quality of VCO signal in term of disturbing noise (through $\sigma_{\phi vco}$) has an impact as significantly as that from the BPSK signal (via $\sigma_{\phi bpsk}$). This significance of $\sigma_{\phi vco}$ to the overall *SER* is generally applicable to *m*-PSK demodulation as will be obvious in the following analysis results.

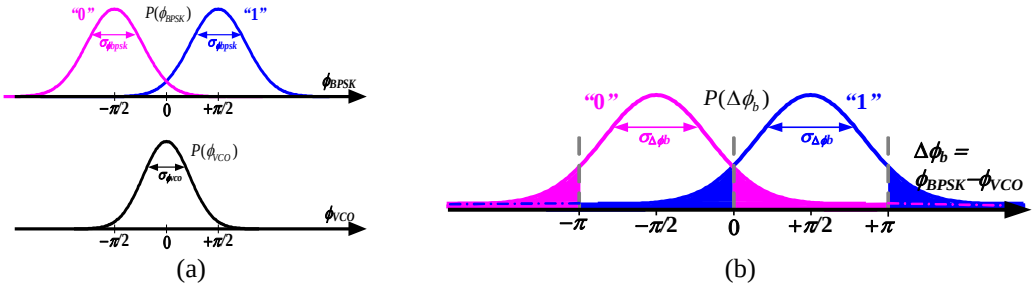


Figure 5. The *PDF*'s of (a) the BPSK and VCO phase signals at the phase detector's inputs, $P_{\phi_{BPSK}}$ and $P_{\phi_{VCO}}$ and (b) the corresponding phase difference, $P_{(\Delta\phi b)}$

Similarly, with the illustrations in Figure 6 the SER can also be found for QPSK by using the QPSK's constellation diagram in Figure 6(a) and the PDF of the phase difference between QPSK and VCO signals, $P_{(\phi QPSK-\phi VCO)} = P_{\Delta\phi q}$ in Figure 6(b). The SER for this QPSK demodulation, $SER_{\phi,QPSK}$ can be found as (10),

$$SER_{\phi,QPSK} = 2Q\left(\frac{\frac{+\pi}{4}}{\sigma_{\Delta\phi q}}\right) - 2Q\left(\frac{\frac{+7\pi}{4}}{\sigma_{\Delta\phi q}}\right) \tag{10}$$

with $\sigma_{\Delta\phi b} = \sqrt{\sigma^2_{\phi qpsk} + \sigma^2_{\phi vco} - 2\rho_{\phi qv}\sigma_{\phi qpsk}\sigma_{\phi vco}}$ and $\rho_{\phi qv}$ being a correlation factor between ϕ_{QPSK} and ϕ_{VCO}. The analysis can be repeated for a general case of *m*-PSK demodulation, the SER is found to be

$$SER_{\phi,m-PSK} = 2Q\left(\frac{\frac{+\pi}{m}}{\sigma_{\Delta\phi m}}\right) - 2Q\left(\frac{2\pi-\left(\frac{\pi}{m}\right)}{\sigma_{\Delta\phi m}}\right) \tag{11}$$

with $\sigma_{\Delta\phi m} = \sqrt{\sigma^2_{\phi m-psk} + \sigma^2_{\phi vco} - 2\rho_{\phi mv}\sigma_{\phi m-psk}\sigma_{\phi vco}}$ and $\rho_{\phi mv}$ being a correlation factor between $\phi m - psk$ and ϕvco. The value $\left((+\pi/m) \,/\, \sigma_{\Delta\phi m}\right)$ inside the *Q* function can be considered as a square-root of the phase SNR, therefore the last step in SER analysis is to relate a typical power SNR to this phase SNR. Converting a signal power *SNR* into its corresponding phase *SNR* can be done by re-considering a constellation diagram of symbol "1" in Figure 4(b). By simple geometry consideration, the largest phase standard deviation, σ_ϕ from the carrier phase of $\pi/2$ rad is given by (12),

$$\sigma_\phi = 2\,arcsin\left(\frac{\sigma_n}{2\sigma_S}\right) = 2\,arcsin\left(\frac{1}{2\sqrt{SNR_S}}\right) \tag{12}$$

where σ_S and σ_n are the rms values of the signal and the noise, respectively while $(\sigma_n/\sigma_S)^{-1}$ represents a typical square-root of the power-related signal-to-noise ratio, SNR_S for any *m*-PSK modulated and the VCO signals. The relation in (12) can thus be applied to obtain the largest$\sigma_{\phi bpsk}$, $\sigma_{\phi qpsk}$,…, $\sigma_{\phi m-psk}$ and $\sigma_{\phi vco}$ as required for SER calculations in (9) to (11). For a small $(\sigma_n/\,\sigma_S)$ value or a large SNR_S ratio, σ_ϕ in (12) can be approximated to $\sigma_\phi \simeq (\sigma_n/\,\sigma_S) \simeq 1/\sqrt{SNR_S}$ indicating a directly proportional relation between σ_ϕ and σ_n. This approximation therefore justifies the earlier assumption on Gaussian distribution of the large-SNR *m*-PSK and VCO signals' phases if their amplitudes are disturbed by Gaussian interference.

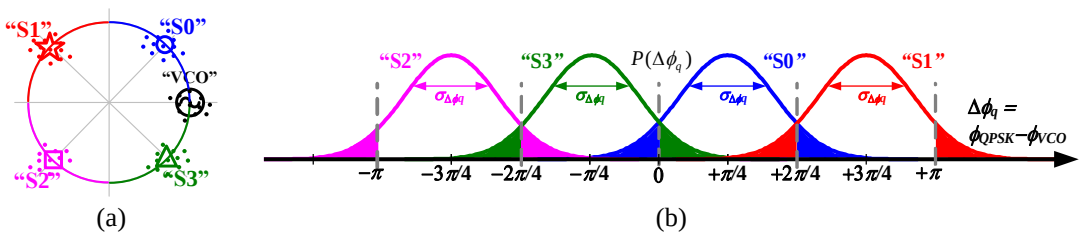


Figure 6. A coherent, PLL-based QPSK demodulation concept for SER analysis: (a) constellations and (b) PDF of $P_{(\Delta\phi q)}$

Re-consider (11) for a large value of *m* or a high signal-to-noise power ratio, the second term in the equation could be neglected and approximately reduced to

$$SER_{\phi,m-PSK} \simeq 2Q\left(\frac{\frac{+\pi}{m}}{\sigma_{\Delta\phi m}}\right) \simeq 2Q\left(\frac{\frac{+\pi}{m}}{\sqrt{\sigma^2_{\phi m-psk}+\sigma^2_{\phi vco}-2\rho_{\phi mv}\sigma_{\phi m-psk}\sigma_{\phi vco}}}\right) \quad (13)$$

If $\sigma_{\phi m-psk}$ and $\sigma_{\phi vco}$ are related by a simple factor α, e.g., $\sigma_{\phi vco} = \alpha\sigma_{\phi m-psk}$, (16) can be re-written as (14).

$$SER_{\phi,m-PSK} \simeq 2Q\left(\frac{\frac{+\pi}{m}}{\sigma_{\phi m-psk}\sqrt{1+\alpha^2-2\rho_{\phi mv}\alpha}}\right) \simeq 2Q\left(\frac{\frac{+\pi}{m}}{2\,arcsin\left(\frac{1}{2\sqrt{SNR_S}}\right)\sqrt{1+\alpha^2-2\rho_{\phi mv}\alpha}}\right) \quad (14)$$

For a large value of SNR_S, this gives $\left(\frac{1}{2\sqrt{SNR_S}}\right) \cong \frac{1}{2\sqrt{SNR_S}}$ and this SER is reduced to

$$SER_{\phi,m-PSK} \simeq 2Q\left(\frac{(\pi/m)\sqrt{SNR_S}}{\sqrt{1+\alpha^2-2\rho_{\phi mv}\alpha}}\right) \quad (15)$$

In the case of an ideal VCO where $\sigma_{\phi vco}$is negligibly small or $\alpha = 0$, the expression can be further simplified to (16).

$$SER_{\phi,m-PSK} \simeq 2Q\left((\pi/m)\sqrt{SNR_S}\right) \quad (16)$$

Comparing this to the SER_{m-PSK} expression from a well-known adjacent-symbol distance-measuring method [4]–[6],

$$SER_{dist,m-PSK} \simeq k \cdot Q\left(sin(\pi/m)\sqrt{SNR_S}\right) \quad (17)$$

where $k = 1$ for $m = 2$ (BPSK case) and $k = 2$ for $m \geq 4$ (this formula excludes the SER from the QPSK demodulation using an orthogonal quadrature VCO for bit recovery). For a large value of *m*, this can be approximated to the same expression in (16). In case of BPSK demodulation ($m = 2$), the SER from the distance measuring method of (17) is reduced to $SER_{dist,BPSK} \simeq Q\left(sin(\pi/2)\sqrt{SNR_S}\right) \simeq Q\left(\sqrt{SNR_S}\right)$ which is the same as the *BER* of the binary antipodal signal [4]. The discrepancy between the two SER analysis techniques is quite significant for BPSK demodulation where $SER_{\phi,BPSK} \simeq 2Q\left((\pi/2)\sqrt{SNR_S}\right)$with $\alpha = 0$ as compared to $SER_{dist,BPSK} \simeq Q\left(\sqrt{SNR_S}\right)$. That is, the ideal phase-detection technique (with an ideal zero-noise VCO) would render a better SER owing to the presence of (π/2) inside the $Q(\cdot)$ function. However, if a non-ideal VCO is considered where the VCO's SNR is the same as that of the BPSK signal but with zero correlation, i.e., $\sigma_{\phi vco} = \sigma_{\phi bpsk}$ (or $\alpha = 1$) and $\rho_{\phi bv} = 0$, while in another case $\alpha = \sqrt{2}$ and $\rho_{\phi bv} = 1/\left(2\sqrt{2}\right)$, the $SER_{\phi,QPSK}$ of (15) is modified to (18),

$$SER_{\phi,BPSK}\big|_{@\alpha=1,\rho_{\phi bv}=0} = SER_{\phi,BPSK}\big|_{@\alpha=\sqrt{2},\rho_{\phi bv}=\frac{1}{2\sqrt{2}}}$$

$$\simeq 2Q\left(\frac{(\pi/2)\sqrt{SNR_S}}{\sqrt{1+\alpha^2-2\rho_{\phi bv}\alpha}}\right) \simeq 2Q\left(\frac{(\pi/2)\sqrt{SNR_S}}{\sqrt{2}}\right) \simeq 2Q\left(1.111\sqrt{SNR_S}\right) \quad (18)$$

which is not too far from $SER_{dist,BPSK}$ obtained from the distance-measuring technique. The practical values of α as well as $\rho_{\phi mv}$ inside the *m*-PSK demodulation would be another important issue for future study.

Theoretically, under a matched-filter scenario, the SNR_S can be further converted into energy per bit (E_b) per noise power spectral density (N_o) or E_b/N_0 by $SNR_S = P_S/P_n = P_S/\sigma_n^2 = E_S/(N_0/2) = \log_2(m)E_b/(N_0/2)$ [4], [6] with E_S being the signal symbol energy. This turns (15) into:

$$SER_{\phi,m-PSK} \simeq 2Q\left(\frac{(\pi/m)\sqrt{(log_2 m)(E_b/(N_0/2))}}{\sqrt{1+\alpha^2-2\rho_{\phi mv}\alpha}}\right) \quad (19)$$

As compared to the SER from the distance calculation of (20),

$$SER_{dist,m-PSK} \simeq k \cdot Q\left(sin(\pi/m)\sqrt{(log_2 m)(E_b/(N_0/2))}\right) \quad (20)$$

where $k = 1$ for $m = 2$ (BPSK case) and $k = 2$ for $m \geq 4$. Comparison plots of *SER vs* E_b/N_0 (as usually done in [4], [6]) from (19) and (20) are illustrated in Figure 7 with $\alpha = 0$. Specifically, for the $SER_{\phi,BPSK}$, two cases with (*i*) $\alpha = 0$ and (*ii*) $\alpha = 1$, $\rho_{\phi bv} = 0$ are plotted in the figure where the latter gives the identical curve as that of $SER_{\phi,QPSK}$ with $\alpha = 0$. With a low-noise VCO (small α), the BPSK demodulation using a phase-detection technique has potential to outperform the conventional distance-decision method.

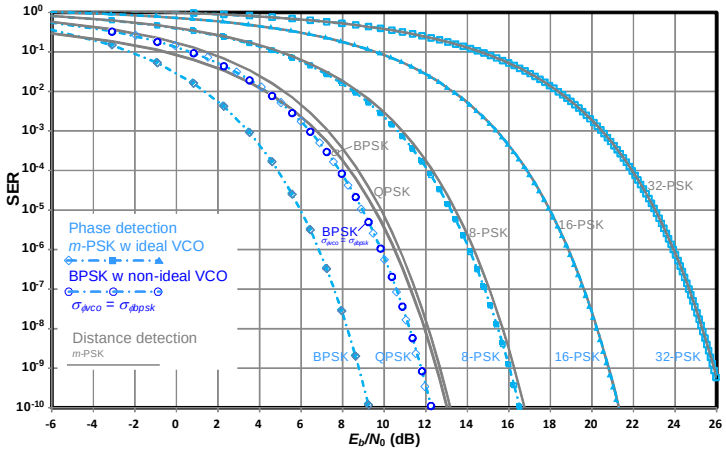


Figure 7. Calculated SER vs Eb/No using the phase detection technique as compared to the conventional distance-decision technique [4], [6]

4. BUILDING BLOCKS AND DESIGN CONSIDERATIONS

Circuit design techniques for the building blocks of the proposed demodulators for CMOS integration will be described in this section. Stability issue is a major concern in the demodulator loop design. However, this loop control is closely similar to a classic negative-feedback PLL system.

4.1. Pole/zero compensation for the single-bit phase-control circuit

A voltage shifter and an NMOS resistive-source-degeneration trans conductor constitute an important part inside a shifting/re-scaling phase controller of Figure 2(b). They are redrawn in Figure 8 with capacitors C_{PC} and C_{SC} respectively connected across R_S (=1/G_S) and R_P (=1/G_P) for pole compensation as in Figure 8(a). The small-signal transfer function of this circuit Figure 8(b) is (21),

$$g_{mps}(s) = \frac{i_{dN}}{v_{in}} = \frac{g_{mN}}{\left(1+\frac{g_{mN}}{G_S(1+sR_SC_{SC})}\right)}\left[1 + s\frac{C_{gsN}}{g_{mN}}\frac{\left(1+\left(\frac{G_S}{G_P}\right)\frac{(1+sR_SC_{SC})}{(1+sR_PC_{PC})}\right)}{\left(1+\left(\frac{G_S}{g_{mN}}\right)(1+sR_SC_{SC})\right)}\right]^{-1} \quad (21)$$

where C_{gsN} is the gate-source capacitance of N_1 with g_{mN} being a small-signal transconductance of N_1. Under a special condition $\frac{C_{SC}}{G_S} = \frac{C_{PC}}{G_P}$ or $C_{SC}R_S = C_{PC}R_P$, the i_{dN}/v_{in} can be reduced to (22).

$$g_{mps}(s) = \frac{i_{dN}}{v_{in}} = \frac{g_{mN}\left(\frac{G_S}{g_{mN}}\right)\left(1+s\frac{C_{SC}}{G_S}\right)}{\left[1+\left(\frac{G_S}{g_{mN}}\right)+s\left[\frac{C_{gsN}}{g_{mN}}\left(1+\frac{G_S}{G_P}\right)+\left(\frac{C_{SC}}{g_{mN}}\right)\right]\right]} \quad (22)$$

The presence of the zero at $s_s = -1/\left(\frac{C_{SC}}{G_S}\right) = -1 / (R_S C_{SC})$ can help improve the demodulator's stability. The pole at $S_p = -\left[1 + \left(\frac{G_S}{g_{mN}}\right)\right]\left[\frac{C_{gsN}}{g_{mN}}\left(1 + \frac{C_S}{G_P}\right) + \frac{C_{SC}}{g_{mN}}\right]^{-1}$ can be effectively cancelled by such zero if the condition $\frac{C_{SC}}{G_S} g_{mN} = C_{gsN}\left(1 + \frac{C_S}{G_P}\right)$ or $C_{SC} R_S = \frac{C_{gsN}}{g_{mN}}\left(1 + \frac{R_P}{R_S}\right)$is met. This simply yields (23),

$$\frac{i_{dN}}{v_{in}} = g_{mps}(s) = \frac{g_{mN}\left(\frac{G_S}{g_{mN}}\right)}{\left(1+\left(\frac{G_S}{g_{mN}}\right)\right)} = \frac{g_{mN}}{1+\left(\frac{g_{mN}}{G_S}\right)} = \frac{g_{mN}}{1+g_{mN}R_S} \tag{23}$$

which is the well-known *v*-to-*i* conversion for a resistive source-degeneration circuit.

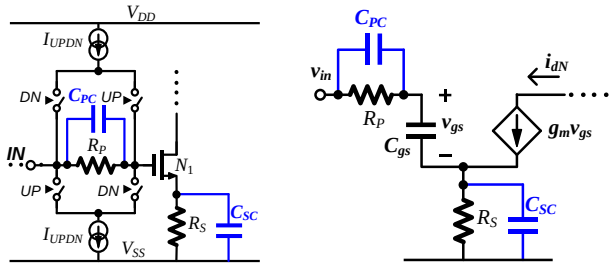


Figure 8. Pole compensation (a) with capacitors C_{PC}, C_{SC} and (b) its small-signal circuit

4.2. A positive-edge-triggered RSFF as a phase detector

The positive-edge-triggered RSFF with characteristic shown in Figure 1 can be simply constructed by cascading a positive-edge detector followed by an RS latch as depicted in Figure 9. In Figure 9(a), the positive-edge detection is carried out by performing an AND operation between the incoming modulated signal and its inverted delayed (using three simple logic inverters). The implemented *RS* latch is based on a well-known NOR-gate feedback structure. The measured characteristic of this phase detector is shown in Figure 9(b) where the average output voltage is plotted against the phase difference with the 60 MHz logic signals.

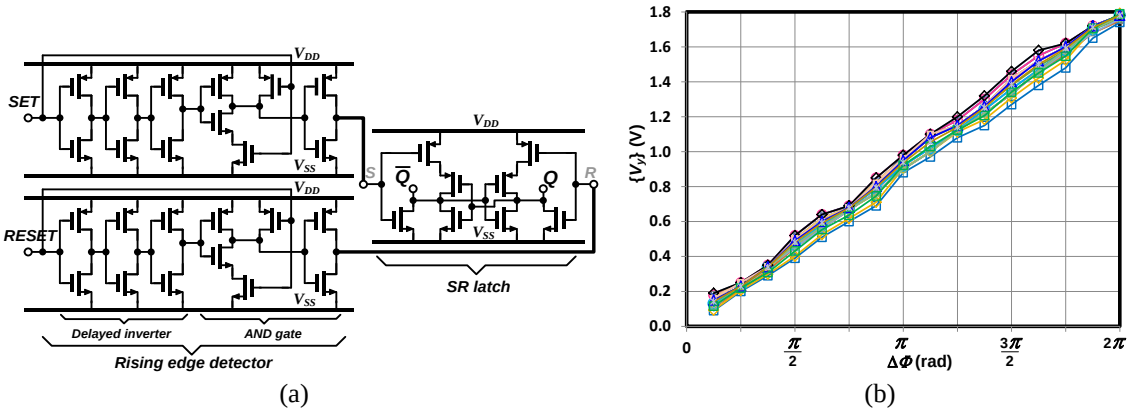
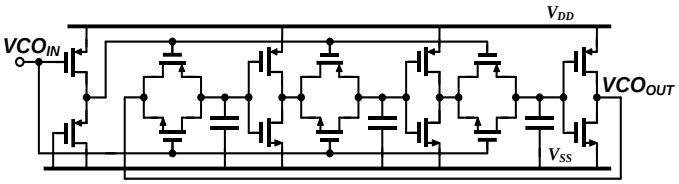


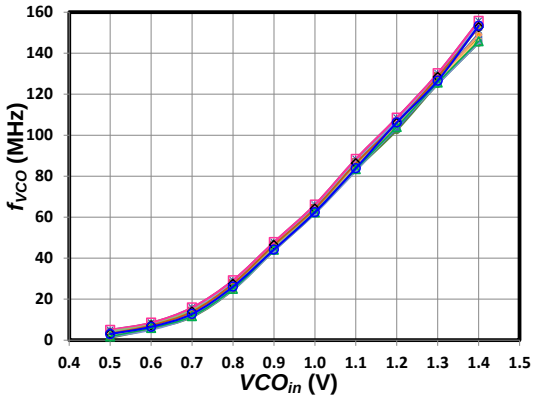
Figure 9. Positive-edge-triggered RSFF: (a) schematic and (b) characteristic with 60 MHz signals from 20 chips

4.3. A voltage-controlled oscillator

A three-stage inverter-based/transmission-gate ring VCO in Figure 10 [32] has been employed due to its simplicity. In Figure 10(a), the frequency tuning is done by controlling the gate voltages of NMOS and PMOS inside the three transmission gates. The measured VCO characteristic is shown in Figure 10(b) displaying a tuning range from 5 to 150 MHz when VCO_{in} is varied from 0.5 to 1.4 V. The VCO's constant K_{VCO} has been found to be around 400π Mrad/s/V.



(a)



(b)

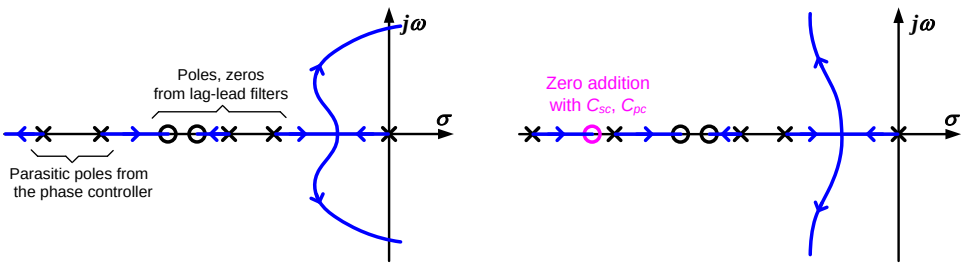
Figure 10. Voltage-controlled oscillator (a) VCO schematic [30] and (b) characteristic from 20 chip samples

4.4. Stability consideration for the proposed BPSK and QPSK demodulators

The BPSK demodulator in Figure 3(a) is considered as a design example with the loop filters being a lag-lead type. The open-loop transfer function $T_{OL}(s)$ is given by (24),

$$T_{OL}(s) = K_{PD}\underbrace{\left(\frac{1+sR_BC_B}{1+s(R_A+R_B)C_B}\right)}_{1^{st}\text{ lag-lead filter}}\overbrace{g_{mps}(s)\underbrace{\frac{1}{\left(1+s\frac{C_{gsP}}{g_{mP}}\right)}}_{\text{current mirror}}}^{\text{phase controller}}\underbrace{\left(\frac{R_D(1+sR_EC_E)}{1+s(R_D+R_E)C_E}\right)}_{2^{nd}\text{ lag-lead filter}}\frac{K_{VCO}}{s} \quad (24)$$

where the phase detector constant $K_{PD} = V_{DD}/2\pi$ for the rising-edge-triggered RSFF. The root locus in Figure 11 is explored for the demodulator design where the root locus of the uncompensated phase controller is conceptually shown in Figure 11(a). The loop stability can be enhanced by utilizing an additional zero introduced by the capacitors C_{SC} and C_{PC} inside the phase controller as already analyzed in Figure 8 and $g_{mps}(s)$ can be taken from (22). The original root locus is modified into the new one shown in Figure 11(b) where better stability can be clearly observed. Theoretically, as already mentioned in a design of the 1-bit phase controller section 4.1, the additional zero can be used to perfectly cancel the phase controller's pole which would further improve the loop stability (its root locus will be similar to that of Figure 11(b).



(a) (b)

Figure 11. The BPSK demodulator design with a root locus: (a) original poles and zeros and (b) zero addition with compensation capacitors C_{SC}, C_{PC}

5. ESPERIMENTAL VERIFICATION

The proposed single-phase lock-loop BPSK/QPSK demodulators have been fabricated in UMC 0.18 µm CMOS process. The chip microphotograph is shown in Figure 12 where the two demodulators share some circuit together (PD, VCO, phase controller). The carrier frequency at 60 MHz has been selected for deep-implant HBC applications. The BPSK and QPSK modulators as well as a 2^{16}–1 pseudo-random symbol generator has been implemented with a FPGA platform (Xilink Zybo zynq 7000).

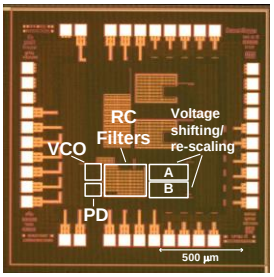
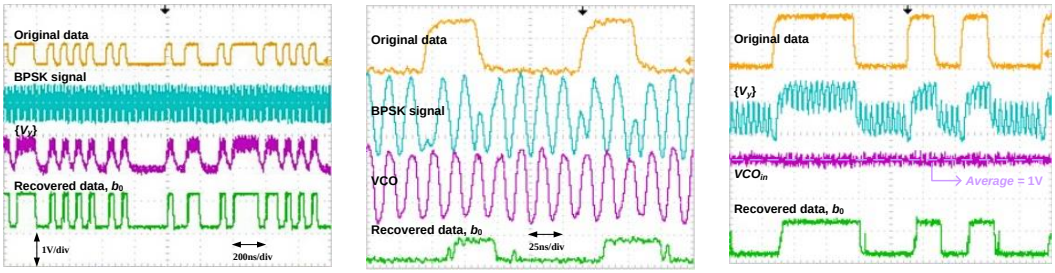


Figure 12. Chip microphotograph

5.1. BPSK demodulator

BPSK demodulation and bit recovery is illustrated in Figure 13. In Figure 13(a), the digital bit has been correctly recovered when the locked condition has been successfully attained. Figure 13(b) displays the frequency-locked VCO signal with a constant phase relative to the BPSK signal regardless of the modulating data bits which solidly confirms the proposed coherent demodulation concept. Figure 13(c) demonstrates how the phase controller operates on the filter's output after the RSFF, $\{v_y\}$ which produces the constant VCO's input voltage, $\{v_z\}$. It can be seen that $\{v_y\}$ shows two distinguished levels according to the original data bits (with a high-frequency component equal to the carrier frequency). The recovered data bit b_{rx0} is then obtained from $\{v_y\}$ with a bandwidth-limited comparator. The BPSK demodulator's capture range is between 55 MHz and 65 MHz. It achieves the maximum bit rate of 25 Mbps while consuming 0.68 mW. This essentially gives a figure of merit (FoM) in term of energy per bit, E_b equal to 27.2 pJ.



(a) (b) (c)

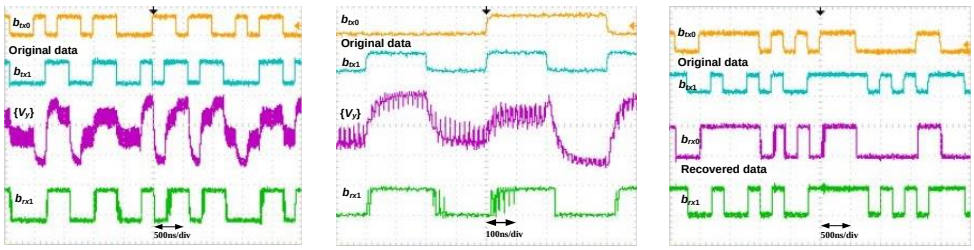
Figure 13. BPSK demodulation: (a) bit recovery at 25 Mbps, (b) a constant-phase VCO under a locked condition regardless the data bits and (c) an operation by the phase controller $\{v_y\}$, $\{v_z\}$ = VCO_{in}

5.2. QPSK demodulator

Figure 14 shows a lock condition inside the QPSK demodulator. Figure 14(a) depicts the signal $\{v_y\}$ at the RSFF filter's output possessing four different levels which uniquely correspond to the original 2-bit data symbols $b_{tx1}b_{tx0}$. The signal $\{v_y\}$ enters the first comparator to produce the first data bit (MSB), b_{rx1}. The closed-up of the similar measurement is also shown in Figure 14(b) where $\{v_y\}$ clearly illustrates the loop transient dynamic. Two digital data bits $b_{rx1}b_{rx0}$ can be successfully recovered as compared to the original bits $b_{tx1}b_{tx0}$ in Figure 14(c). The QPSK demodulator achieves a capture range from 58 to 63 MHz. The loop can perform demodulation at the maximum symbol rate of 12.5 Msymb/s where it consumes 0.79mW hence E_b = 31.7 pJ. Charts in Figure 15 summarize power contributions from each individual blocks for both BPSK Figure 15(a) and QPSK Figure 15(b) demodulators.

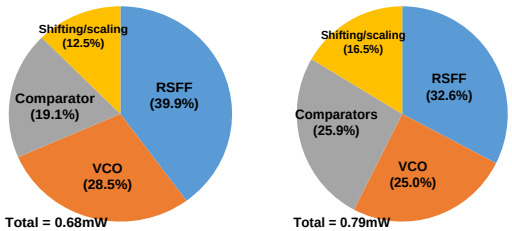
An SER measurement has been carried out by comparing the recovered symbol to its transmitted counterpart using appropriate data re-timing and sampling by another FPGA platform. The online symbol-error counting algorithm has also taken into account the phase ambiguity issue. The SER has been measured against the modulated signal's SNR_S, i.e., the power ratio between the BPSK or QPSK modulated signal P_S and the noise P_n at the input of the demodulator. Plots of the measured SER vs E_b/N_o have been obtained as shown in Figure 16 using the relation $SNR_S = \log_2(m)E_b/(N_0/2)$ as suggested in section 3 [4], [6]. These measured SERs from the BPSK and QPSK demodulators are also compared with the calculations from (19) and (20) using the phase detection and the conventional distance-decision methods, respectively.

Table 1 summarizes the performance of the demodulator prototypes as compared to the prior arts. The proposed demodulators' E_b (= FoM) are plotted against the process's (node size)$^{-1}$ and compared with the previous works as shown in Figure 17. It can be seen that the proposed demodulators are highly competitive as compared to the other locked-loop-based BPSK, QPSK demodulators. The best FoM is achieved by the non-locked-loop BPSK demodulator in [22] whose architecture is somewhat non-modular and rather hard to be extended for demodulating QPSK or *m*-PSK signals.



(a) (b) (c)

Figure 14. QPSK demodulation: (a) bit recovery at 5 Msymb/s, (b) the close-up of (a) showing the dynamic of $\{v_y\}$ and (c) recovered bits b_{rx1}, b_{rx0} compared to the original data b_{tx1}, b_{tx0}



(a) (b)

Figure 15. Power dissipation breakdowns for (a) BPSK and (b) QPSK demodulators

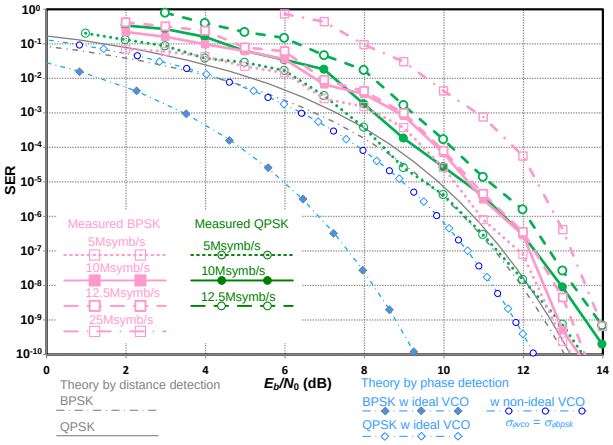


Figure 16. Measured SER plotted against Eb/N0 from the BPSK and QPSK demodulators

Table 1. Performance comparison with high-performance BPSK, QPSK demodulators

References	[12] (TCASI' 12)	[18] (LSSC' 20)	[11] (JSSC' 18)	[10] (JSSC' 15)	[6] (JSSC' 11)		[16] (JSSC' 08)	[17] (JSSC' 11)	[13] (JSSC' 10)	This work	
Demodulation	QPSK	BPSK	BPSK	BPSK	BPSK	QPSK	BPSK	BPSK	DPSK	BPSK	QPSK
CMOS process, node size	0.18 µm	0.18 µm	0.18 µm	0.13 µm	65 nm		0.18 µm	65 nm	0.18 µm	0.18 µm	
V_{DD}	1.8 V	0.9 V	2.0 V	1.2 V	1.2 V		1.8	1.2	1.8 V	1.8 V	
Techniques	Carrier-recovery (CR)	Open-loop, data flipping	PLL-based, transition detection	Costas Delay-Locked loop	Costas loop with frequency detection loops		Digital Lock Loop + *I*/*Q* gen.	Injection Lock + Amplitude detection	Open loop, CR from power carrier	PLL-based, single-phase, single loop with a positive-edge RSFF and analog phase controllers	
Carrier freq. (MHz)	2400	13.56	13.56	21	9300	9700	1400	750	22	60	60
Max. data rate (Mbps)	1	13.56	0.211	1.3125	2500	2500	622	5	2	25	25 (12.5 Msymb/s)
Power	10.8 mW	12.2 µW	217 µW	2.0 mW	79 mW	110 mW	40.8 mW	228 µW	5.7 mW	0.68 mW	0.79 mW
BER (or SER)	$< 10^{-3}$	$< 10^{-6}$	10^{-5}	N/A	$<10^{-9}$	$<10^{-11}$	$<4.4\times 10^{-13}$*	1.2×10^{-3}	$<10^{-7}$	$<7.9\times 10^{-10}$	SER $<9.8\times10^{-10}$
$FoM = E_b$ (pJ/bit)	10800	0.9	1027	1524	31.6	44	65.6	45.6	2850	27.2	31.7
Area (mm^2)	0.097**	0.00383	0.137	N/A	0.27**	0.27**	0.0315	0.116	0.322	0.022	0.063

*with a limiting pre-amplifier, ** approximated from the literatures

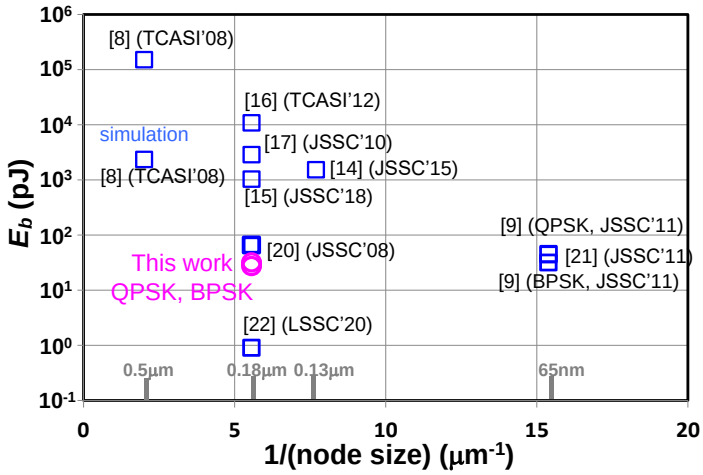


Figure 17. E_b $(= FoM)$ plot against 1/(process node size)

5.3. Discussion and future works

Although the measured results show competitive performances, the proposed demodulator can be further improved. This can be done at both circuit and architecture levels. Improvement on three important aspects, namely, power consumption, lower V_{DD} and SER can be done in the future works as briefly overviewed below:

a) Power consumption: The power consumption of the positive-edge-triggered RSFF can be further reduced by using a current-mode-logic (CML) circuit structure. From the charts in Figure 15, this would help bring down both demodulators' overall power consumption as well as improve their FoMs.

b) Lower supply voltage VDD: Under a very low V_{DD} e.g. $V_{DD} \leq 0.5$ V, the proposed demodulation principle can still be applied with all-digital circuits where all the signal processing is considered in time domain. Therefore, a pulse-width to digital converter (PW2D) can be employed to measure the RSFF output's pulse width rendering a digital number for a digital phase controller which in turn provides an appropriate digital number to the control input of the digital-controlled oscillator (DCO). Alternatively, the phase control operation can be executed directly on the incoming *m*-PSK signal by another RSFF while the other input selectively comes from the DCO with the appropriate phase shift. The pulse width from this dedicated phase-control RSFF's output can then be converted to a digital number to control the DCO.

c) Symbol-error rate: From the SER analysis in (9) to (11), it is persuasive trying to reduce $\sigma_{\phi vco}$ of the VCO to lower the SER. One way to achieve this is by providing a low-interference control signal $\{v_z\}$ to the VCO's input from the phase controller. This can be done by utilizing multiple phases from the VCO, e.g., $\phi_{VCO} = \{0, \pi\}$ and $\{0, \pi/2, \pi, 3\pi/2\}$ for BSPK and QPSK, respectively with an equal number of RSFF's. Averaging the output signals from these RSFF outputs can be co-operated with a sub-ranging process to perform the necessary phase control. Such averaging operation can help reduce level of interference to VCO's input hence lowering the $\sigma_{\phi vco}$ and the overall SER. The chip results of such concept will be reported in another literature.

6. CONCLUSION

Coherent BPSK and QPSK demodulators using a single-phase VCO inside a single-loop PLL-based structure has been reported. The demodulators are truly modular and they employ a simple phase controller that operates on the average voltage from the rising-edge RSFF phase detector's output. The demodulator chip prototype has been fabricated in a 0.18 μm CMOS process from UMC. The measurements have successfully verified the proposed m-PSK demodulation concept with competitive energy-per-bit figure.

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