RESEARCH ARTICLE

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Design and Implementation of Low Power Time-To-Digital Converter using MGDI Technique

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Abstract: This paper introduces a novel Time to Digital Converter (TDC) architecture based on the Modified Gate Diffusion Input (MGDI) technique, which is derived from the well-established GDI method. Through the utilization of MGDI-based logic gates and digital circuitry, this innovative approach leads to a substantial reduction in the number of transistors required for implementation. As a result, it offers significant advantages in terms of circuit area, power consumption, and propagation delay, while simultaneously simplifying the complexity of the overall logic design. The functional blocks within the TDC have been optimized to efficiently process an internal clock frequency of 5MHz. This achievement is realized using cutting-edge 90nm MGDI technology, operating at a supply voltage of 1V. Practical implementation of this design can be carried out seamlessly with Cadence Virtuoso tools in the 90nm technology node. In essence, this research effort represents a promising advancement in the realm of time-to-digital conversion. By harnessing the capabilities of MGDI and its transistor-saving attributes, the proposed TDC not only enhances performance but also addresses critical concerns such as power efficiency and chip area utilization. These advancements make it a compelling choice for applications requiring precise time measurements, while the compatibility with contemporary technology nodes ensures its relevance and applicability in modern integrated circuit design.

Keywords: Gate Diffusion Input (GDI), Time to Digital Converter (TDC), Modified Gate Diffusion Input (M-GDI), Low Power.

1. Introduction

VLSI technology is being enhanced over these years thereby increasing the performance of the chip in basic constraints such as delay, area, power [1]. In most computing systems, the time to digital converter (TDC) plays a critical role [2, 3]. It is accountable for converting the time interval into digital values which exists between two clock edges. The time interval between two signal pulses is determined using TDC. It converts the arrival difference between two input pulses known as START and STOP pulses into a binary code. TDC have been broadly used for

making very accurate time measurement. This high accuracy is obtained by sub division of reference clock and by referencing delay time of the buffer to an external clock. TDC is used in places where high resolution time measurements are needed [4, 5]. It's employed in a variety of applications, including jitter measurements, space research instruments and ADPLLs [6, 7]. It is frequently utilized in high precision time-of-flight [8] due to recent advancements in TDC performance. TDC has been utilized in the field of particle and high-energy physics for more than a decade to measure time intervals. In low-power and low-voltage applications, optimizing numerous components for power and speed is a significant concern. The GDI (Gate Diffusion Input) approach can be used to solve these problems.

GDI is a low-power design approach that employs a basic cell. [9] G (common gate input of PMOS and NMOS), N (input given to the source/drain of NMOS), and P (input given to the source/drain of PMOS) are the three inputs in the cell. Simple adjustments in the GDI cell's input settings are used to secure certain Boolean functions. GDI method also provides an enhancement in tolerating hazards [10]. GDI methodology reduces the complexity of cell and offers better less static power dissipation and logic swing [11, 12]. This technology can be used to create low-power circuits and high speed with minimum transistors [13]. The main disadvantage of GDI is that the bulk terminal is not correctly biased, resulting in threshold drop in the circuit. MGDI is proposed to address this issue. With the advancement of technology, the influence of source body voltage on transistor threshold voltage has increased to the point that it now exceeds the body coefficient. The MGDI technique uses only two transistors to understand a large range of logic functions [14, 15]. This technique can be utilized to construct high-speed and low-power circuits using fewer transistors while still improving power characteristics [16]. MGDI is an advanced version of GDI [17]. It is comparable to a GDI cell, except that in MGDI, the majority of NMOS is fixed to VDD and PMOS is fixed to GND, respectively [18]. In this paper static TDC is compared with MGDI based TDC.

2. Conventional TDC

TDC converts the delay time between two digital pulses, such as the start and stop signals, into digital code. Figure 1 depicts the delay line TDC block, while Figure 2. depicts the static or conventional TDC circuit, which consists of a delay element buffer and a D flip flop. Here, ripples of start signal through the buffer chain. The outputs of buffers are bridged to the flip-flops. The operation of the delay line buffer TDC is shown in Fig. 3. The flip-flops sample the status of the delay line once the stop signal arrives. The reference clock is subdivided and TDC intervals improves the measurement resolution [19]. The resolution is increased by delaying the original reference clock, and the resolution is dependent on the delay of the delay element in the chain. As soon as the stop signal arrives, the sampling technique freezes the state of the delay line [20].

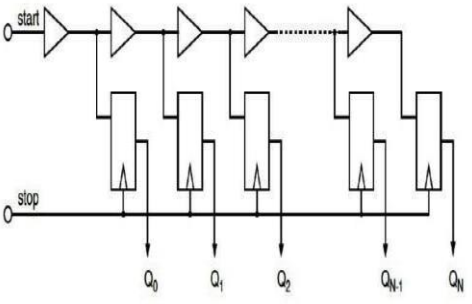

Figure 1. Delay Line TD

At the sampling element's output, all delay stages that have been passed by the start signal have a HIGH value, while those that have not been passed by the start signal have a LOW value. The position of the HIGH-LOW transition in the thermometer code (1's and 0's) designates the point up to which the start signal could spread within the time interval spanned by start and stop signals. But the complexity of the system is very high and more number of transistors are required. Where there is a requirement of Time-Interval measurement in the field such as particle and high energy TDCs are employed. Its basic structure i.e. N-bit delay line TDC comprises of a chain of 2N delay units. The digital pulse is substantially propagated through a delay line when the start signal is enabled and then the stop signal arrives. In this stage the output digital states are sampled by a D flip-flops (D-FF).

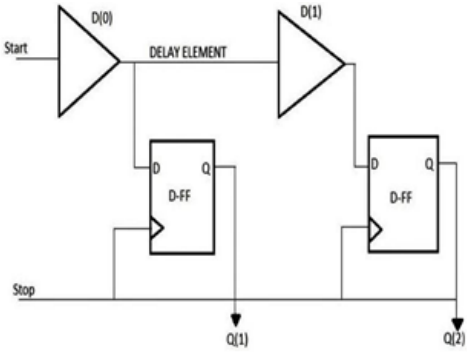

Figure 2. Static TDC

The current thermometer code of DFFs is then converted to a binary code in relation to the input delay line by a thermometer to binary decoder (Tin). A consistent resolution can be achieved by dividing one clock cycle asynchronously into small time intervals. It also improves high dynamic range measurements.

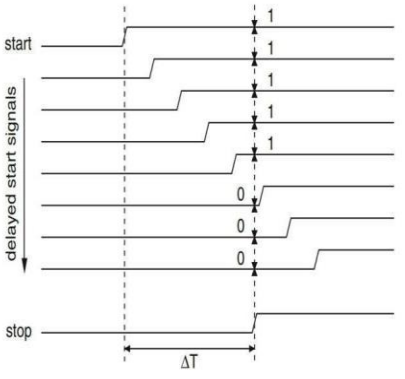

Figure 3. Operation of delay line TDC

3. Proposed Modified Gate Diffusion Input Tdc

MGDI is a method that is built on the GDI method. MGDI is a technology for creating low-power digital circuits that has been presented. GDI cell is like CMOS inverter, but the difference is it consists of 3 inputs namely P, N and G. To minimize the bulk impact, the PMOS and NMOS bulks are coupled to the diffusion P and N. Different Boolean functions can be produced by making simple changes to GDI. In comparison to conventional CMOS, it also reduces gate leakage current and sub-threshold leakage current. When implemented in or below 90nm technology, however, GDI's performance suffers. Traditional p-well development does not allow for the fabrication of GDI cells.

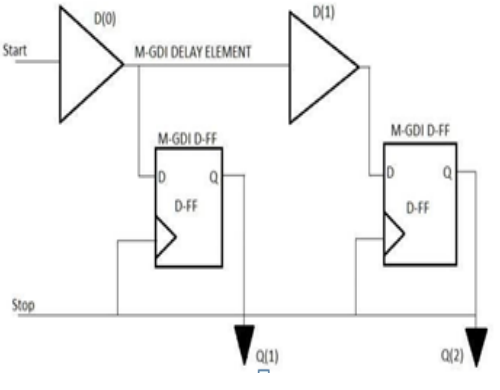

Figure 4. M-GDI Based TDC

MGDI overcomes the drawbacks of GDI cell. Here, the bulk of NMOS is connected to a GND or low constant voltage, while the bulk of a PMOS is connected to a VDD or high

constant voltage or supply voltage. This MGDI can be implemented with all the current process of fabrication. By using single MGDI cell different logic operations can be designed. AND gate, OR gate is implemented using only 2 transistors while in conventional CMOS 6 transistors are required and only 3 transistors are required to design XOR and XNOR in MGDI whereas it is 8 in CMOS logic. Using this basic MGDI concept, MGDI based inverter and D flip flop is designed. Figure 4 show the circuit of MGDI based TDC. Here, the number of transistors gets reduced and power consumption also gets reduced. In high performance applications the power dissipation becomes one of the most key restrictions. The optimization of primary logic gates is critical for improving the performance of a wide range of high-performance and low-power devices. MGDI helps to overcome these limitations.

A. Preliminary

- D-flip flop - The D flip flop is made up of a gated SR flip-flop and an inverter connected between the inputs that allows for single input data. D flip flop is more efficient compared to other clocked types as it ensures that both the inputs are never equal to 1.
- Delay Buffer - A digital buffer is a component that isolates the input from the output by using either no voltage or the same voltage as the input. To achieve high input impedance, a voltage buffer is employed.
- MGDI cell - The modified GDI cell has a similar basic structure to the GDI cell. It includes three input terminals like G, N, and P. The bulk or body of PMOS is fixed to VDD, whereas the bulk or body of NMOS is fixed to ground in a modified GDI cell. Figure 5 depicts the fundamental circuit of a modified GDI cell.

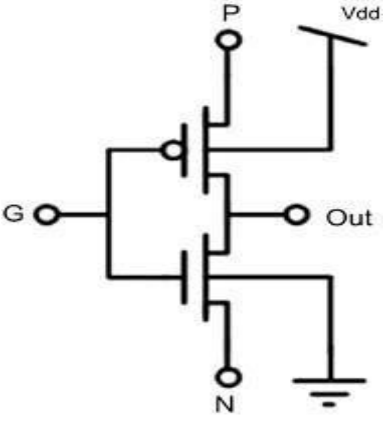

Figure 5. Structure of MGDI Cell

The modified GDI logic is implemented in all current CMOS transistor fabrication technologies. The MGDI technique's main benefit is that it minimizes transistor area, resulting in lower power consumption. As a result, using the MGDI technique, it is simple to construct a complex circuit.

4. Result and Discussion

Using Cadence 90nm technology, both static and MGDI-based TDCs are analyzed and simulated. Here the power consumption of the MGDI based TDC is much less than the static TDC. Fig. 6. shows the schematic view of static TDC. Fig. 7. shows the output waveform of static TDC. Fig. 8 shows the schematic view of M-GDI TDC. Fig. 9 shows the output waveform of M-GDI TDC. Table I represent the average power and peak to peak power consumption comparison of static TDC and proposed MGDI TDC. Fig. 10 depicts the peak to peak and average power consumption of static TDC at 1V. Fig. 11 shows the average power consumption and peak to peak power consumption of MGDI based TDC at 1V. Table II shows the power consumption comparison of static TDC and proposed MGDI based TDC with various supply voltage.

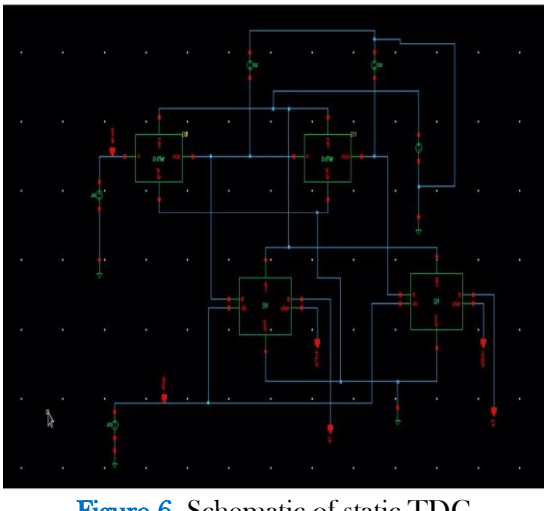

Figure 6. Schematic of static TDC

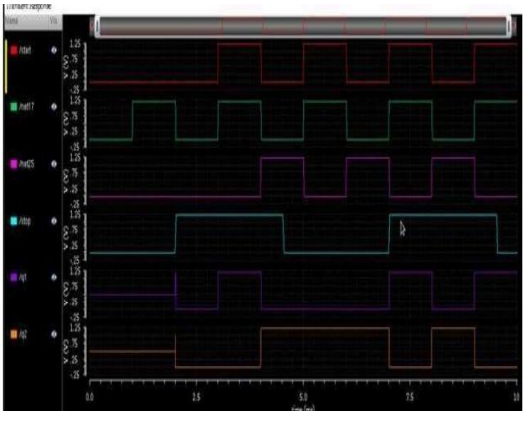

Figure 7. Static TDC output

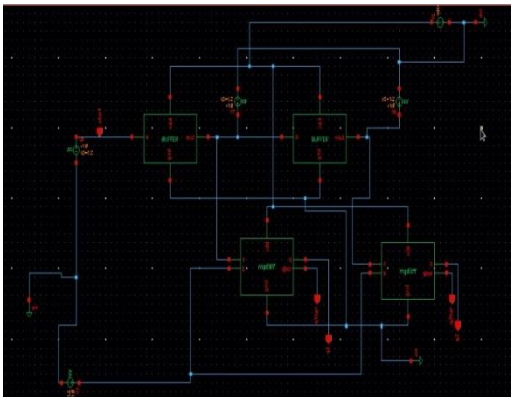

Figure 8. schematic of M-GDI TDC

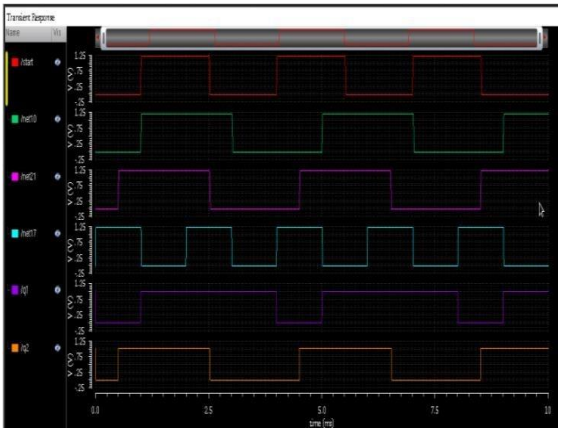

Figure 9. M-GDI based TDC OUTPUT

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Option
1	start		☑	☐	allv
2	net17		☑	☐	allv
3	net25		☑	☐	allv
4	stop		☑	☐	allv
5	q1		☑	☐	allv
6	q2		☑	☐	allv
7	power	688.228903121142m	☑	☐	
8	peak to peak	1.19998473215761	☑	☐	

Figure 10. Power output of static TDC at 1V

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	net23		☑	☐	allv
2	net12		☑	☐	allv
3	net16		☑	☐	allv
4	net13		☑	☐	allv
5	q1		☑	☐	allv
6	q2		☑	☐	allv
7	power	504.606m	☑	☐	
8	peak to peak	999.773m	☑	☐	

Figure 11. Power output of M-GDI based TDC at 1V Supply

Table 1. Power Consumption of Static TDC and M-GDI Based TDC at Various Supply Voltage

Supply Voltage	Static TDC	M-GDI Based TDC
0.4V	154.553m	83.467m
0.5V	203.618m	127.712m
0.6V	267.893m	182.812m
0.7V	306.917m	245.766m
0.8V	412.631m	320.134m
0.9V	562.768m	405.342m
1V	688.228m	504.606m

5. Conclusion

All the simulations are performed through cadence 90nm CMOS technology, and the results demonstrate a comparison of power consumption between the conventional static TDC and proposed MGDI based TDC. The simulation outcome shows much reduction in power to delay product in MGDI. By implementing the logic gates and digital circuits using MGDI technique, the number of transistors used are reduced up to 25%, area and the power consumption is reduced drastically compared with static TDC. This technique also increases the efficiency of the digital circuits and also in MGDI, the switching power and the leakage power is much lower when compared to the conventional TDC. The digital code of a new sample is determined by the difference between two consecutive samples, according to the designed structure. The decrease of power consumption in digital circuits is critical since it is preferable

to maximize run time while using low area and power. In comparison to a traditional TDC, the MGDI-based TDC features lower power consumption, a shorter latency, and a lower transistor count.

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Conflict of interest

The Authors have no conflicts of interest to declare that they are relevant to the content of this article.