ARC FURNACE AND SHUNT REACTIVE COMPENSATION MODELLING FOR VOLTAGE FLICKER REDUCTION

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

by

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SUMMARY

This thesis describes the modelling of a 56MVA electric arc furnace installation and its high voltage supply from 275kV. Models were constructed both in the laboratory, and mathematically using a mainframe digital computer. In both cases an investigation of the supply voltage distortion was carried out, with the disturbances that cause complaint from other consumers at the lowest distortion level being identified as the visible flickering of tungsten filament lamps. Model static shunt reactive compensators were applied to each system model, in order to reduce the voltage flicker annoyance levels caused by a given arc furnace demand.

Both arc furnace models utilised digital recordings of 33kV three-phase currents to reproduce measured supply voltage distortion.

The laboratory model system had a three-phase rating of 452VA, using an AIM-65 8-bit microcomputer and commercial power amplifiers to draw non-sinusoidal currents from a 175V supply.

The mathematical model used the same 1.8 sec data span of recorded current data to generate distorted supply voltage waveforms. The step-by-step solution of differential equations allowed a theoretical performance study of a six-pulse static shunt compensator.

Different thyristor-controlled reactor (TCR) schemes were applied to the laboratory arc furnace model, with fast phase angle control of conduction achieved with a voltage-integral algorithm using Intel 8088 16-bit microprocessor. The TCR control methods are fully described, with theoretical and experimental performance studies.

The results use power spectrum analysis and an internationally recognised flickermeter to show that the compensation methods reduced flicker levels, giving an improvement factor of 40 percent.

ACKNOWLEDGEMENTS

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GLOSSARY AND ABBREVIATIONS

α The phase angle between voltage peak and start of inductive current conduction. Units: Degrees.

ϑ The phase angle between voltage zero-crossing and start of inductive current conduction. Units: Degrees.

ε The phase angle between voltage zero-crossing and start of 'first-stage' inductive current conduction in the twelve-pulse TCR only. Units: Degrees.

δ The phase angle by which arc furnace busbar voltage lags 'infinite busbar' voltage. Units: Degrees.

σ A phase angle used for calculation of voltage depression. Equal to $(180^{\circ}-\vartheta)$. Units: Degrees.

ω Angular frequency, $2\pi f$. Units: Radians/sec.

ω_c Filter cut-off frequency. Units: Radians/sec.

Δ A three-phase circuit connection arrangement.

p.c. Percent.

p.f. Power factor.

p.u. Per unit.

@ Preceeds a hexadecimal number.

ACE Association of Chief Engineers (UK)

ADC Analogue to digital converter.

C Three-phase TCR compensator rating. Units: VA.

GLOSSARY AND ABBREVIATIONS (cont'd)

[C] A three-phase transformation matrix.

$[C_t]$ The transposed matrix of [C].

CEGB Central Electricity Generating Board (UK)

CIGRE Centre International des Grandes Reseaux Electriques

CIRED Conference International des Reseaux Electrique de Distribution

CVRY The time series values of computationally calculated $v_R - v_Y$.

D Sample loop delay. Units: Seconds.

DAC Digital to analogue converter.

DCVRY The time series of computationally demodulated values of calculated $v_R - v_Y$.

DFT Discrete Fourier transform.

DMVRY The time series of computationally demodulated values of recorded $v_R - v_Y$.

E A continuous integration sum. Units: Volt seconds.

EDF Electricite de France

E.PROM Erasable programmable read-only memory.

ERA Electrical Research Association (UK)

ESI Electricity Supply Industry (UK)

GLOSSARY AND ABBREVIATIONS (cont'd)

F	Arc furnace three-phase rating. Units: VA.
FFT	Fast Fourier transform.
F_N	Nyquist frequency. Units: Hertz.
F_S	Sampling frequency. Units: Hertz.
FSD	Full scale deflection.
IEE	The Institution of Electrical Engineers (UK)
IEEE	The Institute of Electrical and Electronic Engineers (USA)
IMP	Flicker improvement factor.
I_{RYB}	The vector representing the three-phase currents i_R, i_Y and i_B.
i_{TH}	Thyristor holding current. Units: Amperes.
i_{TL}	Thyristor latching current. Units: Amperes.
L_C	The inductance connected in each branch of a three-phase TCR. Units: Henries.
LIMIT	Discrete sample integration limit. Units: Volts.
M	Mutual inductance. Units: Henries.
MUSDU	Multi-user microprocessor system development unit.
MVRY	The time series recordings of $v_R - v_Y$ stored and used computationally.

GLOSSARY AND ABBREVIATIONS (cont'd)

N	Transformer voltage ratio.
N_q	Quantisation noise. Units: dB w.r.t. signal level.
PCC	Point of common coupling.
R	Resistance. Units: Ohms.
RAM	Random access memory.
S_c	Fault level. Units: VA.
S_t	Short circuit power. Units: VA.
SGT	Super-grid transformer (275/33kV).
TCR	Thyristor controlled reactor.
TNA	Transient network analyser.
UIE	Union International Electrothermic
VIA	Virtual interface adaptor.
V_{RMS}	RMS voltage. Units: Volts.
v	Instantaneous voltage.
v_f	Flicker voltage. Units: Volts.
V_{fg}	Guage point fluctuation voltage.
v_R	A constant sinusoid used for reference in an integration process.

GLOSSARY AND ABBREVIATIONS (cont'd)

V_t	Short circuit voltage depression. Units: Percent.
VDU	Visual display unit.
X	Reactance. Units: Ohms.
Z	Complex impedance R + jX. Units: Ohms.

CHAPTER ONE

INTRODUCTION

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1.1 THE ARC FURNACE LOAD

1.1.1 Electrical Supply to Arc Furnaces

Arc furnace installations have a well-established reputation as sources of harmonic and sub-harmonic disturbances of the supply system voltage[1,2,3]. Being rapidly fluctuating loads, their large electrical rating requires that they be connected at points on the supply system having a low source impedance. The allowable level of resulting voltage distortion is fixed by the electricity supply authority; customers proposing to install such plant face not only the capital cost of their own equipment, but also the costs incurred by the supply authority in strengthening or segregating the supply to that installation. These costs, for arc furnaces up to 40MVA, were debated as early as 1963 during the discussion period following an IEE symposium on transient, fluctuating and distorting loads[2,3,4,5]. At that time, the sum of £300,000 was agreed reasonable to achieve suitable segregation.

This economic factor has naturally made necessary a precise calculation of the level of segregation required, in conjunction with a detailed study to define acceptable levels of supply voltage distortion.

The UK Electricity Council issued guidelines in 1970 in the form of an Engineering Recommendation P7/2, 'Supply to Arc Furnaces'[6] that is now well known. The UK Association of Chief Engineers (of the supply industry) followed this document with their own detailed report[7], which explored the subject in greater depth.

1.1.2 Supply Voltage Distortion

The voltage distortion effect of the arc furnace load has been the subject of discussion and research for over twenty years[3]. This type of distortion causes annoyance by the visible flickering of tungsten filament lamps. This occurs even at low levels of voltage distortion, due to the fourth power relationship between voltage and light output.

In the UK, Dixon, Kendall and Thomas have published results of many studies[4,5,8,9] into the annoyance effects of such lamp flicker caused by different types of supply voltage distortion. In 1963 Kendall advocated the need for a flicker meter and its proper application, and further research into the nature of arc furnace voltage distortion followed[10,11,12,13], with work towards the development of a flicker meter being carried out both in the UK[14,15,16] and abroad[17,18]. Internationally, the 'Union International Electrothermie' (UIE) has co-ordinated the efforts towards flicker evaluation through its Disturbances Study Committee (DSC), and its flicker measuring methods working group published a valuable review of arc furnace disturbances[19] and found common agreement for a flicker measuring method[20], resulting in the internationally standardised flicker meter now used by the UK Electricity Supply Industry (ESI)[16].

1.2 SHUNT REACTIVE COMPENSATION

Shunt reactive compensation techniques are well established as a means of controlling power system voltages[21,22,23]. Mechanical switching of inductors and capacitors could only compensate for relatively slow reactive load variations, and a faster response was obtained by excitation control of synchronous rotating machines[24].

Rapidly fluctuating loads, particularly the arc furnace, demanded a speed of response even faster than could be obtained from the synchronous compensator, and in the early 1960s static compensator systems utilising saturated iron[25,26] were installed at arc furnace installations with some success[27,28,29,30].

1.2.1 Compensation for Arc Furnaces

The UK Electricity Council published a document 'Compensators for Arc Furnaces'[31], which with other review documents[19,32,33,34,35] identified thyristor-switched reactive devices as having potential for flicker compensation duties, with the general reservation that practical experience at that time was limited and their performance had then to be established.

A large amount of research and application of thyristor-controlled reactive compensators followed, with early success for transmission system voltage control. The literature contains many detailed reports of such work, and many of those up to 1982 are referenced in a bibliography of static VAR compensators, published by the IEEE[36].

1.2.2 Thyristor Controlled Reactors For Flicker Reduction

The control systems utilised to obtain the required compensator performance vary between manufacturers. The reactive compensator theory and control methods applicable to flicker reduction have been included in many publications[32,37,38,39,40,41,42], but evidence of the successful application of thyristor-controlled equipment for flicker reduction is not so widespread. Those schemes which show flicker improvement[43,44,45,46] use thyristor-controlled reactors as the variable VAR element, with fixed capacitors for filtering and power factor improvement. Measurement methods used to demonstrate their efficacy comprise both power spectrum analysis and different 'flickermeter' equipment.

The successful control methods are rarely presented in detail, for sound commercial reasons. However, a digital control system can be made flexible enough to allow its application to a variety of different control strategies. This digital approach, using minicomputers or microprocessors, offers the capability for greatest speed and accuracy of control.

1.3 DIGITAL COMPUTER CONTROL OF POWER EQUIPMENT

This research project makes extensive use of modern digital techniques for the control of laboratory power equipment. To show that such work may be of use in the environment for which it is eventually intended, a brief review of previous applications follows.

1.3.1 Applications of Digital Control

The many advantages of using computer control, for almost any scheme, are now well-known and widely accepted. Primary reasons for their wide application are:

(i) Arithmetic processing power and accuracy

(ii) Flexibility

(iii) Cost

(iv) Ease of monitoring and data logging

Initial applications to power equipment included simple sequence controllers and data loggers, and early problems of size, component reliability and electromagnetic interference and isolation have now been largely overcome. The last five years have seen the development of an extremely wide range of low cost robust programmable logic controllers for process control in an industrial environment, and dedicated systems are easily designed for high speed control of specific equipment such as power equipment protection and control[47,48,49,50] and HVDC Converter Control[51,52,53,54].

1.3.2 Digital Control of Thyristor Switches

Fibre-optic isolation techniques, effective electromagnetic screening and 'hardening' of sensitive equipment now allows digital controllers working at ground potential to control thyristor switch assemblies at voltages in excess of 33kV.

Thyristor technology has advanced rapidly, allowing simpler and more effective switch assemblies to be built. Recent advances include symmetric and asymmetric light-triggered thyristors, controlled turn-on, gate-assisted turn-off, and voltage break-over protection[55,56,57,58,59,60].

1.3.3 Microprocessor Control of a TCR Compensator

A microprocessor controller has not, to the author's knowledge, yet been applied to a full-scale TCR compensator scheme. A control system is presented in this thesis, and the available technology demonstrated in other engineering schemes may be suitably applied to this system.

1.4 MODELLING

Historically, modelling has been used by researchers to overcome difficulties in understanding caused by the size or complexity of the real system. Scale models, with all parameters under the control of the researcher, give savings in both the cost of equipment and the time required for the solution of a problem.

More recently, the advent of the digital computer has allowed researchers to extend mathematical modelling to include the most complex of systems.

These two types of modelling - physical and mathematical - have been represented in various studies into shunt static compensation techniques and the nature of voltage flicker.

1.4.1 Physical Modelling of Static Compensators

Cooper and Yacamini presented a review of modelling methods at the 1979 IEE seminar, 'Reactive Compensation in Power Systems'[51], and concluded that small scale physical modelling of thyristor controlled devices was a valuable study method, whilst warning of a reduced X/R ratio and the need for a wide frequency response.

Many papers show how Transient Network Analysers (TNAs) can be applied for physical modelling of static compensators and networks[62,63,64,65], but the TNA is not generally applied to an evaluation of static compensator performance for voltage flicker reduction. A difficulty appears to be the generation of a suitably distorted voltage waveform, accurately reproducing the frequency components causing flicker effect.

The results of other forms of static compensator physical modelling have recently been presented[66,67], and this thesis treats aspects of this work in greater depth.

1.4.2 Digital Modelling of Compensator Systems and Flicker

The advent of the digital computer allowed the study of network transient phenomena by the step-by-step solution of differential equations. Dommel[68,69,70,71] has published widely on this subject, and he demonstrates how various system components may be represented in the differential equations[68] of a general numerical model. The computational step-width is identified as an important factor in non-linear circuit solutions[69] and frequency dependence of components, especially lines, is accommodated using convolution between the frequency domain and the time domain[71]. The frequency dependence of parameters in digital models is further discussed by Budner[72] and Marti[73], while Feero, Juves and Long[74] give a study of the mathematical modelling of power system components.

Particular cases of computer modelling applied to static compensators are few[13,75,76]. Arc furnace load modelling has been attempted[76,77,78,79] and both of these subjects are explored further in this thesis.

Digital models studying voltage flicker[13,14,76,80] have used either voltage waveforms synthesised from low frequency sinusoids, or they have utilised recordings of arc furnace currents to aid the study of the flicker effect.

The basis for work in this thesis is that in order to model system voltage disturbances, the use of measurements of real arc furnace currents will offer the most realistic tests of performance for any model static compensator. This principle is applied for both a physical model in the laboratory and a mathematical model on a digital computer.

CHAPTER TWO

MODELLING OF AN ARC FURNACE

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2.1 REQUIREMENTS FOR A PHYSICAL MODEL

The aim of modelling an arc furnace and its electrical supply is simply to reproduce in the laboratory the type of voltage disturbances found in the full-scale case. If this can be done successfully, then any modifications made in the laboratory having an effect on the voltage fluctuations should have a full-scale parallel. In particular a means of reducing those voltage disturbances causing tungsten-filament lamp flicker by means of shunt compensation may be sought. Synthesized currents may have some value for investigating the annoyance factors of different combinations of disturbances at different frequencies, but for a practical study involving current compensation, it must be necessary to use load currents modelling actual currents as closely as possible, to make the results most relevant.

In its broadest terms, the Templeborough system to be modelled comprises:

(i) From the supply system:

An 'infinite busbar', or supply having a source impedance which is very low compared to the impedances of the components that it supplies. Thus the supply voltage is practically independent of the current drawn from it.

(ii) At the 'furnace busbar':

A load, drawing non-sinusoidal currents described by recordings made at this voltage. These are not the furnace line currents, but the currents drawn by the primary of the 33kV/500 V furnace transformer.

(iii) Between (i) and (ii) above:

A complex impedance representing the lumped parameters of components between the 'infinite busbar' and the load.

The infinite busbar can be modelled simply by using a suitable low-impedance, three phase supply. The load will require some device or devices that, when driven by a continuous signal derived from the recordings of the currents at 33kV, will faithfully reproduce the waveform at a suitable magnitude of current in each of the three phases.

The impedances present between supply and load can be modelled using components with values of complex impedance such that, for given base levels of current and voltage, their per unit impedance is as close as possible to that found in the full scale system.

2.2 THE SYSTEM TO BE MODELLED

In June of 1977 the System Technical Branch of the CEGB Headquarters organised a programme of measurements on an arc furnace supply at 33kV. The measurements were made at the Templeborough 275kV/33kV substation, which supplied six arc furnaces having a collective nameplate rating of 360MVA.

The aim of the exercise was to investigate the supply voltage 'flicker' fluctuations (see Chapter III) and harmonics produced by arc furnace operation. The three-phase current waveforms were recorded simultaneously with the voltage waveforms, and a record of relevant stages in the arc furnace melt cycles was kept. The varying electrical characteristics of single and multi-furnace operation could, therefore, be obtained.

2.2.1 The Templeborough Installation and its Supply

The six arc furnace transformers are supplied at 33kV from five 275/33kV supergrid transformers (SGTs) local to the steelworks. The SGTs are connected to the 275kV Sheffield ring between the Brinsworth and Pitsmoor switching stations (Figure 2.1).

The fault level on the Sheffield 275kV ring was 8500MVA, the system reactance being:

$$X_s = \frac{\text{Base VA}}{\text{Fault Level}}$$

$$= 1.18\text{p.c. on 100MVA base}$$

The fault level at the 33kV 'furnace busbar' is governed by the configuration of SGT transformers connected to it. Measurements (detailed further in 2.2.3 below) were taken on the left hand side of the split 33kV busbar shown in Figure 2.1. This enables a simplified supply diagram to be drawn (Figure 2.2) which also shows the impedances of each component.

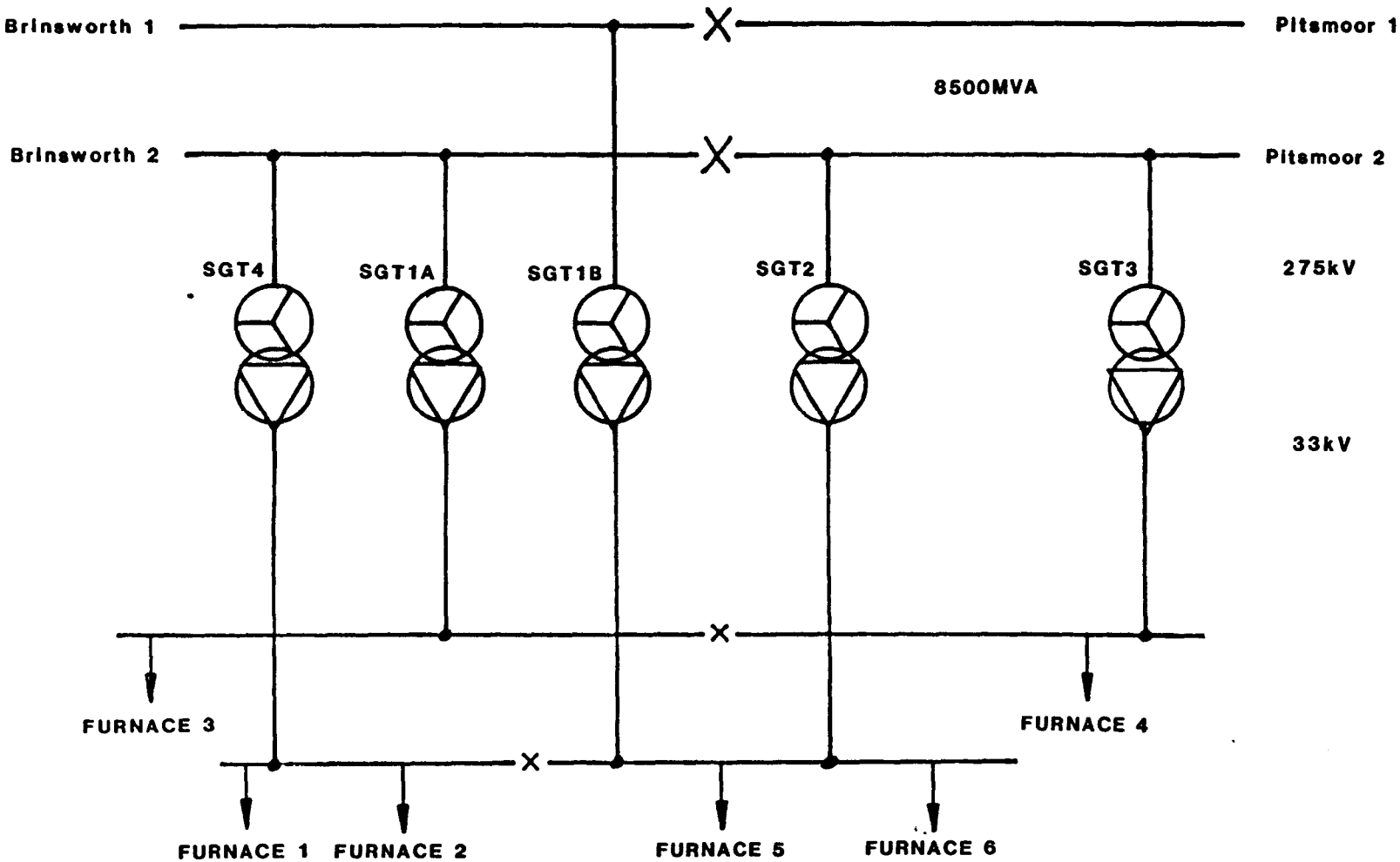


Fig. 2.1 : Templeborough arc furnace installation - supplies from 275kV

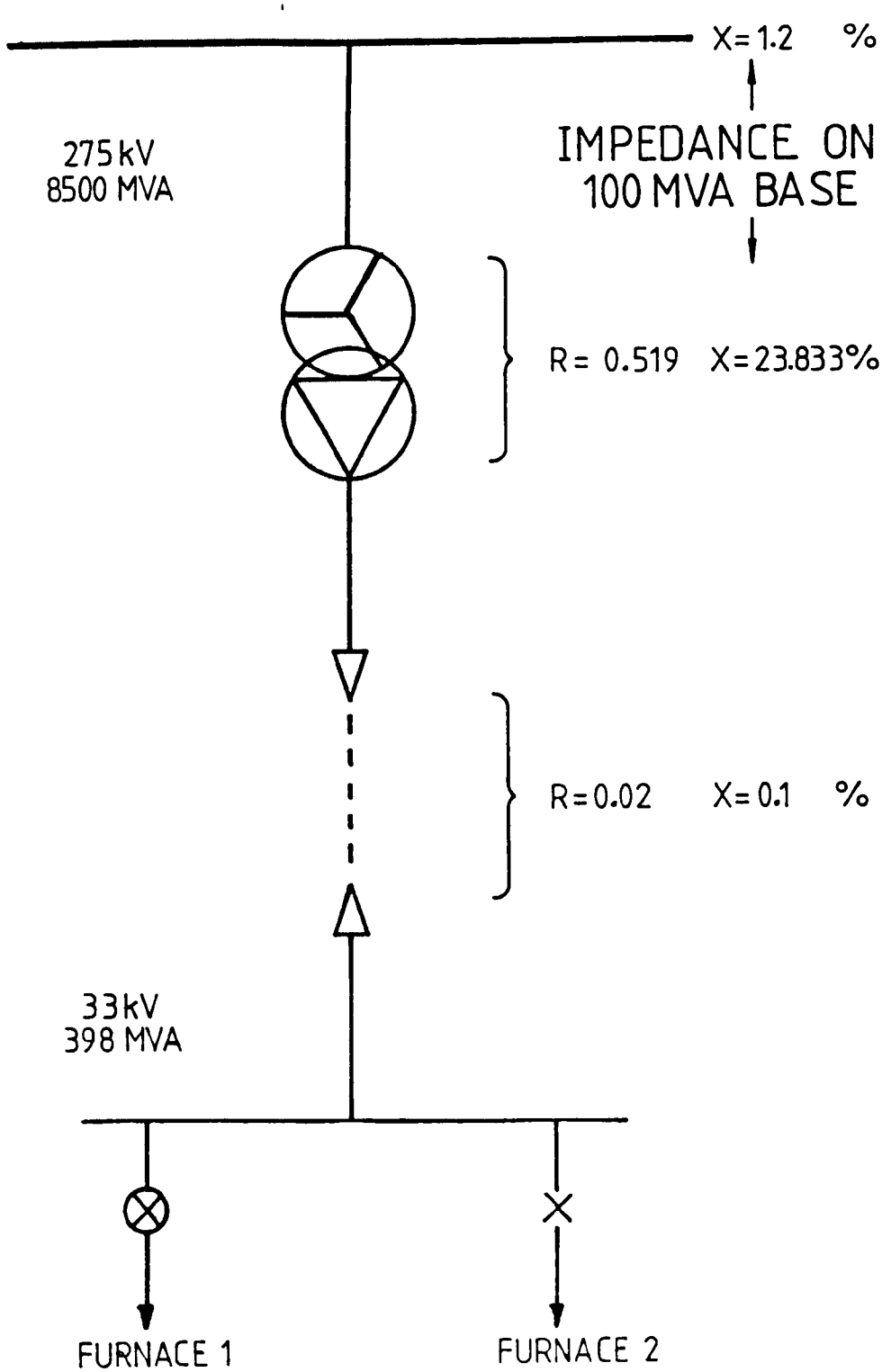


Fig. 2.2 : Simplified supply diagram for Templeborough furnaces 1 & 2

The total system impedance for the 33kV busbar is therefore:

$$Z_{tot} = (0 + j\ 1.2)\text{p.c.} \quad \text{275kV supply}$$
$$+ (0.519 + j\ 23.833)\text{p.c.} \quad \text{SGT 4}$$
$$+ (0.02 + j\ 0.1)\text{p.c.} \quad \text{33kV cable}$$

$$Z_{tot} = 0.539 + j\ 25.133\text{p.c. on 100MVA base}$$

The X/R ratio, or 'Q factor' for the supply circuit is then:

$$\underline{Q = 46.6}$$

The individual furnace 33kV/500 V Δ-Δ transformers are not considered here because there are no records for the currents and voltages in the secondary circuits.

Also not shown in Figures 2.1 and 2.2 is a Y-Y connected earthing transformer for the 33kV circuit. This transformer has a high impedance connected from the primary star-point to earth, to ensure that the otherwise isolated system does not depart from an earth reference. This transformer was judged to be unimportant in that its contribution towards the source impedance and its effects on current imbalances were negligible.

There were no connections to other consumers at 33kV, therefore the Point of Common Coupling (PCC) is at 275kV.

The short circuit level, S_c, of the furnace installation is shown in Appendix A to be 87.46MVA. The importance of this value relative to the fault level at the point of common coupling is discussed further in Part 3.3, with particular emphasis on the voltage flicker levels that are to be expected.

2.2.2 Measurements made at 33kV

Data acquisition at the Templeborough installation was by means of a digital recording and measuring (DREAM) system which has been widely used in power system studies[81,82].

The equipment and its possible operating modes are described in great detail in CEGB internal documents and need not be repeated here. However, the principal features of the mode used at Templeborough are:

(i) Simultaneous sampling of eight analogue signals every 800 microseconds.

(ii) Each sample has 15 data bits plus one sign bit. Quantisation noise is thus -90dB relative to the full scale signal.

(iii) Digital storage on magnetic tape in blocks of 2048 Bytes up to a maximum of 30 MBytes per tape.

Long-term studies may be made using repetitive short samples, but for this application a continuous stream of data was recorded, the length of which is limited only by the magnetic tape spool capacity.

Recordings of line current were made using current transformers (CTs) developing a voltage across resistors for conversion to a digital value.

Y-connected 33kV/110V voltage transformers (VTs) supplied the three phase voltages for ADC conversion. It could not be ascertained whether the star point of these VTs was connected to any neutral or earth reference. The continually changing imbalance of the system voltages and a floating star point may then have given rise to measurement of 'phase' voltages unrepresentative of the true system phase voltages.

To eliminate the possibility of studying misleading voltage measurements, the equivalent line voltages were calculated for every set of data samples. These derived line voltages were then independent of any neutral reference, and would give a true measurement of the three phase system voltages.

2.2.3 Selection of Data

Study of the reproduction of large amounts of Templeborough data by chart recorder at CEGB headquarters revealed a particularly interesting section. The record corresponded to one 56MVA furnace operating in isolation from others, and effectively supplied through its own supergrid transformer (SGT).

The data for this period was transferred to magnetic tape for use at Liverpool University. Appendix B describes in detail the operations required to recover analogue data from the digital magnetic tape recordings supplied to the University. The voltage and current recordings used for the studies are shown in Figures 2.3 (a),(b) and (c).

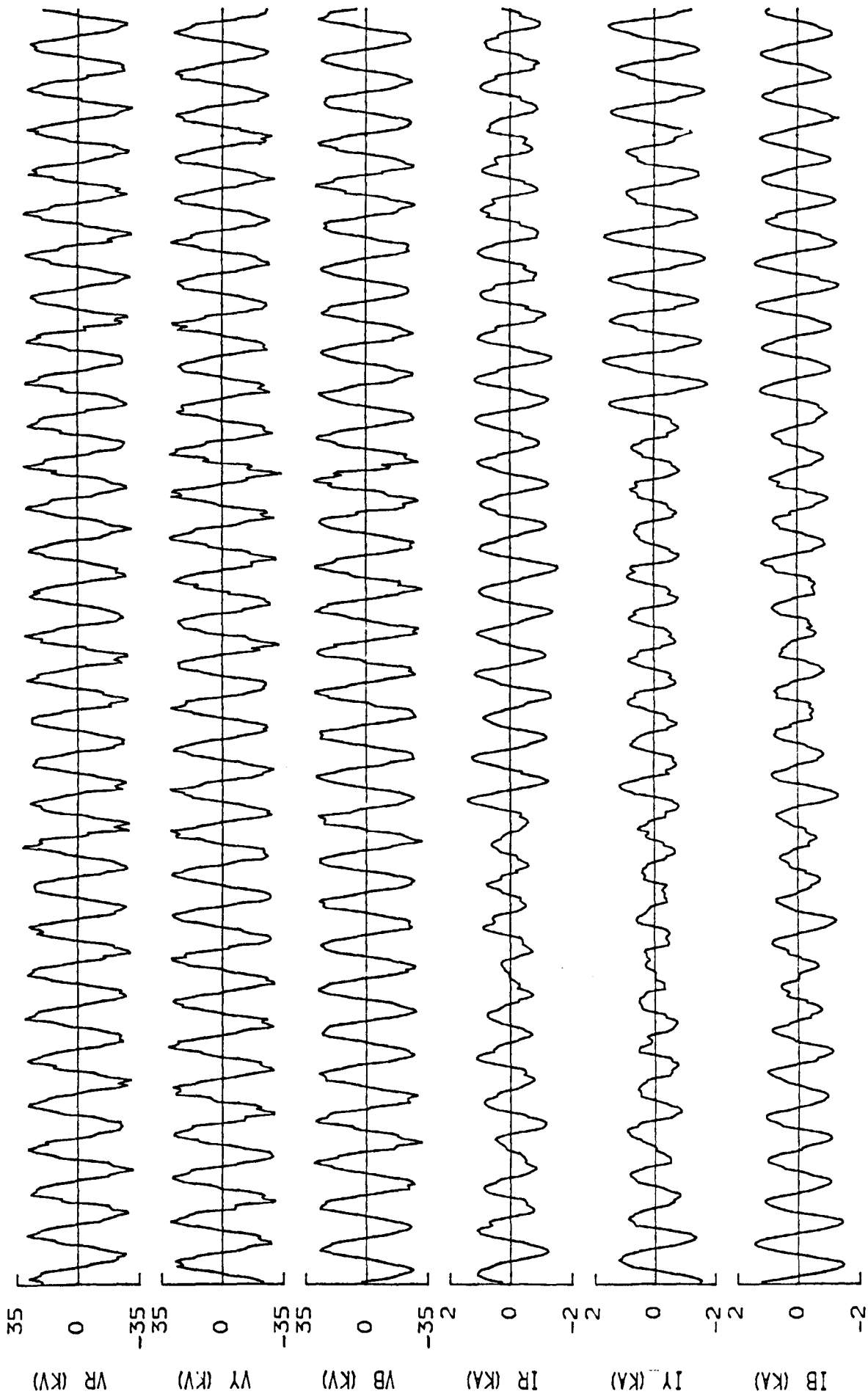


Fig. 2.3(a) : First 30 cycles of three phase voltages and currents used for modelling

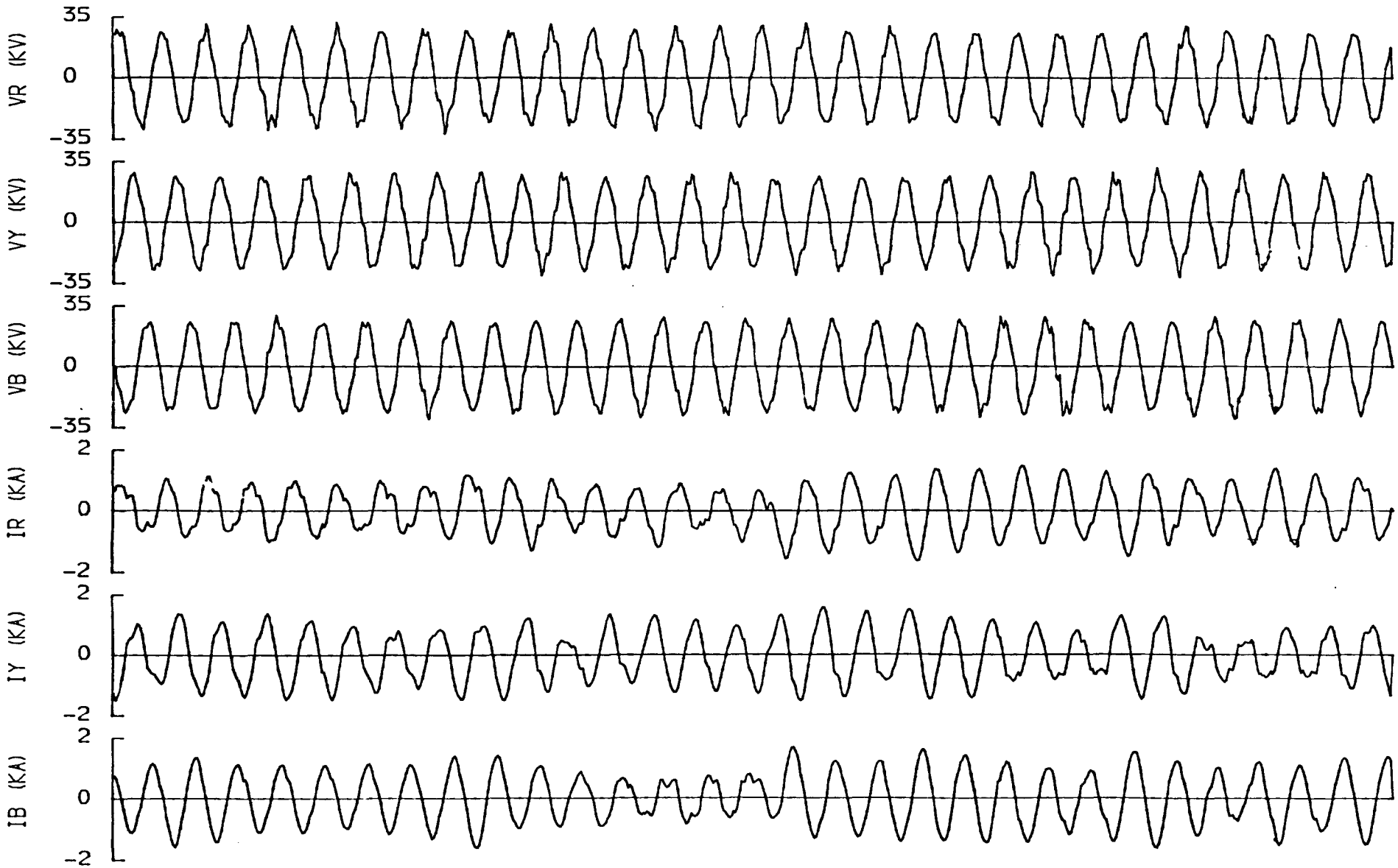


Fig. 2.3(b) : Second 30 cycles of three phase voltages and currents used for modelling

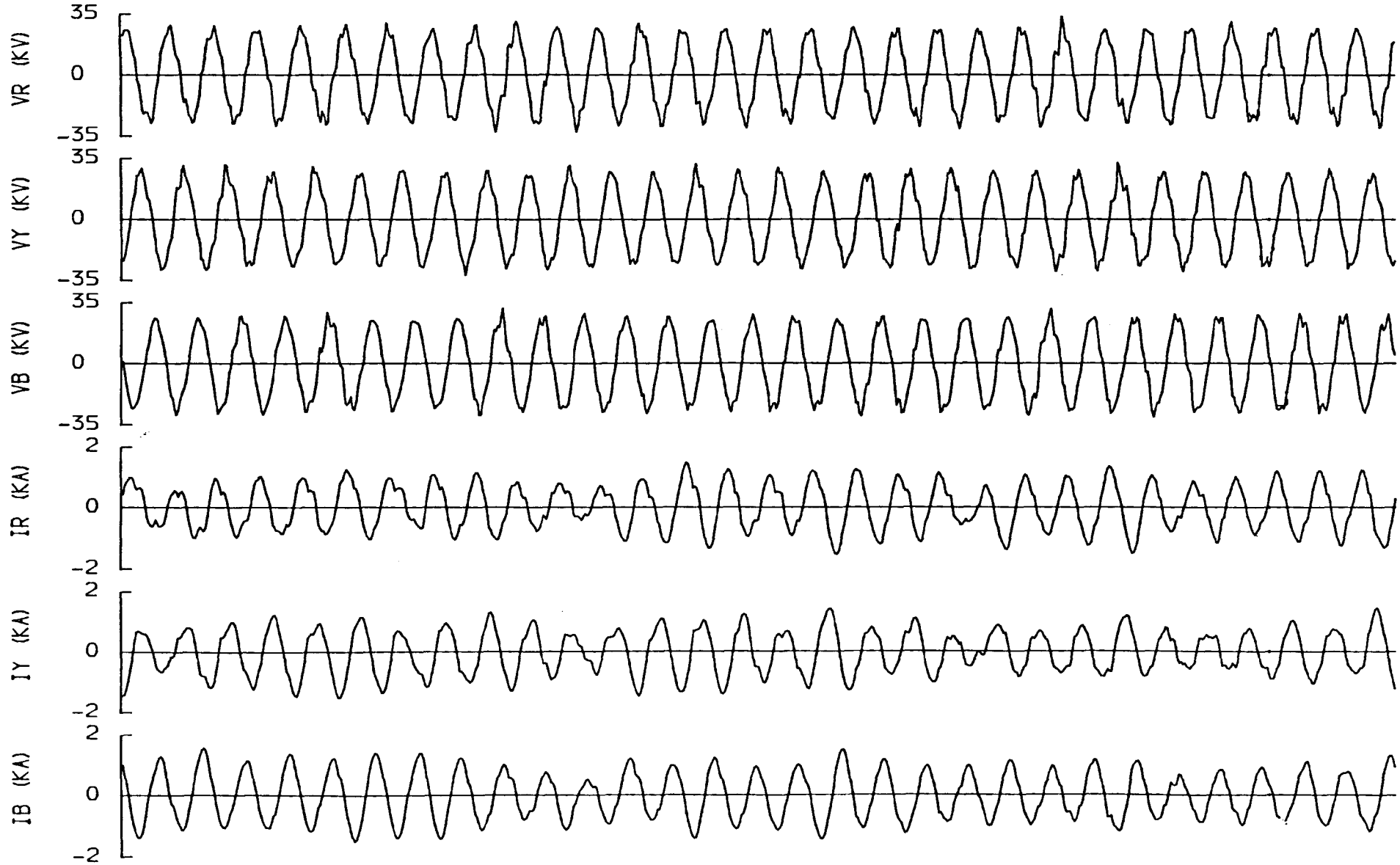


Fig. 2.3(c) : Final 30 cycles of three phase voltages and currents used for modelling

2.3 THE PHYSICAL MODEL OF ARC FURNACE AND SUPPLY

Section 2.1 above discusses, in broad terms, the requirements for a laboratory model. The methods used to fulfill those requirements will now be presented.

2.3.1 The Model's Supply

Modification of the laboratory 200 V three-phase supply to that shown in Figure 2.4 provided a source with a per-phase impedance of

$$Z_s = (0.0165 + j\ 0.0073)\ \text{Ohms}$$

This impedance, with an X/R ratio of 0.4, is not intended to model exactly the real 275kV Sheffield ring. The impedance is, however, of such a low value that it will be almost negligible compared to the impedances of the equipment it is to supply (2.3.3 below).

2.3.2 Line Current Reproduction

It was desired that a scale model of a particular arc furnace installation should be subjected to the same form of non-sinusoidal currents that the real installation suffered. This demanded a variable impedance capable of very fast response - in fact the frequency response had to be at least within the range 20-80Hz to allow the critical 0-30Hz modulations of the 50Hz carrier to be impressed upon the system, without distortion away from the driving signal. The driving signal would, of course, be derived from the recordings of the on-site current measurements at 33kV.

A feasibility study was undertaken, using a professional audio power amplifier as a 'current sink'. Using such a device for the variable load offered the advantages of easily controllable gain that would be practically uniform from 20Hz to 20kHz, and a short development time for the prototype system.

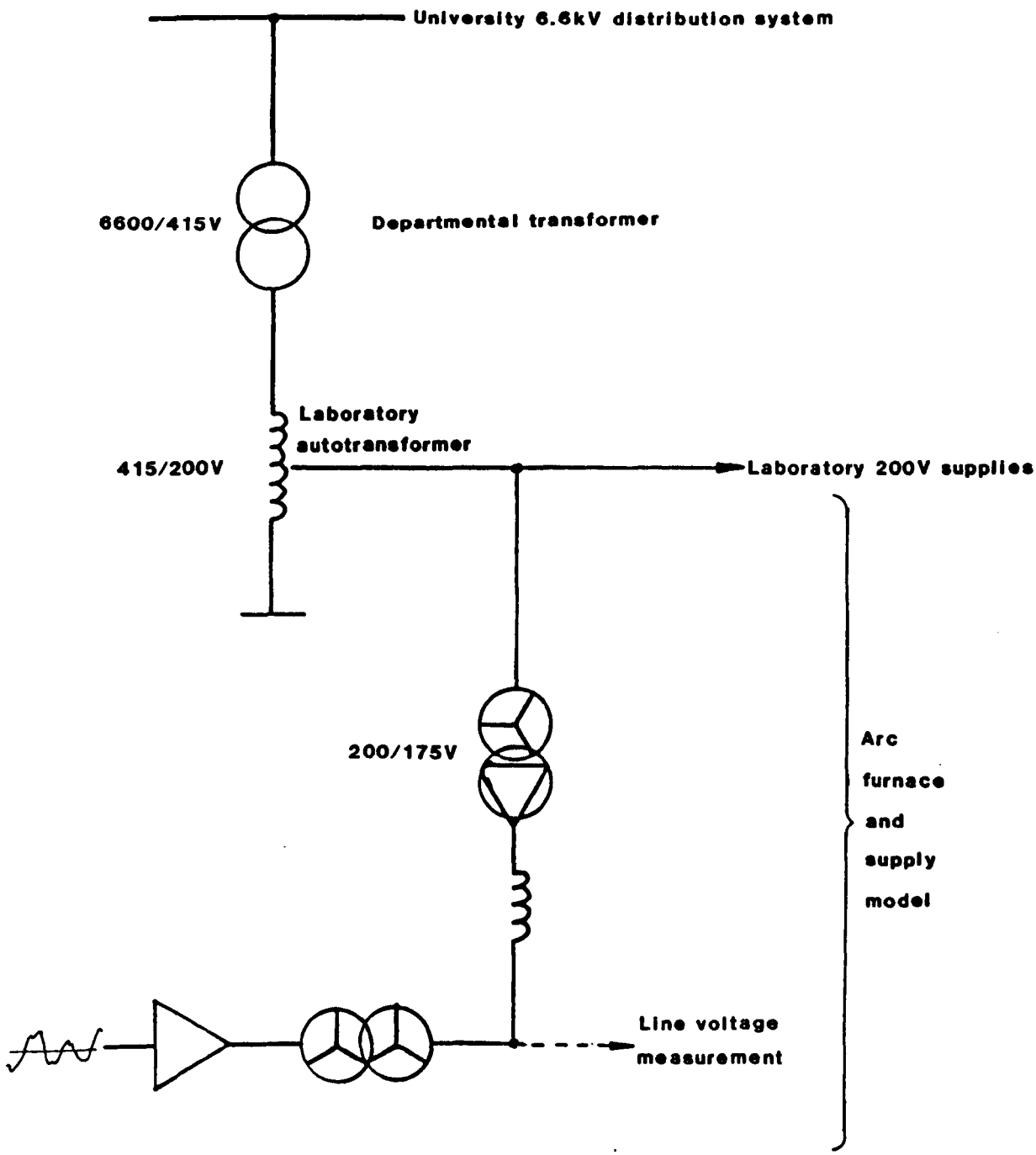


Fig. 2.4 : The laboratory supply from 6.6kV

An analogue input to the power amplifier was required, which would represent the line current waveform at 33kV. The necessary data was available on magnetic tape, and this was transferred via punched paper tape to a flexible microcomputer system dedicated to driving the power amplifier input. This method allowed many different sections of data to be applied to the variable load, including waveforms purely synthesized on the mainframe computer for test purposes.

The results of the feasiblity study were encouraging[66], and an extension to three-phase operation was undertaken.

The block diagrams illustrating the system used for the three-phase arc furnace model are given in Figure 2.5 (a),(b),(c).

A problem identified early in the project was the 800 microsecond sampling period used for the CEGB measurements and recordings. Although sufficiently small for data analysis, with a Nyquist frequency of 625Hz, the step lengths for current waveform reproduction were large. Figure 2.6 illustrates the step waveform produced with no smoothing.

Physical smoothing with low-pass filter networks could not achieve a suitable waveform. The data was therefore modified on the mainframe computer before punch tape output. Various interpolation and curve-fitting procedures were studied, and the method of least-squares cubic-spline approximation used to obtain three extra data points between each pair of recorded values. This reduced the time between data points from 800 microseconds to 200 microseconds. The computational principles and their practical application are further detailed in Appendix C.

The interpolation routines could easily be adjusted to produce any number of data points from the original samples. The obvious restriction, apart from punch tape length, was the capacity of the microcomputer memory.

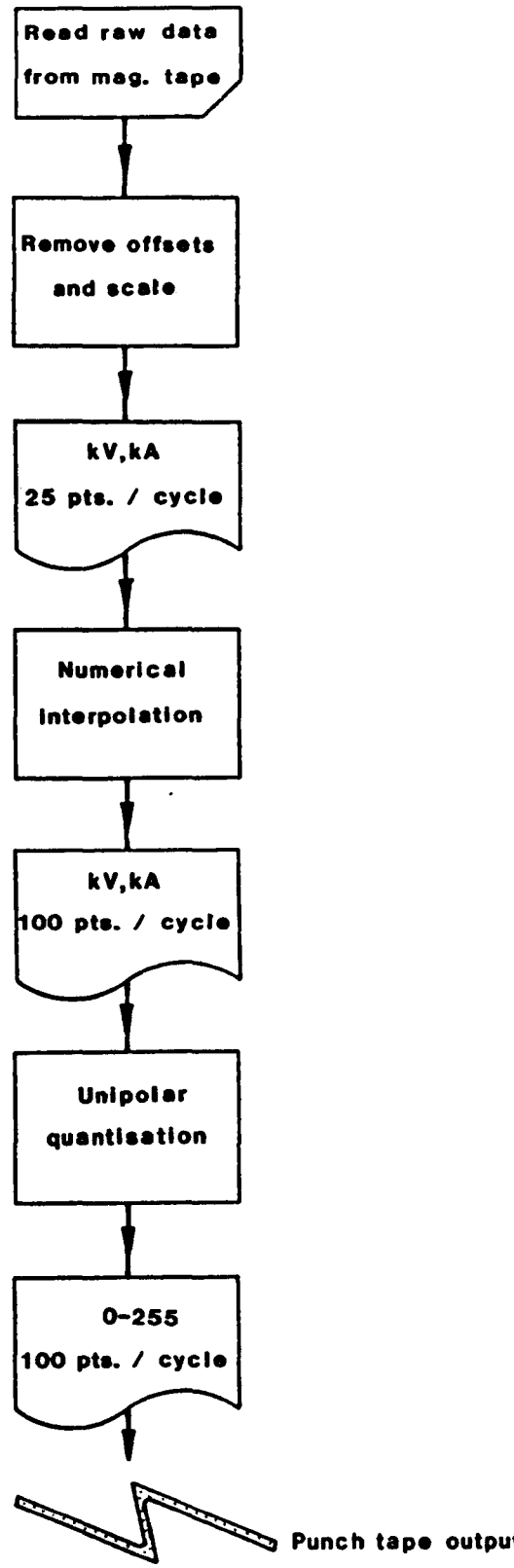


Fig 2.5(a) : Arc furnace model - mainframe computer data processing

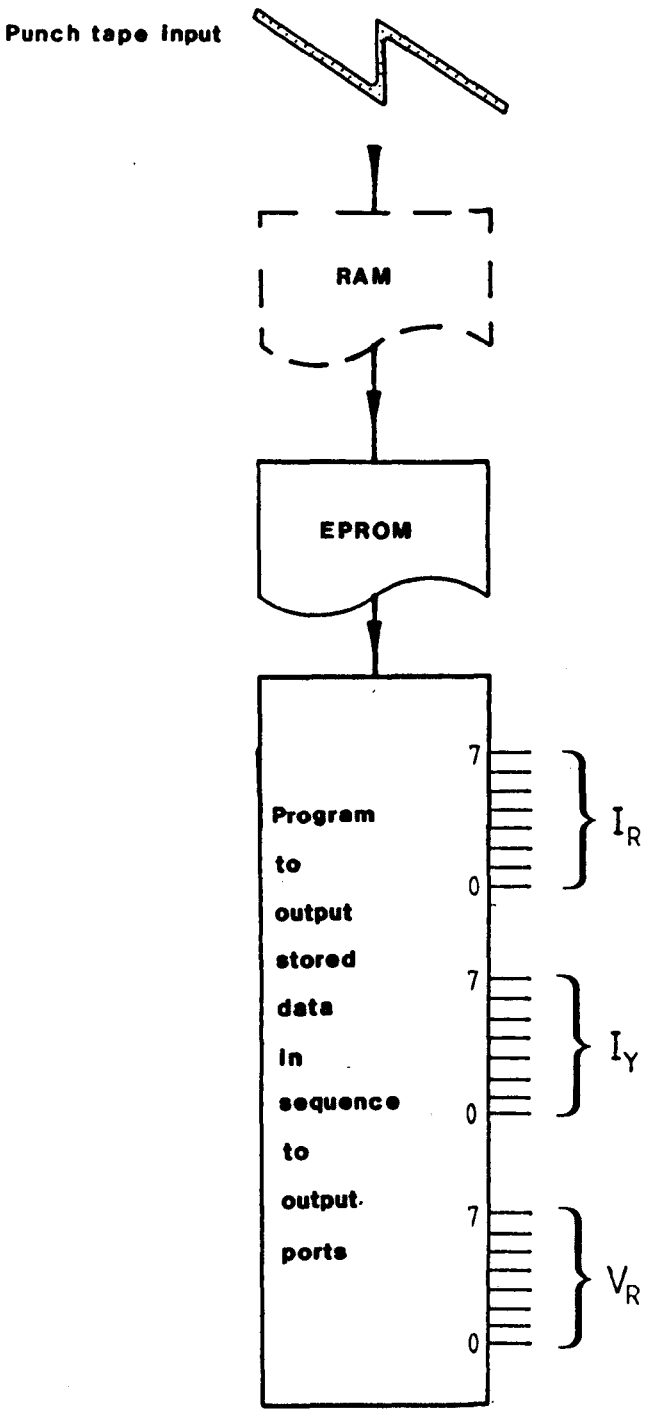


Fig. 2.5(b) : Arc furnace model - use of data by microcomputer

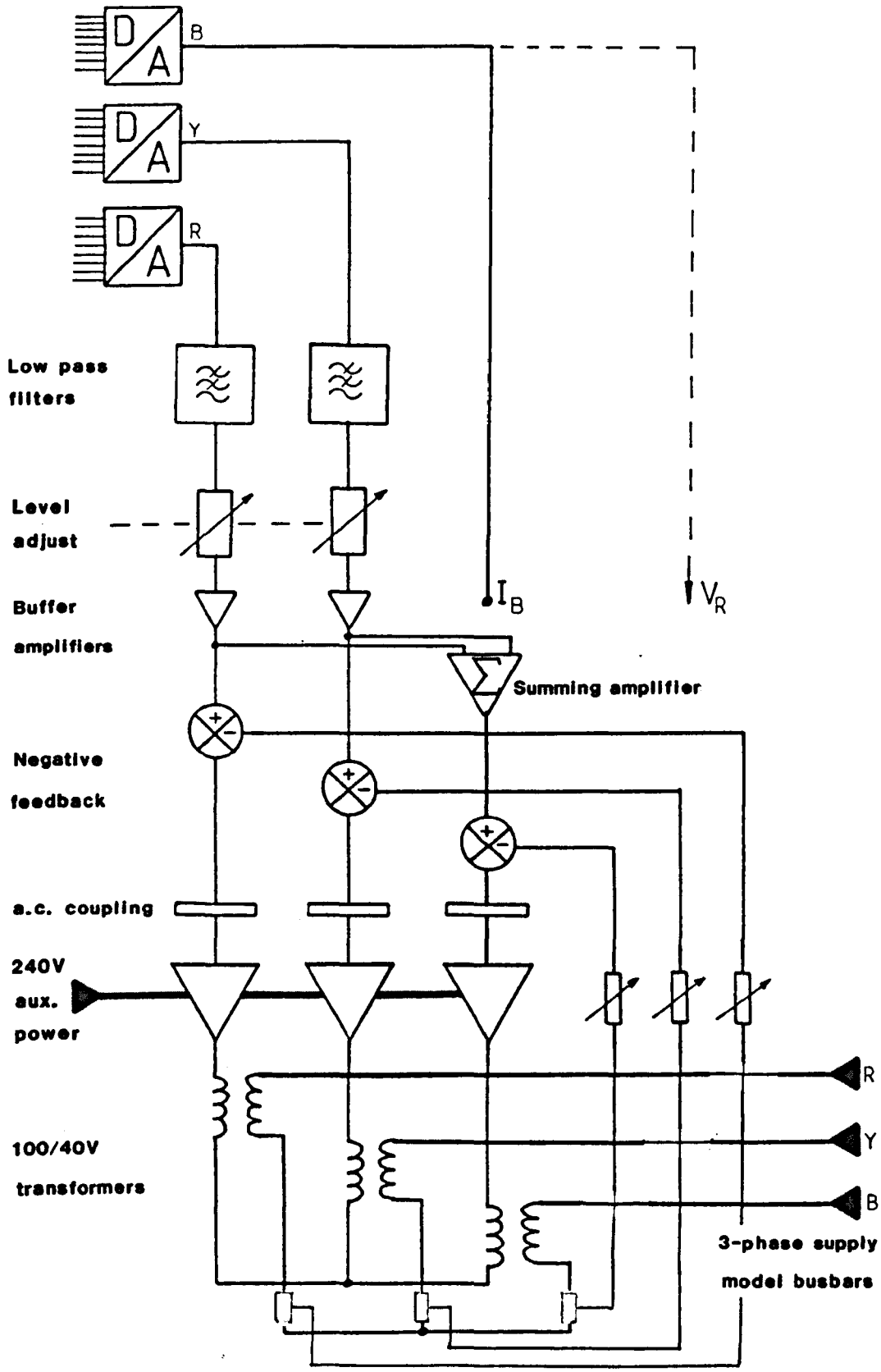


Fig. 2.5(c) : Arc furnace model - signal conditioning and current amplification

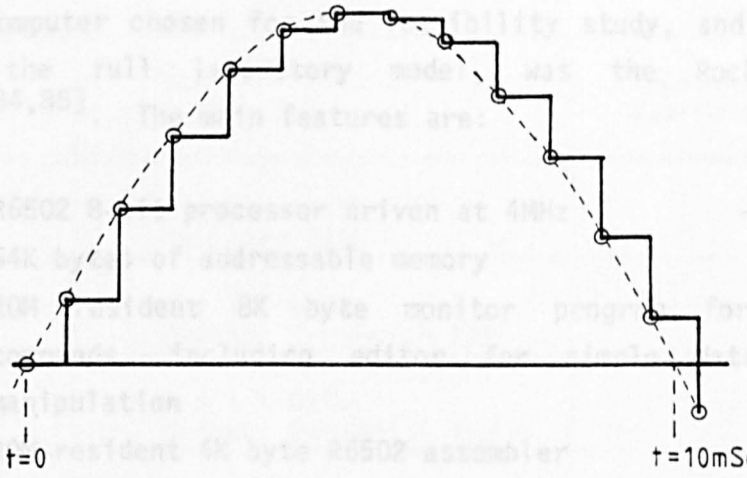


Fig. 2.6 : 800 microsecond quantisation of a 50 Hz waveform

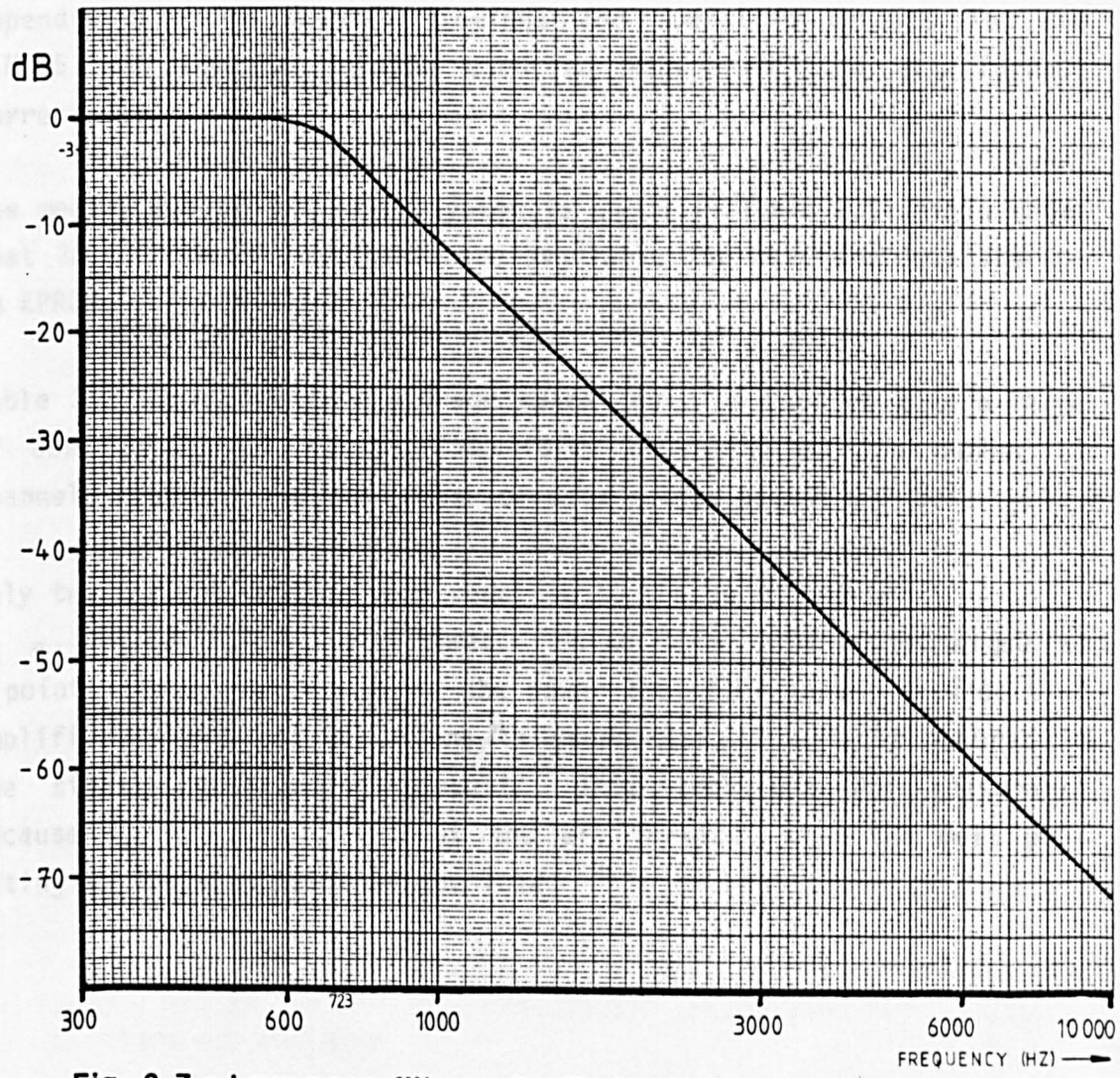


Fig. 2.7 : Low pass filter cut-off characteristics

The microcomputer chosen for the feasibility study, and subsequently used in the full laboratory model, was the Rockwell AIM-65 system[83,84,85]. The main features are:

(i) R6502 8-bit processor driven at 4MHz
(ii) 64K bytes of addressable memory
(iii) ROM resident 8K byte monitor program for single-key commands, including editor for simple data entry and manipulation
(iv) ROM-resident 4K byte R6502 assembler
(v) Single line display, thermal printer and full-size keyboard

A Dram Plus multi-purpose expansion board[86] provided 16K bytes of dynamic RAM and two R6522 Virtual Interface Adaptors (VIAs) each providing two independent 8 bit I/O ports.

Appendix D gives program listings and operating details for the AIM-65 microcomputer system used to regenerate the arc furnace current waveforms.

The memory map of the final system is shown in Table 2.1. This shows that 28,672 memory locations were available for waveform data storage in EPROM.

Table 2.2 shows how this storage space could be used to give a range of 50Hz cycles of recorded waveforms depending on the number of channels required and the number of data points output per 50Hz cycle.

Only two current outputs were required to the model, since $i_B = -(i_R + i_Y)$ at all times. Using this summing technique at a point in the system near to the power amplifier inputs ensured that amplifiers would not be acting in opposition if a fault occured in the signal conditioning circuit. This technique was reasonable because $i_R + i_Y + i_B = 0$ at the arc furnace, with the melt pool acting as the star point of the load.

Address	Use	Locations for Waveform Storage
0000 0FFF	4 x 1 K byte On-board RAM	-
1000 1FFF	4 x 1 K byte Dynamic Expansion RAM	-
2000 2FFF	4 x 1 K byte Dynamic Expansion RAM	-
3000 3FFF	4 x 1 K byte Dynamic Expansion RAM	-
4000 4FFF	4 x 1 K byte Dynamic Expansion RAM	-
5000 5FFF	2 x R6522 VIA	-
6000 6FFF	1 x 4 K byte EPROM	0 - 4,095
7000 7FFF	1 x 4 K EPROM	4,096 - 8,191
8000 8FFF	1 x 4 K EPROM	8,192 - 12,287
9000 9FFF	1 x 4 K EPROM	12,288 - 16,383
A000 AFFF	AIM-65 Printer, key-board, display, I/O etc	-
B000 BFFF	1 x 4 K byte EPROM	16,384 - 20,479
C000 CFFF	1 x 4 K byte EPROM	20,480 - 24,575
D000 DFFF	1 x 4 K byte EPROM	24,576 - 28,671
E000 EFFF	AIM-65 Monitor	-
F000 FFFF	AIM-65 Monitor	-

Table 2.1 Memory Map of the AIM-65 microcomputer system used for waveform reproduction

No. of Channels	Number of Data Points Per Cycle					
	25	50	75	100	125	150
2	573	286	191	143	114	95
3	382	191	127	95	76	63
4	286	143	95	71	57	47

Table 2.2 Showing maximum number of complete 50Hz cycles of recorded data that could be output using only 28 K bytes of EPROM for storage

Frequency wrt ω_c	0.1 ω_c	0.25 ω_c	0.5 ω_c	ω_c
Phase	-12°	-29°	-60°	-135°

Table 2.3 Phase response of a -60 dB/decade low-pass active filter ω_c = 723Hz

A third output channel from the microcomputer was allowed for in the memory considerations. This was used:

(i) To output the recorded i_B for comparison with the i_B derived as described above.

(ii) To output the recorded V_R for phase and form comparison with the model's V_R.

Spline interpolation was used for each channel, to give 100 points per cycle from the original 25 points per cycle. This was sufficient to give a smooth waveform after low pass filtering of the DAC output waveform. The low pass filter used had the passband characteristics shown in Figure 2.7.

This filter characteristic was found necessary in order to eliminate severe oscillations, which occurred in early models at the data output frequency of 5kHz. The filter circuit diagram is given in Figure 2.8. It comprises a -40dB/decade Butterworth cascaded with a -20dB/decade low pass active filter. The phase response of such a filter is important, and is given in Table 2.3. The 50Hz current fundamental is at $0.07\omega_c$, and the varying amplitude modulation components of the distorted 50Hz signal may be phase-shifted by many degrees. Close inspection of the signal waveforms before and after filtering showed that the effect of this phase delay was extremely slight.

The continuous output from the signal conditioning circuits was fed to the inputs of three commercial power amplifiers. The maximum rating of the 'arc furnace model' was determined by the rating of these power amplifiers. Figure 2.9 shows the limits of VI output available[87]. It can be seen that the maximum continuous a.c. power falls-off rapidly above 100 volts and 20 amps when current flow matches voltage polarity. The high inductive current component measured at 33kV presented the possibility of driving current in opposition to the voltage applied to the amplifiers, and the quadrants of Figure 2.9 show the de-rating necessary.

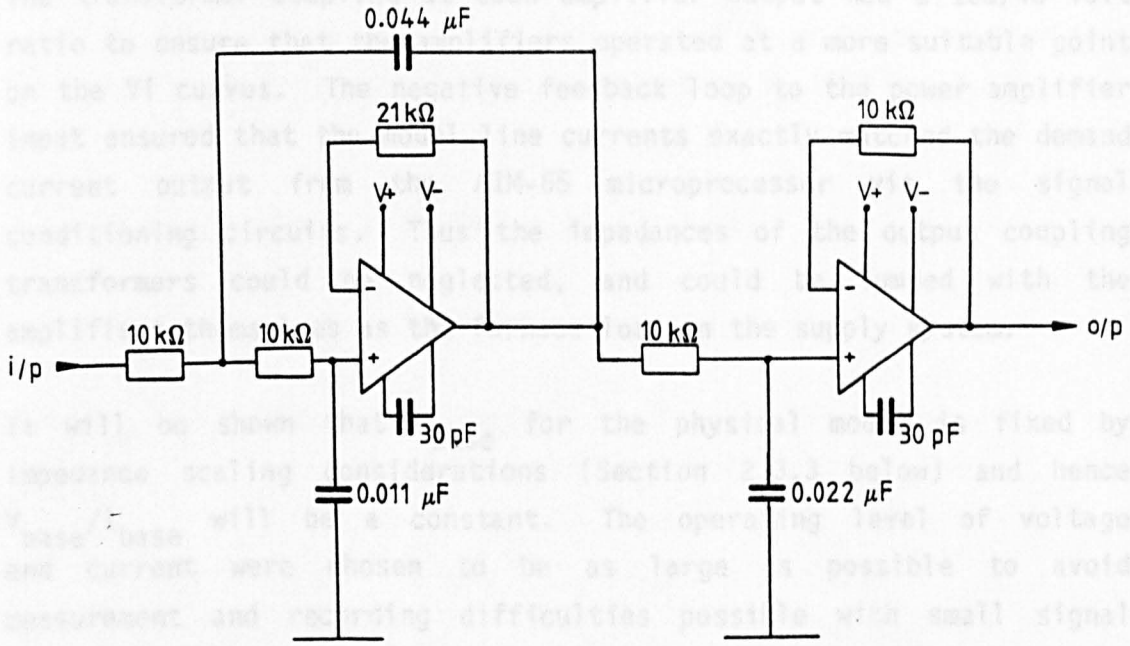


Fig. 2.8 : -60dB/decade low pass filter circuit diagram

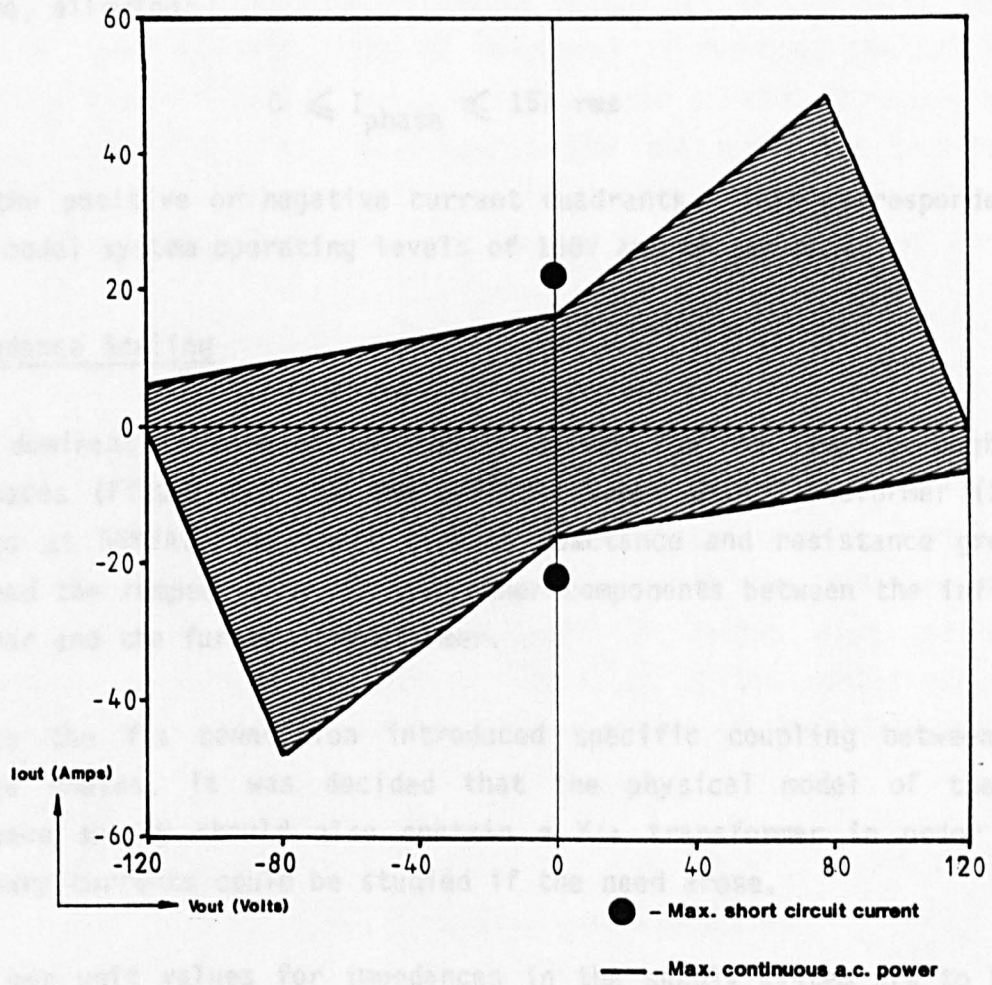


Fig. 2.9 : Power amplifier VI output curves

The transformer coupling at each amplifier output had a 100/40 Volt ratio to ensure that the amplifiers operated at a more suitable point on the VI curves. The negative feedback loop to the power amplifier input ensured that the model line currents exactly matched the demand current output from the AIM-65 microprocessor via the signal conditioning circuits. Thus the impedances of the output coupling transformers could be neglected, and could be lumped with the amplifiers themselves as the furnace load on the supply system.

It will be shown that Z_{base} for the physical model is fixed by impedance scaling considerations (Section 2.3.3 below) and hence V_{base}/I_{base} will be a constant. The operating level of voltage and current were chosen to be as large as possible to avoid measurement and recording difficulties possible with small signal levels and thyristor switching.

V_{phase}=40V rms lies well within the amplifiers continuous operation curve, allowing:

$$0 \leqslant I_{phase} \leqslant 15A \text{ rms}$$

in the positive or negative current quadrants. This corresponded to the model system operating levels of 100V and 6A per phase.

2.3.3 Impedance Scaling

The dominant feature of the supply system for the Templeborough arc furnaces (Figure 2.1) is the 275/33kV Super Grid Transformer (SGT), rated at 56MVA. Its short circuit reactance and resistance greatly exceed the lumped value for all other components between the infinite busbar and the furnace transformer.

Since the Y-Δ connection introduced specific coupling between the three phases, it was decided that the physical model of the arc furnace supply should also contain a Y-Δ transformer in order that primary currents could be studied if the need arose.

The per unit values for impedances in the supply system are to bases of 33kV and 100MVA, giving a base value of line current of 1.75kA.

Suitable model system operating levels were chosen as 100V and 3A per phase to ensure that the power amplifiers[87] would be well within their operating range. Setting base values of V_L=175V and I_L=3A gives

$$\text{3-phase VA base} = \sqrt{3}\,(V_L \text{ base})\,(I_L \text{ base})$$

$$= \underline{909.3\text{VA}}$$

$$\text{and } Z_{base} \text{ (per phase)} = \frac{(V_L \text{ base})^2}{\text{3-phase VA base}}$$

$$= \underline{33.67} \text{ Ohms}$$

These base values were used to specify equipment with impedances suitable to model the real system.

The ratio of resistance to reactance of the SGT is Q = 45.9. As the physical size of such items of equipment is reduced, the X/R ratio also reduces - a typical value for equipment of 1000 VA rating being approximately 10. The specifications for the model Y-Δ transformer emphasized a maximum value for short-circuit resistance which would approximately equal the per unit value of resistance found for the real SGT.

i.e. Rsc max = 0.00519 p.u. x 33.67 Ohms = $\underline{0.174}$ Ohms

Ideally X_{sc} would then be 8.02 Ohms (representing 0.2383 p.u.) but the much reduced X/R ratio for the model transformer will give X_{sc} considerably less than this. This difference between actual and desired reactance could then be overcome with the addition of an inductance with low series resistance in series with the model transformer. Fine adjustment of the value of the series reactance gave a suitable lumped parameter representation of the supply system.

For the 200/175V Y-Δ transformer:

$$R_{sc} = 0.124 \text{ Ohms per phase wrt 175V}$$

$$X_{sc} = 0.069 \text{ Ohms per phase wrt 175V at 50Hz}$$

For each additional line choke:

R_{series} = 0.80 Ohms

X_{series} = 9.36 Ohms at 50Hz

Thus the impedance of the line choke dominates, and the X/R ratio of the lumped parameters is 10.2. The magnetising current of the Y-Δ transformer was found to be 0.8 Amps and non-sinusoidal at rated voltage. It is therefore important that the series line chokes are not inserted between the Y-Δ transformer and the low impedance supply, since considerable distortion of the voltage waveform results. With the Y-Δ transformer primary connected directly to the low impedance supply, its magnetising current can be safely ignored.

Although the model's X/R ratio is a factor of four lower than that of the Templeborough system, the inductive reactance remains the dominant component. The ratio of lumped inductive reactances was used to determine the exact base value for line current as follows:

For the Templeborough System

Lumped impedance
to infinite busbar = SGT impedance + supply impedance

= (0.00519 + j0.2383) + (0.0 + j0.01) p.u.

= (0.00519 + j0.2483) p.u.

To bases of 100MVA, 33kV, 1.749kA

For the Analogue Model

Lumped impedance to secondary of 6.6kV transformer = Line choke impedance + Y-Δ transformer impedance + supply impedance

= (0.8 +j9.36) + (0.124 + j0.069)

+ (0.0165 + j0.0073) Ohms wrt 175V

= (0.9405 + j9.436) Ohms wrt 175V

Let j9.436 Ohms at 175V represent j0.2483 p.u. to bases of 100MVA and 33kV.

Therefore, Z_{base} for the model = $\frac{X \text{ Ohms}}{X \text{ p.u.}}$ = j38.0 Ohms

Then $VA_{base} = \frac{(V_L base)^2}{Z_{base}} = \frac{(175V)^2}{38.0} = 805.90VA$

And $I_{base} = \frac{VA_{base}}{\sqrt{3}\,(V_L base)} = \frac{805.90}{\sqrt{3}(175.0)} = 2.659$ Amps

This is only slightly less than the base current value of 3A initially chosen for the model.

The magnitude of the input signal to the amplifiers was adjusted until the first peak of the model yellow phase line current, I_Y, representing 1.1978 kA, was:

$$1.1978\text{kA} \times \frac{I_{baseMODEL}}{I_{baseSYSTEM}}$$

$$= 1.1978\text{kA} \times \frac{2.659\text{A}}{1.749\text{kA}}$$

$$= 1.81 \text{ Amps}$$

As shown in Figure 2.10.

The signal conditioning circuits and amplifier gains were each adjusted to give exactly balanced amplification for each phase under steady-state sinusoidal conditions.

A circle diagram is shown in Figure 2.11 for the laboratory 200V 3-phase supply at the receiving end. This diagram gives the lumped supply impedance for the model, and demonstrates how reactive power flow is due to the magnitude of the voltage difference along the line rather than the phase angle between sending and receiving end.

Figure 2.12 shows that currents drawn from the supply have frequency components in the range -20dB to -50dB, relative to the fundamental, in the band 1-100Hz. The power spectrum to 600Hz is shown in Figure 2.13, with peaks visible at 3rd, 5th, 7th, 9th and 11th harmonic frequencies.

Macedo[88] investigated the characteristics of supply impedances, highlighting the possibility of resonant nodes at frequencies up to 19th harmonic. Components of current at such nodes would produce disproportionate voltage fluctuations and would need to be recognised in any study. Calculations[89] for the real Templeborough system showed that such nodes existed at 6th and 17th harmonic (Figure 2.14), due to the combination of system capacitance and inductance.

Any disproportionate voltage fluctuations arising at these frequencies are, however, well outside the range of those necessary for lamp flicker analysis.

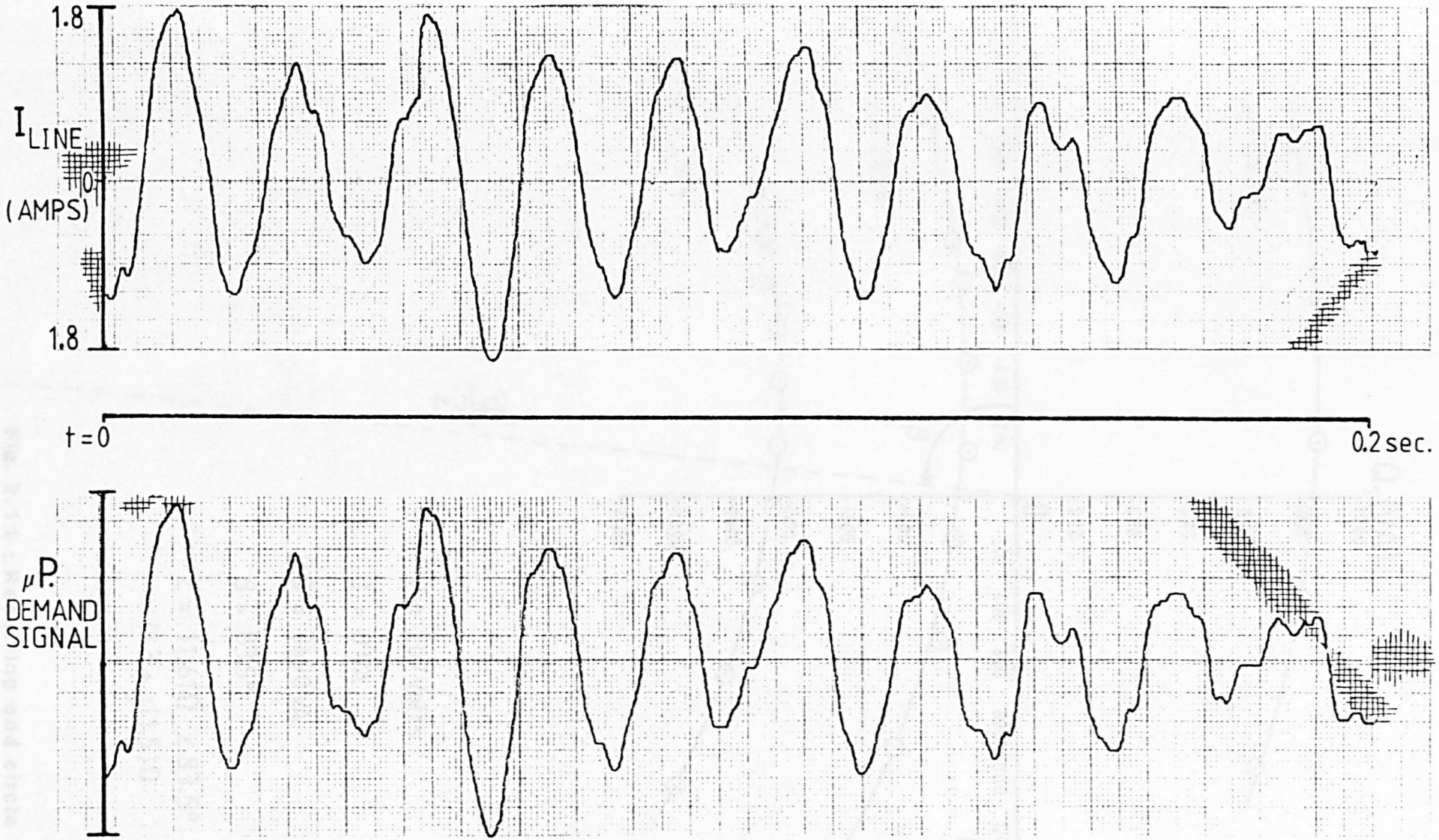


Fig. 2.10 : Comparison of demand signal and model line current

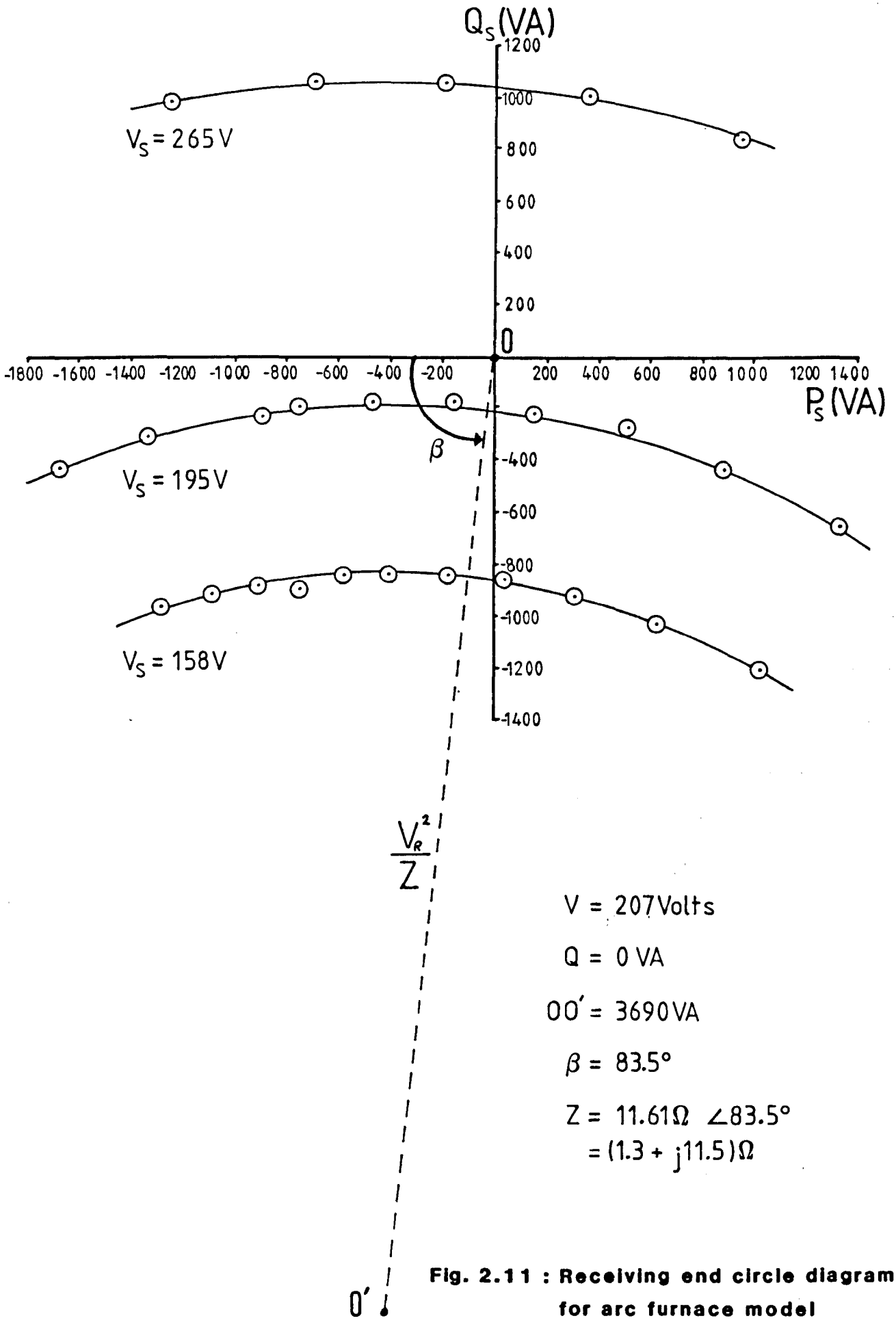


Fig. 2.11 : Receiving end circle diagram for arc furnace model

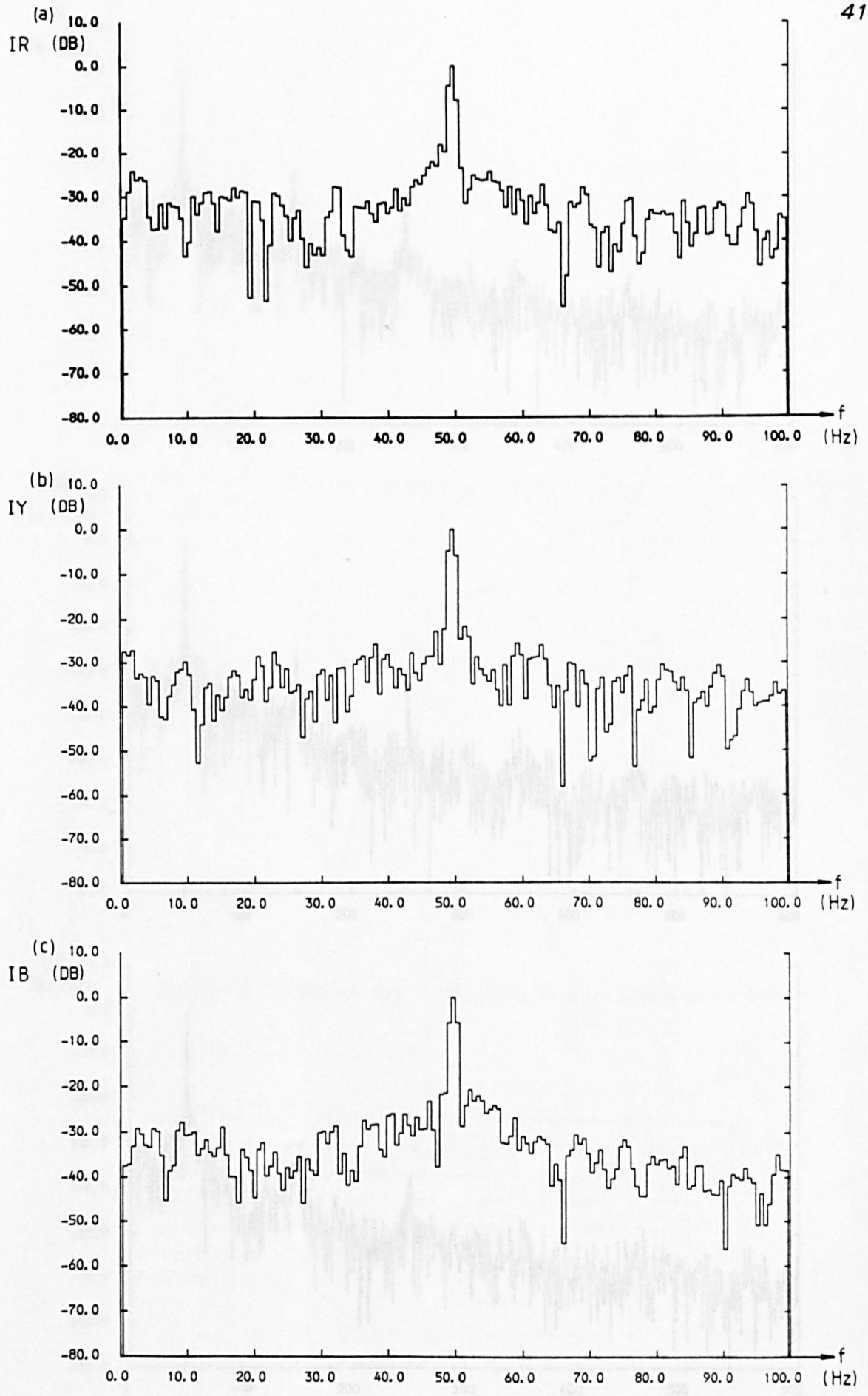


Fig. 2.12 : 0-100Hz power spectra of recorded arc furnace three phase currents

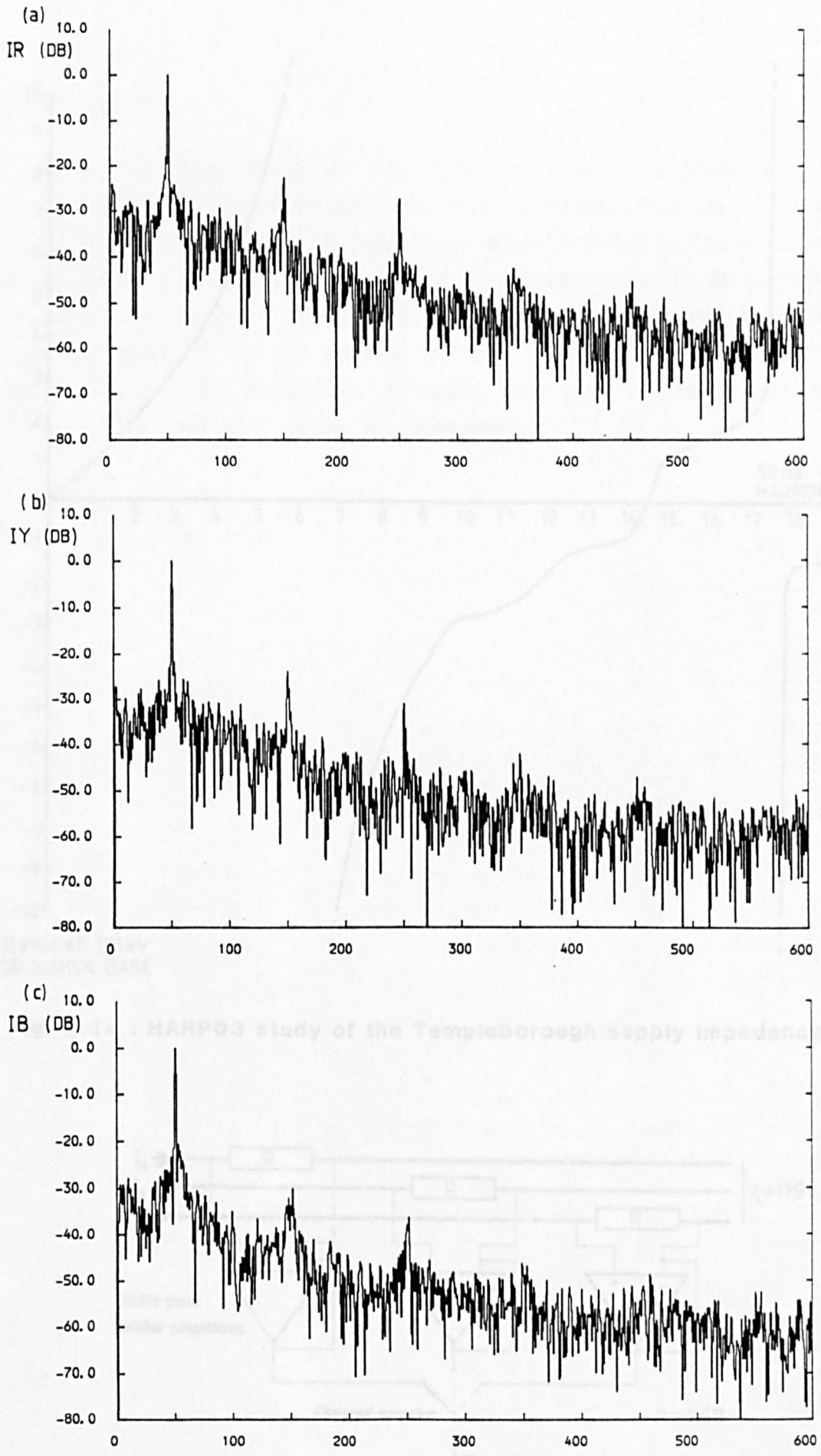


Fig. 2.13 : 0-600Hz power spectra of recorded arc furnace three phase currents

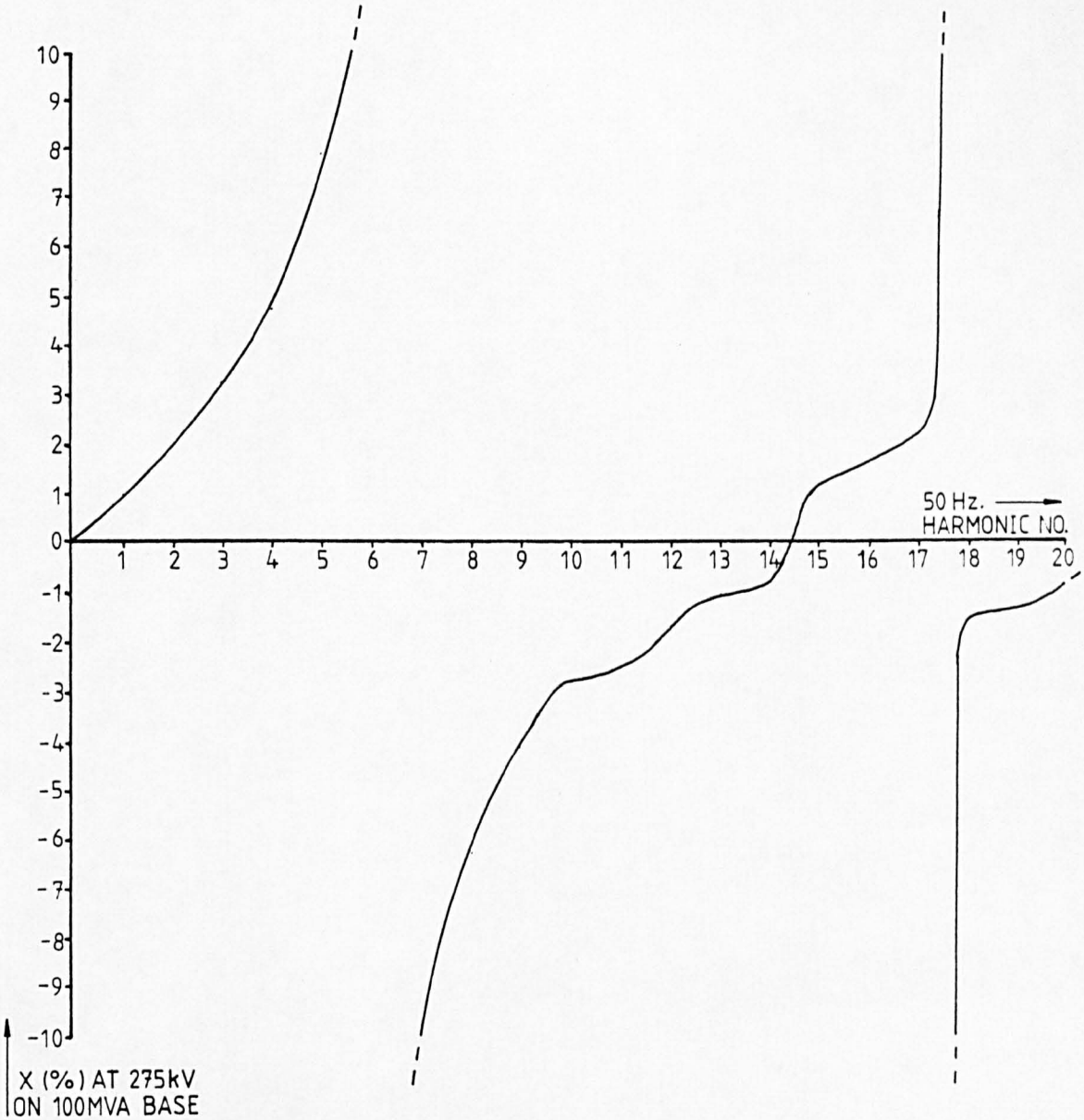


Fig. 2.14 : HARP03 study of the Templeborough supply impedance

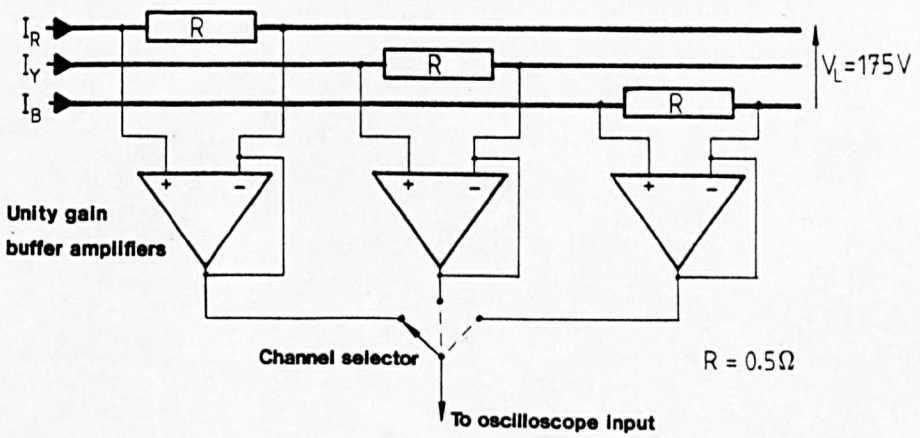


Fig. 2.15 : Method used for measurement of line current

2.3.4 Safety Sequence

The particular arrangement of the laboratory model allowed a safe sequence of events to be followed for its start-up. Appendix E gives a schematic of the complete laboratory model, and the 'safe-start' sequence. This sequence avoided the application of large voltage transients or current surges to the equipment, thus allowing protective devices to be graded to the relatively low operating levels. A safety contactor allowed complete disconnection of supplies in the event of danger to personnel.

2.4 RESULTS

Measurement of the characteristics of non-sinusoidal waveforms may be attempted in a number of ways. Modern oscilloscopes have now replaced high speed chart recorders for most applications, and digital measurement techniques enable large amounts of data to be stored and retrieved easily.

The study of the success of the laboratory model in reproducing arc furnace supply characteristics was undertaken in three stages.

(i) The accuracy with which the line currents produced by the power amplifiers compared with those line currents measured at 33kV at the Templeborough installation

(ii) The voltage fluctuations at 175V that the model line currents produced, again compared to those measured at 33kV

(iii) The frequency components of the currents and voltages described above.

Section 2.3.2 describes how the same stream of data is continually cycled through to drive the model's power amplifiers. This meant that the model was operating in a continuous mode, and different measurements could be taken sequentially using the same recording equipment. For (i) and (ii) above, where the measured quantities were studied as a function of time, it was essential that some common time reference be available for comparison between non-concurrent recordings. This was achieved using a short triggering pulse output from the microcomputer driving the power amplifiers. The pulse was output only at the beginning of each complete cycle of the 1.78 second data stream. Further details of this synchronising pulse output may be found in Appendix D.

2.4.1 Line Current Waveforms

Laboratory recordings of the model waveforms were made using a 0.5 Ohm resistive shunt in each line of the model. The voltage thus developed was fed directly to the AC coupled input of a Gould digital storage oscilloscope. The full specification of this instrument is given in Reference [90].

Figure 2.15 details the recording method. A Bryants 25000 flat bed X-Y plotter was used to present the results in a suitable A4 format.

Figure 2.16 shows the first five 50Hz cycles of the red, yellow and blue line current waveforms with the data points output from the microcomputer memory presented adjacent to the measurement of line current for direct comparison.

The fine stepped effect on both waveforms is a characteristic of the digital storage oscilloscope and plotter, and should not be confused with the output of quantised data at 5kHz from the microcomputer. The low pass filter described in Section 2.3.2 attenuates this 5kHz component, and possible phase errors due to this filter are not apparent in the results.

The magnitude of the line currents was determined by the setting of the 'level adjust' potentiometers (Appendices D and E). In practice the first peak of the yellow line current waveform was always carefully set to equal 1.8 Amps.

Then = 1.8A x 0.5 Ohms = 0.9 Volts to oscilloscope

2.4.2 Voltage Waveforms

The laboratory model was normally made to cycle over 89 complete 50Hz cycles of digitally stored data, this being the limit of that which could be stored in the microcomputer memory.

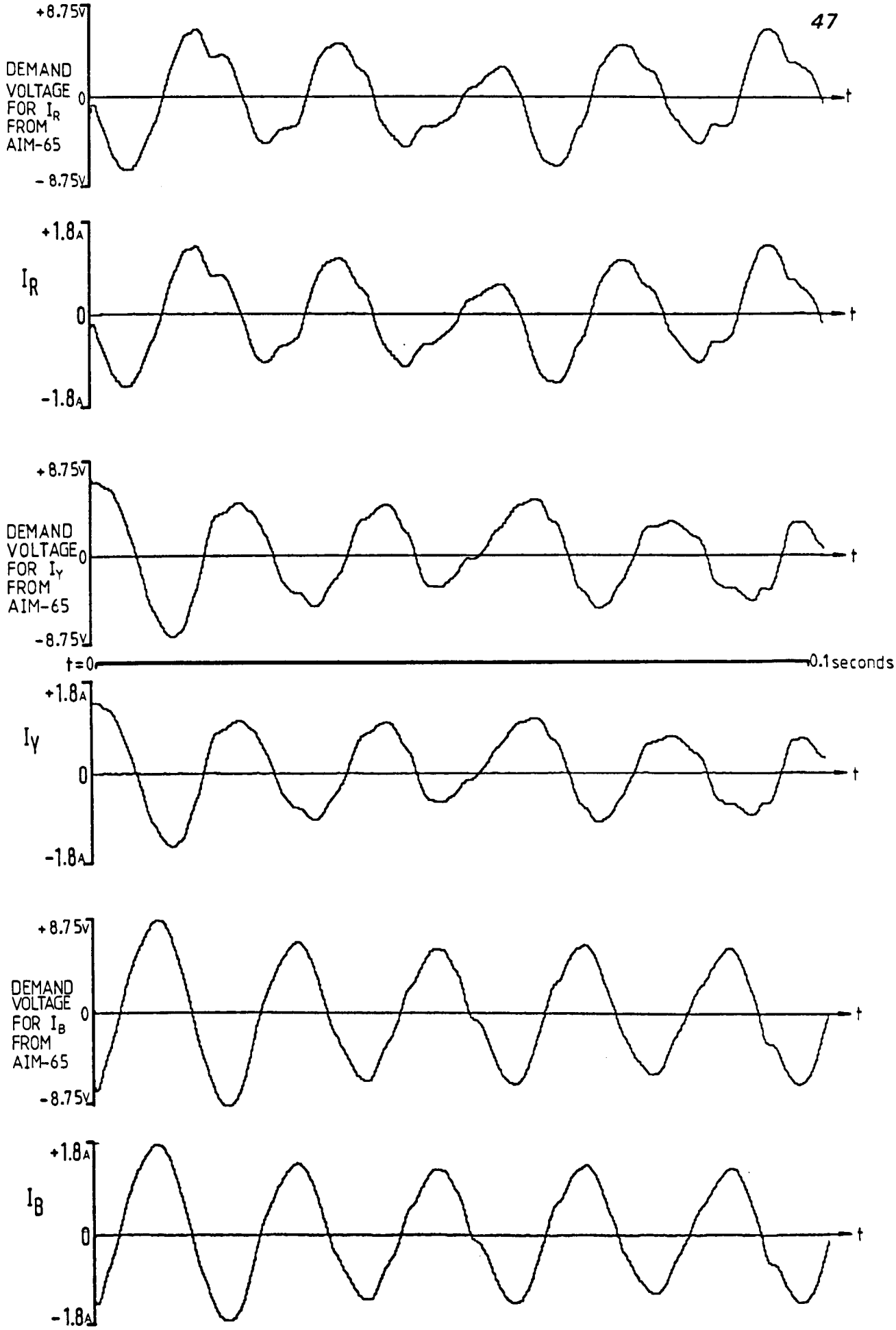


Fig. 2.16 : First 5 cycles of arc furnace model line current

Presentation of results in the time domain in a suitable format suffers in that:

(i) To show all 89 cycles loses much useful detail.

(ii) Showing only one or two cycles may be criticised for being unpresentative.

Figures 2.17(a),(b) show the line voltage V_B-V_R with the model current off and at rated magnitude respectively. There is little value in presenting the open circuit voltage in the fashion of Figure 2.17(a) again, now that it has been shown to be a steady sinusoid. Figure 2.18 repeats Figure 2.17(b), with the open circuit voltage level now only indicated by a straight line. The low frequency fluctuations imposed on V_{BR} are clearly evident from the varying level of the voltage peaks.

Figures 2.19 and 2.20 show the corresponding variations for V_R-V_Y and V_Y-V_B respectively.

The form of Figure 2.17 is repeated for the first 2.5 cycles only in Figure 2.21. This shows clearly the voltage fluctuations due to the arc furnace model within each cycle for V_R-V_Y.

Figures 2.22 and 2.23 give the corresponding variations for V_Y-V_B and V_B-V_R respectively.

Figure 2.24 shows the phase relationship between line voltage and current in the laboratory model for each of the three phases.

2.4.3 Power Spectra of Voltage Waveforms

The voltage waveforms presented in Section 2.4.2 clearly show distortion from a sinusoidal form. A precise evaluation of the distortion is difficult when the 50Hz fundamental is present, and the 'flicker voltage', V_f, may be obtained if this fundamental frequency is removed.

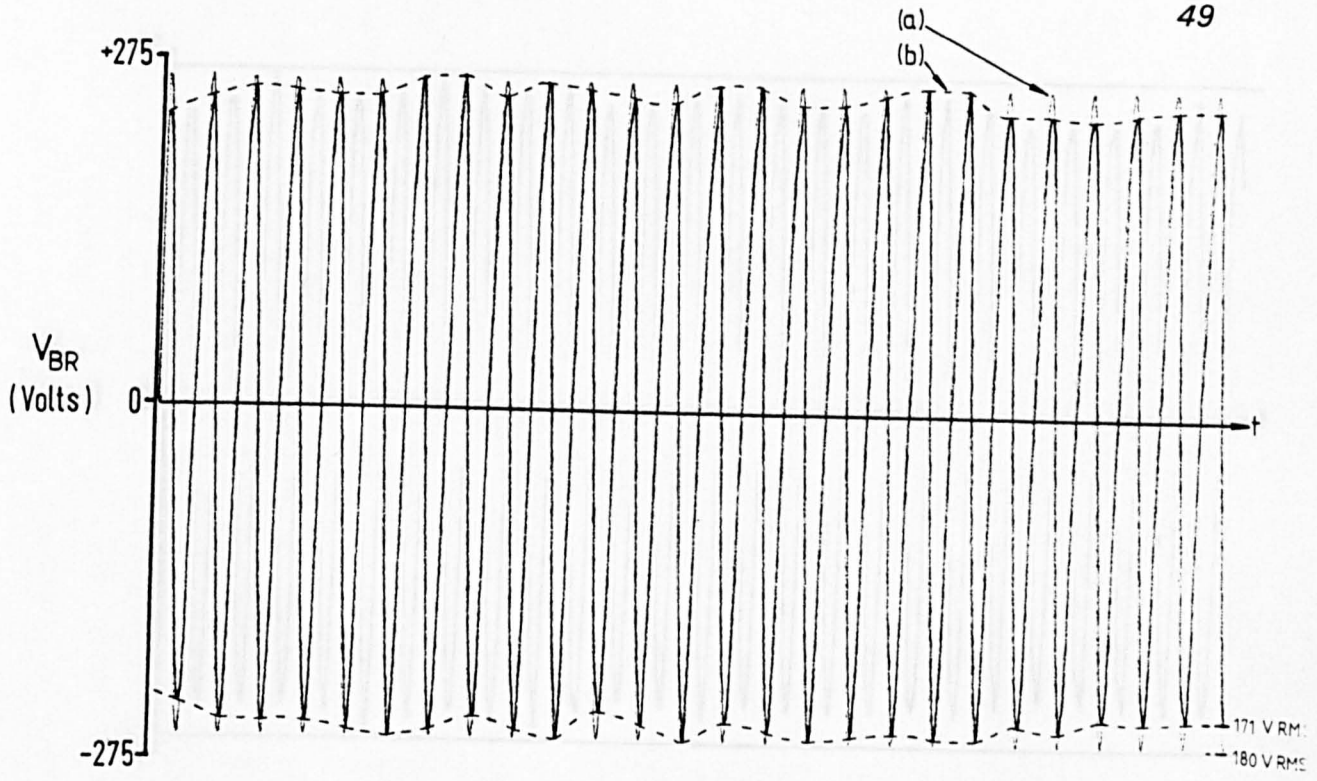


Fig. 2.17(a) : Arc furnace model open circuit line voltage Vbr
(b) : Vbr with arc furnace model operating

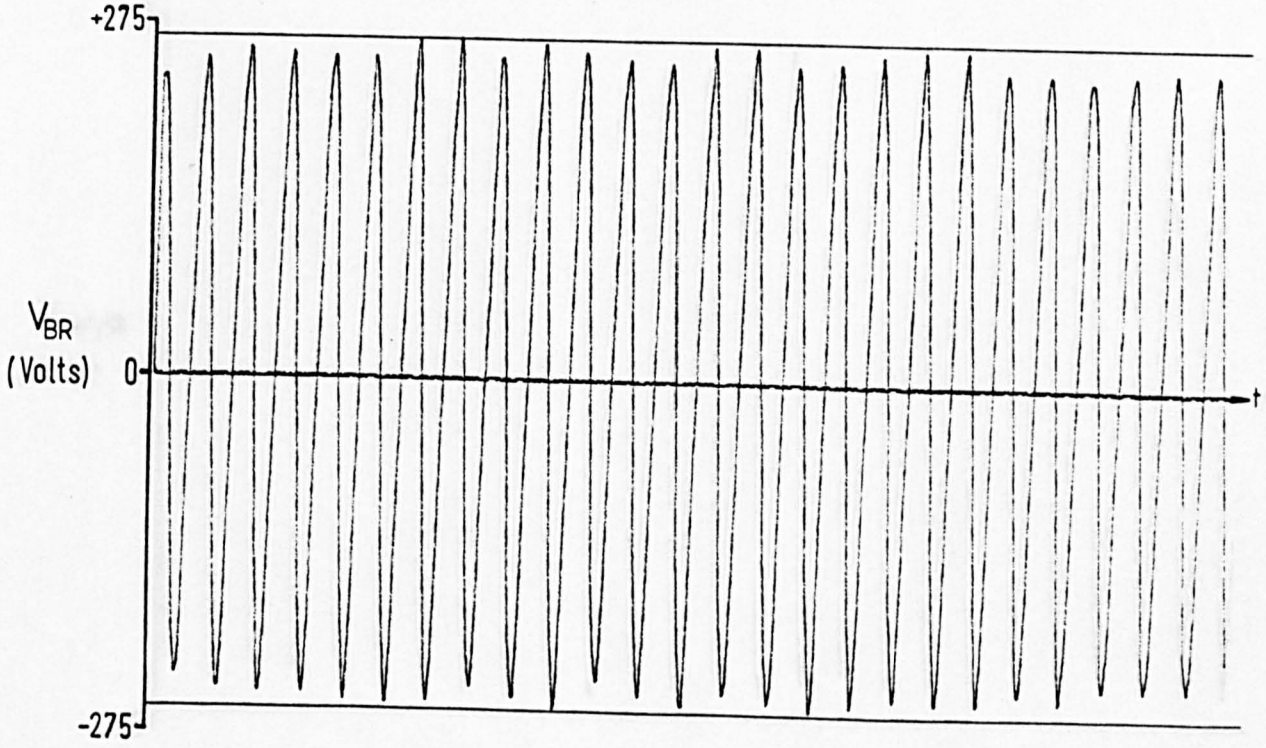


Fig. 2.18 : Vbr with arc furnace model operating

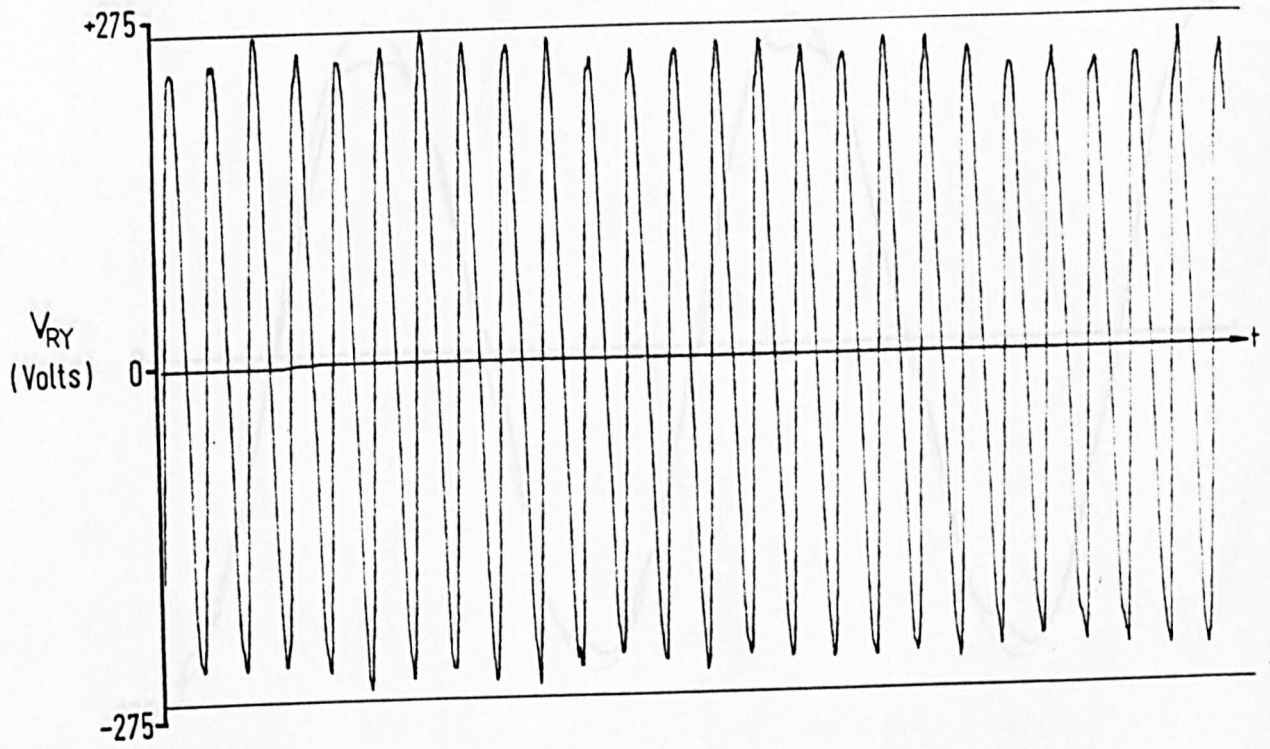


Fig. 2.19 : V_{ry} with arc furnace model operating

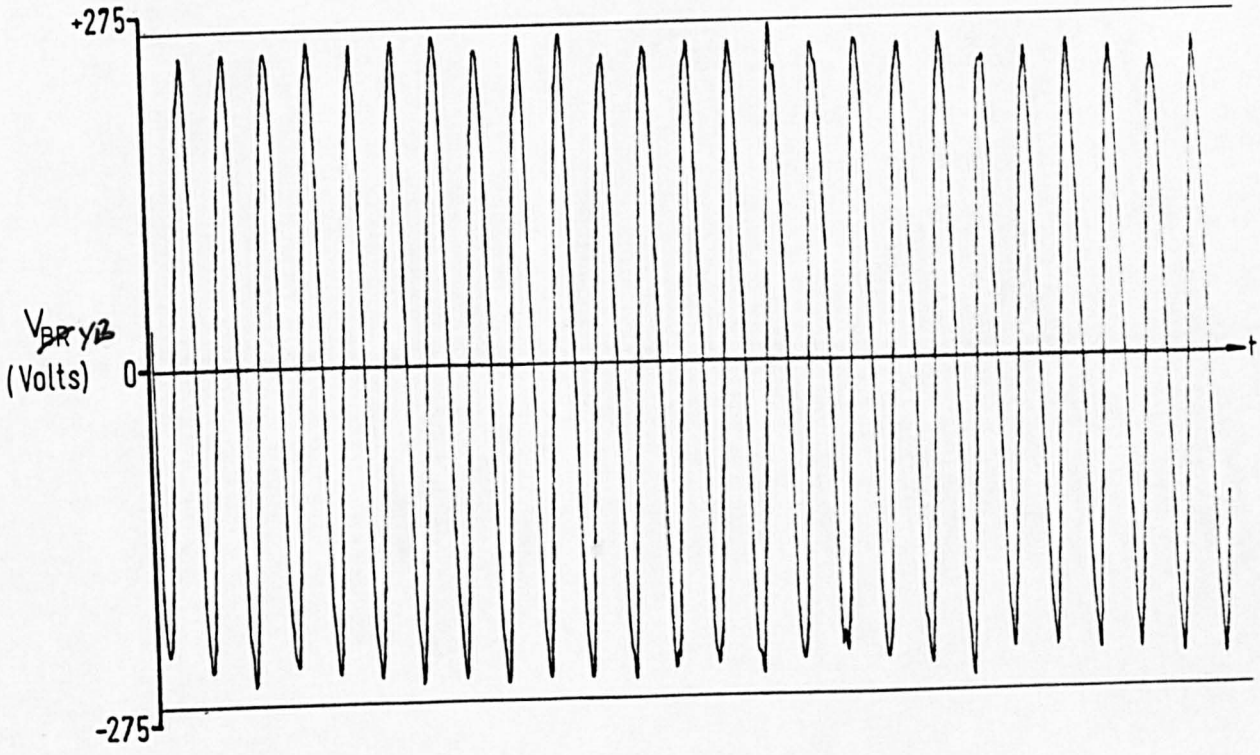


Fig. 2.20 : V_{yB} with arc furnace model operating

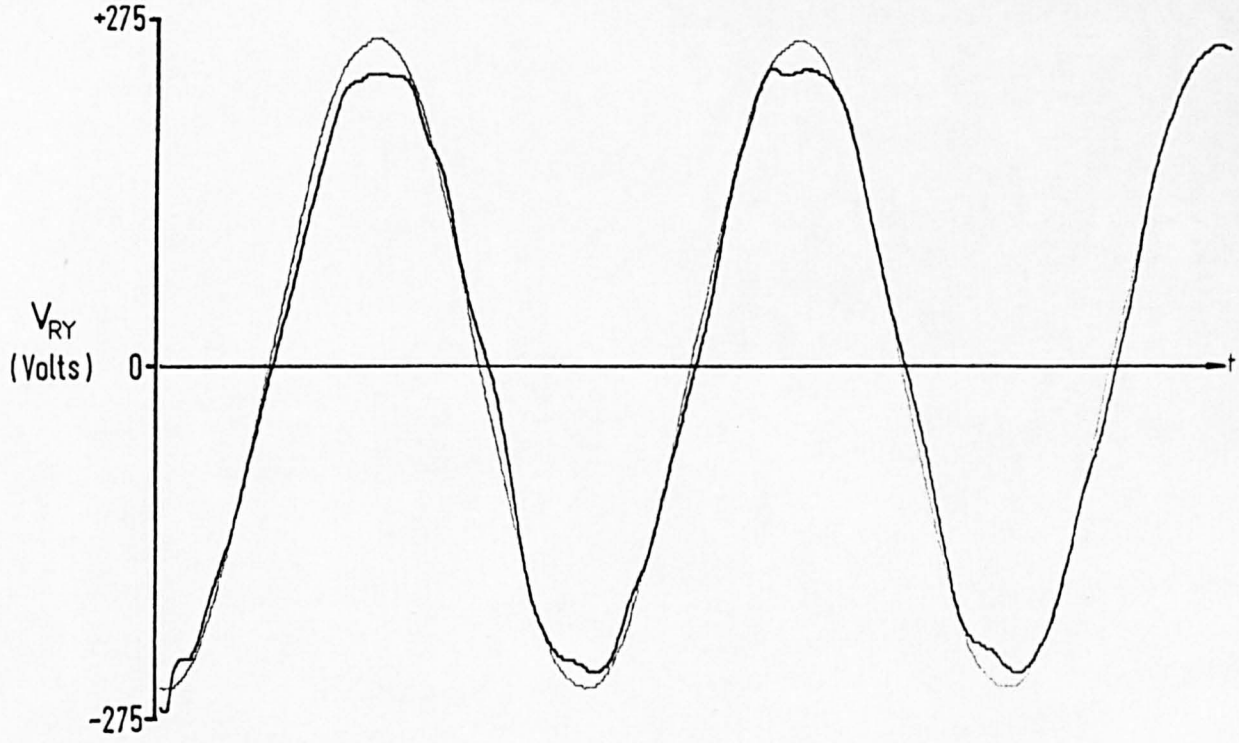


Fig. 2.21 : Detail of distorted ~~Vbr~~ ry

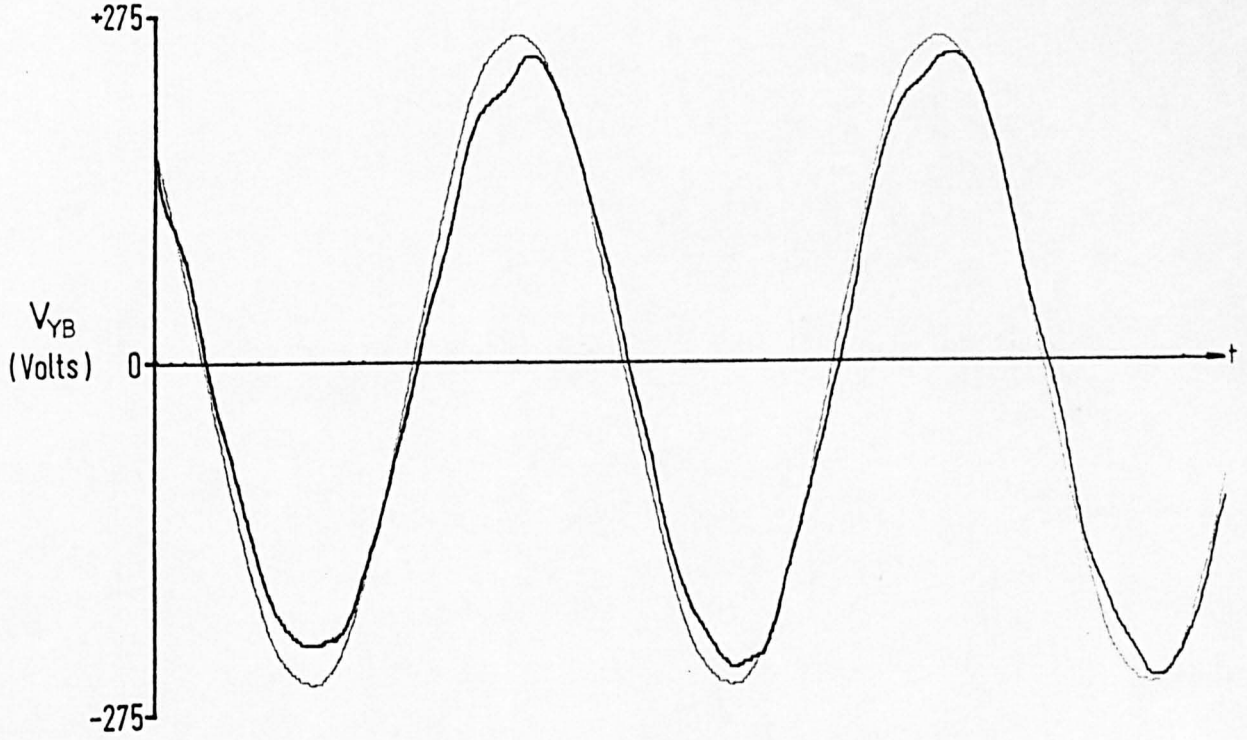


Fig. 2.22 : Detail of distorted Vyb

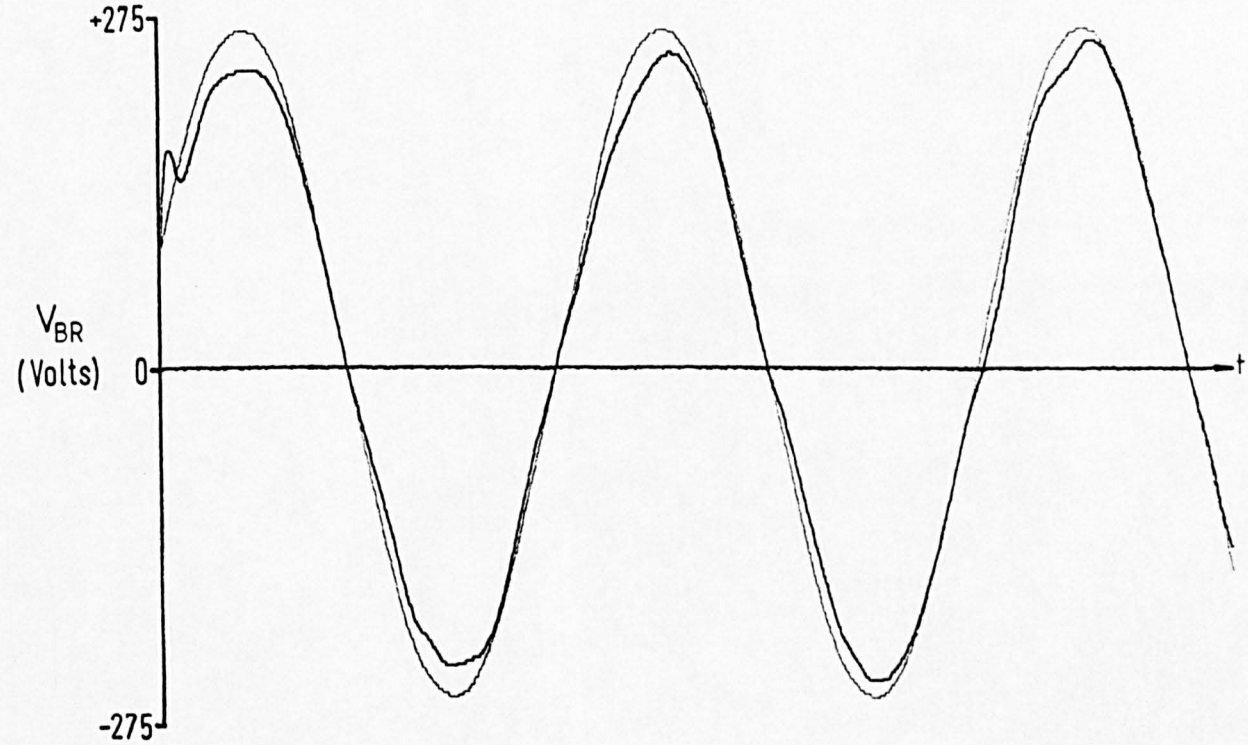


Fig. 2.23 : Detail of distorted Vby

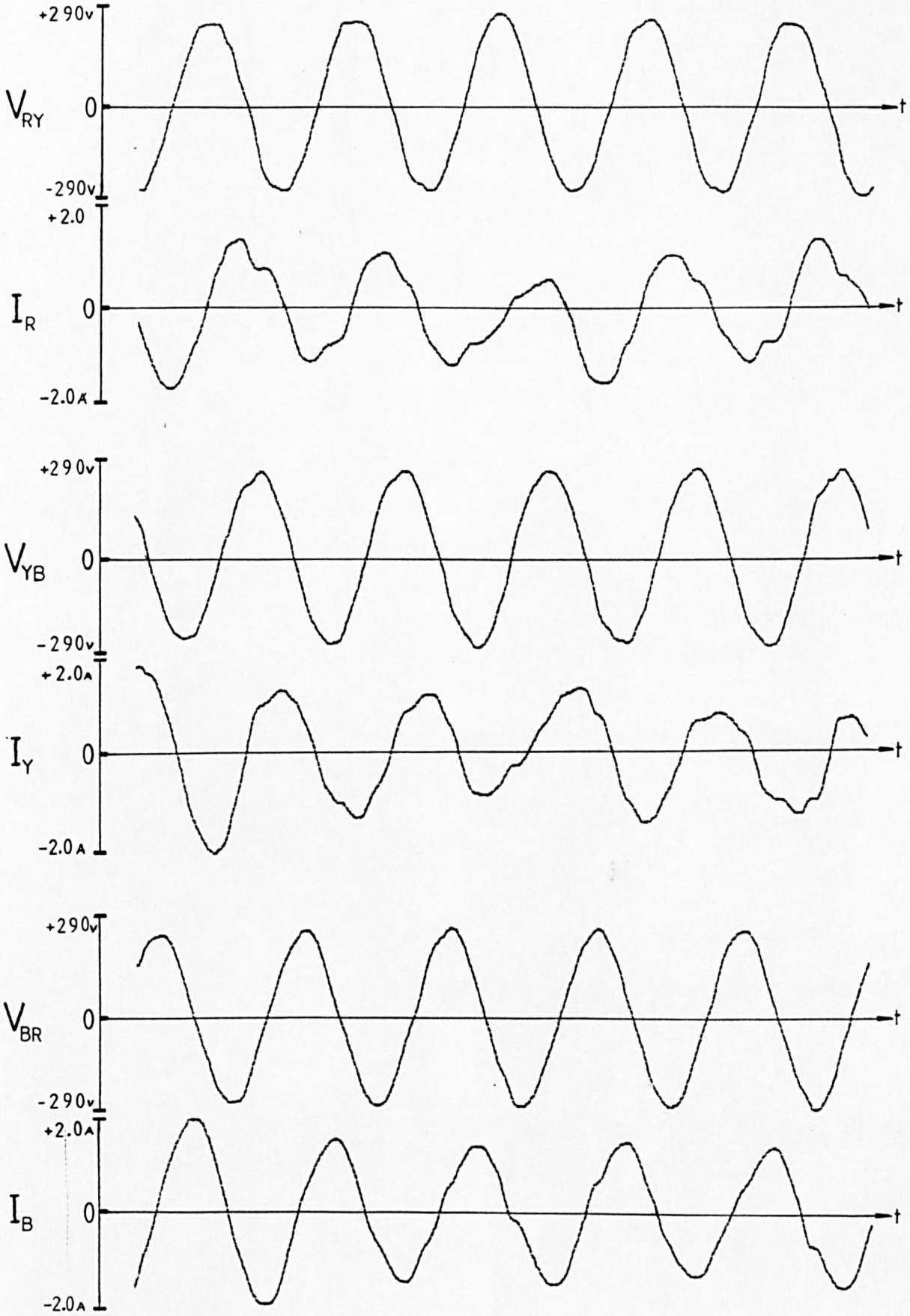


Fig. 2.24 : Arc furnace model three phase voltages and currents

The relevance of V_f in these studies is described further in Part 3.1, and Section 8.4.3 studies the results from a digital model in both the full form and the demodulated form. It is shown that analysis of the power spectral density can give valuable information about the continuous signal in the time domain. A large number of power spectra are used for performance studies in Chapter V, and Section 5.2.1 discusses further the procedures available for obtaining a power spectrum, and explains the techniques chosen for the laboratory.

The aim here is simply to present power spectra of the time domain signals seen in 2.4.2 above, in order to demonstrate the laboratory model's ability to reproduce distorted voltages which model those occurring in the full size system.

Each spectrum gives a measure of the power of frequency components which make up the continuous signal. The power components at different frequencies are presented in decibels (dBs) relative to the power in the fundamental component at 50Hz. Measurements were made using a commercial spectrum analyser[118] with output to an X-Y flat-bed plotter.

Figure 2.25 shows the power spectrum to 250Hz of a laboratory signal generator producing only a 50Hz sinusoid. The 3rd harmonic component is visible at approximately -60dB relative to the fundamental, and noise is present across the spectrum between -75dB and -80dB.

Figure 2.26 gives the equivalent power spectrum of the open circuit laboratory supply line voltage. The 2nd, 3rd, 4th and 5th harmonic components are clearly shown above the same noise levels of approximately -75dB.

Figure 2.27 shows the power spectrum to 500Hz of the line voltage distorted by operation of the arc furnace model at the rated level of current. Disturbances across the whole spectrum are evident between -45dB and -65dB, and the magnitude of the harmonic voltages is also increased slightly by components in the current waveform of the furnace model.

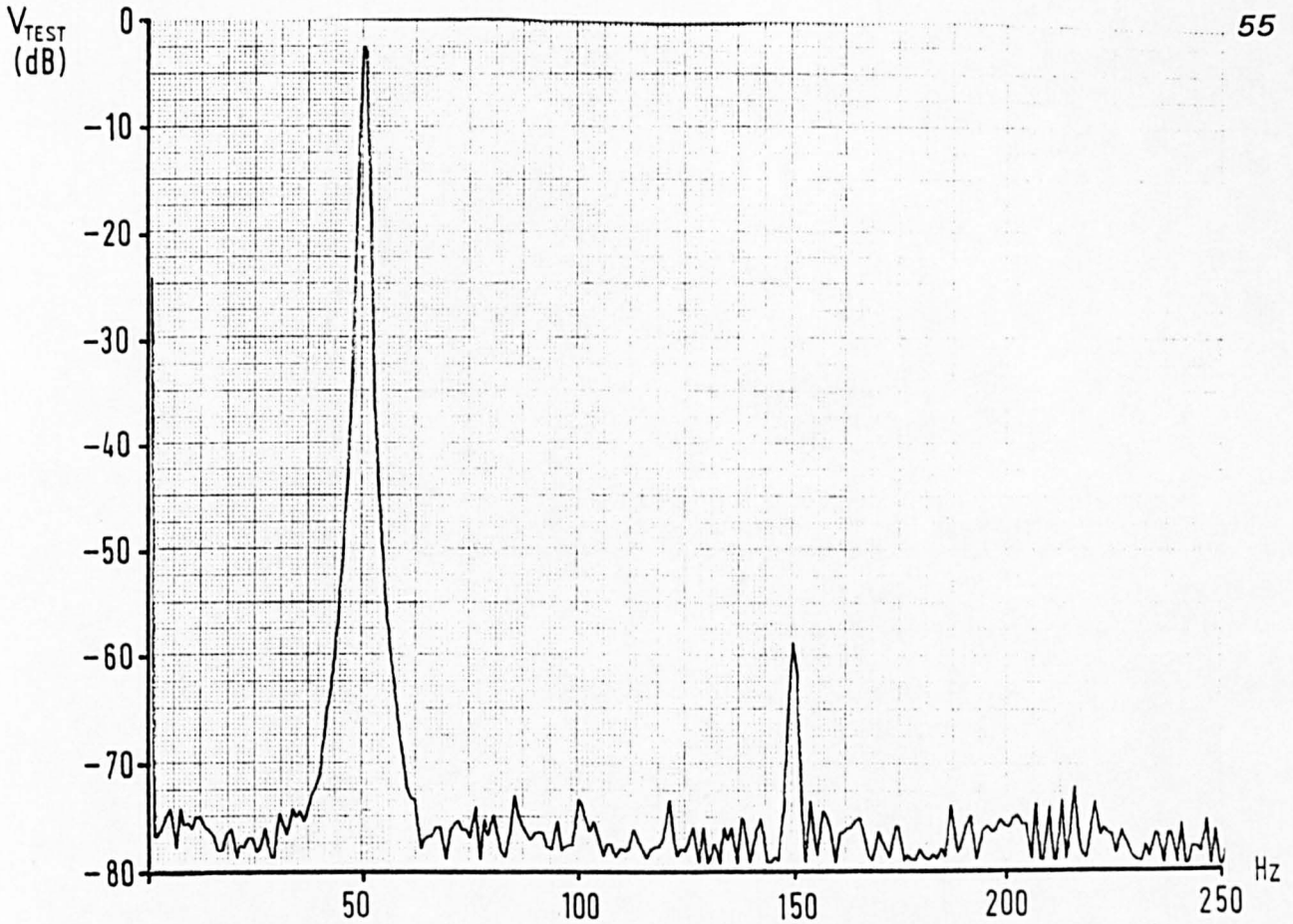


Fig. 2.25 : Power spectrum of 50Hz test sinusoid

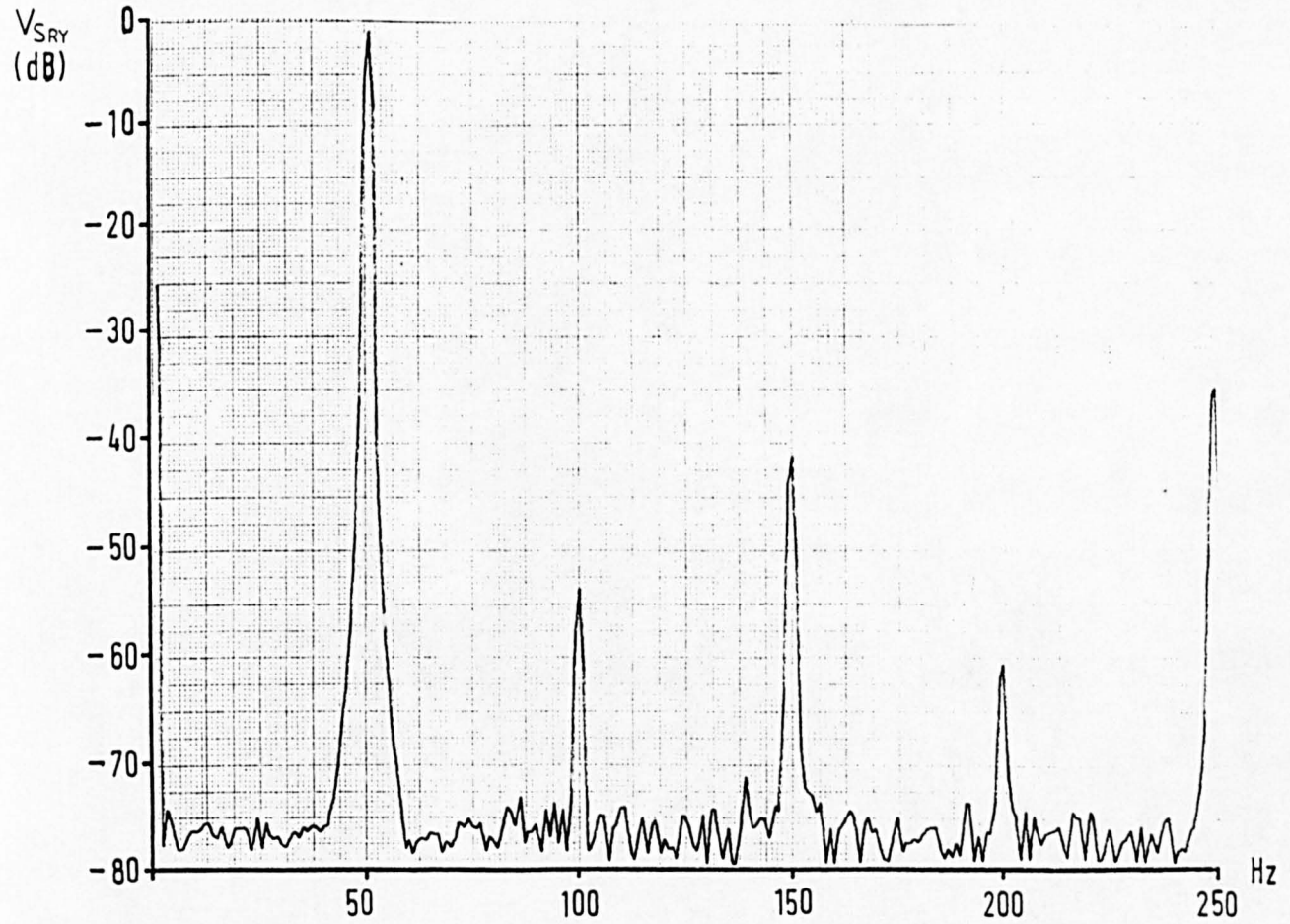


Fig. 2.26 : Power spectrum of open circuit supply line voltage

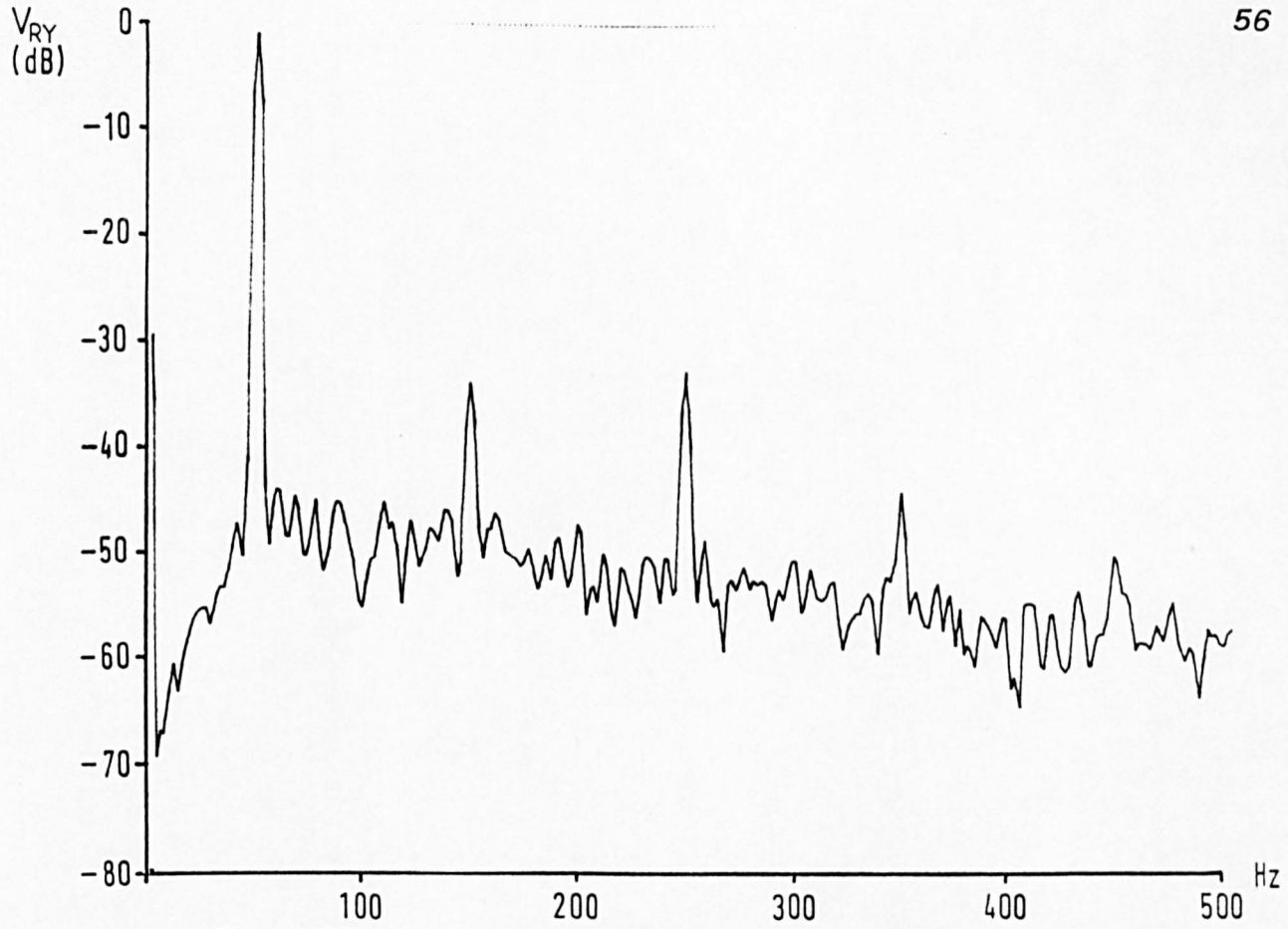


Fig. 2.27 : Arc furnace model Vry power spectrum to 500Hz

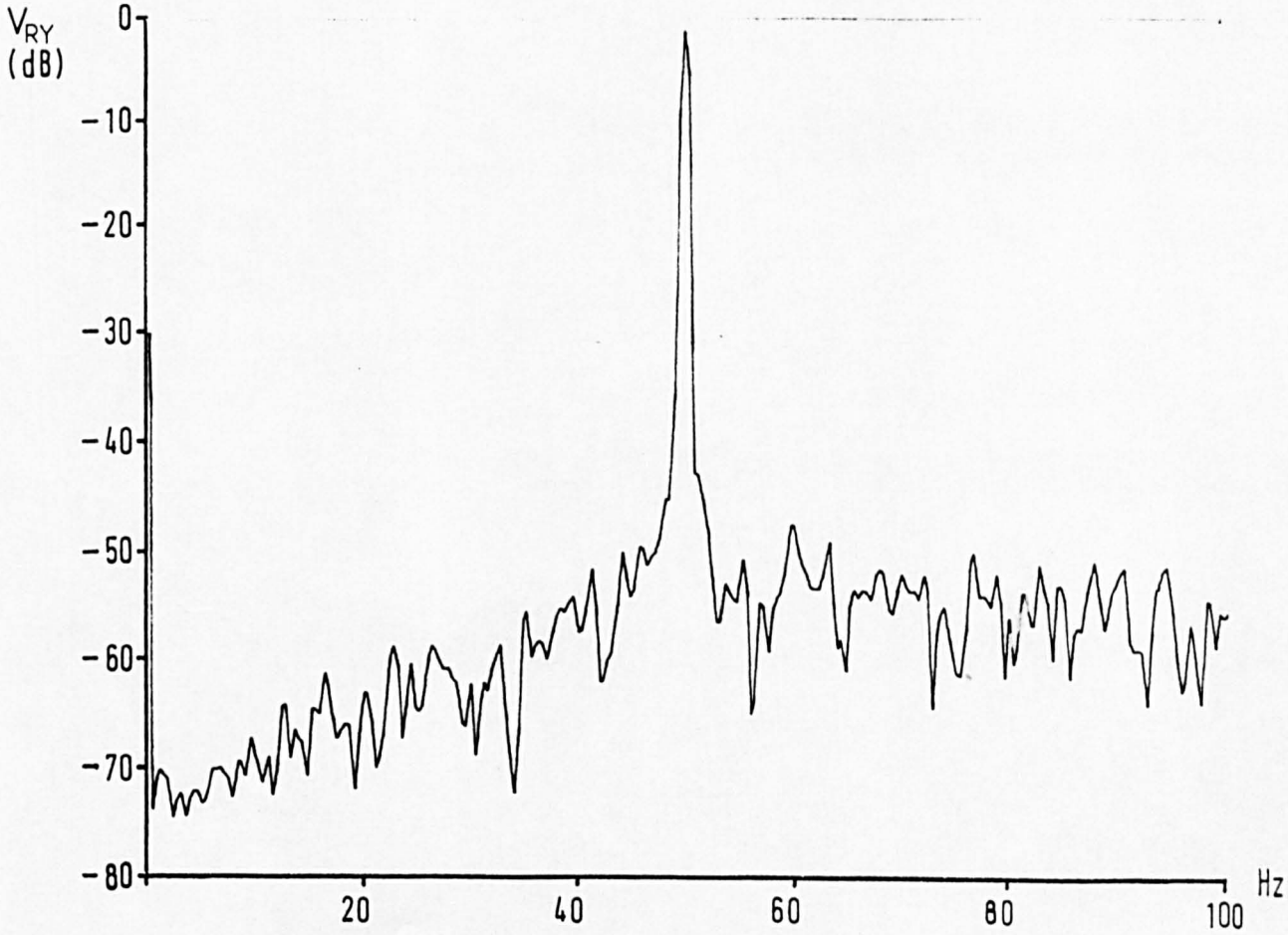


Fig. 2.28 : Arc furnace model Vry power spectrum to 100Hz

Chapter III shows that modulation frequencies between 1Hz and 30Hz are of primary interest for the investigation of tungsten filament lamp flicker. The power from these modulating frequencies will lie in the sidebands above and below the 50Hz 'carrier' signal. These are shown more clearly in Figure 2.28 - the disturbance levels of between -50dB to -70dB in the power spectrum will correspond to voltage components between -25dB and -35dB relative to the 50Hz voltage waveform.

Figures 2.27 and 2.28 may be compared with Figures 2.29 and 2.30 which show the corresponding power spectra of the line voltage recordings made at 33kV. This comparison illustrates the success of the model in reproducing the voltage disturbances evident at the Templeborough installation.

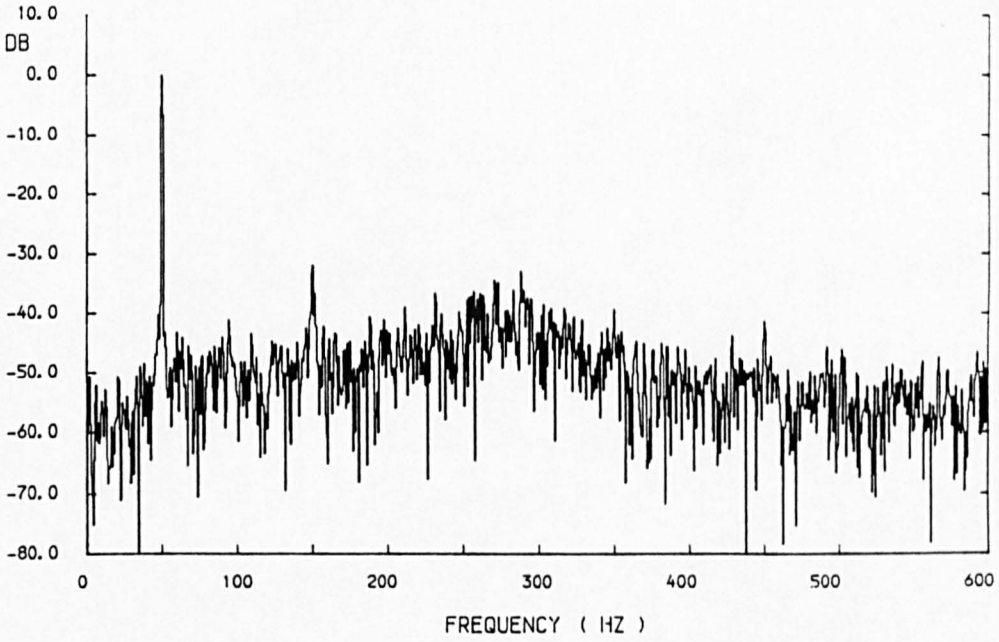


Fig. 2.29 : 0-600Hz power spectrum of CEGB recorded Vry

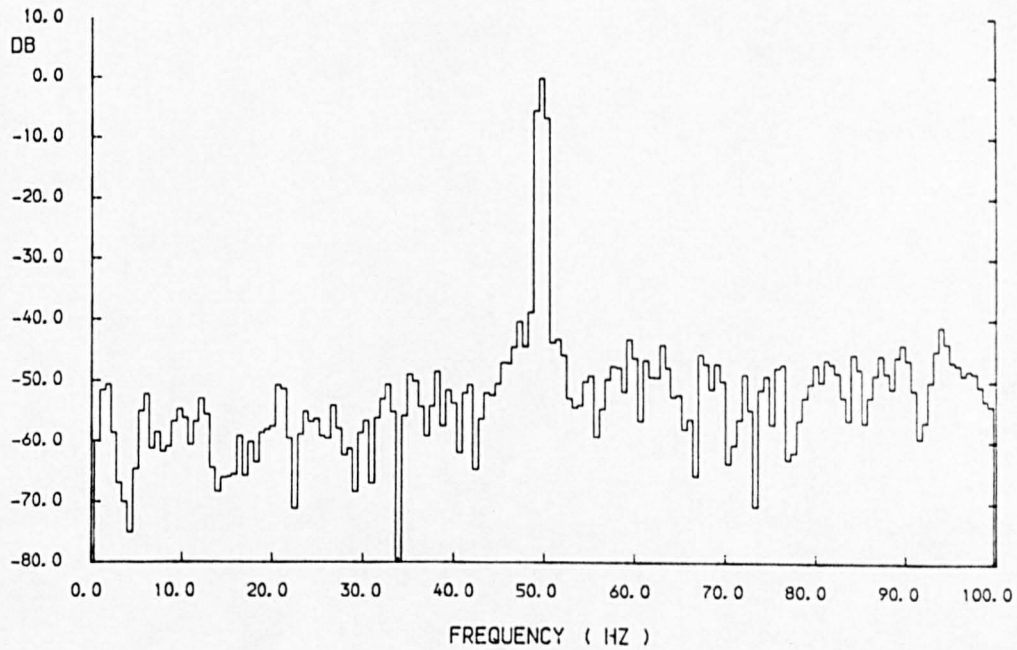


Fig. 2.30 : 0-100Hz power spectrum of CEGB recorded Vry

CHAPTER THREE

FLICKER AND ITS REDUCTION

3.1 FLICKER

The flickering of tungsten filament lamps due to distortion of the supply voltage waveform is not a new phenomenon. A survey in 1956[1] associated the occurence of flicker with arc furnace installations connected to the power supply system. Since that time there have been significant advances in the understanding of how various factors in a distorted supply voltage effect flicker perception and annoyance[2-20]. Naturally, an understanding of the causes of lamp flicker perception is useful when its reduction is being considered.

3.1.1 V_f - A 'Flicker Voltage'

Dixon and Kendall[8] used the concept of a 'flicker voltage', V_f, in their studies of annoyance factors for different combinations and magnitudes of frequencies superimposed on the supply voltage waveform. If the distorted waveform is considered as a 50Hz 'carrier' frequency that is amplitude modulated by any combination of other frequencies, then V_f represents the arithmetic sum of those frequency components in the time domain. Figures 3.1(a),(b) show a graphical representation of V_f that is often used.

V_f can be obtained in practice using 50Hz notch filters with passband and cut-off characteristics to suit the levels and frequencies of modulation voltage that are to be studied. Digital filtering techniques may also be employed where suitable processing capability is available.

3.1.2 Frequency Dependence of Flicker

A distorted supply voltage waveform may easily be synthesised - methods include repetitive load switching, on-line computation and electronic modulation techniques[13]. V_f can then be simply restricted to a single frequency that may be varied at will.

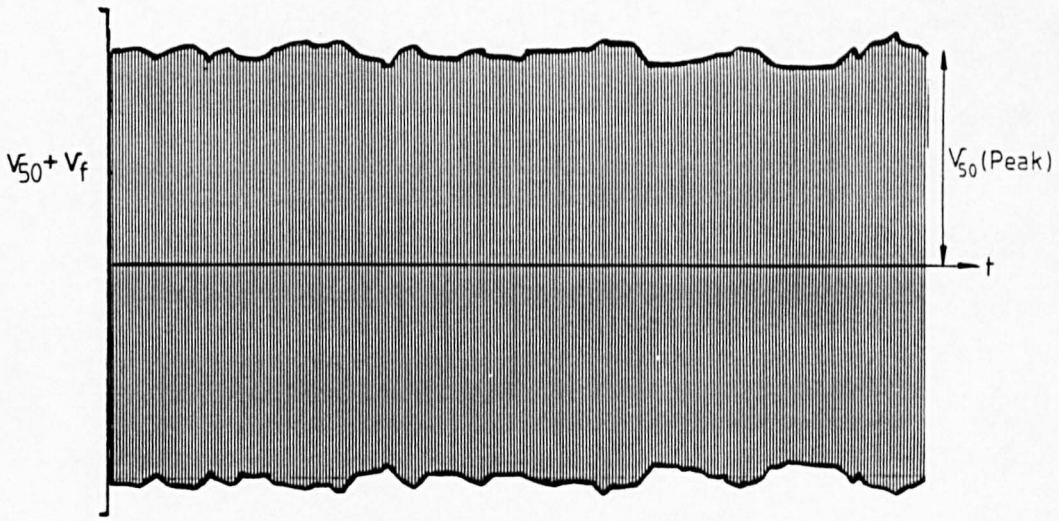


Fig. 3.1(a) : Amplitude modulated 50Hz supply waveform

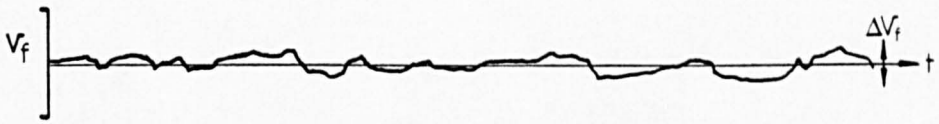


Fig. 3.1(b) : Flicker voltage Vf from demodulation

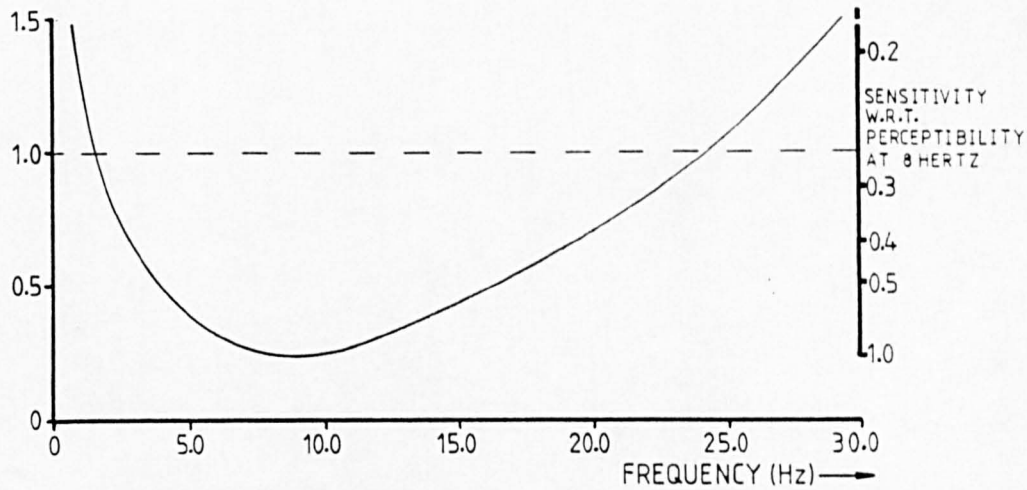


Fig. 3.2 : Normalised sensitivity to flicker frequency

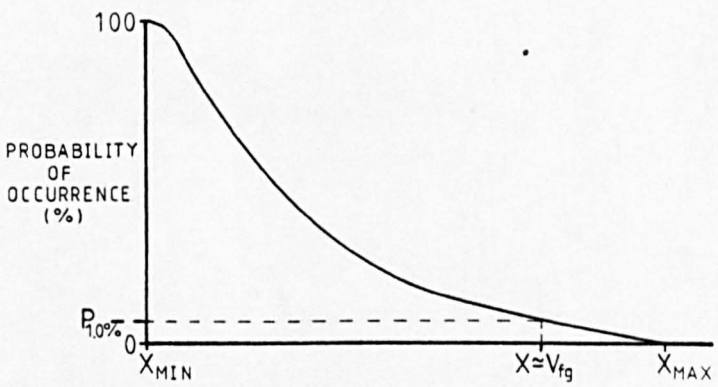


Fig. 3.3 : Example of a cumulative probability curve

The magnitude of V_f that gives an annoying level of lamp flicker at a given frequency is highly subjective, it is also related to the environment and activity of the subjects. Research has enabled a weighting curve to be produced[5],[7],[14],[16] (Fig. 3.2). This curve represents the transfer function of lamp + eye + brain, with a distorted voltage as the input and physiological response to lamp flicker as the output. It is clear that flicker voltages with frequencies in the range 2-20Hz will cause greatest complaint if the level of V_f is constant.

Flicker voltages with frequencies outside of this range cannot be neglected if the relative magnitude of V_f is large at such frequencies.

The flicker voltage, V_f, will rarely be a sinusoid at a single frequency. Any $v_f(t)$ can, however, be represented by its spectrum of sinusoids in the frequency domain $v_f(\omega)$[91,92]. The annoyance effect of non-sinusoidal $v_f(t)$ can thus be evaluated using the magnitudes of its individual frequency components.

3.1.3 Annoyance Levels

No mention has yet been made of the magnitude of V_f. Since V_f is a measure of the distortion of a sinusoidal supply voltage V_{fund}, it is logical to relate V_f to V_{fund}. The UK Electricity Council's 1970 Recommendations[6] use the ratio of RMS quantities, but increasing use is being made of the definition

$$V_f(\text{p.c.}) = \frac{V_f \text{ (peak to peak volts)}}{V_{fund} \text{ (peak volts)}} \times 100\text{p.c.}$$

which is used by the UIE[19].

In most cases $V_f(t)$ is not a periodic function but is a stochastic process - random within certain statistical bounds. In such cases an observation lasting only a short time may not be representative of the continuous signal, and the question of how to treat successive observations becomes important. The accepted method in the UK for analysis of flicker measurements is to generate a Cumulative Probability Function (CPF)[14,16].

Figure 3.3 shows an example of a CPF - the ordinate is a percentage probability that the abcissa (the measured quantity) corresponding to a point on the curve will be equalled or exceeded. The percentage probability is based purely on all observations within some time period. Thus all of the observations exceed the lowest measured value, and the probability that this lowest measured value will be exceeded is 100p.c.,

i.e. $P_{100p.c.} = Xmin$

The UK Electricity Council's recommendation[6] is that the RMS ratio $V_f(p.c.)$ be used as the measured quantity. The value of V_f then corresponding to $P_{1.0p.c.}$ is defined as V_{fg}, the gauge-point fluctuation voltage. Obviously for different levels of supply voltage distortion V_{fg} will take a different value. The recommendation[6] is that the limits for V_{fg} be set at:

V_{fg} = 0.25p.c. for network voltages up to 132kv
V_{fg} = 0.20p.c. for networks above 132kv

These values were chosen in view of tests[7] which showed how a continuous level of fluctuation voltage related to subjective flicker perception:

V_f = 0.20p.c, -54.0dB Just perceptible, but not annoying
V_f = 0.25p.c, -52.0dB Obvious, but not annoying
V_f = 0.30p.c, -50.5dB Uncomfortable or intolerable
V_f > 0.30p.c, -50.5dB Intolerable

Later studies[14,16] have shown the importance of frequency-weighting the measured value V_f, and of using more figures from the CPF (e.g. $P_{0.1p.c.}$, $P_{1.0p.c.}$, $P_{3.0p.c.}$, $P_{10.0p.c.}$) for a more accurate representation of the flicker severity factor of a distorted supply voltage waveform.

3.2 THE ELECTRIC ARC FURNACE AS A FLICKER SOURCE

The non-sinusoidal nature and imbalance of three-phase currents drawn by an arc furnace has already been illustrated, using a block of data from the CEGB recordings, (Fig. 2.3). The severity of these current fluctuations for a given furnace installation is not constant, but a function of several factors:

(i) The point in the arc furnace melt-cycle.

(ii) The type of material to be melted down, and its movement within the furnace crucible.

(iii) The combined effects of electrode control apparatus and human operator actions.

The consequent disturbances of the supply voltage waveform experienced by other consumers will then depend on:

(iv) The point from which their electrical supply is derived (the Point of Common Coupling).

(v) The impedances present between furnace installation, consumer and the 'infinite busbar'.

Each of the above points are now examined in more detail.

3.2.1 The Arc Furnace Melt-Cycle

The melt-cycle is defined as the sequence of events normally followed in order to produce usable molten steel from solid constituents. The start of the cycle sees the first 'basket' of metal dropped into the furnace crucible. The electrodes lower and arcs are struck between them and the surface of the metal.

As the electric arc bores down into the heap of metal, the electrodes are lowered. When the electrode tips are below the top of the metal, maximum voltage is applied via the on load tap changer. For this 'bore-down' stage the arcs are now long and maximum energy is transferred to the scrap surrounding the arcs (Figure 3.4(a)). The full power 'bore-down' is continued until much of the metal lies in a molten pool. The arc is then extinguished and a second basket of metal is added. The 'bore-down' process is repeated, then medium power is used when there is little metal projecting from the molten pool - this reduces wear on the refractory lining of the furnace, which would otherwise be exposed to the full power output from the arcs (Figure 3.4(b)).

When all of the metal has been liquified, a sample of the melt indicates how the metal can be refined to give the quality of steel required. Chemical additions are made and refining is carried out with very low power input to the molten pool (Figure 3.4(c)).

Example times for the above processes for a 100 Tonne, 70MVA furnace are[121]:

First Basket Bore-down	30 mins
Second Basket Bore-down	25 mins
'Medium Power' melting	10 mins
Refining	20 mins

The most severe fluctuations in furnace current occur during the two 'bore-down' periods when large pieces of metal may fall in the immediate region of each arc, which will be operating at full power. Phase to phase short circuit and/or single phase open circuit conditions lasting for several seconds may arise, and the cycle-by-cycle current waveform is mainly non-repetitive, reflecting varying arc length after the extinguishment and re-striking of the arc around current-zero.

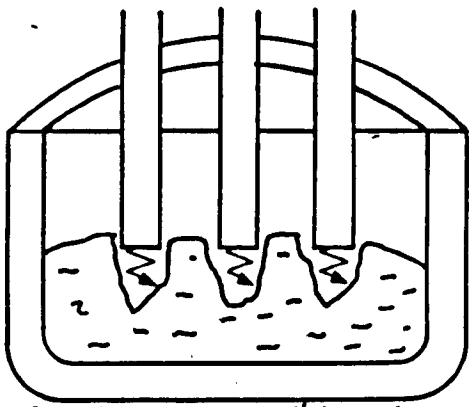


Fig. 3.4(a) : Arc furnace crucible - bore down

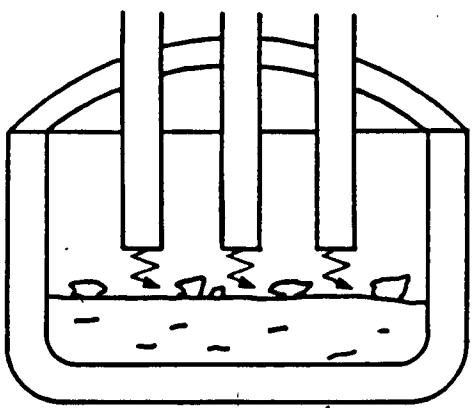


Fig. 3.4(b) : Arc furnace crucible - medium power

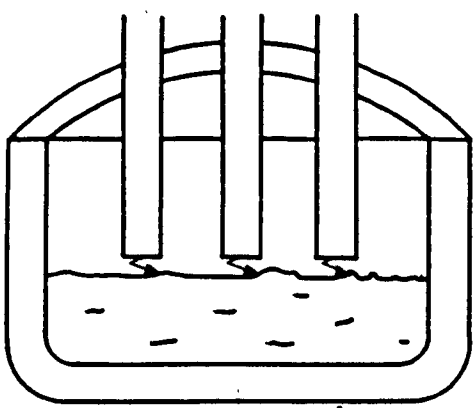


Fig. 3.4 : Arc furnace crucible - refining

3.2.2 Composition of Melt-Baskets

Each basket of metal to be melted may contain a mixture of the following types of scrap metals:

(i) Turnings - From industrial machining process.
(ii) 'Fragmentised' medium duty steel structures.
(iii) Rod or Billets - probably produced at the same steelworks.
(iv) Slag scrap collected from previous melts.
(v) 'No. 1' scrap - an assortment of heavy and medium duty steel previously cut to fit into crucible.
(vi) Plate iron.
(vii) 'Bales' - a clean scrap steel compressed into large blocks.

The composition of particular baskets is varied to suit the grade of steel required, and to a lesser extent the relative quantities available[121].

Turnings or 'swarf' will give the most consistent arc behaviour and hence the smallest current variations. 'bales' of compressed steel take longest to melt down and their movement in the crucible can create severe fluctuations in arc current.

3.2.3 Operators and electrode control systems

Automatic electrode control systems are used on all but the smallest of arc furnaces. Their primary function is to keep the arc current near constant for a given electrode voltage. If the electrode voltage is increased, a larger arc can be sustained and the power input to the furnace is greater.

Short circuits in the furnace cause the electrodes to be withdrawn, open circuits cause them to be lowered. The methods of control need not be discussed here since there is much information in the literature[93,94].

Operators in the furnace control room will manipulate furnace transformer on-load tap changers and circuit breakers, and utilise electrode controllers to progress through the melt cycle in a way that they see fit. Thus additional variations will exist for different melt-cycles.

Further information on almost every aspect of electric arc furnace operations is given by Robiette[93].

3.2.4 Voltage Distortion due to an Arc Furnace Installation

A load drawing a non-sinusoidal current from a sinusoidal supply e.m.f. will cause distortion of the voltage at its terminals provided there is some impedance present in the current path.

Figure 3.5 shows a representation of a power system supplying an arc furnace installation and other consumers. The 'point of common coupling' (PCC) is defined[6] as the electrical point nearest to the arc furnace installation to which other consumers are connected.

On a large power system, the reactive components of impedances usually exceed the corresponding resistive components by a factor of at least 20, thus if

$$Z_s = R_s + jX_s \quad \text{and} \quad Z_f = R_f + jX_f$$

then $$Zs \simeq jXs \quad \text{and} \quad Zf \simeq jXf$$

Where Z_s and Z_f represent the system and furnace impedances respectively. The corresponding phasor diagram for $I = Is \simeq If$ lagging V_0 by a phase angle $\emptyset$ is shown in Figure 3.6. Clearly if $V_{af} \gg IX_{tot}$ then the arithmetic difference, ΔV, between the voltages V_0 and V_{af} can be written:

$$\Delta Vaf \simeq I \sin \emptyset \, Xtot$$

$$\text{and} \quad \Delta VPCC \simeq I \sin \emptyset \, Xs$$

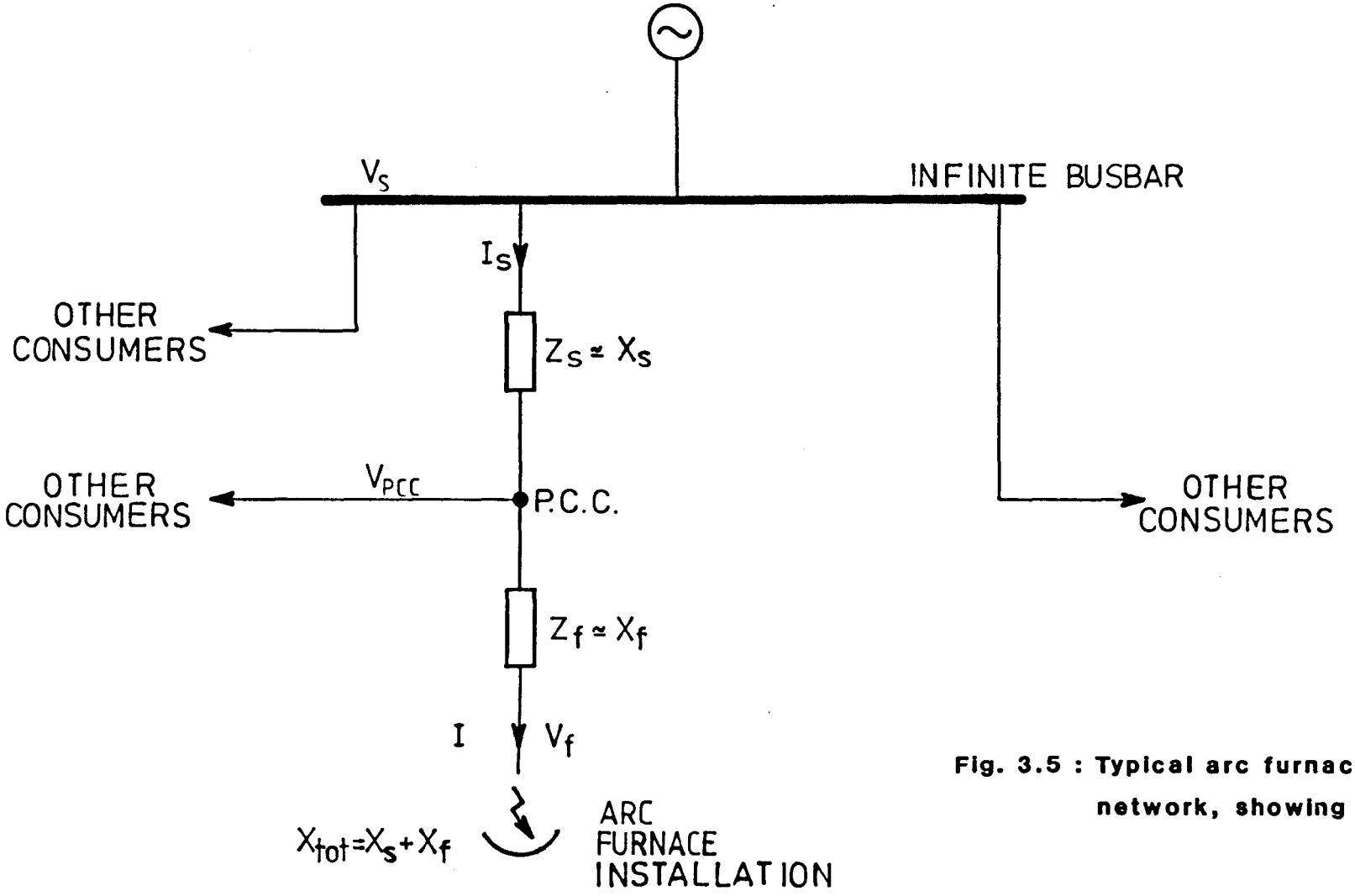


Fig. 3.5 : Typical arc furnace supply network, showing PCC

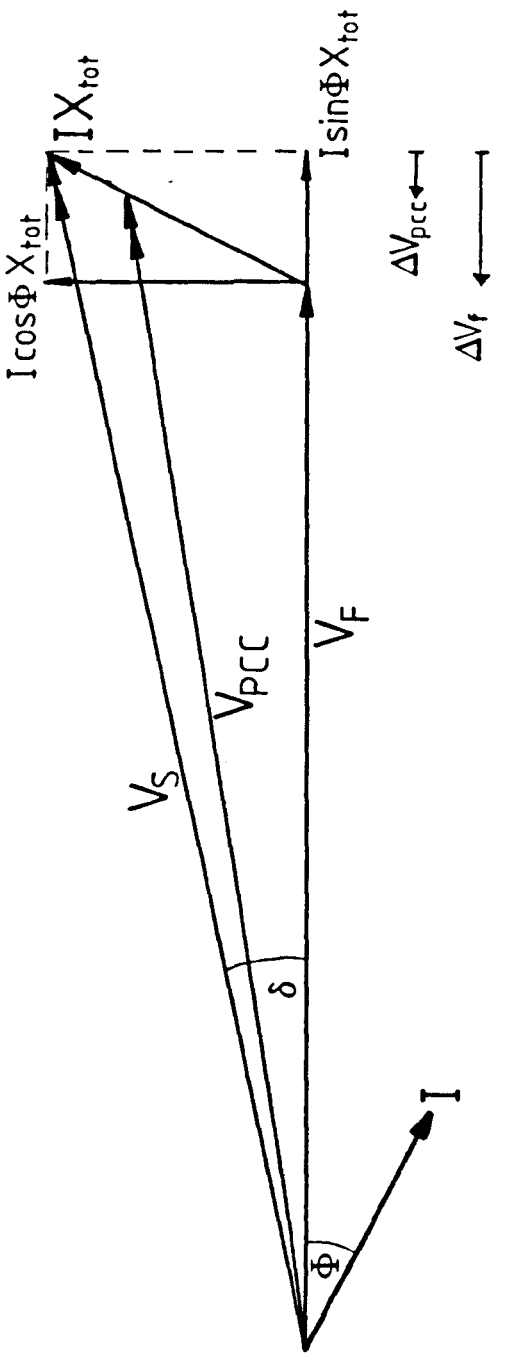


Fig. 3.6 : Phasor diagram for voltages at system, PCC and furnace installation

Thus the voltage fluctuations at the point of common coupling are primarily due to variations in the reactive component of I.

Arc furnaces operate at a power factor of 0.7-0.8 at full load [93] i.e. $I\sin\phi \simeq 0.6I$. Thus the reactive component of I(t) is not negligible. The measurements of i(t) (Figure 2.3) were shown to have power spectral density components at levels between -25dB and -45dB in the critical modulation band of 0-30Hz (Figure 2.12) - the effect of these current fluctuations is further studied below.

3.3 FLICKER LEVELS ON A PARTICULAR FURNACE SUPPLY AND ITS MODEL

A method for predicting the severity of perceived tungsten filament lamp flicker from a knowledge of the arc furnace and supply system details is contained in the UK Electricity Council Recommendations on arc furnaces and their supply[6]. Firstly, this method will be applied to the Templeborough power system used for the CEGB measurements (see Section 2.1.1), and secondly to the laboratory model of that system. Impedances in each network may be represented in the form used in reference [6], and repeated in Figure 3.7.

The results may then be related to measured values of the flicker voltage, V_f.

3.3.1 Study for the Templeborough Installation

The voltage depression caused at a point on the supply network to an arc furnace installation is primarily dependent upon two quantities:

(i) The short-circuit power of the arc furnace,

and (ii) The fault level at the point of study.

A quantity V_t, the Short-Circuit Voltage Depression, is defined[6] as:

$$V_t = \frac{S_t}{S_c} \times 100\text{p.c.}$$

Where S_t and S_c are the furnace short-circuit power and fault level at the point of common coupling respectively. The precise definition of these quantities and a discussion of typical values is given in detail in Reference [6] and need not be repeated here.

The short-circuit power, S_t, of the arc furnace can be either measured directly or calculated from other data[6]. A general method for performing this calculation given in Reference [6] is followed in Appendix A. This gives:

$$\underline{S_t = 87.46\text{MVA}}$$

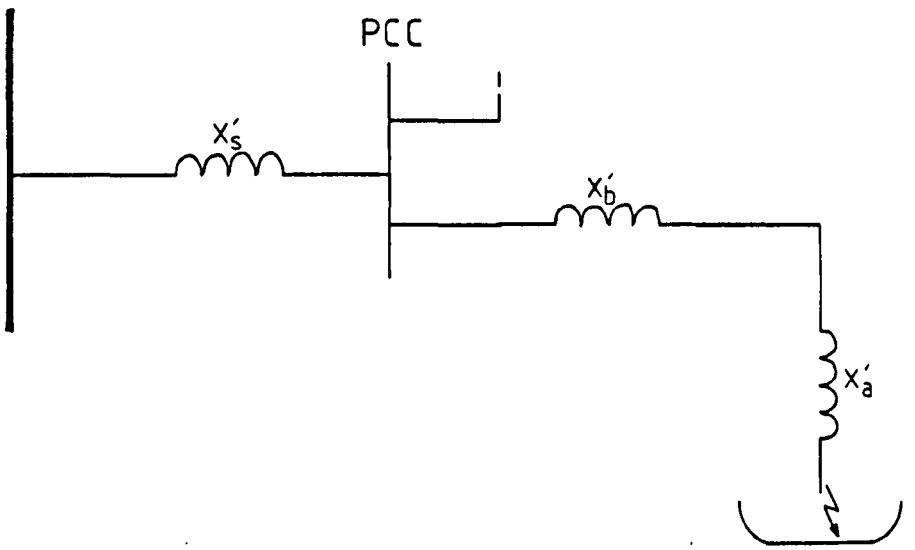


Fig. 3.7 : Electricity Council notation for arc furnace supply system

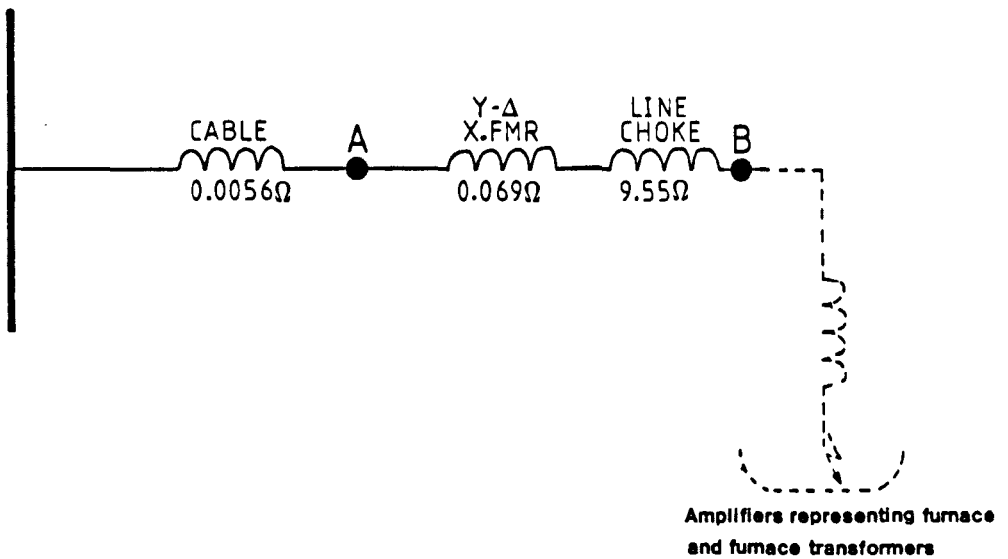


Fig. 3.8 : One line diagram of the laboratory arc furnace model supply

It will be useful to note the 33kV short circuit current here:

$$Isc = \frac{87.46 \times 10^6}{\sqrt{3} \times (33 \times 10^3)} = 1.53kA \text{ or } \underline{0.875}p.u.$$

S_c, the fault level for the point of calculation of V_t is easily found:

At 275kV $S_c = \frac{100}{X_s'}$ = 8500MVA, giving V_t (275kV) = 1.03p.c.

At 33kV $S_c = \frac{100}{X_s' + X_b'}$ = 400MVA, giving V_t (33kV) = 21.87p.c.

V_{fg} can now be predicted from V_t:

$$V_{fg} = k_s V_t$$

where the 'severity factor', k_s, is usually in the range 0.09 to 0.15 with a mean at 0.12[6].

Thus for k_s =	0.09,	0.12,	0.15
V_{fg} (275kv) =	0.093p.c.,	0.123p.c.,	0.154p.c.
V_{fg} (33kv) =	1.97p.c.,	2.62p.c.,	3.28p.c.

It will be noted that the theoretical value of V_{fg} at 275kV is well below the flicker perceptibility threshold of 0.20p.c. described in Section 3.1.3. Tests conducted by the Electrical Research Association (ERA)[6] for the same system support this, in so far as there were no complaints from consumers with the PCC at 275kV.

3.3.2 Study for the Physical Model

If the Templeborough system has been modelled with sufficient accuracy, then the model's values of V_{fg} will be identical to those found in the preceeding section. It will be useful to give an analysis for the physical model, so that the relevance of different impedances may be appreciated.

In section 3.3.1 the furnace short-circuit current, I_{sc}, was shown to be 0.875p.u. If the model's current base has been scaled correctly, this will be equivalent to a current of:

$$\begin{aligned} I_{sc} &= 0.875\text{p.u.} \times I_{base} \\ &= 0.875\text{p.u.} \times 2.659\text{A} \\ &= 2.33\text{A} \end{aligned}$$

For V_L = 1.0p.u. = 175v, the short-circuit power is therefore:

$$S_t = \sqrt{3}\,(175)(2.33) = \underline{706\text{VA}}$$

Figure 3.8 gives a one line representation of the model, with all ohmic impedances referred to 175 volts. Point A corresponds to the 275kV point of common coupling whilst point B corresponds to the 33kV busbar.

The model's bases will be repeated here for reference:

V_{base}=175V, X_{base}=38.0 Ohms, I_{base}=2.659A, VA_{base}=805.9VA

$$X_s' = 0.0056\ \text{Ohms} = \frac{0.0056}{38.0}\ \text{p.u.}$$

$$= 0.00015\ \text{p.u. to the model's bases}$$

$$X_b' = 0.069 + 9.55\ \text{Ohms} = \frac{9.619}{38.0}\ \text{p.u.}$$

$$= 0.2531\text{p.u. to the model's bases}$$

Then the Fault Level at A is:

$$S_{CA} = \frac{805.9}{0.00015} = 5.37\text{MVA}$$

and at B:

$$S_{CB} = \frac{805.9}{0.2531} = 3184\text{VA}$$

These values are calculated using reactive impedance components only, as for the full scale system. However, the X/R ratio for the system is large - typically 20 or more, against the models' X/R ratio of approximately 10. The error in Sc introduced by not taking account of resistances is thus -0.5p.c. for the model compared to -0.1p.c. for the real system. Although small, these errors should be borne in mind.

To find the short circuit voltage depression, V_t, at A and B:

$$V_t = \frac{S_t}{S_c},$$

Therefore, $$V_{tA} = \frac{706}{5.37\ 10^6} = 0.013\text{p.c.}$$

$$V_{tB} = \frac{706}{3184} = 22.8\text{p.c.}$$

and using $V_{fg} = k_s V_t$

for k_s = 0.09, 0.12, 0.15

V_{fgA} = 0.0012p.c., 0.0016p.c., 0.0020p.c.

V_{fgB} = 2.05p.c., 2.74p.c., 3.42p.c.

Thus the short-circuit voltage depression at B accurately represents that in the real system at 33kV.

(The real system has V_t = 1.05p.c. at 275kV
and V_t = 21.87p.c. at 33kV)

This is reasonable if the voltage fluctuations at the 33kV busbar are to be studied - although in the case of Templeborough this was not the PCC. The disturbance levels at point B (Figure 3.8) will be much higher than those found to be 'just annoying' since the theoretical V_{fg} is approximately 2.0p.c. compared with the 0.25p.c. limit[6].

If flicker compensation at this level can be achieved, then any improvement factor will still hold true for voltage disturbances further away from the flicker source.

Figure 2.30 showed the power spectral density of the red-yellow line voltage derived from the CEGB recordings at 33kV. The section of data corresponds to those 90 cycles used by the physical model, and it was presented in Section 2.4.3 to allow comparison of 33kV and modelled line voltage power spectra.

Communication theory[92] would present the power spectrum of a simple amplitude modulated carrier wave as sidebands symmetrical about the carrier frequency. The total signal power P_{TOT} is related to the carrier power P_c and the modulation index 'm' as:

$$P_{TOT} = P_c \left(1 + \frac{m^2}{2}\right)$$

with power $\frac{P_c m^2}{4}$ in each sideband.

The arc furnace non-sinusoidal current's power spectra (Figure 2.12) show reasonable symmetry about the 50Hz fundamental frequency. But the corresponding power spectra for the distorted supply voltage (Figure 2.28) show that the frequency components in the upper sideband have slightly higher powers than the frequency components in the lower sideband. Such an effect may be caused by a system impedance that varies in the range 0-100Hz, with a shunt inductance component becoming relevant at very low frequencies.

3.4 FLICKER REDUCTION

Chapter I introduced a variety of methods for reducing the levels of flicker at a PCC. Each method achieves a reduction in the flicker voltage, V_f, as a proportion of the 50Hz fundamental. This objective may be achieved either by reducing the impedance across which V_f is generated, or by altering the components of the currents that generate V_f. It is worthwhile to remember here that V_f may be resolved into many frequency components, with those centred around 8Hz having annoying effects at very low levels.

Once it has been decided to attempt flicker reduction by connection of a device in parallel with a varying load, careful thought must be given both to the characteristics of the load and to the requirements for the shunt-connected compensator.

3.4.1 Shunt Reactive Compensation

The electrical supply to high power installation is generally of such a rating that the Q factor of the equipment is greater than 20. It can easily be shown (Section 3.3.2) that for sinusoidal conditions it is the contribution of the reactive component of the current that dominates in the voltage drop across an impedance $Z = R + jX$ where $X/R \geqslant 20$ (Figure 3.6).

It is for this reason that REACTIVE compensation has been accepted and used for the control of voltage changes due to large fluctuating loads.

Miller[95] provides an excellent reference text on a wide variety of reactive compensation techniques. He and others[43,44,45,46] identify the Thyristor Controlled Reactor (TCR) as being able to offer the performance necessary for arc furnace voltage flicker reduction.

Point on wave control of thyristor firing results in non-continuous inductive currents in each TCR branch (Figure 3.9). Control of the firing angle 'α' thus controls the compensator load on the power system.

When the arc furnace demand is high, often approaching short circuit, the shunt compensator demand is set low. The compensator demand is then set high to compensate for a low furnace demand.

Ideally then, the changes in furnace demand will be inversely matched by the balancing TCR. The magnitude and phase of the current drawn from the supply will then be constant. For the case where the balancing is achieved by an inductive system, the current drawn from the supply will remain constant at the maximum value drawn by the furnace installation, i.e. short circuit. This will be at extremely poor power factor ($\simeq 0.1$), and may therefore require further reactive compensation in the form of fixed capacitor banks at the load.

Such capacitor banks simply shift the mean reactive power demand of the dynamically balanced load nearer to zero, thus lowering the magnitude of current through the supply impedance and increasing the load voltage. In practice the fixed capacitors will have values calculated to create a tuned circuit with existing inductances, to act as harmonic filters.

A circuit tuned to absorb harmonic current components is often necessary, due to the non-continuous form of TCR branch conduction.

Fourier analysis of the TCR branch current waveform shown in Figure 3.9 enables the RMS value of the n^{th} harmonic current component to be calculated[95] as:

$$I_n = \frac{4}{\pi} I_0 \left[\frac{\sin(n+1)\alpha}{2(n+1)} + \frac{\sin(n-1)\alpha}{2(n-1)} - \cos\alpha \left(\frac{\sin n\alpha}{n} \right) \right]$$

Where $I_0 = \frac{V}{X_L}$ and $n = 3,5,7,9.....$

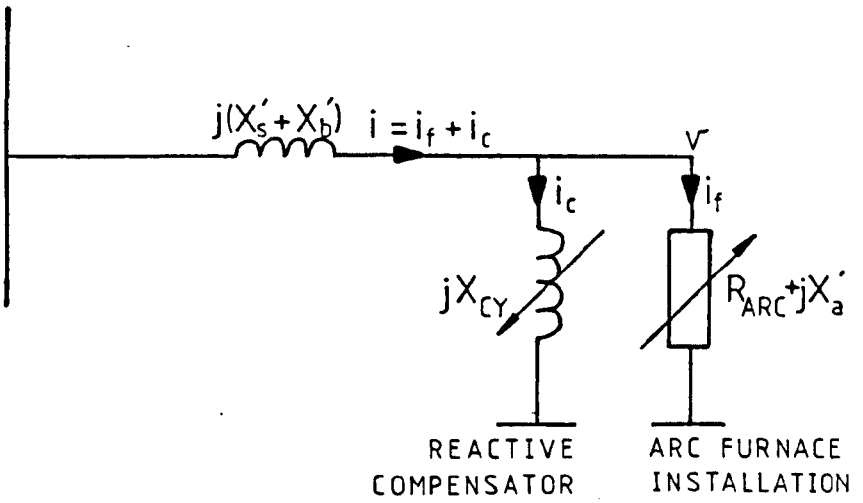


Fig. 3.9(a) : Shunt reactive compensation principle

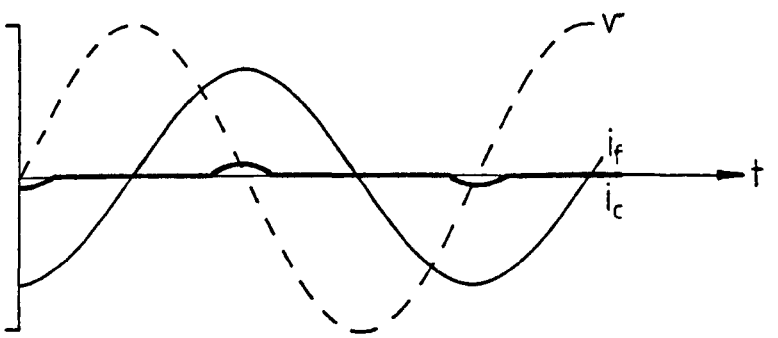


Fig. 3.9(b) : High furnace demand and low compensator demand

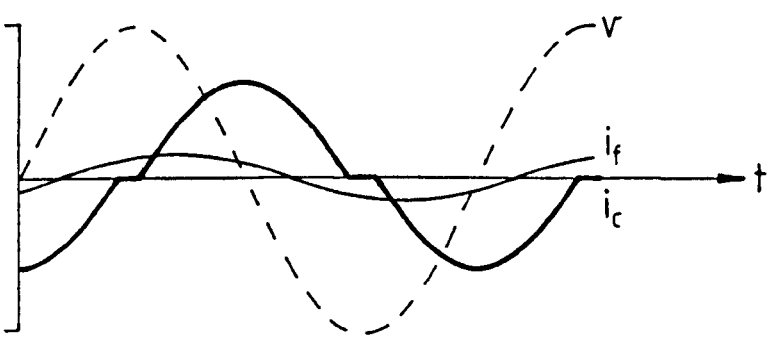


Fig. 3.9(c) : Low furnace demand and high compensator demand

Maximum amplitudes are then 5.05, 2.59, 1.05 percent for 5th, 7th and 11th harmonic currents respectively. The total harmonic content is a maximum of approximately 5 percent, occuring at $\alpha \simeq 20°$.

Several stages of Y-connected capacitor banks may then be used, each rated for a different harmonic frequency[37,96,97,98]. Using a TCR to balance the rapid variations in reactive power demand by the arc furnace then has the advantages of:

(a) Continuous control of compensating currents between zero and maximum values.

(b) Fast variation in demand - changes in the conduction angle may be made every 50Hz half cycle.

3.4.2 The Rating of a Reactive Compensator

Having understood the principle of shunt reactive compensation using a TCR, we must decide the details of its construction - in particular its rating. Any compensator equipment will be connected in parallel with an arc furnace installation to achieve a given flicker 'improvement factor', IMP, defined as:

$$IMP = \left[1 - \frac{\text{Compensated Flicker Voltage}}{\text{Uncompensated Flicker Voltage}}\right] \times 100\%$$

Flicker severity is itself a function of both the system fault level and the furnace installation short circuit power (Part 3.3), and the TCR VAR rating is then proportional to:

(a) The required improvement factor.

(b) The arc furnace installation's short circuit MVA.

(c) The supply system fault level.

Furthermore, compensator performance is inextricably linked to its method of control. TCR rating may be calculated from theory exactly in accordance with (a),(b),(c) above and yet be unable to give any flicker improvement, solely due to its method of phase angle control.

It was decided to investigate the method of control of a three-phase TCR rated adequately for full reactive power compensation. Subsequent refinements in the phase angle control system could then offer the substantial benefit of reduction in TCR rating for a given improvement factor.

The Templeborough arc furnace installation has direct relevance to this project, and will therefore be studied between the two extremes of arc furnace operation: Open circuit to short circuit. If a TCR's operating range extends to both of these conditions, then a control system will have available the resources to match the most onerous fluctuations of the arc furnace load.

Not all electrical parameters are known. We are able to give the exact electrical representation of the furnace supply as far as the furnace transformer, and it is known that the arc is equivalent to a variable resistance[93,99,100], therefore the equivalent circuit of Fig. 3.10(a) is missing only the unknown values of R_u and X_u. R_k and X_k are the lumped known parameters of the furnace installation's supply.

They were given in Section 3.2.1 as:

$$X_s' = 1.2\text{p.c.}$$
$$X_b' = 23.833\text{p.c.} \qquad R_b' = 0.519\text{p.c.}$$
$$X_a' = 89.3\text{p.c.}$$

on 100MVA base, giving a furnace short-circuit level of 87.46MVA.

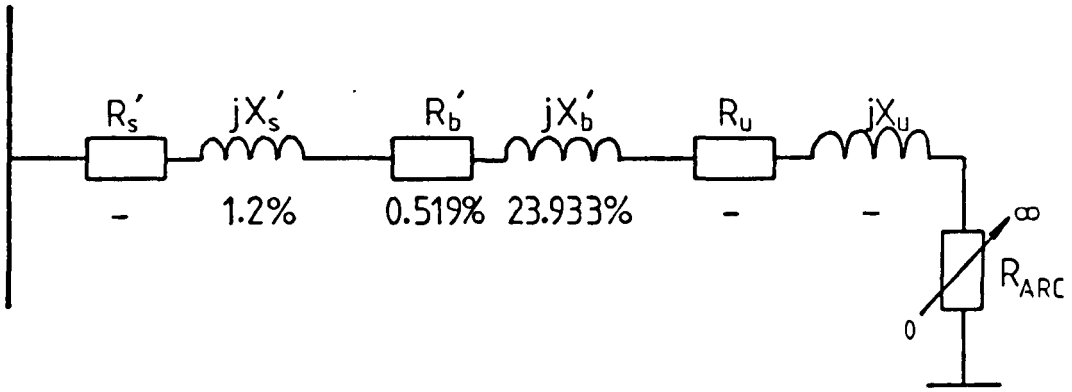


Fig. 3.10(a) : Templeborough supply one line diagram with percentage impedances to 100MVA base

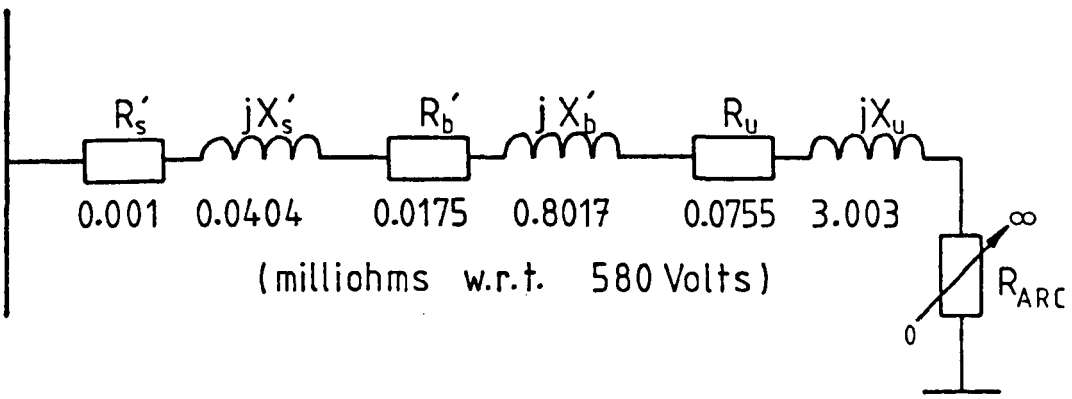


Fig. 3.10(b) : Templeborough supply one line diagram with derived equivalent ohmic impedances

Only values of reactance are used in the short-circuit level calculations[6], since resistive components are generally relatively small and often unknown. An analysis including circuit resistive components, however, will be of great benefit in understanding circuit power factor and other parameters.

Knowing the furnace short-circuit level, S_t, and letting the furnace transformer secondary voltage be V_{LV}, then the arc current has a range of tens of thousands of amps:

For $V_{base} = V_{LV} = 580V$, and $VA_{base} = 100MVA$:

$$Z_{base} = 3.364 \text{milliohms}$$

We know that the X/R ratio of the supply transformer is approximately 45, therefore assume X/R ≃ 40 for the complete supply system to the furnace.

$S_t = 87.46MVA$, and $V_{LV} = 580V$ gives:

$$I_{sc} = 87{,}060 \text{ Amps } \angle 88.6^\circ \text{ lagging}$$

Therefore the total supply impedance will be:

$$Z_{tot} = 3.846 \text{milliohms } \angle 88.6^\circ$$
$$= 0.094 + j3.845 \text{milliohms}$$

The values for X_s', X_b' and R_b' are known and were given above.

Their corresponding ohmic values are:

$$X_s' = 0\ 0404 \text{milliohms}$$
$$X_b' = 0.8017 \text{milliohms} \qquad R_b' = 0.0175 \text{milliohms}$$

then $$X_u = 3.003 \text{milliohms}$$

Let $R_s' = \frac{X_s'}{40} = 0.001 \text{milliohms}$

then $Ru \simeq 0.075 \text{milliohms}$

The equivalent circuit so derived is given as Fig. 3.10(b). This one-line diagram shows per phase values, therefore:

$$\text{VA} = \sqrt{3}\,(580)\,I$$
$$\text{Arc Power} = 3\,I^2\,R_{ARC}$$
$$\text{Supplied Power} = \text{Arc Power} + 3\,I^2\,(R_u + R_b')$$
$$\text{Supplied VAR}_s = 3\,I^2\,(X_b' + X_u)$$
$$\text{Power Factor} = \frac{\sum R}{\sum Z}$$

The quantities are plotted against circuit current in Figure 3.11, and the equivalent 'circle diagram' from the same results is shown in Figure 3.12.

Figure 3.11 shows that maximum power transfer to the arc furnace installation occurs at 61kA, 0.707p.f. and 61MVA. In practice this point is not within the normal operating range[93]. The full load working current for the 56MVA furnace is shown to be at a p.f. of approximately 0.8.

Furnace reactive power swings are:

Open circuit to short circuit = 87MVAR, 1.6 x Furnace Rating
Normal operating range = 35MVAR, 0.63 x Furnace Rating

A survey of published ratings of TCR type shunt compensators installed for arc furnace voltage flicker reduction is summarised in Table 3.1. The range of compensator rating (C) to furnace rating (F), C/F, varies between 1.1 and 0.37. Unfortunately these ratios cannot be correlated with details of the system fault levels, nor with any measured improvement factor, since such information is often excluded from published work.

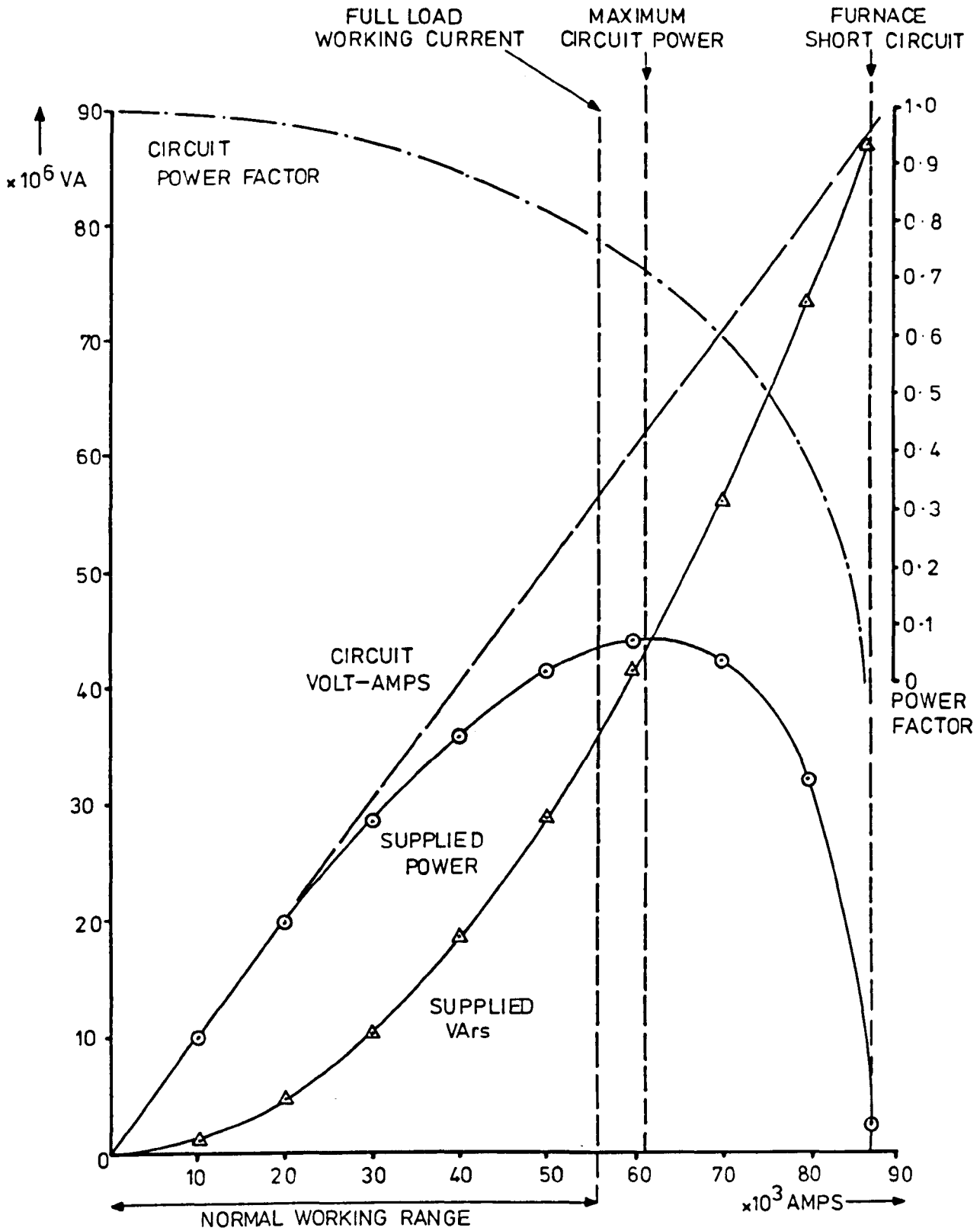


Fig. 3.11 : Arc furnace parameters as a function of current

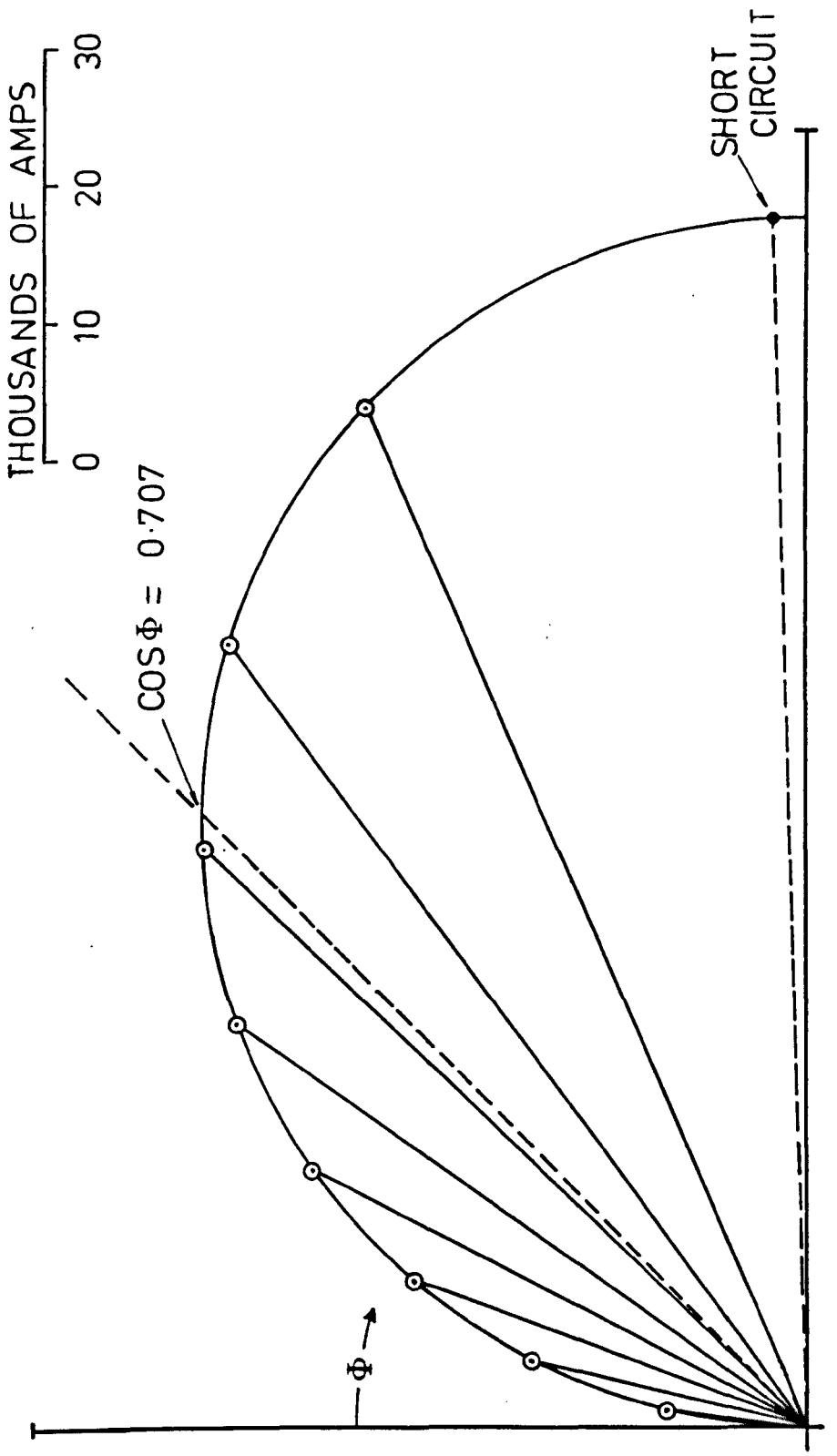


Fig. 3.12 : Arc furnace circle diagram

ITEM	DATE	FURNACE INSTALLATION		REACTIVE COMPENSATOR		MANUFACTURER	REF
		CAPACITY (TONNES)	RATING (MVA)	FIXED MVA	TCR MVA		
1.	1973	50	30	-	18		[43]
2.	1974	30	18	-	20		[43]
3.	1975	50	30	-	25	Nissin	[43]
4.	1976	20 + 50	10 + 36	-	18	Electric	[43]
5.	1976	20 + 20	12 + 12	-	9	Company	[43]
6.	1976	20 + 15 + 15	12 + 6.25 + 6.25	-	12		[43]
7.	1977	30 + 15	-	-	23		[43]
8.	1978	60 + 40 + 20	25 + 25 + 12	36	30	Oy Nokia Ab	[44]
9.	1978	100 + 100	72 + 72	146	120	Mitsubishi	[45]
10.	1978	20	4.6 + 15	14.7	9.5	EDF	[45]
11.	1981	-	65 + 65	-	65 + 65	-	[104]

Table 3.1 : Summary of published details of installed TCR schemes for arc furnace static shunt compensation

Figure 3.11 shows that the reactive power swing over the normal working range of the arc furnace is 0.63 x Furnace MVA rating, and this MVA value was used for the intial TCR compensator study (Section 4.1.1).

3.4.3 Control of Static Shunt Reactive Compensators

The function of the control system, for a compensator incorporating thyristor-switched reactors or capacitors, is simply to control conduction in the compensator limbs by means of point on wave switching. This principle has been used successfully for many years, where closed-loop systems effect control of static compensators for transmission line voltage support[37,38,39,101,102].

The simplest closed-loop system will compare a rectified measured system voltage with same d.c. reference signal. The derived error signal is then used by a proportional control section to determine TCR firing angles[102].

Other feedback parameters, such as currents and reactive power, may be added and used by a more complex firing angle controller[63]. The controller may refer to a pre-set relationship between system admittance and compensator susceptance to set the thyristor firing angles[38,101]. Positive and negative sequence voltages are easily calculated from the three-phase system voltages, and have found use in some systems, where phase imbalance is to be corrected by an overall three-phase controller rather than by three individual systems[38,39].

In any such closed loop control system, the control loop will take a finite time to respond to system changes, and the delay may comprise:

(a) T_D, a pure time delay or 'transport delay' between a control system's 'decision' and the required action.

(b) T_C, the time constant of the control system.

In the context of voltage support for large systems, where compensation may be for widely distributed loads, such time delays rarely cause control difficulties. Indeed the response may be heavily damped deliberately to avoid instability of the large system.

When investigating the response of closed-loop systems, classical control theory[103] enables Laplace transforms to be used to great benefit. In particular, the transfer function of the system will show the response of the output, C, for any input, R.

For a time constant, T_C, $C(t) = \frac{K}{T_C} \exp[-t/T_C]\, R(t)$

the Laplace transform is $C(s) = \frac{K}{1 + sT_C} R(s)$

Where K is the open loop gain of the system.

Adding a pure time delay modifies the transfer function to:

$$\frac{C(t)}{R(t)} = \frac{K}{T_C} \exp[-(t-T_D)/T_C]$$

with Laplace transform:

$$\frac{C(s)}{R(s)} = \frac{K}{1 + sT_C} \exp[-sT_D]$$

This transfer function may then be used to represent TCR compensator feedback control[40,126]. If the input to the control system is an uncompensated reference flicker signal R(t), and the response of the system is the controlled output C(t), then the flicker improvement factor, IMP, may be expressed as:

$$IMP = 1 - \frac{\text{Compensated Flicker Voltage}}{\text{Uncompensated Flicker Voltage}} = 1 - \frac{C(t)}{R(t)}$$

The Laplace transform above then gives:

$$IMP = 1 - \frac{C(s)}{R(s)} = 1 - \frac{K}{1 + sT_C} \exp[-sT_D]$$

in the frequency domain.

The steady state gain and phase of the control system may be found by substituting for $s = j\omega$ in the transfer function, giving:

$$\frac{K}{1 + j\omega T_C} \exp[-j\omega T_D]$$

$$= \frac{K}{1 + \omega^2 T_C^2} (\cos\omega T_D - \omega T_C \sin\omega T_D) - j(\sin\omega T_D + \omega T_C \sin\omega T_D)$$

Ashmole[32,40] shows how the compensator improvement factor varies with frequency for different values of compensator time constant T_C.

T_C and T_D will vary according to the closed loop control scheme used. The 'transport delay', T_D, may be reduced practically to 5 milliseconds for most compensator schemes, but the time constant, T_C, is generally longer. T_C will be affected by filtering, sampling or processing circuitry, and a value of TC ≃ 20 milliseconds would be considered as fast compensator closed loop control.

Given values of T_C and T_D, the gain and phase of the control system's transfer function may be calculated over a range of operating frequencies. Results from such calculations are plotted in polar form in Figure 3.13 with per unit gain and phase angle shown for T_C = 5, 10, 20 milliseconds for fixed T_D = 5 milliseconds. Each characteristic shows that reasonable gain may be obtained with phase delays of up to $\pi/2$ radians. Positive feedback is encountered in the third quadrant.

Most important for flicker frequency compensation is effective attenuation in the 0-30Hz disturbance frequency range. Figure 3.13 shows clearly that true negative feedback is only obtained up to 15Hz for T_C = 20 milliseconds, compared to 28Hz when T_C = 5 milliseconds. The corresponding frequencies at which positive feedback is encountered are 55Hz and 65Hz respectively. System gain at the critical frequency of 8Hz for T_C = 20 milliseconds is only 65p.c. of that given by a system with T_C = 5 milliseconds.

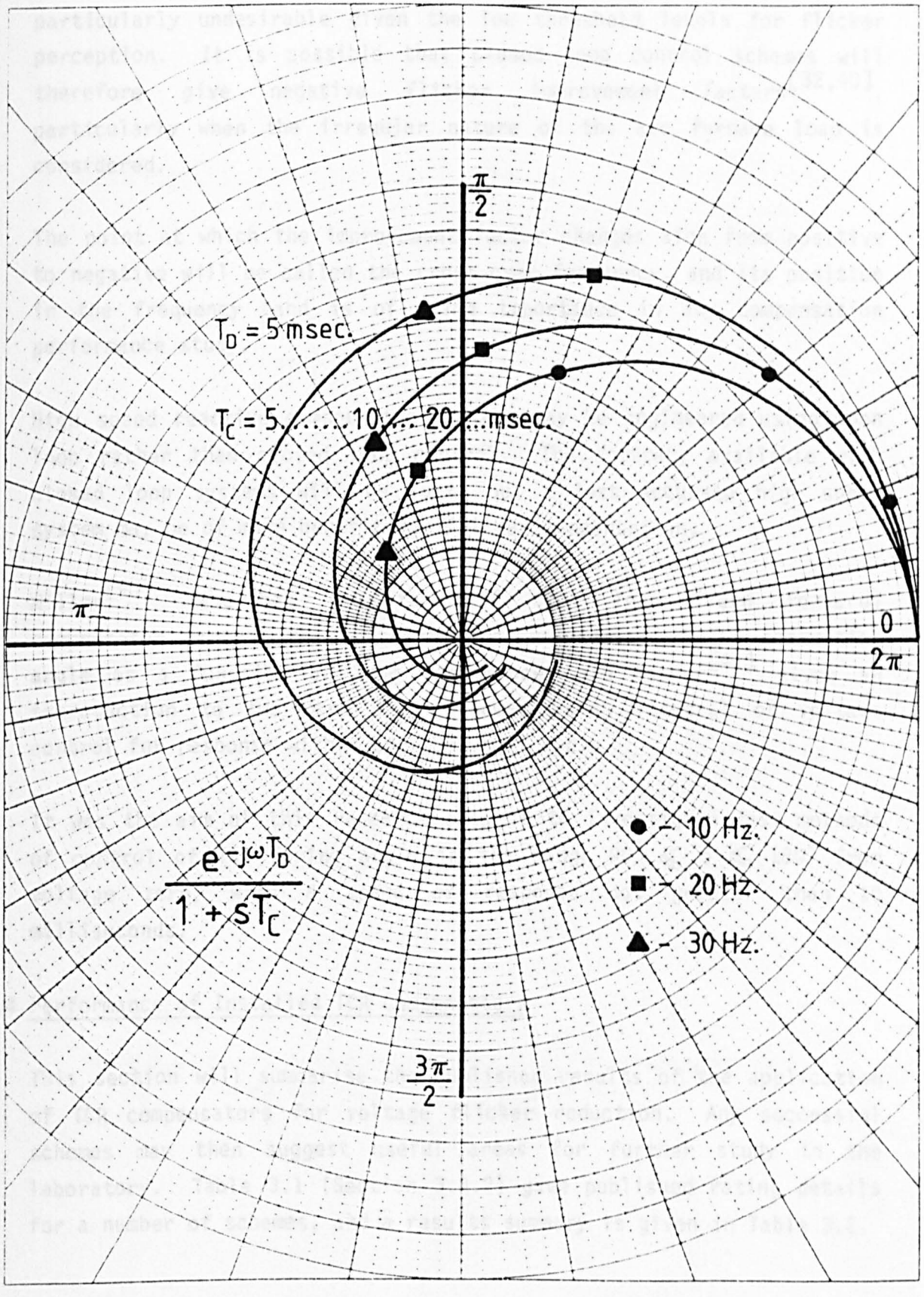


Fig. 3.13 : Polar plot for control system gain and phase

In practice, T_c = 5.0 milliseconds would prove difficult to obtain, and amplification of higher frequencies of distortion are particularly undesirable given the low threshold levels for flicker perception. It is possible that closed loop control schemes will therefore give negative flicker improvement factors[32,40], particularly when the irregular nature of the arc furnace load is considered.

The point at which the improvement factor changes sign from positive to negative will be called the cross-over frequency, and its position in the frequency band is of prime importance in any compensation performance study.

High speed reactive compensator systems may be engineered using open loop rather than closed loop control. The accuracy available with closed loop systems will be lost, but a less accurate high speed system may be of more benefit for flicker compensation.

Miller[95] describes one form of open loop (feed forward) compensator control that requires pre-programming of TCR conduction angle as a function of load admittance, and Cooper[41] gives an introduction to two open loop schemes using integral of voltage control for response within one 50Hz half cycle.

It was the aim of this research project to investigate fast methods of control of TCR firing angle in the range $90^\circ \leqslant a \leqslant 180^\circ$ from voltage zero, with a speed of response not greater than 10 milliseconds.

3.4.4 Performance of Installed TCR Compensators

This section will summarise the published results of the application of TCR compensators for voltage flicker reduction. Any successful schemes may then suggest useful areas for further study in the laboratory. Table 3.1 (Section 3.4.2) gave published rating details for a number of schemes, and a results summary is given in Table 3.2.

Ref. from Table 3.1 and Manufacturing	Control Method	Results	Flicker Measurement Method
1. 2. 3. 4. 5. 6. 7. Nissin Electric Company[43]	TCR thyristor firing when a reference voltage is exceeded by a signal proportional to busbar voltage plus furnace current. 90° phase lag may be incorporated. Claimed TD = 5mSec.	Flicker supression factors between 0.22 and 0.59 for different arc furnace installations. Cross-over frequency = 15Hz.	Both ΔV_{10} flicker-meter and power spectrum analysis of voltage.
8. Oy Nokia Ab.[44]	Open loop; TCR thyristor firing after measurement of VAR within each half cycle. Claimed speed response LT 10msecs.	Power factor improvement from 0.87 to 0.99. Max. RMS voltage fluctuations reduced from 7 percent to 1 percent.	None
9. Mitsubishi[21]	Open loop; TCR thyristor firing after calculation of reactive component of load current and comparison with a preset characteristic for each half cycle.	Frequency independent 'flicker' voltage improvement ratios up to 65 percent. Frequency characteristics show flicker voltage attenuation up to 20Hz.	Custom 'flicker-meter' equipment and Power Spectrum analysis of voltage.
10. EDF[46]	Details not given.	Reduction in Q flicker modulation frequencies. Cross-over frequency at 26Hz.	Power spectrum analysis of system reactive power fluctuations.

Table 3.2 : Summary of published TCR flicker compensation results based on schemes listed in table 3.1

There are schemes offering reasonable evidence of a reduction of the power in flicker modulation frequencies, they use fast open loop control methods measuring both busbar voltage and load current. Multiplication or addition of these parameters is then used for comparison with a pre-set characteristic or level[43,45].

This process is restricted to each half cycle, and thus speeds of response between 5 milliseconds and 10 milliseconds are claimed.

The highest cross-over frequency evident is at approximately 20Hz[45], but none of the schemes studied use an internationally recognised flicker meter to obtain an improvement factor.

CHAPTER FOUR

A SIX-PULSE THYRISTOR-CONTROLLED REACTOR

4.1 THE LABORATORY MODEL THYRISTOR CONTROLLED REACTOR

Section 3.4.2 gave a VA rating for a shunt reactive compensator to suit the laboratory arc furnace model. Such a small scale model will have inherent differences in performance from any full size compensator, and these differences should be understood.

The main advantage of a small scale model is flexibility at low cost, and a major objective of this research project was to allow many different control methods to be studied for a given compensator arrangement. The arrangement of the reactances and thyristor switch circuits is given below, with a brief study of the principles of variable phase inductive conduction.

4.1.1 Modelling Requirements

Full scale Thyristor Controlled Reactors (TCRs) presently have three-phase ratings up to 120MVA[45], and current thyristor technology allows direct connection of thyristor switch assemblies to 33kV[44,45]. In such equipment series voltage sharing is necessary, and parallel current sharing with built-in redundancy is operationally desirable. For modelling purposes these switch assemblies may be represented by a single low cost thyristor of a suitable rating, that has the required turn-on and turn-off characteristics.

The rating of the uncontrolled three-phase shunt reactor shown in Figure 4.1 is simply:

$$C = \frac{3V_l^2}{\omega L_c} \text{ VAR}$$

Figure 4.2 shows how the compensator rating, C, varies with L_c for a 175V, 50Hz system. ~~Also shown are the equivalent reactive power swings of the arc furnace model.~~

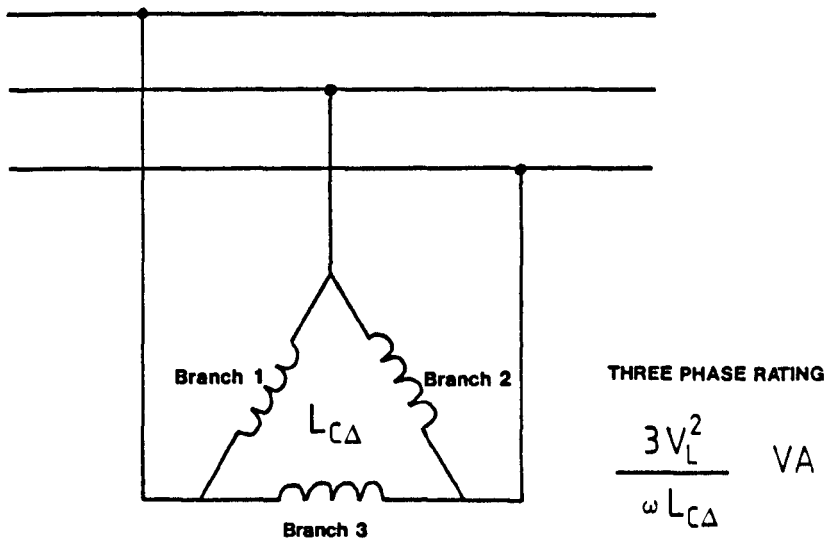


Fig. 4.1 : A fixed delta-connected shunt reactive compensator

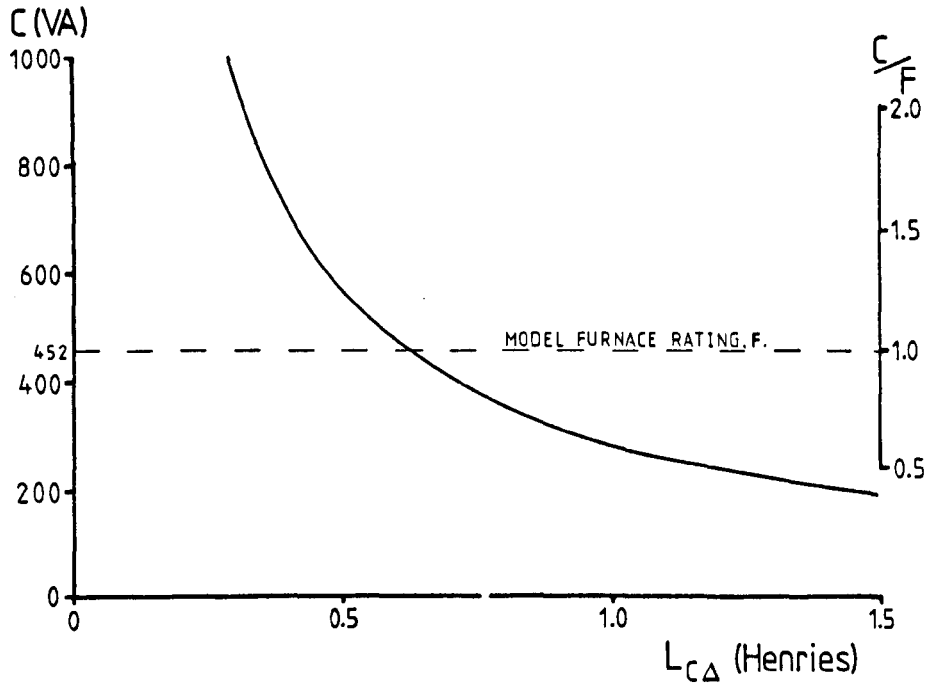


Fig. 4.2 : Compensator 3-phase rating as a function of branch inductance

The reactive power swings in the normal working range of the arc furnace model can be met by a compensator rating, C, of 0.63 times the model furnace rating, F, of 452VA (Section 3.4.2).

A coil having 1.0 Henry of inductance gives a compensator rating, C, of 286.5VA and then C/F = 0.63.

The coils used in the compensator branches were specially wound in copper strip to give an X/R ratio high with respect to their operating VA. An adjustable air gap between C-cores was designed to avoid saturation of the laminated iron cores, and facilitate changing of inductance values using an adjustable clamping system.

The impedances in the compensator branches were then:

Branch 1, $Z_1 = (0.70 + j333.01)$
Branch 2, $Z_2 = (0.69 + j333.32)$
Branch 3, $Z_3 = (0.70 + j324.84)$

The high X/R ratio of 475 minimises any resistive losses in the compensator, and the current waveform will follow that predicted by the theory for pure inductances.

The voltage across each branch is $v = V\sin\omega t$

where $V_{RMS} = 175$ volts and $V = 175\sqrt{2}$

$$\frac{di}{dt} = \frac{v}{L}$$

hence, for symmetrical current flow $\quad i = -\frac{V}{\omega L}\cos\omega t$

i.e. $\quad i = -I\cos\omega t$

where $I_{RMS} = \frac{175}{\omega L}$ and $I = \frac{175}{\omega L}\sqrt{2}$

If conduction is delayed by some angle 'α' from the point of uncontrolled current zero crossing, which corresponds to the symmetrical voltage peak, then the current waveform becomes non-sinusoidal as shown in Figure 4.3. (The voltage waveform shown is for reference only, and all amplitudes are normalised with respect to a sinusoidal peak value of 1.0).

The effects of such a conduction pattern with increasing α are:

(a) Decreasing I_{RMS}.

(b) Decreasing peak current, I.

(c) Increasing harmonic components.

(d) Decreasing $\frac{di}{dt}$ at the beginning of the conduction period.

The equation of the current waveform can be found by considering one half cycle (Figure 4.4). The constant term $I_0 \sin\alpha$ needs to be subtracted during conduction from the sinusoidal value.

Hence, $i = (I_0 \sin\omega t - I_0 \sin\alpha)$ for $\alpha < \omega t < (\pi - \alpha)$

Whence, $I_{RMS} = \sqrt{\frac{1}{T}\int_0^{\pi} (I_0 \sin\omega t - I_0 \sin\alpha)^2 \, dt}$ for $T = \pi/\omega$

$$= I_0 \sqrt{\frac{2}{\pi}\left[\left(\frac{\pi}{2} - \alpha\right)\left(\frac{1}{2} + \sin^2\alpha\right) - \frac{3\sin 2\alpha}{4}\right]}$$

Also, $I = I_0 (1 - \sin\alpha)$ for $0 \leqslant \alpha \leqslant \frac{\pi}{2}$

And, $\left.\frac{di}{dt}\right|_{\alpha} = \frac{V\cos\alpha}{L}$ for $0 \leqslant \alpha \leqslant \pi/2$

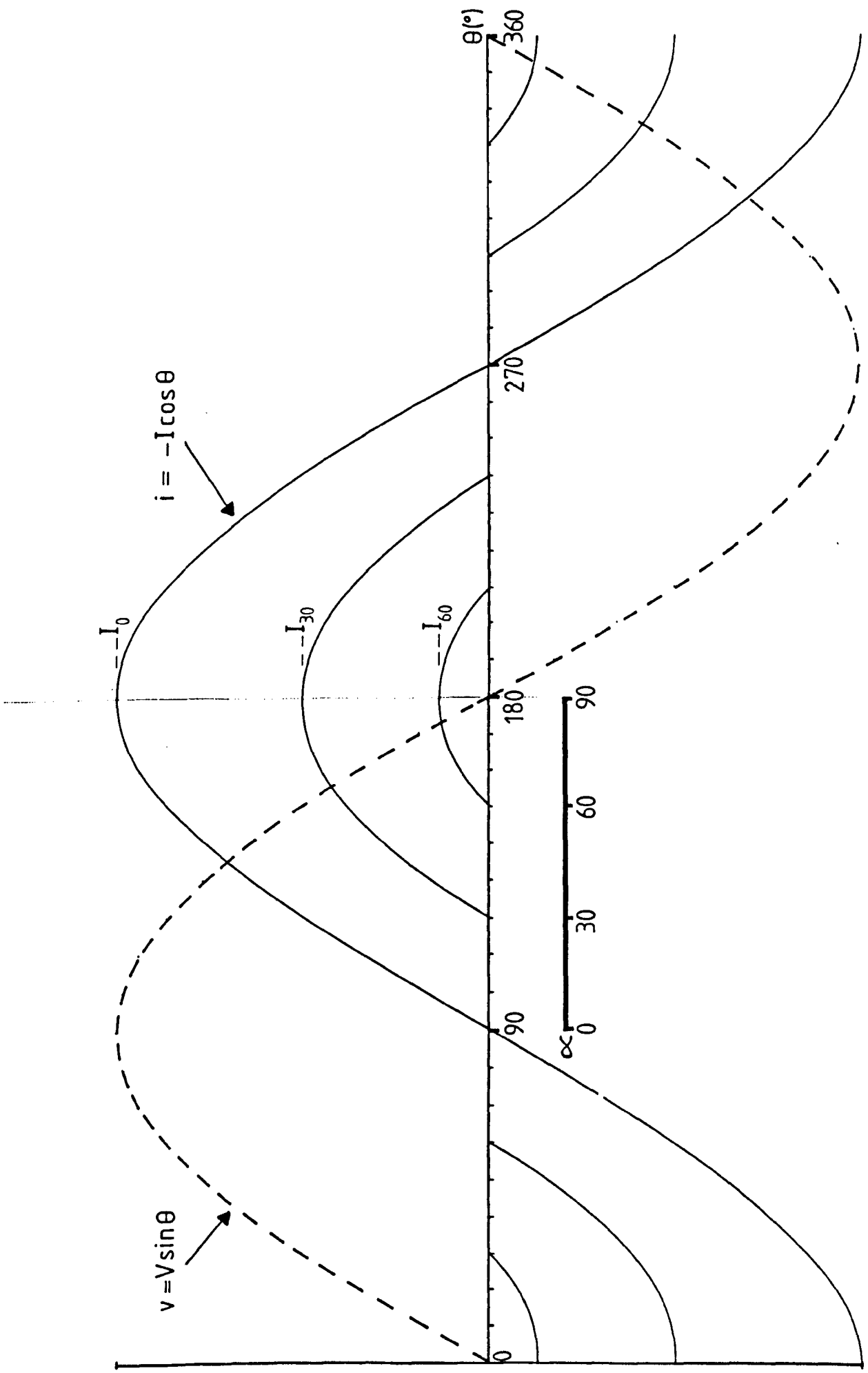
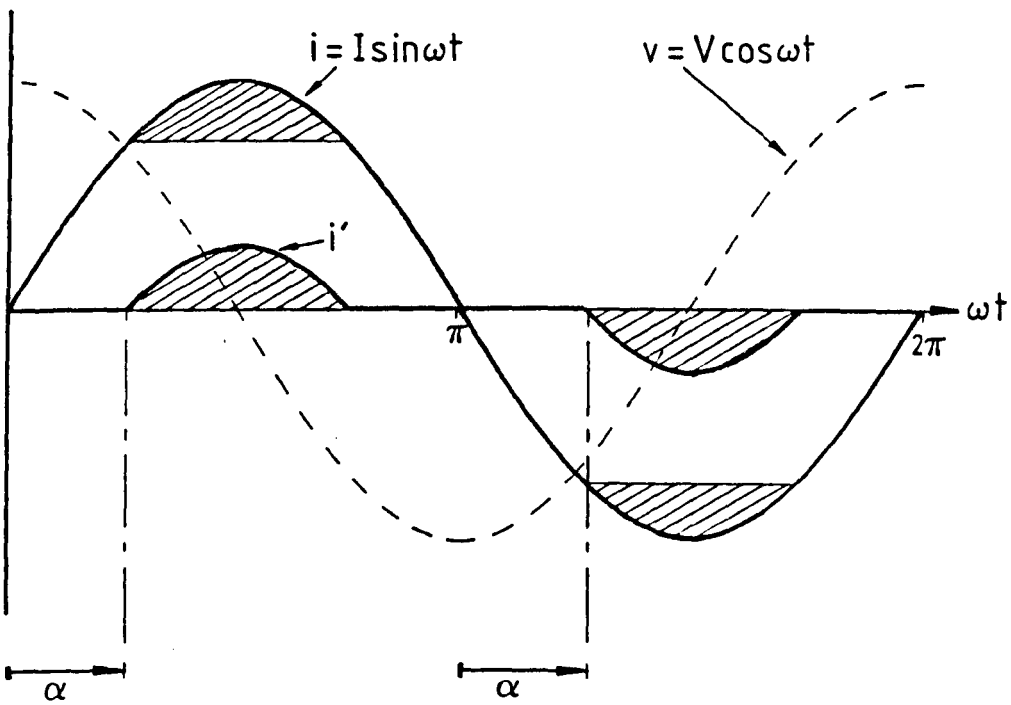


Fig. 4.3 : Conduction patterns resulting from phase angle control of inductive current



$i' = 0$ for $0 \leqslant \omega t \leqslant \alpha$

& $\pi - \alpha \leqslant \omega t \leqslant \pi + \alpha$

& $2\pi - \alpha \leqslant \omega t \leqslant 2\pi$

$i' = (I\sin\omega t - I\sin\omega t)$ for $\alpha < \omega t < \pi - \alpha$

& $\pi + \alpha < \omega t < 2\pi - \alpha$

Fig. 4.4 : Firing angle 'α'

Figure 4.5 shows I_{RMS} for $0 \leqslant \alpha \leqslant 90^{\circ}$ normalised with respect to I_0.

Figure 4.6 shows the variation of peak current I, normalised with respect to I_0, for $0 \leqslant \alpha \leqslant 90^{\circ}$.

Section 3.4.1 briefly described the components of current occurring at harmonic frequencies when the current waveform is non-continuous, as shown in FIgure 4.4. Such harmonic components will, of course, be generated by a laboratory TCR model. It was decided initially not to apply shunt-connected capacitors to the laboratory model. Harmonic current generation would then be studied as a separate exercise, and suitable capacitors connected at a later stage for the dual purpose of harmonic filtering and power factor correction.

di/dt at the point of start of conduction is of interest because thyristors are to be the devices controlling conduction. Their turn-on characteristics are not negligible, and it must be established that anti-parallel connection of thyristors in each compensator branch allows continuous control of the current in each branch. Figure 4.7 gives the notation used for references to the compensator Δ-connected components.

For symmetrical conduction about the voltage zero point it is necessary for the branch current to have reached the thyristor latching current, i_{TL} before the voltage zero.

Conduction will then continue until the current falls below the thyristor holding current, i_{TH} (Figure 4.8). Thus the line voltage, the branch inductance and the thyristor characteristics possibly present restrictions on the maximum value of α that may be used in practice.

Figure 4.9 gives I for values of α near to the voltage zero crossing point for $V_2 = 175V$ and $L_c = 1.0H$.

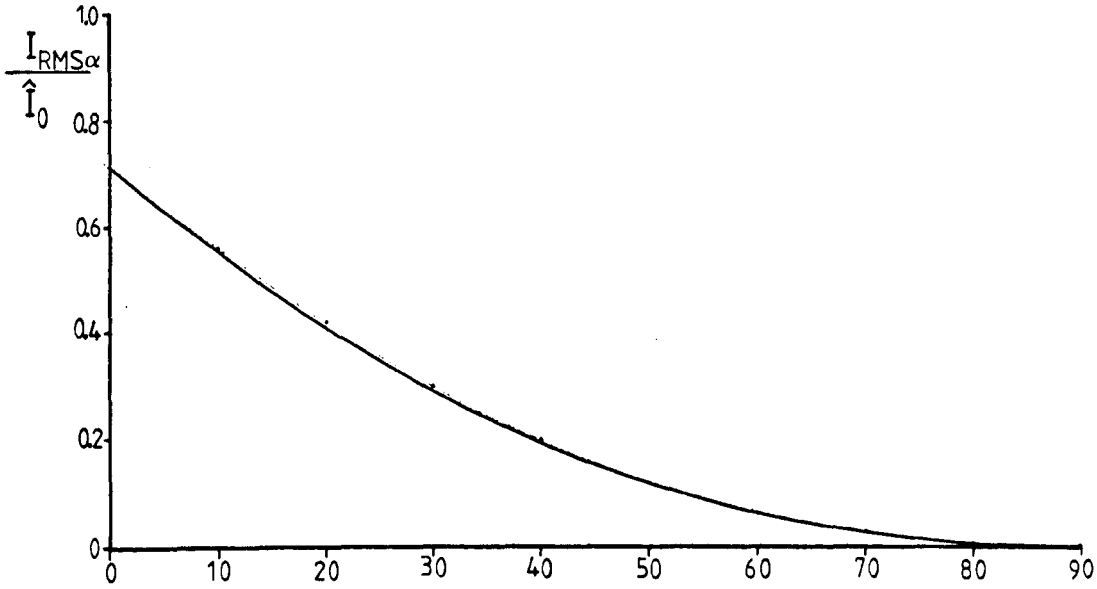


Fig. 4.5 : Variation of RMS current as a function of 'α'

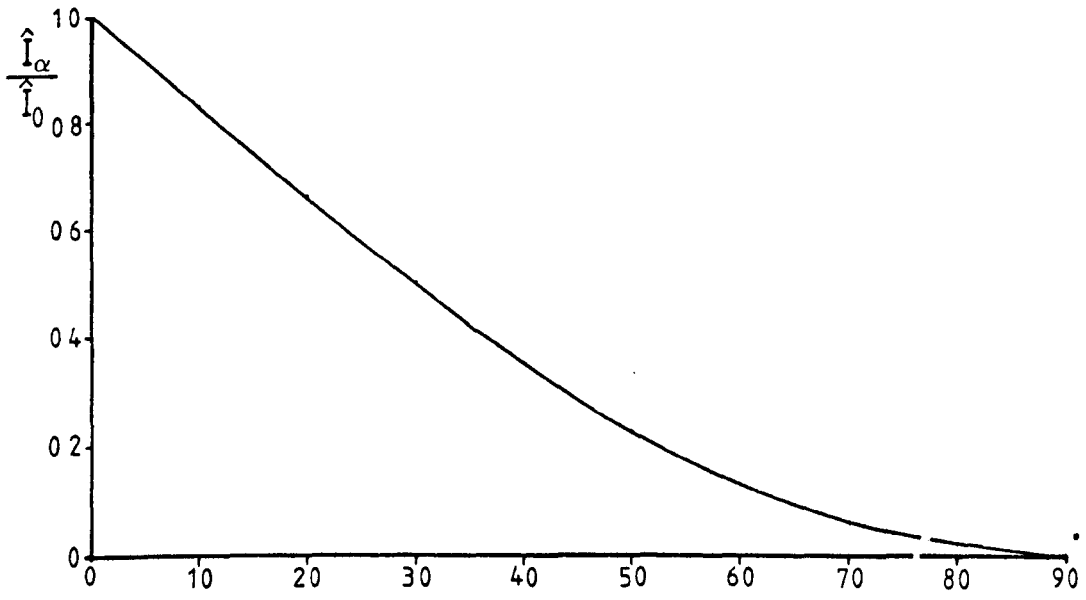


Fig. 4.6 : Variation of peak current as a function of 'α'

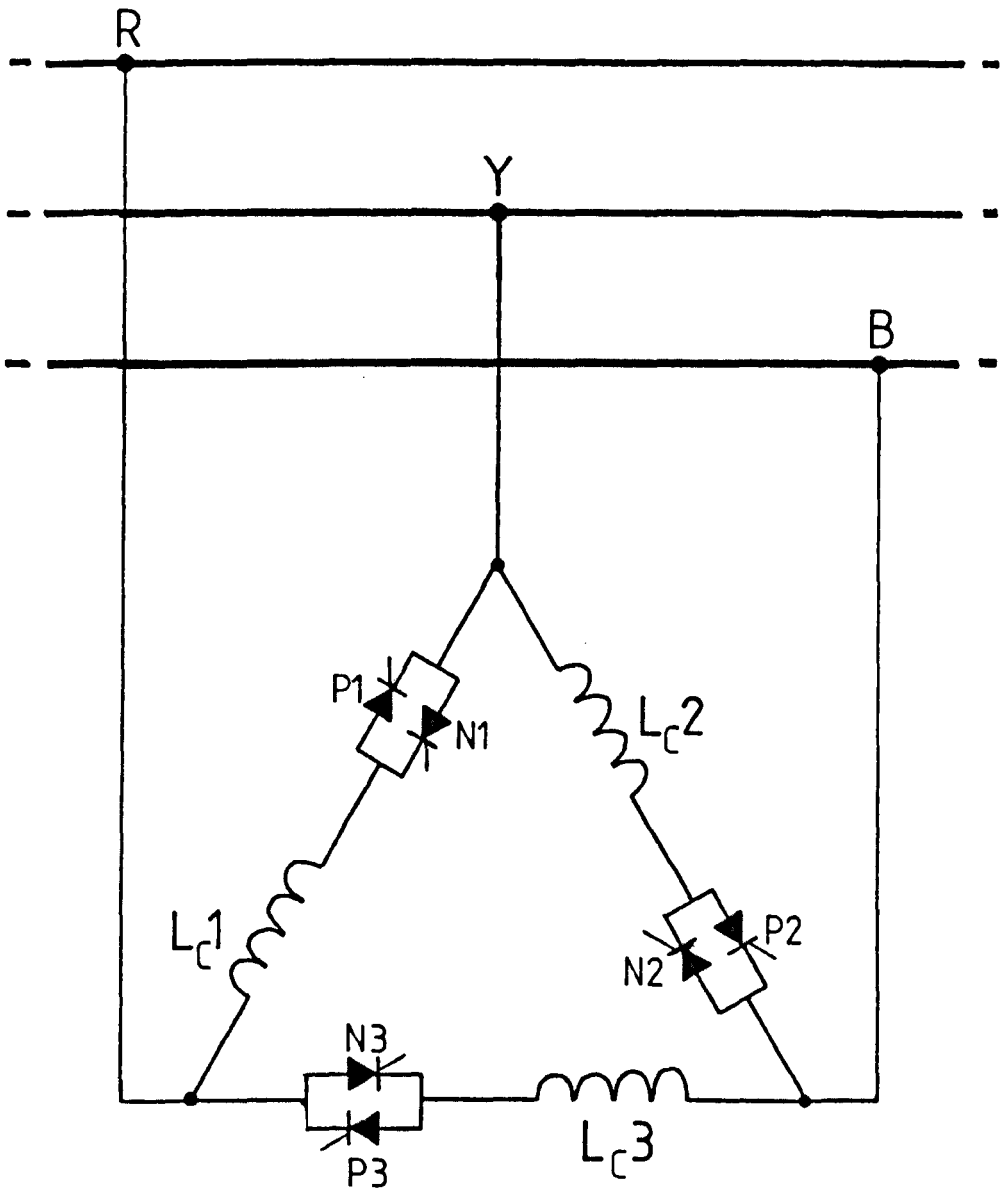


Fig. 4.7 : Laboratory 6-pulse TCR arrangement

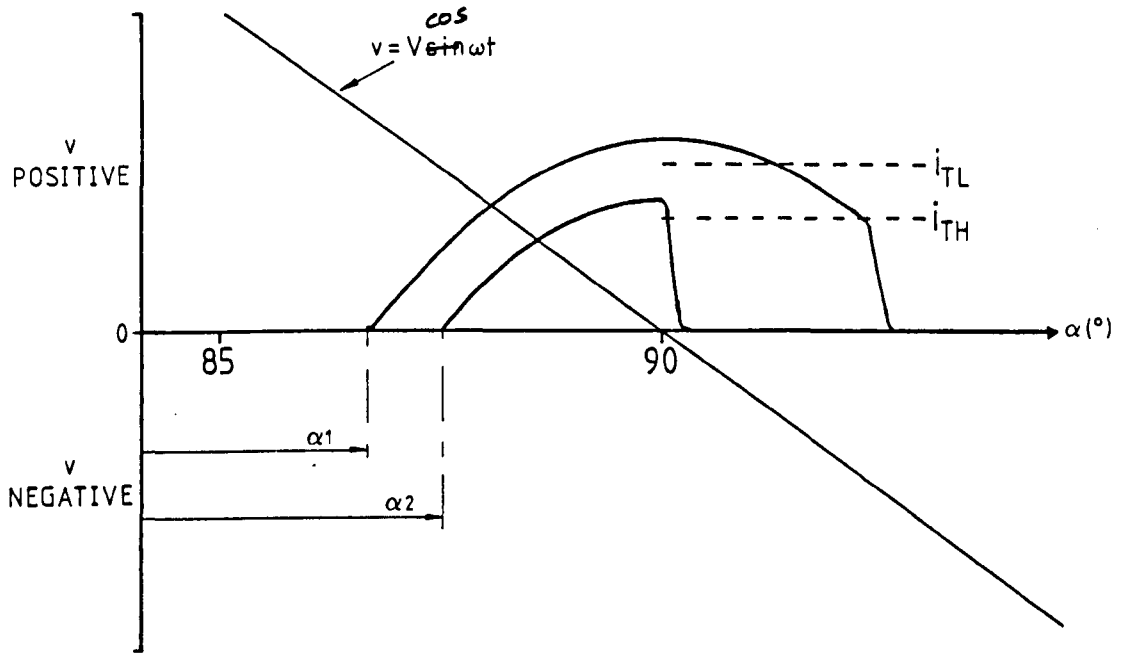


Fig. 4.8 : Thyristor conduction near to voltage zero

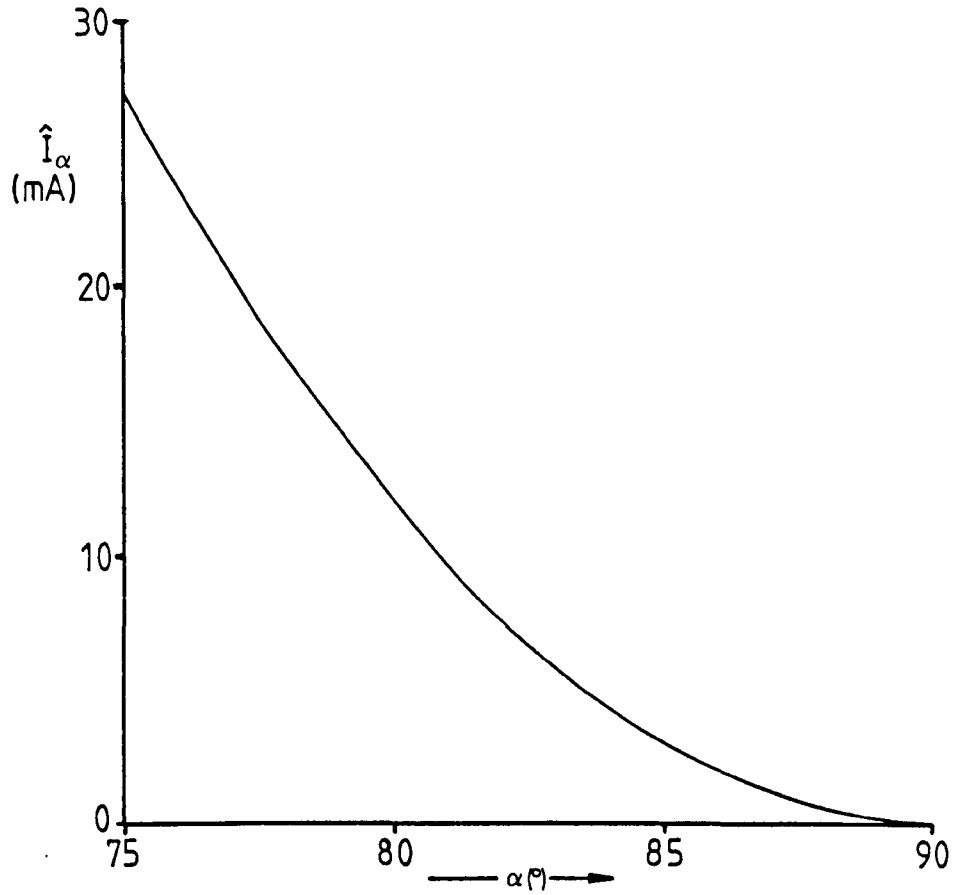


Fig. 4.9 : Peak inductive current for 'α' near to 90°

The thyristors used in the early models were Mullard BT 152-400 and intermittent firing late in the half cycle was eventually traced to the high values of:

$$\text{and} \quad \begin{matrix} i_{TL} < 80 \text{ mA} \\ i_{TH} < 60 \text{ mA} \end{matrix} \quad [105]$$

$I = 80$ mA is only reached for $\alpha < 64^\circ$

The thyristor used in all later studies was the Mullard BTX 18-500 having:

$$\text{and} \quad \begin{matrix} i_{TL} < 10 \text{ mA} \\ i_{TH} < 5 \text{ mA} \end{matrix} \quad [106]$$

With the compensator branch inductance, L_C, of 1.0 Henry the confidence limit for firing is $\alpha \simeq 82.52^\circ$. In practice intermittent firing was found to occur at approximately $\alpha = 86^\circ$.

4.1.2 Control Requirements

Section 3.4.3 identified the general control requirements for different types of shunt reactive compensator. The particular system for controlling a 6-pulse TCR was required to have an equivalent delay in control response of less than 10 milliseconds. Cooper and Hussayni[41] studied practicable TCR control methods and highlighted the advantages of 'Integral of Voltage' control methods whilst commenting on the inadequacy of systems which restricted thyristor firing to $60^\circ \leqslant \alpha \leqslant 90^\circ$.

It was decided at an early stage that an investigation of integral of voltage control should be included in this research project, with the possibility of studying TCR response times shorter than those achieved elsewhere.

Implementing control schemes using a digital processor offered definite advantages:

(i) Ease of changing the control algorithm.

(ii) Standard compensator hardware, including all signal conditioning circuits.

(iii) The possibility of adaptive or 'intelligent' control.

(iv) Simple inclusion of a data logging facility.

Digital sampling of the analogue system variables introduces two possible major sources of error[107]:

(a) Quantisation noise.

(b) Aliasing distortion.

The former arises from the discretisation process employed by all analogue-to-digital converters and occurs when the analogue quantity does not exactly correspond to one of the 'N' defined levels within the span of the device.

Aliasing distortion will arise when the sampling rate is too low, and higher frequency components in the sampled signal corrupt the information that can reliably be recovered from the sampling process.

The Nyquist Frequency, F_N, is the sampling frequency necessary to recover all of the information in a continuous signal with frequency components below the frequency f_{MAX},

Where $$F_N = 2\, f_{MAX}$$

The highest frequency component able to be reconstructed from the CEGB recordings by the arc furnace model is then half the sampling frequency, F_{SM}.

$$f_{MAX} = F_{SM}/2 = \frac{1}{2}\left[\frac{1}{800\ 10^{-6}}\right] = 625\text{Hz}$$

The spline interpolation process (Section 2.3.2 and Appendix C) will introduce higher spurious frequency components up to

$$f'_{MAX} = 4\ F_{SM} = 5000\text{Hz}$$

but, these will be attenuated by the low-pass filters in the power amplifier input circuits.

The TCR data sampling frequency, F_{sc}, should then be:

$$F_{sc} \geqslant 1250\text{Hz or } \Delta t \leqslant 800 \text{ microseconds}$$

The control system should perform a 'real time' process, therefore the calculation of whether thyristor firing is required or not must be completed within this time period, before the next sample. It follows that if one processor is controlling all three of the compensator branches, it is required to perform three times as many calculations as each of three separate processors each dedicated to the operation of one branch.

The structure of the Intel 8088 processor made it suitable for its application as an independent controller for each compensator branch (Figure 4.10(a)) and for the later development of a supervisory system whereby each of the three processors would be controlled from a central processor via interrupts and a common bus structure. (Figure 4.10(b)).

Both arrangements offered advantages in processing speed over other microprocessors and minicomputers, and the Intel 8088 was used in the form of the SDK-88 microcomputer[108].

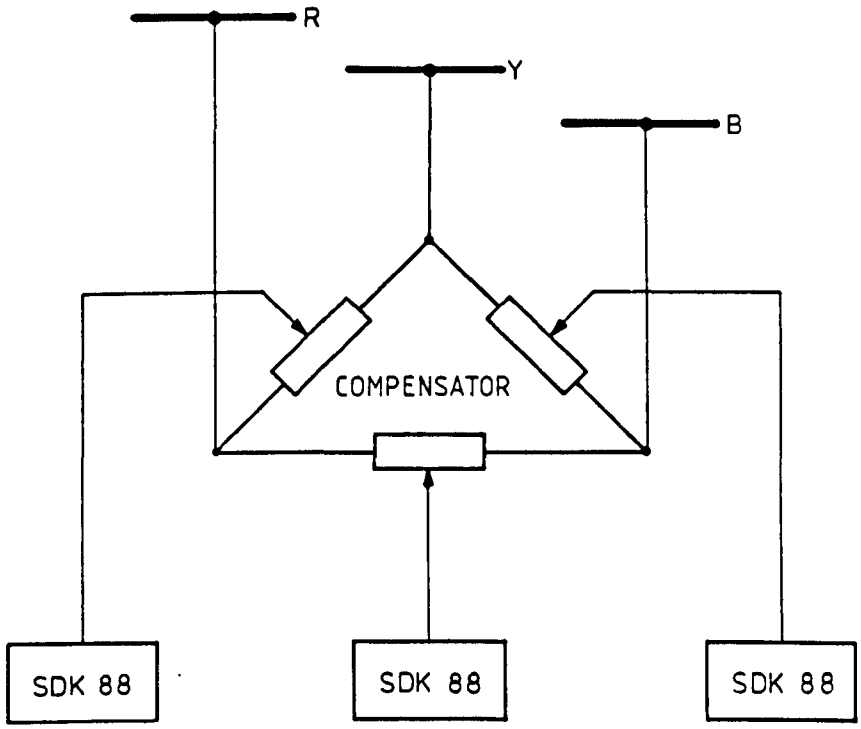


Fig. 4.10(a) : Independant phase control of compensator branches

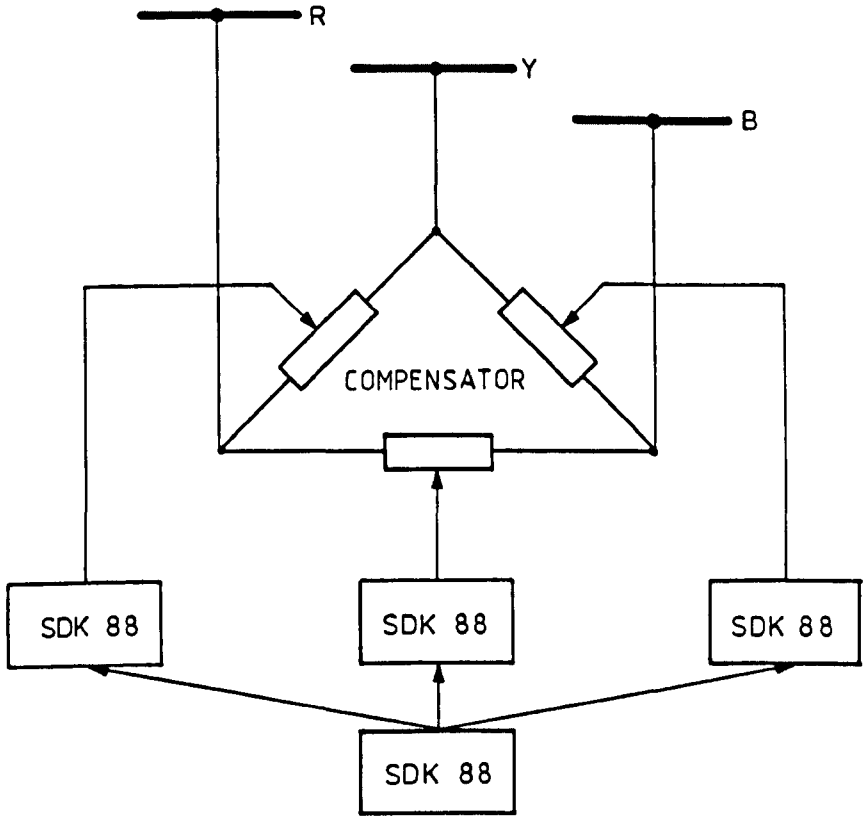


Fig. 4.10(b) : Development to supervisory control

4.2 MICROPROCESSOR CONTROL

Three separate SDK-88 microcomputer systems were installed in the laboratory for the control of the 6-pulse TCR. Each system contained rack-mounted analogue to digital converters fed from identical signal conditioning circuits, for measurement of the three-phase system parameters.

Control programs could be written locally using a ROM-resident monitor and keyboard routine, or remotely using a high level development system in Liverpool University's Microprocessor Laboratory.

Local program control was used for fault finding and the study of program operation. Variables within the program machine code could be adjusted for the control of the individual compensator branches.

4.2.1 System Operation

A Video Display Unit (VDU) and keyboard was sited adjacent to the laboratory equipment allowing individual control of each SDK-88 via the ROM-resident monitor routine. This could also be connected to act as a remote terminal of a Tektronix 8650 Multi-User System Development Unit (MUSDU)[110]. The MUSDU supported file storage under the TNIX operating system and allowed high level language programs to be compiled and linked with assembler language programs. The final machine code could be stored in a file, ready to be downloaded from the MUSDU to the SDK-88 RAM at any time.

Figure 4.11 illustrates the system operating principles. In practice the high-level PASCAL programming language was used for 'supervisory' functions, such as text manipulation and program flow control apart from the compensator control algorithm. The control algorithm was written in Intel ASM-86 Assembler language for increased speed and simpler fault-finding.

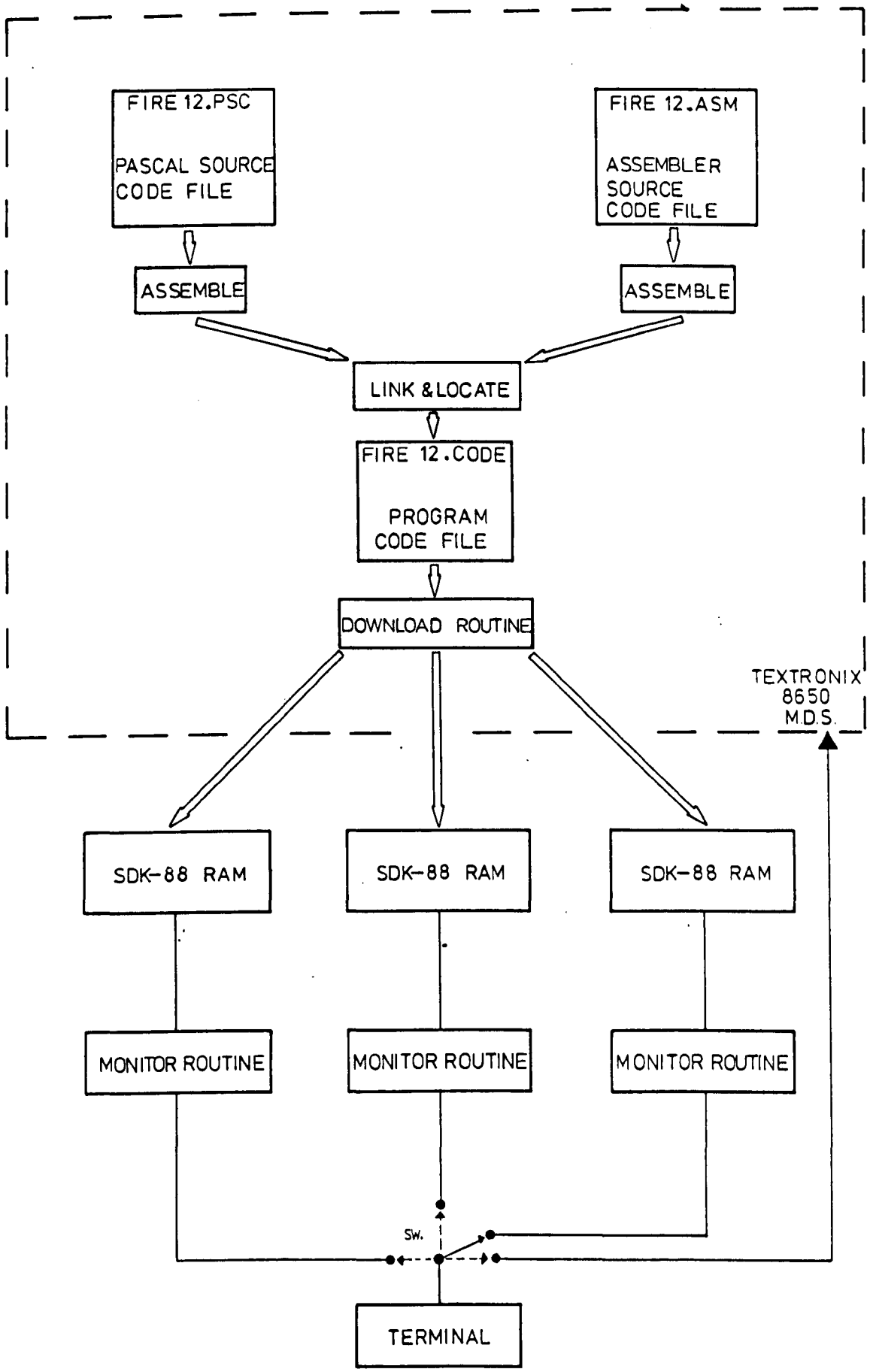


Fig. 4.11 : SDK-88 microprocessor programming arrangements

4.2.2 Sampling

Each of the three SDK-88s used the signal conditioning circuit shown in Figure 4.12 to feed the sample and hold circuit and analogue to digital converter (ADC) shown in Figure 4.13. The logic timing diagram in Figure 4.14 illustrates the sequence of events required to get data on to the Intel 8088 data bus.

From the program environment, a data sample is initiated by an OUT DX instruction, where DX is the data register containing the ADC address. After time has been allowed for the sampling process the digital word may be read to the accumulator, AL, using the IN DX instruction.

Typical instruction times for the 8088 processor with 4.9MHz clock are less than 10 microseconds[108,109], therefore some delay needed to be incorporated between the OUT DX and IN DX instructions to allow the 12 microseconds ADC conversion[111].

For the ADC located at address a F800 the assembler code required is then:

```
MOV DX, @ 0F800H    ;    Load address of ADC
OUT DX, AX          ;    Initiate conversion
MOV CL, @ 0FH       ;    Conversion -
SHR CL, CL          ;    delay
XOR AH, AH          ;    Set accumulator word to zero
IN AL, DX           ;    Input sample to accumulator low
                         byte
```

The time between successive samples will be dictated by the amount of code required by the control algorithm. N-bit sampling of the model supply voltage gives 2^N possible quantisation levels, and therefore a maximum signal to noise ratio of:

$$20 \log_{10} \left[\frac{1}{2^N} \right] \text{ dB} = -6N \text{ dB}$$

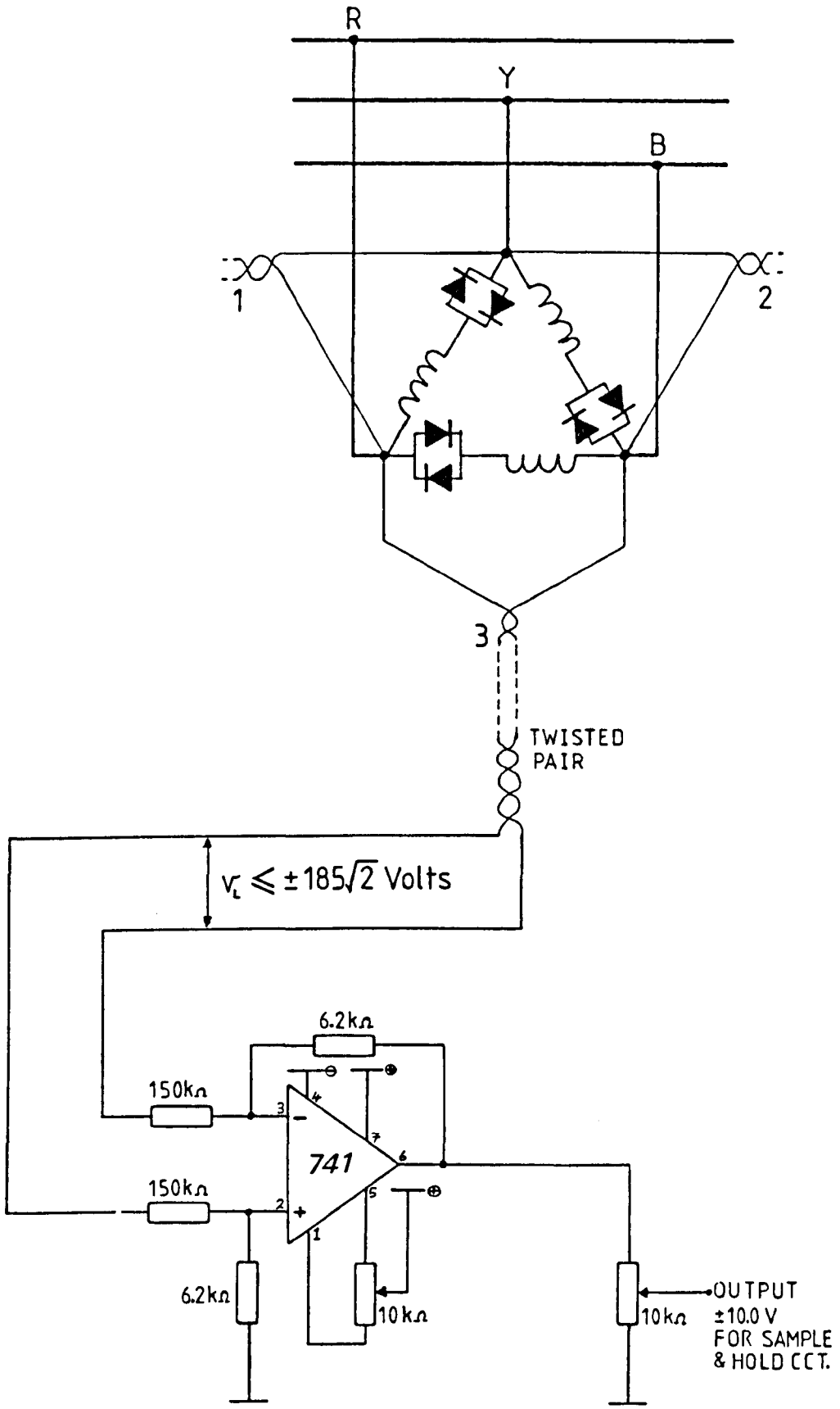


Fig. 4.12 : Signal conditioning circuit for voltage measurement

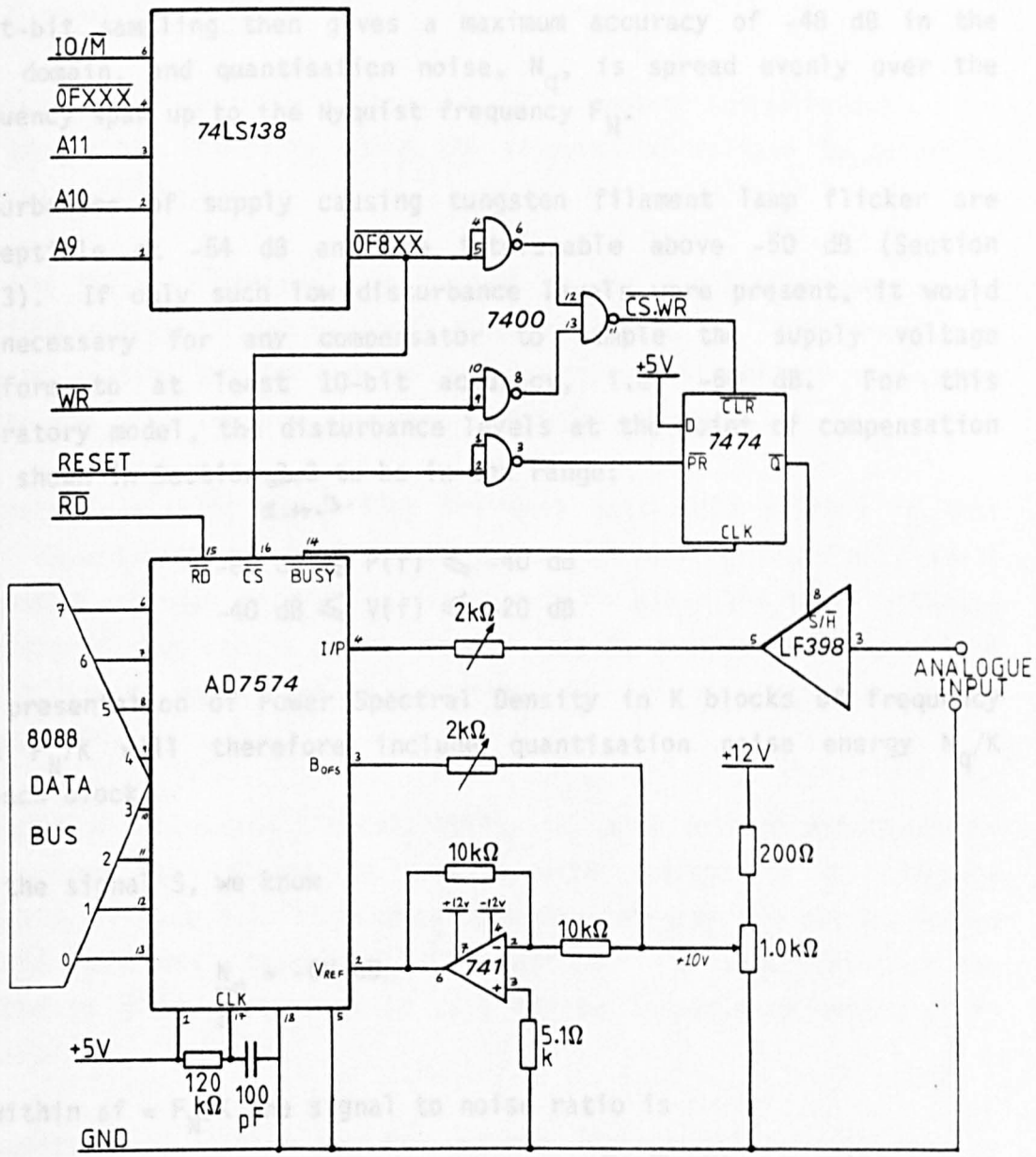


Fig. 4.13 : Sample and hold circuit for voltage measurement

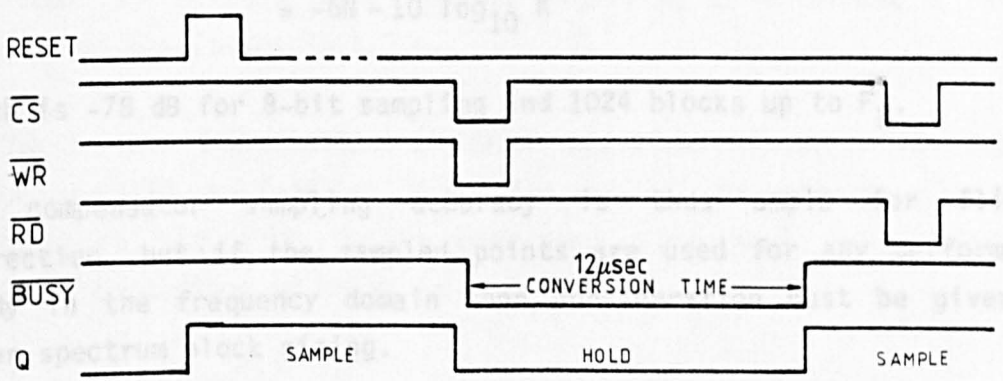


Fig. 4.14 : Logic timing diagram for sample and hold circuit

Eight-bit sampling then gives a maximum accuracy of -48 dB in the time domain, and quantisation noise, N_q, is spread evenly over the frequency span up to the Nyquist frequency F_N.

Disturbances of supply causing tungsten filament lamp flicker are perceptible at -54 dB and are intolerable above -50 dB (Section 3.1.3). If only such low disturbance levels were present, it would be necessary for any compensator to sample the supply voltage waveform to at least 10-bit accuracy, i.e. -60 dB. For this laboratory model, the disturbance levels at the point of compensation were shown in Section ~~3.3~~ 2.4.3. to be in the range:

$$-80 \text{ dB} \leqslant P(f) \leqslant -40 \text{ dB}$$

then

$$-40 \text{ dB} \leqslant V(f) \leqslant -20 \text{ dB}$$

The presentation of Power Spectral Density in K blocks of frequency span F_N/K will therefore include quantisation noise energy N_q/K in each block.

For the signal S, we know

$$\frac{N_q}{S} = -6N \text{ dB}$$

So within $\Delta f = F_N/K$ the signal to noise ratio is

$$10 \log_{10} \frac{N_q}{KS} = 10 \log_{10} \frac{N_q}{S} - 10 \log_{10} K$$

$$= -6N - 10 \log_{10} K$$

which is -78 dB for 8-bit sampling and 1024 blocks up to F_N.

The compensator sampling accuracy is thus ample for flicker correction, but if the sampled points are used for any performance study in the frequency domain then consideration must be given to power spectrum block sizing.

4.2.3 The Control Algorithm

Section 4.1.2 briefly discussed TCR control requirements, and introduced the method of using the integral of voltage to determine thyristor firing angles.

V_f, the 'flicker voltage', is evident as the modulation envelope of the 50Hz supply voltage waveform (Figures 2.3, 3.1). The severity of this modulation may be reduced by attempting to minimise variations of the RMS value of each half-cycle of supply voltage.

Evaluating $v^2(t)dt$ or $v(t)dt$ for each half-cycle suffers in that small departures in v(t) from the sinusoidal will produce only small percentage changes in the integral sum. An algorithm that initiates thyristor firing when a given integral sum is reached would thus lack sensitivity to small voltage variations if the full integral were to be employed.

A method of increasing the sensitivity to small voltage variations is to perform the integration process with respect to a reference sinusoid. Figure 4.15 illustrates how the integral sum may be formed using a reference sinusoid $v_R(\omega t) = R\sin\omega t$. The sensitivity of the process to given variations in v(t) may be lessened by making $|V-R|$ larger.

The undistorted voltage waveform $v(\omega t) = V\sin\omega t$ may be disturbed by additional components $v_f(\omega t)$. Figures 4.15(a) and (b) indicate how the point in the half cycle at which a given integral sum is reached will vary for $v_f(\omega t)dt$ negative and positive respectively. This variation may be used by a control algorithm to determine a firing angle α for thyristors in a TCR.

Turning on the TCR applies a sudden additional load to the supply system and the voltage at the point of TCR connection will fall accordingly. It will remain depressed throughout the period of thyristor conduction as shown in Figure 4.16.

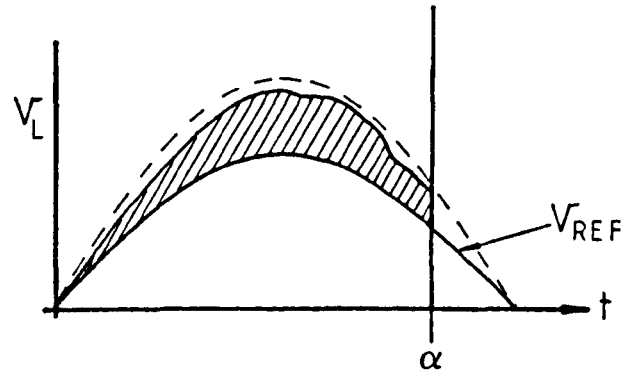


Fig. 4.15(a) : Integral of voltage difference - late firing

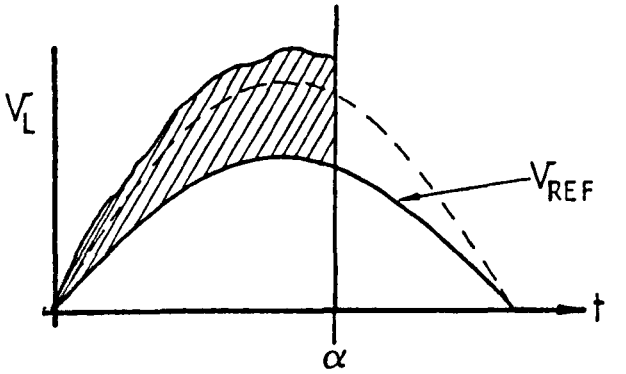


Fig. 4.15(b) : Integral of voltage difference - early firing

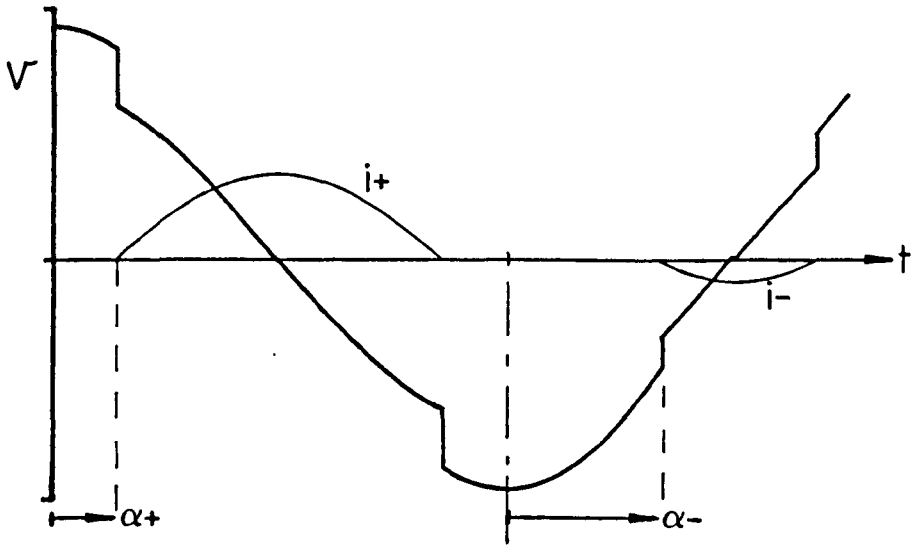


Fig. 4.16 : Voltage depression due to shunt TCR conduction

The principle of the control algorithm is now established:

> A voltage waveform that is overall greater than some nominal reference within one half cycle will cause earlier switching of the TCR compensator. This will depress the voltage for the remainder of the half cycle.
>
> Conversely, a voltage waveform lower than nominal will cause later switching of the TCR, causing less depression of the voltage waveform within the half cycle.

Thus it is intended to balance supply voltage variations with those impressed by the TCR. This is of course the principle of shunt compensation whereby the compensator inversely balances the varying load characteristics.

Cooper and Hussayni[41] surmised that the use of a reference sine wave integration process may present difficulties in the synchronisation of the reference sinusoid $v_R(\omega t)$ to the distorted voltage

$$v'(\omega t) = v(\omega t) + v_f(t)$$

The relative size of the reference sinusoid is also of obvious importance, and is related to the process by which a thyristor firing angle is decided. Fortunately, where this process is determined by a computer program, numerical techniques may be used to investigate and experiment with the control method. Figure 4.17(a) and (b) give the full flow chart for the control algorithm. The full program compiler listing is given in Appendix F.

The integration procedure begins after each zero-crossing of the supply voltage waveform, each digital sample is added to give a cumulative sum. When the sum exceeds a pre-set value, a short pulse is output to cause the thyristor that is correctly biassed to turn on. Thyristor turn-off follows naturally at the next current zero, approximately 180-2α degrees later.

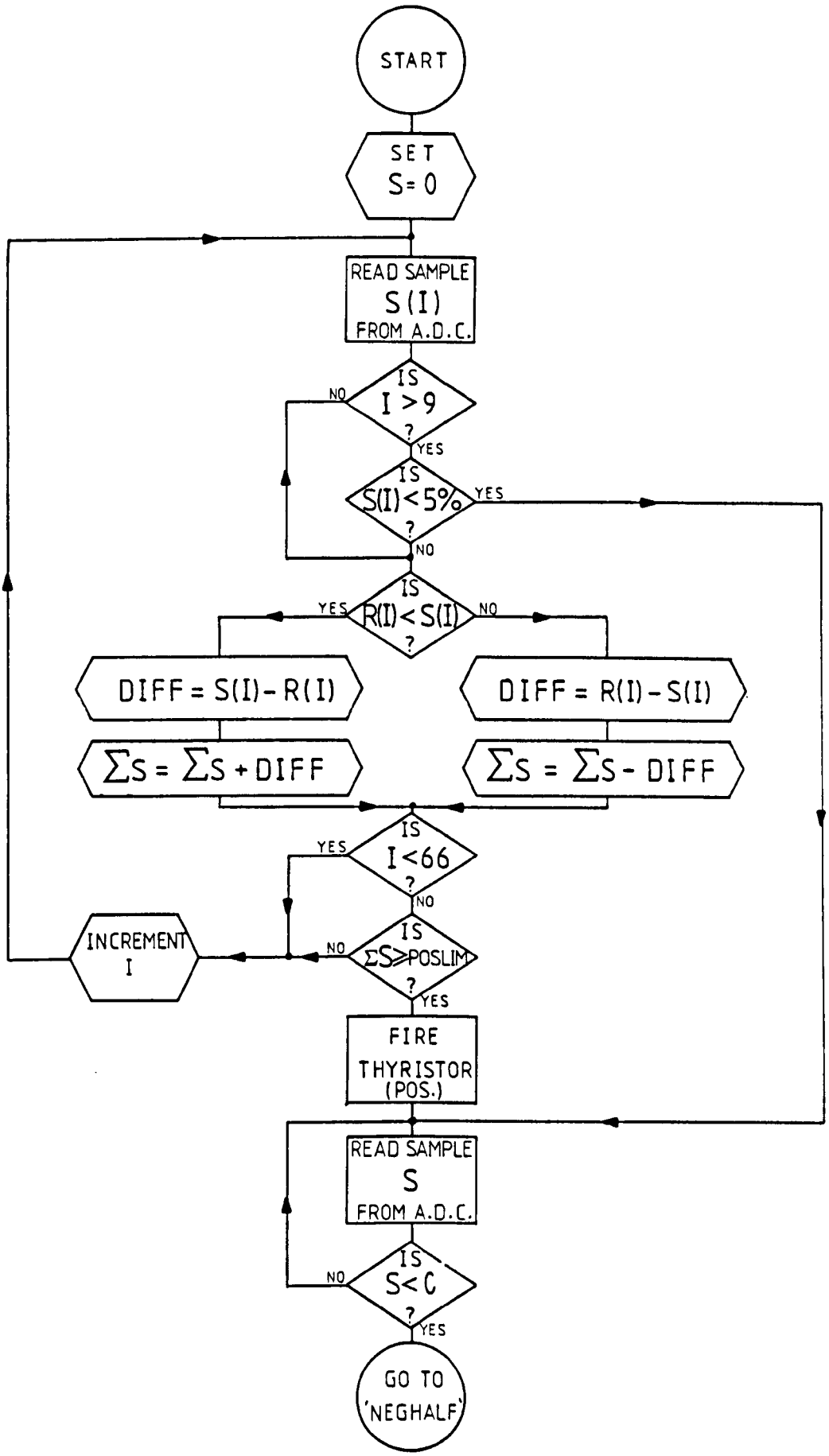


Fig. 4.17(a) : 6-pulse TCR compensator control algorithm flow chart

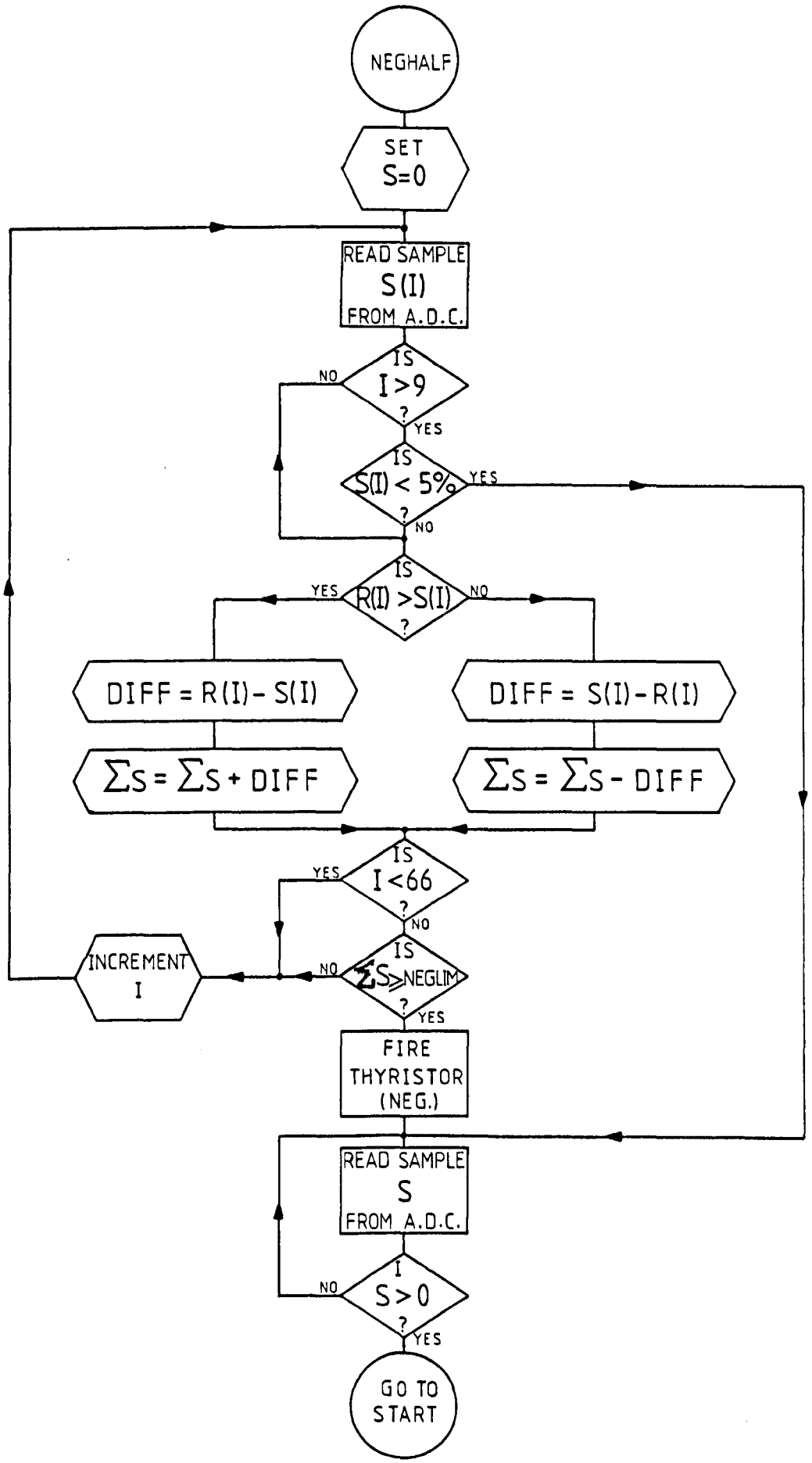


Fig. 4.17(b) : 6-pulse TCR compensator control algorithm flow chart (cont'd)

This procedure therefore performs the discrete equivalent of the continuous integral

$$\int_0^{a/\omega} v'(\omega t)dt$$

where a is measured from the preceding voltage zero-crossing.

The machine code was stored in a file on the Tectronix 8560 MUSDU and downloaded in turn to each of the three SDK-88s. Small differences between the three SDK-88 systems necessitated that changes be made once the code was in the processors RAM.

All variables in the program could be changed via the terminal and SDK-88 Monitor routine, those requiring attention are considered below, together with reasoning for their values.

4.2.4 Control Variables

The variables in the control program that require consideration are:

(i) The sample loop delay, D.

(ii) The reference sine wave, $v_R(\omega t)$.

(iii) The integration limit, LIMIT

and these are now considered in turn.

(i) Sample Loop Delay, D

It was found that free running of the program, with no additional delays inserted, gave consecutive ADC read pulses approximately every 65 microseconds. This time, Δt, varied slightly between the three SDK-88 systems:

System 1, Δt approximately 63 μseconds
System 2, Δt approximately 66 μseconds
System 3, Δt approximately 64 μseconds

Although small, these differences would mean that a particular integration limit would be reached at different times in different processors.

For example, 7.5 milliseconds would contain 119, 113, 117 samples by 1,2,3 respectively, giving approximately 0.4 milliseconds difference between the firing times in two different branches of the TCR.

In order to balance the three systems as best as possible, a software 'sample loop delay', D, was inserted in the program using the software:

```
--------------
  MOV  CL,'D'
  SHR  CL, CL
--------------
```

(See Appendix F for full program listing.)

Δt was fixed close to 74.0 microseconds using the following values of D:

System 1, positive half cycle, D = 9 @ 09 : Δt = 74.4 μsecs
negative half cycle, D = 8 @ 08 : Δt = 74.2 μsecs
System 2, positive half cycle, D = 6 @ 06 : Δt = 74.1 μsecs
negative half cycle, D = 4 @ 04 : Δt = 74.6 μsecs
System 3, positive half cycle, D = 8 @ 08 : Δt = 74.1 μsecs
negative half cycle, D = 6 @ 06 : Δt = 74.6 μsecs

The final location of bytes representing 'D' in RAM were 14 and 116 bytes respectively from the start of the 'fireAsub' object code program block.

(ii) The Reference Sine Wave, $v_R(\omega t)$

The signal conditioning circuits and ADCs were carefully adjusted so that ±262 volts for the model supply line voltage, v_L, would just be within the range of the 8-bit ADCs. This ± 262 volt range allowed the nominal supply line voltage to rise by 5p.c. and just be within the extreme range of the ADC.

Figure 4.18 shows how use of the ADC in its unipolar mode results in:

v_L = -262 Volts is sampled as @ 00 or @ 01

v_L = 0 Volts is sampled as @ 7F or @ 80

v_L = +262 Volts is sampled as @ FE or @ FF

Ajustment enabled the underlined values to be repeatedly obtained with a test 262v dc supply.

Thus the least significant bit (LSB) of the data byte represents 2.063 volts of the model supply v_L.

The nominal model line voltage of V_{RMS} = 175 volts will then give an equivalent sampled sine wave of:

$$v_S = 127 + 120 \sin\omega t$$

Similarly $v_S = 127 + 116 \sin\omega t$ for V_{RMS} = 179 Volts
and $v_S = 127 + 113 \sin\omega t$ for V_{RMS} = 165 Volts

Full conduction of the TCR with 1.0 Henry inductances in each branch would produce the equivalent circuit shown in Figure 4.19, and the model busbar voltage will fall to
V_{RMS} = 160.44 Volts.

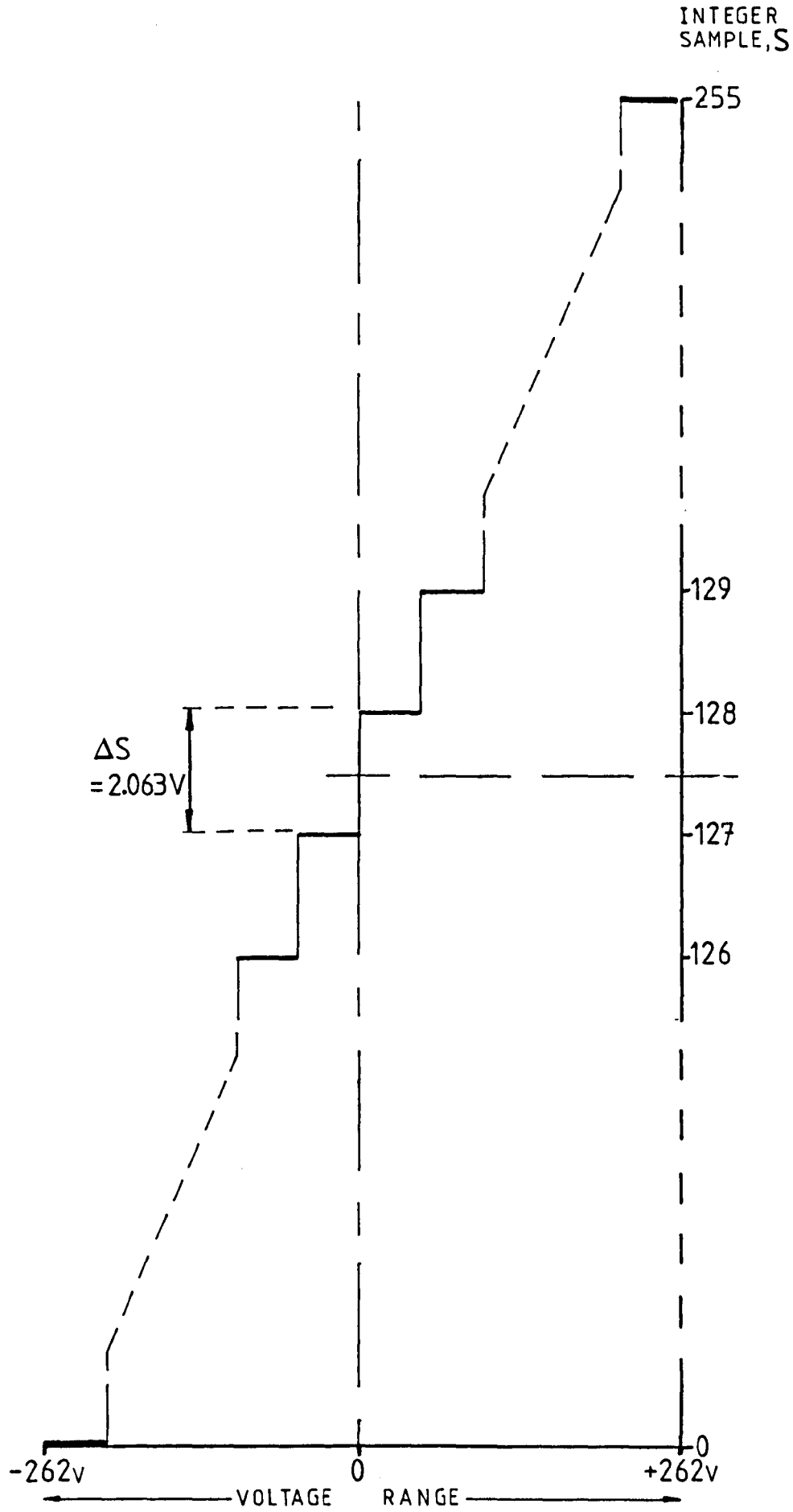
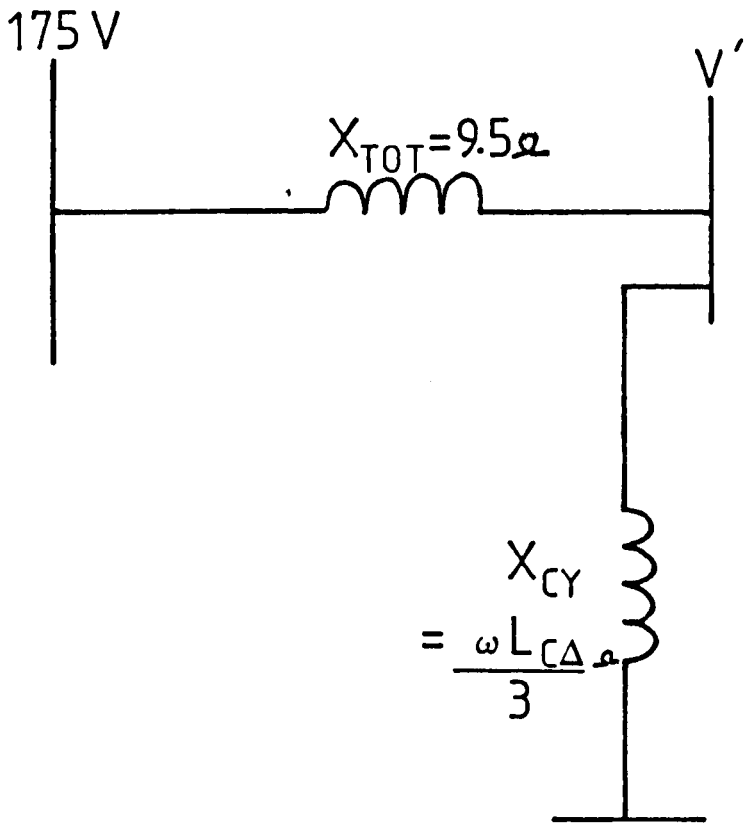


Fig. 4.18 : ADC range and span



FOR $L_{C\Delta}$ = 1.0 HENRY, V' = 160.4 VOLTS

Fig. 4.19 : RMS Voltage depression for full compensator conduction

This would be represented by an equivalent sampled sine wave of:

$$v_S = 127 + 110 \sin\omega t$$

Making the reference sinusoid equal to this ensured that most sampled points would be greater than or equal to the 'reference' values:

$$\text{ie } \underline{v_R = 127 + 110 \sin\omega t}$$

With the knowledge that the sampling interval, Δt, is approximately 74.0 microseconds, it would be a simple matter to calculate values for v_R to correspond to each of the sampled data points v_s. Close examination of the ADC sample circuitry, however, revealed that the first sample was being made 100 microseconds after voltage zero, instead of 74 microseconds. This occured because of a 25 microsecond delay introduced by the section of the program that detected the voltage-zero crossing.

A nominal supply frequency of 50Hz allows 133 reference points to be calculated for each half cycle.

t_o=0, t_1=100, t_2=175, t_3=250 .....t_{133}=10,000 µsecs

The points for the positive half-cycle v_R were stored in a look-up table beginning at the memory location labelled 'sine1'. Similarly, 'sine2' located the negative half-cycle of v_R. All were individually calculated for unipolar operation to eliminate the maximum amount of real time processing.

iii) Integration limit, LIMIT

Section 4.2.3 described how a digital integration process decided the TCR firing angle in each half-cycle of the supply voltage waveform, $v = V\sin\omega t$, for an equivalent reference sinusoid $v_R = R\sin\omega t$.

The continuous integral to be evaluated would be:

$$E = \int_0^{\frac{\partial}{\omega}} (V\sin\omega t - R\sin\omega t)dt$$

$$= \frac{(V - R)}{\omega} [1 - \cos\partial]$$

Where
- E = The summated error of $v - v_R$.
- ∂ = The phase angle, after the voltage zero-crossing, at which E is reached.
- V = The sinusoidal peak value of v.
- R = The sinusoidal peak value of v_R.

The discretised equivalent of this continuous integral may be written:

$$\sum_{\Delta t} S = \frac{(V' - R')}{\omega} \left[1 - \cos\partial\right]$$

Where
- Δt = The sampling interval
- S = A single digital sample of the difference $(v - v_R)$
- V' = The equivalent digital value of V
- R' = The equivalent digital value of R

and $\sum S$ is the LIMIT value set in RAM to fix the firing angle ∂ w.r.t. voltage zero crossing

or α w.r.t. voltage peak

The units of S and $\sum S$ are simply Volts, although scaling of the digital sample values are required to obtain Volts since:

1 bit = 2.063Volts (Figure 4.18)

Then the relationship between E and $\sum$S or LIMIT is:

$$E = S \times 2.063 \times \Delta t$$

$$= S \times 2.063 \times 74.0\ 10^{-6}$$

$$= S \times 152.7\ 10^{-6}$$

$$= LIMIT \times 152.7\ 10^{-6} \quad \text{Volt Seconds}$$

i.e. $$LIMIT = \frac{E}{152.7\ 10^{-6}} \quad \text{Volt Seconds}$$

Let $$v'_R = 127 + 110 \sin\omega t$$

Then for the digital value 127 = 0 Volts,

$$v_R = 226.9 \sin\omega t \text{ Volts}$$

i.e. $$R = 226.9 \text{ Volts}$$

If v is typically 175V RMS, then

$$V = 247.5$$

thus for $\vartheta = \pi$ radians,

$$E_{MAX} = \frac{[V - R]}{\omega} \times 2$$

$$= 0.131$$

and $LIMIT_{MAX}$ = 858 dec. = 35D hex.

This is the maximum value of integration limit to be expected for R = 226.9 Volts, and it has been calculated assuming a perfectly sinusoidal supply voltage waveform.

For $\vartheta = \pi/2$ radians, LIMIT will be 429 dec. = 1AE hex. These values are clearly dependent upon the choice of reference sinusoid and the distortion of the supply voltage waveform. A theoretical approach will be able to show how combinations of V_R and LIMIT will influence the compensator performance. This is explored further in Section 4.3.3 in the study of steady state reactive compensation.

The compensator performance for different combinations of the control variables above was studied. A 'steady-state' analysis is given in Section 4.3.3, and Chapter V presents the results of experiments using the three-phase compensator with the laboratory arc furnace model.

4.3 STEADY STATE TUNING AND PERFORMANCE

Having established the control variables that would affect the TCR compensator performance, studies were made with an un-modulated 50Hz supply voltage. Varying the RMS value of the voltage illustrated the range of voltage control that the TCR compensator could effect.

These early experiments, with the three-phase TCR arrangement drawing current from the supply for the first time, highlighted the need for careful 'tuning' of the three compensator phases. The more important aspects are now presented.

4.3.1 Thyristor Firing and Conduction Limits

Thyristor turn-on was initiated with a logic '1' applied to the relevant bit of the 8-bit output port at address @ 0F000H. This signal was latched for 100 microseconds and logically ANDed with a 21kHz square wave to produce a 100 microsecond 21kHz burst for application to the thyristor gate through a transistor and isolating pulse transformer. Figure 4.20 gives the firing circuit for each inverse-parallel pair of thyristors switched from the microprocessor output port A. The 5V d.c. supply to the transistor circuits was separate from the 5V d.c. logic supply, and was only energised when firing was required.

The latching circuit meant that the processor was only committed for a very short time at each pulse output, timing and pulse turn-off being executed in hardware rather than software.

The 8088 microprocessor 'SI' register was used to hold the incremented address for each successive reference sinusoid sample, and could thus be used to calculate the number of samples taken after voltage-zero crossing. Each pre-programmed reference sinusoid, 'sine1' and 'sine2' are given in Appendix F.

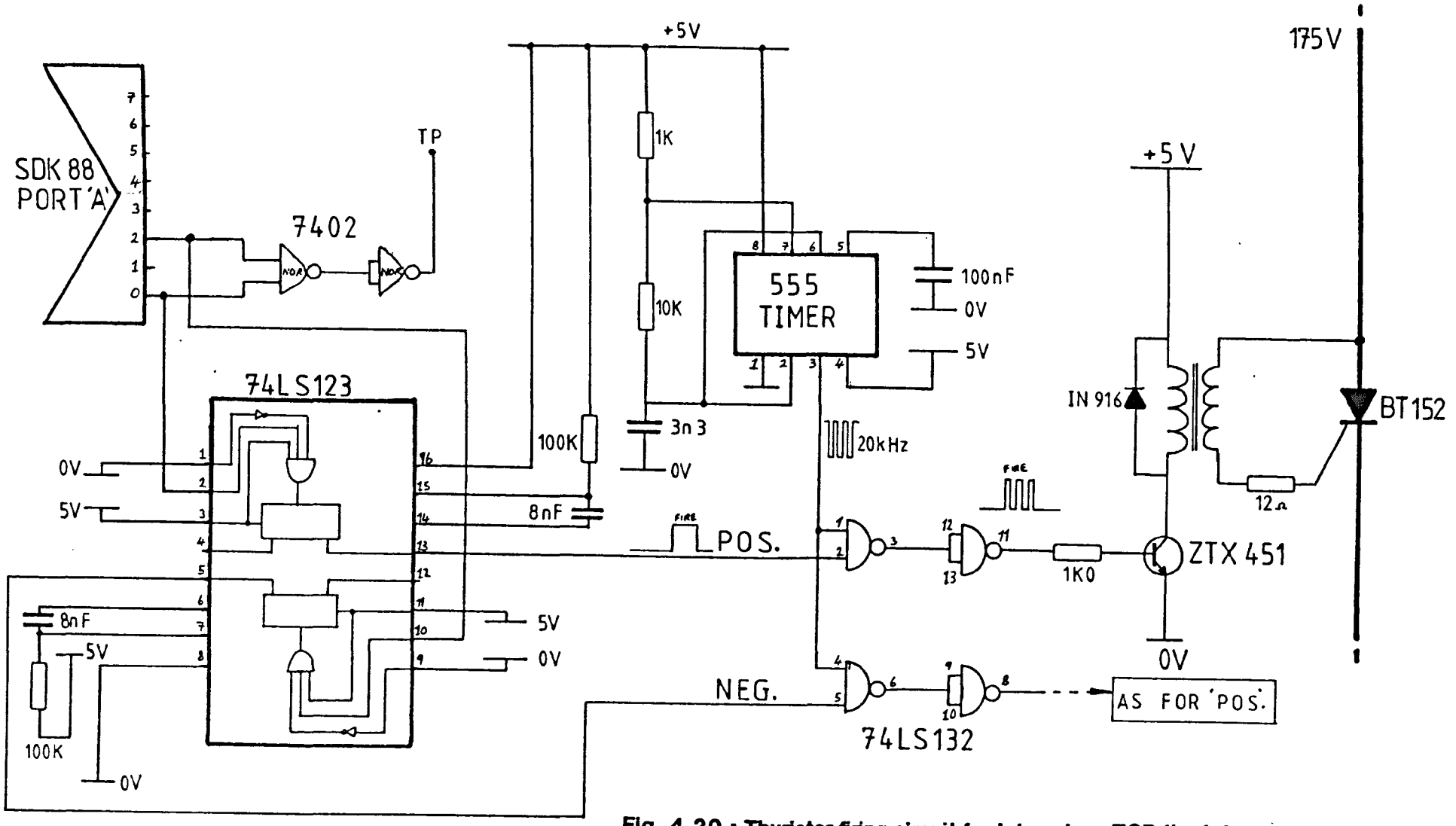


Fig. 4.20 : Thyristor firing circuit for laboratory TCR thyristors

Figure 4.3 shows how the start of conduction for each thyristor must be $0^\circ \leqslant \alpha \leqslant 90^\circ$, where $\alpha = 0^\circ$ is 90° after the relevant voltage zero-crossing.

This range corresponds to:

sine1 $\leqslant$ SI $\leqslant$ sine1 + @ 42 for the positive 1/2-cycle
sine2 $\leqslant$ SI $\leqslant$ sine2 + @ 42 for the negative 1/2-cycle

The program flow chart (Figure 4.17) shows that even if the integral limit is reached, the thyristor firing pulse is not allowed until SI = @ 109A or @ 111F for positive and negative half-cycles respectively.

The control system was also prevented from initiating thyristor firing pulses at the very end of each half cycle of the voltage waveform. This ensured that the program flow proceeded to the section where rapid sampling detects a voltage zero-crossing necessary before the integration process in the following half-cycle may proceed. The program flow chart (Figure 4.17) shows that integration is abandoned if the sampled voltage falls below 14 volts. This is reasonable since thyristor conduction is only prevented beyond $\alpha \simeq 87^\circ$, where compensation effects are a minimum.

4.3.2 Phase Balancing

Small differences in offset and gain in the sampling circuitry for each branch of the compensator, coupled with the slight variance in the sampling rate, resulted in a slightly different firing angle α when identical values of LIMIT were set.

The integration sum LIMIT was then adjusted for the positive and negative half-cycle firing pulse of each compensator branch to achieve totally balanced operation under given conditions.

This required values of LIMIT which varied from each other by up to ± 10p.c., the exact values are given with corresponding theory and results in Section 4.3.3 and Chapter 5.

4.3.3 Steady State Reactive Compensation Theory

Theory will predict the interaction between LIMIT and the reference sinusoid v_R for reactive compensation under sinusoidal conditions. Part 5.1 then presents comparable results obtained in the laboratory, and a choice of control variables may be made before proceeding with laboratory studies for non-sinusoidal conditions.

Figure 4.21 shows the one line diagram and voltage waveform for a three-phase TCR compensator connected to the infinite busbar through an inductance L_S. The single phase equivalent of the delta connected compensator inductance $L_{C\Delta}$ is $L_{CY} = L_{C\Delta}/3$.

When the TCR is OFF, $v_2 = v_1$

When the TCR is ON, $v_2 = Kv_1$

$$\text{Where } K = \frac{L_{CY}}{L_S + L_{CY}}$$

Thyristor conduction occurs for $\sigma \geqslant \omega t \geqslant \partial$, $\sigma = \frac{\pi - \partial}{2}$ radians

The resulting RMS value of the waveform is then:

$$V_{RMS} = \sqrt{\frac{\omega}{\pi}\left\{\int_0^{\frac{\sigma}{\omega}}(Kv_1)^2dt + \int_{\frac{\sigma}{\omega}}^{\frac{\partial}{\omega}}(v_1)^2dt + \int_{\frac{\partial}{\omega}}^{\frac{\pi}{\omega}}(Kv_1)^2dt\right\}}$$

$$= \sqrt{\frac{K^2V_1^2}{\pi}\left[\pi - \partial + \frac{\sin 2\partial}{2}\right] + \frac{V_1^2}{2\pi}\left[2\partial - \pi - \sin 2\partial\right]}$$

.....Equation I

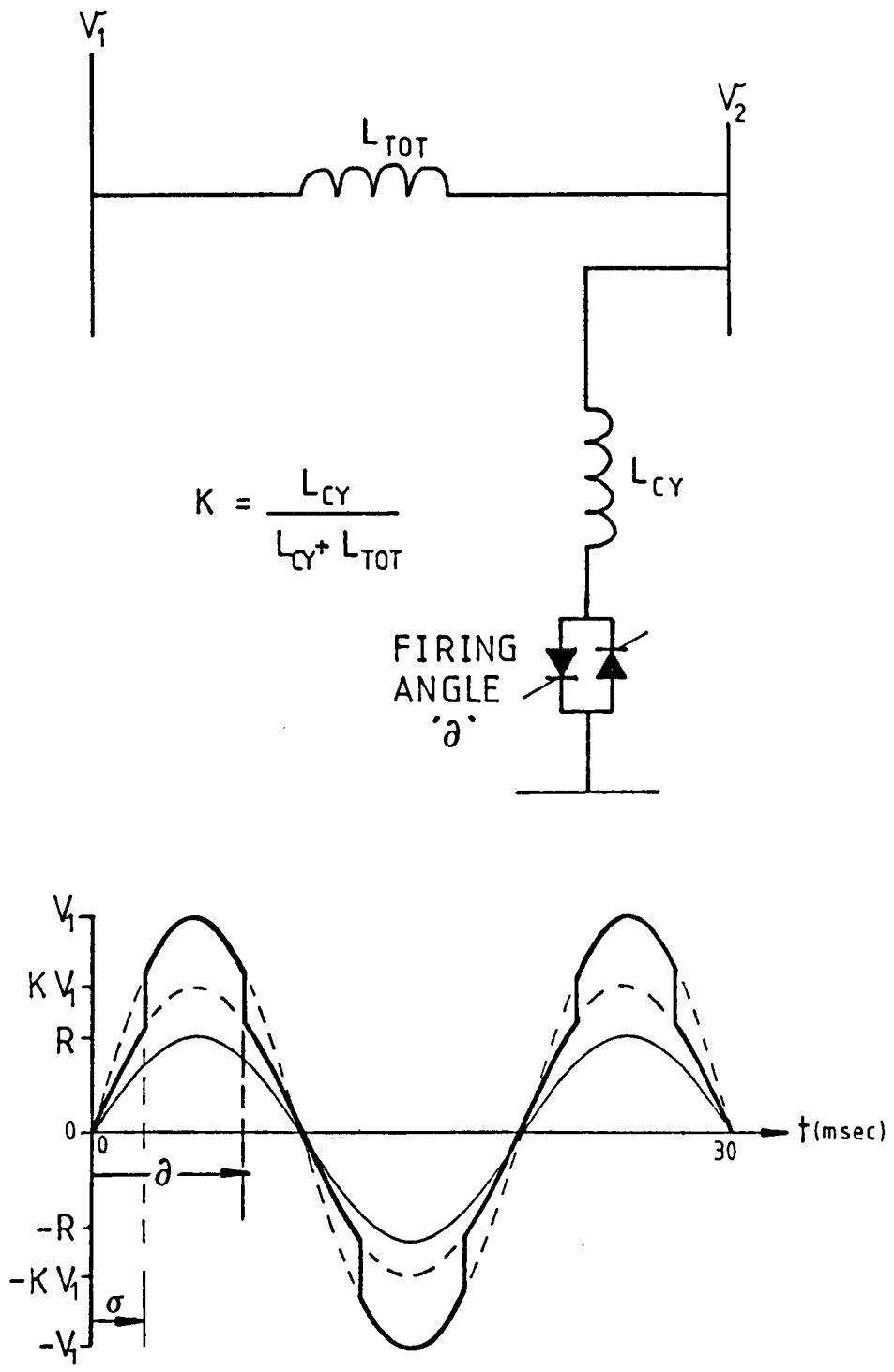


Fig. 4.21 : One line diagram for 'open circuit' TCR compensation equations

The continuous integral sum, from the voltage zero crossing to firing angle ∂, is:

$$E = \int_0^{\frac{\sigma}{\omega}} (KV_1 - R)\sin\omega t\, dt + \int_{\sigma}^{\frac{\partial}{\omega}} (V_1 - R)\sin\omega t\, dt$$

$$= \frac{KV_1}{\omega} - \frac{R}{\omega} - \cos\partial \left[\frac{KV_1 + R - 2V_1}{\omega}\right] \quad \text{Volt Seconds}$$

$$\partial = \cos^{-1}\left[\frac{\omega E + R - KV_1}{R - V_1(2-K)}\right] \text{ radians}$$

.....Equation II

For a given value of LIMIT (and hence E), the values of V_1, K and R may be set as required, and ∂ from Equation II substituted into Equation I to give V_{RMS}.

V_1 is nominally 247.5 Volts corresponding to 175 Volts RMS.
R = 110 x 2.063 = 226.9 Volts
L_S = 30.4millihenries

For $L_{C\Delta}$ = 1.0H ; L_{CY} = 0.333H and K = 0.916

The variation of ∂ versus LIMIT for K = 0.916 is shown in Figure 4.22.

Three steady-state values of the firing angle α were chosen for experiments with the laboratory TCR. These are shown in Figure 4.22, ∂1 ≃ 100°, ∂2 ≃ 135° and ∂3 ≃ 170°. They represent only a lower mid and upper setting for $90° \leqslant \partial \leqslant 180°$, with the greatest range of VAR control occurring from ∂1 ≃ 100°. However, including three values of the integration limit will highlight its effects in the control scheme.

Figure 4.22 gives:

LIMIT1 = 150 dec. for ∂_1
LIMIT2 = 610 dec. for ∂_2
LIMIT3 = 843 dec. for ∂_3

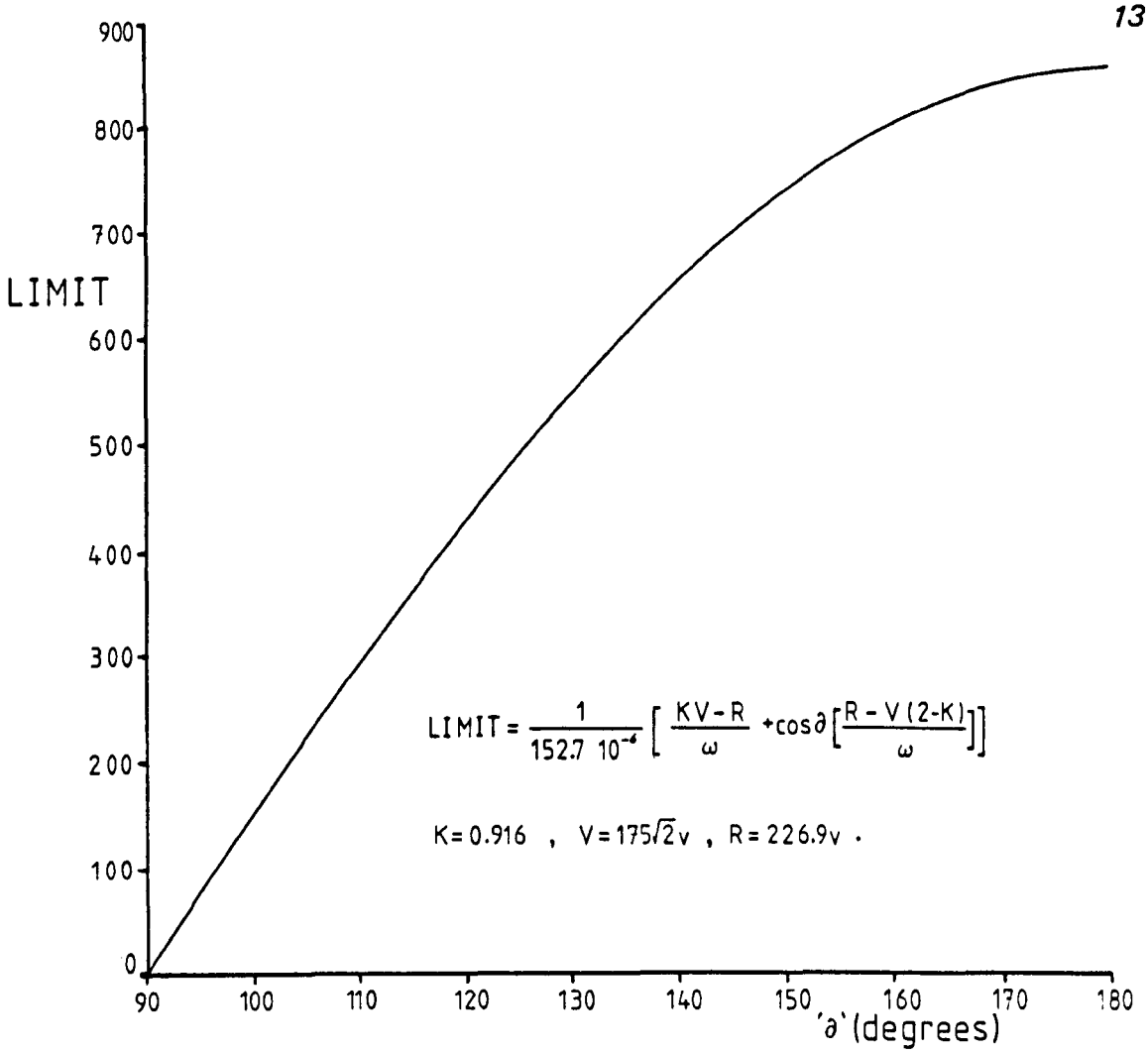


Fig. 4.22 : Theoretical variation of LIMIT versus '∂'

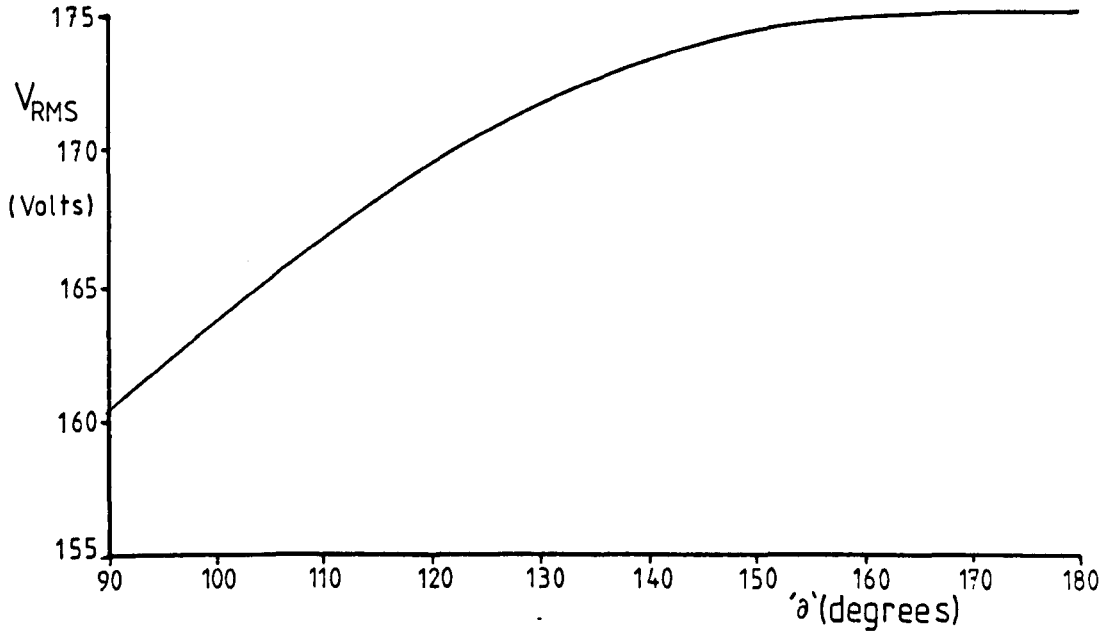


Fig. 4.23 : Theoretical variation of RMS voltage versus '∂'

For a fixed value of V_1, V_{RMS} can be plotted as a function of a only. This is shown in Figure 4.23.

Once the parameters D, v_R and LIMIT have been set for a constant supply voltage peak V_1, it is sensible to undertake a study of the effects of varying V_1 for a set combination of control variables. This will allow the compensator performance to be evaluated as a function of the control parameters.

A simple investigation of the TCR compensator's ability to control the voltage at its point of connection may be carried out using the circuit representation of Figure 4.24. This will give results for open-circuit voltage control. Shunt load TCR compensation may then be studied using the circuit representation of Figure 4.25.

(i) Open Circuit Voltage Control

Open-circuit voltage control describes the function of the TCR compensator when there is no other load connected in parallel to the point of TCR connection (Figure 4.24).

With a fixed reference sinusoid, v_R, V_1 may be varied over a set range. V_{2RMS} may then be calculated using equations I and II, provided that a suitable value for LIMIT is set. Figure 4.26 shows the effect of using LIMIT1, LIMIT2 and LIMIT3 above for fixed R = 226.9 Volts.

The flatter portions of each curve indicate the full range of TCR control, with a progressing from 180° to 90° as V_1 increases. Figure 4.26 shows clearly that the lower value of integration limit will give the flattest voltage control region. The linear portions above the range of control have gradient K = 0.916 since here $V_2 = KV_1$. The linear portions below the range of voltage control are of gradient 1 since $V_2 = V_1$ before conduction in the TCR.

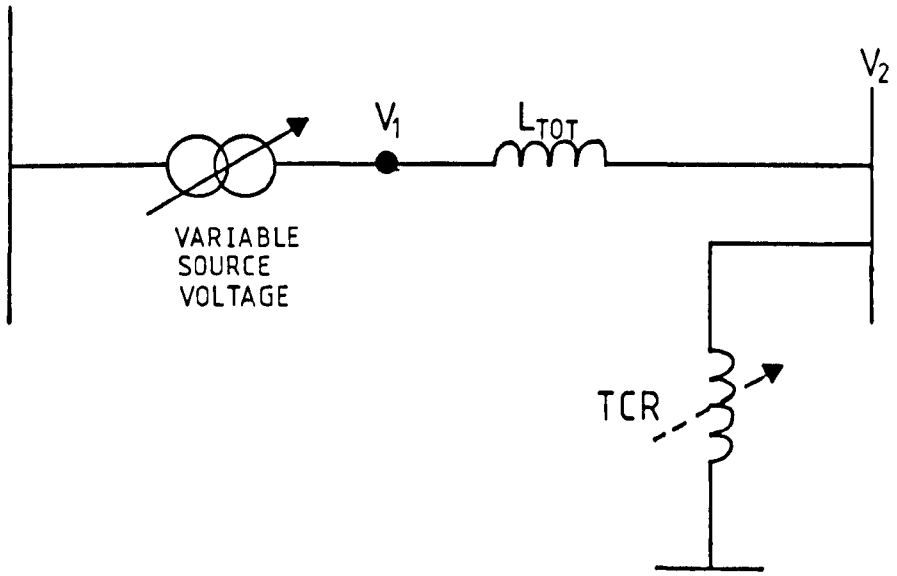


Fig. 4.24 : Experimental circuit for steady state 'open circuit' compensation

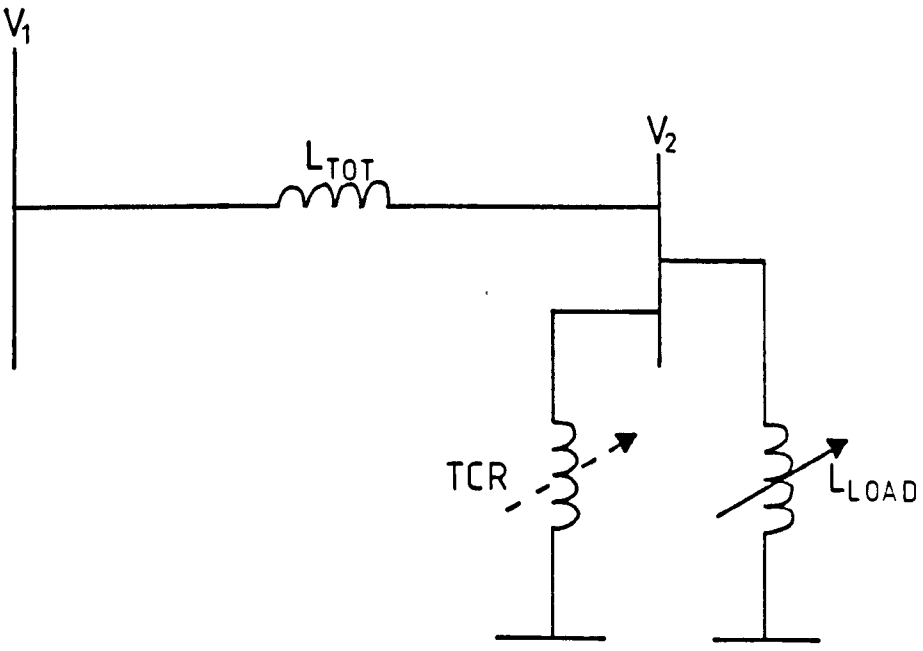


Fig. 4.25 : Experimental circuit for steady state shunt load compensation

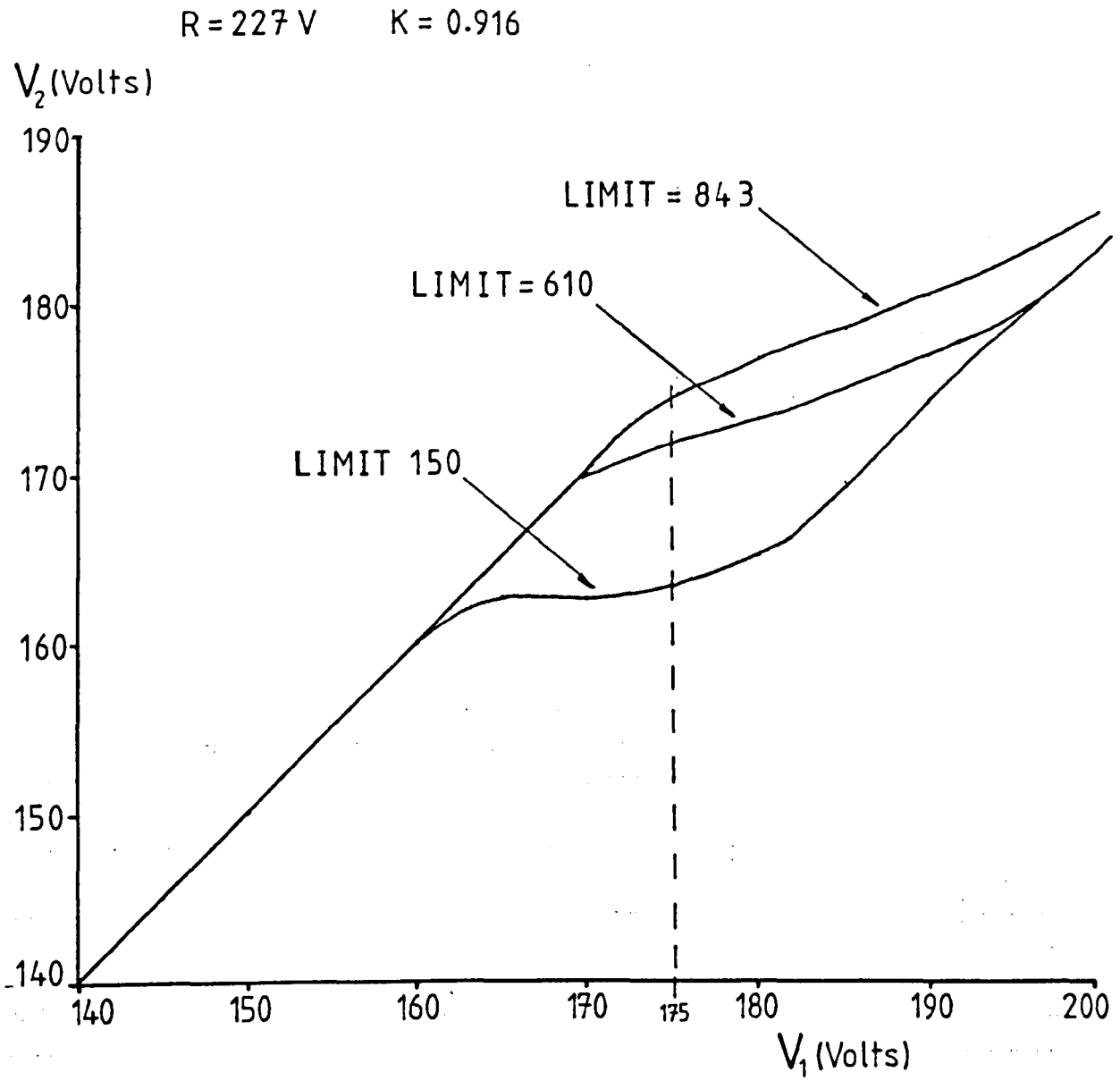


Fig. 4.26 : Theoretical 'open circuit' TCR voltage control characteristics for varying LIMIT

Having established that LIMIT1 is most likely to give the best TCR performance, we may investigate the effect of varying the value of the reference sinusoid $v_R(\omega t) = R\sin\omega t$, whilst keeping LIMIT constant at LIMIT1.

Figure 4.27 shows how the calculated level of the flat, controlled region, of V_{2RMS} is proportional to the magnitude of the reference sinusoid, typically within one percent of $R/\sqrt{2}$ Volts, and that voltage fluctuations up to the operating level of 175 Volts are best controlled with a value of R = 226.9 Volts.

Figure 4.28 shows how the calculated characteristics are changed by higher ratings of shunt TCR compensators, using values of K = 0.915, K = 0.861, K = 0.731, representing TCR three-phase ratings of L_C = 1.01, 0.57 and 0.25 Henries respectively. The flat control region is extended for increased TCR rating.

(ii) Shunt Load TCR Compensation

With a variable load shunt-connected with the TCR compensator (Figure 4.25), the value of v_2 becomes:

While the TCR is not conducting: $v_2 = K_1 v_1$

where: $K_1 = \dfrac{L_1}{L_L + L_S}$

While the TCR is conducting: $v_2 = K_2 v_1$

where: $K_2 = \dfrac{L_{CY}}{L_{CY} + L_S + L_S L_{CY}/L_L}$

as illustrated in Figure 4.29.

The equations for firing angle α and V_{2RMS} are now:

$$V_{2RMS} = \sqrt{\left(\frac{K_2 V_1}{\pi}\right)^2 \left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right] + \left(\frac{K_1 V_1}{2\pi}\right)^2 \left[2\alpha - \pi - \sin 2\alpha\right]}$$

.....Equation III

$$\alpha = \cos^{-1}\left[\frac{\omega E + R - K_2 V_1}{R - V_1(2K_1 - K_2)}\right]$$

.....Equation IV

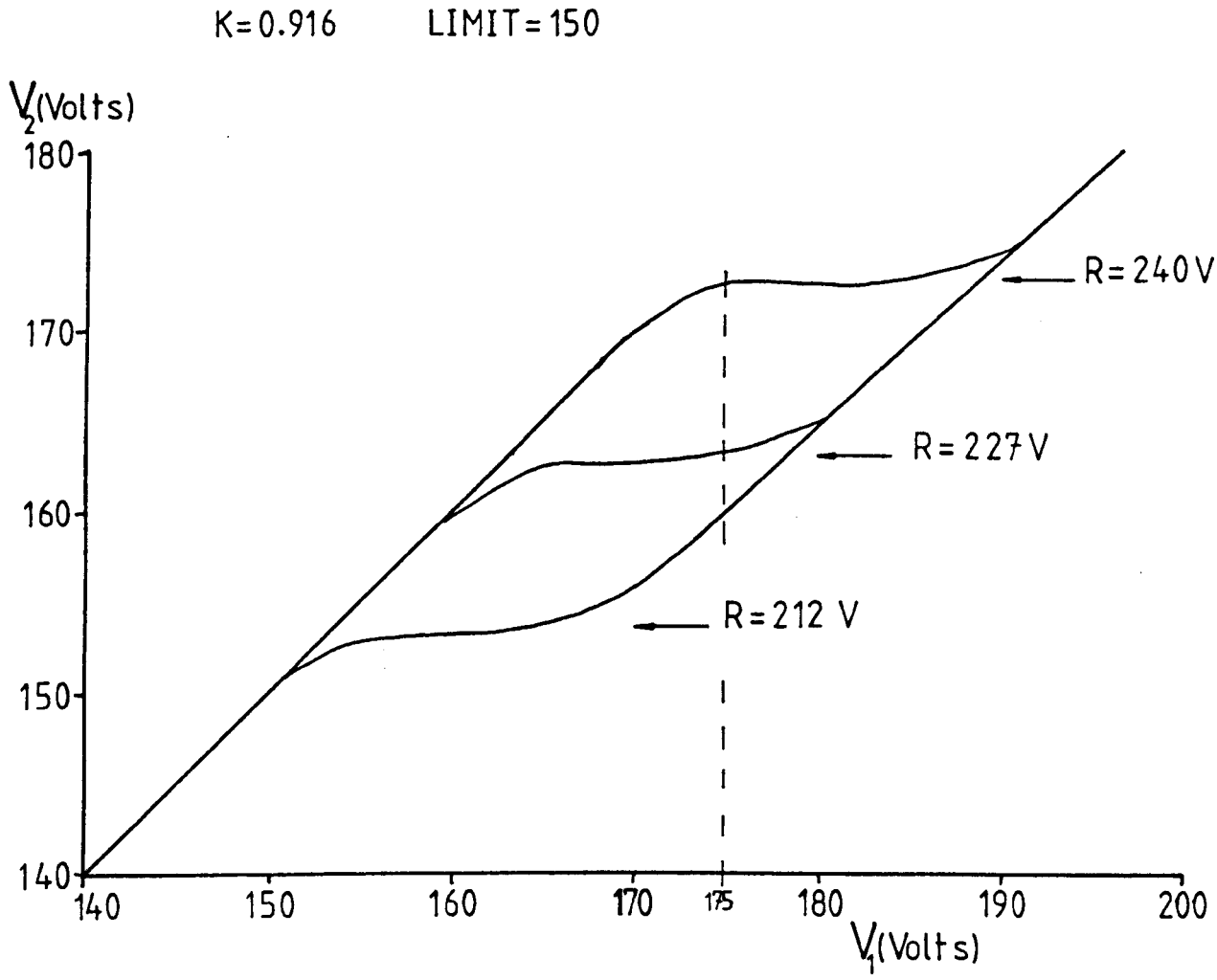


Fig. 4.27 : Theoretical 'open circuit' TCR voltage control characteristic for varying Vref

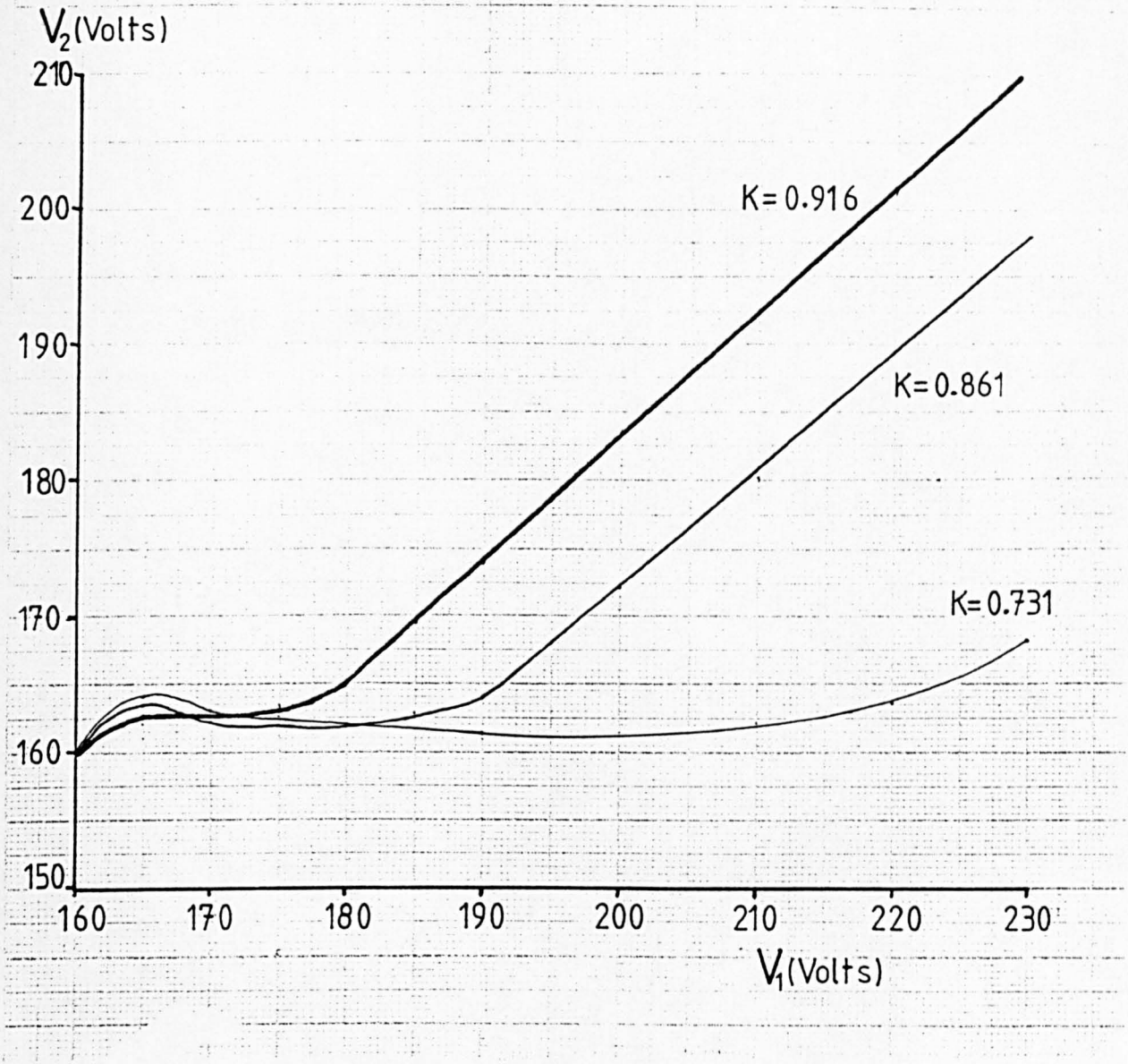


Fig. 4.28 : Theoretical 'open circuit' TCR voltage control characteristics for varying TCR rating

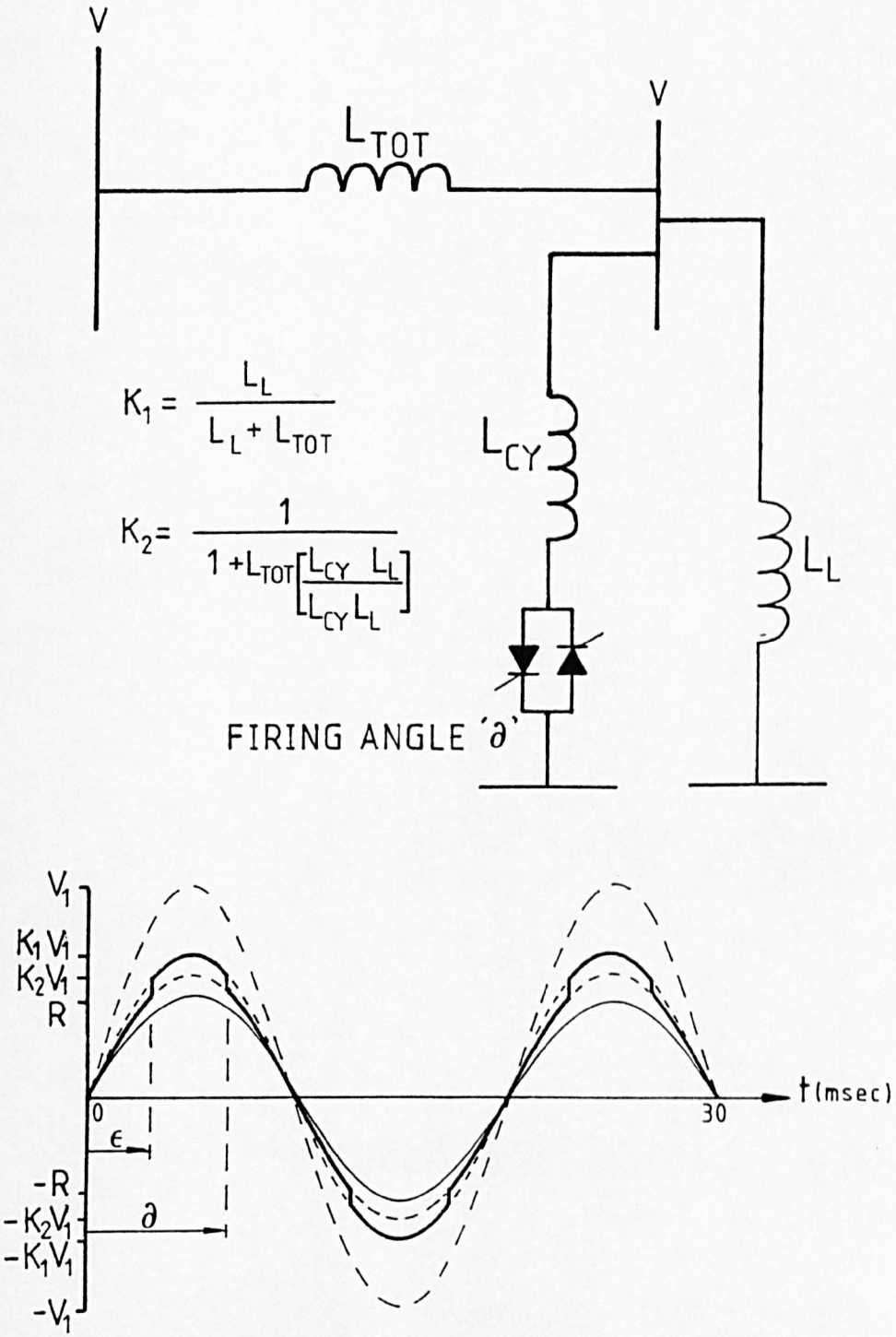


Fig. 4.29 : Theoretical voltage depression for shunt load TCR compensation

v_1 may now remain fixed at 175V RMS, and v_2 will vary as a function of the load current, i_L. Varying i_{LRMS} over the range 0 to 2.5 Amps will cause uncompensated linear voltage depression from 0 to -14p.c.

Figure 4.30 shows the calculated effect of varying LIMIT with fixed reference sinusoid $v_R = R\sin\omega t$. It can again be seen that the compensation span calculated for LIMIT1 is flatter than that for higher integration limits.

The calculated effects of varying V_{REF} for fixed LIMIT = LIMIT1 are shown in Figure 4.31, and the curves for fixed LIMIT and V_{REF} are shown in Figure 4.32 for three values of TCR compensator branch inductance.

These theoretical results suggest the optimum values for control algorithm parameters

(a) Set the integration limit to be as low as possible for a given TCR compensator rating.

then (b) Adjust the peak reference sinusoid value, R, to be such that firing angle control is obtained over the full range from $90^\circ \leqslant \alpha \leqslant 180^\circ$ as near as possible to the operating voltage.

The complementary results from laboratory experiments are presented in Chapter V.

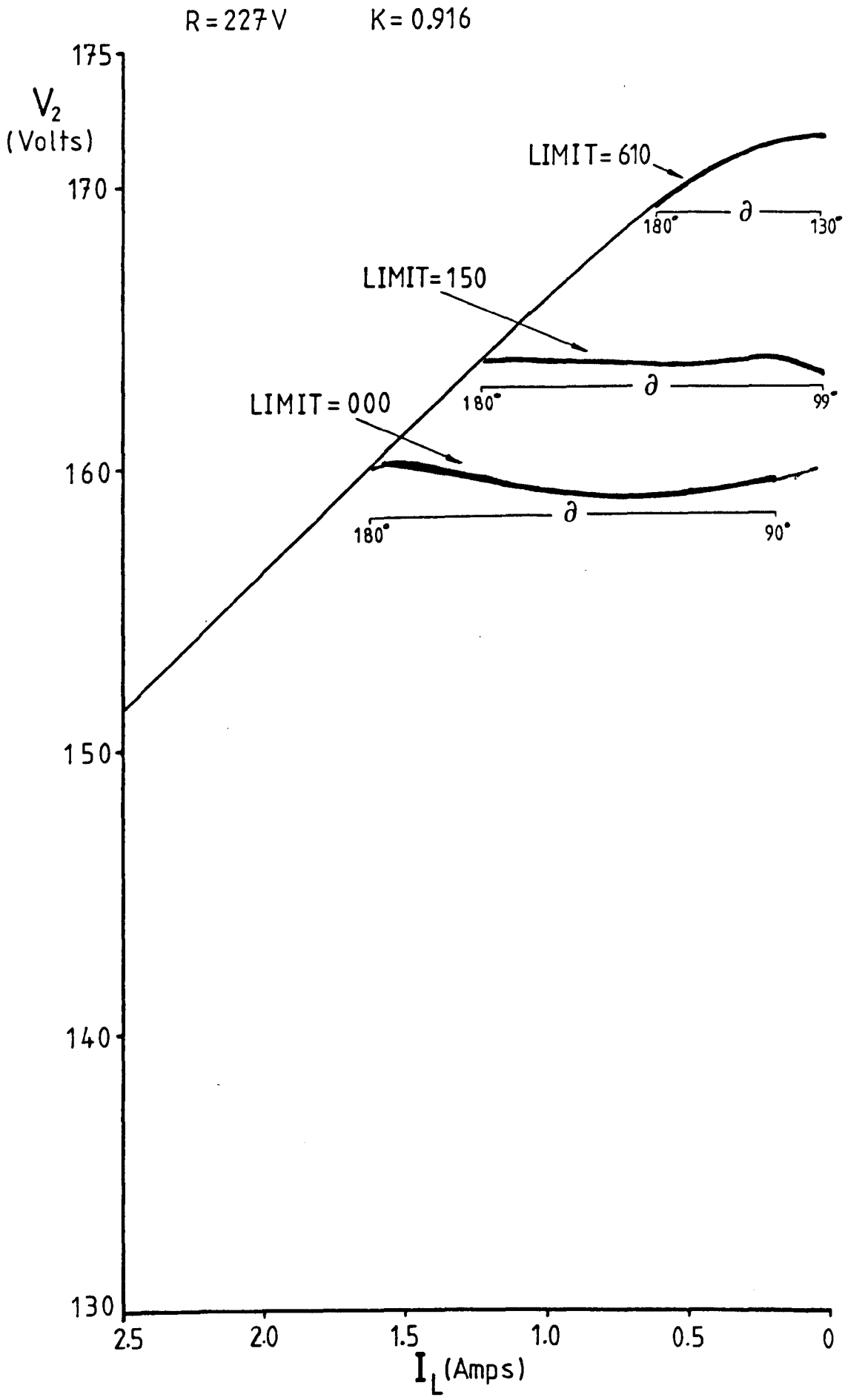


Fig. 4.30 : Theoretical shunt load compensation TCR voltage control characteristics for varying LIMIT

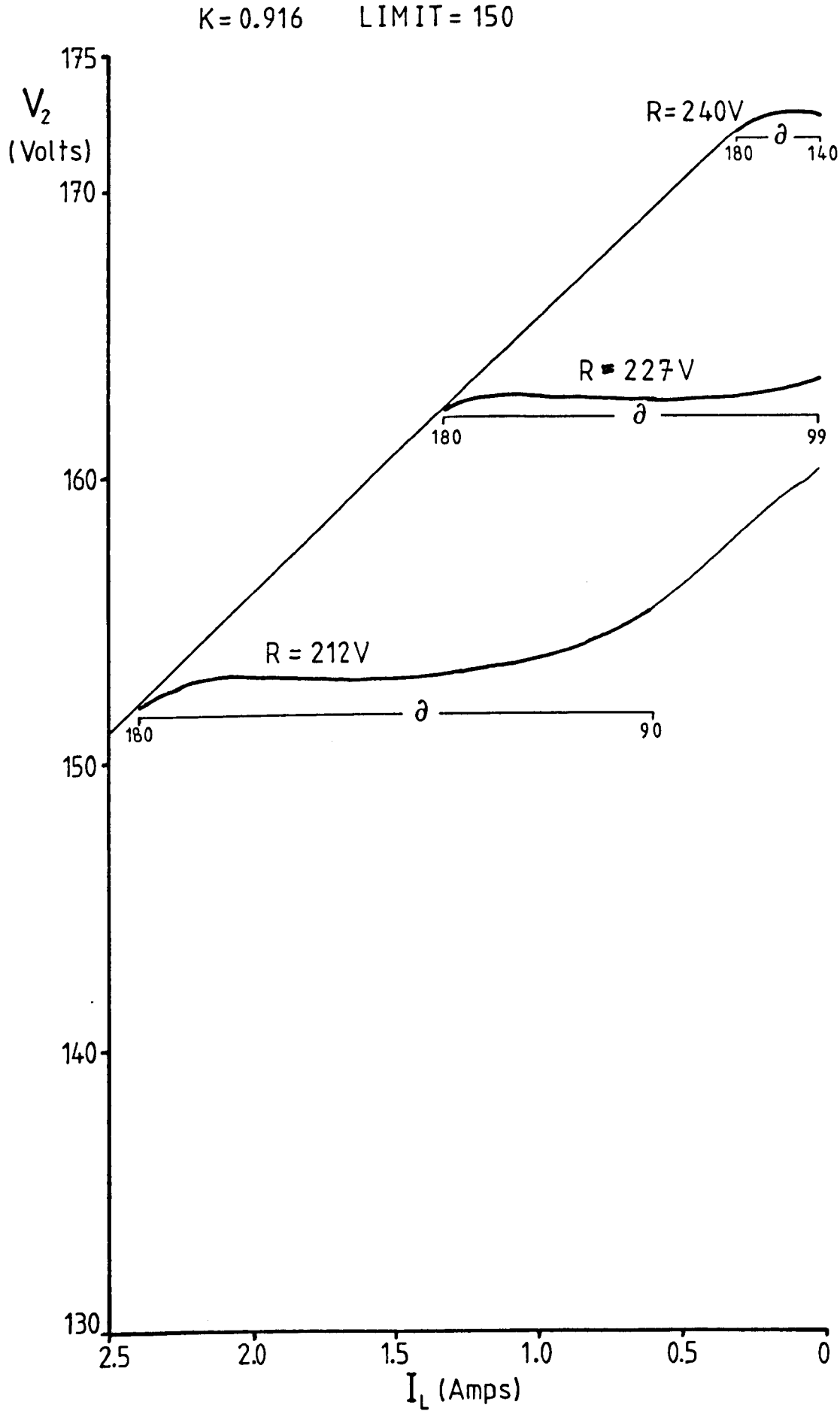


Fig. 4.31 : Theoretical shunt load compensation TCR voltage control characteristics for varying Vref

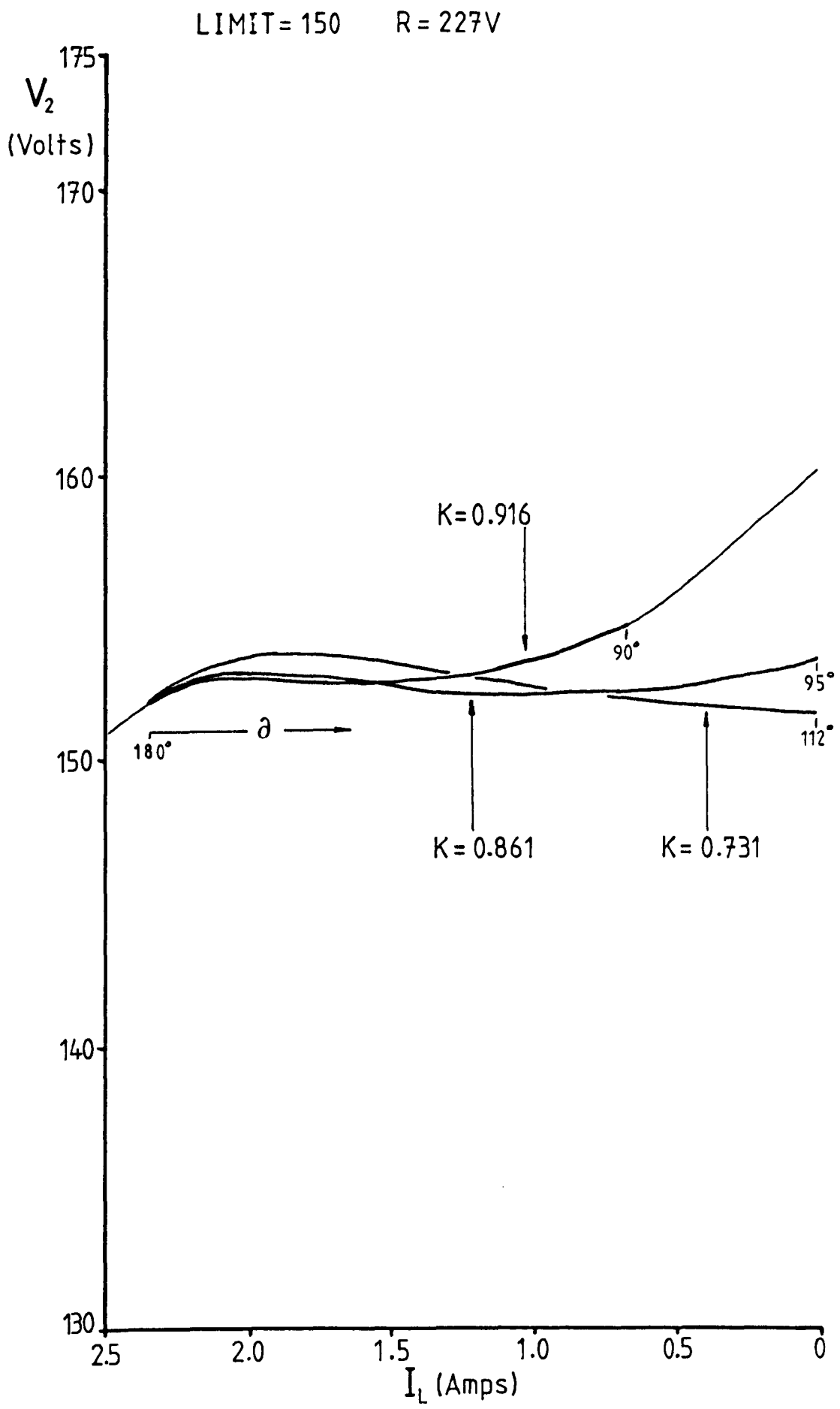


Fig. 4.32 : Theoretical shunt load compensation TCR voltage control characteristics for varying TCR rating

4.4 USE OF THE TCR UNDER NON-SINUSOIDAL CONDITIONS

When the principles behind the control and operation of the laboratory TCR compensator were understood, it was connected to the arc furnace model (Part 2.3) as shown in Figure 4.33.

With the arc furnace model's feedback gain set to zero, no 'furnace' current was drawn from the laboratory supply, and the TCR compensator currents caused all of the observed line voltage distortion (Section 4.3.3). Values of the integration sum LIMIT1 at which firing occurred, was carefully set to give a firing angle of $\alpha 1 \simeq 100°$. The gain in the arc furnace model feedback circuit was then increased to its normal operating level. Peaks in furnace current caused α to increase proportionally, up to the maximum of 180°.

The values of the integration sum LIMIT used in the model TCR compensator control system are tabulated in Chapter V, with a range of results showing the compensator performance as a function of the control parameters.

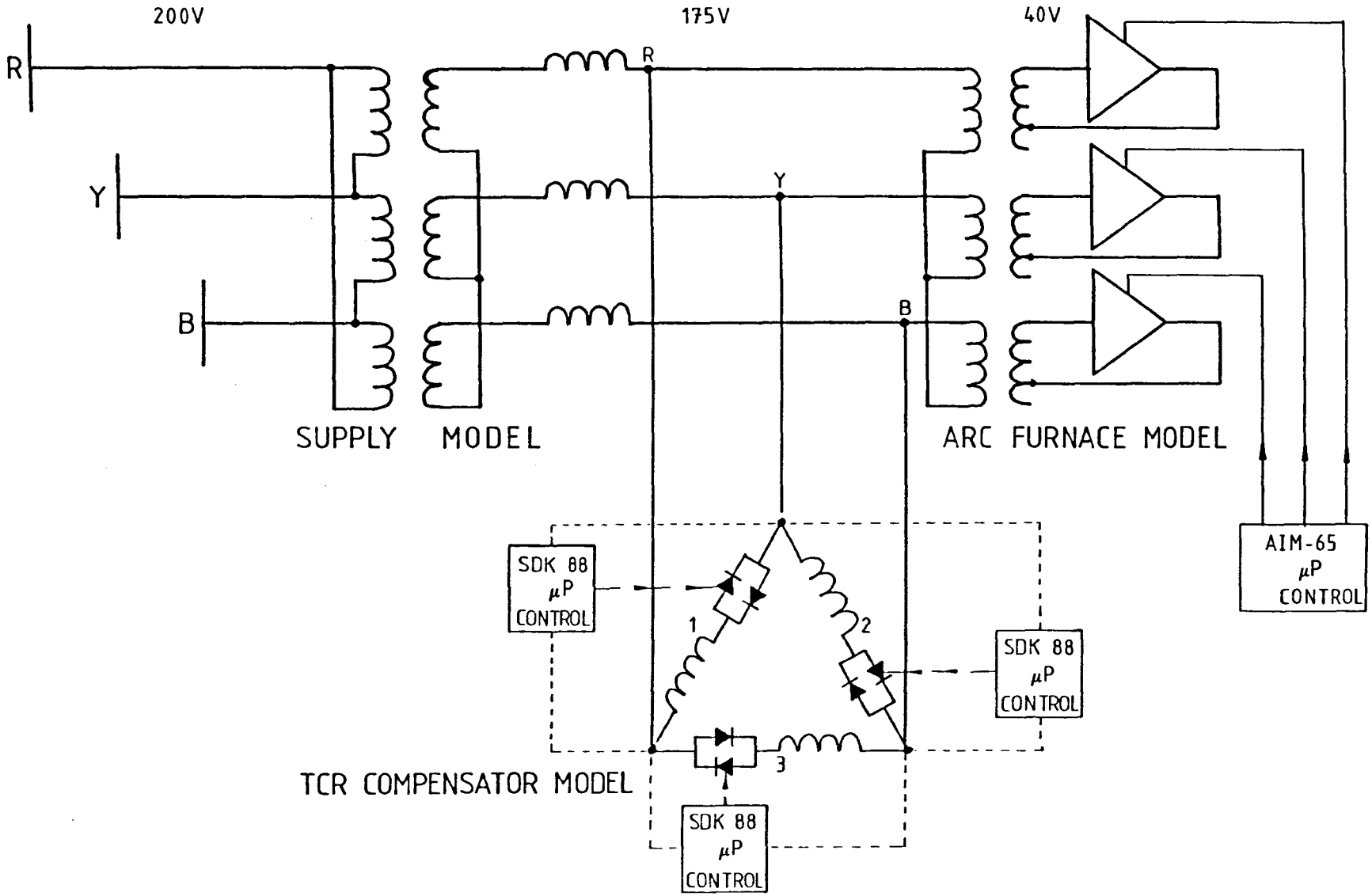


Fig. 4.30 : Connection of the 6-pulse TCR compensator to the arc furnace model

CHAPTER FIVE

SIX PULSE TCR RESULTS

CHAPTER FIVE

SIX PULSE TCR RESULTS

A 'steady state' performance analysis was carried out in Section 4.3.3 to show the theoretical voltage regulation characteristics of the TCR under sinusoidal conditions. The corresponding laboratory measurements were in agreement with theory, and the TCR was then used with the laboratory arc furnace model.

The method of spectral analysis was used to judge the performance of the laboratory models and the TCR control. A reduction in the power spectral density components of modulating frequencies up to 30Hz was achieved.

The TCR rating was then increased, and a further set of results taken for comparison with those from the original TCR rating.

Finally, measurements were taken with the CEGB/Electricity Council 'flickermeter'[14,16] to allow the disturbance levels on the laboratory model to be related to those elsewhere.

5.1 STEADY STATE TCR COMPENSATOR PERFORMANCE

The two circuit configurations studied computationally in Section 4.3.3 are shown in Figures 4.22 and 4.23. Both studies were repeated using laboratory equipment and the TCR.

5.1.1 Open Circuit Voltage Characteristics

Figure 5.1 shows the voltage characteristics for the TCR compensator only connected to the supply having an equivalent source inductance of L_s = 30.4 millihenries. V_1 and V_2 are the voltages at the source and at the compensator respectively.

V_1 was varied using a three-phase variable transformer with a maximum output line voltage of 240V for 200V input. V_2 is not equal to V_1 before TCR conduction because the source impedance is that of the 200/175V Y-Δ transformer. Any measured gradients should therefore be multiplied by the factor 200/175 = 1.143 to take account of this.

The corrected gradient of the linear region before TCR conduction is 1.006, after full conduction it is 0.869. The theoretical values are 1.000 and 0.916 respectively.

The effect of varying the integration limit can be seen clearly - a flatter but shorter control region results from the lower integration limits. The hexadecimal and decimal LIMIT values are given in Table 5.1.

The tests were repeated for a higher TCR rating of 512VA corresponding to a value of C/F = 1.13. This uses L_c = 0.56 Henries giving K = 0.860.

Figure 5.2 gives the open circuit voltage characteristics for the higher rating TCR for three values of LIMIT giving steady state firing angles of $\alpha = 110^\circ$, 135° and 170° respectively. The corrected gradient of the linear region before TCR conduction is 0.976, with 0.853 after full conduction.

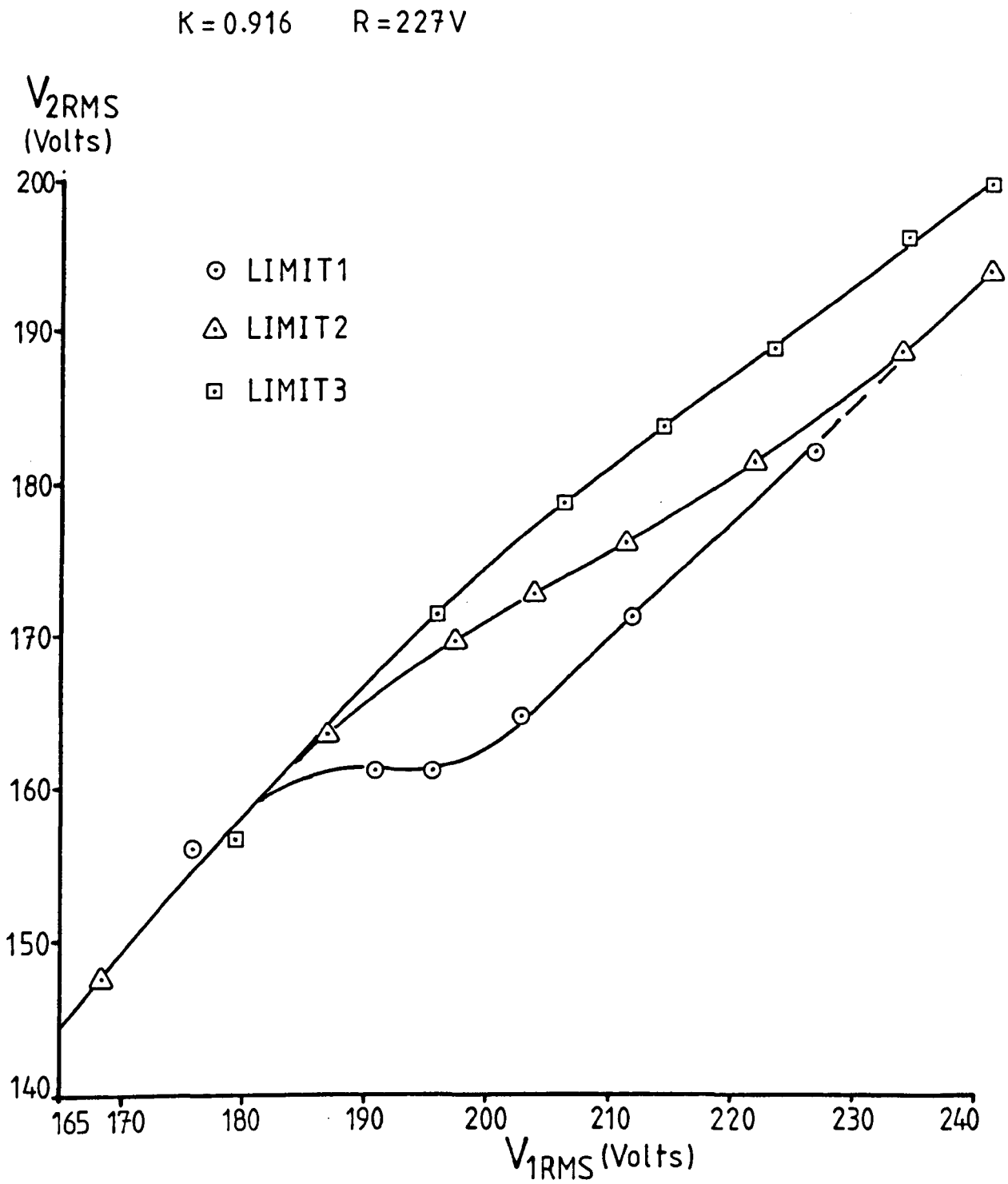


Fig. 5.1 : Measured open circuit TCR voltage characteristic for K=0.916 and varying LIMIT

		Compensator Branch	POSLIM (Hexadecimal)	NEGLIM
LIMIT 1	$\alpha \simeq 100^{\circ}$	Branch 1	0018	0020
		Branch 2	0040	0040
		Branch 3	0040	0040
LIMIT 2	$\alpha \simeq 135^{\circ}$	Branch 1	01A0	0250
		Branch 2	0220	0230
		Branch 3	01F0	0280
LIMIT 3	$\alpha \simeq 170^{\circ}$	Branch 1	03D0	0570
		Branch 2	0440	04C0
		Branch 3	0380	0480

Table 5.1 Integration limits set for 6-pulse TCR compensator performance studies

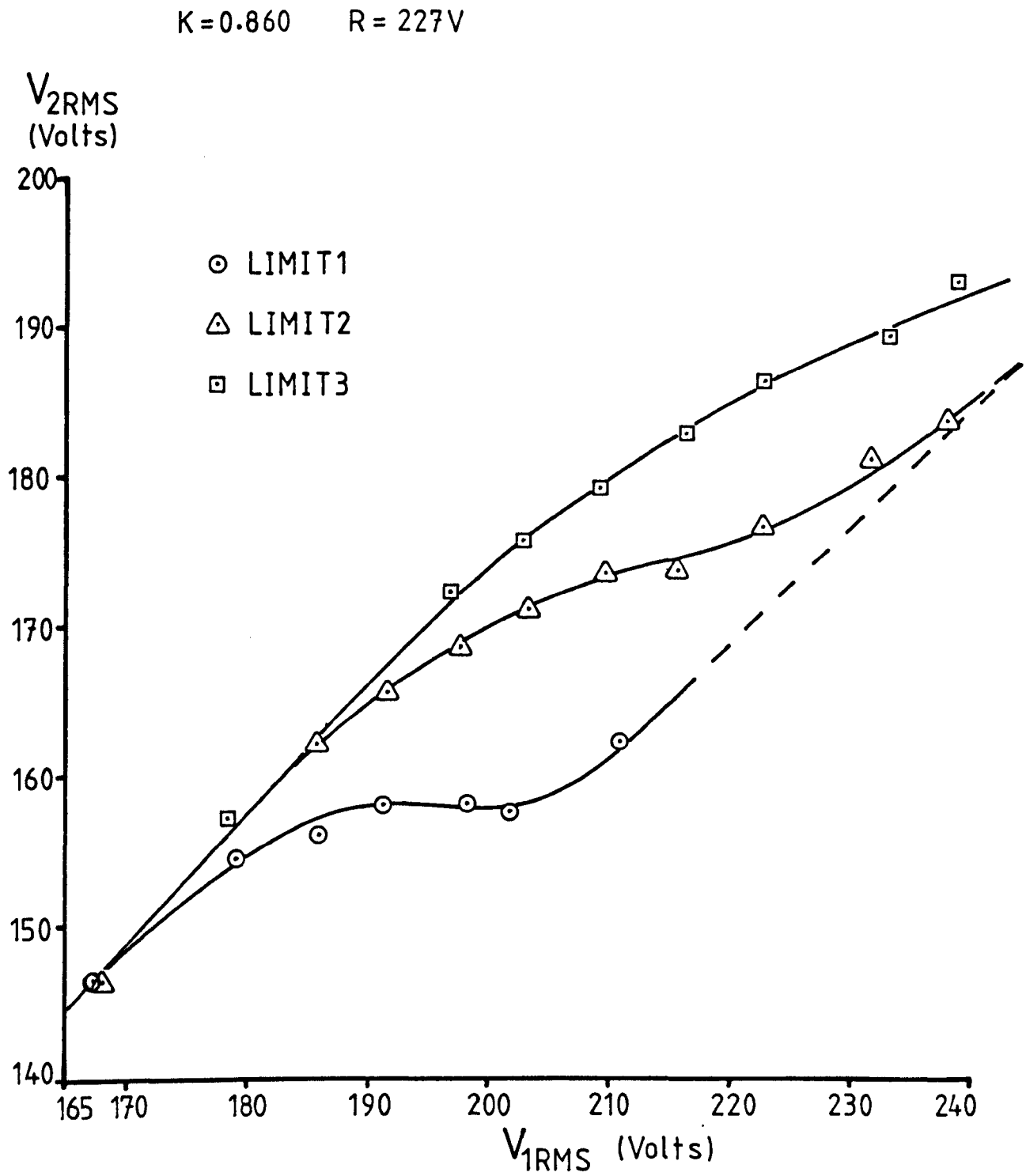


Fig. 5.2 : Measured open circuit TCR voltage characteristics for K= 0.860 and varying LIMIT

The corresponding theoretical values are 1.000 and 0.860, and the results show that increasing the TCR rating affects the control region of the curves such that:

(a) Where the gradient is not zero it is decreased.

(b) Where the gradient is zero, the span of the flat region is increased.

5.1.2 Shunt Load Compensation

A variable three-phase inductance was connected in parallel with the TCR compensator. Varying this load current between zero and approximately 1.4 Amps would act to vary V_2 linearly in the range

$$161 \leqslant V_2 \leqslant 175 \text{ Volts}$$

if there were no TCR compensator acting. The results of connecting the compensator are shown in Figure 5.3. Characteristics are again plotted for each of three values of LIMIT. At $I_2 = 0$, the TCR firing angle α is at a minimum which is set by the value of LIMIT.

i.e. For $I_2 = 0$ and LIMIT = LIMIT1, $\alpha = \alpha_1 \simeq 100^\circ$
For $I_2 = 0$ and LIMIT = LIMIT2, $\alpha = \alpha_2 \simeq 135^\circ$
For $I_2 = 0$ and LIMIT = LIMIT3, $\alpha = \alpha_3 \simeq 170^\circ$

As I_2 is increased, V_2 is depressed and α increases, thus I_{COMP} inversely balances I_2.

Figure 5.3 shows once again that the smaller value of LIMIT is of maximum benefit for voltage control. The shape of the characteristic in the control region is approximately 3.5V/-1.0A = -3.5V/A, although the characteristic is far from linear.

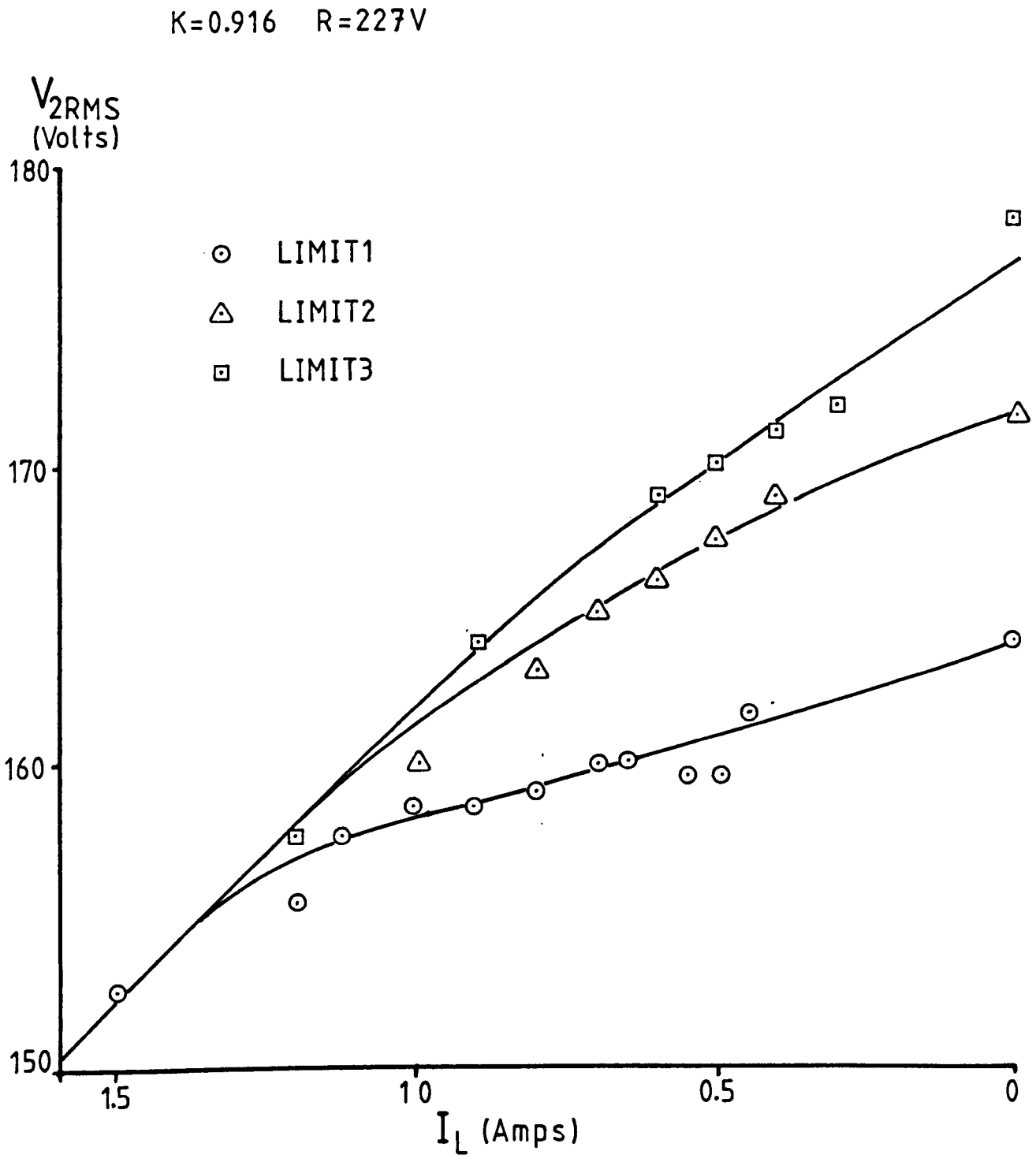


Fig. 5.3 : Measured shunt compensation TCR characteristics for K=0.916 and varying LIMIT

The tests were repeated with the higher rating compensator used in the previous section. The results are given in Figure 5.4, and the main effect of increasing the TCR rating is to decrease the slope of each characteristic in the control region.

The curve for LIMIT = LIMIT1 has an approximate gradient of 2.8V/-1.3A = -2.2V/A. The characteristic within the control region is again far from linear. It was observed that even after careful 'tuning' of each compensator branch, firing angles would vary between each branch by up to ± 10 degrees. This imbalance between the three TCR control systems may contribute to the non-linearities observed in the ideally 'flat' controlled region of the characteristics.

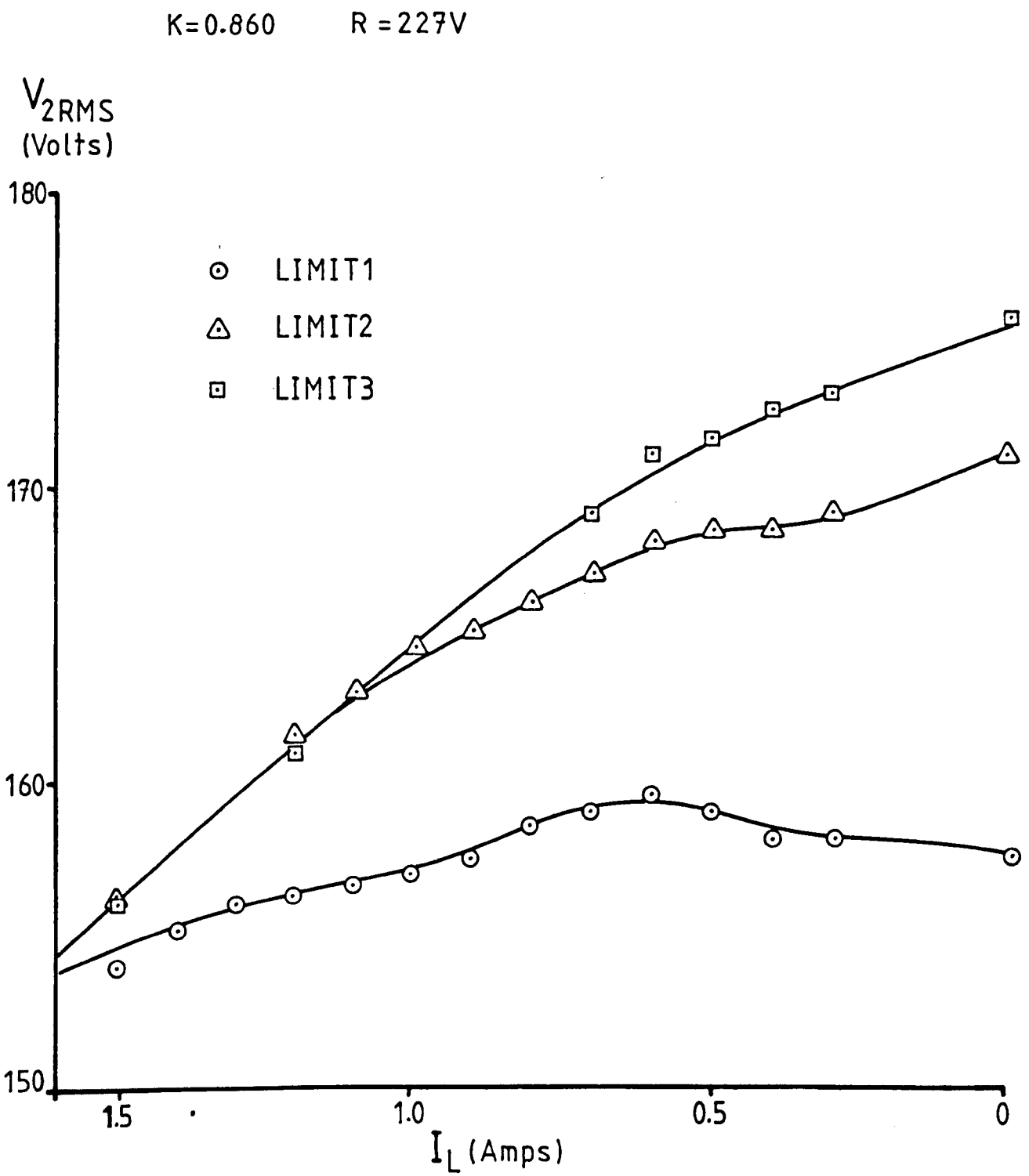


Fig. 5.4 : Measured shunt compensation characteristics for K=0.860 and varying LIMIT

5.2 ANALYSIS OF VOLTAGE DISTORTION

Chapter III used the concept of a 'flicker voltage', V_f, when discussing the distortion of the 50Hz supply voltage waveform. Section 3.1.2 in particular showed how the annoyance effect of V_f was frequency dependent.

The laboratory arc furnace model has been shown to reproduce successfully the wide range of frequency components impressed upon the 50Hz supply waveform at the levels encountered at a real installation (2.4.3).

The laboratory TCR compensator aims to reduce the annoyance effect of the arc furnace model load currents by shunt compensation, thus reducing the magnitude of components of V_f. It is then essential that the results of TCR compensator operation are clear, and that a reliable method for evaluating annoyance levels can be used to demonstrate some improvement factor.

These final points are now discussed in turn.

5.2.1 The Use of Spectral Analysis

The technique of spectral analysis enables the power components of a wide range of frequencies to be evaluated simultaneously. This is particularly useful in the study of the 'flicker voltage', V_f, where the magnitudes of a range of frequency components of the real time signal are of interest.

Methods of obtaining a power spectrum include direct estimation, recurvisve and non-recursive digital filtering[112], mean-lagged products[113], complex demodulation and the discrete Fourier transform. Direct estimation involves the use of special purpose analogue devices such as harmonic analysers, wave analysers and filter banks. Early generations of computers made possible the use of

digital filtering techniques and complex demodulation algorithms. The larger workspace capacity of later computers made the discrete Fourier transform (DFT) practicable, enabling the Fourier series coefficients to be calculated at discrete frequencies[114]. The fast Fourier transform (FFT) is simply an efficient method of computing the DFT of time series data[115,116].

A suite of FORTRAN programs, for the calculation of a Fourier power spectrum, was made available to the author by the Speech Research Group of Liverpool University. Although primarily intended for use in the 20-20,000Hz frequency band, the method of operation allowed them to be modified for use around 50Hz. Appendix G describes the method and gives program listings where necessary. The necessary workspace was only available on Liverpool University's mainframe IBM 4341 computer; data acquisition and transfer was therefore necessary before computational analysis could be carried out (see 5.2.2).

Bogert[117] identifies two important requirements for the use of computational techniques for power spectrum analysis as a laboratory tool. The first is a set of subroutines to enable parameters to be varied at will. The second is adequate display of the output.

Although the mainframe computer more than satisfied both of these requirements, it was found that a commercial power spectrum analyser[118] offered the advantage of an immediate and variable display from an automatic data acquisition process. The digital technology employed in the instrument gave 157 blocks of data in the frequency domain for storage and display. The bandwidth therefore varied as the frequency span was altered. The bandwidth here is the frequency band that contributes to a single point of the discrete power spectrum.

Increasing the bandwidth contributing to each point requires a correspondingly larger block of time series data for analysis. With a fixed sampling frequency the time span for which each power spectrum was calculated would vary between 10 milliseconds and 250 seconds.

The data repetition rate for the arc furnace model was 1.78 seconds, giving a high probability that individual blocks of time series data would differ, with corresponding differences in the power spectrum.

Welch[119] describes an averaging process that may be used for successive power spectra. The Hewlett Packard spectrum analyser allowed such averages to be performed - the displayed power spectrum then being the average of 2^N samples. Using the RMS value of eight successive spectral analyses ensured that the variations within the 1.78 seconds of repeated data would not cause confusing discrepancies in the presentation of the power spectrum.

The Hewlett Packard spectrum analyser included the facility for the output of stored digital data to an X-Y plotter, and the results presented in Section 5.3 were produced by this method.

5.2.2 Data Logging

For analysis of data from the laboratory, it was necessary to transfer recordings from the laboratory equipment to the University's mainframe computer. Here large amounts of data could be stored, retrieved and analysed at will. The spectral analysis package described in Section 5.2.1 was set to operate on 2048 ($=2^{11}$) time series data points from the CEGB recordings. To allow a common analysis routine to be used for computational and laboratory data the time between samples for all time series data for input was set at 800 microseconds - corresponding to the sampling interval used for the CEGB measurements.

This sampling rate gives a Nyquist limit frequency of 625Hz, which more than covers the flicker frequency band. Harmonic frequencies up to the eleventh harmonic of 50Hz will also be recorded accurately. A further SDK-88 microprocessor system was used to undertake all data logging from the laboratory equipment.

Such a system was used because it could easily be incorporated into the system established for programming the TCR control SDK-88s from the Departmental Microprocessor Laboratory's development system. The 8088 processor posessed a 16-bit data highway, allowing high accuracy data handling, and the 20-bit address bus could give access to up to 1M 16-bit words.

Twelve-bit analogue to digital converters (ADCs) were used, giving a quantisation noise threshold of -72dB in the time domain. This would enable high-accuracy studies of recorded data to be carried out on the mainframe computer. The program listings for the sampling program is given in Appendix H.

The sampling process was initiated by a 10 microsecond pulse output from the AIM-65 system (Appendix D) in synchronism with the first point in the 1.78 second data cycle. The sampling SDK-88 detected this pulse on 8-bit ADC addressed at F800, and then executed a 3-channel, 800 microsecond sampling loop 2225 times.

The stored data could then be uploaded from the SDK-88 memory to a data file on the Tektronix 8650 MUSDU, for transfer by IBM 3470 format floppy disc to the IBM mainframe computer.

The 12-bit ADCs proved to be more susceptable to temperature effects than were the 8-bit ADCs used for the TCR control scheme. Re-calibrating the sampling circuitry proved to be time consuming and tedious. The problem was solved by preceeding the sampling program by a short block which interactively sampled each ADC three times for each of three externally applied voltages: Positive Full Scale Deflection (FSD), ZERO and Negative FSD. Thus each block of data would always be accompanied by digital samples of known reference voltages - enabling absolute sampled values to be calculated computationally.

The 12-bit ADC and sampling circuitry are shown in Appendix H after the sampling program.

5.3 TCR PERFORMANCE WITH THE ARC FURNACE MODEL

The TCR compensator was connected in parallel with the laboratory arc furnace model - at the point shown as 'B' in Figure 3.8. Disturbances of the line voltage waveform at the point of coupling produced varying firing angles in each branch of the TCR. The effect of the TCR compensator operation may be studied both in the frequency domain and in the time domain.

The values of integration limit, LIMIT, set for different sets of results were given in Table 5.1.

5.3.1 Frequency Domain Study of Compensator Action

Section 5.2 showed the advantages of using spectral analysis techniques for the examination of distorted waveforms where a range of frequency components are of interest.

Figures 2.26, 2.27 and 2.28 gave the power spectral density of the supply voltage with and without the arc furnace model operating. The power levels of frequencies modulating the 50Hz 'carrier' are obtained by the summation of the components in the upper and lower sidebands. The arithmetic sum of the power in all modulating frequencies is then the power component of the 'flicker voltage' V_f. The frequency components of V_f that are of primary interest are those in the range 0-30Hz. These then occur in the absolute frequency range 50Hz ± 30Hz, i.e. $20\text{Hz} \leqslant f \leqslant 80\text{Hz}$. For some flicker improvement factor to be obtained, it was necessary that the TCR compensator reduce the level of disturbances within this particular frequency band.

The results show the power spectra of the distorted voltage waveforms in dB. A change in level of 6dB at a particular frequency represents a change in voltage ratios by a factor of two. -6dB is therefore one half of the relative voltage level, and +6dB is double the relative voltage level, at the chosen frequency.

All plots of power spectra showing TCR compensator action are shown with the uncompensated distorted voltage plotted on the same axes. The compensated power spectrum is shown as a fine line, to be compared with the heavier line plotted to show the uncompensated spectrum.

The areas where a reduction in power was achieved by the TCR compensator are shaded so that the regions of attenuation may be more easily compared with any regions of amplification. This form of presentation also highlights the 'cross-over' frequency between amplification and attenuation.

Figure 5.5 gives a comparison of the line voltage power spectral density with and without the operation of the TCR compensator. All results presented in this form give the uncompensated line voltage power spectrum as a heavy line, and the compensated line voltage as the lighter line.

If the plots are studied in isolation from each other, differences between them are not immediately clear. Presenting dual plots on the same axes allows comparisons to be made, and the effects of changing TCR compensator control parameters are now studied.

(i) LIMIT = LIMIT1, R = 226.9, K = 0.916

Figure 5.5 shows the power spectrum of the line voltage V_R-V_Y.

A reduction in the power of components in the absolute frequency range 20Hz-90Hz is evident, but the details of such improvement lack clarity.

Figure 5.6 shows only the lower sideband of Figure 5.5. The power in modulation frequencies 0-30Hz (absolute frequencies 50-20Hz) is reduced by the compensator by between 0 and -6dB.

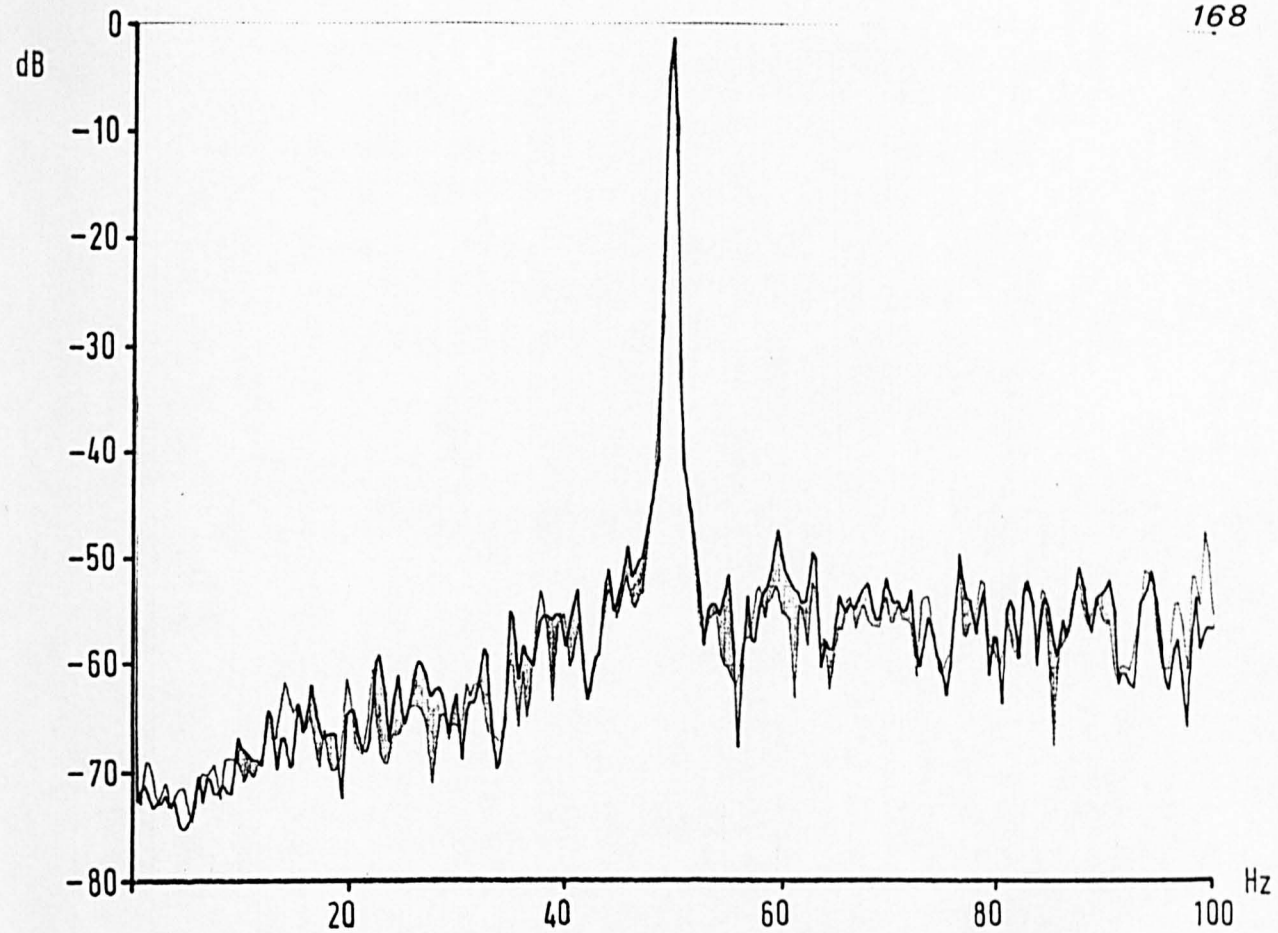


Fig. 5.5 : 0-100Hz power spectrum of Vry for K = 0.916, LIMIT 1

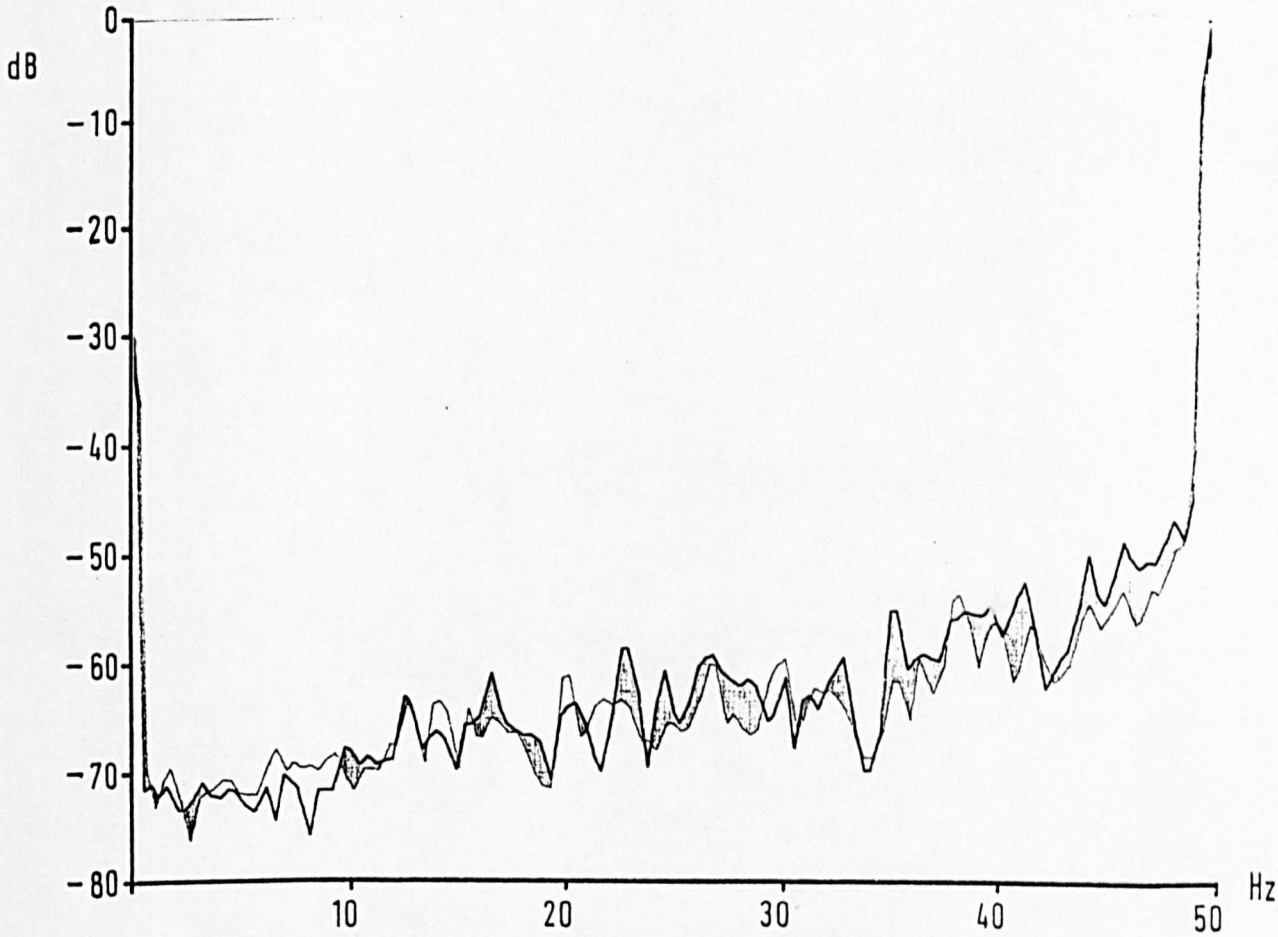


Fig. 5.6 : 0-50Hz power spectrum of Vry for K = 0.916, LIMIT1

The 'cross-over frequency' where the compensator acts to increase rather than attenuate is at a modulation frequency of approximately 35Hz (15Hz and 85Hz absolute). What can be seen from the upper sideband in Figure 5.5 would suggest a similar if not better performance. The higher frequency effects are shown in Figure 5.7 with the V_{RY} line voltage power spectrum to 500Hz.

The changes in harmonic power amplitudes due to the TCR compensator are:

3rd Harmonic : +4dB
5th Harmonic : -4dB
7th Harmonic : +2.5dB

(ii) LIMIT = LIMIT2, R = 226.9 Volts, K = 0.916

The reduction in the power of frequency components in the 0-30Hz modulation band was far less for this value of LIMIT corresponding to a steady state $\alpha \simeq 135°$.

Figure 5.8 shows the lower 50Hz modulation sideband in detail - the sharper appearance is due to the use of a 300mHz bandwidth, giving higher resolution in the frequency domain. Any improvement due to the TCR compensator operation is always less than 4dB.

The corresponding power spectrum to 500Hz is shown in Figure 5.9. This shows a marked increase in the power of frequency components in the 200Hz-500Hz band for TCR operation.

The effects on harmonic amplitudes of TCR operation are:

3rd Harmonic : 0dB
5th Harmonic : +3dB
7th Harmonic : +3dB

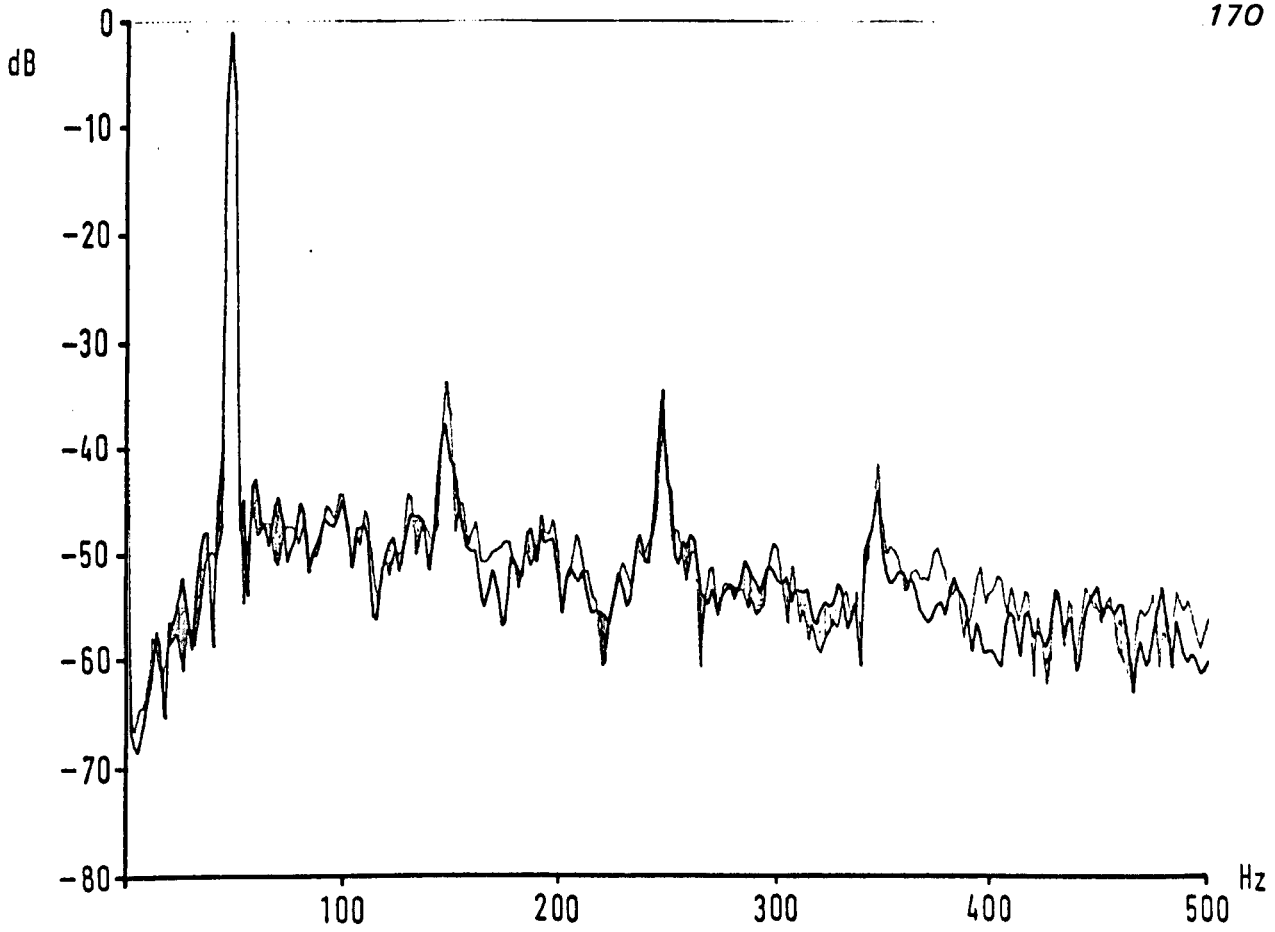


Fig. 5.7 : 0-500Hz power spectrum of Vry for K = 0.916, LIMIT 1

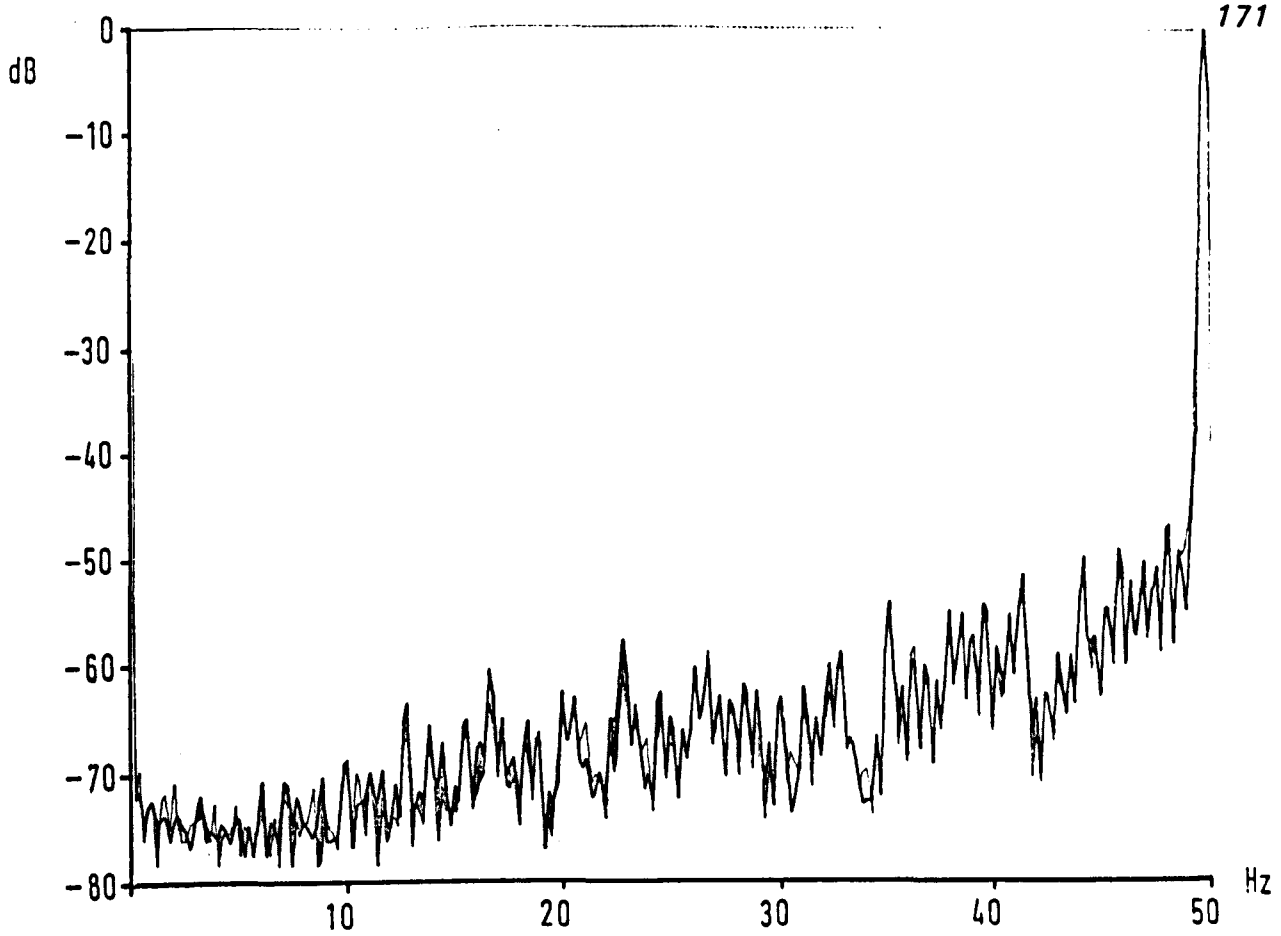


Fig. 5.8 : 0-50 z power spectrum of Vry for K=0.916, LIMIT2

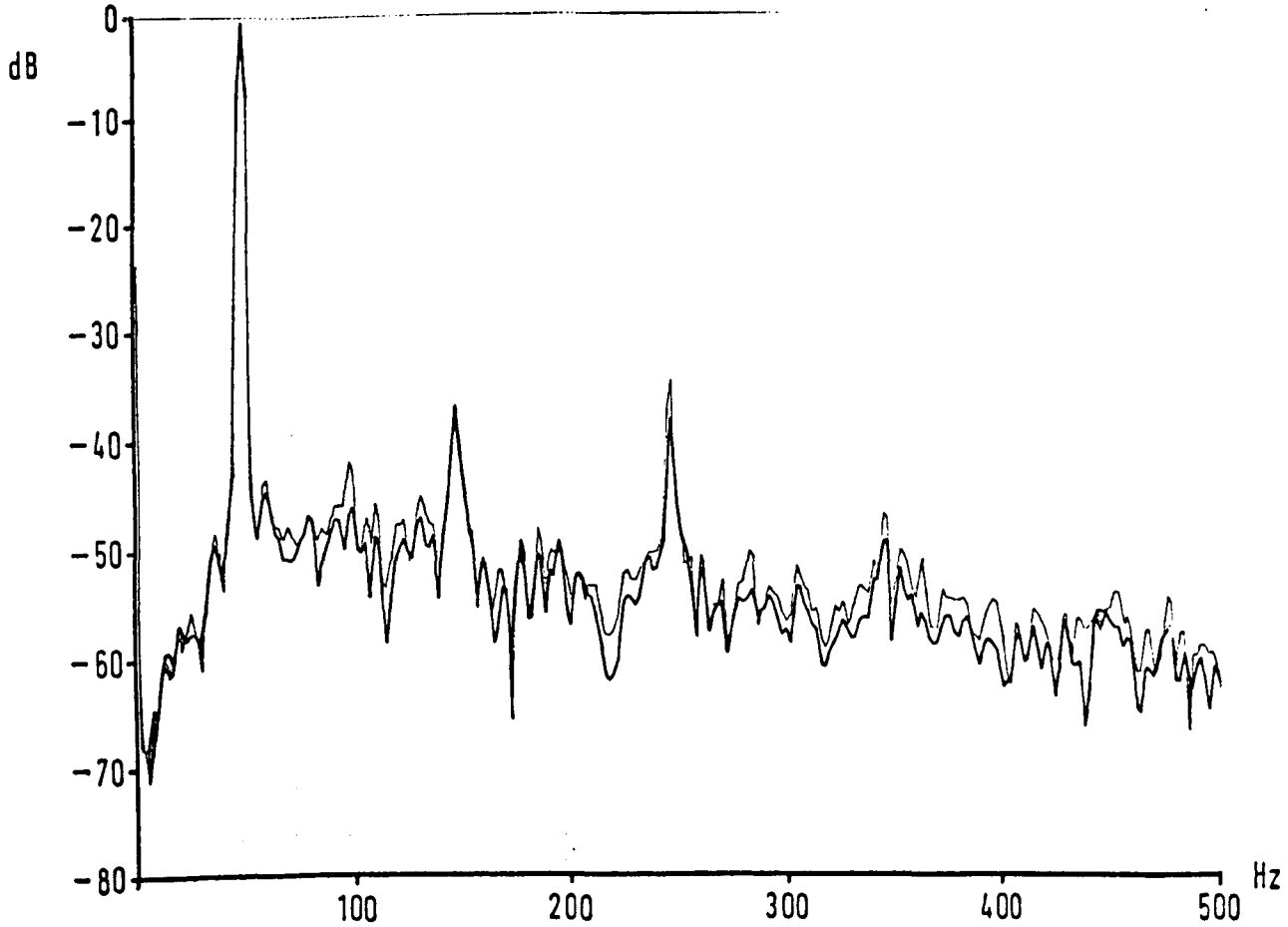


Fig. 5.9 : 0-500Hz power spectrum of Vry for K=0.916, LIMIT2

(iii) LIMIT = LIMIT3, R = 226.9 Volts, K = 0.916

Steady-state sinusoidal tests (5.1) indicate that this value of LIMIT, giving a steady-state $\alpha \simeq 170^{\circ}$, will offer poor shunt reactive compensation.

This is borne out by the results for operation with the arc furnace model, presented in Figures 5.10 and 5.11.

(iv) LIMIT = LIMIT1, R = 226.9 Volts, K = 0.860

This increased rating of the TCR compensator corresponds to that used for the later 'steady state sinusoidal' tests in Sections 5.1.1 and 5.1.2. The three phase rating is 512 VAR corresponding to a C/F value of 1.11 (see Section 5.1.1).

Figure 5.12 shows the line voltage spectrum to 100Hz. Compensator action is particularly marked in the upper modulation sideband, and the cross-over frequency is approximately 20Hz. Figure 5.13 shows that increasing the compensator rating has increased the amplification of frequencies above 100Hz - there are particularly noticeable peaks in the power spectrum at 100Hz and 200Hz, where the amplification is approximately 10dB.

Figures 5.14 and 5.15 indicate some improvement in the attenuation of modulation frequencies up to approximately 25Hz (i.e. $25 \leqslant f \leqslant 75$Hz absolute), but with greater amplification of modulating frequencies between 40 and 50Hz relative to the 50Hz carrier.

(v) LIMIT = LIMIT2, R = 226.9 Volts, K = 0.860

Increasing the integration limit from LIMIT1 to LIMIT2 (see Table 5.2) can be seen from Figures 5.16 and 5.17 to give a large increase in the amplification of modulation frequencies between 40Hz and 50Hz relative to the 50Hz carrier.

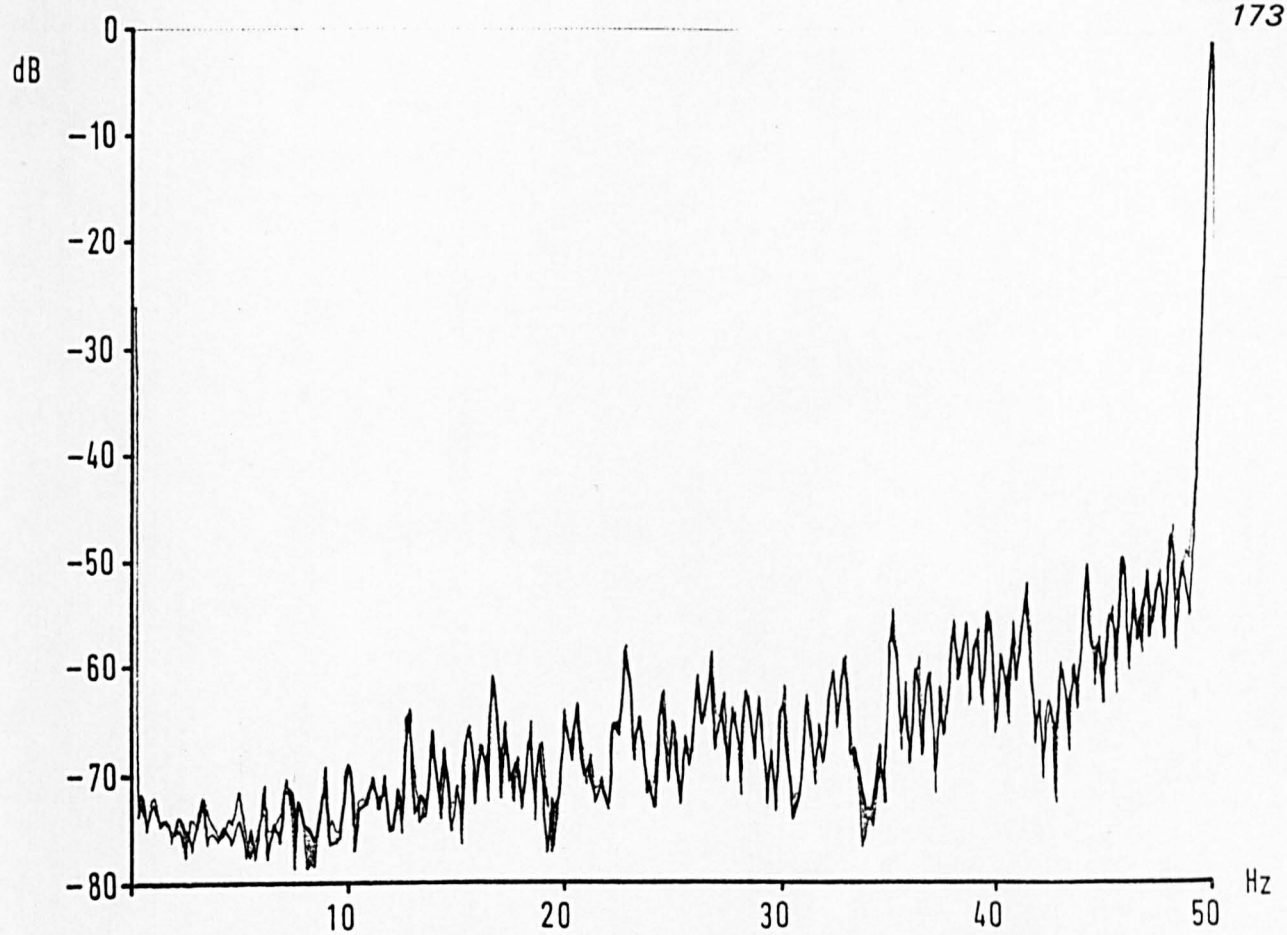


Fig. 5.10 : 0-50Hz power spectrum of Vry for K=0.916, LIMIT3

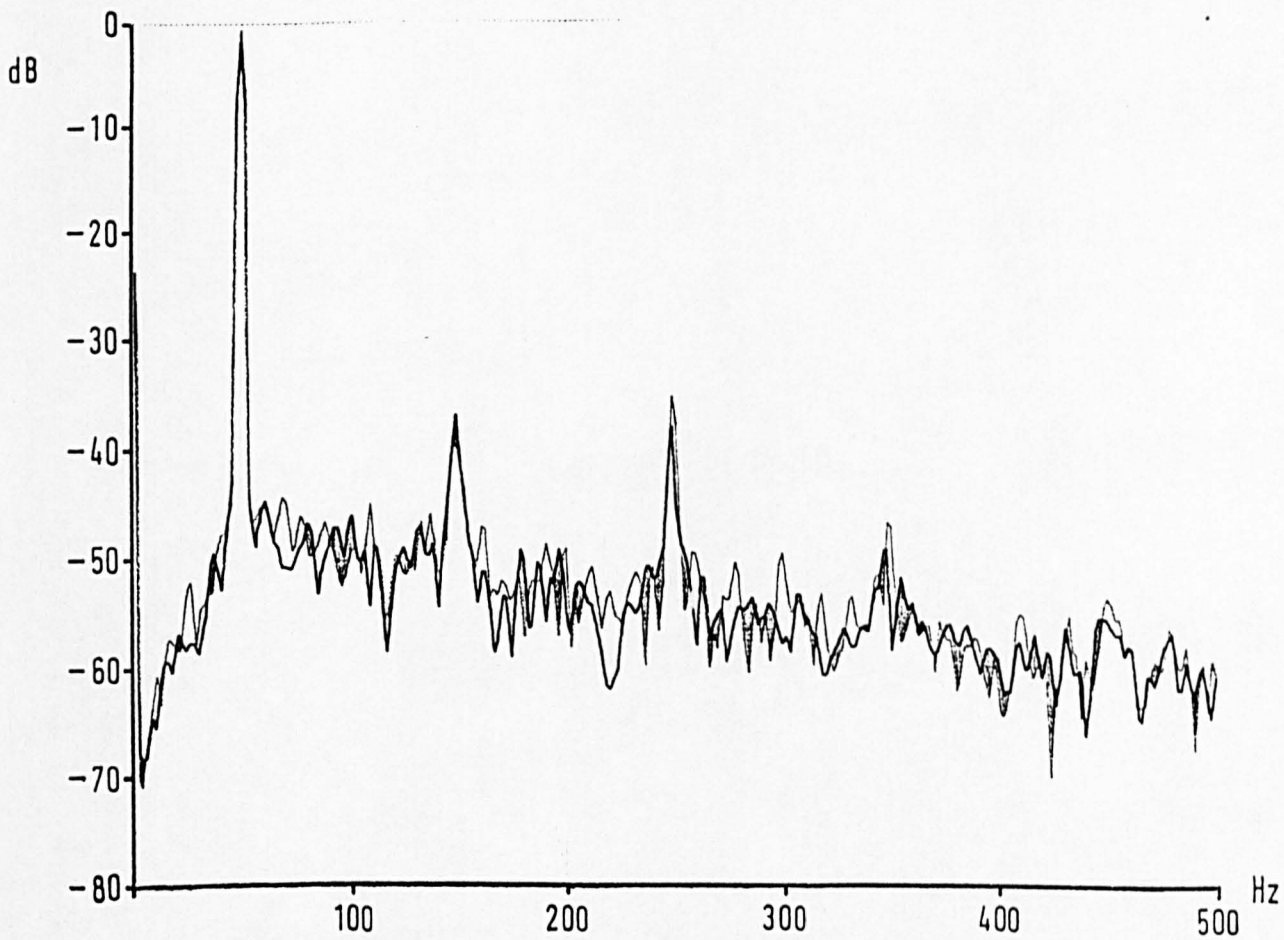


Fig. 5.11 : 0-500Hz power spectrum of Vry for K=0.916, LIMIT3

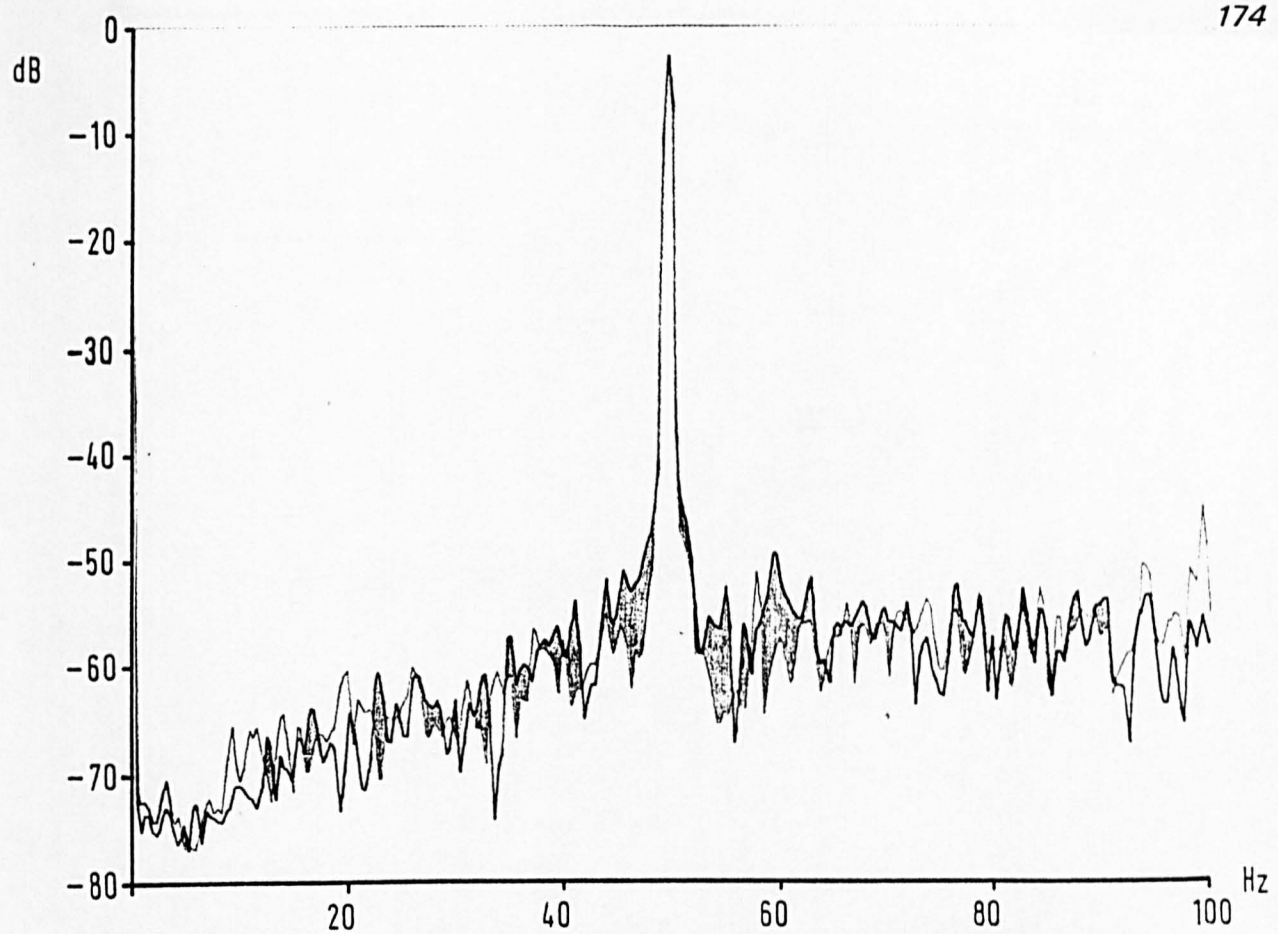


Fig. 5.12 : 0-100Hz power spectrum of Vry for K=0.860, LIMIT1

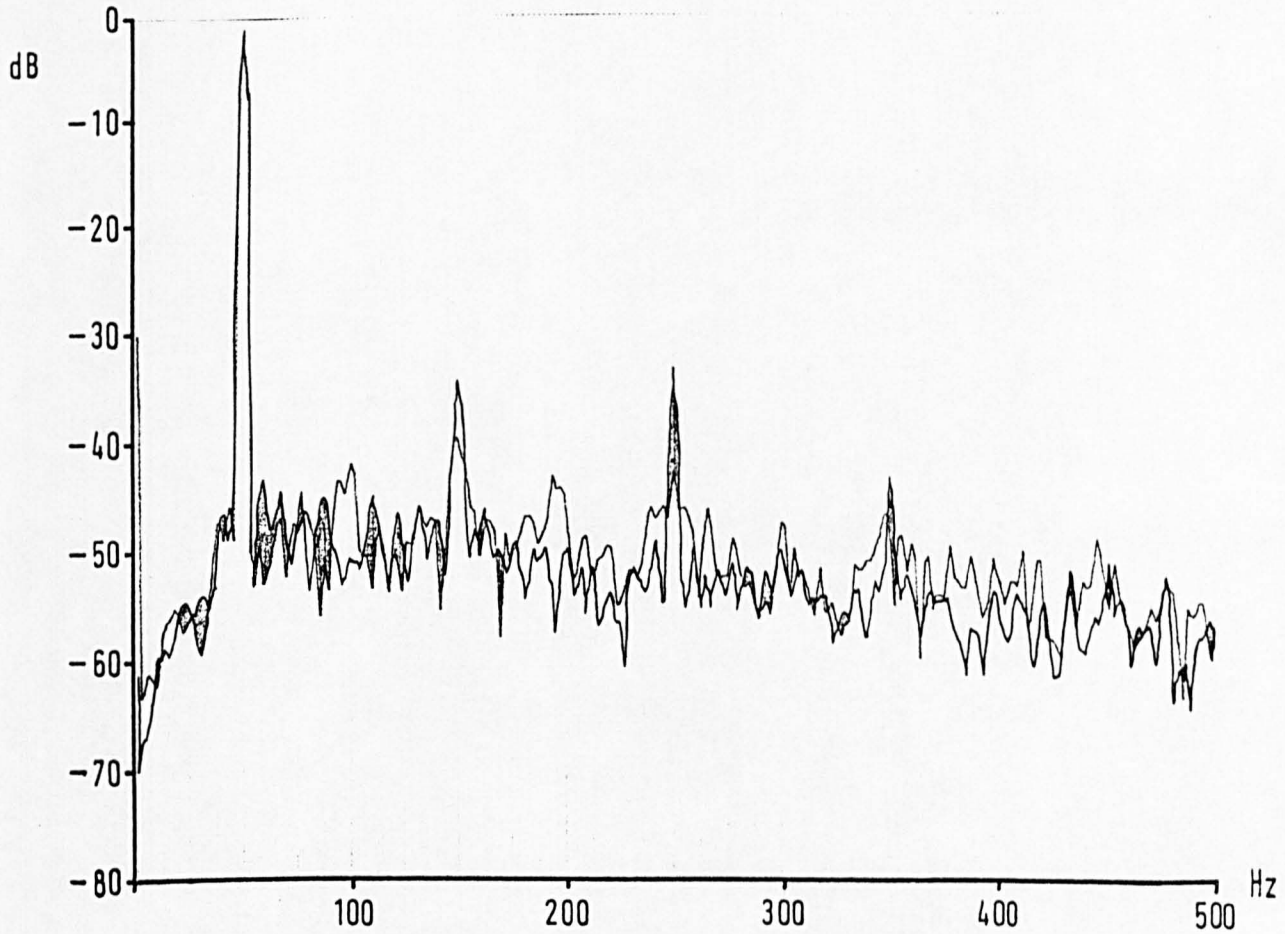


Fig. 5.13 : 0-500Hz power spectrum of Vry for K=0.860, LIMIT 1

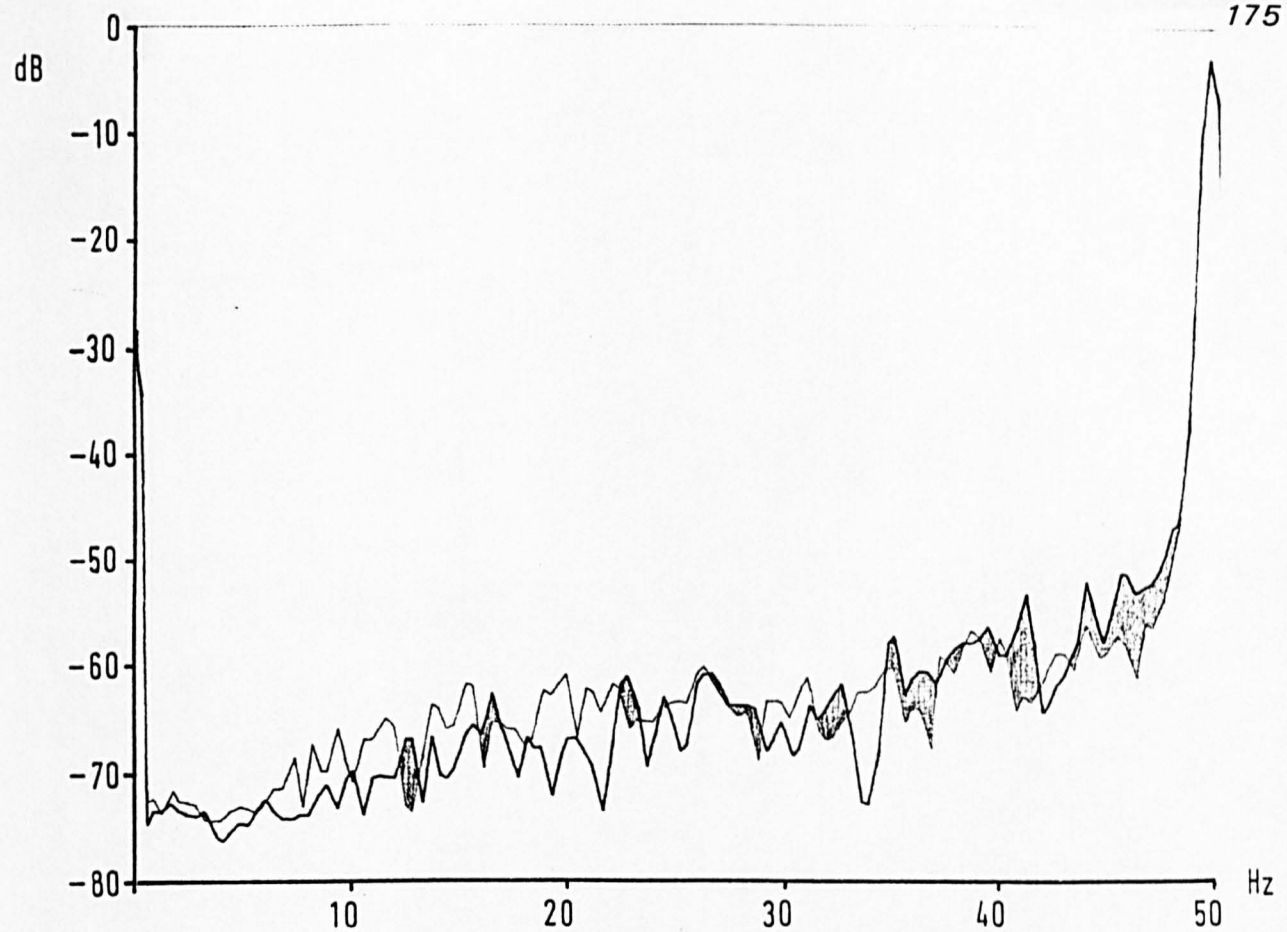


Fig. 5.14 : 0-50Hz power spectrum of Vry for K=0.860, LIMIT 1

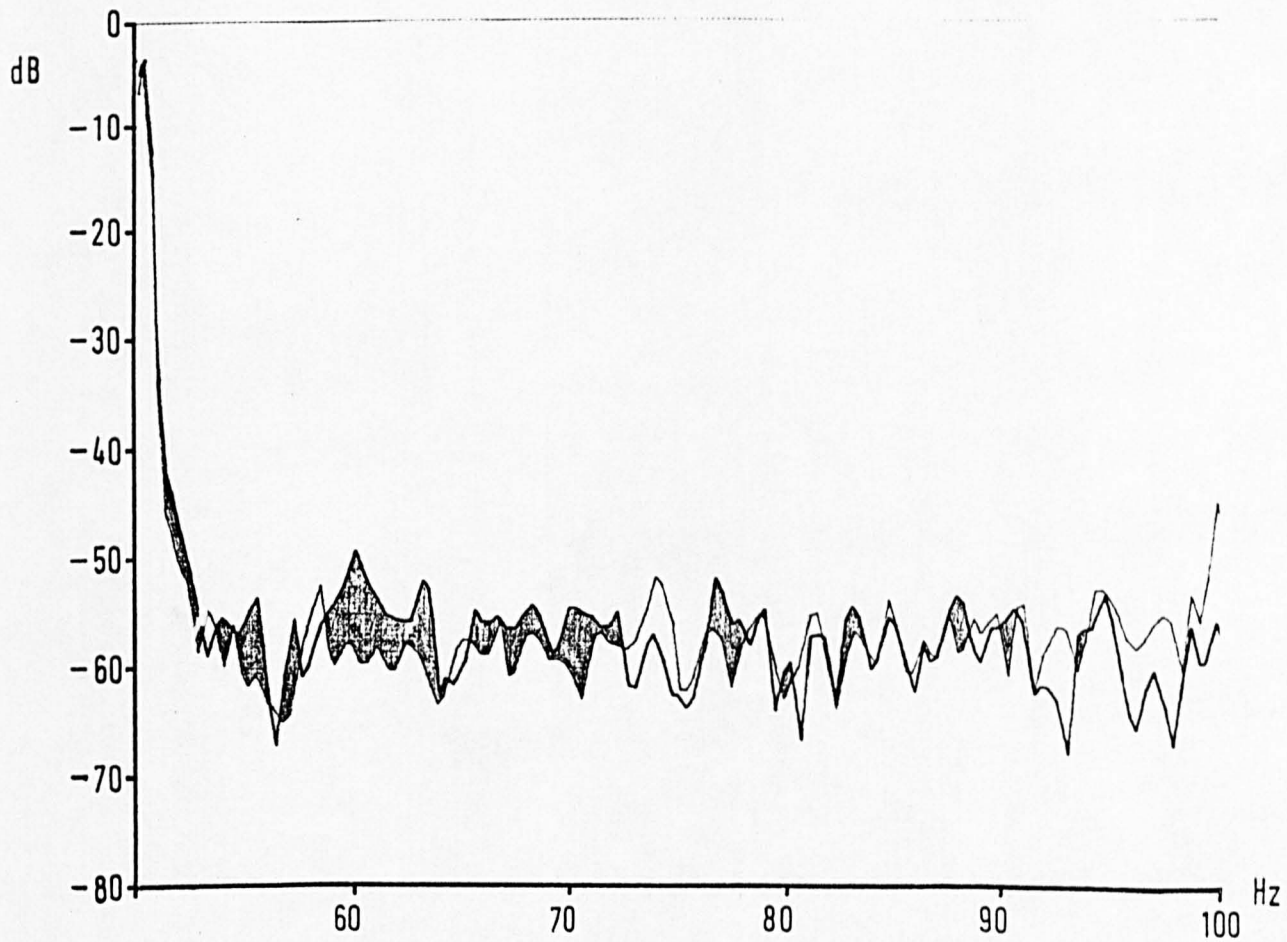


Fig. 5.15 : 50-100Hz power spectrum of Vry for K=0.860, LIMIT 1

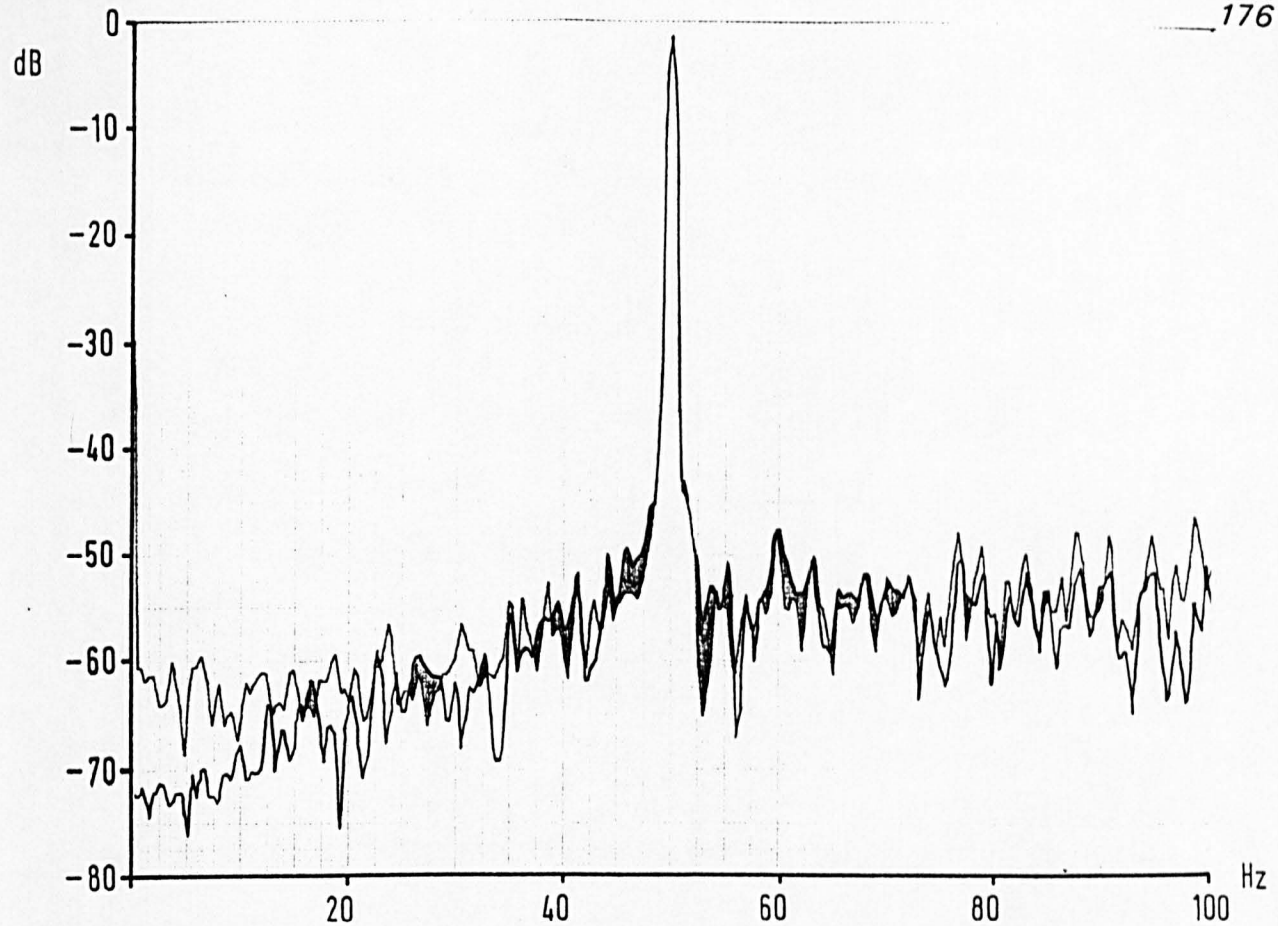


Fig. 5.16 : 0-100Hz power spectrum of Vry for K=0.860, LIMIT2

The cross-over frequency is unchanged at approximately 25Hz. The 'flicker band' attenuation is lessened but it is still noticeably better than that obtained with K = 0.916 (Figure 5.8).

The power spectrum to 500Hz in Figure 5.18 highlights the amplification at 100Hz and 200Hz absolute, and shows general broadband amplification similar to that found for K = 0.916 (Figure 5.9).

(vi) LIMIT = LIMIT3, R = 226.9 Volts, K = 0.860

The change in the power spectrum due to TCR operation is once again extremely slight for the large integration limit. Figures 5.19 and 5.20 show an almost identical power spectrum to that obtained with K = 0.916 (Figures 5.10 and 5.11), with possibly greater amplification of absolute frequencies less than 10Hz.

5.3.2 Time Domain Study of Compensator Action

The depression of the line voltage due to TCR operation is illustrated in Figure 5.21. The three line voltage waveforms at the point of compensator connection are shown, but the plots are not synchronous and aim only to show the distortion of the 50Hz supply waveform due to TCR conduction. The varying firing angle is shown clearly for one branch of the compensator in Figure 5.22, and the corresponding laboratory line voltage, V_B-V_R, at the point of compensator connection is shown above the current trace. The time t = 0 for Figure 5.22 is fixed by the pulse output from the AIM-65 system at the start of each furnace model data cycle.

The same pulse fixed t = 0 for each trace of Figure 5.23 which shows the TCR compensator branch currents when connected in parallel with the arc furnace model.

Only 0.2 seconds of the full 1.78 second data cycle are shown in the interests of clarity. However, the independent phase angle control of each TCR branch is clear, with variation of the conduction angle over the full working range.

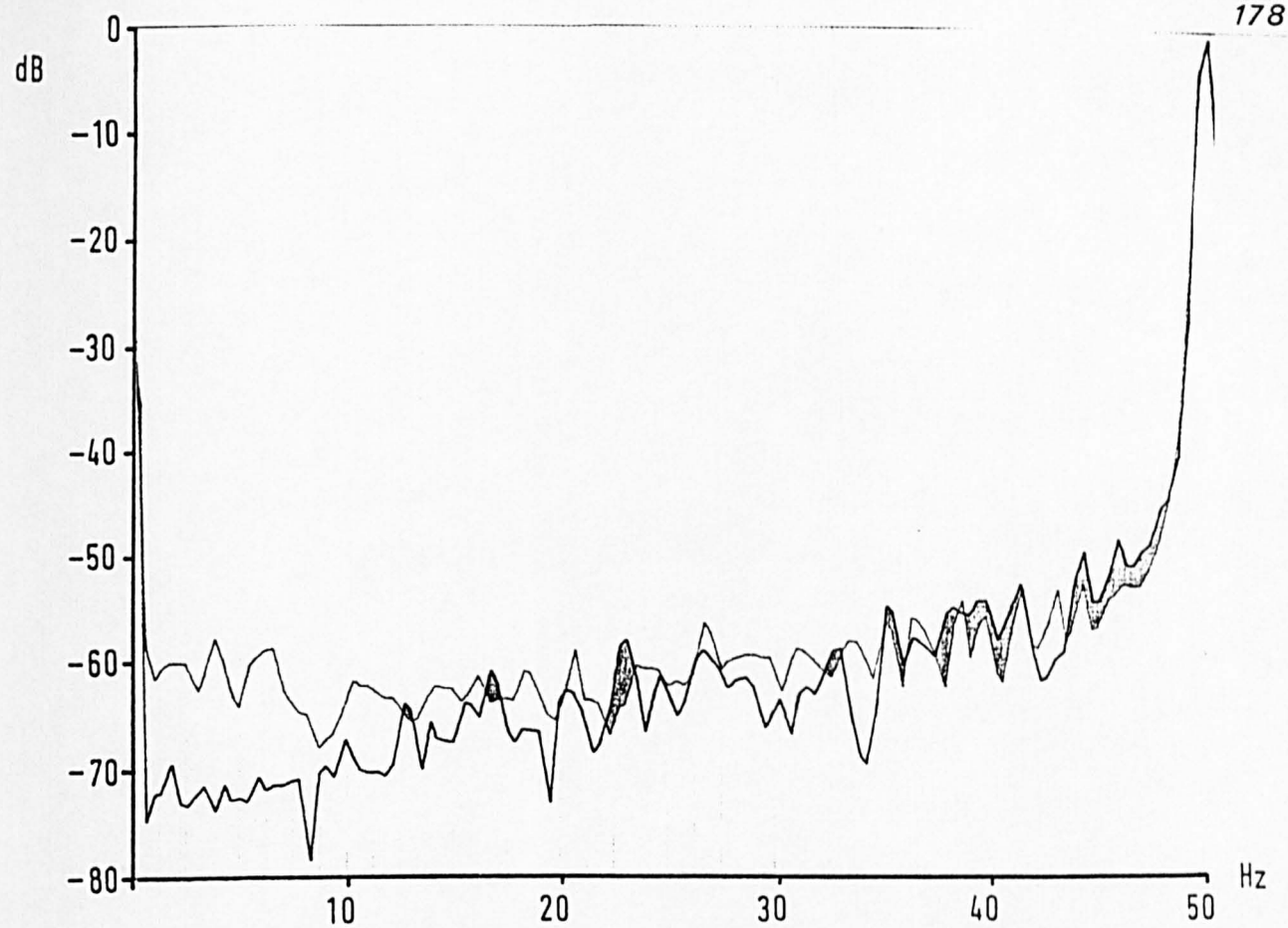


Fig. 5.17 : 0-50Hz power spectrum of Vry for K= 0.860, LIMIT2

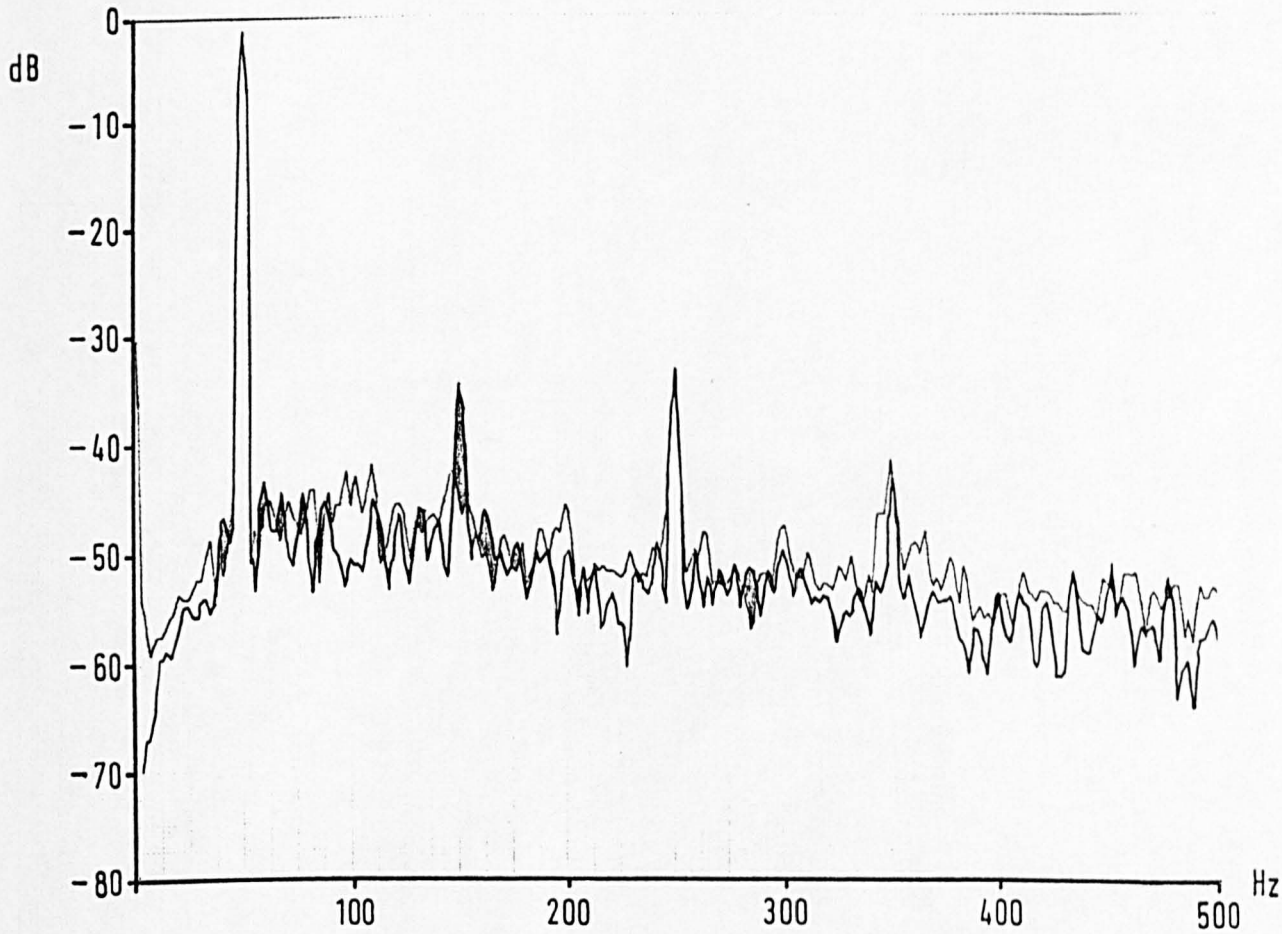


Fig. 5.18 : 0-500Hz power spectrum of Vry for K= 0.860, LIMIT2

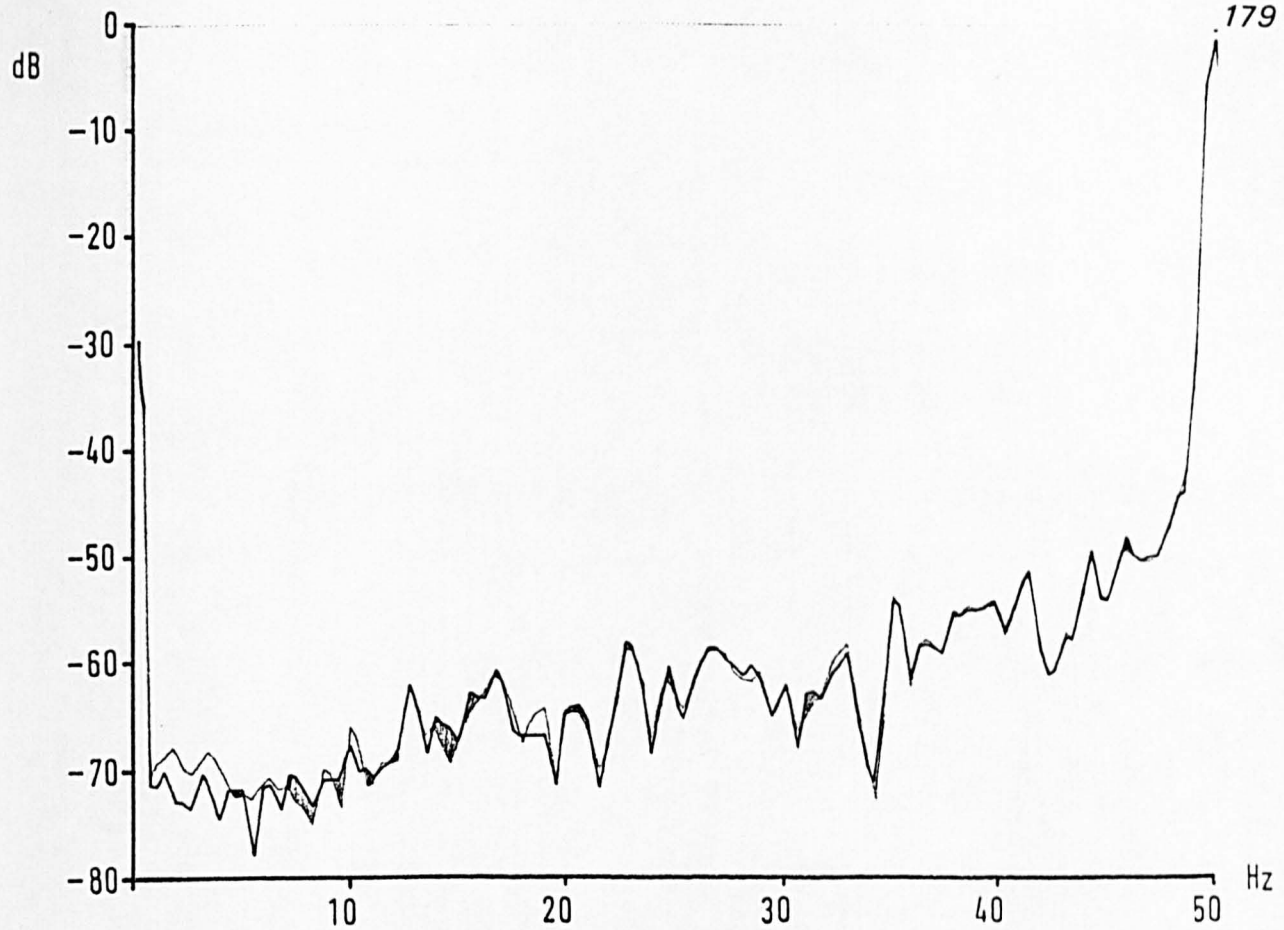


Fig. 5.19 : 0-50Hz power spectrum of Vry for K=0.860, LIMIT3

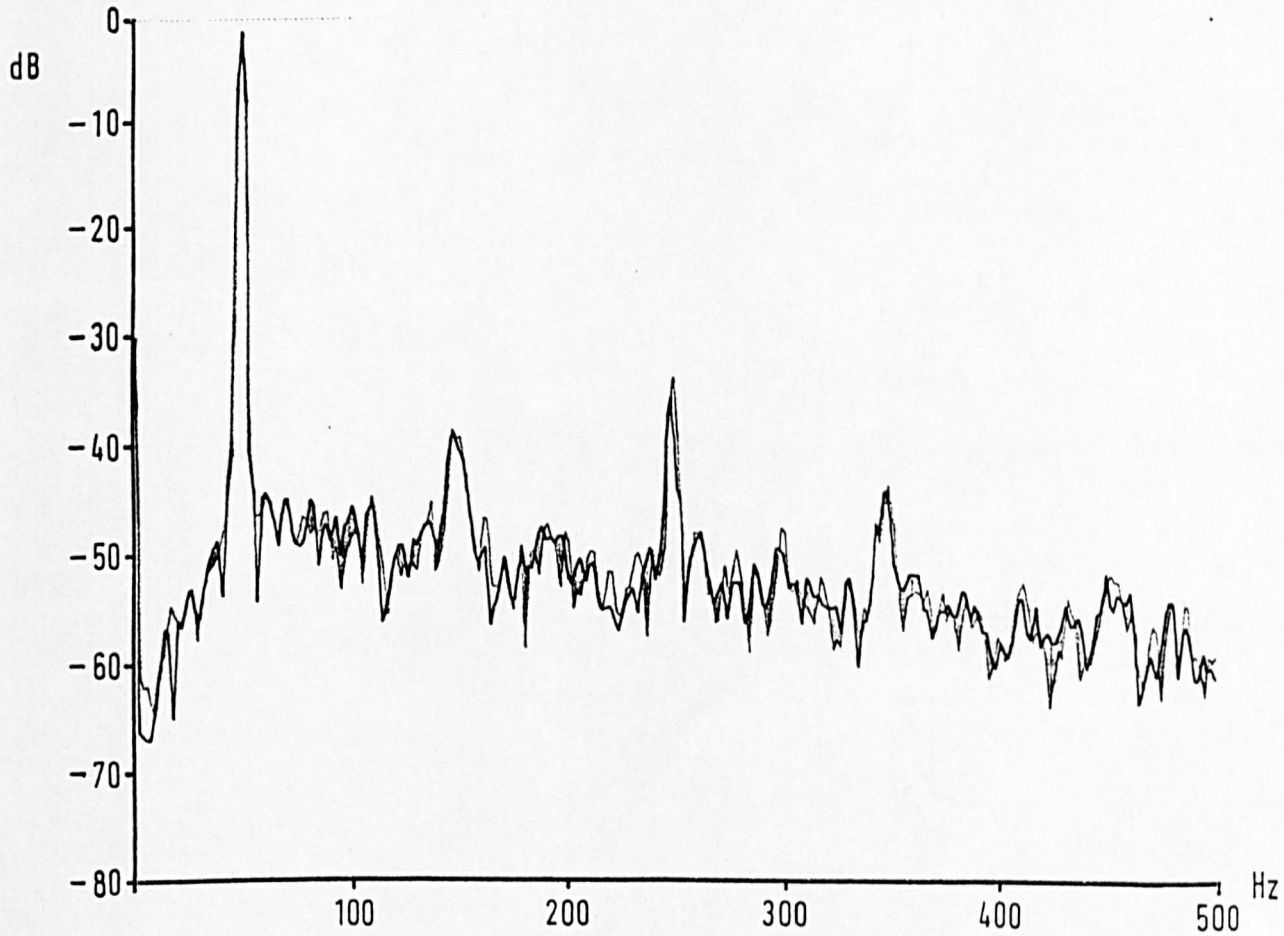


Fig. 5.20 : 0-500Hz power spectrum of Vry for K=0.860, LIMIT3

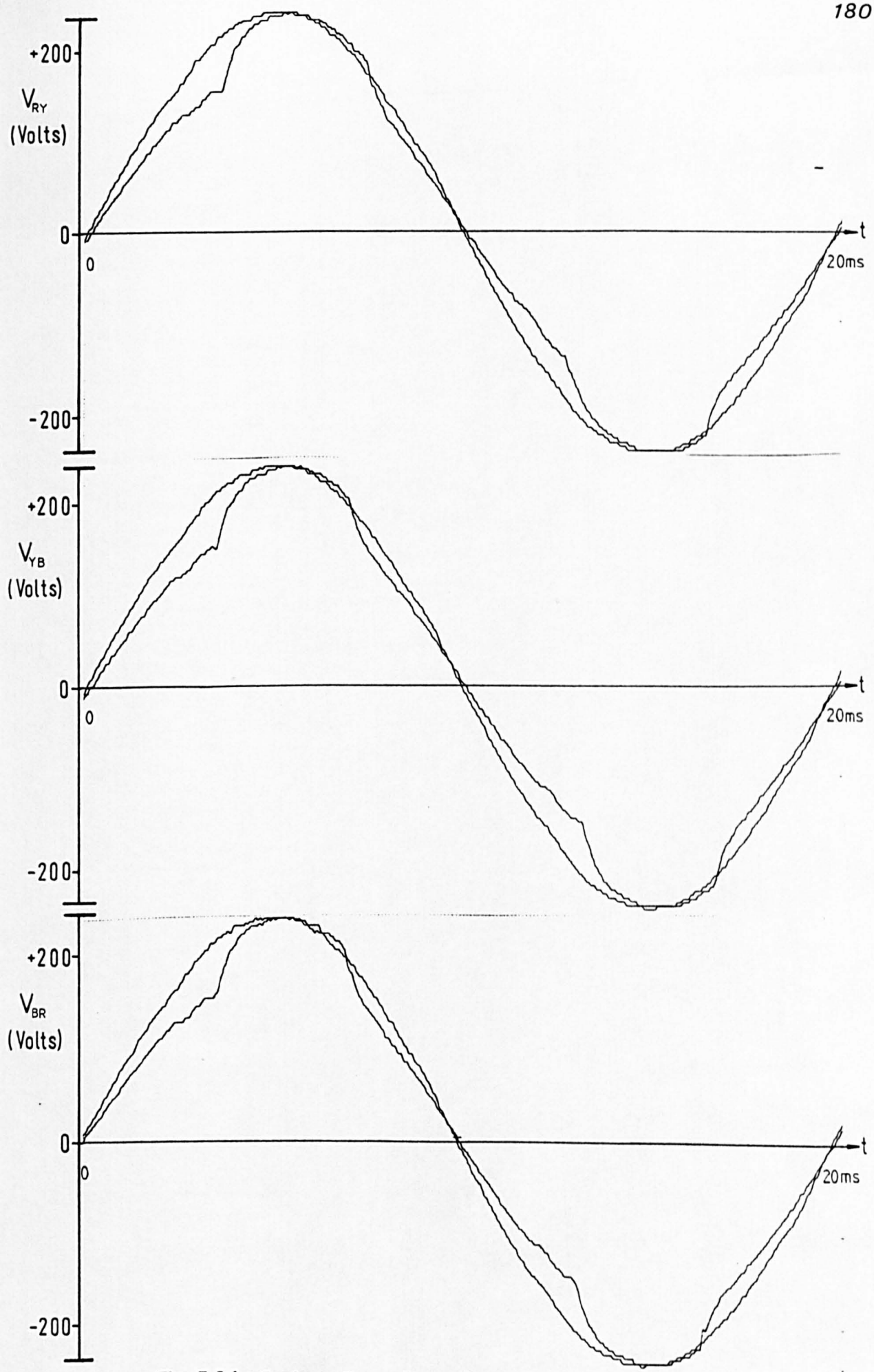


Fig. 5.21 : 3-phase line voltage depression due to TCR switching

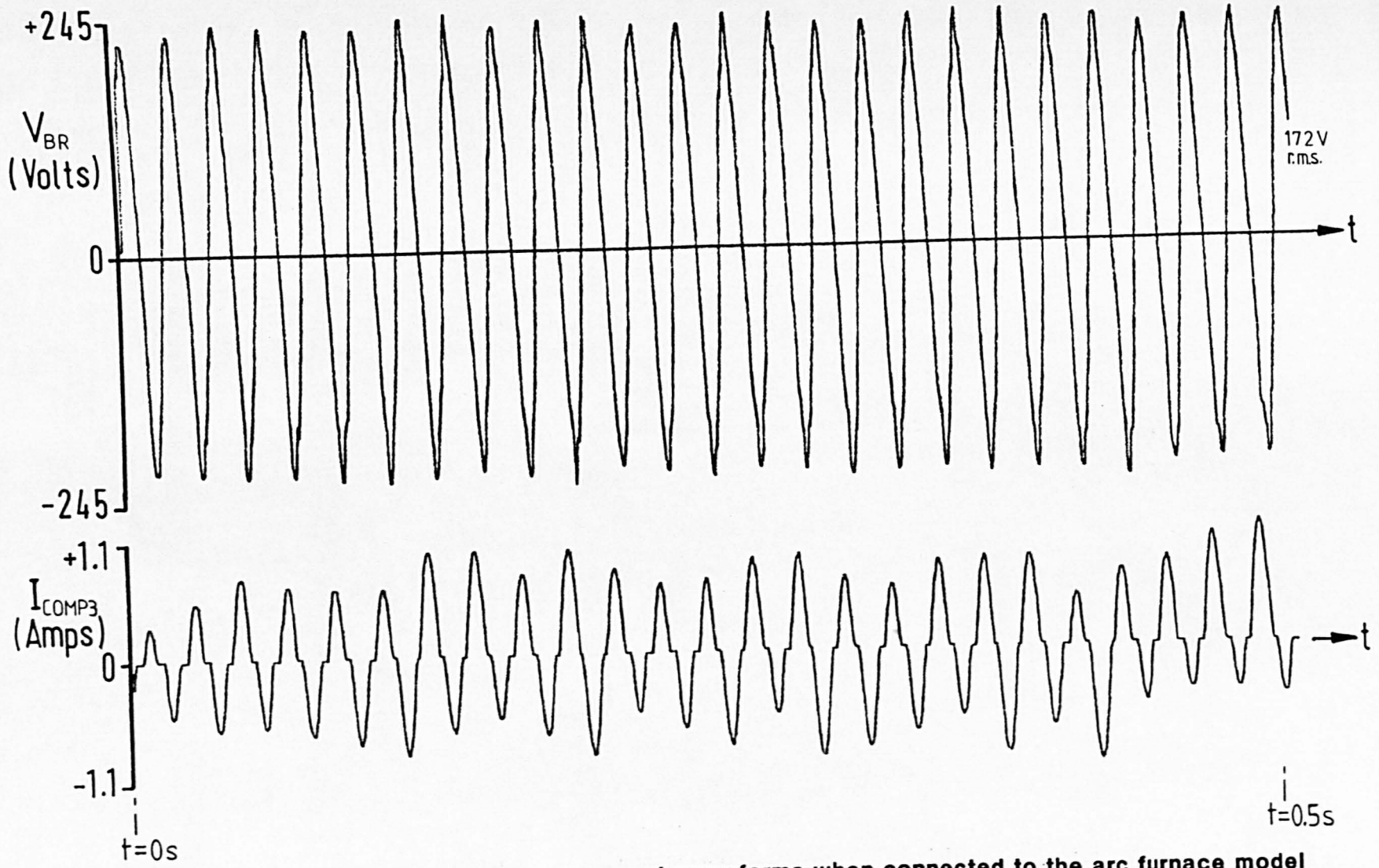


Fig. 5.22 : TCR branch voltage and current waveforms when connected to the arc furnace model

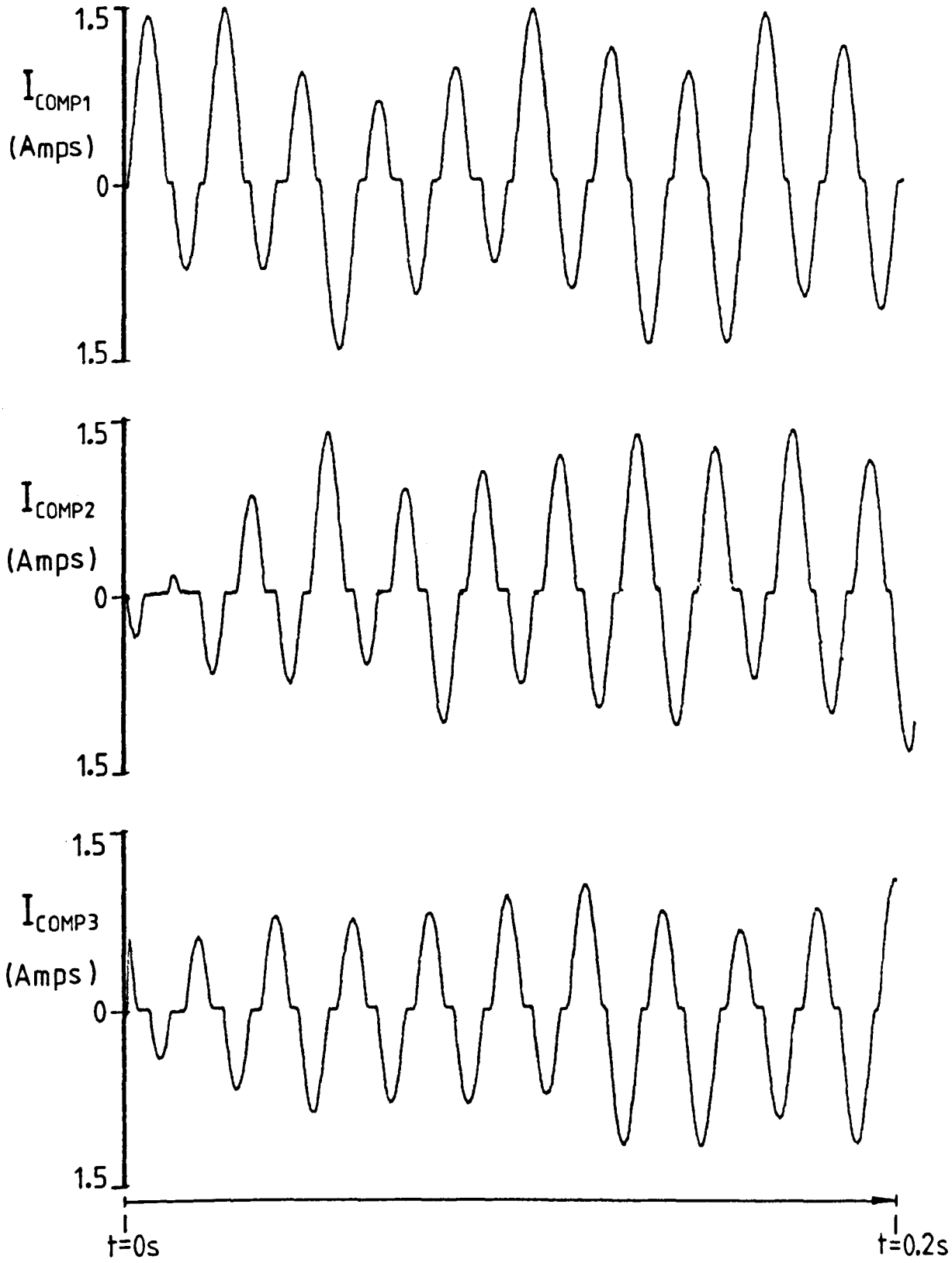


Fig. 5.23 : TCR three-phase branch currents when connected to the arc furnace model

5.4 ESI FLICKERMETER STUDIES

Spectrum analysis has been shown to be a suitable tool for the comparison of compensator performance in different frequency bands (see Section 5.3.1). However, this thesis has not yet related the measured magnitudes of frequency components to the 'annoyance level' described in Section 3.1.3. A comparative study in the laboratory must at some stage be judged in absolute terms.

5.4.1 The Use of the Digital Flickermeter

In the United Kingdom the CEGB and the Electricity Council worked closely with the UIE disturbances committee to find a method for accurately assessing the flicker annoyance factor of a distorted supply voltage waveform. The result of this work was a UIE digital flickermeter, first shown and described at the IEE Third International Conference on Sources and Effects of Power System Disturbances in May 1982.

Its measurement method has been accepted as a standard[20], and it is now being used widely for monitoring both flicker and voltage harmonics. Only a brief description of its operating method will be given here - more detailed treatments are available elsewhere[16].

A Digital Equipment Corporation (DEC) LSI 11/23 minicomputer controls all sampling, digital processing and outputs. Fourteen-bit digital samples are made at the rate of 300 per second. Analogue signal conditioning circuits demodulate the supply waveform and weight V_f to simulate the lamp and eye response. The time series output is sampled 75 times each second.

A cumulative probability function (CPF) is then constructed for the selected one of five ranges. Each range spans 200 classified levels, thus:

Range 1 constructs a CPF from 0.05-10
Range 2 constructs a CPF from 0.5-100
Range 3 constructs a CPF from 5-1,000
Range 4 constructs a CPF from 50-10,000

The CPF is evaluated after each ten minutes, and also as a running average.

Thus probability levels

e.g. $P_{0.1}$, $P_{1.0}$, $P_{3.0}$, $P_{10.0}$

may be evaluated, giving the classified level that was exceeded for 0.1, 1.0, 3.0, 10.0 per cent of the time.

The Electricity Council's Engineering Recommendation P7/2 used only $P_{1.0}$ to give a 'guage point fluctuation voltage' V_{fg}. The UIE Disturbances Study Committee has since agreed that a combination of different probability levels is required to give a representation of the 'flicker severity factor' P_f [19,20].

P_f is calculated for three levels of flicker severity:

(a) Annoyance
(b) Perceptible
(c) Visible

A factor of 1.0 for one of these levels would indicate that the measured disturbances were JUST annoying, perceptible or visible. A factor of 10.0 would indicate that the disturbances were ten times worse than just annoying, perceptible or visible.

5.4.2 Arc Furnace Model without TCR Compensator

In order to obtain 'reference' disturbance levels for the effect of the laboratory arc furnace model operating without a compensator, the ESI flickermeter was left connected to the point corresponding to point B in Figure 3.9. The arc furnace model was continously operated at its normal rating, and the TCR compensator was disconnected.

The displayed results are given in Table 5.2. The values tabulated opposite probability levels P_{XX} are the classified levels described in Section 5.4.1. The values P_{MEAN} and P_{SD} have no meaning for flicker severity, but P_{MEAN} may be treated as a number representative of power.

The important values are those opposite 'annoyance', 'perception' and 'visible'. Thus the flicker voltage at point B (see Figure 3.9) is 10 times more severe than 'just annoying', and 15 times worse than 'just perceptible' or 'just visible'. The measured values do not change between calculations for the 1 minute, 10 minute or overall levels because the model is repeating identical data every 1.78 seconds. Thus even the 10 second uppercentile level is constant.

5.4.3 Arc Furnace Model with TCR Compensator

The compensator control was set to have parameters identical to those which indicated the best performance from Section 5.3.2.

These parameters were:

LIMIT = LIMIT1 (see Table 5.1)
R = 226.9
K = 0.860

as reviewed in Section 5.3.2 (iv), Figures 5.12, 5.13, 5.14 and 5.15. The four Figures, 5.12 to 5.15, were produced at the same time as the flickermeter results were taken.

CHANNEL 2
RANGE 3

	1 MINUTE LEVEL	10 MINUTE LEVEL	OVERALL LEVEL
P_{MAX}	230	230	230
$P_{0.1}$	230	230	230
$P_{1.0}$	225	225	225
$P_{3.0}$	215	215	215
$P_{10.0}$	200	200	200
P_{MEAN}	142	141	141
P_{SD}	42	42	42
Annoyance	10	10	10
Perception	15	15	15
Visible	15	15	15

Previous 10 second uppercentile level 225

Table 5.2 Flickermeter results for the arc furnace model only

Table 5.3 shows the displayed results. The classified levels for each probability value are less than half those for the uncompensated model, and the annoyance factor has been reduced from 10 times worse to 6 times worse than 'just annoying'.

It was encouraging to note that the flickering of a tungsten filament lamp connected at the point of measurment was also visibly reduced.

CHANNEL 2
RANGE 3

	1 MINUTE LEVEL	10 MINUTE LEVEL	OVERALL LEVEL
P_{MAX}	105	105	105
$P_{0.1}$	100	100	100
$P_{1.0}$	90	90	90
$P_{3.0}$	85	85	85
$P_{10.0}$	75	75	75
P_{MEAN}	57	57	57
P_{SD}	13	13	13
Annoyance	6	6	6
Perception	10	10	10
Visible	10	10	10

Previous 10 second uppercentile level 90

Table 5.3 Flickermeter results for the compensated arc furnace model

CHAPTER SIX

A TWELVE-PULSE THYRISTOR-CONTROLLED REACTOR

CHAPTER SIX

A TWELVE-PULSE THYRISTOR-CONTROLLED REACTOR

Twelve-pulse schemes have been successfully used in reactifier equipment[127] to reduce the harmonic current generation. Such schemes use different sets of three-phase secondary windings on the same transformer core to achieve current cancellation at harmonic frequencies greater than the third.

Miller[95] concludes his study of TCR compensator harmonics by presenting a twelve-pulse arrangement. Such a scheme will be investigated here, with a study of control methods and their application for voltage flicker reduction.

6.1 MODELLING AND CONTROL

The six-pulse TCR compensator described in Chapters IV and V was shown to give a reduction in the flicker frequency components of an arc furnace supply voltage waveform. The same laboratory modelling techniques were then applied to the construction of a twelve-pulse TCR compensator, for application with the arc furnace model described in Chapter II.

6.1.1 Modelling Requirements

A twelve-pulse thyristor scheme will consist of two equally rated six-pulse units connected in parallel. Phase displacement of one unit from the other may be obtained using different three-phase transformer secondary winding arrangements for each six-pulse unit, the primary windings being connected at the same point. This is more easily accomplished by using a single transformer with two secondary sets of windings sharing the same magnetic circuit with only one primary. Such a transformer is shown in Figure 6.1 together with the relevant voltage and current relationships.

The twelve-pulse TCR compensator three-phase rating was required to be equal to the rating of the six-pulse compensator which gave the best flicker improvement results in Chapter V. The rating for full conduction was then 579VA, with the rating equally divided between the two six-pulse secondary circuits of the Δ-Δ/Y transformer. Each compensator branch was constructed as a 'unit' of 1.00H inductance, connected in series with a BTX 18-500[106] thyristor and 0.50hm resistor for branch current measurement. Firing circuits were constructed to be identical to those used for the six-pulse TCR.

The short circuit impedance of the Δ-Δ/Y transformer was approximately 0.5 + j0.20hms, considered to be negligible compared to the reactance of the compensator inductances. The transformer magnetising current was approximately 0.4A, and slight distortion of the supply voltage waveform was observed because of this.

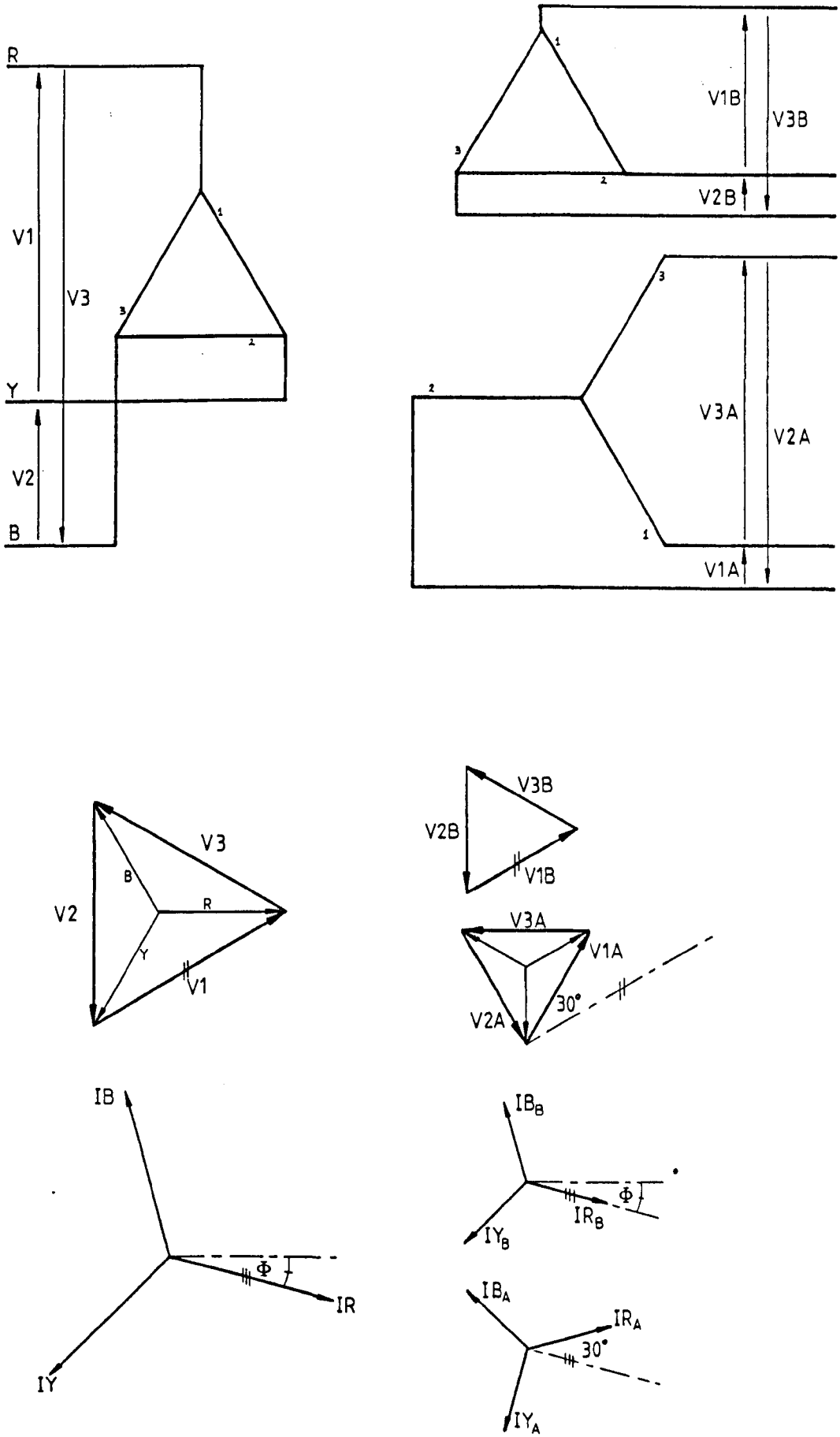


Fig. 6.1 :Y-Δ/Y transformer winding connections with voltage and current relationships

6.1.2 Conduction Patterns

Both the transformer Y and Δ secondaries were connected to identical Δ-connected three-phase TCR units. The definition of circuit parameters is given in Figure 6.2. The conduction patterns within each of the Δ-connected TCR units are identical to those shown in Chapter IV, but to a common time reference all voltages and currents in the arrangement connected to the Y secondary lead those connected to the Δ secondary by a phase angle of 30° as shown in Figure 6.1.

The sum of the currents drawn by the two secondary circuits is then drawn from the supply by the transformer primary. Conduction patterns are best studied for each secondary six-pulse TCR arrangement operating in isolation from the other, then the principle of superposition may be used to obtain the combined effect on the primary circuit. Figure 6.3 shows the current conduction patterns for thyristor firing delayed at 100, 135 and 170 degrees after the respective voltage zero crossing. Figure 6.4 shows how the currents add in the primary circuit.

6.1.3 Control Requirements

An advantage of the Y-Y/Δ twelve-pulse TCR system is that thyristor conduction in the relevant branch of the Δ-connected secondary circuit may lead the conduction in the Y-connected secondary circuit by a phase angle of 30°. The flexibility of the microprocessor-based control equipment allowed it to be easily adapted for use with the twelve-pulse scheme. Each of the three microprocessors continued to sample separate line voltages, and decide on thyristor firing angles using an 'integral of voltage difference' calculation similar to that described in Chapter IV.

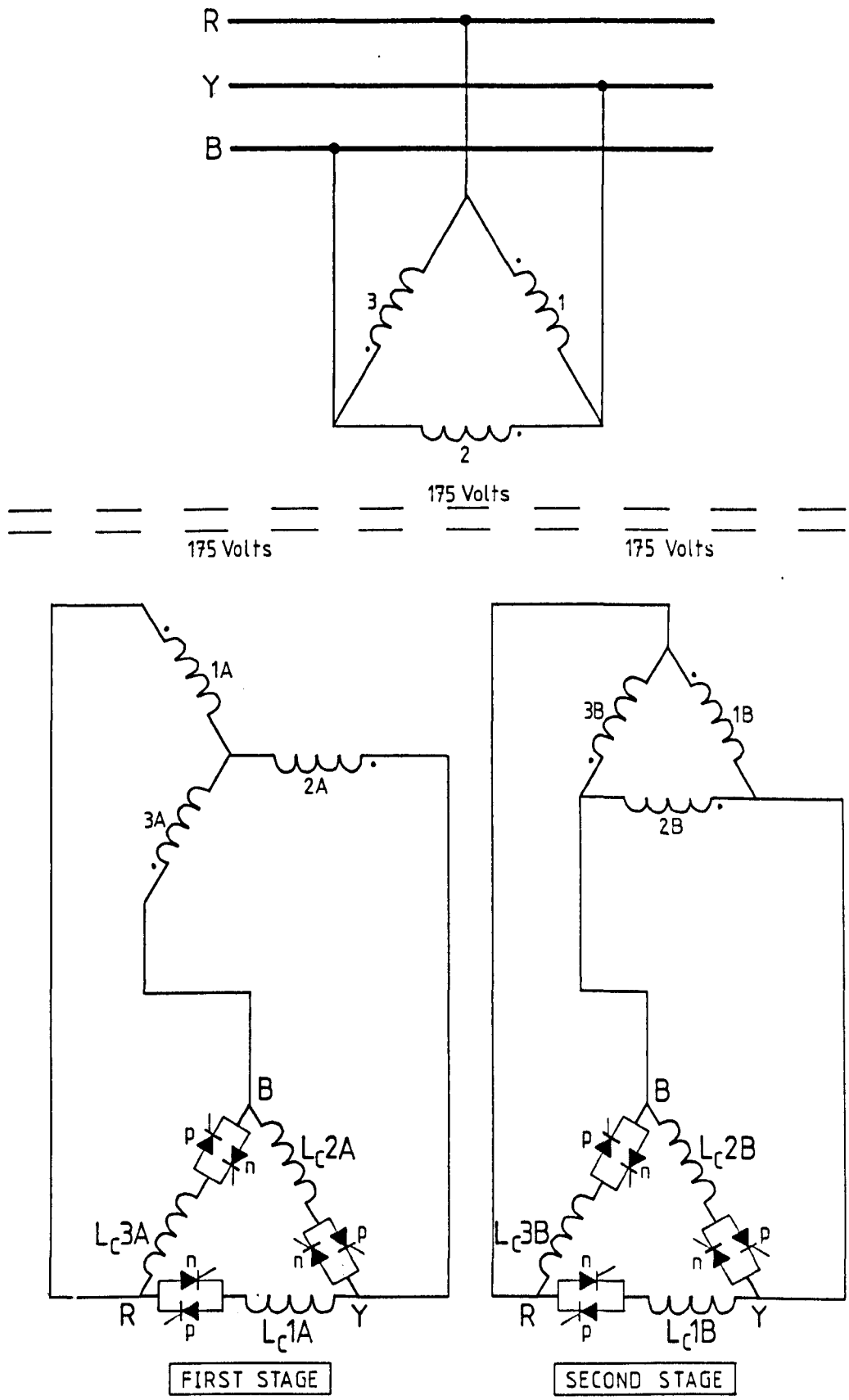


Fig. 6.2 : Connection diagram of 12-pulse TCR compensator

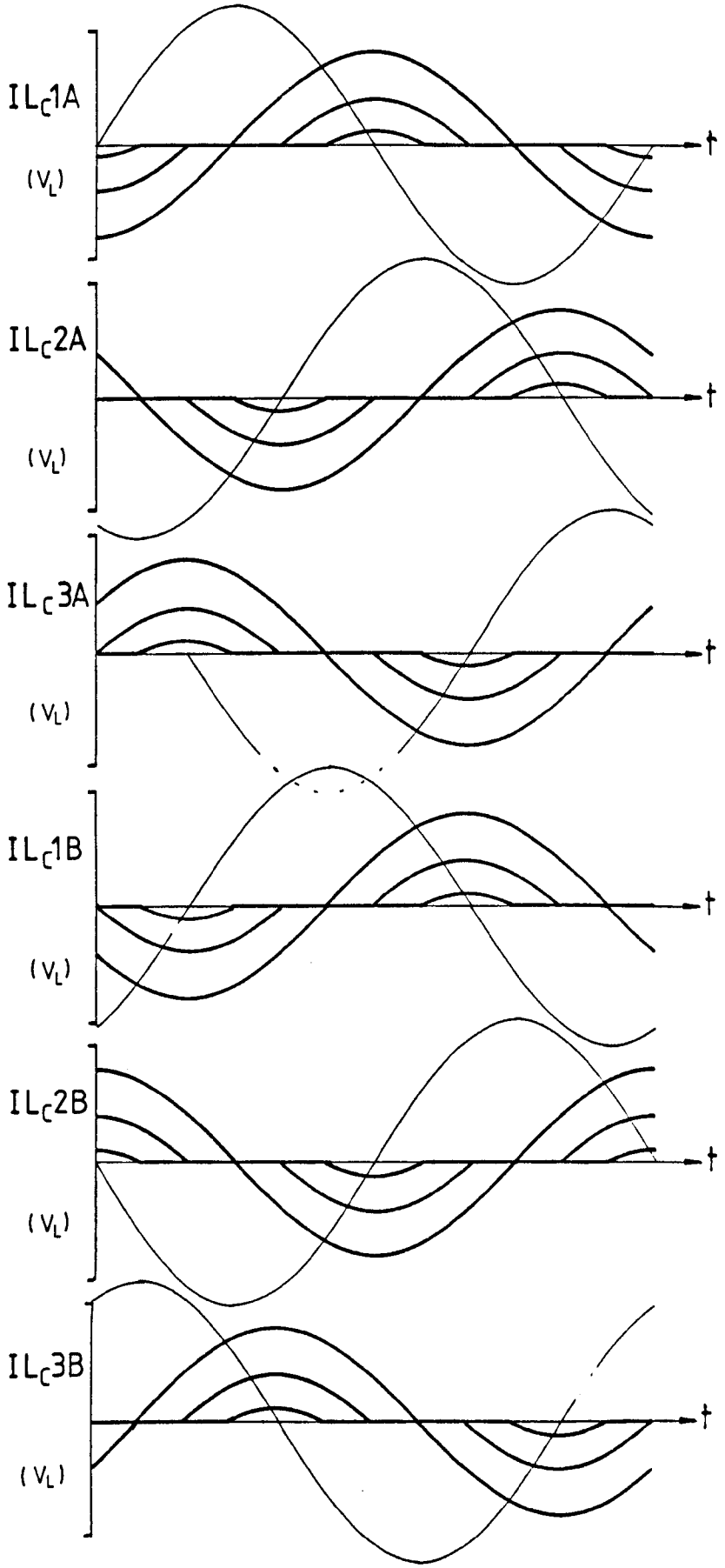


Fig. 6.3 : Y-Δ/Y Transformer secondary current conduction patterns

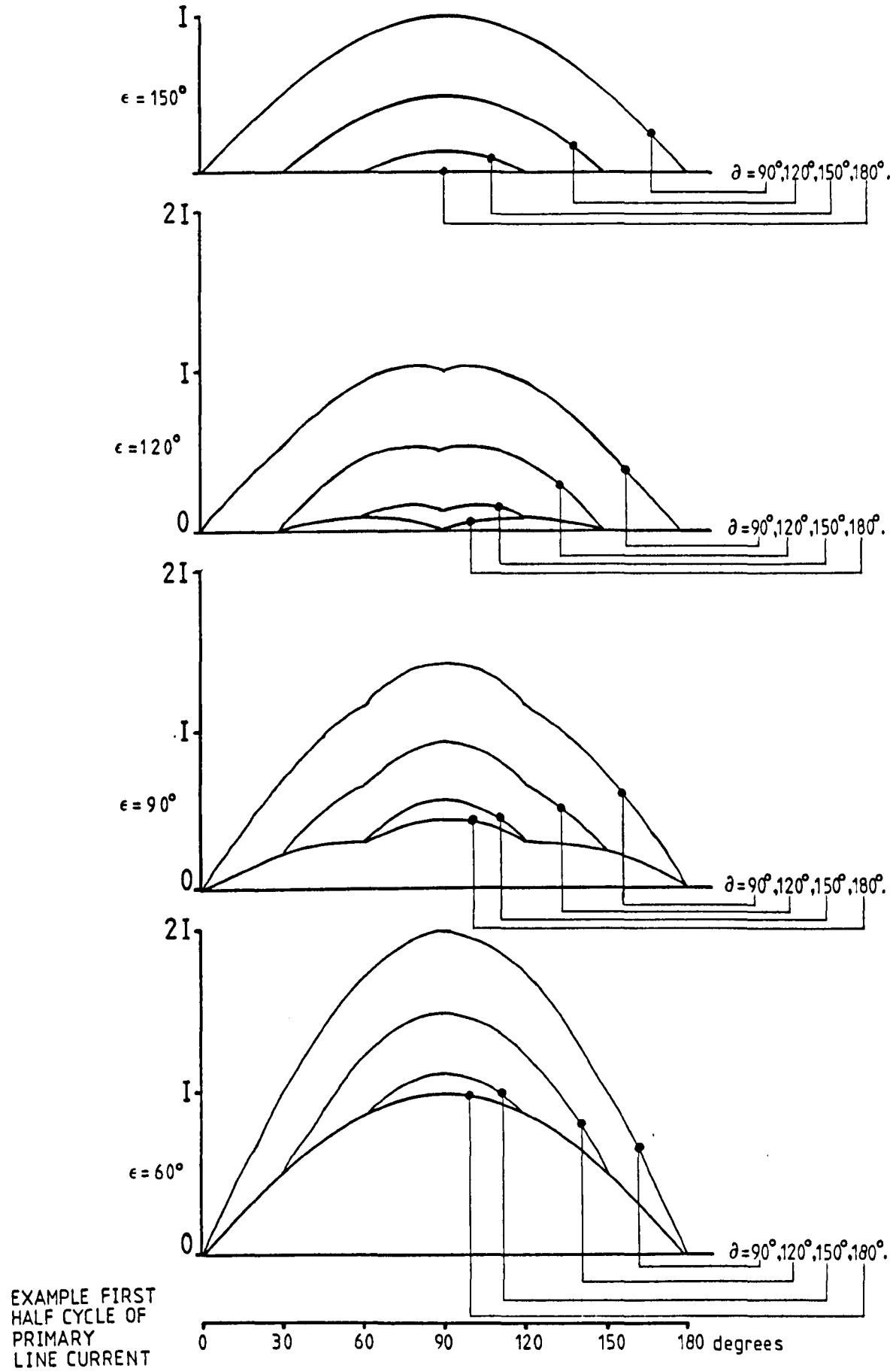


Fig. 6.4 : Y-Δ/Y Transformer primary current conduction patterns

Figure 6.5 shows the allowable conduction angles for both of the secondary circuits, with respect to the primary line voltage that is sampled by the control system. We define the period when current is flowing in the 30 degrees phase advanced six-pulse unit as 'first stage conduction', and that period when current is flowing in the in-phase six-pulse unit as 'second stage conduction'. It is clear from Figure 6.5 that if the voltage-zero crossing is retained for initiation of the integration procedure (see Section 4.2.3), then the earliest firing angle for first-stage conduction is preceded by an integration period of only 3.33 milliseconds. This shorter integration period could easily have been overcome, but the control philosophy for the twelve-pulse system did not demand such action.

It was intended that the speed of response of the TCR compensator could be improved by having the ability to initiate first-stage firing as soon as possible.

It was highly likely that such shortening of the integration period would result in some loss of accuracy in the compensation system, and therefore the second-stage conduction period would be used for slower and more accurate control.

The microprocessor systems required modification of the control programs to achieve the following items in both positive and negative half-cycle sections of the control routine:

(a) Integration from voltage zero-crossing to a lower integration limit, LIMIT1, set to initiate first-stage conduction. Integration then to continue to a higher integration limit, LIMIT2, for second-stage conduction.

(b) Restriction of first-stage firing pulse output to between 3.33 and 8.33 milliseconds after primary voltage zero-crossing.

The assembler language program, 'FirBsub.asm', is listed in full in Appendix K.

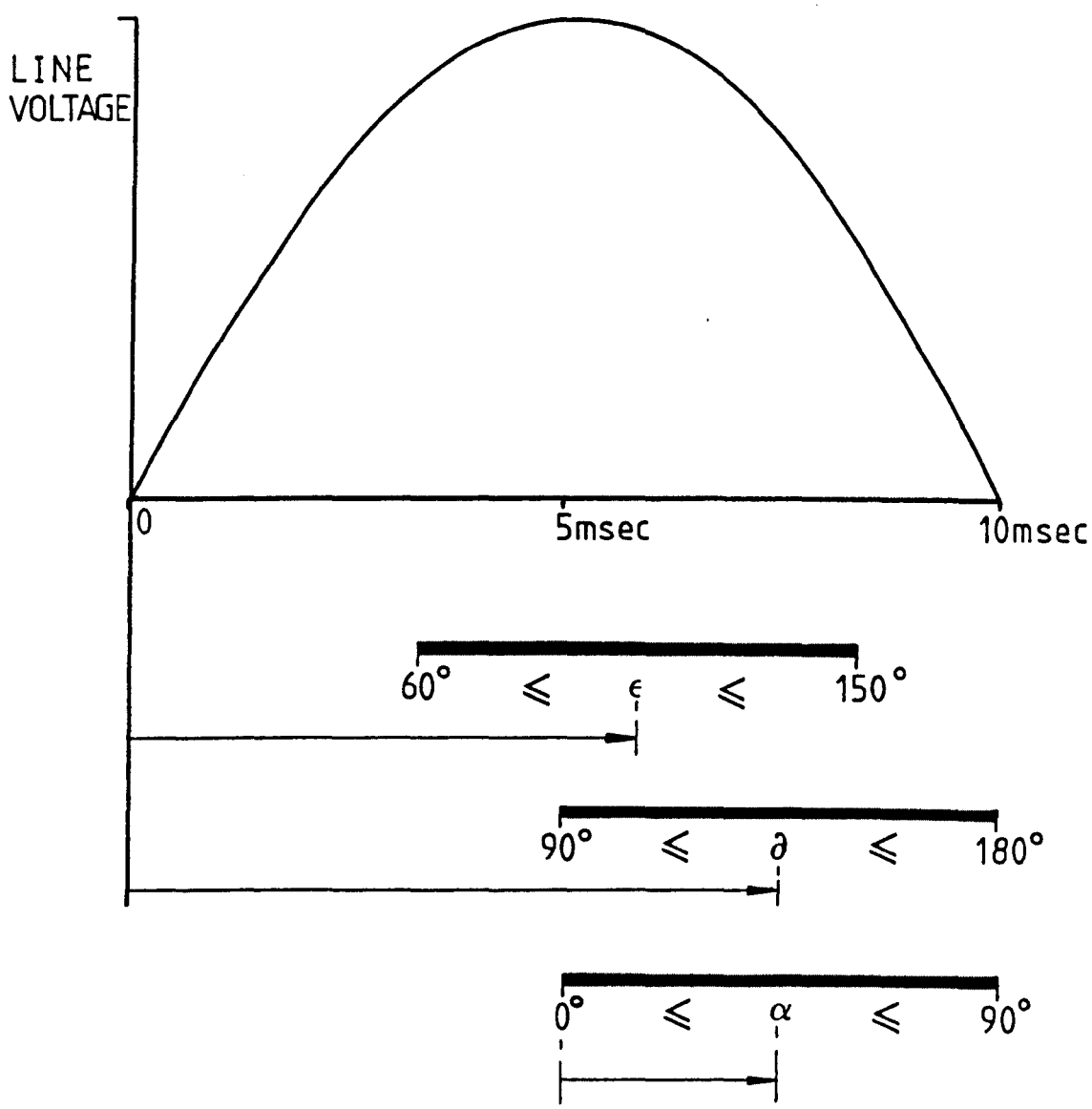


Fig. 6.5 : Y-Δ/Y transformer primary line voltage with secondary current conduction angles

6.1.4 Control Variables

The variables in the twelve-pulse TCR control algorithm are similar to those treated in Section 4.2.4 for the six-pulse version:

i.e. (i) The sample loop delay, D.

(ii) The reference sinusoid $v_R(\omega t)$.

(iii) The integration limit, LIMIT.

and these are once again considered in turn.

(i) Sample Loop Delay, D

The same block of program code as given in Section 4.2.4 was used to allow a variable hexadecimal value, D, to be inserted into every sampling loop. There are now four such sampling loops in the program, covering the integration periods before the first and second stage firing for positive and negative half cycles.

The sample loop delay time, Δt, was thus adjusted to be as near as 74.0 microseconds as possible, and the times obtained were:

System 1, positive half cycle, first stage : Δt = 74.1 μsecs
positive half cycle, second stage : Δt = 74.5 μsecs
negative half cycle, first stage : Δt = 74.1 μsecs
negative half cycle, second stage : Δt = 74.3 μsecs
System 2, positive half cycle, first stage : Δt = 74.1 μsecs
positive half cycle, second stage : Δt = 73.9 μsecs
negative half cycle, first stage : Δt = 74.1 μsecs
negative half cycle, second stage : Δt = 73.6 μsecs

System 3, positive half cycle, first stage : Δt = 74.1 μsecs
positive half cycle, second stage : Δt = 73.4 μsecs
negative half cycle, first stage : Δt = 73.3 μsecs
negative half cycle, second stage : Δt = 73.9 μsecs

The final location of bytes representing 'D' in RAM were 20, 101, 194 and 275 bytes respectively from the start of the 'FirBsub' object code program block.

(ii) The Reference Sinusoid, $v_R(\omega t)$

The ADCs and sampling circuitry was left as set for the six-pulse TCR compensator.

The open circuit line voltage of the laboratory model was nominally 175 volts, and it was found that the magnetising current of the Δ-Δ/Y transformer depressed this voltage to approximately 171 volts.

Full three-phase TCR conduction, in both first and second stage units, further depressed the line voltage to approximately 149 volts. The reference sinusoid values were set in RAM to be equivalent to a sine wave with an RMS value of 146 volts.

The LSB of the data byte represents 2.063 volts, therefore

$$v_R = 127 + 100 \sin\omega t$$

With the sampling frequency at approximately 74 microseconds, there were once again 133 reference points calculated for each half cycle. These were stored in look-up tables 'sine1' and 'sine2' in RAM and are given in Appendix K.

(iii) Integration Limit, LIMIT

Each of the three controllers required four integration limits to be set in RAM to determine the position of the four thyristor firing pulses through each 50Hz voltage cycle.

POSLIM1 - Determined the position of the first-stage firing pulse in the positive half-cycle.

POSLIM2 - Determined the position of the second-stage firing pulse in the positive half-cycle.

NEGLIM1 - Determined the position of the first-stage firing pulse in the negative half-cycle.

NEGLIM2 - Determined the position of the second-stage firing pulse in the negative half-cycle.

The most successful thyristor firing angles for the six-pulse TCR were shown in Chapter V to be those giving $\partial = 100^{\circ}$; allowing the greatest range of control as the model arc furnace current increases toward the short-circuit value.

The integration limits were set in the twelve-pulse TCR to correspond to $\partial = 100^{\circ}$

i.e. $\varepsilon = 70^{\circ}$ and $\partial = 100^{\circ}$

Part 6.2 details how these integration limits were set for a steady-state study, and Part 6.3 gives the results of applying the system to the fluctuating model arc furnace load.

6.2 STEADY-STATE TUNING AND PERFORMANCE

The studies performed for the six-pulse TCR compensator in Part 4.3 gave an appreciation of the effects of changing different control variables. The most useful of these was judged to be the 'shunt load TCR compensation' experiment (4.3.3 (ii)) and this was repeated in various forms for the twelve-pulse scheme.

6.2.1 Thyristor Firing and Conduction Limits

The thyristor firing circuitry and isolation transformers were identical to those used for the six-pulse TCR compensator described in Section 4.3.1. The same 8-bit output port was used to transfer firing commands to the pulse stretching and amplification circuitry. The latching circuitry was particularly important for this application, where to apply a long output pulse from the processor would have inhibited integration following first-stage firing.

The SDK88 'SI' register was again used as a counter and incremented through 133 steps, one for each analogue to digital conversion made in the half-cycle. Tables of the reference sinusoids 'sine1' and 'sine2' are not presented here, but may be found at the end of the 'FirBsub.asm' program listing in Appendix K.

This counter 'SI' was again used as a reference for the program to determine whether firing should be allowed, and the values were used to limit ε and ϑ to:

$$60^\circ \leqslant \varepsilon \leqslant 150^\circ$$

and

$$90^\circ \leqslant \vartheta \leqslant 180^\circ$$

The limiting values appear in the program listing (Appendix K).

6.2.2 Steady-State Reactive Compensation Results

The step changes and depression of the model supply line voltage waveform varied according to the firing angles ε and ϑ.

Figure 6.6 shows how the open circuit line voltage is depressed by operation of the first-stage unit, with the second stage unit disconnected. The limits required for this steady-state 'open circuit' condition were:

POSLIM1 = 256 dec, @ 0100 NEGLIM1 = 192 dec, @ 00C0

for each of the three systems, giving $\varepsilon \simeq 70^{\circ}$.
The corresponding waveforms for second-stage conduction only are given in Figure 6.7. A value of $\vartheta \simeq 110^{\circ}$ was obtained with limits set at:

POSLIM2 = 448 dec, @ 01C0 NEGLIM2 = 384 dec, @ 0180

Further tests were performed with the first and second stages acting in isolation from each other to compare the shunt compensation effects of the separate halves of the twelve-pulse TCR system before both stages were used together.

Figure 6.8 shows the steady-state inductive load compensation test circuit, and the V-I characteristics obtained.

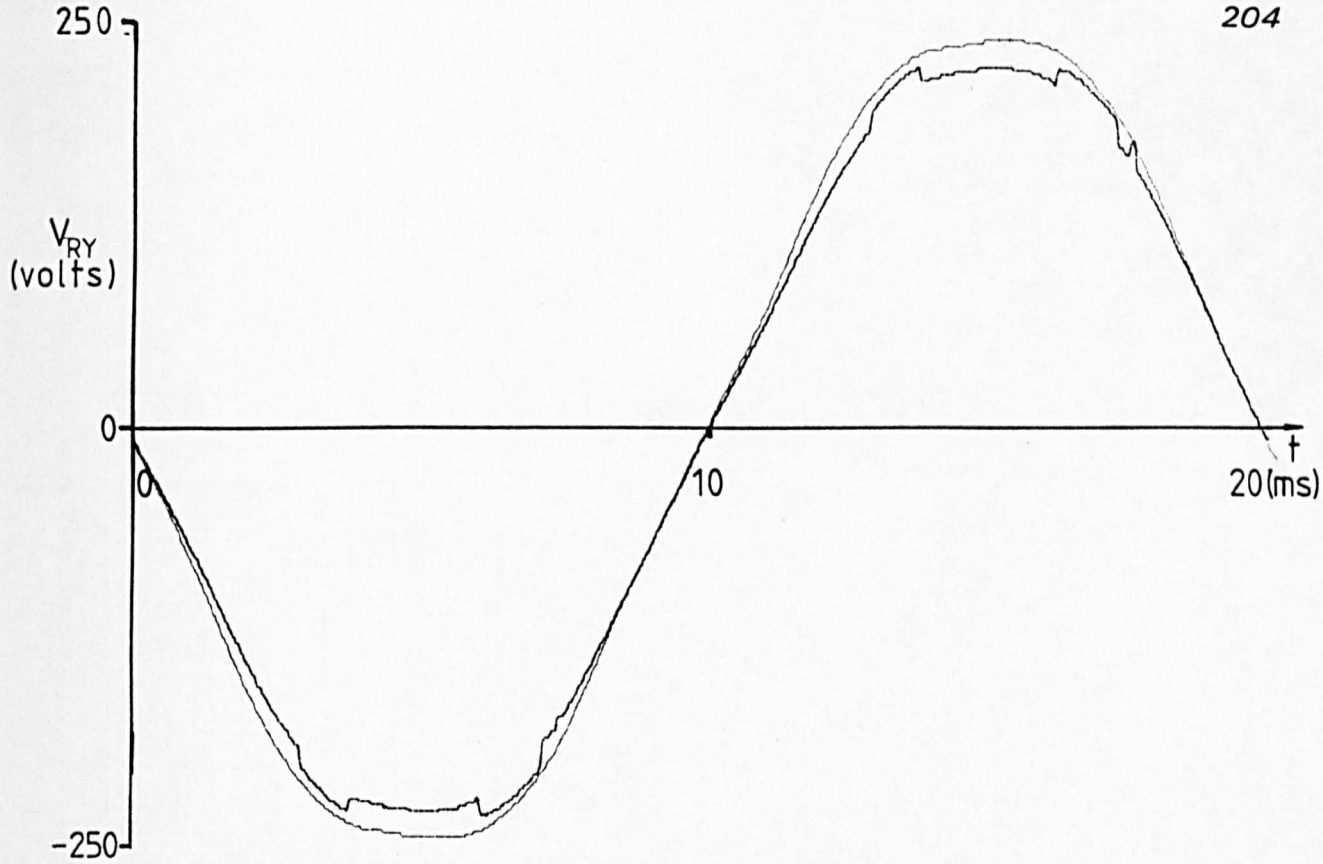


Fig. 6.6 : Line voltage depression for 12-pulse TCR first stage operation

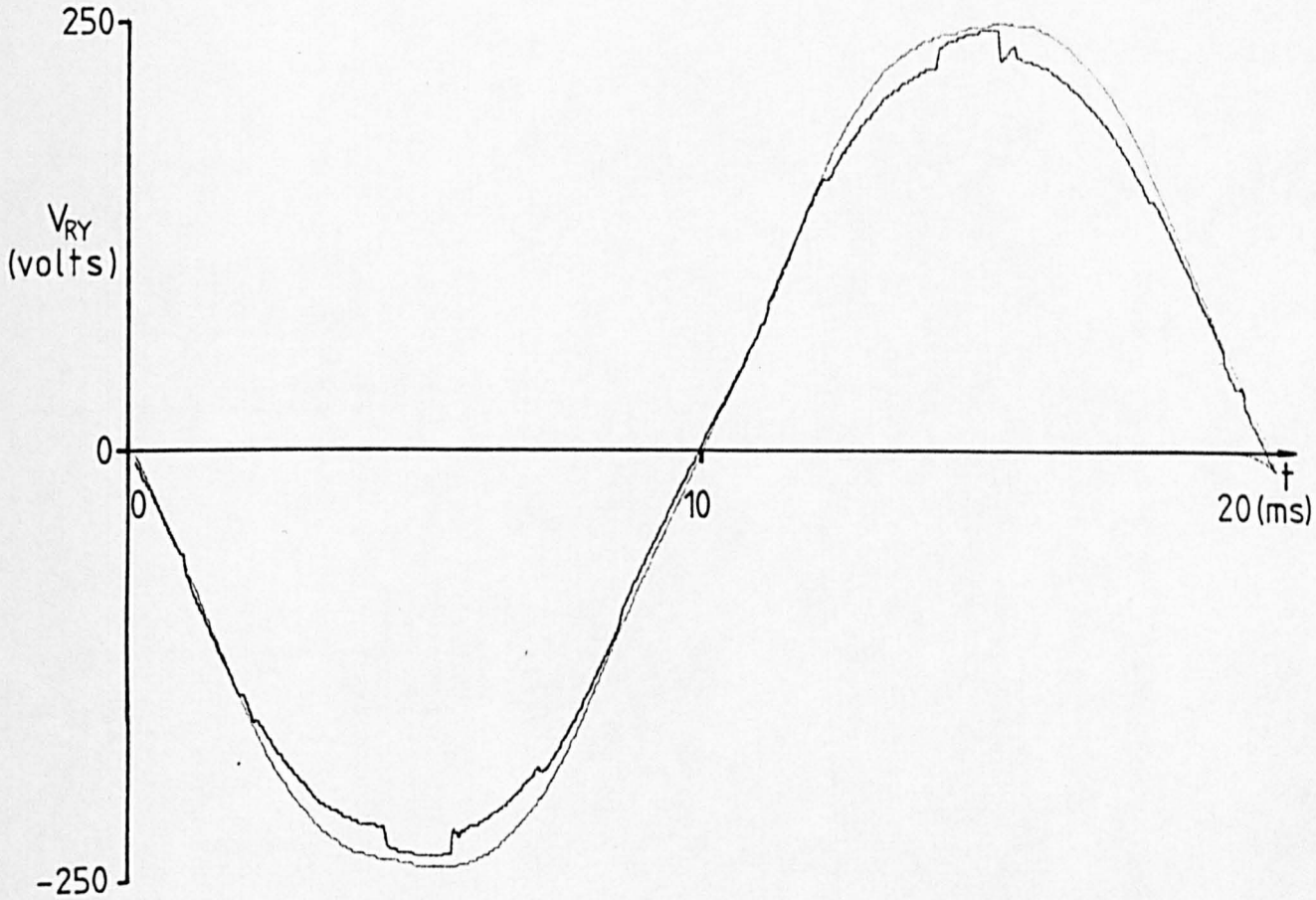


Fig. 6.7 : Line voltage depression for 12-pulse TCR second stage operation

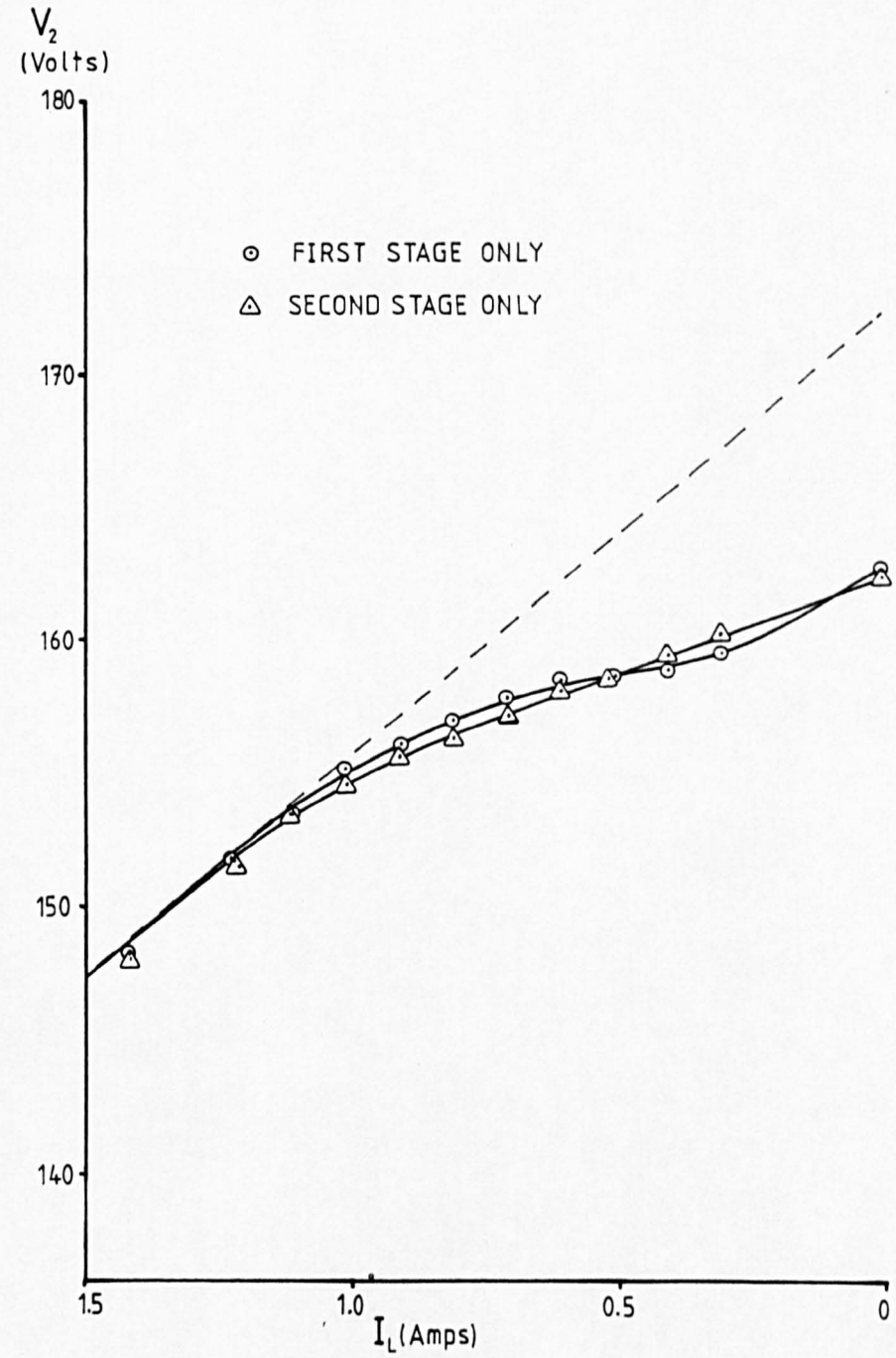


Fig. 6.8 : 12-pulse TCR steady state inductive load shunt compensation V-I characteristic

6.3 TWELVE-PULSE TCR PERFORMANCE WITH THE ARC FURNACE MODEL

Before attempting to operate both stages of the twelve-pulse compensator together, each stage was connected in turn to the laboratory arc furnace model.

The integration limits given in Section 6.2.2 remain applicable, since they were set for the condition where the inductive test load current was zero.

The arc furnace model was operated at its rated value as described in Chapter II, causing the TCR conduction angles to change cycle-by-cycle.

Figures 6.9, 6.10, 6.11 and 6.12 show the change in the line voltage power spectrum caused by operation of only the first-stage of the twelve-pulse TCR. Figures 6.13, 6.14, 6.15 and 6.16 show the spectra corresponding to operation of the second-stage only.

Both stages give a reduction in the 0-50Hz modulation frequency sidebands similar to the results presented for the six-pulse TCR compensator in Chapter V.

Operating both the first- and second-stage units of the twelve-pulse TCR system together required that the integration limits be adjusted in order to keep $\varepsilon \simeq 70^{\circ}$ and $\vartheta \simeq 110^{\circ}$ for the three-phase system.

The limits set to achieve these firing angles, with no model arc furnace current flowing, are shown in Table 6.1.

Figures 6.17, 6.18, 6.19 and 6.20 show the change in power spectra caused by operation of both stages of the twelve-pulse TCR compensator.

It is apparent that the twelve-pulse system as operated did not achieve as great a reduction in low frequency modulation power as the six-pulse TCR compensator showed. The reasons for the disappointing results may possibly lie in the control strategy used, and this is discussed further in Section 8.1.2.

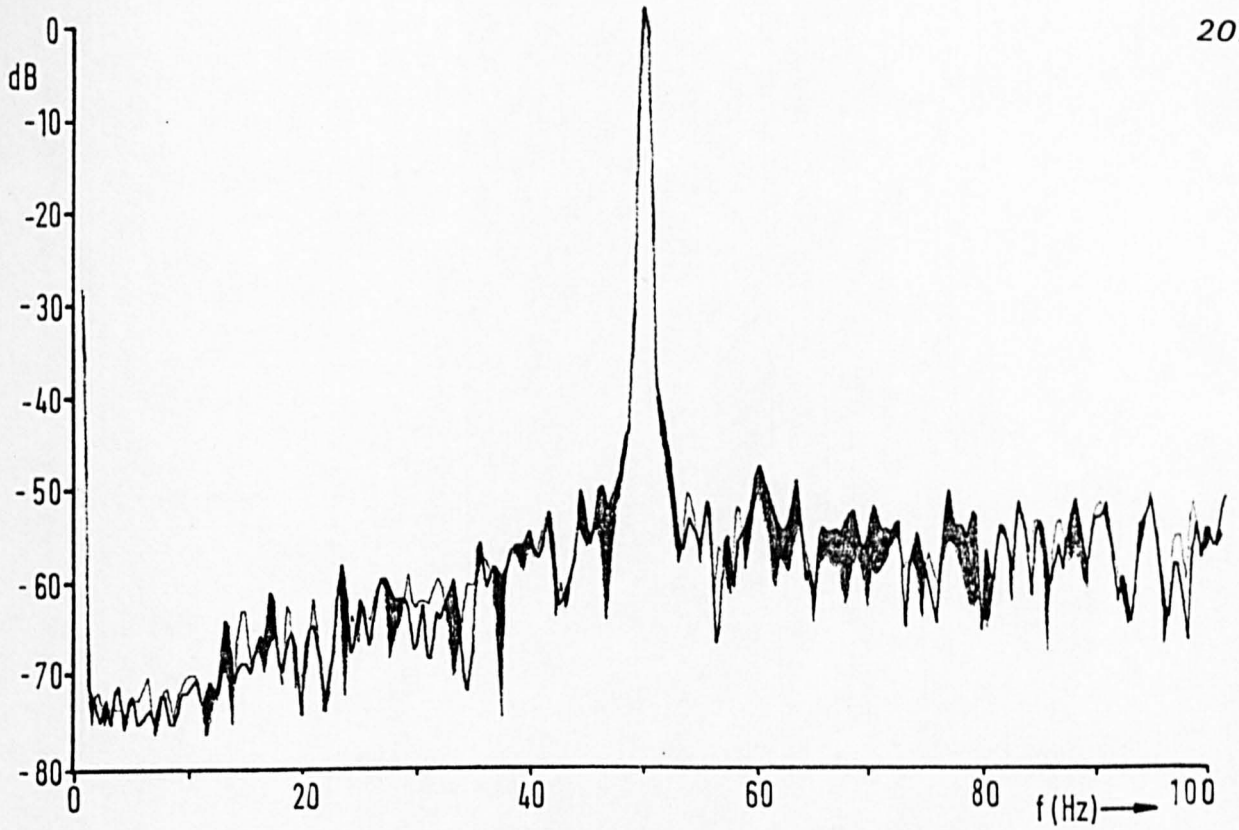


Fig. 6.9 : 0-100Hz power spectrum of Vry showing effect of 12-pulse TCR first stage operation

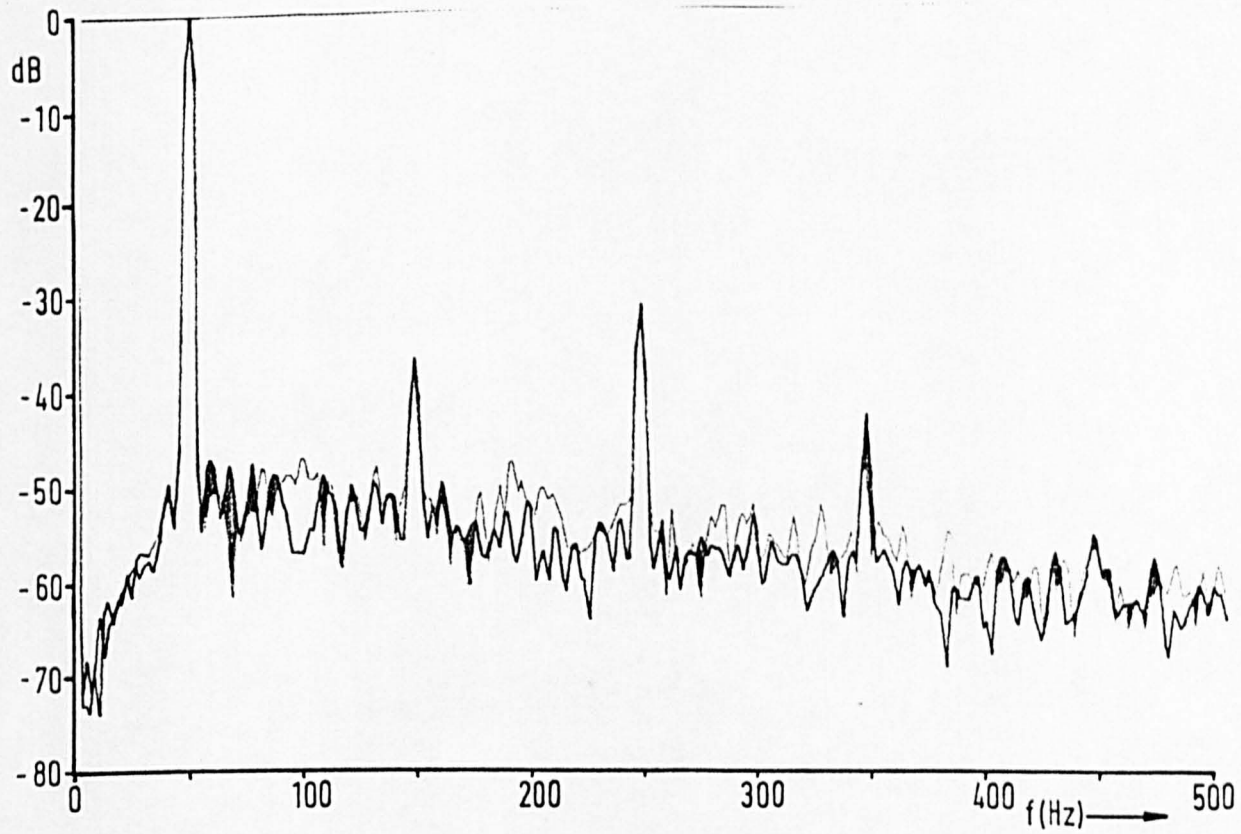


Fig. 6.10 : 0-500Hz power spectrum of Vry showing effect of 12-pulse TCR first stage operation

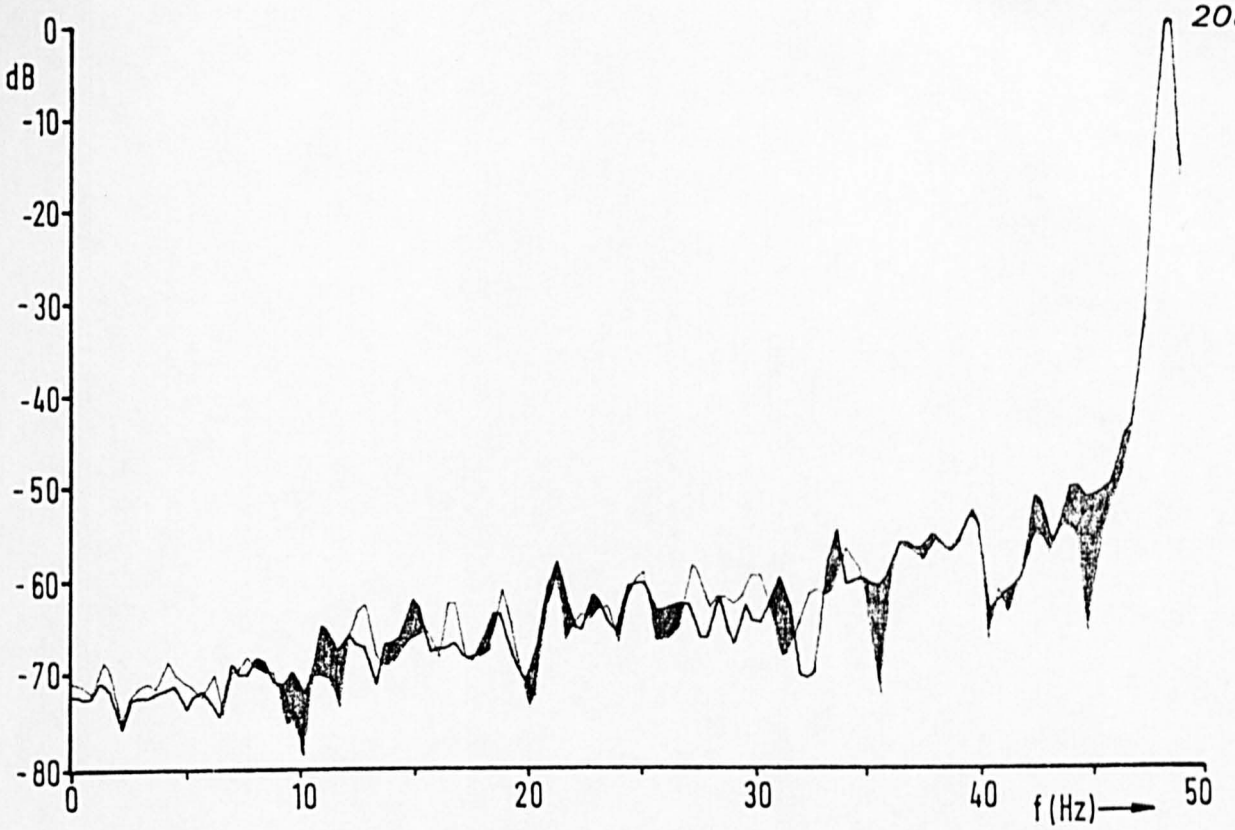


Fig. 6.11 : 0-50Hz power spectrum of Vry showing effect of 12-pulse TCR first stage operation

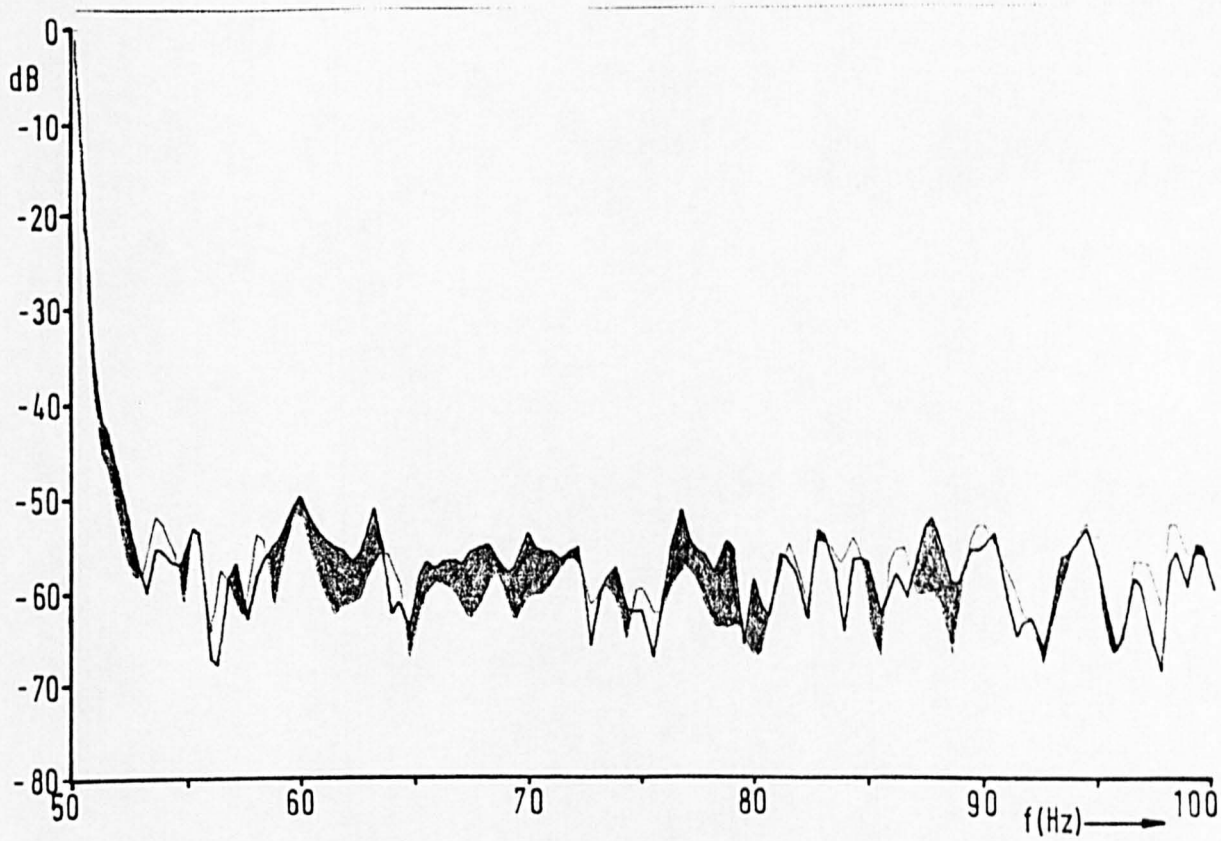


Fig.6.12 : 50-100Hz power spectrum of Vry showing effect of 12-pulse TCR first stage operation

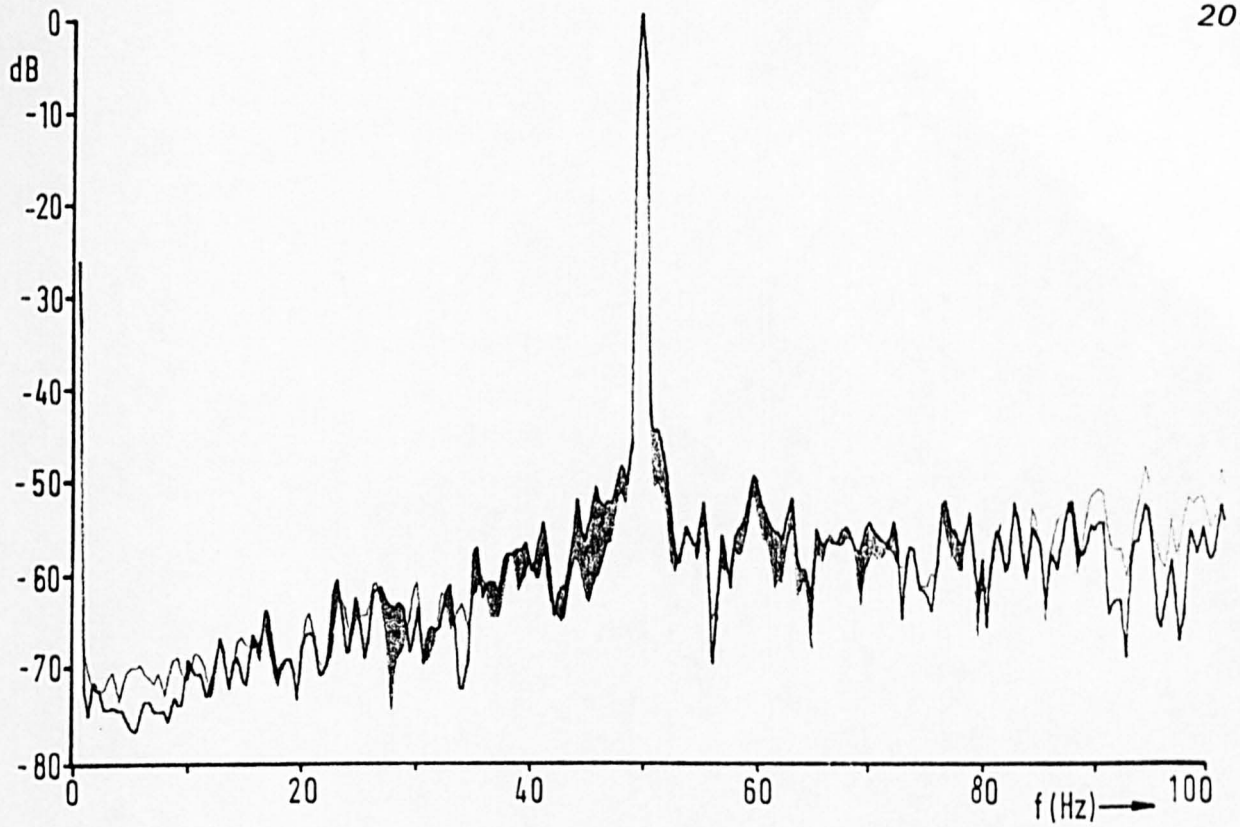


Fig. 6.13 : 0-100Hz power spectrum of Vry showing effect of 12-pulse TCR second stage operation

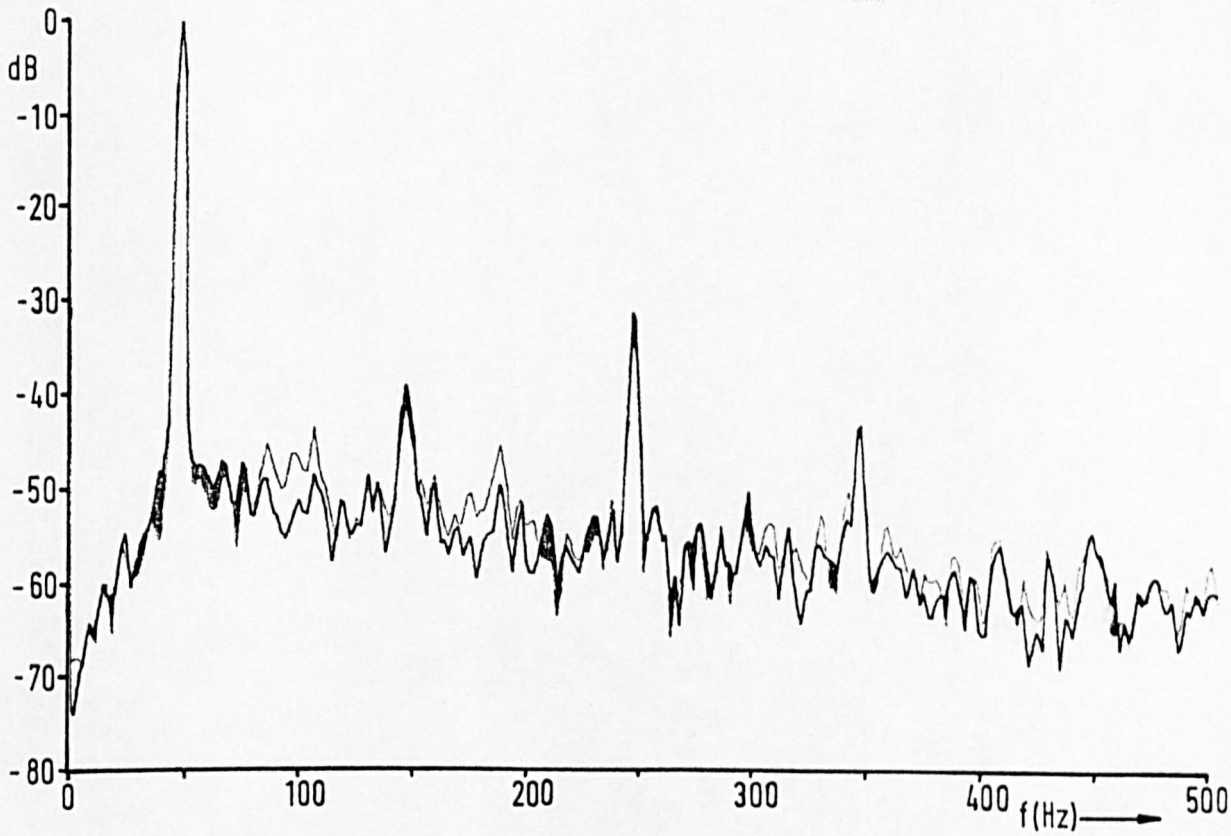


Fig. 6.14 : 0-500Hz power spectrum of Vry showing effect of 12-pulse TCR second stage operation

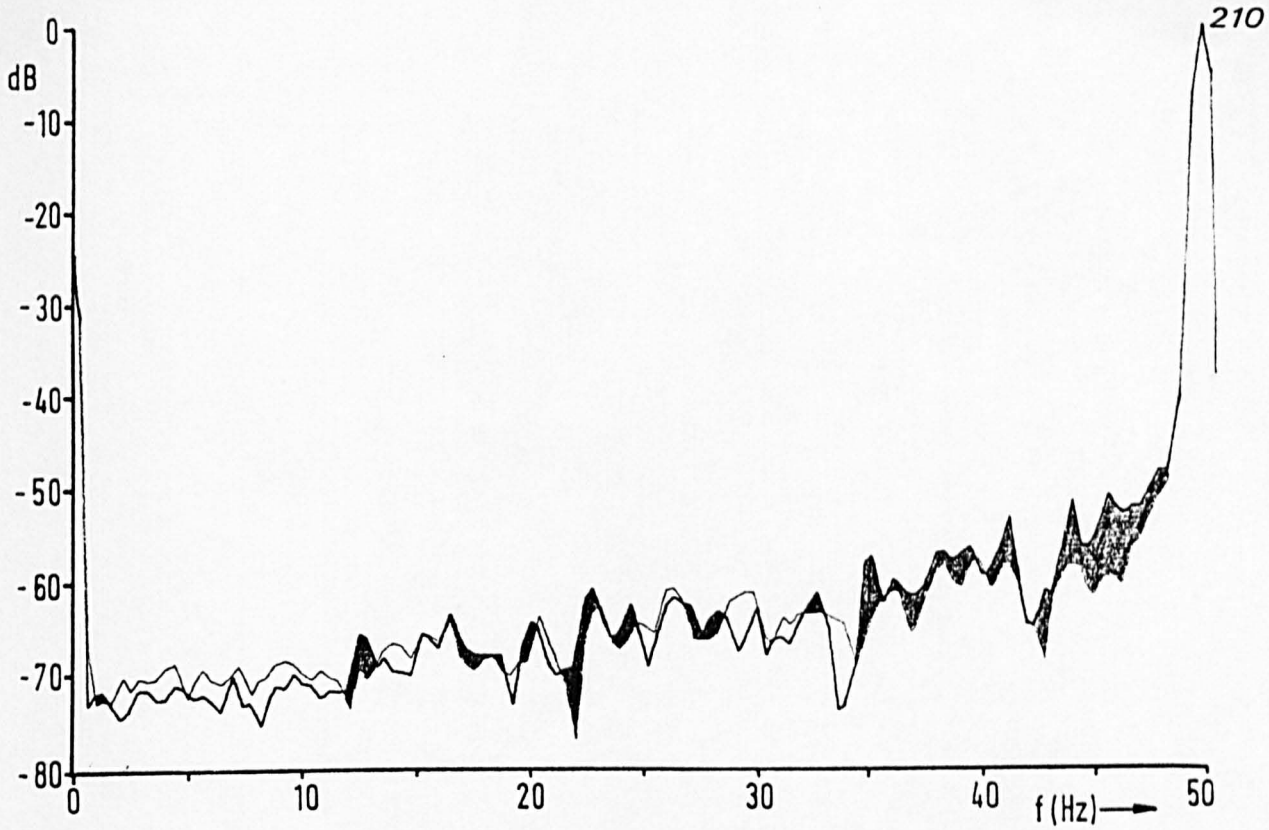


Fig. 6.15 : 0-50Hz power spectrum of Vry showing effect of 12-pulse TCR second stage operation

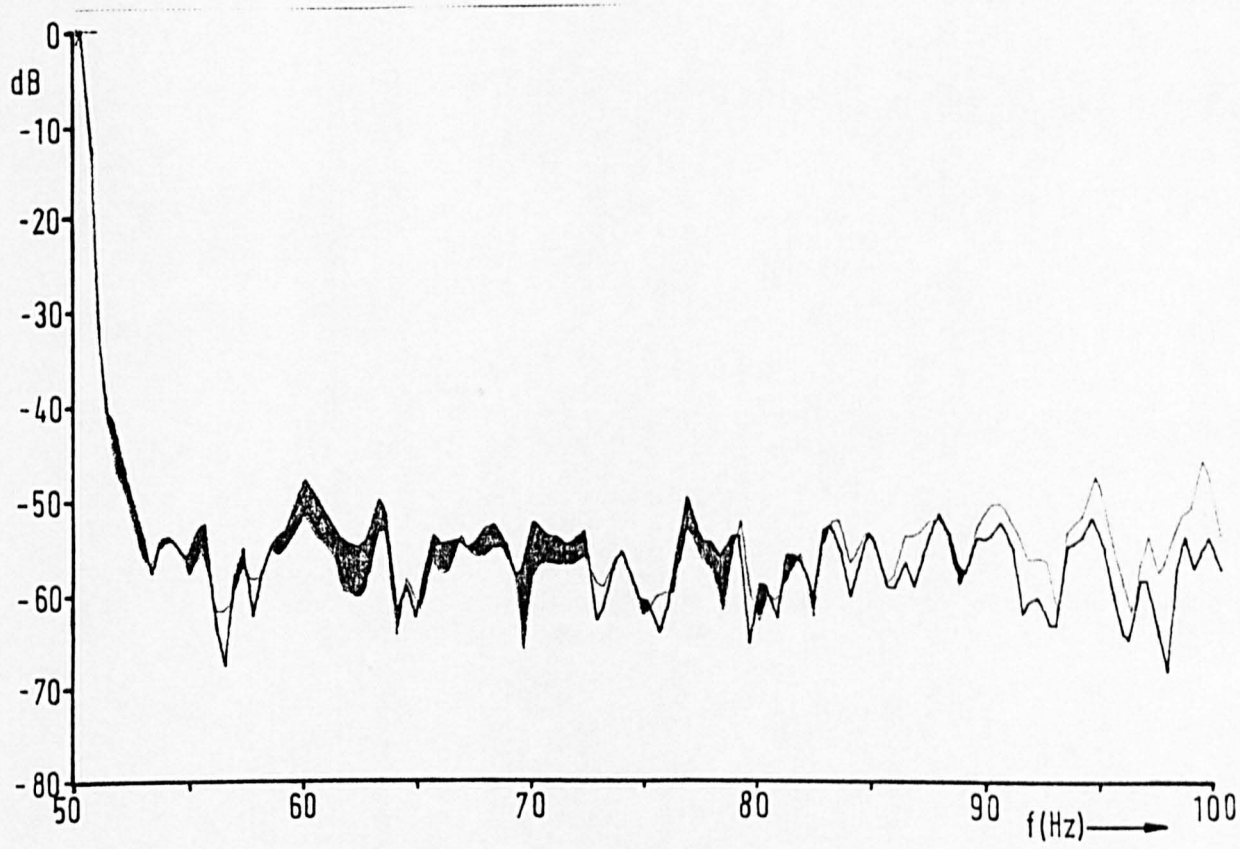


Fig. 6.16 : 50-100Hz power spectrum of Vry showing effect of 12-pulse TCR second stage operation

	SYSTEM 1	SYSTEM 2	SYSTEM 3
POSLIM1	0080	0080	0060
POSLIM2	0120	0120	00B0
NEGLIM1	0060	0020	0020
NEGLIM2	00C0	00B0	0040

Table 6.1 Hexadecimal Integration Limits for the twelve-pulse TCR Compensator

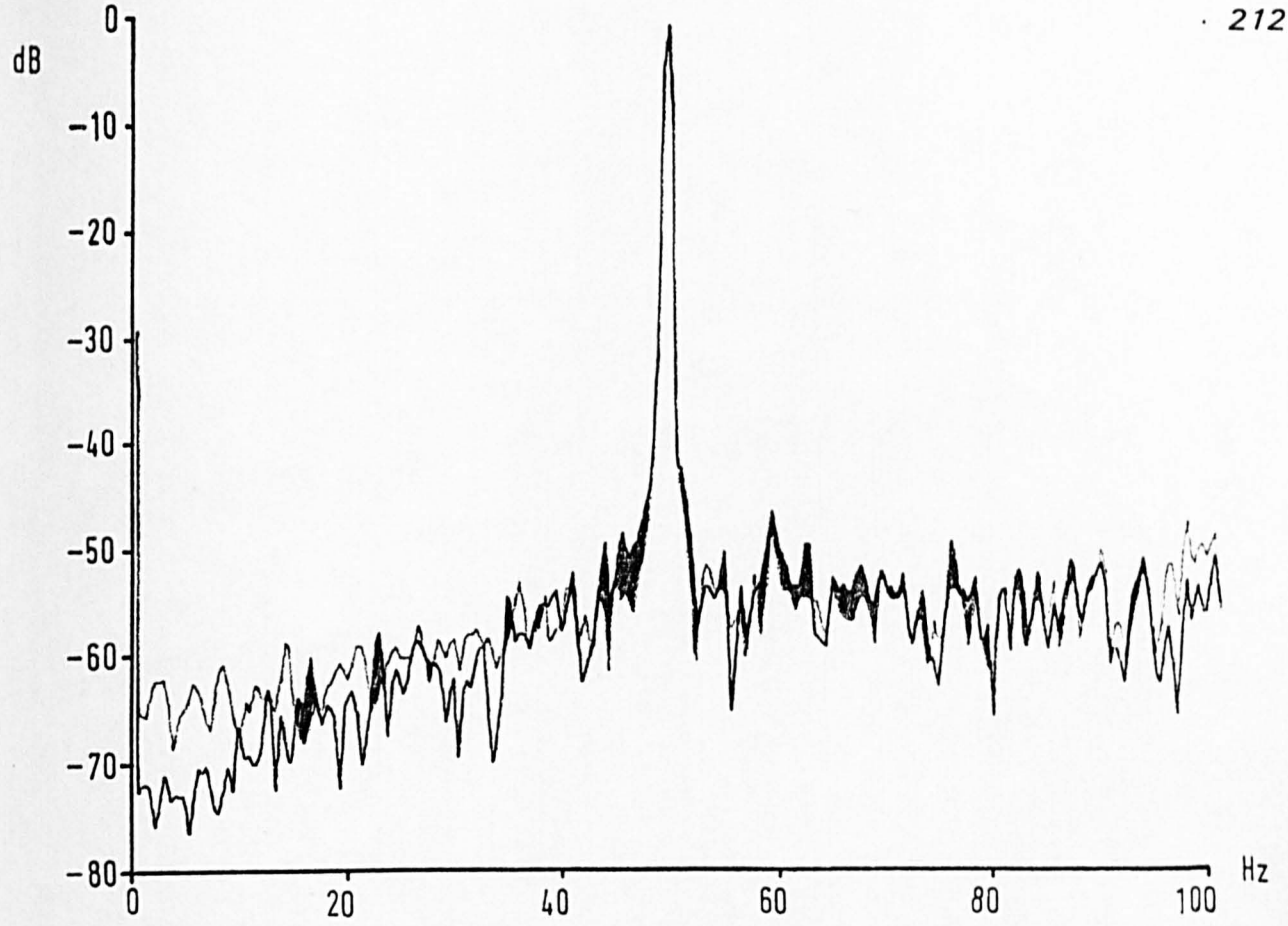


Fig. 6.17 : 0-100Hz power spectrum of Vry showing effect of 12-pulse TCR full operation

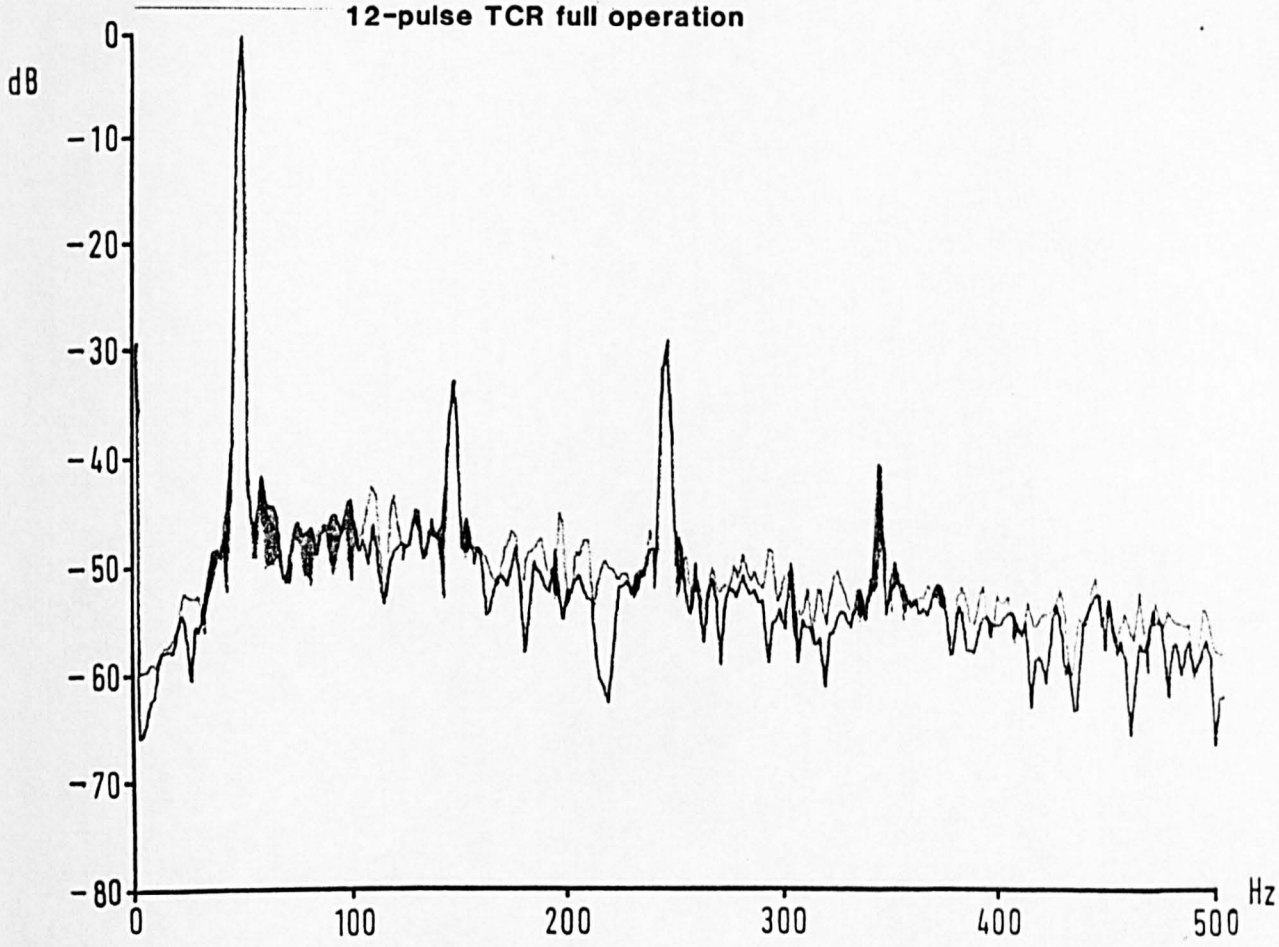


Fig. 6.18 : 0-500Hz power spectrum of Vry showing effect of 12-pulse TCR full operation

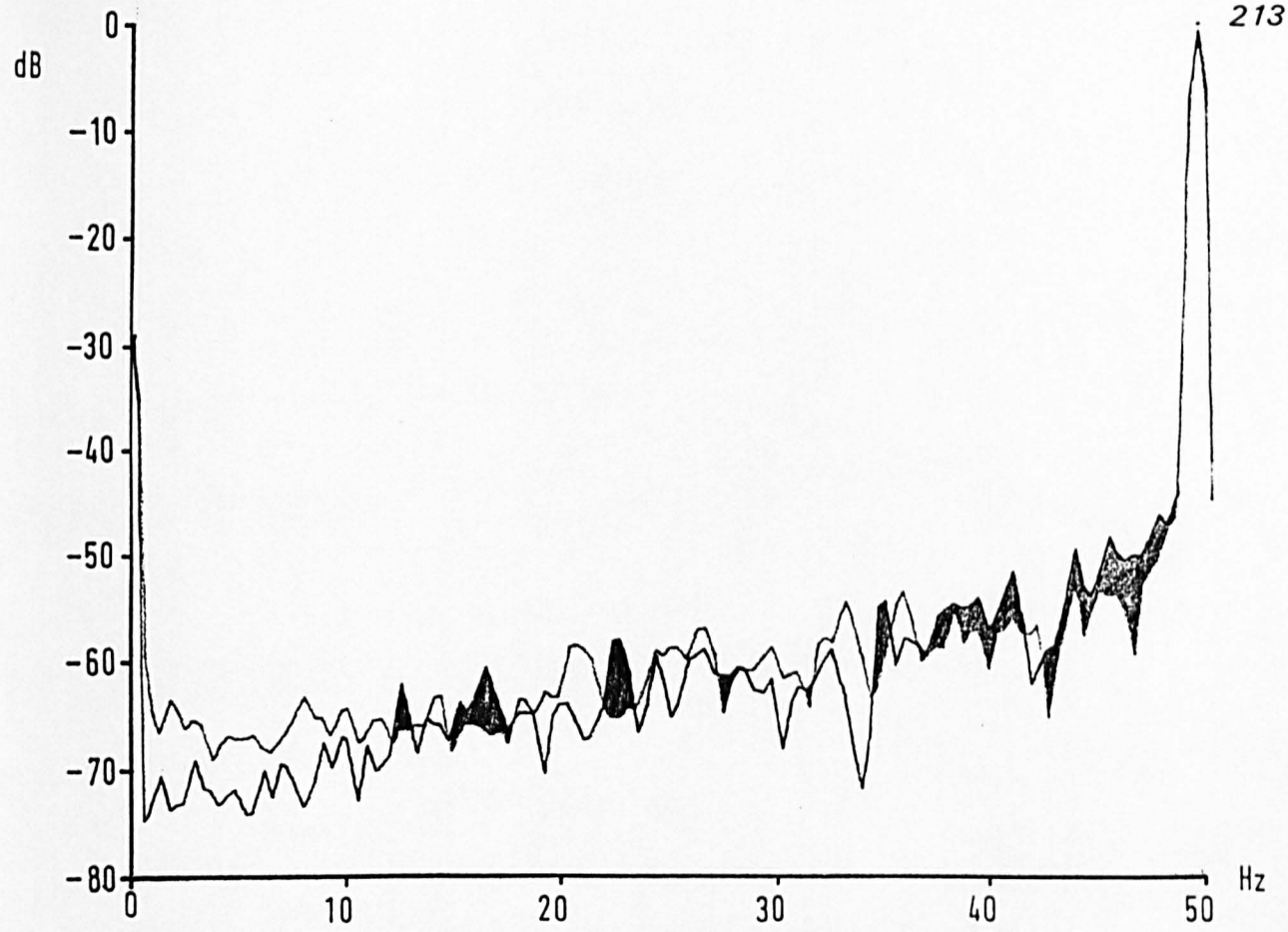


Fig. 6.19 : 0-50Hz power spectrum of Vry showing effect of 12-pulse TCR full operation

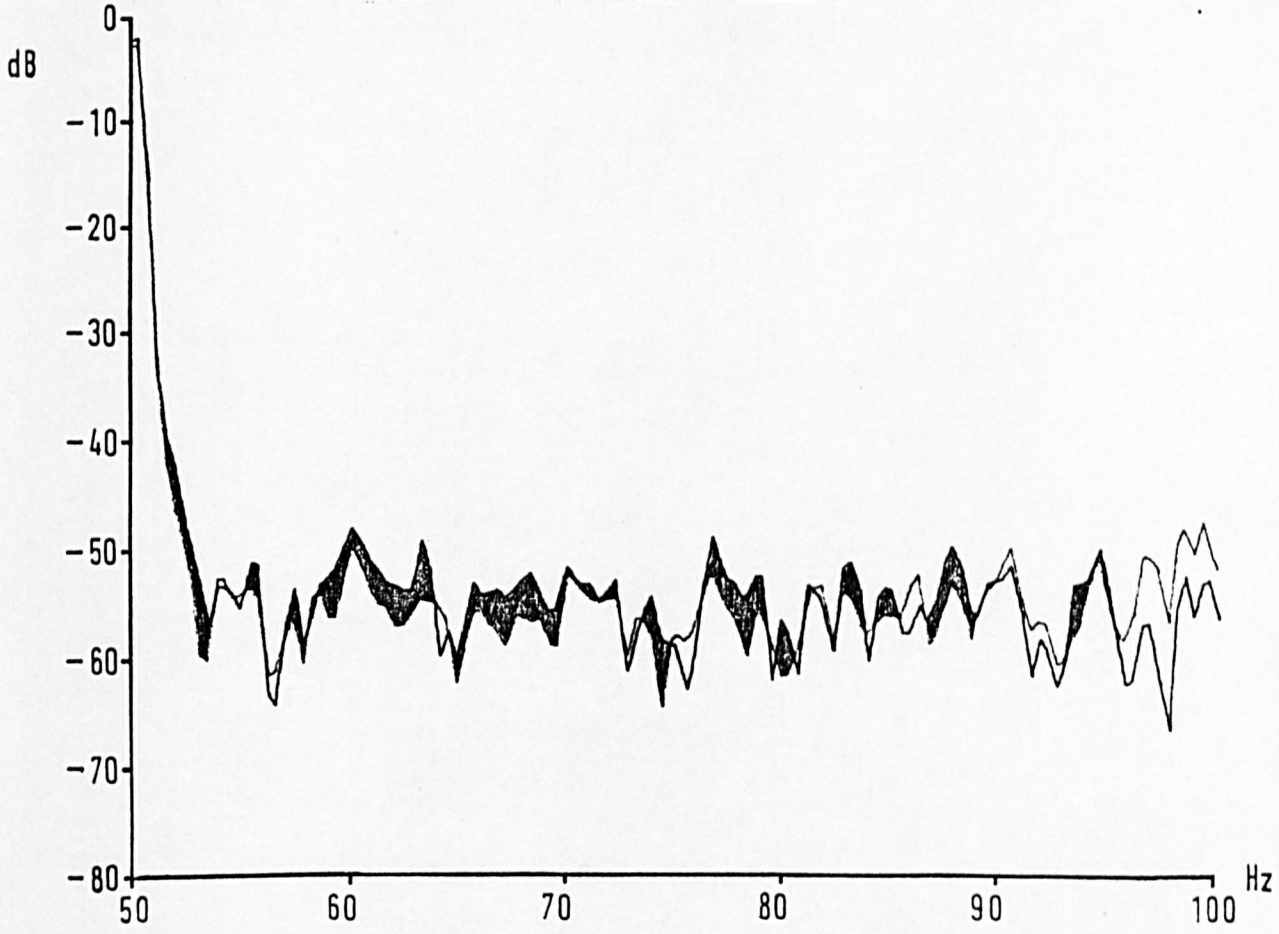


Fig.6.20 : 50-100Hz power spectrum of Vry showing effect of 12-pulse TCR full operation

CHAPTER SEVEN

COMPUTATIONAL MODELLING AND ANALYSIS

7.1 THE PRINCIPLE OF THE COMPUTATIONAL MODEL

As the Templeborough arc furnace installation and its supply (Part 2.2) were modelled physically in the laboratory (Part 2.3), it was a parallel aim of this research project to construct a digital model. The main benefits of such a model would be found in the study of various compensator arrangements and their control. This could be achieved prior to the construction of such systems in the laboratory.

The approach to the digital modelling was essentially simple: Values of current measured at the installation would be used to calculate volt-drops across known impedances. The voltage at any point in the network would thus be known with respect to some reference. Additional currents due to compensator connection would suitably modify the calculated voltages.

The details of such a technique are studied below.

7.1.1 The System to be Modelled

Chapter II, Part 2, describes the Templeborough system in detail, and shows how the impedance of the supergrid transformer SGT4 dominates in the supply impedance to the 33kV furnace busbar. The transformer windings were connected Y primary and Δ seconday. If per unit (p.u.) values are maintained the transformer voltage ratio need not concern us.

The form of the measured current waveforms is extremely non-sinusoidal (Figure 2.3), and a step-by-step solution of circuit equations required instataneous circuit equations rather than a treatment for RMS quantities.

The impedances for the supply system were given in Section 2.2.1 as percentage values to a 100MVA base. Referring all impedances to 33kV gives Z_{base} = 10.89 Ohms and the following ohmic impedances for the supply system at 50Hz:

$$Z_{tot} = (0 + j0.1307)\ \text{Ohms} \quad \text{275kV Supply}$$
$$+ (0.0565 + j2.595)\ \text{Ohms} \quad \text{SGT4}$$
$$+ (0.00218 + j0.01089)\ \text{Ohms} \quad \text{33kV Cable}$$

$$\therefore\ Z_{tot} = 0.0587 + j2.737\ \text{Ohms}$$

The total 50Hz inductance of the system is then 8.711 millihenries.

The three phase resistance and inductance network is shown in Figure 7.1. For balanced sinusoidal conditions the RMS values of i_1, i_2, i_3, i_4, i_5, and i_6 would be equal, and a one-line diagram would suffice. For this study of instantaneous unbalanced currents, all three primary and secondary circuits must be considered.

7.1.2 Measured and Calculated Currents and Voltages

The line currents corresponding to i_R, i_Y and i_B in Figure 7.1, and the phase voltages at those points, were measured and recorded by the CEGB (see Section 2.2.2 and Appendix B). The Δ-Y transformation described in Section 7.2 yields i_1, i_2 and i_3. The knowledge of these current values allows resistive volt drop to be calculated, and the value of di/dt at the same instant (see Section 8.3.2) may be used to obtain the values of voltages at all points in the network using:

$$\Delta V = Ri + L \frac{di}{dt}$$

for each branch.

Figure 7.2 gives the notation used to refer to currents and voltages at different points of the network. At this stage i_4, i_5, i_6 and derivatives are equal to i_R, i_Y, i_B and derivatives.

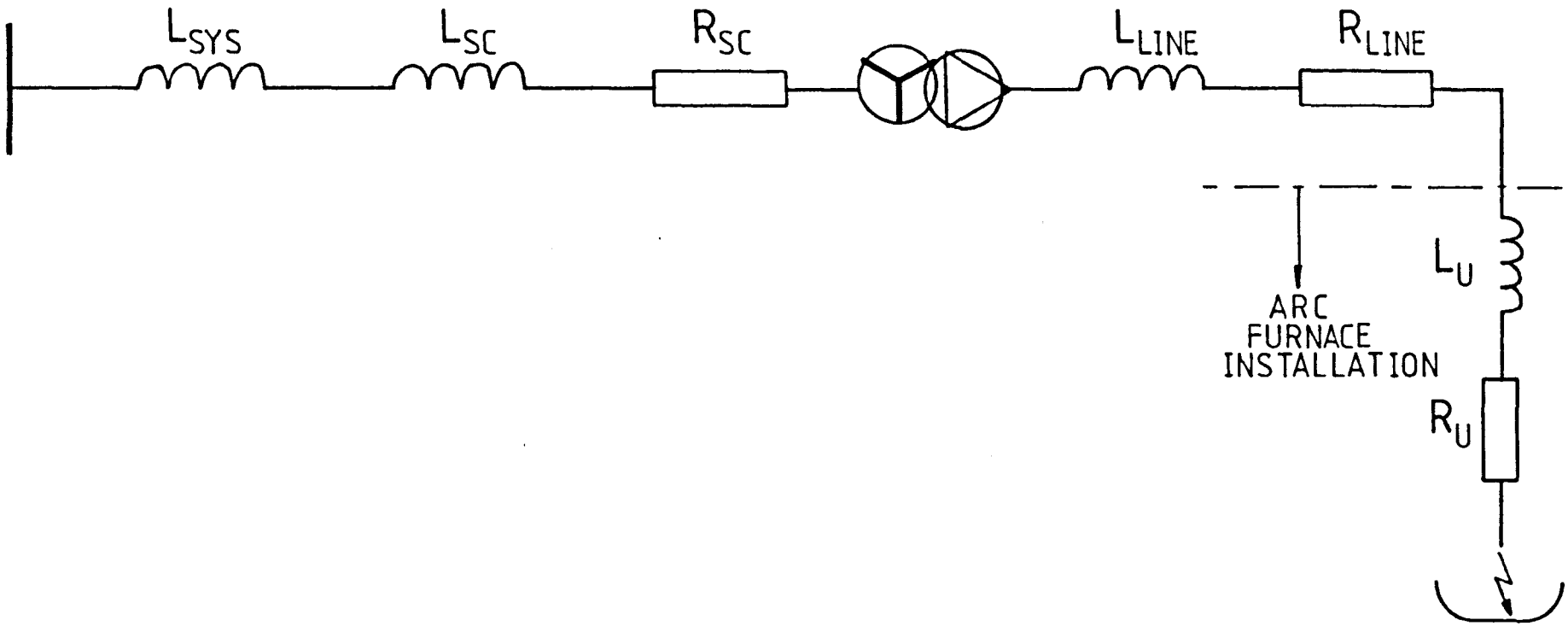


Fig. 7.1 : The resistance and inductance network for the computational model

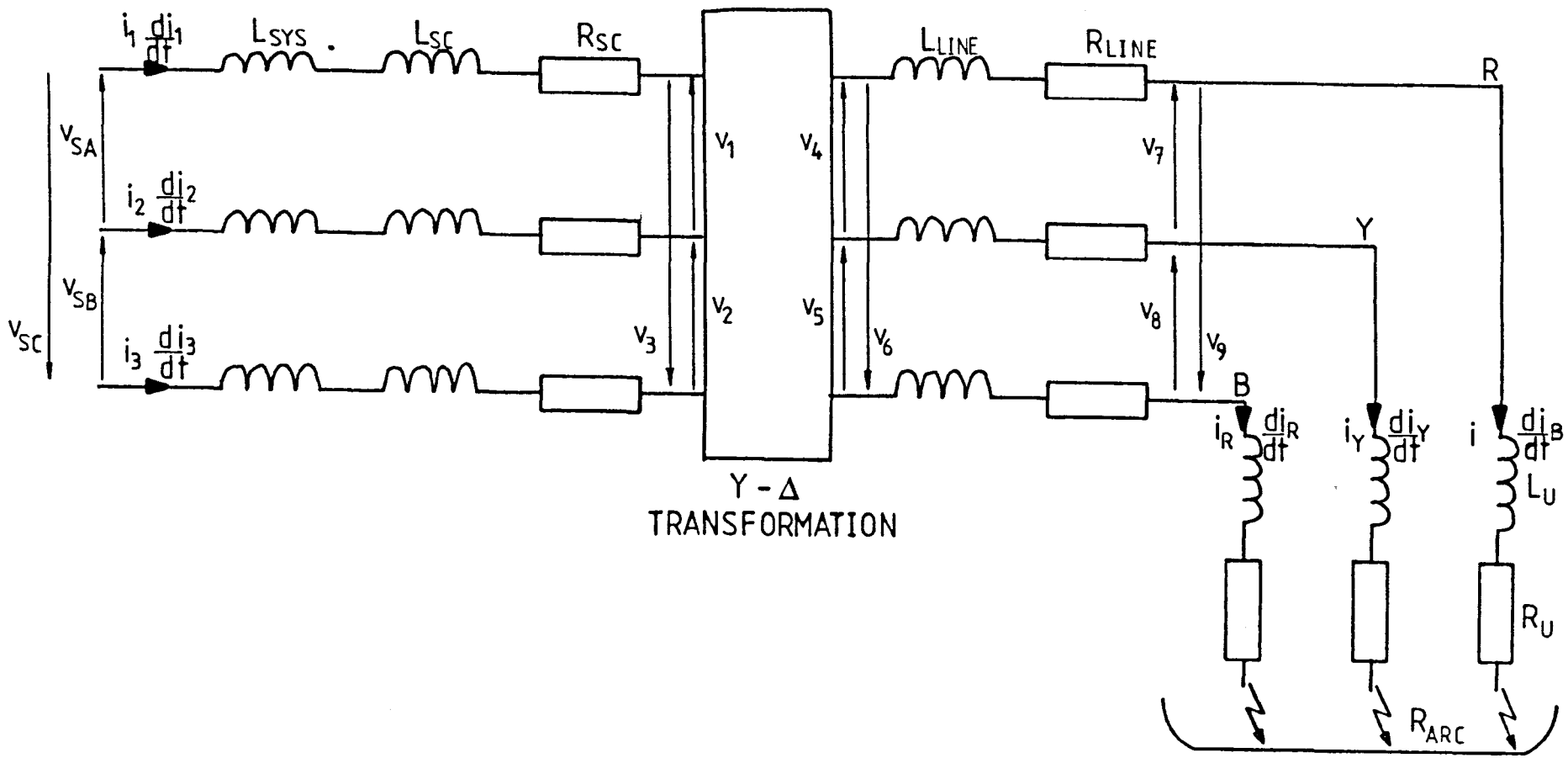


Fig. 7.2 : Definition of network voltages and currents

A step-by-step computational process was then used with the recorded furnace currents as the driving function. The same span of data as used for the physical laboratory model was used, without cubic spline interpolation between recorded values of current. The currents i_1, i_2, i_3 and their derivatives may be calculated from i_4, i_5, i_6 and their derivatives, via the Δ-Y current transformation (see Section 7.2). Then the voltages v_1, v_2, v_3 may be found at each step by subtracting a calculated voltage drop from the sinusoidal infinite busbar voltages v_{S1}, v_{S2} and v_{S3}.

i.e. $$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} v_{S1} \\ v_{S2} \\ v_{S3} \end{bmatrix} - R_{SC} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} - (L_S + L_{SC}) \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix}$$

Where $$v_{S1} = V_S \sin \omega t$$
$$v_{S2} = V_S \sin(\omega t + 2\pi/3)$$
$$v_{S3} = V_S \sin(\omega t - 2\pi/3)$$

and $$\omega = 100\pi$$

The Y-Δ voltage transformation from Section 7.2 then yields v_4, v_5 and v_6, and:

$$\begin{bmatrix} v_7 \\ v_8 \\ v_9 \end{bmatrix} = \begin{bmatrix} v_4 \\ v_5 \\ v_6 \end{bmatrix} - R_{CAB} \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix} - L_{CAB} \frac{d}{dt} \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix}$$

It is the 'flicker voltage' component of v_7, v_8 and v_9 that may be reduced by the addition of a suitable compensating network to modify i_4, i_5 and i_6. This is studied further in Part 7.4.

The computational process was carried out for each of the 2225 sequential samples in the 89 cycles used. The real time sampling interval of 800 microseconds was not relevant to the computational process.

The program to model the supply system carrying arc furnace currents was written in the FORTRAN language, and the full program listing is given in Appendix J. Comment statements within the listing explain its operation.

7.1.3 Inputs to the Arc Furnace Model

The main FORTRAN program, SYSMOD6 (Appendix J) was stored in compiled form, and run repeatedly with varying input parameters read from files of data set up for input to the program. The system, and files used, is described further in Appendix J.

The main requirement for the operation of the arc furnace numerical model is the accurate time-series data for arc furnace three-phase line currents and their first derivatives. A further three channels were used to input the recorded three-phase voltages for comparison with calculated values, giving:

CHANNEL:	1	2	3	4	5	6	7	8	9
INPUT:	v_R	v_Y	v_B	i_B	i_R	i_Y	$\frac{di_B}{dt}$	$\frac{di_R}{dt}$	$\frac{di_Y}{dt}$

The first derivatives of line current were calculated using the cubic spline fitting routines described in Appendix C. A further input file, 'SYSMOD OPTION', contained the required settings for program flow bit settings, results formats and iteration loop limits.

7.1.4 The Phase Angle 'δ'

When the current drawn by the arc furnace installation is low, the voltages $v_{7,8,9}$ will be practically in phase with the supply voltages $v_{S1,S2,S3}$. The circuit impedance is dominantly inductive, and as the current drawn from the supply increases so $v_{7,8,9}$ will lag $v_{S1,S2,S3}$ by an increasing amount.

The CEGB recordings of current, $i_{R,Y,B}$, were accompanied by simultaneous recordings of phase voltage, $v_{R,Y,B}$. The voltage recordings were used to generate line voltage values $v_{RY,YB,BR}$ for comparison with the calculated values $v_{7,8,9}$. The recordings alone give no indication of the phase of the recorded currents relative to infinite busbar voltage. The varying phase angle which may be observed between $i_{R,Y,B}$ and $v_{R,Y,B}$ is a function of the changing value of the unknown impedance Z_U (see Figure 3.10).

where $$Z_U = R_{ARC} + R_U + jX_U$$

The values of $i_{R,Y,B}$ and $v_{7,8,9}$ will both vary in phase relative to $v_{S1,S2,S3}$; and a nominal angle of 'δ' radians may be attached to the difference between the first zero crossings of i_R and v_{S1}.

Running the full program for each of the 2225 points will generate the calculated values of $v_{7,8,9}$ for 89 cycles. If 'δ' has been set incorrectly then $v_{7,8,9}$ will be out of phase with the voltage $v_{RY,YB,BR}$ obtained from the recordings. This phase error was used to adjust 'δ' iteratively until the error magnitude was reduced below a set average limit of 0.1 radians per cycle, giving

$$'\delta' = -0.235 \text{ radians}$$

which is a phase angle of 14 degrees.

7.2 Y-Δ TRANSFORMER CURRENT AND VOLTAGE TRANSFORMATIONS

Figure 7.3(a) shows the primary and secondary currents and voltages at the terminals of a Y-Δ transformer, and gives a notation to be used for the winding voltages and currents where necessary.

Figure 7.3(b) shows the coil sense notation to be used.

7.2.1 Current Transformation

The star point of the load on the secondary windings is the arc furnace melt pool. The melt pool is insulated from surrounding metal work by refractory brick, and there is no 'neutral' return to the Δ winding. Therefore there can be no zero sequence component in the secondary circuit, and:

$$i_X + i_Y + i_Z = 0$$

and $$i_4 + i_5 + i_6 = 0$$

If $$v_1 = N v_4$$

Then $v_4 = \frac{\sqrt{3}}{N} v_B$ and $i_Y = \frac{N}{\sqrt{3}} i_2$, where N is the turns ratio.

For the secondary circuit:

$$i_4 = i_Y - i_X$$
$$i_5 = i_Z - i_Y$$
$$i_6 = i_X - i_Z$$

Giving,

$$i_X = \frac{i_6 - i_4}{3} \; ; \qquad i_Y = \frac{i_4 - i_5}{3} \; ; \qquad i_Z = \frac{i_5 - i_6}{3}$$

Using the vectors

$$I_{XYZ} = \begin{bmatrix} i_X \\ i_Y \\ i_Z \end{bmatrix} \quad \text{and} \quad I_{456} = \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix}$$

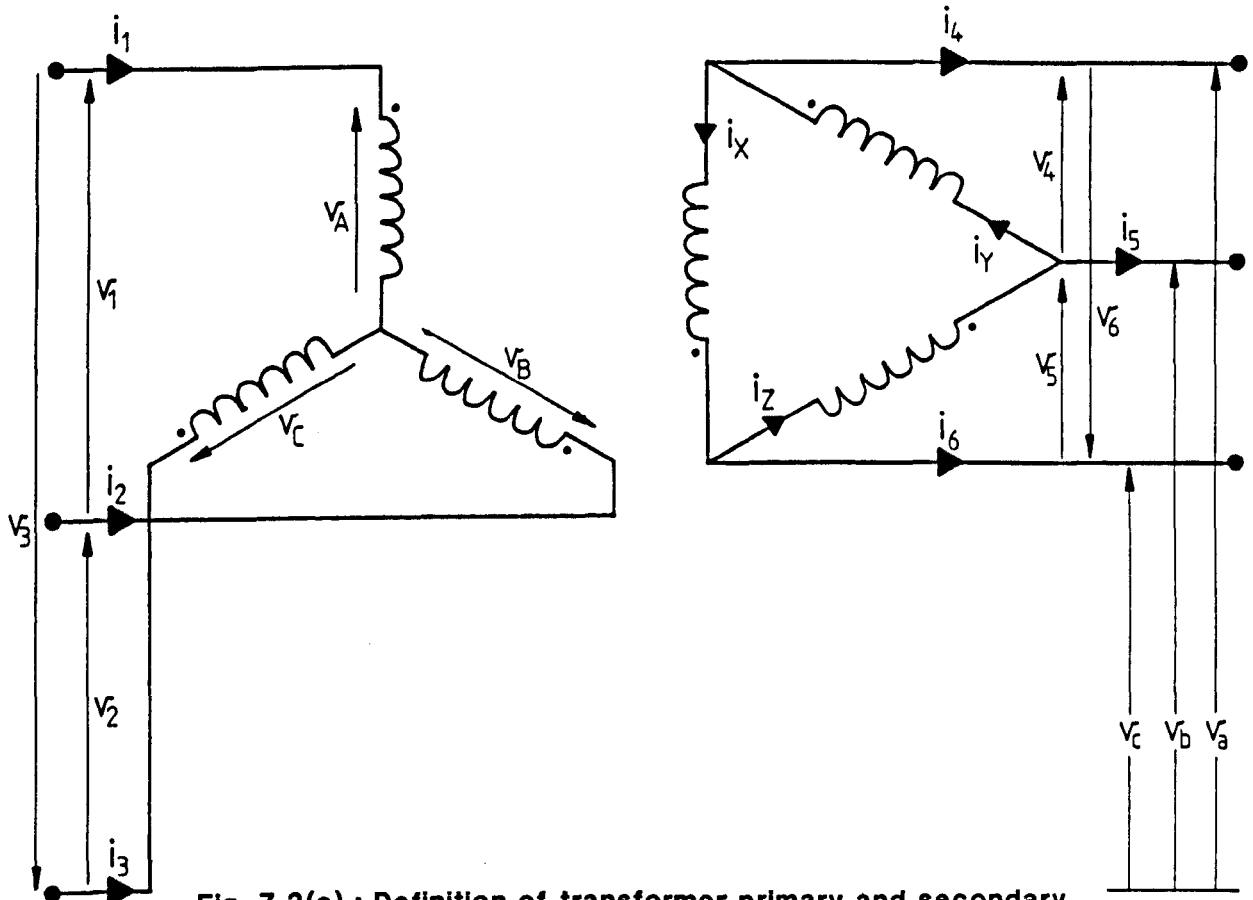


Fig. 7.3(a) : Definition of transformer primary and secondary winding voltages and currents

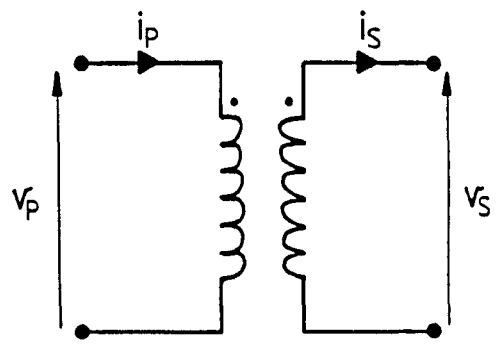


Fig. 7.3(b) : Transformer winding voltage - current conventions

We have,

$$I_{XYZ} = \frac{1}{3}[C]\, I_{456}$$

where [C] is the matrix $\begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$

But, $I_{123} = \frac{\sqrt{3}}{N} I_{XYZ}$, where N is the turns ratio.

Then, for N = 1,

$$I_{123} = \frac{1}{\sqrt{3}}[C]\, I_{456}$$

It may also be shown that, for N = 1,

$$I_{456} = [C_t]\, I_{123}$$

where $[C_t]$ is the transposed matrix of [C].

7.2.2 Voltage Transformation

Using the vector and matrix notation for

$$V_{ABC} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}, \quad V_{123} = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \quad \text{and} \quad V_{645} = \begin{bmatrix} v_6 \\ v_4 \\ v_5 \end{bmatrix}$$

then,

$$V_{ABC} = \frac{1}{3}[C]\, V_{123}$$

But,

$$V_{645} = \frac{\sqrt{3}}{N} V_{ABC}$$ where N is the turns ratio.

Then, for N = 1,

$$V_{645} = \frac{1}{\sqrt{3}} [C] V_{123}$$

It may also be shown that, for N = 1,

$$V_{123} = -\sqrt{3} [C_t] V_{645}$$

$$V_{abc} = \frac{1}{\sqrt{3}} [C_t] V_{ABC}$$

and $V_{ABC} = \sqrt{3} [C] V_{abc}$

where $[C_t]$ is the transposed matrix of [C].

7.2.3 Current Derivative Transformation

For each of the primary-secondary coil pairs as shown in Figure 7.3(b) the mutual inductance, M, relates voltage and current such that:

$$V_P = -M \frac{dI_S}{dt} \quad \text{and} \quad V_S = -M \frac{dI_P}{dt}$$

Giving,

$$\frac{-V_P}{dI_S/dt} = \frac{-V_S}{dI_P/dt} = M$$

For N = 1, $I_S = I_P$

$$V_S = V_P$$

and $$\frac{dI_S}{dt} = \frac{dI_P}{dt}$$

The current transformations established in Section 7.2.1 therefore hold for the first order differentials of I_{123}, I_{456} and I_{XYZ}.

7.3 PERFORMANCE OF THE COMPUTATIONAL ARC FURNACE MODEL

Comparisons of measured voltage waveform distortion have been made (Sections 2.4.3 and 5.3.1) by studying the distribution of each signal's power spectral density. The modulation frequencies of particular interest for a 'flicker' analysis are contained in the 0-30Hz sidebands of the 50Hz supply voltage power spectrum.

The computational model, described in this Chapter, used measured values of line current and its first derivative to calculate a distorted supply waveform. The comparisons between real and calculated distorted voltages are now presented, firstly in the frequency domain and secondly in the time domain. Finally, the results of demodulating the supply voltage waveform are shown to require careful interpretation.

7.3.1 Results Comparison using Power Spectra

Only the phase voltages at the Templeborough 33kV busbars were measured and recorded by the CEGB. Section 2.2.2 showed how the study of line voltages calculated from these phase voltages is valid. The line voltages derived from the phase voltage recordings are denoted MVRY MVYB MVBR, and their power spectra are given in Figure 7.4(a)(b)(c).

The computational model described in 7.1.2. and listed in Appendix J, produced the line voltages CVRY CVYB CVBR representing those occurring at the 33kV busbar. The power spectra of MVRY and CVRY are given in Figure 7.5(a) and (b) respectively. The equivalent comparisons for MVYB/CVYB and MVBR/CVBR are not presented, because the red-yellow line voltage spectra compared in Figure 7.5 are representative of the three-phase voltages.

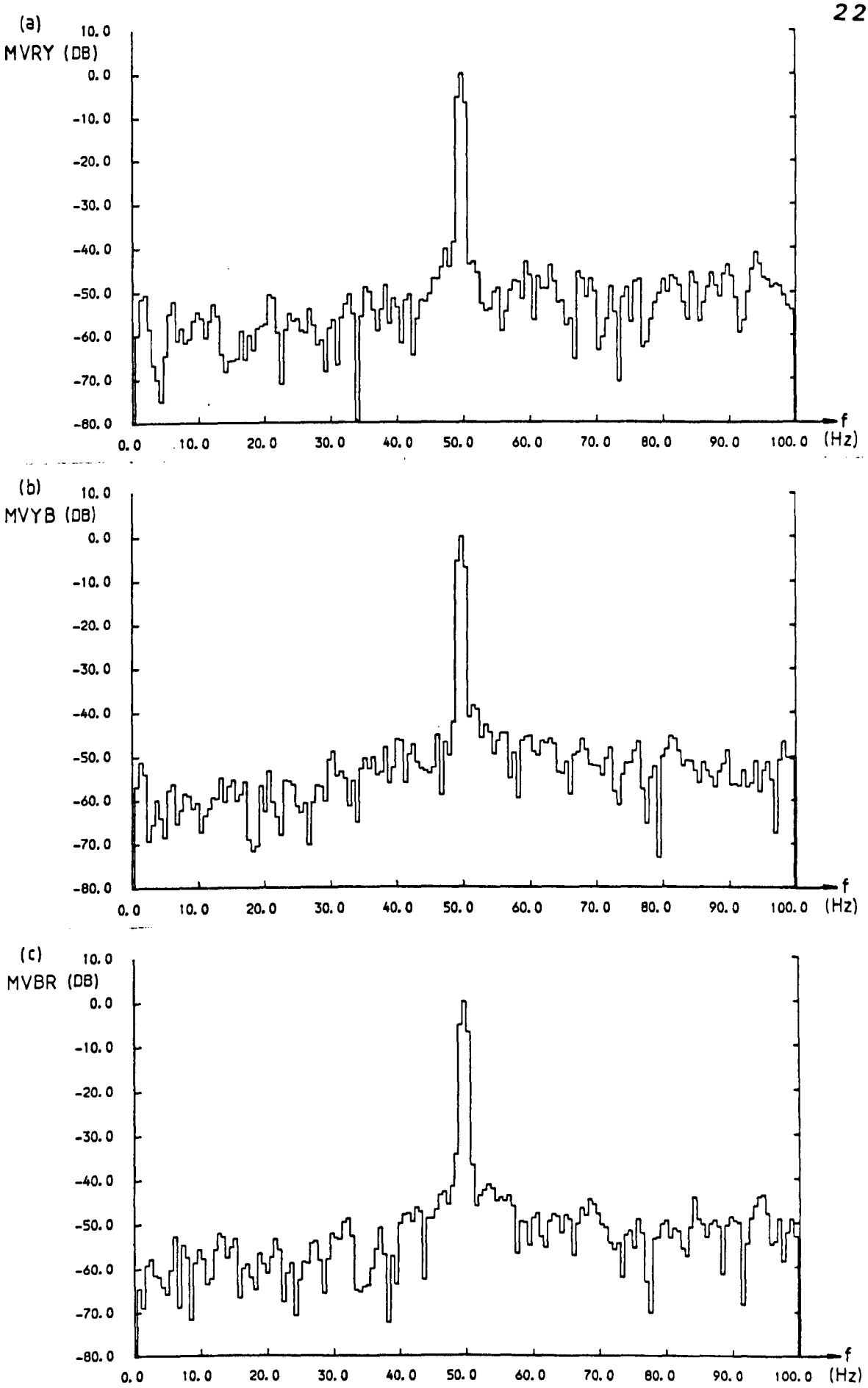


Fig. 7.4 : 0-100Hz power spectrum of line voltages derived from measured phase voltages

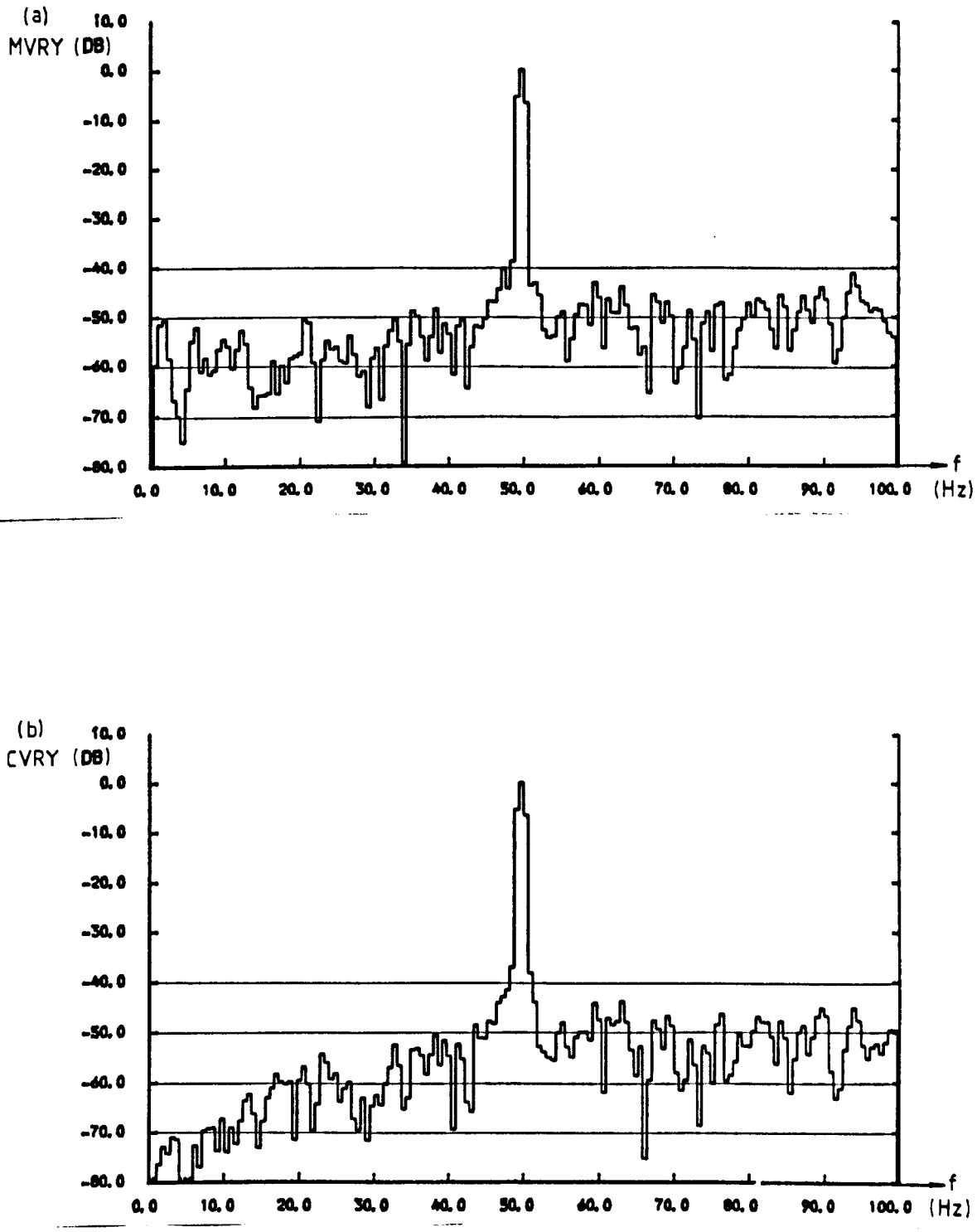


Fig. 7.5 : Comparison of power spectra of measured and calculated arc furnace line voltages MVRY and CVRY

Points arising from a study of Figure 7.5 are:

(i) The upper modulation sideband of CVRY has a power spectral density distribution very close to that of MVRY. The 'peak and trough' formation of the spectrum in this band is almost identical, with the most obvious differences being in the absolute power levels of a few frequency blocks (e.g. 57Hz, 66.5Hz, 77Hz, 92Hz).

(ii) The lower modulation sideband of CVRY is far less in agreement with that of MVRY. The most striking difference occurs in the absolute frequency range 1Hz to 20Hz. Here the power spectral components are, on average, some 20dB lower for CVRY than those in MVRY.

(iii) Modulation frequencies that are most important for any 'flicker' study have been calculated with reasonable accuracy. There are some discrepancies, but it is not necessary for CVRY exactly to equal MVRY. CVRY will be a perfectly satisfactory reference distorted voltage from which to proceed with a study of reactive compensation. Reactive compensation will modify the power spectrum of CVRY and allow changes in the powers of the modulating frequencies to be assessed for a relative improvement factor.

7.3.2 Results Comparison in the Time Domain

Early work placed greater significance on the distorted voltage waveform rather than its power spectrum[8,66]. The 33kV phase voltages from the recorded Templeborough data were shown in Figure 2.3 as MVR, MVY and MVB. Each of these voltages shows severe distortion from the sinusoidal form, and the distortion is particularly noticeable about the voltage peaks.

The computational model described in Section 7.1.2 and listed in Appendix J, produced the line voltages CVRY CVYB CVBR representing those occurring at the 33kV busbar. MVRY is repeated for comparison with CVRY over ninety 50Hz cycles in Figure 7.6. The corresponding waveforms for MVYB/CVYB and MVBR/CVBR are not presented, because the red-yellow voltage is representative of the form of the other line voltages.

A cursory study of Figure 7.6 shows that the sudden and severe voltage changes for MVRY are absent from CVRY, and suggests that the modulation voltage, V_f, is far lower for CVRY.

The first four 50Hz cycles of MVRY and CVRY are presented in more detail in Figure 7.7, which clearly shows the greater magnitude of MVRY's departures from a sinusoidal form.

The disagreement between these measured and calculated line voltages is then most pronounced for high frequency disturbances of the sinusoidal waveform. Lower frequency modulation of the 50Hz supply voltage cannot be discerned from Figure 7.7, but closer inspection of Figure 7.6 shows that the sub-harmonic modulation is of a similar magnitude for both waveforms. This is highlighted when MVRY and CVRY are given in the time-compressed form of Figure 7.8. The quantitative study in Section 7.3.1 shows that the power levels of modulating frequencies between 1 and 30Hz are almost identical.

7.3.3 Demodulation

Modulating frequencies causing lamp flicker may be seen in greater detail in the time domain if the 50Hz fundamental 'carrier' waveform is removed from the time series data.

Such a process was easily accomplished on the mainframe computer for the 90 cycles of data used by both the physical and computational model.

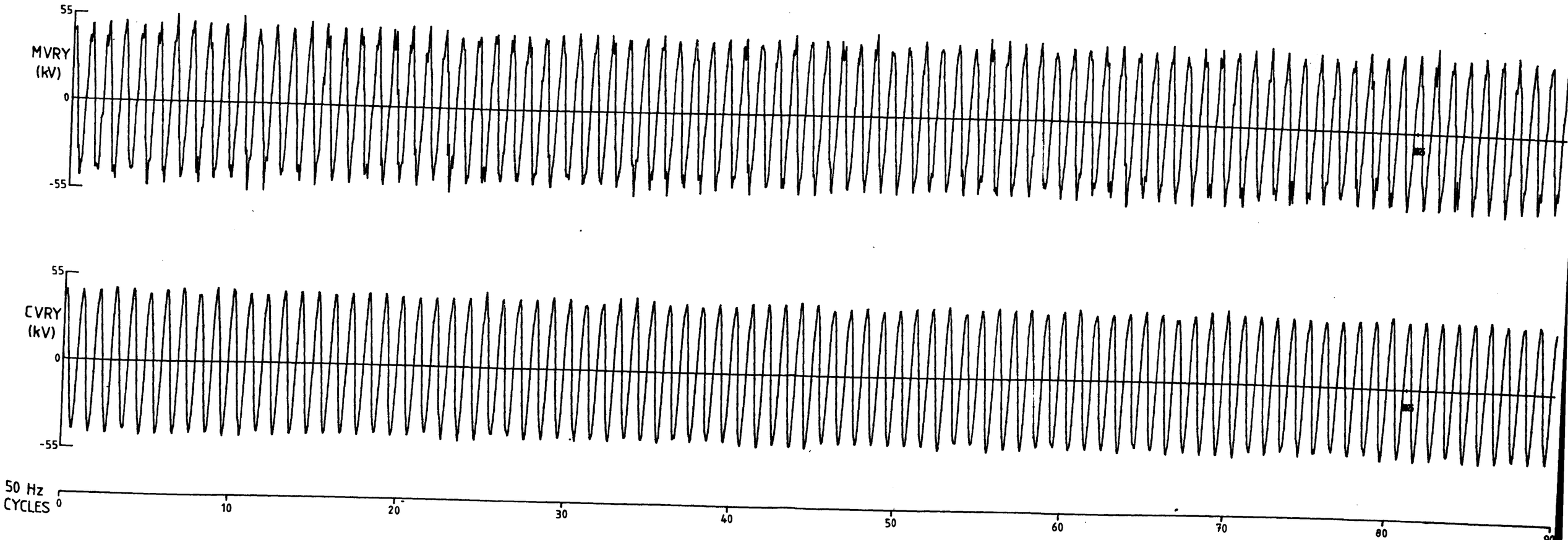


Fig. 7.6 : Comparison of MVRY and CVRY over 90 cycles

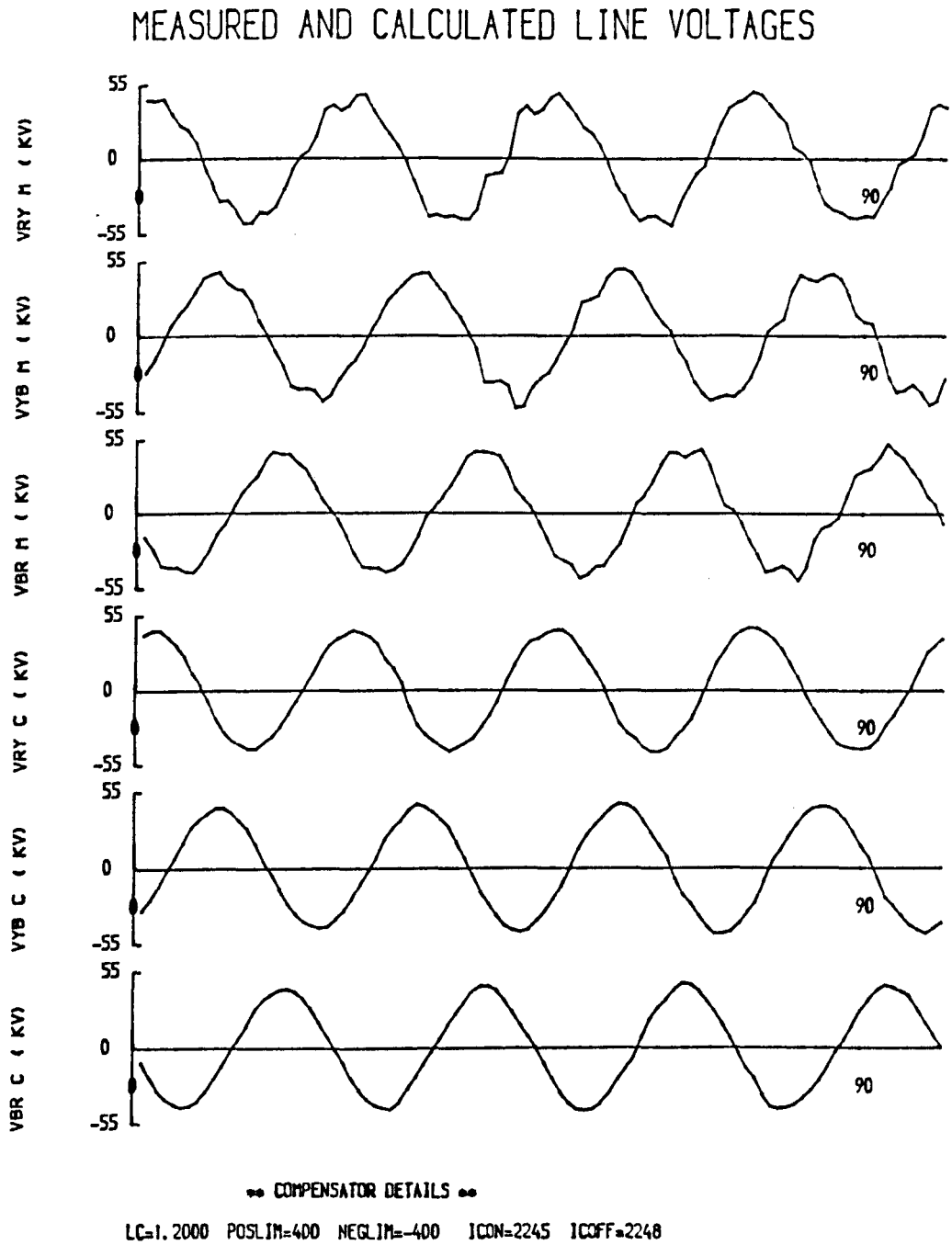


Fig. 7.7 : Comparison of MVRY and CVRY over 4 cycles

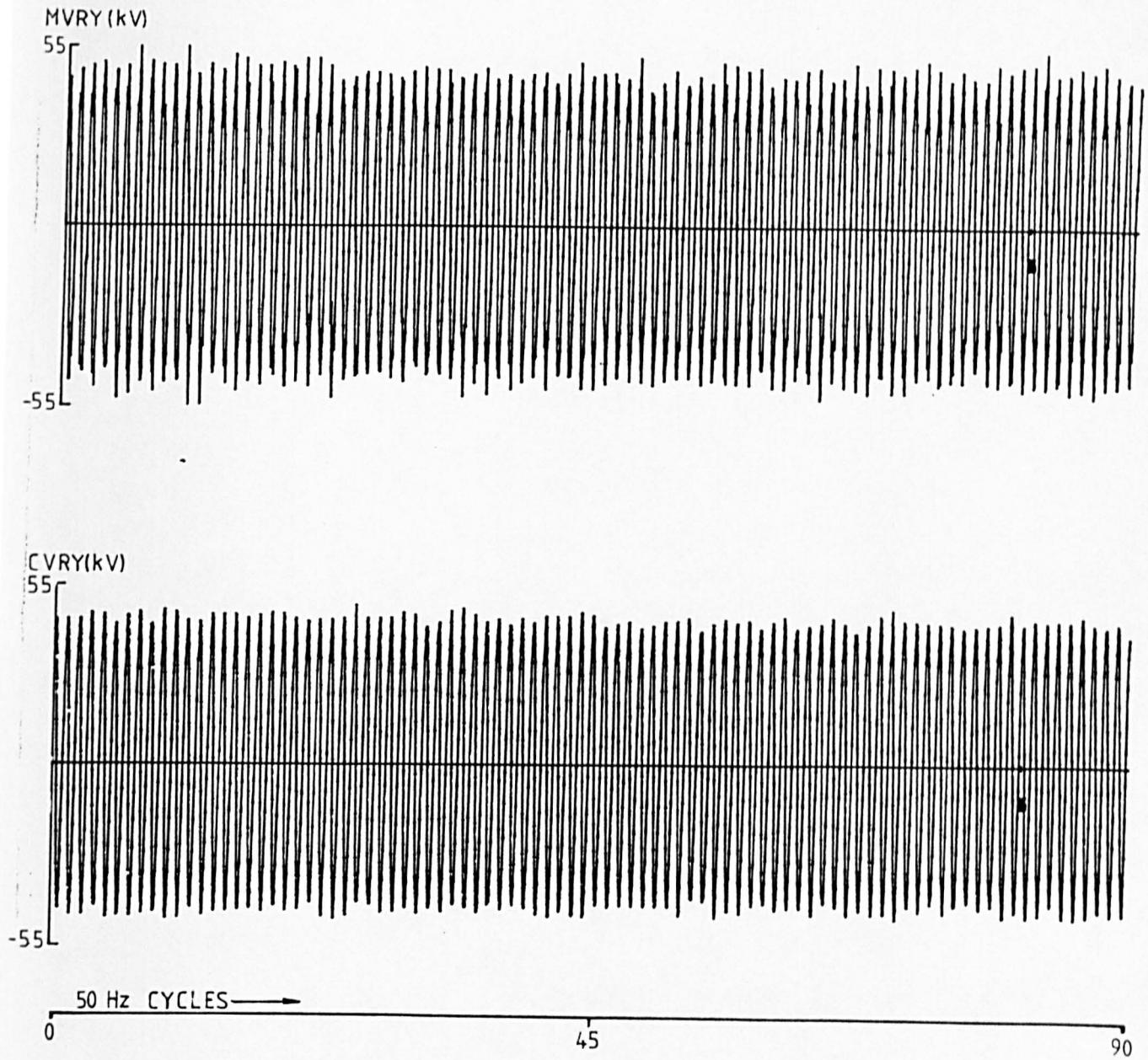


Fig. 7.8 : Comparison of MVRY and CVRY over compressed 90 cycles

The FORTRAN subroutine DEMOD called from the main SYSMOD6 program effected numerical demodulation of any waveform with a dominant fundamental frequency. The listing of DEMOD, together with all other subroutines called from SYSMOD6 is given in Appendix J.

Figure 7.9 presents the original and calculated line voltage as for Figure 7.6, except that a 50.06Hz sinusoid with RMS value 33.41kV has been subtracted from MVRY and CVRY to give the demodulated voltages DMVRY and DCVRY. The greater magnitude of distortions for MVRY is once again emphasised by this time-domain presentation. The time-compressed plots in Figure 7.10 begin to show how the lower frequency fluctuations are not dissimilar for DMVRY and DCVRY.

Finally the power spectral density plots for DMVRY and DCVRY in Figure 7.11 show that the numerical demodulation process has succeeded in removing only the 50Hz 'carrier' frequency. The remaining sidebands in the 1 to 100Hz band are identical to those presented in Figure 7.5, except that they are presented in dBs relative to the 3rd harmonic component rather than the 50Hz fundamental.

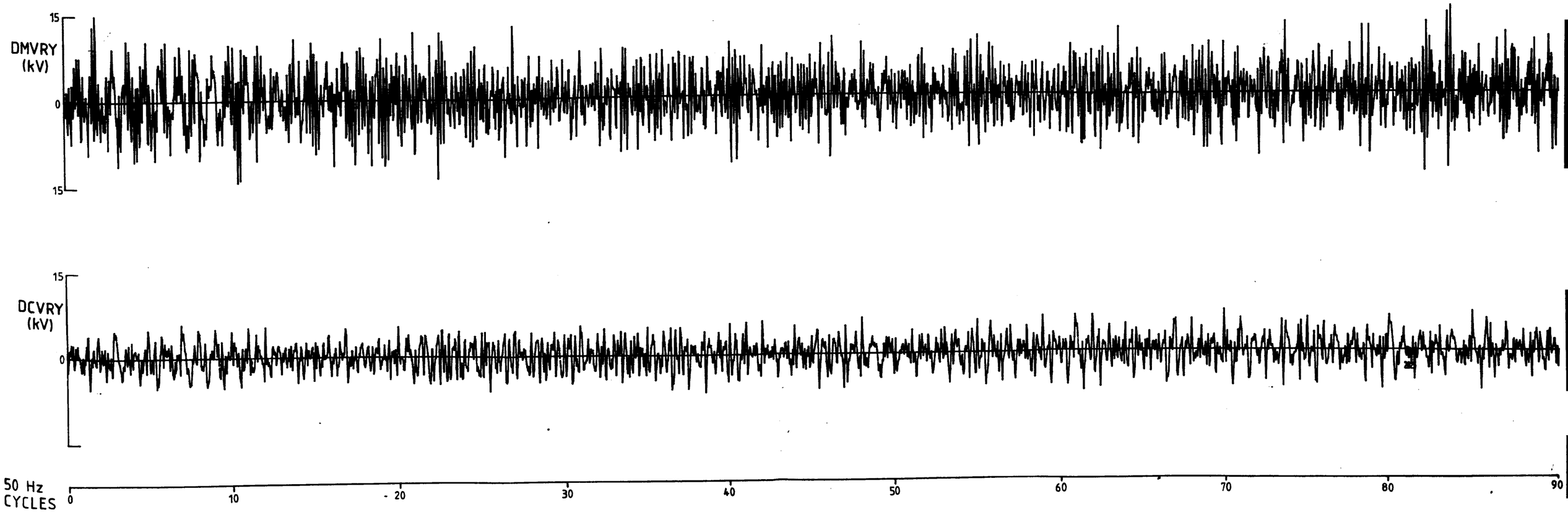


Fig. 7.9 : Comparison of demodulated measured and calculated voltages DMVRY, DCVRY over 90 cycles

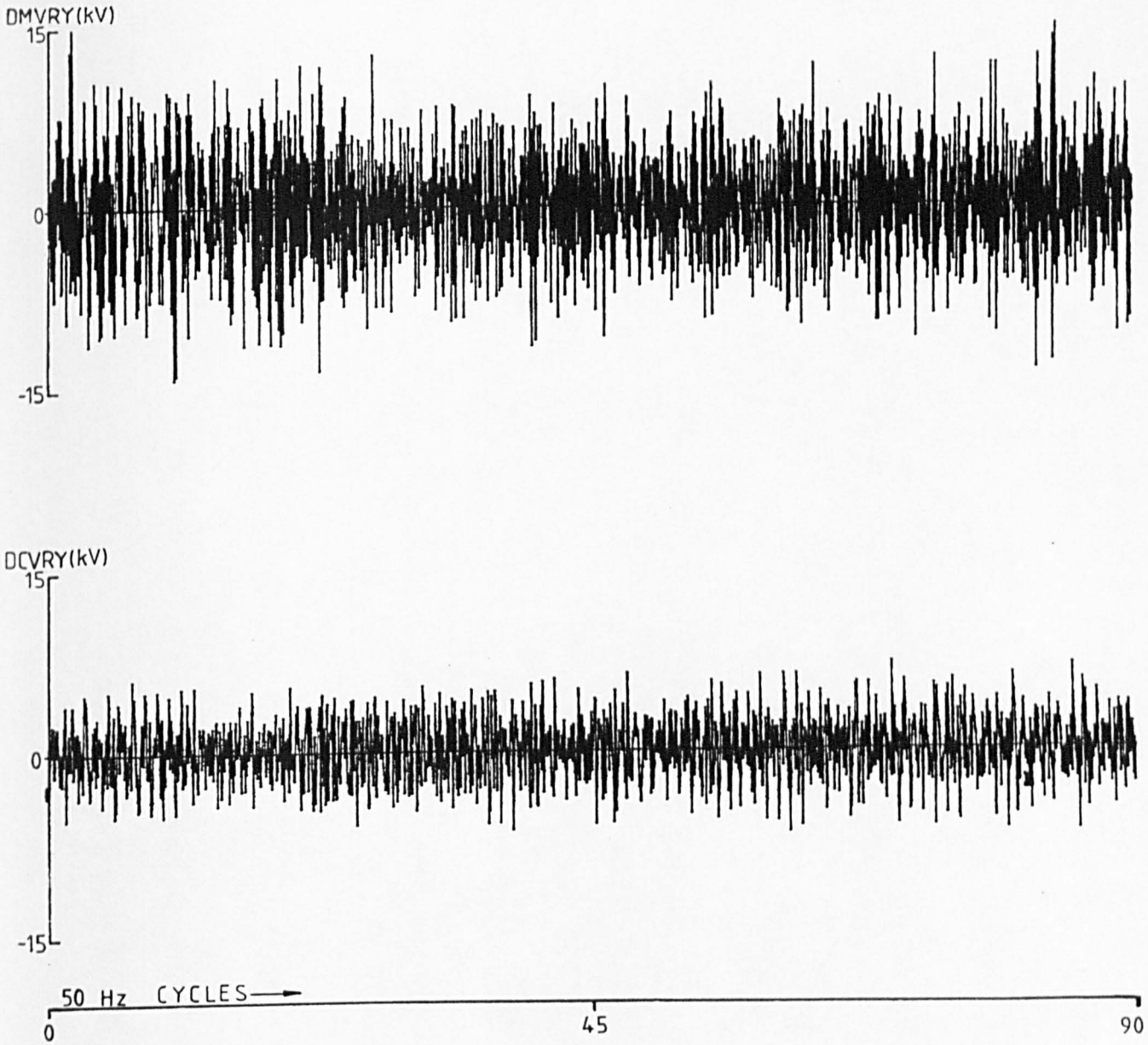


Fig. 7.10 : Comparison of DMVRY and DCVRY over compressed 90 cycles

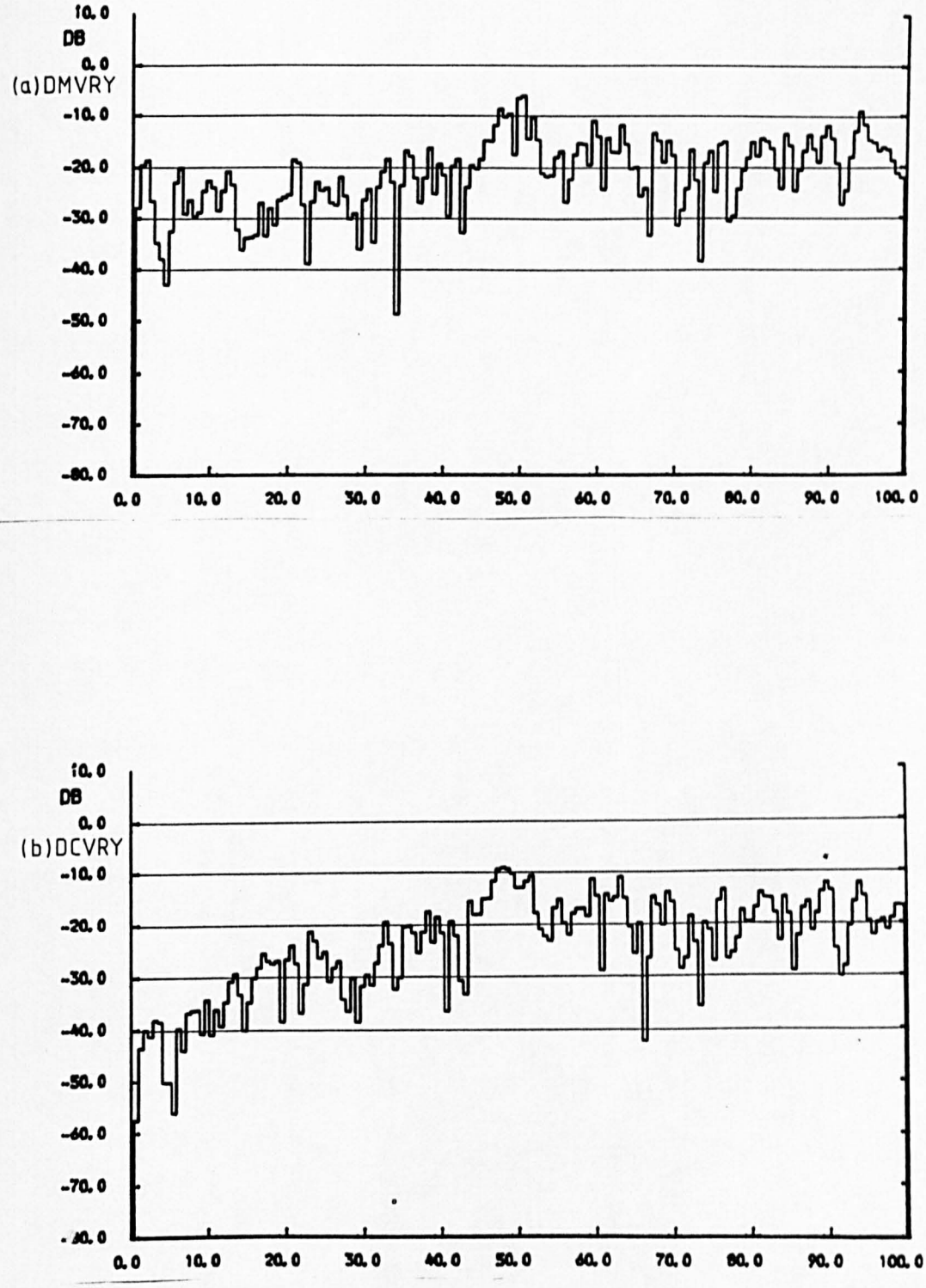


Fig. 7.11 : Comparison of power spectra of DMVRY and DCVRY

7.4 COMPUTATIONAL MODELLING OF A TCR COMPENSATOR

Adding a compensating shunt inductance to the computational arc furnace model described above will modify the line currents drawn from the source.

An algorithm to calculate the required conduction angles for a TCR compensator is easily constructed on this totally digital model. Then, when inductive conduction in the compensator has been initiated, a first order differential equation must be solved using a step-by-step approach as part of the digital model's function.

Correct solution of the differential equation shows the expected compensator branch current waveforms, and modification of the line currents drawn from the system. An improvement factor may then be calculated for different combinations of TCR compensator ratings and control algorithm.

7.4.1 TCR Compensator Circuit Definitions

The compensator is shunt connected with the arc furnace load. The line voltages applied to the compensator are then v_7, v_8 and v_9 (the vector V_{789}). The currents drawn through the supply impedances will no longer be just I_{RYB}, since they will have been modified by the compensator line currents.

Figure 7.12 defines the computational model parameters when a shunt-connected compensator is included. The currents i_4, i_5 and i_6 are therefore defined, using vector notation, as:

$$I_{456} = I_{RYB} + I_{LCRYB}$$

also $$I_{LCRYB} = -[C]\, I_{LC123}$$

the same algebraic equations apply to the derivatives of the currents above.

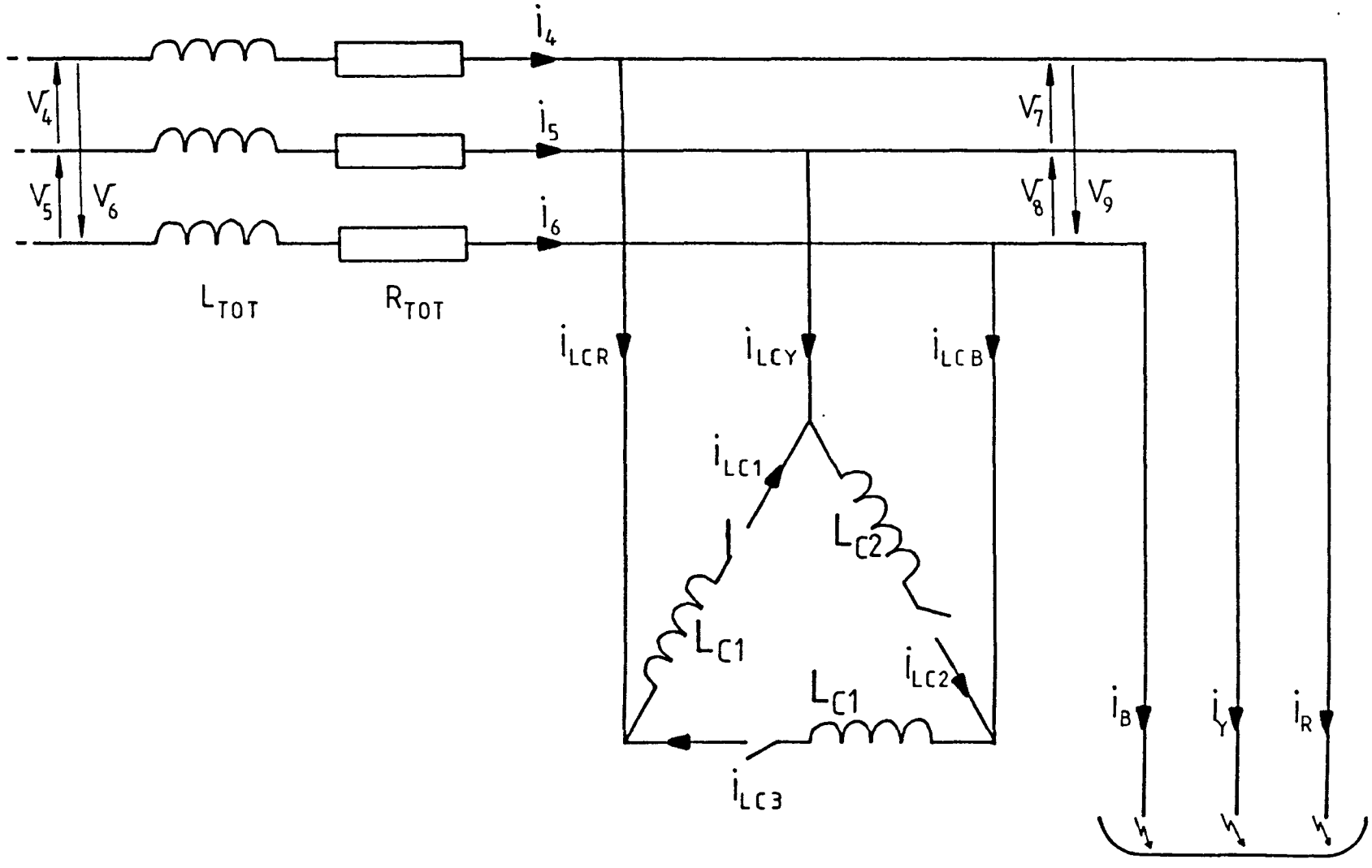


Fig. 7.12 : Definition of computational model voltages and currents when a shunt TCR compensator is included

7.4.2 The Differential Equations of Compensator Currents

Simple circuit theory gives the relationship between the parameters defined in Figure 7.12:

$$v_7 = v_4 - \left[R_{sum}\,(i_R - i_Y + i_{LCR} - i_{LCY}) + L_{sum}\left(\frac{di_R}{dt} - \frac{di_Y}{dt} + \frac{di_{LCR}}{dt} - \frac{di_{LCY}}{dt}\right)\right]$$

.....Equation 7A

$$v_8 = v_5 - \left[R_{sum}\,(i_Y - i_B + i_{LCY} - i_{LCB}) + L_{sum}\left(\frac{di_Y}{dt} - \frac{di_B}{dt} + \frac{di_{LCY}}{dt} - \frac{di_{LCB}}{dt}\right)\right]$$

.....Equation 7B

$$v_9 = v_6 - \left[R_{sum}\,(i_B - i_R + i_{LCB} - i_{LCR}) + L_{sum}\left(\frac{di_B}{dt} - \frac{di_R}{dt} + \frac{di_{LCB}}{dt} - \frac{di_{LCR}}{dt}\right)\right]$$

.....Equation 7C

But $V_{789} = L_c \frac{dI_{LC123}}{dt}$ and $I_{LCRYB} = -[C]\, I_{LC123}$

Therefore

$$\frac{di_{LC1}}{dt} = \frac{1}{L_c}\left\{V_4 - R_{sum}\left[i_R - i_Y + (2i_{LC1} - i_{LC2} - i_{LC3})\right] - L_{sum}\left[\frac{di_R}{dt} - \frac{di_Y}{dt}\right]\right\} - \frac{L_{sum}}{L_c}\left[2\frac{di_{LC1}}{dt} - \frac{di_{LC2}}{dt} - \frac{di_{LC3}}{dt}\right]$$

.....Equation 7D

$$\frac{di_{LC2}}{dt} = \frac{1}{L_c}\left\{V_5 - R_{sum}\left[i_Y - i_B + (-i_{LC1} + 2i_{LC2} - i_{LC3})\right] - L_{sum}\left[\frac{di_Y}{dt} - \frac{di_B}{dt}\right]\right\} - \frac{L_{sum}}{L_c}\left[-\frac{di_{LC2}}{dt} + 2\frac{di_{LC2}}{dt} - \frac{di_{LC3}}{dt}\right]$$

.....Equation 7E

and

$$\frac{di_{LC3}}{dt} = \frac{1}{L_c}\left\{V_6 - R_{sum}\left[i_B - i_R + (-i_{LC1}-i_{LC2}+2i_{LC3})\right] - L_{sum}\left[\frac{di_B}{dt} - \frac{di_R}{dt}\right]\right\} - \frac{L_{sum}}{L_c}\left[-\frac{di_{LC1}}{dt} - \frac{di_{LC2}}{dt} + 2\frac{di_{LC3}}{dt}\right]$$

.....Equation 7F

The equations above have the following solutions for

$\frac{di_{LC1}}{dt}$, $\frac{di_{LC2}}{dt}$ and $\frac{di_{LC3}}{dt}$:

$$\frac{di_{LC1}}{dt} = \frac{1}{L_c+3L_{sum}}\left\{V_4 - R_{sum}\left[i_R-i_Y+(2i_{LC1}-i_{LC2}-i_{LC3})\right] - L_{sum}\left[\frac{di_R}{dt} - \frac{di_Y}{dt}\right]\right\}$$

.....Equation 7G

$$\frac{di_{LC2}}{dt} = \frac{1}{L_c+3L_{sum}}\left\{V_5 - R_{sum}\left[i_Y-i_B+(-i_{LC1}+2i_{LC2}-i_{LC3})\right] - L_{sum}\left[\frac{di_Y}{dt} - \frac{di_B}{dt}\right]\right\}$$

.....Equation 7H

$$\frac{di_{LC3}}{dt} = \frac{1}{L_c+3L_{sum}}\left\{V_6 - R_{sum}\left[i_B-i_R+(-i_{LC1}-i_{LC2}+2i_{LC3})\right] - L_{sum}\left[\frac{di_B}{dt} - \frac{di_R}{dt}\right]\right\}$$

.....Equation 7I

Provided that

$$V_4 + V_5 + V_6 = 0,$$

$$i_R + i_Y + i_B = 0$$

and $\frac{di_R}{dt} + \frac{di_Y}{dt} + \frac{di_B}{dt} = 0$

Equations 7G, 7H and 7I above apply only to the circuit shown in Figure 7.12. In the arc furnace model described in Part 7.1 and 7.2, this circuit only included voltages, currents and impedances from the secondary terminals of the super grid transformer (SGT).

Voltage and current transformations (Part 7.2) were necessary to include the transformer short circuit impedance and the system impedance in the model, since they were positioned in the transformer primary circuit.

To incorporate primary circuit impedances into the differential equations 7G, 7H and 7I above would bring many more terms into the equations, requiring proportionally greater computing effort. To avoid this, the SGT short circuit impedance was transferred to its secondary circuit.

The secondary circuit parameters were then lumped as

$$R_{sum} = R_{SC} + R_{LINE}$$

and $$L_{sum} = L_{SC} + L_{LINE}$$

Treating v_4,v_5 and v_6 as the infinite busbar then ignored L_{SYS} and eliminated the need to perform the voltage and current transformations.

This simplified computational model of the arc furnace and supply system produced distorted '33kV equivalent' voltage waveforms and power spectra that were almost indistinguishable from those produced by the complete model described in Part 7.1 and 7.2.

7.4.3 Step-by-Step Solution of Compensator Differential Equations

In equations 7G, 7H and 7I above, i_R, i_Y, i_B, $\frac{di_R}{dt}$, $\frac{di_Y}{dt}$ and $\frac{di_B}{dt}$ are known variables - as they form the input to the arc furnace model described in Parts 7.1 and 7.2. R_{sum} and L_{sum} are the resistance and inductance shown in Figure 7.4. For each computational step both I_{LC123} and $\frac{dI_{LC123}}{dt}$ must be found before V_{789} may be obtained from equations 7A, 7B and 7C.

For the first step at which current flows in a compensator branch,

$$i_{LC}(n) = 0 \quad \text{and} \quad \frac{di_{LC}}{dt}(n) = \frac{v_L}{L_C}$$

For the next step-by-step calculation,

$i_{LC}(n+1)$ and $\frac{di_{LC}}{dt}(n+1)$ can only be calculated from $i_{LC}(n)$ and $\frac{di_{LC}}{dt}(n)$.

Equations 7G, 7H and 7I are first-order differential equations in the explicit form such that

$$y' = f(x,y)$$

Step-by-step numerical solution of such an equation evaluates y at

$$t = t_0$$
$$t = t_1 = t_0 + \Delta t$$
$$t = t_2 = t_1 + \Delta t$$

'Δt' is the step size, and here is fixed on the data sampling interval of 800 microseconds.

The Euler-Cauchy method[120] crudely calculates

$$y(n+1) = y + \Delta t y'$$

This first order method results in truncational errors of the order h^2 per step. An improved Euler-Cauchy method reduces these errors to order h^3, and the important Runge-Kutta method gives truncation errors of order h^5 per step[120].

Four auxiliary values, A,B,C and D, are calculated for each step of the numerical process, and they combine to give

$$y(n+1) = y(n) + \frac{1}{6}\left[A(n) + 2B(n) + 2C(n) + D(n)\right]$$

The values for A(n), B(n), C(n) and D(n) are described generally in the literature[120] and are shown for this particular application in the FORTRAN program listing in Appendix J.

Where variables at t(n) are required, the known values of i_R, i_Y, i_B, $\frac{di_R}{dt}$, $\frac{di_Y}{dt}$ and $\frac{di_B}{dt}$ are used. Similarly, values for t(n+1) will use the next set of values from the input data. However, the half-step values at $t(n+\Delta t/2)$ are always unknown, and these are calculated at each stage by simple linear interpolation between t(n) and t(n+1).

7.4.4 Compensator Control

A separate input file to the SYSMOD6 program contained details of the required compensator parameters. These controlled the compensator rating and conduction angle.

Control of conduction in the compensator branch inductances followed an integration procedure. The line voltage zero-crossing points were used to initiate integrations and conduction in the relevant compensator branch was allowed when a pre-set limit was reached. The equations given in Section 7.4.2 were then used to calculate the compensator currents until 'commutation' at current-zero.

The integration procedure used to calculate 'firing angle' in the computer model was first set up as a simple integration of line voltage. Ideally this control method would have been extended to model the system used for the laboratory analogue model, but further work is required to achieve this.

The file 'SYSCOMP OPTION' contained the following parameters defining the TCR compensator.

L_C - The compensator branch inductance (Henries)
POSLIM - The positive integration limit (Volt seconds)
NEGLIM - The negative integration limit (Volt seconds)

The compensator branch inductance was set to give a three-phase compensator rating corresponding to the C/F value of 1.13 as used in Chapters IV, V and VI of this thesis. For the 56MVA numerically modelled furnace, this demanded a compensator rating of 63.4MVA, with the compensator branch inductance, $L_{C\Delta}$, equal to 0.164 Henries.

The integration limits were set to approximate to those obtained from simple integration theory, such that for

$\alpha_1 \simeq 100^\circ$; POSLIM = NEGLIM = 174kV secs
$\alpha_2 \simeq 135^\circ$; POSLIM = NEGLIM = 253kV secs
$\alpha_3 \simeq 170^\circ$; POSLIM = NEGLIM = 294kV secs

7.4.5 Results from the Computer Model Compensator

(i) Compensator Currents

The calculation of conduction angles was first tested over only four cycles of input data to avoid the use of excessive computational effort. The values ICON and ICOFF set the step value 'N' at which the compensator is judged to be on and off respectively.

Figure 7.13(a) shows the three-phase compensator branch currents calculated for an integration limit of 200 units. This value initiates 'conduction' at a point corresponding to $\alpha \simeq 100^{\circ}$.
Also shown in Figure 7.13(a) is the compensator branch voltage waveform from ICON onwards.

Figure 7.13(b) shows how the delta-connected compensator branch currents combine on three-phase line currents, and compares them with the fixed arc furnace line currents.

The effect of varying the integration limit is shown in Figures 7.14 and 7.15, where conduction angles decrease for limits of 250 and 285 respectively. The compensator current peaks are always plotted to fill the scale available, and the scales show that current peaks decrease with decreasing conduction angle as expected.

(ii) Compensator Voltages

Study of the calculated compensator branch voltages presented in Figures 7.13(c), 7.14(a) and 7.15(a) shows that the characteristic form of voltage depression is apparently missing from the line voltage waveforms.

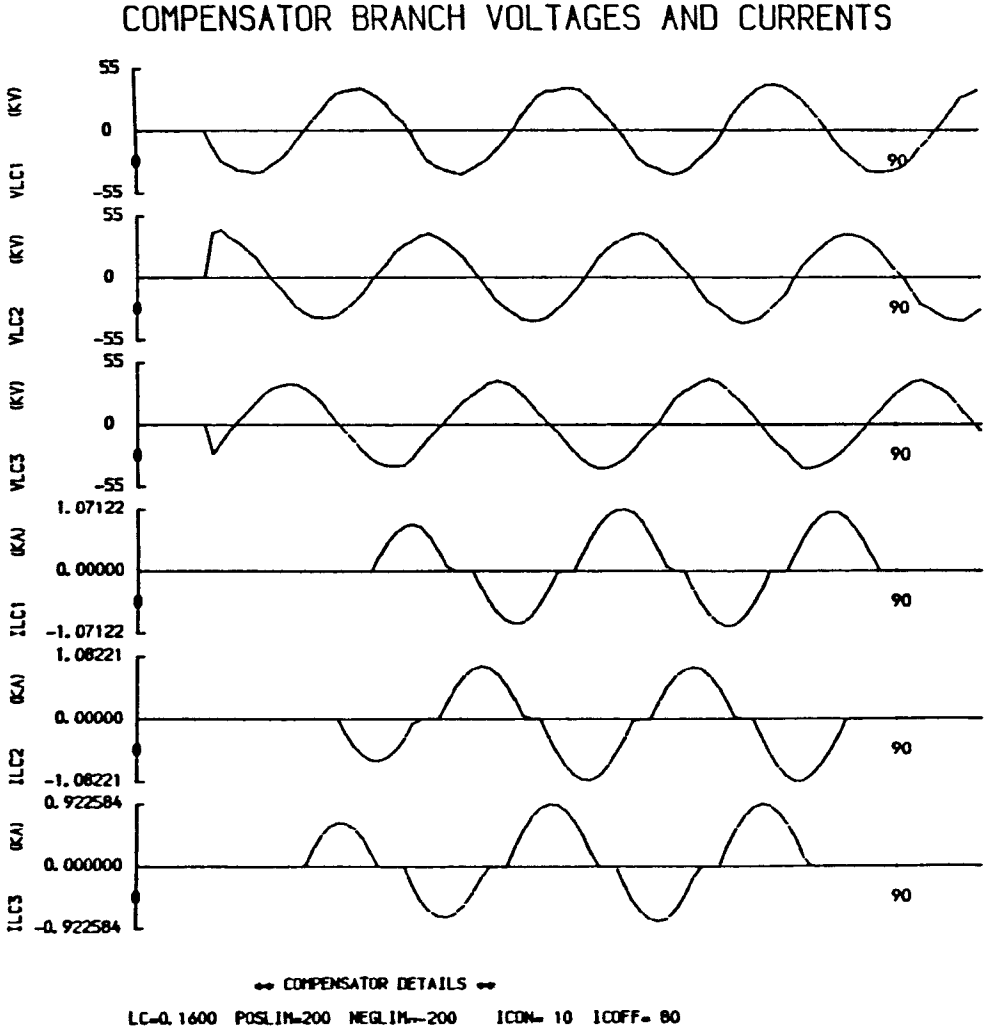


Fig. 7.13(a) : Computed 6-pulse TCR branch voltages and currents with LIMIT = 200

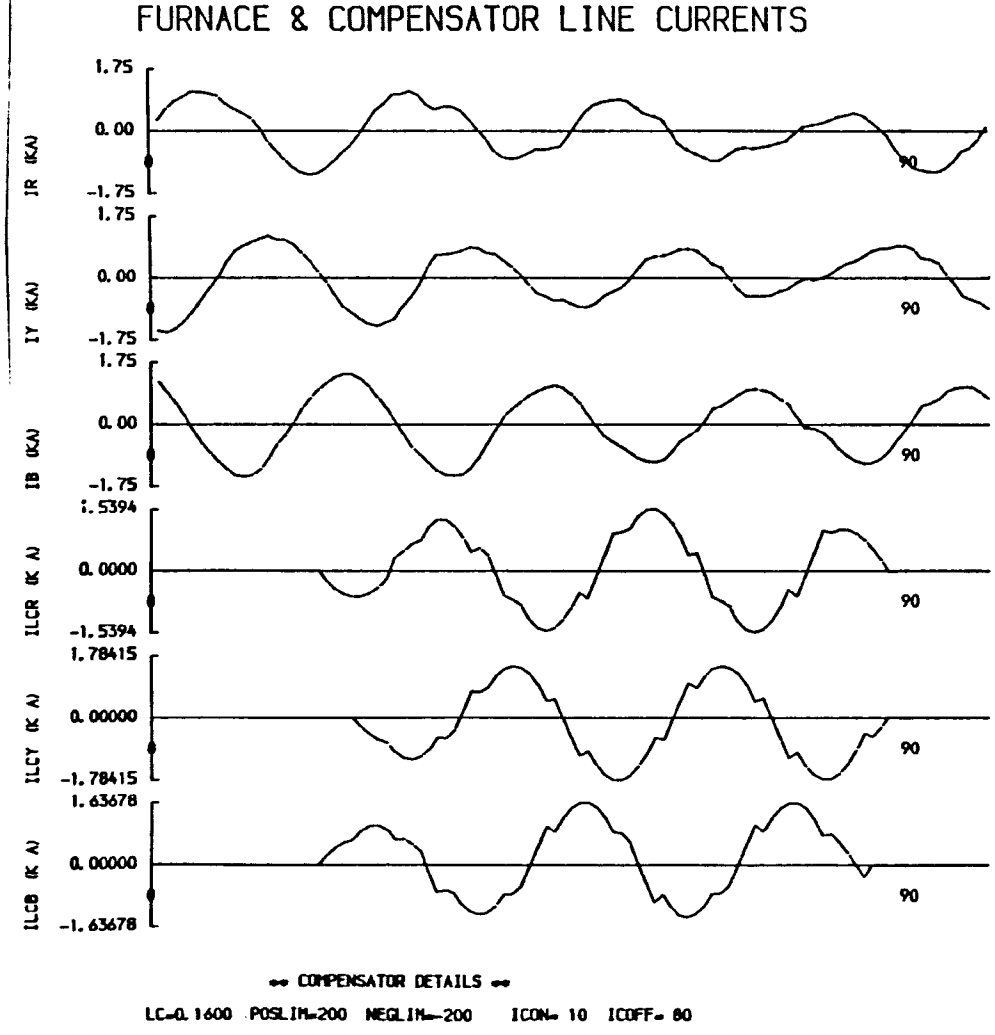


Fig. 7.13(b) : Computed line currents for arc furnace and TCR with LIMIT = 200

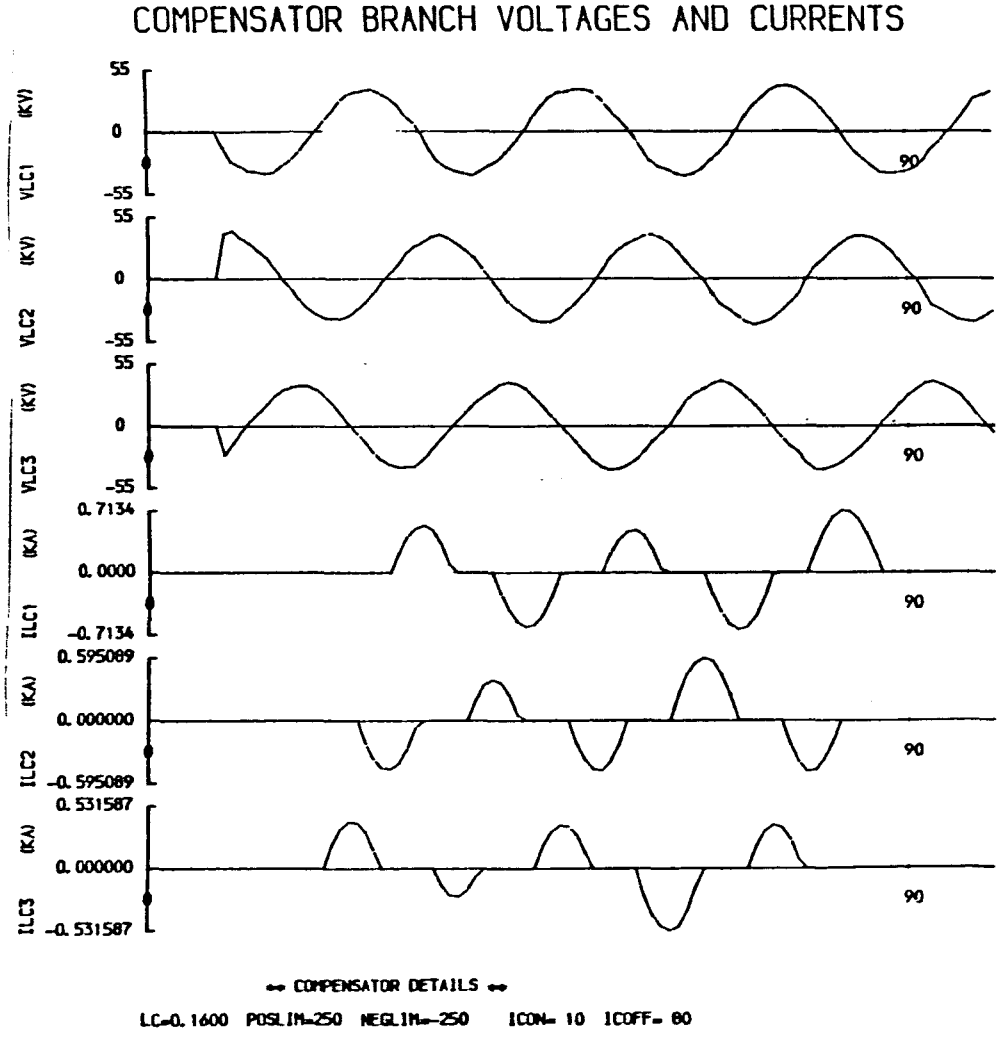


Fig. 7.14(a) : Computed 6-pulse TCR branch voltages and currents with LIMIT = 250

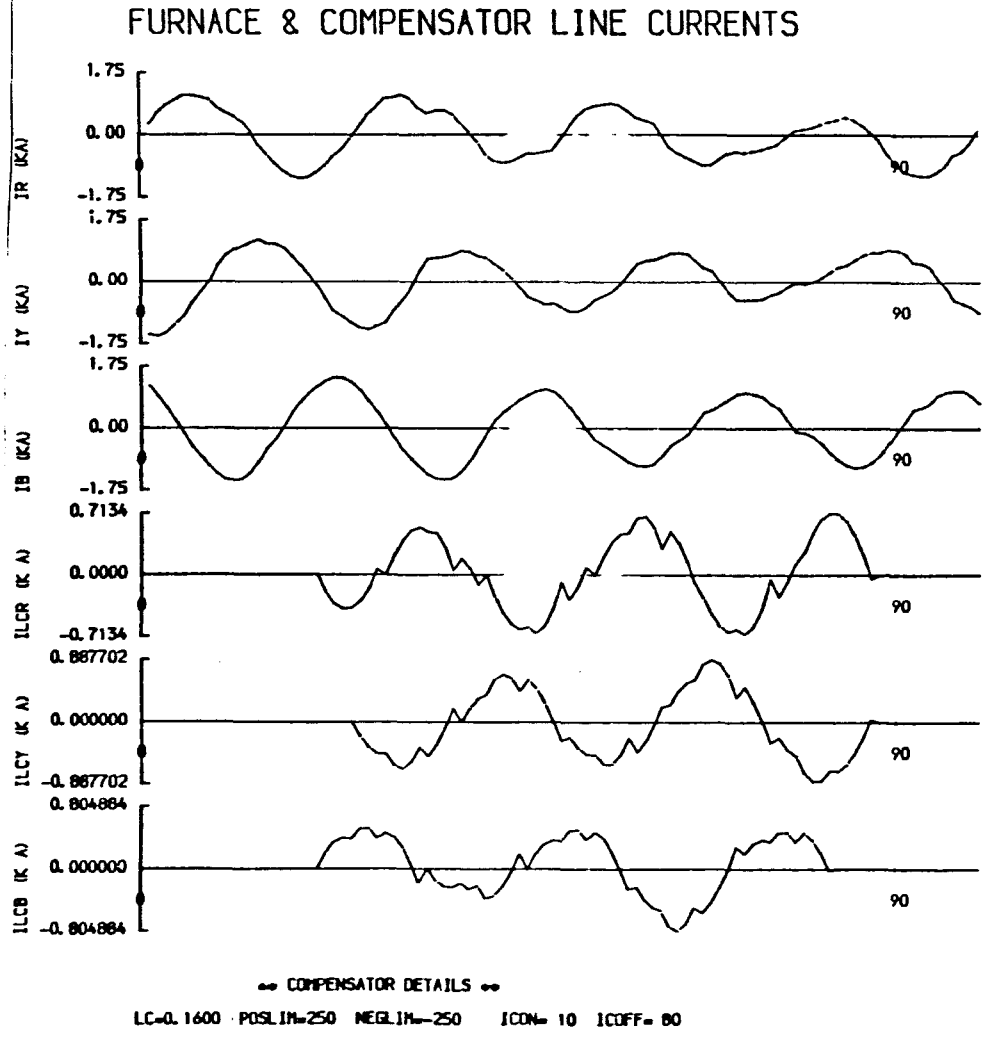


Fig. 7.14(b) : Computed line currents for arc furnace and TCR with LIMIT = 250

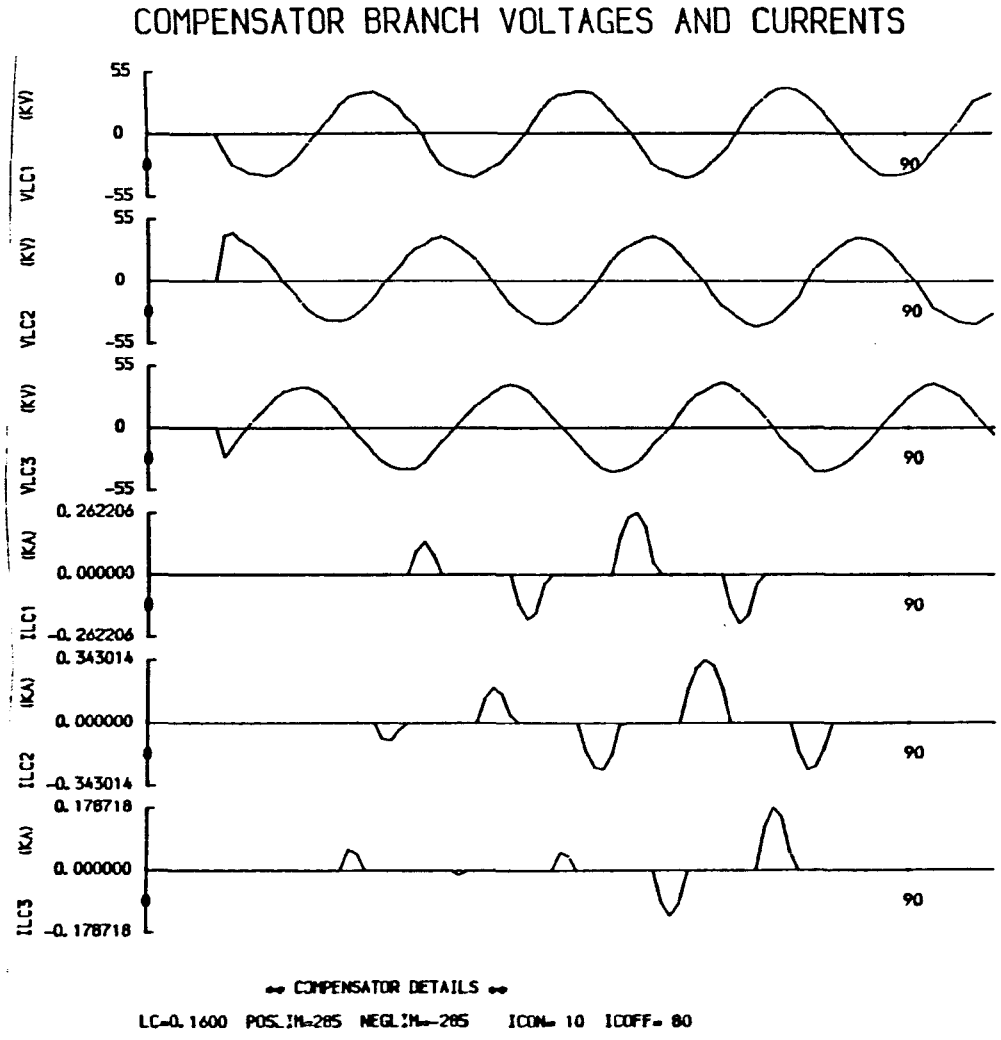


Fig. 7.15(a) : Computed 6-pulse TCR branch voltages and currents with LIMIT = 285

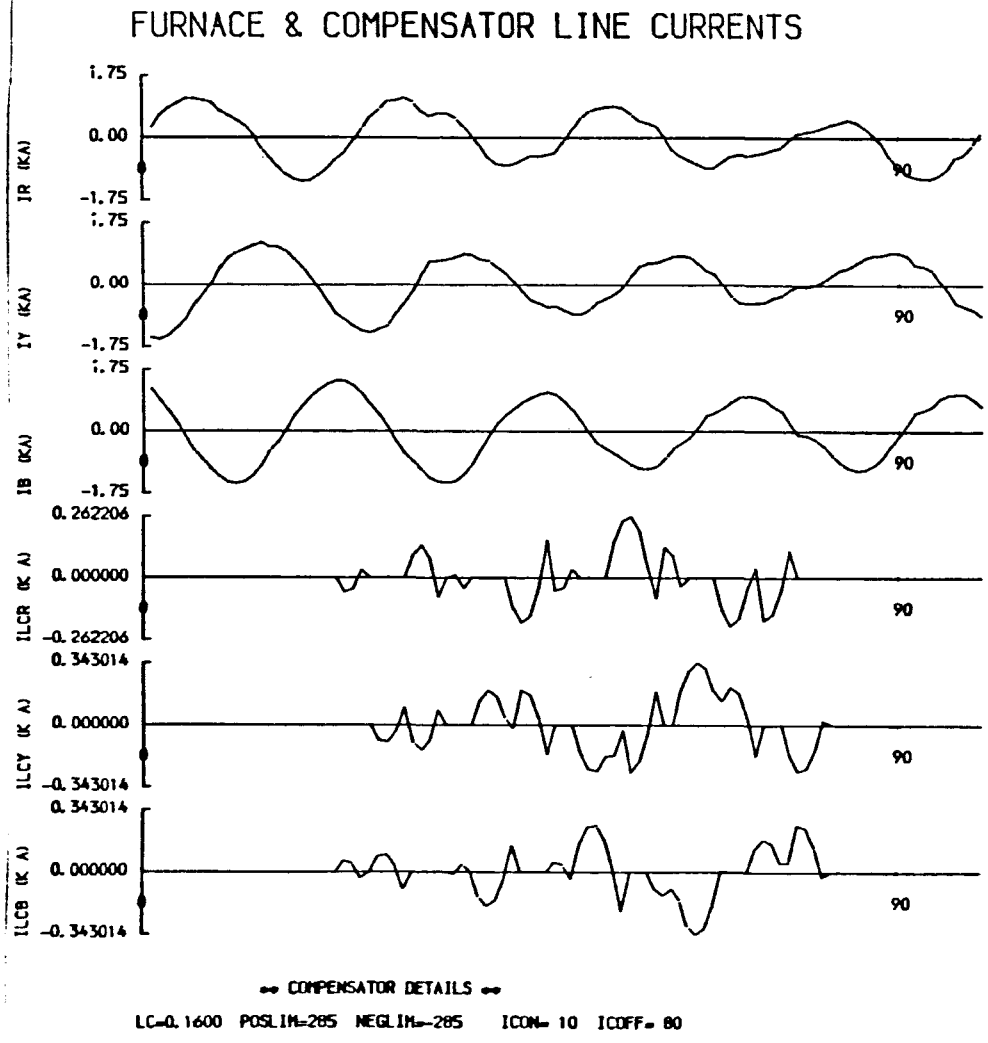


Fig. 7.15(b) : Computed line currents for arc furnace and TCR with LIMIT = 285

Since this is the means by which the compensator would achieve voltage flicker reduction, further investigation was carried out into the effect of the compensator's calculated 'shunt compensation'.

Figure 7.16(a) gives the first 4 cycles of three-phase line voltages calculated by the 'uncompensated' computational arc furnace model together with the 'demodulated' flicker voltage. Figure 7.16(b) then shows, for comparison, the equivalent three-phase line voltages calculated for the 'compensated' computational arc furnace model.

The demodulated 'compensated' line voltage waveforms show a greater 50Hz component than the corresponding 'uncompensated' waveform, and this is due to the slight voltage depression due to compensator branch conduction.

The two demodulated three-phase waveforms are compared on a larger scale in Figure 7.17 where the 50Hz component is more visible.

The power spectrum of the compensated line voltage time series data was obtained for comparison with the uncompensated form, but the results were disappointing and showed hardly any improvement in the 0-100Hz frequency band.

Possible reasoning for this is given in the discussion in Section 8.1.4, and further work is suggested in Part 8.3.

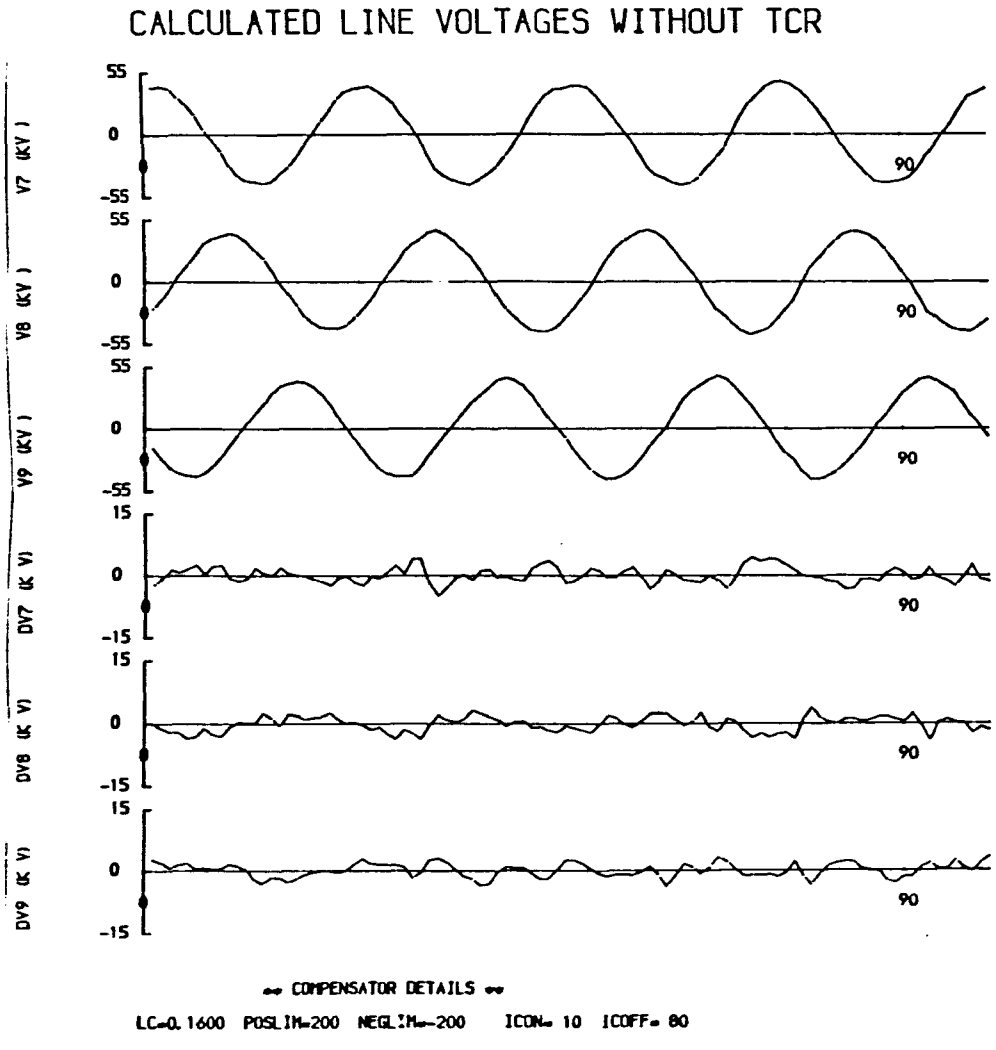


Fig. 7.16(a) : Computed uncompensated arc furnace line voltages

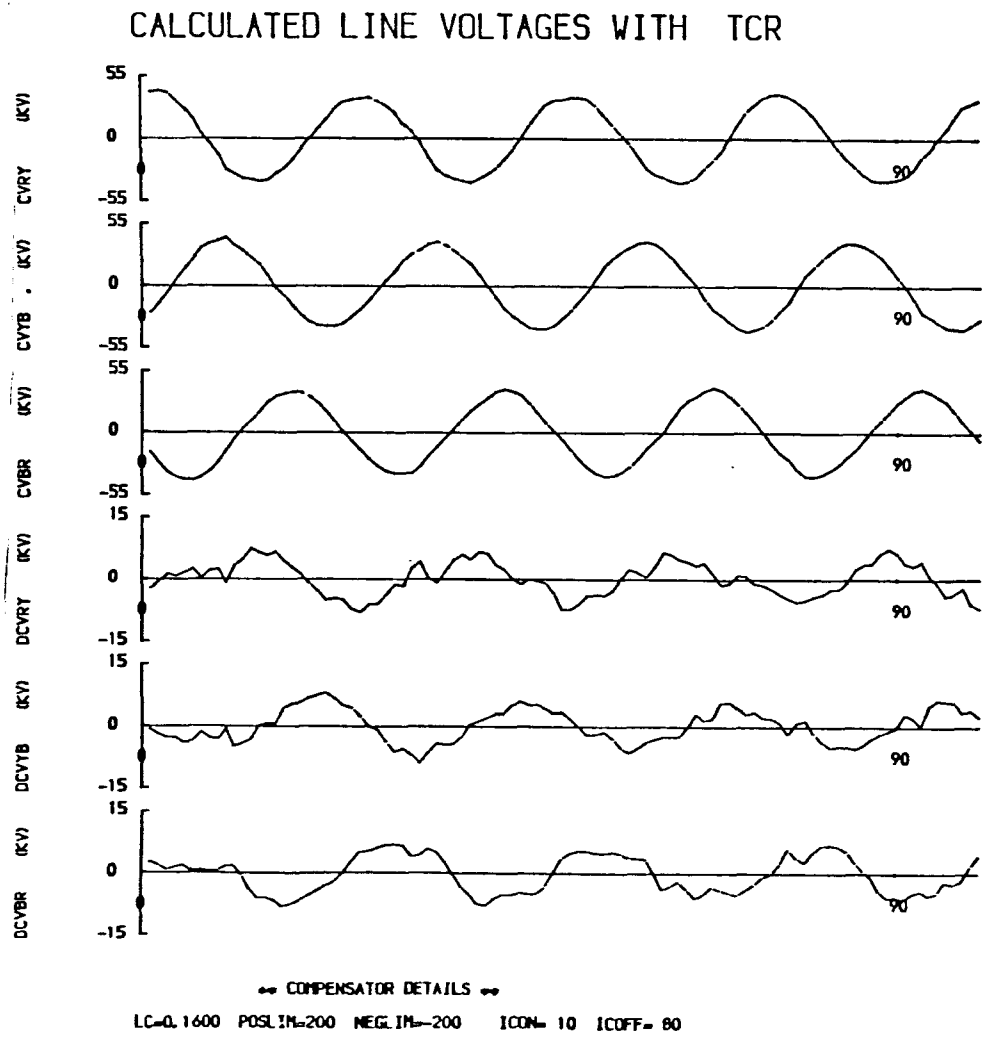


Fig. 7.16(b) : Computed compensated arc furnace line voltages

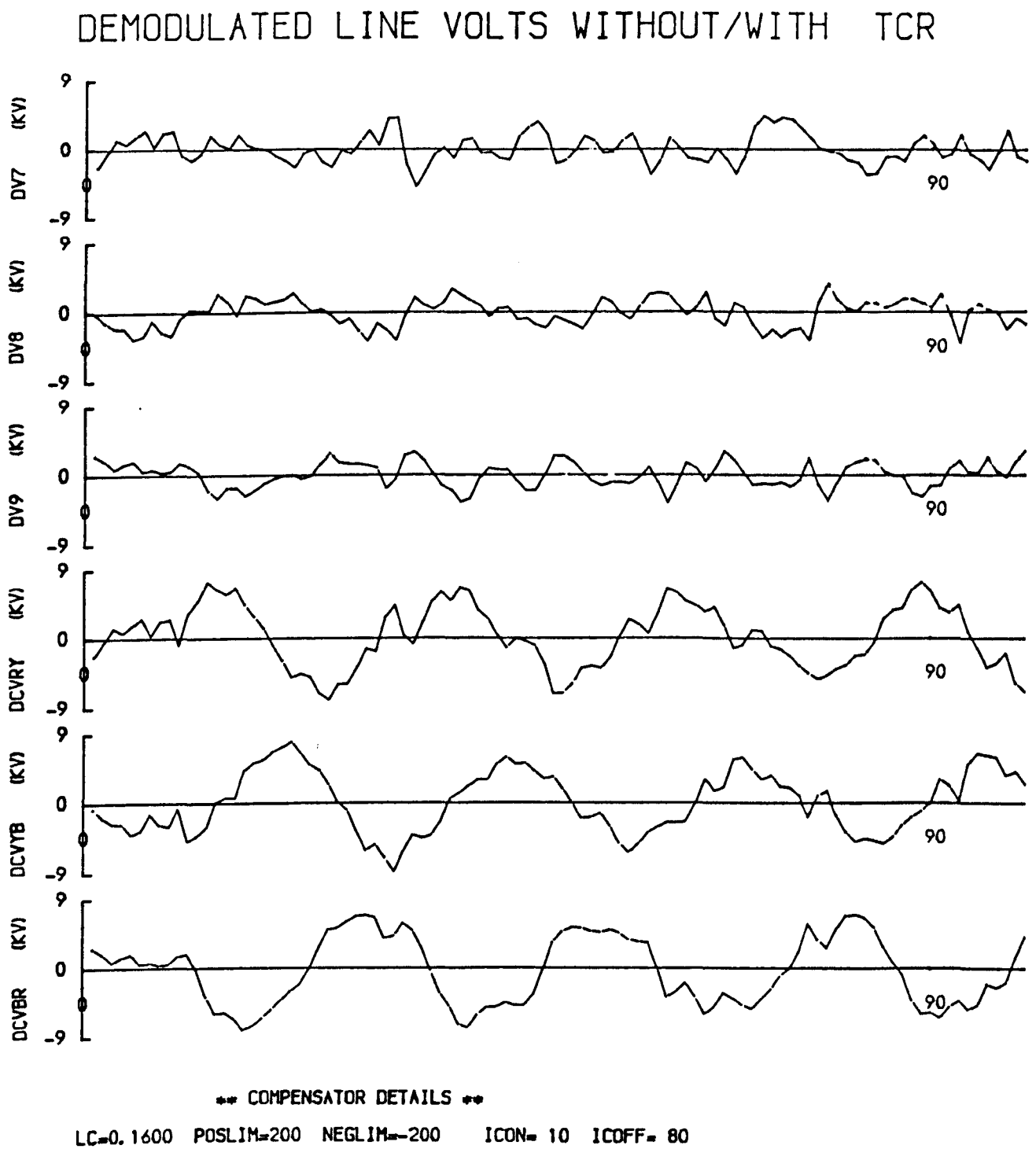


Fig. 7.17 : Computed compensated and uncompensated demodulated arc furnace line voltages

CHAPTER EIGHT

DISCUSSION, CONCLUSIONS AND FURTHER WORK

8.1 DISCUSSION

8.1.1 The Laboratory Arc Furnace Model

(i) Current Waveform Reproduction
(ii) Voltage Waveform Reproduction

8.1.2 The Laboratory TCR Compensator Models

(i) The Six-Pulse TCR Compensator
(ii) The Twelve-Pulse TCR Compensator

8.1.3 Data Analysis

8.1.4 Mathematical Modelling

8.2 CONCLUSIONS

8.3 FURTHER WORK

8.1 DISCUSSION

The summary of this thesis describes briefly the areas of work covered, and it is felt that the work was successful in the following areas:

(a) The establishment of laboratory and numerical models of an arc furnace and supply system that gave repeatable results for use with different compensation studies.

(b) The presentation of a detailed description and results from the use of a six-pulse TCR compensator. Its success was demonstrated with a very simple but fast control method.

This discussion will now present aspects of the research work that have not been covered in the preceding chapters, and will attempt to assess the suitability of techniques used in the work to obtain the results.

8.1.1 The Laboratory Arc Furnace Model

(i) Current Waveform Reproduction

Using the AIM-65 microcomputer system imposed a number of restrictions upon small-signal current waveforms generated to drive the power amplifiers. It was apparent at an early stage that the storage capacity of a machine with only 28 kbytes of available addressable RAM would restrict the cycling period of the data to be output in its analogue form. The dynamic expansion RAM was continually refreshed, and would not operate reliably at the higher clock rate of 6MHz used instead of the 4MHz standard.

Data transfer to the model from the mainframe computer was laborious, using punch tape output from old equipment. Errors in reading to the AIM-65 microcomputer were frequent, and early plans to have a selection of data spans available for reproduction were dropped in favour of one set span stored in EPROM.

The data output frequency of 5kHz was more than sufficient for a study of flicker voltages, but the 8-bit resolution could not make full use of the accuracy of the 15-bit recording equipment used by the CEGB. The data cycling period of eighty-nine 50Hz cycles allowed only a reproduction of frequency components above 1.8Hz. Frequencies below this value have a low weighting on the flicker sensitivity curve, but ideally should they not be neglected.

The Y-connected commercial power amplifiers driven by the small analogue signals were a success. The voltage feedback method of driving their inputs gave reliable fine control, and established a useful technique for current reproduction at frequencies other than 50Hz.

After the arc furnace model had been constructed, it was clear that the power amplifiers were only being used at less than one third of their full current rating. This was because of the original safety margin used in deciding the base operating levels of the model. The real operating current levels were then less than the base level and the safety margin excessive. Increasing the gain of the control feedback loop caused the model to draw currents of identical form, and greater than twice the normal magnitude, without ill-effect. The base values for the model were by then fixed by the modelling impedances; the compensator ratings were established, and increasing the VA rating of the model would have lost much time.

Establishment of the current waveform reproduction data in EPROM and the provision of separate AC supplies for laboratory technical equipment meant that the arc furnace model became reliable and simple to use.

(ii) Voltage Waveform Reproduction

The early stages of the physical model design worked towards a small scale reproduction of the Templeborough system as a whole. Only at a later stage was it decided that the very small voltage fluctuations occurring on the 'system' side of the Y-Δ transformer would not be included as part of a reactive compensation study. With the bulk of the model supply impedance appearing in the 'line inductances', it is now apparent that the Y-Δ transformer could be removed from the model. Such a step, however, would detract from the generality of the system modelling approach and would preclude any measurement of primary parameter at a later date.

The X/R value obtained in the model was approximately 11, compared with 40 for the real system. This disparity could have been reduced by using physically larger components, but for a laboratory model it was felt that 91p.c. reactance compared reasonably with the 98p.c. reactance of the real system. Resistive losses or dampening effects did not give difficulties in any part of the arc furnace modelling.

It was noticeable that the distorted line voltages in the time domain did not show the same sudden instantaneous departures from the sinusoidal as those recorded at 33kV. This lack of agreement was at first disappointing, but subsequent comparison of power spectra in the relevant frequency bands showed that the power frequency distribution was very similar. This firstly showed that sudden voltage changes do not contribute significantly to low frequency power, and secondly suggested that the sudden voltage changes may not have been attributable to the measured arc furnace load but rather to loads elsewhere on the supply system.

The flicker level at the point of application of shunt reactive compensation was considerably higher than that defined as 'just perceptible' by the UIE. This was judged to be useful for comparative studies of compensator performance. Varying the feedback gain to the power amplifier inputs could greatly change the percentage voltage distortion obtained, and it would be simple to undertake an investigation of compensator performance for very different flicker levels.

8.1.2 The Laboratory TCR Model

(i) The Six-Pulse TCR Compensator

The rating of the first laboratory TCR compensator was intended to give effective compensation of the flicker voltages found in the normal operating range of the arc furnace model. The results obtained with this compensator were disappointing, and the rating was duly increased to allow for the full change in demand between furnace open- and short-circuit.

Some thought must be given to why the design calculations for the original TCR compensator had to be modified. The answer may lie in the method used for control of thyristor firing angles: The efficacy of the control method will depend on the level of success in each of the following:

(a) Sensitivity
(b) Accuracy
(c) Speed of response

The sensitivity of the system was determined by adjustment of the magnitude of the 'reference' sinusoid used in all half-cycle integrations. This was carefully set to be as close as possible to the sampled distorted sinewave, whilst being less than the sampled values at all times. If the reference

sinusoid is made too large in an attempt to gain greater sensitivity, then it can be shown that the control algorithm begins to give an effect opposite to that desired and the sensitivity is duly impaired. Attempts for maximum sensitivity may have brought the sampled values of the depressed line voltage waveform below those values stored as the reference sinusoid, although calculations show that this condition should not occur.

The accuracy of the equipment is determined by a number of elements of the system, both in hardware and software. Most important is the accuracy to which the line voltage is sampled, and this is a function of both the ADC bit number and the sampling rate. The sampling rate was software-timed, and therefore subject to 'float' due to device temperature effects. The decision to use 8-bit ADCs was based on a brief study of noise levels together with the limited availability of suitable 10- and 12-bit devices. The 8-bit device was shown to give reasonable results on the model arc furnace supply system with relatively high flicker levels. Nevertheless, it must be noted that the resolution of an 8-bit sampling system is 0.4 percent of full scale, which is greater than the 'just perceptible' limit of 0.2 percent peak-to-peak that is widely recognised. This compensator system was thus applied, with limited accuracy, to a supply system with flicker levels high enough to be detected and compensated. The lower levels of voltage fluctuation, still sufficient to cause annoyance, could not be detected by an 8-bit sampling system and therefore remained uncompensated.

The speed of response of the system may be estimated by considering the times between start of sampling and subsequent initiation of the thyristor firing pulse. This time will always be within one half-cycle, and it may be after one quarter-cycle. This suggests a speed of response between 5 and 10 milliseconds. No studies were conducted to attempt to measure the speed of response of the control system used, although such an investigation would have been relatively easily conducted with the equipment available.

An advantage of the laboratory system used was that the same compensator control system could be applied to a TCR compensator with different rating, with only minimal changes to the system software. A second six-pulse TCR compensator, of higher rating than the first, was successfully used for the same equipments, and proved considerably more successful. The flicker improvement factor of 0.4 and the cross-over frequency of 25Hz compare very favourably with the published results of work elsewhere.

It is accepted, however, that this model shunt reactive compensator is not a full model of any particular system in service, or likely to be in service, on a full scale supply system. No attempt was made to filter harmonic frequencies, and the flicker levels compensated were of a high level. It is hoped that the work on the six-pulse TCR compensator scheme will encourage the presentation of comparable results from work elsewhere, in order to promote the objective assessment of this subject in greater depth.

(ii) The Twelve-Pulse TCR Compensator

The twelve-pulse TCR compensator scheme was developed in order to obtain a compensator with a faster speed of response for given rating, sensitivity and accuracy. The system functioned adequately, but failed to achieve results to improve on the six-pulse scheme.

The control algorithm used was a simple extension of that used successfully for the six-pulse compensator, and it is possible that a superior scheme could have been developed, given more time. A particular improvement may have been to increase the rating of the 'first stage' TCR unit to give fast, coarse control of voltage, to be followed by the conduction of a smaller rating 'second stage' for finer control.

Higher pulse numbers could be accommodated by the control scheme if necessary, and this is an obvious development of this aspect of the work. An eighteen-pulse TCR compensator design could give even earlier 'coarse' control, with finer control spaced over two following stages per half-cycle.

Such control schemes, of greater complexity, may benefit from the type of 'supervisory' control suggested in Chapter IV of this thesis. The response of the individual phase TCR controllers could be tuned by a master controller acting from a longer response time constant or from prior information on the furnace melt cycle.

Such a scheme could be applied to this laboratory model by enabling a 'master controller' to select the control variables to be used by each of the three-phase controllers. In this way the phase controllers would be dedicated to a fast response, whilst the master controller calculated the necessary values of reference sinusoid, sampling time and LIMIT.

8.1.3 Data Analysis

The bulk storage of the recorded Templeborough arc furnace voltages and currents on a mainframe computer gave fast and simple access, and enabled many different studies of sections of data to be made using modern graphical output programs.

Logging of results from the laboratory models, and subsequent transfer of this data to the mainframe computer, provided a very large storage facility for blocks of data obtained from different experimental conditions.

It must be noted that the work towards providing such data transfer facilities was, although apparently straightforward, very time consuming; transfer of data from one format through three other formats was not unusual. The ability to transfer experimental results from the laboratory to mainframe computer files was not achieved until the very final stage of the research project, and in fact little use was made of this facility.

The bulk of the laboratory modelling results were then obtained from benchtop equipment such as the spectrum analyser, two-channel storage oscilloscope and flat bed plotter. Careful measurement techniques allowed these to be used to good effect, and they saved many hours of programming effort which would have been required to obtain the same results via the mainframe computer.

Where the modelling was itself carried out on the computer, standard spectral analysis and graphical output routines were written and tailored to suit exactly the needs and interests of this research project.

One analysis method which was not achieved, even though the facilities were available, was the mainframe computer modelling of the UIE digital flickermeter. Applying such a facility to the results from arc furnace and TCR compensator models would have completed the link between simple observation and comparison of power spectra on the one hand, and the knowledge of a 'flicker severity factor' on the other.

8.1.4 Mathematical Modelling

It was an early aim of the research project to develop a numerical model of the arc furnace installation, in parallel with modelling work undertaken in the laboratory. This would have allowed investigative work to be done computationally in advance of capital expenditure on different arrangements of equipment.

The computational arc furnace model has been shown to successfully reproduce the flicker frequency disturbances found in the real system, although there is still some disparity between the observed time domain line voltages produced. Sudden severe voltage fluctuations are absent from the modelled line voltage, and it was suggested that such fluctuations may not be an effect of the arc furnace load currents measured by the CEGB, but rather are caused by other loads on the 275kV system.

This explanation rapidly solves the problem, but the disturbance levels observed would then indicate that the 275kV 'Sheffield ring' supply had large transient voltage changes regularly impressed upon it for the duration of the measurement period.

The numerical model was eventually developed at a stage after results had been obtained from the laboratory model, and there was in fact little parallel development carried out. The two areas of study progressed separately, and far more work is still required on the mathematical modelling of the TCR compensator. The program listings show that considerably more computational effort was involved for the compensator modelling than was required for the arc furnace model, and the control algorithm used was not subjected to sufficient investigation once the TCR compensator equations were established. The control algorithm described in Chapter VII was even simpler than that used in the laboratory, and it is possible that further development to integral of voltage difference or 'voltage difference squared' may yet produce results to assist in the understanding of TCR compensator control schemes.

8.2 CONCLUSIONS

The work carried out shows that recordings of arc furnace current waveforms may be used to reproduce successfully the voltage fluctuations appearing on the real supply system. The numerical model allows this to be undertaken in an environment where supply system parameters may be rapidly changed to suit different investigative approaches.

The laboratory model provided a facility for obtaining voltage fluctuations with frequency components accurately representing those found on the real arc furnace supply network, and the magnitude of these fluctuations relative to the 50Hz 'carrier' amplitude was easily changed.

The disturbances produced by the models formed an excellent reference for studies aiming for their reduction by shunt compensation techniques, and the reproduction of low frequency disturbances in particular allowed shunt compensation for voltage flicker reduction to be carried out in the laboratory.

The compensation studies employed a thyristor controlled reactor configuration commonly used in the industry, and it was shown how a simple, low-cost microcomputer system could be used to achieve effective reduction in the frequency components of the voltage fluctuations that cause tungsten filament lamp voltage flicker.

8.3 FURTHER WORK

The models now established form an excellent facility for the research and testing of other types of TCR compensator control algorithm. A common assessment method, and presentation of the results obtained from each scheme, would contribute much to the industry's understanding of the benefits of different TCR control strategies.

The twelve-pulse TCR compensator design requires further development of its control algorithm to achieve results comparable with those already presented for the six-pulse scheme, and it is possible that the computer modelling methods described may be extended towards the study of a twelve-pulse scheme. The two stage conduction patterns of the twelve-pulse arrangement allow a wide range of control strategies to be investigated, which will be new to the field of research in this subject.

Improvement of the laboratory model may be obtained by increasing its VA rating to allow greater levels of current to be drawn by the thyristor controlled reactances.

The presentation of the results of TCR compensator schemes would be considerably strengthened by the application of an internationally recognised digital flickermeter, such as that now recommended by the UIE.

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APPENDIX A

SHORT CIRCUIT POWER OF A 56MVA ARC FURNACE AT TEMPLEBOROUGH

The arc furnace installation is supplied from the 275kV busbar as shown in Figure 2.2.

Define X_s', X_b' and X_a' as:

X_s' = Source Reactance - between PCC and infinite busbar

X_b' = Any reactance between furnace transformer and PCC

X_a' = Reactance of furnace transformer, supplementary reactors and arc furnaces

as illustrated in Figure 3.7.

X_a' is often unknown, and typical values based on furnace nameplate rating can be consulted[6].

Thus X_a = 50p.c. on 56MVA base for a 56MVA furnace

and $X_a' = 50\text{p.c.} \times \frac{100}{56}$ on 100MVA base

$= 89.3\text{p.c.}$ on 100MVA base

For this network (see Figure 2.2):

$X_s' = 1.18\text{p.c.}$ on 100MVA base

and $X_b' = 23.933\text{p.c.}$ on 100MVA base

Then:

$$S_t = \frac{100}{X_a' + X_b' + X_s'} \text{ MVA}$$

$$\underline{S_t = 87.46 \text{ MVA}}$$

SGT4 incorporates an on-load tap changer with taps between +10p.c. and -20p.c. in 18 steps. For a constant primary voltage of 275kV, the SGT4 secondary voltage may vary between $29.7kV \leqslant V_2 \leqslant 39.6kV$. The percentage impedance, X_{33}, given for those components at 33kV will then vary with the true voltage V_2 as: $X = X_{33} \times \frac{33^2}{V_2^2}$. Thus X_a' may vary from the nominal value of 0.893 per unit between 0.62 per unit and 1.102 per unit. These impedance values then show how S_t may vary from the nominal value given above, depending on SGT4 tap position:

$$S_{tMAX} = 114.8MVA$$
$$S_{tMIN} = 73.9MVA$$

The CEGB measurements were made at point B, between the impedances X_b' and X_a', therefore the measured short circuit MVA will be proportionally less than the theoretical value from the infinite busbar by the factor

$$\frac{X_a'}{X_a' + X_b' + X_s'}$$

Then:

$$S_{tMAX} = 81.71MVA$$
$$S_t = 68.21MVA \text{ Nominal}$$
$$S_{tMIN} = 61.19MVA$$

APPENDIX B

RECOVERY OF DATA FROM CEGB MAGNETIC TAPE STORAGE

Recordings were made over a period of 3 days at the Templeborough 275kV/33kV substation. Six arc furnaces were supplied from this substation, with a collective nameplate rating of 360MVA.

Up to 8 channels of data could be sampled using the DREAM recording equipment[81,82]. Studies of oscillograms for the bulk of the recorded data revealed trends in the recordings which would not be so apparent for a cycle by cycle analysis. On the basis of these visual studies two different sections of data were selected for further use at Liverpool University. Blocks of selected data were transferred to magnetic tape number LSN201, to be held in the Liverpool University Computer Centre tape library.

Each block or record of data contains 2048 bytes of information:

8 bytes - block number and time GMT at start of block

2032 bytes - data. 2 bytes x 8 channels x 127 lines

8 bytes - spare at end of each block

Each line of 8 channels is time-spaced from the next line by 800microseconds. Thus each block contains approximately 5 cycles of data.

Each 2-byte channel gives a 16-bit signed integer value in the range -32767 to +32767 which needs to have a small offset removed before a scale factor is applied to give values of kV or kA.

Recording details and comments on the data content are now given:

(i) First 600 Blocks on LSN201

From RF07, tape No 3, blocks 60 to 660 inclusive.
16.11.00 hours to 16.21.30 hours 28/6/1977

Furnace No 2 operating in isolation. (Furnace No 1 off and bus section switch open - see Figure 2.1.)

Start-up of Furnace No 2 occurs in block 60.

This 'start-up' data is the same as that used by CEGB STB for various studies(REFS).

See table B1 for scaling and offset values.

(ii) Blocks 600 to 1500 on LSN201

From RF18, tape No 2, blocks 2600 to 3500 inclusive.

Furnace No 5 and Furnace No 6 on. Severe low frequency oscillations in furnace No 6 line current peaks. Furnace No 6 becomes almost open circuit for several seconds before returning to full power during melt-down.

See table B2 for scaling and offsets.

CHANNEL	1	2	3	4	5	6	7	8
ADD TO INTEGER VALUE	-2	-5	-1	+71	+80	-109	+32	-12
MULTIPLY BY	3.404	3.393	3.411	0.3364	0.3360	0.3452	0.3374	0.3382
QUANTITY (UNITS)	VR1 kV	VY1 kV	VB1 kV	IR1 kA	IY1 kA	IB2 kA	IR2 kA	IY2 kA

Table B1 Scaling and Offsets for RF07

CHANNEL	1	2	3	4	5	6	7	8
ADD TO INTEGER VALUE	-145	-128	-150	-111	-72	-72	-49	-
MULTIPLY BY	3.390	3.394	3.387	0.3836	0.3748	0.3787	0.3790	-
QUANTITY (UNITS)	VR6 kV	VY6 kV	VB6 kV	IR5 kA	IB5 kA	IR6 kA	IB6 kA	-

Table B2 Scaling and Offsets for RF18

APPENDIX C

CUBIC SPLINE CURVE FITTING AND ITS APPLICATION

C.I Introduction

The time series data obtained from the CEGB (see Appendix B) gave only the measured instantaneous three-phase voltages and currents with a sampling interval of 800 microseconds.

The modelling work undertaken in this Thesis used the measured three-phase currents as the 'driving signal' in physical and mathematical models to reproduce voltage distortion.

In each model, some additional information was required from this data, namely:

(i) In the physical model (Chapter 2), interpolation between points was used to increase the number of points output in each cycle to give smoother waveforms.

(ii) In the mathematical model (Chapter 8), the value of di/dt was required for each value of measured current, i.

All large-scale data handling was performed on a mainframe computer, and numerial techniques were used to obtain the data required by (i) and (ii) above. The Numerical Algorithms Group (NAG) Library[122,123] subroutine E02BAF was used to compute a weighted least-squares approximation to the original data by a cubic spline. The same subroutine was then used for interpolation to satisfy (i) above. NAG subroutine E02BCF was then used to evaluate derivitives from the B-spline to satisfy (ii) above.

C.II Applications Programs

Cox[124,125] describes how the set of N data points (x_r, y_r) may be used to calculate a cubic spline approximation

$$S(x) = \sum_{i=1}^{N+3} C_i N_i(x)$$

where the coefficients are c_i, and the normalised B-spline is $N_i(x)$. The B-spline $N_i(x)$ is defined upon 'knots' K_{i-4}, K_{i-3}, K_{i-2}, K_{i-1} and K_i.

Once $N_i(x)$ has been calculated from y(x), the B-spline parameters can then be passed to NAG subroutine E02BCF, which may be used to evaluate S(x) or its derivatives at any value of x. At those values of X where the input parameters y(x) is known, then

$$E(x) = S(x) - y(x)$$

may be calculated to show the error magnitudes due to use of the B-spline rather than use of original data at this point.

This procedure was followed for each of the four channels i_R, i_Y i_B, v_R (see Section 2.3.2) in sequence. Each channel consisted of 2250 time-series data points, corresponding to ninety 50Hz cycles. Attempting B-spline evaluation for 2250 points involved large computational effort, and program failures were frequent. The process was therefore restricted to data blocks of 780 points - representing one-third of the total span, plus 15 points at each end of the block.

The FORTRAN program to perform the interpolation process for the analogue model is shown in C.III and comment statements within the program explain the program flow.

The FORTRAN program to obtain values of di/dt for all values of 'i' is shown in C.IV.

C.III SPLI3OM FORTRAN Program Listing

FILE: SPLI30M FORTRAN A1 (EE68)

```
C                                                                       SPL00010
      DOUBLE PRECISION FIRST(1),LAST(1),SECOND(1),THIRD(1),FOURTH(1),   SPL00020
     +WORK1(800),WORK2(4,800),C(800),K(800),W(800),SS,                  SPL00030
     +VR(800),VY(800),VB(800),IP(800),IQ(800),                          SPL00040
     +IR(800),IY(800),IB(800),X(800),Y(800),                            SPL00050
     +OUT1(4000),OUT2(4000),OUT3(4000),OUT4(4000),                      SPL00060
     +T(4000),TIME(4000),T1(4000,8),TIME1(4000),                        SPL00070
     +XTOT,XSTART,XFIN,XVAR,XARG,RES,FIT(4)                             SPL00080
      INTEGER I,NCAP,NCAP7,J,IFAIL,J2,M,L,N,R,M1,M2,M3,LEFT,            SPL00090
     +KOUNT,RESULT,ITIME,Z,ENDNOT                                       SPL00100
      LOGICAL AMIDPT                                                    SPL00110
      DATA  FIRST/8H   FIRST/                                           SPL00120
      DATA   LAST/8H    LAST/                                           SPL00130
C     DATA SECOND/8H  SECOND/                                           SPL00140
C     DATA  THIRD/8H   THIRD/                                           SPL00150
C     DATA FOURTH/8H  FOURTH/                                           SPL00160
C                                                                       SPL00170
C.....SPLINE30M....SAME AS SPLINE10M BUT FOR 30 CYCLES OF DATA          SPL00180
C          INSTEAD OF 10 CYCLES.                                        SPL00190
C          (ONLY GIVES IR,IY,IB,VR FOR THE ANALOGUE MODEL)              SPL00200
C                                                                       SPL00210
C          THE PROGRAM WILL INTERPOLATE 'EXTRA'  EXTRA POINTS           SPL00220
C          BETWEEN DATA POINTS.                                         SPL00230
C                                                                       SPL00240
C          SINCE OUTPUT OF A DETAILED RESULTS LIST FOLLOWED BY A        SPL00250
C          CONTINUOUS LISTING FOR USE AS INPUT DATA IS OFTEN EXESSIVE,  SPL00260
C          'RESULTS' SHOULD BE SET AT :                                 SPL00270
C                    1 -FOR BOTH LISTINGS                               SPL00280
C                    2 -FOR ONLY THE 'DETAILED'LISTING                  SPL00290
C                    3 -FOR ONLY THE 'CONTINUOUS' LISTING               SPL00300
C                                                                       SPL00310
C                                                                       SPL00320
C          TSTEP IS THE TIME STEP OF INPUT DATA .                       SPL00330
C                                                                       SPL00340
C                                                                       SPL00350
      M=780                                                             SPL00360
      NCAP=M-7                                                          SPL00370
      RESULT=1                                                          SPL00380
      TSTEP=0.0008                                                      SPL00390
      EXTRA=3.0                                                         SPL00400
      IXTRA=IFIX(EXTRA)+1                                               SPL00410
C                                                                       SPL00420
C                                                                       SPL00430
C          THE FOLLOWING LOOP READS ALL EIGHT CHANNELS OF DATA,         SPL00440
C          SPECIFIES  THE   DEPENDANT   VARIABLE  TO  BE  USED,         SPL00450
C          SETS ALL WEIGHTS TO 1.0  AND SPECIFIES KNOTS K(5) TO         SPL00460
C          K(NCAP+3)  TO  BE AT THE SAME ORDINATES  AS  X(5) TO         SPL00470
C          X(NCAP+3). THE  X-AXIS  IS SCALED SUCH THAT THERE IS         SPL00480
C          AN  INPUT  DATA VALUE AT EVERY FOURTH INTEGER POINT.         SPL00490
C                                                                       SPL00500
C                                                                       SPL00510
      T1(1,1)=0.0000                                                    SPL00520
      T1(1,2)=0.0000                                                    SPL00530
      T1(1,3)=0.0000                                                    SPL00540
      T1(1,4)=0.0000                                                    SPL00550
      T1(1,5)=0.0000                                                    SPL00560
      T1(1,6)=0.0000                                                    SPL00570
      T1(1,7)=0.0000                                                    SPL00580
      T1(1,8)=0.0000                                                    SPL00590
      READ(5,996)VR(1),VY(1),VB(1),IP(1),IQ(1),IB(1),IR(1),IY(1)        SPL00600
      W(1)=1.0                                                          SPL00610
      DO 10 R=2,M                                                       SPL00620
          READ(5,996)VR(R),VY(R),VB(R),IP(R),IQ(R),IB(R),IR(R),IY(R)    SPL00630
          IF(VR(R).EQ.0.0.AND.VY(R).EQ.0.0)GOTO 555                     SPL00640
          DO 9 ICHAN=1,8                                                SPL00650
              T1(R,ICHAN)=T1(R-1,ICHAN)+TSTEP                           SPL00660
    9         CONTINUE                                                  SPL00670
        W(R)=1.0                                                        SPL00680
   10 CONTINUE                                                          SPL00690
```

```
C                                                                       SPL00700
C          THE NEXT LOOP VARIES  'KOUNT' , SPECIFYING WHICH             SPL00710
C          CHANNEL THE SPLINE IS FITTED FOR.                            SPL00720
C                                                                       SPL00730
C          ORIGINALLY THESE  WERE   IB,IR,IY,VR,  BUT SINCE             SPL00740
C          IB IS DERIVED ON THE PHYSICAL MODEL THE SEQUENCE             SPL00750
C          HAS BEEN MODIFIED TO  IR,IY,VR.                              SPL00760
C          ( IB  CAN BE  OBTAINED  SIMPLY  BY  CHANGING THE             SPL00770
C            FOLLOWING  'DO'  LOOP TO 4 PASSES ....REMEMBER             SPL00780
C            THAT  OUTPUT  STATEMENTS MAY  REQUIRE CHANGING             SPL00790
C            TOGETHER WITH RELEVANT FORMAT STATEMENTS ).                SPL00800
C                                                                       SPL00810
      DO 1111 KOUNT=1,3,1                                               SPL00820
      IF(KOUNT.EQ.1)GOTO 12                                             SPL00830
      DO 11 R=1,M                                                       SPL00840
           K(R)=0.0                                                     SPL00850
           C(R)=0.0                                                     SPL00860
   11 CONTINUE                                                          SPL00870
      SS=0.0                                                            SPL00880
   12 CONTINUE                                                          SPL00890
      ENDNOT=M-4                                                        SPL00900
      DO 14 R=1,M,1                                                     SPL00910
          IF(KOUNT.NE.1)GOTO 124                                        SPL00920
          Y(R)=IR(R)                                                    SPL00930
          IF(R.GT.4.AND.R.LE.ENDNOT)K(R)=T1(R,7)                        SPL00940
          TIME1(R)=T1(R,7)                                              SPL00950
          GOTO 14                                                       SPL00960
  124     IF(KOUNT.NE.2)GOTO 125                                        SPL00970
          Y(R)=IY(R)                                                    SPL00980
          IF(R.GT.4.AND.R.LE.ENDNOT)K(R)=T1(R,8)                        SPL00990
          TIME1(R)=T1(R,8)                                              SPL01000
          GOTO 14                                                       SPL01010
  125     IF(KOUNT.NE.3)GOTO 126                                        SPL01020
          Y(R)=VR(R)                                                    SPL01030
          IF(R.GT.4.AND.R.LE.ENDNOT)K(R)=T1(R,1)                        SPL01040
          TIME1(R)=T1(R,1)                                              SPL01050
          GOTO 14                                                       SPL01060
  126     IF(KOUNT.NE.4)GOTO 13                                         SPL01070
          Y(R)=IB(R)                                                    SPL01080
          IF(R.GT.4.AND.R.LE.ENDNOT)K(R)=T1(R,6)                        SPL01090
          TIME1(R)=T1(R,6)                                              SPL01100
          GOTO 14                                                       SPL01110
   13     WRITE(6,979)KOUNT                                             SPL01120
          GOTO 888                                                      SPL01130
   14 CONTINUE                                                          SPL01140
C                                                                       SPL01150
C                                                                       SPL01160
C          AFTER  PRINTING  RESPECTIVE HEADINGS , THE FIRST TEN         SPL01170
C          CHOSEN  DATA  VALUES  ARE  WRITTEN ,  TOGETHER  WITH         SPL01180
C          VALUES OF R , X(R) AND  K(R).                                SPL01190
C                                                                       SPL01200
C                                                                       SPL01210
C     IF(KOUNT.EQ.1)YNUM=FIRST(1)                                       SPL01220
C     IF(KOUNT.EQ.2)YNUM=SECOND(1)                                      SPL01230
C     IF(KOUNT.EQ.3)YNUM=THIRD                                          SPL01240
C     IF(KOUNT.EQ.4)YNUM=FOURTH                                         SPL01250
      IF(RESULT.GT.2)GOTO 30                                            SPL01260
      WRITE(6,997)M,NCAP                                                SPL01270
      WRITE(6,995)FIRST                                                 SPL01280
      DO 20 R=1,20,1                                                    SPL01290
          WRITE(6,994)R,TIME1(R),Y(R),K(R)                              SPL01300
   20 CONTINUE                                                          SPL01310
      L=M-20                                                            SPL01320
      WRITE(6,995)LAST                                                  SPL01330
      DO 30 R=L,M,1                                                     SPL01340
          WRITE(6,994)R,TIME1(R),Y(R),K(R)                              SPL01350
   30 CONTINUE                                                          SPL01360
C                                                                       SPL01370
C                                                                       SPL01380
C          NCAP7 IS THE HIGHEST DIMENSION OF K TO BE GENERATED          SPL01390
C          BY THE SUBROUTINE E02BAF. THIS SUBROUTINE GENERATES          SPL01400
C          A B-SPLINE REPRESENTATION OF A FUNCTION REPRESENTED          SPL01410
C          BY THE CHOSEN DATA VALUES .                                  SPL01420
C                                                                       SPL01430
C                                                                       SPL01440
      NCAP7=NCAP+7                                                      SPL01450
      IFAIL=0                                                           SPL01460
      CALL MYBAF(M,NCAP7,TIME1,Y,W,K,WORK1,WORK2,C,SS,IFAIL)            SPL01470
      IF(IFAIL.NE.0)GOTO 777                                            SPL01480
```

```
C                                                                       SPL01490
C                                                                       SPL01500
C         IN THE FOLLOWING SECTION IF 'AMIDPT' IS .TRUE. THEN           SPL01510
C         THE  RESPECTIVE  VALUE  OF X  LIES  INBETWEEN  KNOT           SPL01520
C         ( AND INPUT DATA )  POSITIONS AND A Y VALUE MUST BE           SPL01530
C         FOUND . M2 AND M3  SET THE  START AND FINISH POINTS           SPL01540
C         FOR  THE  FITTING  AND  THE  FINAL  DATA  LISTING .           SPL01550
C                                                                       SPL01560
C                                                                       SPL01570
      AMIDPT=.TRUE.                                                     SPL01580
      LEFT=1                                                            SPL01590
      M1=IXTRA*M                                                        SPL01600
      M2=14*IXTRA+1                                                     SPL01610
      M3=M1-((14*IXTRA)+1)                                              SPL01620
C                                                                       SPL01630
C           'STEP' IS THE TIME BETWEEN EACH OF THE                      SPL01640
C           INTERPOLATED POINTS.                                        SPL01650
C                                                                       SPL01660
C           THE FOLLOWING  'DO LOOP' SETS UP AN ARRAY                   SPL01670
C           T(IXTRA),T(IXTRA+1),T(IXTRA+2)....ETC.                      SPL01680
C           CONTAINING ALL VALUES OF TIME AT WHICH A                    SPL01690
C           VALUE IS REQUIRED FROM THE SPLINE FIT.                      SPL01700
C                                                                       SPL01710
C                                                                       SPL01720
      STEP=TSTEP/IXTRA                                                  SPL01730
      DO 60 L=IXTRA,M1,IXTRA                                            SPL01740
         J=L/IXTRA                                                      SPL01750
         Z=0                                                            SPL01760
   58    IF(KOUNT.EQ.1) T(L+Z)=T1(J,6)+0.0000086+STEP*Z                 SPL01770
         IF(KOUNT.EQ.2) T(L+Z)=T1(J,7)+0.0000150+STEP*Z                 SPL01780
         IF(KOUNT.EQ.3) T(L+Z)=T1(J,8)+0.0000214+STEP*Z                 SPL01790
         IF(KOUNT.EQ.4) T(L+Z)=T1(J,1)+0.0000288+STEP*Z                 SPL01800
         Z=Z+1                                                          SPL01810
         IF(Z.GT.EXTRA)GOTO 59                                          SPL01820
         GOTO 58                                                        SPL01830
   59    CONTINUE                                                       SPL01840
   60    CONTINUE                                                       SPL01850
      J=0                                                               SPL01860
      I=0                                                               SPL01870
      ITIME=0                                                           SPL01880
      IF(RESULT.EQ.1.OR.RESULT.EQ.2) WRITE(6,992)                       SPL01890
      DO 40 N=M2,M3                                                     SPL01900
         XVAR=T(N)                                                      SPL01910
         IFAIL=1                                                        SPL01920
         CALL MYBCF(NCAP7,K,C,XVAR,LEFT,FIT,IFAIL)                      SPL01930
         IF(IFAIL.NE.0)GOTO 320                                         SPL01940
         IF(N.GT.M2+30.AND.N.LT.M3-30) GOTO 295                         SPL01950
         IF(RESULT.EQ.1.OR.RESULT.EQ.2) WRITE(6,990)XVAR,T(N),FIT(1),   SPL01960
     +   FIT(2)                                                         SPL01970
  295    IF(KOUNT.EQ.1)OUT1(N)=FIT(1)                                   SPL01980
         IF(KOUNT.EQ.2)OUT2(N)=FIT(1)                                   SPL01990
         IF(KOUNT.EQ.3)OUT3(N)=FIT(1)                                   SPL02000
         IF(KOUNT.EQ.4)OUT4(N)=FIT(1)                                   SPL02010
         I=I+1                                                          SPL02020
         IF(I.NE.IXTRA) GOTO 340                                        SPL02030
  300    I=0                                                            SPL02040
         AMIDPT=.NOT.AMIDPT                                             SPL02050
         IF(KOUNT.EQ.1) T(N)=T(N)-0.0000086                             SPL02060
         IF(KOUNT.EQ.2) T(N)=T(N)-0.0000150                             SPL02070
         IF(KOUNT.EQ.3) T(N)=T(N)-0.0000214                             SPL02080
         IF(KOUNT.EQ.4) T(N)=T(N)-0.0000288                             SPL02090
         XVAR=T(N)                                                      SPL02100
         IFAIL=0                                                        SPL02110
         CALL MYBCF(NCAP7,K,C,XVAR,LEFT,FIT,IFAIL)                      SPL02120
         IF(IFAIL.NE.0)GOTO 320                                         SPL02130
         R=N/IXTRA                                                      SPL02140
         RES=FIT(1)-Y(R)                                                SPL02150
         IF(N.GT.M2+30.AND.N.LT.M3-30) GOTO 340                         SPL02160
         IF(RESULT.EQ.1.OR.RESULT.EQ.2)WRITE(6,991)XVAR,T(N),           SPL02170
     +   FIT(1),RES,FIT(2)                                              SPL02180
         GOTO 340                                                       SPL02190
  320    WRITE(6,989)XVAR                                               SPL02200
         J=J+1                                                          SPL02210
         IF(J.GE.50) GOTO 1111                                          SPL02220
  340    CONTINUE                                                       SPL02230
   40 CONTINUE                                                          SPL02240
 1111 CONTINUE                                                          SPL02250
      IF(RESULT.EQ.2) GOTO 1113                                         SPL02260
      WRITE(6,981)                                                      SPL02270
      M4=M2                                                             SPL02280
      DO 1112 R=M2,M3,1                                                 SPL02290
         WRITE(6,980) OUT1(R),OUT2(R),OUT3(R),OUT4(R)                   SPL02300
 1112 CONTINUE                                                          SPL02310
```

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 1113 CONTINUE                                                          SPL02320
      GOTO 888                                                          SPL02330
  555 WRITE(6,988)R                                                     SPL02340
      GOTO 888                                                          SPL02350
  777 GOTO(360,380,400,420,440),IFAIL                                   SPL02360
  360 WRITE(6,987)                                                      SPL02370
      GOTO 888                                                          SPL02380
  380 WRITE(6,986)                                                      SPL02390
      GOTO 888                                                          SPL02400
  400 WRITE(6,985)                                                      SPL02410
      GOTO 888                                                          SPL02420
  420 WRITE(6,984)                                                      SPL02430
      GOTO 888                                                          SPL02440
  440 WRITE(6,983)                                                      SPL02450
      GOTO 888                                                          SPL02460
  999 FORMAT(6A4)                                                       SPL02470
  998 FORMAT(4(1X/),1H ,6A4)                                            SPL02480
  997 FORMAT(2(1X/),30H     M = NO. OF DATA POINTS = ,I4,               SPL02490
     + //52H NCAP = NO. OF INTERPOLATED INTERVALS BETWEEN INTERN,        SPL02500
     + 11HAL KNOTS = ,I4)                                               SPL02510
C 996 FORMAT(1H ,8(F8.4,1X))                                            SPL02520
  996 FORMAT(1H ,8(F12.8,1X))                                           SPL02530
  995 FORMAT(2(1X//),2H  ,A8,29H 20 LINES OF DATA FOR FIT AND,          SPL02540
     + 15H KNOT POSITIONS,                                              SPL02550
     +/52H  ------------------------------------------------//,         SPL02560
     +/58H      R             T1(R)           Y(R)              K(R)//) SPL02570
  994 FORMAT(1X/,4H    ,I4,8X,F10.5,8X,F8.4,8X,F10.5)                   SPL02580
  993 FORMAT(3(1X/),16H     OUTPUT DATA,1X/,17H    ------------)        SPL02590
  992 FORMAT(2(1X/),48H         X      TIME       FITTED Y      RESIDUE,SPL02600
     +16H        GRADIENT,                                              SPL02610
     +/53H     ------------------------------------------------,        SPL02620
     +18H-----------------,                                             SPL02630
     +/53H     ------------------------------------------------,        SPL02640
     +18H-----------------//)                                           SPL02650
  991 FORMAT(1H ,2X,F9.6,2X,F9.6,3X,F8.4,4X,E12.4,4X,F12.4)             SPL02660
  990 FORMAT(1H ,2X,F9.6,2X,F9.6,3X,F8.4,20X,F12.4)                     SPL02670
  989 FORMAT(/1X,27HARGUMENT OUTSIDE RANGE     ,E20.5)                 SPL02680
  988 FORMAT(1X/,15H NO MORE DATA ,,I4,11H LINES READ//)                SPL02690
  987 FORMAT(/47H KNOTS DISORDERED OR NOT INTERIOR TO DATA INTER,       SPL02700
     +3HVAL)                                                            SPL02710
  986 FORMAT(/20H NON-POSITIVE WEIGHT)                                  SPL02720
  985 FORMAT(/46H DISORDERED VALUES OF THE INDEPENDANT VARIABLE)        SPL02730
  984 FORMAT(/42H TOO MANY KNOTS FOR TKE NUMBER OF DISTINCT,            SPL02740
     +35H VALUES OF THE INDEPENDANT VARIABLE)                           SPL02750
  983 FORMAT(/42H NO UNIQUE SOLUTION SINCE SHOENBURG-WITNEY,            SPL02760
     +20H CONDITIONS VIOLATED)                                          SPL02770
  982 FORMAT(6(1X/),22H        ****** KOUNT = ,I2,6H ******)           SPL02780
  981 FORMAT(6(1X/),40H  COMPLETE LISTING OF OUTPUT NOW FOLLOWS,        SPL02790
     +/41H ---------------------------------------,                     SPL02800
     +/41H ---------------------------------------,                     SPL02810
     +///55H       TIME      CHANNEL1----GRADIENT      CHANNEL2----    SPL02820
     +8HGRADIENT//)                                                     SPL02830
  980 FORMAT(1H ,4(F12.4,1X))                                           SPL02840
  979 FORMAT(///40H     INVALID VALUE OF  'KOUNT', KOUNT = ,I3,///)     SPL02850
  888 STOP                                                              SPL02860
      END                                                               SPL02870
```

C.IV SPLI30C FORTRAN Program Listing

FILE: SPLI30C FORTRAN A1 (EE68) 2/08/85 15:46:42

```
      DOUBLE PRECISION VR(800),VY(800),VB(800),IP(800),IQ(800),          SPL00010
     +IR(800),IY(800),IB(800),SS,XARG,RES,Y(800),W(800),C(900),          SPL00020
     +WORK1(800),WORK2(4,800),LAST,FIT(4),X(800),K(800),T(800),          SPL00030
     +T1(800),                                                           SPL00040
     +XTOT,XSTART,XFIN,XVAR,OUT1(800),OUT2(800),OUT3(800),OUT4(800),     SPL00050
     +OUT5(800),OUT6(800),OUT7(800),OUT8(800),OUT9(800)                  SPL00060
      INTEGER I,NCAP,NCAP7,J,IFAIL,J2,M,L,N,R,M1,M2,M3,LEFT,             SPL00070
     +KOUNT,RESULT,ITIME,Z                                               SPL00080
      LOGICAL AMIDPT,OPWIDE                                              SPL00090
C     DATA FIRST/6HFIRST /                                               SPL00100
C     DATA LAST/6HLAST  /                                                SPL00110
C     DATA SECOND/6HSECOND/                                              SPL00120
C     DATA THIRD/6HTHIRD /                                               SPL00130
C     DATA FOURTH/6HFOURTH/                                              SPL00140
C                                                                        SPL00150
C.....SPLI30C.....ATTEMPTS TO GIVE THREE PHASE CURRENTS,THEIR            SPL00160
C          DERIVATIVES AND THE THREE PHASE VOLTAGES .                    SPL00170
C          (FOR THE COMPUTATIONAL MODEL)    (FORMERLY SPLINE6)           SPL00180
C                                                                        SPL00190
C          USING A VALUE OF M GREATER THAN ABOUT 900 IN THIS PROGRAM     SPL00200
C          GIVES ERRORS IN THE SPLINE FITTING ROUTINE RELATING TO        SPL00210
C          THE RATIO OF DATA POINTS TO KNOTS.                            SPL00220
C                                                                        SPL00230
C          THEREFORE IT IS SUGGESTED THAT INTERPOLATION BE PERFORMED     SPL00240
C          REPETITIVELY WHERE MORE THAN 30 CYCLES ARE REQUIRED.          SPL00250
C                                                                        SPL00260
C          EXTRA = 0.0  SO THAT NO INTERPOLATION IS PERFORMED .          SPL00270
C                       ----------------------------                     SPL00280
C                                                                        SPL00290
C          SINCE OUTPUT OF A DETAILED RESULTS LIST FOLLOWED BY A         SPL00300
C          CONTINUOUS LISTING FOR USE AS INPUT DATA IS OFTEN EXESSIVE,   SPL00310
C          'RESULTS' SHOULD BE SET AT :                                  SPL00320
C                    1 -FOR BOTH LISTINGS                                SPL00330
C                    2 -FOR ONLY THE 'DETAILED'LISTING                   SPL00340
C                    3 -FOR ONLY THE 'CONTINUOUS' LISTING                SPL00350
C                                                                        SPL00360
C                                                                        SPL00370
C          'OPWIDE' SET TRUE WILL NEED AN OUTPUT FILE WIDTH 130          SPL00380
C                                                                        SPL00390
C          TSTEP IS THE TIME STEP OF INPUT DATA .                        SPL00400
C                                                                        SPL00410
C                                                                        SPL00420
      M=780                                                              SPL00430
      RESULT=1                                                           SPL00440
      OPWIDE=.TRUE.                                                      SPL00450
      TSTEP=0.0008                                                       SPL00460
      EXTRA=0.0                                                          SPL00470
      IXTRA=IFIX(EXTRA)+1                                                SPL00480
      NCAP=M-7                                                           SPL00490
      NCAP3=NCAP+3                                                       SPL00500
      NCAP7=NCAP+7                                                       SPL00510
C                                                                        SPL00520
C                                                                        SPL00530
C          THE FOLLOWING LOOP READS ALL EIGHT CHANNELS OF DATA,          SPL00540
C          SPECIFIES THE  DEPENDANT  VARIABLE TO BE USED,                SPL00550
C          SETS ALL WEIGHTS TO 1.0 AND SPECIFIES KNOTS K(5) TO           SPL00560
C          K(NCAP+3) TO BE AT THE SAME ORDINATES AS X(5) TO              SPL00570
C          X(NCAP+3). THE X-AXIS IS SCALED SUCH THAT THERE IS            SPL00580
C          AN INPUT DATA VALUE AT EVERY FOURTH INTEGER POINT.            SPL00590
C                                                                        SPL00600
C                                                                        SPL00610
      READ(5,996)VR(1),VY(1),VB(1),IP(1),IQ(1),IR(1),IY(1),IB(1)         SPL00620
      W(1)=1.0                                                           SPL00630
      T(1)=0.0                                                           SPL00640
      DO 10 R=2,M                                                        SPL00650
          READ(5,996)VR(R),VY(R),VB(R),IP(R),IQ(R),IR(R),IY(R),IB(R)     SPL00660
          IF(VR(R).EQ.0.0.AND.VY(R).EQ.0.0)GOTO 555                      SPL00670
          T(R)=T(R-1)+TSTEP                                              SPL00680
      W(R)=1.0                                                           SPL00690
   10 CONTINUE                                                           SPL00700
```

```
C                                                                       SPL00710
C          THE NEXT LOOP VARIES 'KOUNT' ,SPECIFYING WHICH               SPL00720
C          CHANNEL THE SPLINE IS FITTED FOR.                            SPL00730
C                                                                       SPL00740
C                                                                       SPL00750
C     KOUNT=1                                                           SPL00760
      DO 1111 KOUNT=1,6                                                 SPL00770
      IF(KOUNT.EQ.1)GOTO 12                                             SPL00780
      DO 11 R=1,M                                                       SPL00790
           K(R)=0.0                                                     SPL00800
           C(R)=0.0                                                     SPL00810
   11 CONTINUE                                                          SPL00820
      SS=0.0                                                            SPL00830
   12 CONTINUE                                                          SPL00840
      DO 14 R=1,M,1                                                     SPL00850
          IF(KOUNT.NE.1)GOTO 124                                        SPL00860
          Y(R)=IR(R)                                                    SPL00870
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL00880
          GOTO 14                                                       SPL00890
  124     IF(KOUNT.NE.2)GOTO 125                                        SPL00900
          Y(R)=IY(R)                                                    SPL00910
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL00920
          GOTO 14                                                       SPL00930
  125     IF(KOUNT.NE.3)GOTO 126                                        SPL00940
          Y(R)=IB(R)                                                    SPL00950
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL00960
          GOTO 14                                                       SPL00970
  126     IF(KOUNT.NE.4)GOTO 127                                        SPL00980
          Y(R)=VR(R)                                                    SPL00990
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL01000
          GOTO 14                                                       SPL01010
  127     IF(KOUNT.NE.5)GOTO 128                                        SPL01020
          Y(R)=VY(R)                                                    SPL01030
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL01040
          GOTO 14                                                       SPL01050
  128     IF(KOUNT.NE.6)GOTO 13                                         SPL01060
          Y(R)=VB(R)                                                    SPL01070
          IF(R.GT.4.AND.R.LE.NCAP3)K(R)=T(R)                            SPL01080
          GOTO 14                                                       SPL01090
   13     WRITE(6,979)KOUNT                                             SPL01100
   14 CONTINUE                                                          SPL01110
C                                                                       SPL01120
C                                                                       SPL01130
C          AFTER  PRINTING  RESPECTIVE HEADINGS , THE FIRST TEN         SPL01140
C          CHOSEN  DATA  VALUES  ARE  WRITTEN ,  TOGETHER  WITH         SPL01150
C          VALUES OF R , X(R) AND  K(R).                                SPL01160
C                                                                       SPL01170
C                                                                       SPL01180
C     IF(KOUNT.EQ.1)YNUM=FIRST                                          SPL01190
C     IF(KOUNT.EQ.2)YNUM=SECOND                                         SPL01200
C     IF(KOUNT.EQ.3)YNUM=THIRD                                          SPL01210
C     IF(KOUNT.EQ.4)YNUM=FOURTH                                         SPL01220
      IF(RESULT.GT.2)GOTO 30                                            SPL01230
      WRITE(6,997)M,NCAP                                                SPL01240
      WRITE(6,995)FIRST                                                 SPL01250
      WRITE(6,994)((R,T(R),Y(R),K(R)),R=1,20)                           SPL01260
      L=M-20                                                            SPL01270
      WRITE(6,995)LAST                                                  SPL01280
      WRITE(6,994)((R,T(R),Y(R),K(R)),R=L,M)                            SPL01290
   30 CONTINUE                                                          SPL01300
C                                                                       SPL01310
C                                                                       SPL01320
C          NCAP7 IS THE HIGHEST DIMENSION OF K TO BE GENERATED          SPL01330
C          BY THE SUBROUTINE E02BAF. THIS SUBROUTINE GENERATES          SPL01340
C          A B-SPLINE REPRESENTATION OF A FUNCTION REPRESENTED          SPL01350
C          BY THE CHOSEN DATA VALUES .                                  SPL01360
C                                                                       SPL01370
C                                                                       SPL01380
      NCAP7=NCAP+7                                                      SPL0139C
      IFAIL=1                                                           SPL01400
      CALL  MYBAF(M,NCAP7,T,Y,W,K,WORK1,WORK2,C,SS,IFAIL)               SPL01410
      IF(IFAIL.NE.0)GOTO 777                                            SPL01420
```

```
C                                                                       SPL01430
C                                                                       SPL01440
C         IN THE FOLLOWING SECTION IF 'AMIDPT' IS .TRUE. THEN           SPL01450
C         THE  RESPECTIVE  VALUE  OF X  LIES  INBETWEEN  KNOT           SPL01460
C         ( AND INPUT DATA )  POSITIONS AND A Y VALUE MUST BE           SPL01470
C         FOUND . M2 AND M3  SET THE  START AND FINISH POINTS           SPL01480
C         FOR  THE . FITTING  AND  THE  FINAL  DATA  LISTING .          SPL01490
C                                                                       SPL01500
C                                                                       SPL01510
      AMIDPT=.FALSE.                                                    SPL01520
      LEFT=1                                                            SPL01530
      M1=IXTRA*M                                                        SPL01540
      M2=14*IXTRA                                                       SPL01550
      M3=M1-((14*IXTRA)+1)                                              SPL01560
C                                                                       SPL01570
C           'STEP' IS THE TIME BETWEEN EACH OF THE                      SPL01580
C           INTERPOLATED POINTS.                                        SPL01590
C                                                                       SPL01600
C           THE FOLLOWING  'DO LOOP' SETS UP AN ARRAY                   SPL01610
C           T(IXTRA),T(IXTRA+1),T(IXTRA+2)....ETC.                      SPL01620
C           CONTAINING ALL VALUES OF TIME AT WHICH A                    SPL01630
C           VALUE IS REQUIRED FROM THE SPLINE FIT.                      SPL01640
C                                                                       SPL01650
C                                                                       SPL01660
      STEP=TSTEP/IXTRA                                                  SPL01670
      DO 60 L=IXTRA,M1,IXTRA                                            SPL01680
         J=L/IXTRA                                                      SPL01690
         Z=0                                                            SPL01700
   58    T1(L+Z)=T(J)+STEP*Z                                            SPL01710
         Z=Z+1                                                          SPL01720
         IF(Z.GT.EXTRA)GOTO 59                                          SPL01730
         GOTO 58                                                        SPL01740
   59    CONTINUE                                                       SPL01750
   60    CONTINUE                                                       SPL01760
      I=0                                                               SPL01770
      J=0                                                               SPL01780
      ITIME=0                                                           SPL01790
      IF(RESULT.EQ.1.OR.RESULT.EQ.2) WRITE(6,992)                       SPL01800
      DO 40 N=M2,M3,1                                                   SPL01810
         IF(AMIDPT) GOTO 290                                            SPL01820
         GOTO 300                                                       SPL01830
  290    XVAR=T1(N)                                                     SPL01840
         IFAIL=1                                                        SPL01850
         CALL  MYBCF(NCAP7,K,C,XVAR,LEFT,FIT,IFAIL)                     SPL01860
         IF(IFAIL.NE.0)GOTO 320                                         SPL01870
         IF(N.GT.M2+30.AND.N.LT.M3-30) GOTO 295                         SPL01880
         IF(RESULT.EQ.1.OR.RESULT.EQ.2) WRITE(6,990)XVAR,T1(N),FIT(1),  SPL01890
     +   FIT(2)                                                         SPL01900
  295    IF(KOUNT.EQ.1)OUT4(N)=FIT(1)                                   SPL01910
         IF(KOUNT.EQ.1)OUT7(N)=FIT(2)                                   SPL01920
         IF(KOUNT.EQ.2)OUT5(N)=FIT(1)                                   SPL01930
         IF(KOUNT.EQ.2)OUT8(N)=FIT(2)                                   SPL01940
         IF(KOUNT.EQ.3)OUT6(N)=FIT(1)                                   SPL01950
         IF(KOUNT.EQ.3)OUT9(N)=FIT(2)                                   SPL01960
         IF(KOUNT.EQ.4)OUT1(N)=FIT(1)                                   SPL01970
         IF(KOUNT.EQ.5)OUT2(N)=FIT(1)                                   SPL01980
         IF(KOUNT.EQ.6)OUT3(N)=FIT(1)                                   SPL01990
         I=I+1                                                          SPL02000
         IF(I.EQ.IXTRA-1) AMIDPT=.FALSE.                                SPL02010
         GOTO 340                                                       SPL02020
  300    I=0                                                            SPL02030
         IF(IXTRA.NE.1) AMIDPT=.NOT.AMIDPT                              SPL02040
         XVAR=T1(N)                                                     SPL02050
         IFAIL=1                                                        SPL02060
         CALL  MYBCF(NCAP7,K,C,XVAR,LEFT,FIT,IFAIL)                     SPL02070
         IF(IFAIL.NE.0)GOTO 320                                         SPL02080
         R=N/IXTRA                                                      SPL02090
         RES=FIT(1)-Y(R)                                                SPL02100
         IF(N.GT.M2+30.AND.N.LT.M3-30) GOTO 310                         SPL02110
         IF(RESULT.EQ.1.OR.RESULT.EQ.2)WRITE(6,991)XVAR,T1(N),          SPL02120
     +   FIT(1),RES,FIT(2)                                              SPL02130
  310    IF(KOUNT.EQ.1)OUT4(N)=FIT(1)                                   SPL02140
         IF(KOUNT.EQ.1)OUT7(N)=FIT(2)                                   SPL02150
         IF(KOUNT.EQ.2)OUT5(N)=FIT(1)                                   SPL02160
         IF(KOUNT.EQ.2)OUT8(N)=FIT(2)                                   SPL02170
         IF(KOUNT.EQ.3)OUT6(N)=FIT(1)                                   SPL02180
         IF(KOUNT.EQ.3)OUT9(N)=FIT(2)                                   SPL02190
         IF(KOUNT.EQ.4)OUT1(N)=FIT(1)                                   SPL02200
         IF(KOUNT.EQ.5)OUT2(N)=FIT(1)                                   SPL02210
         IF(KOUNT.EQ.6)OUT3(N)=FIT(1)                                   SPL02220
         GOTO 340                                                       SPL02230
  320    WRITE(6,989)XVAR                                               SPL02240
```

```
      J=J+1                                                              SPL02250
      IF(J.GE.50) GOTO 1111                                              SPL02260
  340 CONTINUE                                                           SPL02270
   40 CONTINUE                                                           SPL02280
 1111 CONTINUE                                                           SPL02290
      IF(RESULT.EQ.2) GOTO 1113                                          SPL02300
      WRITE(6,981)                                                       SPL02310
      DO 1112 R=M2,M3,1                                                  SPL02320
         IF(OPWIDE) WRITE(6,978) OUT1(R),OUT2(R),OUT3(R),OUT4(R),        SPL02330
     +   OUT5(R),OUT6(R),OUT7(R),OUT8(R),OUT9(R)                         SPL02340
         IF(.NOT.OPWIDE) WRITE(6,980) OUT1(R),OUT2(R),OUT3(R),OUT4(R),   SPL02350
     +   OUT5(R),OUT6(R),OUT7(R),OUT8(R),OUT9(R)                         SPL02360
 1112 CONTINUE                                                           SPL02370
 1113 CONTINUE                                                           SPL02380
      GOTO 888                                                           SPL02390
  555 WRITE(6,988)R                                                      SPL02400
      GOTO 888                                                           SPL02410
  777 GOTO(360,380,400,420,440),IFAIL                                    SPL02420
  360 WRITE(6,987)                                                       SPL02430
      GOTO 888                                                           SPL02440
  380 WRITE(6,986)                                                       SPL02450
      GOTO 888                                                           SPL02460
  400 WRITE(6,985)                                                       SPL02470
      GOTO 888                                                           SPL02480
  420 WRITE(6,984)                                                       SPL02490
      GOTO 888                                                           SPL02500
  440 WRITE(6,983)                                                       SPL02510
      GOTO 888                                                           SPL02520
  999 FORMAT(6A4)                                                        SPL02530
  998 FORMAT(4(1X/),1H ,6A4)                                             SPL02540
  997 FORMAT(2(1X/),30H     M = NO. OF DATA POINTS = ,I4,                SPL02550
     + //52H NCAP = NO. OF INTERPOLATED INTERVALS BETWEEN INTERN,         SPL02560
     + 11HAL KNOTS = ,I4)                                                SPL02570
C 996 FORMAT(1H ,8(F8.4,1X))                                             SPL02580
  996 FORMAT(1H ,8(F12.8,1X))                                            SPL02590
  995 FORMAT(2(1X//),2H  ,A6,29H 20 LINES OF DATA FOR FIT AND,           SPL02600
     + 15H KNOT POSITIONS,                                               SPL02610
     +/52H  ----------------------------------------------//,            SPL02620
     +/58H      R            T1(R)           Y(R)             K(R)//)   SPL02630
  994 FORMAT(1X/,4H    ,I4,8X,F10.5,8X,F8.4,8X,F10.5)                    SPL02640
  993 FORMAT(3(1X/),16H     OUTPUT DATA,1X/,17H    ------------)          SPL02650
  992 FORMAT(2(1X/),48H         X      TIME       FITTED Y      RESIDUE,SPL02660
     +16H        GRADIENT,                                               SPL02670
     +/53H     ----------------------------------------------,           SPL02680
     +18H-----------------,                                              SPL02690
     +/53H     ----------------------------------------------,           SPL02700
     +18H-----------------//)                                            SPL02710
  991 FORMAT(1H ,2X,F9.6,2X,F9.6,3X,F8.4,4X,E12.4,4X,F12.4)              SPL02720
  990 FORMAT(1H ,2X,F9.6,2X,F9.6,3X,F8.4,20X,F12.4)                      SPL02730
  989 FORMAT(/1X,27HARGUMENT OUTSIDE RANGE     ,E20.5)                  SPL02740
  988 FORMAT(1X/,15H NO MORE DATA ,,I4,11H LINES READ//)                 SPL02750
  987 FORMAT(/47H KNOTS DISORDERED OR NOT INTERIOR TO DATA INTER,        SPL02760
     +3HVAL)                                                             SPL02770
  986 FORMAT(/20H NON-POSITIVE WEIGHT)                                   SPL02780
  985 FORMAT(/46H DISORDERED VALUES OF THE INDEPENDANT VARIABLE)         SPL02790
  984 FORMAT(/42H TOO MANY KNOTS FOR TKE NUMBER OF DISTINCT,             SPL02800
     +35H VALUES OF THE INDEPENDANT VARIABLE)                            SPL02810
  983 FORMAT(/42H NO UNIQUE SOLUTION SINCE SHOENBURG-WITNEY,             SPL02820
     +20H CONDITIONS VIOLATED)                                           SPL02830
  982 FORMAT(6(1X/),22H       ***** KOUNT = ,I2,6H *****)               SPL02840
  981 FORMAT(6(1X/),40H  COMPLETE LISTING OF OUTPUT NOW FOLLOWS,         SPL02850
     +/41H ---------------------------------------,                      SPL02860
     +/41H ---------------------------------------,                      SPL02870
     +///55H       TIME      CHANNEL1----GRADIENT      CHANNEL2----     SPL02880
     +8HGRADIENT//)                                                      SPL02890
  980 FORMAT(1H ,3(F6.2,1X),3(F7.4,1X),3(F8.3,1X))                       SPL02900
  979 FORMAT(///40H     INVALID VALUE OF  'KOUNT', KOUNT = ,I3,///)      SPL02910
  978 FORMAT(1H ,3(F10.6,1X),2X,3(F1'.7,1X),2X,3(F10.4,1X))              SPL02920
  888 STOP                                                               SPL02930
      END                                                                SPL02940
```

C.V Results and Error Magnitudes

The results output from application of the programs to consecutive blocks of 750 time series data points overlapped slightly due to the extra 15 points at each end of the data span. When the three interpolated output files were combined, the overlapping was carefully eliminated, to give output files of:

(i) For input to the physical model:

9000 time-series data records with
I_R, I_Y, I_B on each record.
Record step length = 100 microseconds.

(ii) For input to the computational model:

2250 time-series data records, with
I_R, I_Y, I_B, $\frac{dI_R}{dt}$, $\frac{dI_Y}{dt}$, $\frac{dI_B}{dt}$ on each record.
Record step length = 800 microseconds.

The error magnitudes were estimated by calculation of the quantity,

$$E(x) = S(x) - y(x)$$

and were always less than 10^{-8} percent over the non-overlapping region of the B-spline fit. The end regions of the B-spline were slightly less accurate, with always less than 10^{-4} percentage error.

APPENDIX D

AIM-65 MICROCOMPUTER OPERATION, INTERFACE AND PROGRAM LISTINGS

D.I Overview

The Rockwell R6500 Advanced Interactive Microcomputer[83,84,85,86], (AIM-65), was used in the laboratory for the small signal reproduction of arc furnace installation current waveforms, using data loaded from punch-tape.

A block diagram of the AIM-65 system is given in Figure D.1. An extra 16K bytes of dynamic RAM, and two R6522 versatile Interface Adapters were added using the expansion connector.

The memory map for the 64K bytes of addressable I/O and memory was given in Table 2.1 (Section 2.3.2).

D.II Monitor, Editor and Assembler

The monitor program occupied 8K bytes in ROM between addresses E000 and FFFF hex. Application programs could be entered and changed using the text edit facility of the monitor. Programs written in R6502 assembler language source code could then be assembled into object code using the assembler software located in a separate 4K bytes ROM package.

D.III Program Storage

Once assembled, the programs were stored on magnetic tape using the tape input/output facilities of the monitor routine. When programs were correct, there was no need for them to be stored in their source code form, nor for the assembler chip to occupy memory space.

All programs written for use in this research project were stored and run from the 4K byte on-board RAM at address 0000-00FF.

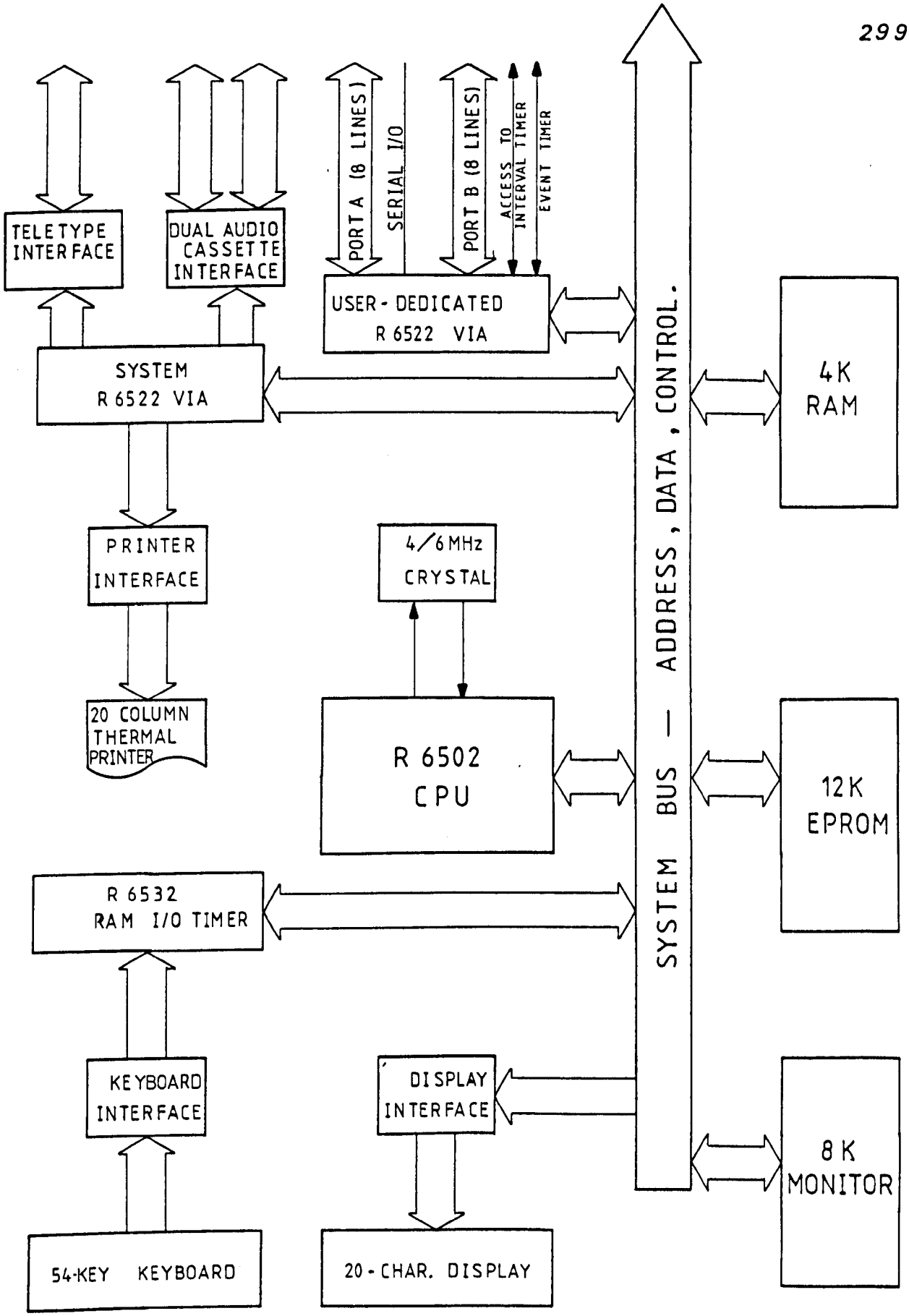


FIG. D1 : AIM-65 BLOCK DIAGRAM

D.IV System Operation

The 'function' keys F1, F3 gave immediate program 'jumps' to memory locations at the start of the program blocks 'START' and 'TAPE READER' respectively.

(a) 'START' The source code listing for this program is given in Section D.V. Once entered, its timing was controlled by a hard wired phase-locked loop outputting a 200kHz square wave in synchronism with the a.c. mains (red phase) voltage. The circuit used to generate the controlling interrupts CA1 and CB1 is shown in Figure D2.

(b) 'TAPE READER' The source code listing this program is given in Section D.VI. The program reads a series of 8-bit values from a punch-tape reader connected at input port A, finishing when a given number of cycles are complete. Data read from the tape is stored in RAM.

When the data output program from 'START' was operating, clock frequency of 6MHz was used to allow a minimum time between consecutive channel outputs (I_R, I_Y, I_B) of 20 microseconds to be achieved. Every 200 microseconds the 8-bit data word for each of channels I_R, I_Y, I_B was sent to port A, with a bit number on Port B selecting a particular DAC to receive the 8-bit word. This value was then held by the DAC until the new value was received 200 microseconds later. The DAC circuit is given in Figure D3, and the analogue outputs fed the low-pass filter circuits shown in Chapter II, Figure 2.5(c).

An additional pulse was output at the start of each repeated 'N' cycles of data, (N = 89 for most applications), to allow measuring and data logging equipment to have a common 'start' time reference. This pulse was output to bit 4 of port B, and was software-timed for a duration of 10 microseconds as shown in the program listing (Section DV).

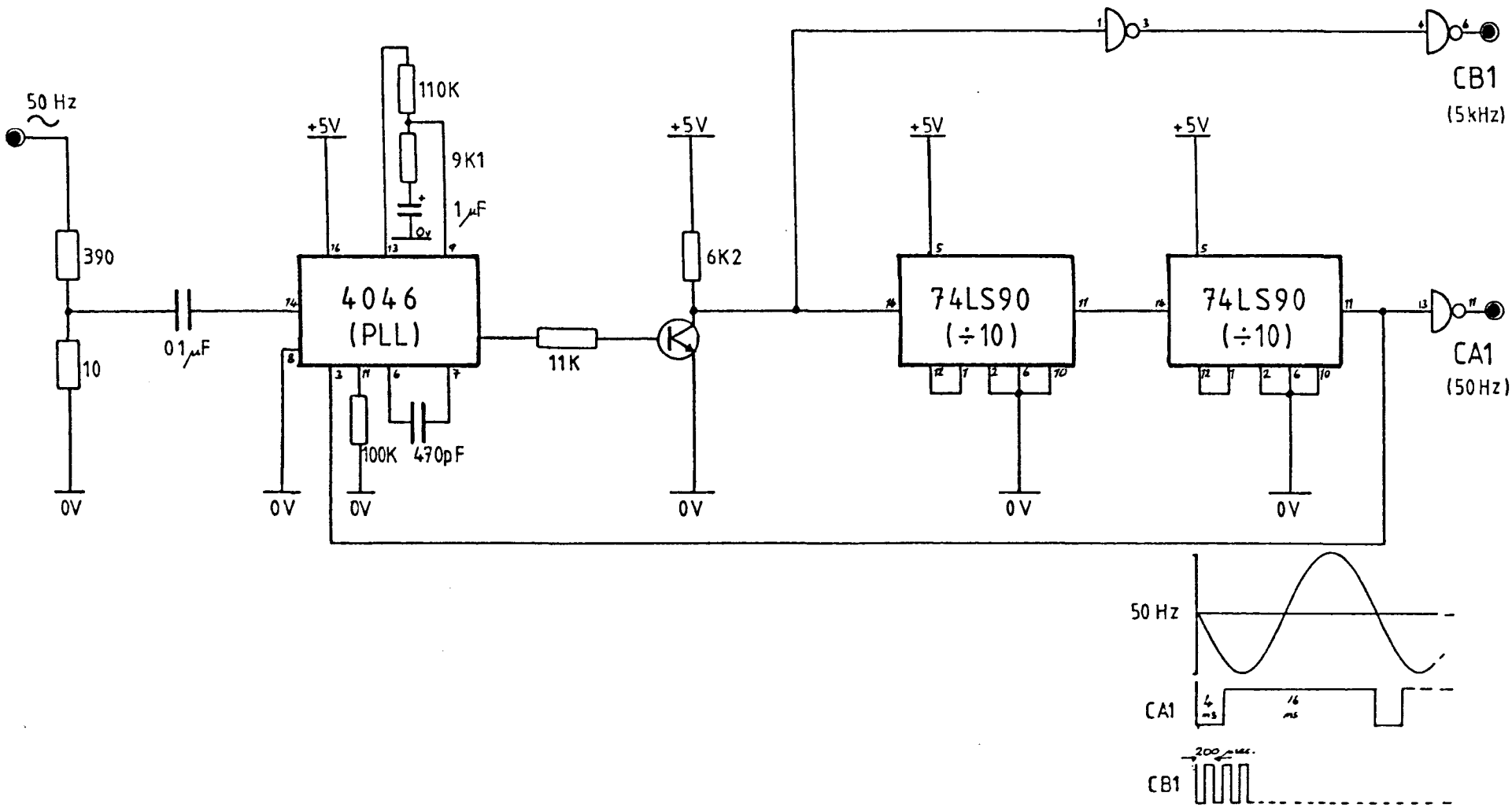
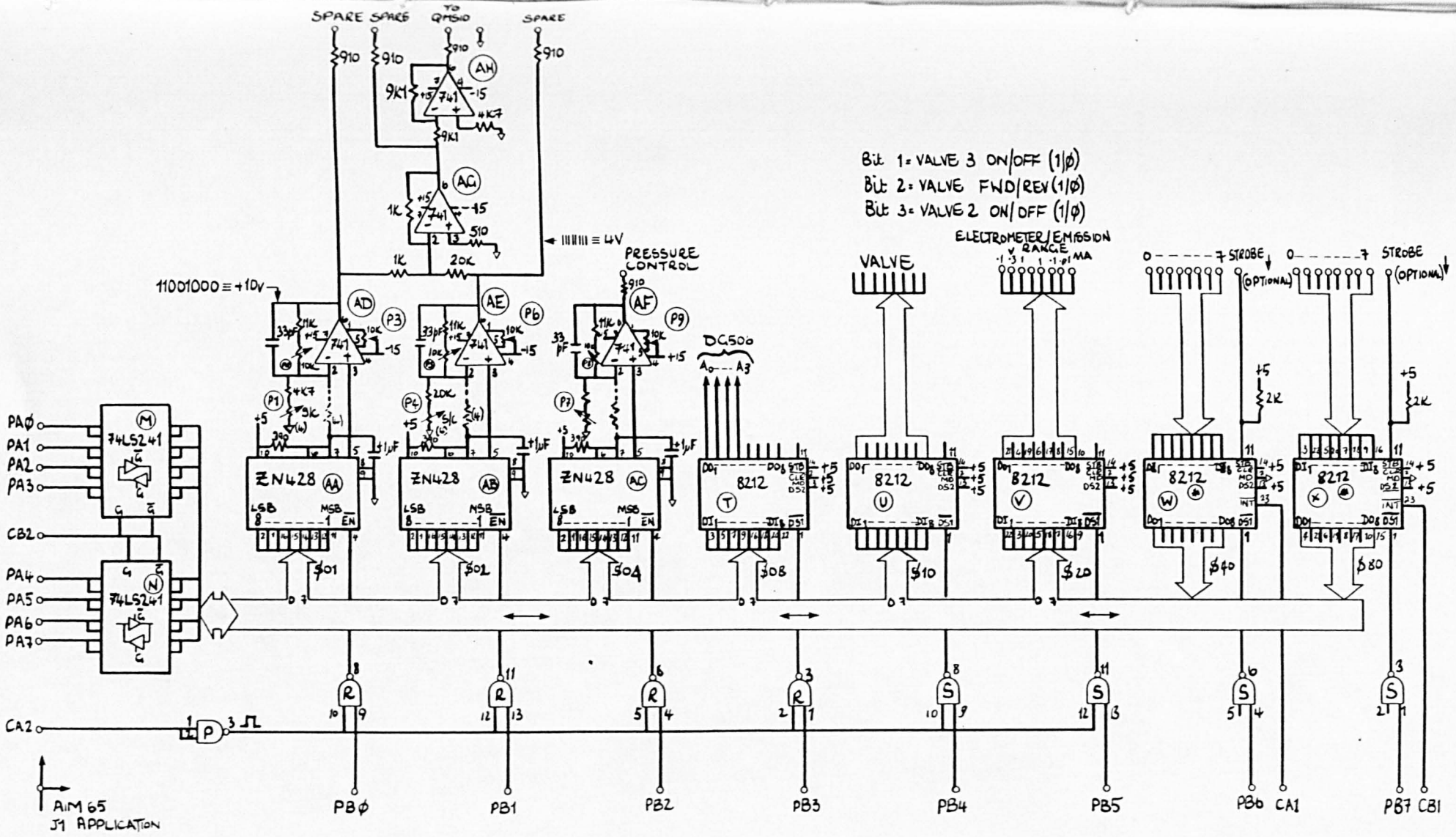


FIG. D2 : Phase-locked loop generation of d ta synchronising pulses



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NOTE

1. ITEMS ⊛ NOT FITTED
2. CB2 IN STATIC MODE, LO → DATA OUT
   HI → DATA IN
   CA2 IN PULSE MODE
3. CA1 & CB1 -VE EDGE INTERRUPT IF REQ'D
4. FITTED FOR BL POLOR OPERATION ONLY

FIG. D3 : Digital to analogue converters for AIM-65

THE UNIVERSITY OF LIVERPOOL ELECTRICAL ENGINEERING AND ELECTRONICS DEPT.		
TITLE 16CHANNEL ADC / I/O	DATE 20/2/81	JOB NO 982

D.V Waveform Regeneration Program Listing

```
;*****************************************************************

;                                       WAVEFORM REGEN. PROGRAM


INITIALISE;                             ;Declares variables.
        NCYCLE  =$00                    ;Current no. of cycles.
        BAL     =$01                    ;Address low.
        BAH     =$02                    ;Address high.
        NUM     =$03                    ;No. of cycles for output.
        TEMP    =$04                    ;For temporary storage.
        HADDR   =$05                    ;Initial address high.
        LADDR   =$06                    ;Initial address low.
        DEVICE  =$A000                  ;Port B output data register.
        OUT     =$A001                  ;Port A output data register.
        PCR     =$A00C                  ;Peripheral control register.
        DDRB    =$A002                  ;Port B data direction register.
        DDRA    =$A003                  ;Port A data direction register.
        IER     =$A00E                  ;Interrupt enable register.
        IFR     =$A00D                  ;Interrupt flag register.
        PRIFLG  =$A411                  ;Printer flag.
        CRCK    =$EA24                  ;CRLF to display.
        M1      =$0500                  ;Message addresses.
        M2      =$050F
        MSG     =$063F                  ;Subroutine addresses
        GETVAL  =$064E
        BCDBIN  =$0666
        RBYTE   =$E3FD

        *=$010C                         ;Start program if 'F1' key pressed.
        JMP START

        *=$0700
START;
        LDA     #01                     ;Printer off.
        STA     PRIFLG
        JSR     CRCK
        LDX     #M1-M2                  ;Read start address and no. of cycles
        JSR     MSG                     ; -of data to be output to DAC.
        JSR     RBYTE
        STA     HADDR
        STA     BAH
        JSR     RBYTE
        STA     LADDR
        STA     BAL
        JSR     CRCK
        LDX     #M2-M1
        JSR     GETVAL
        JSR     BCDBIN
        TAX                             ;Store no. of cycles in X.
        DEX                             ;X-1
        STX     NUM                     ;Save no. of cycles-1.
        STX     NCYCLE
```

```
RERUN;
        LDA     #04             ;Store interrupt vector.
        STA     $A404
        LDA     #$08
        STA     $A405
        LDA     #$CA            ;Set interrupt sense.
        STA     PCR
        LDA     #$FF            ;Set ports A & B to output.
        STA     DDRA
        STA     DDRB
        LDY     #00
        LDA     #$92            ;Allow interrupts.
        STA     IER
        CLI
IDLE;
        NOP                     ;Wait for interrupts.
        JMP     IDLE

        *=$0800
OUTPUT;
        .BYTE   16,4,2,1        ;Set bits to define output channels.
        ;       VR,R,Y,B
INRPT;
        LDA     IFR             ;Any interrupt.
        AND     #$10            ;CB1 flag bit.
        BEQ     CA1FLG          ;Branch if not CB1.
        LDA     #$80            ;Reset CB1 interrupt latch.
        STA     $A000
        LDA     #00
        STA     $A000
CA1FLG;
        LDA     IFR             ;Interrupt type.
        AND     #$02            ;CA1 flag bit.
        BEQ     DATOUT          ;Branch if not CA1.
        LDA     #$40            ;Reset CA1 interrupt latch.
        STA     $A000
        LDA     #00
        STA     $A000
        DEC     NCYCLE          ;Branch if no. of
        BPL     DATOUT          ; - cycles not complete
        LDA     LADDR           ;Reload start address for output data.
        STA     BAL
        LDA     HADDR
        STA     BAH
        LDA     NUM
        STA     NCYCLE
        LDA     #08             ;Configure synch. pulse - bit 4 of B.
        STA     $A000
        LDA     #FF             ;Output pulse to port A.
        STA     $A001
        NOP                     ;Synch. pulse duration 10 usecs.
        NOP
        NOP
        NOP
        NOP
        NOP
        LDA     #00             ;End synch. pulse.
        STA     A001
```

```
DATOUT;
        LDX     #03             ;Set 'X' as no. of output channels.
        LDY     #00             ;Reset address offset.
LOOP;
        DEX
        BPL     CONT            ;Branch if more channels to be output.
        RTI
CONT;
        LDA     OUTPUT,X        ;Select relevant output DAC.
        STA     DEVICE
        LDA     (BAL),Y         ;Select correct data byte.
        STA     OUT             ;Output byte.
        INC     BAL
        BNE     LOOP
        INC     BAH
        LDA     #$A0
        CMP     BAH             ;Skip address block A0 in memory.
        BNE     LOOP
        LDA     #$B0
        STA     BAH
        JMP     LOOP            ;Continue loop.

;*****************************************************************

;                               UTILITIES

        PRIFLG  =$A411          ;Define variables.
        CRCK    =$EA2d
        RBYTE   =$E3FD
        NUMA    =$EA46
        BLANK2  =$E83B
        DEBK1   =$ED2C
        BAL     =$01
        BAH     =$02
        NUM     =$03
        TEMP    =$04
        OUTDP   =$EEFC
        LL      =$E8FE
        REDOUT  =$E973
        PACK    =$EA84
        M1      =$0500
        M2      =$050F
        MSG     =$063F
        GETVAL  =$064E
        BCDBIN  =$0666
        NCYCLE  =$00
        PORTA   =$5801
        DDRA    =$5803
        PCR     =$580C
        ACR     =$580B
        DELAY   =$ED2C
```

D.VI Tape Reader Program Listing

TAPE READER

```
        *=$0112
        JMP     TREAD           ;Start 'TREAD' program if 'F3' key pressed.

        *=$0500
        M1                      ;Messages.
        .BYTE 'START ADDRESS,'
        M2
        .BYTE 'NO.OF CYCLES=,'
TREAD;
        LDA     #01
        STA     PRIFLG
        JSR     CRCK
        LDX     #M1-M1
        JSR     MSG
        JSR     RBYTE
        STA     BAH
        JSR     RBYTE
        STA     BAL
        LDY     #00
        JSR     CRCK
        LDX     #M2-M1
        JSR     GETVAL
        JSR     BCDBIN
        ASL     A
        STA     NCYCLE
        LDA     #00
        STA     DDRA
        STA     ACR
        LDA     #$C0
        LDY     #00
LOOP1;
        LDX     #200
LOOP2;
        LDA     #$E0
        STA     PCR
        LDA     #$C0
        STA     PCR
        JSR     DELAY
        JSR     DELAY
        LDA     PORTA
        STA     (BAL),Y
        INC     BAL
        BNE     STEST
        INC     BAH
STEST;
        DEX
        BNE     LOOP2
        DEC     NCYCLE
        BNE     LOOP1
        JMP     TREAD
```

```
DELAY;
        JSR     DEBK1           ;Delay loop used in 'TREAD'
        DEX
        BNE     DELAY
        JMP     LOOP
MSG;
        LDA     M1,X            ;Loop to output message no. 1.
        CMP     #','
        BEQ     EXIT
        JSR     OUTDP
        INX
        JMP     MSG
EXIT;
        RTS
GETVAL;
        JSR     MSG             ;Reads a 4-byte hex. value
        JSR     LL              ; -from keyboard.
        JSR     REDOUT
        JSR     PACK
        JSR     REDOUT
        JSR     PACK
        PHA
        JSR     CRCK
        PLA
        RTS
BCDBIN;
        PHA                     ;BCD to binary subroutine.
        AND     #$0F
        STA     TEMP
        LDX     #04
J1;
        PLA
        DEX
        BMI     ANSWER
        PHA
        AND     MASK,X
        BEQ     J1
        LDA     BINEQV,X
        CLC
        ADC     TEMP
        STA     TEMP
        JMP     J1
ANSWER;
        LDA     TEMP
        RTS
        MASK
        .BYTE $80,$40,$20,$10   ;BCD to binary masks.
        BINEQV
        .BYTE 80,40,20,10
        .END
```

APPENDIX E

SAFE START SEQUENCE FOR THE LABORATORY MODEL

Figure E1 gives a schematic of the complete laboratory model. The safe-start sequences to be followed for the protection of equipment and personnel was then:

(i) Ensure all switches and contactors open, GAIN and LEVEL adjust potentiometers set at zero, and VARIAC wound to zero secondary volts.

(ii) Start microprocessor cycling of stored data.

(iii) Close MAIN ISOLATOR.

(iv) Close SAFETY CONTACTOR.

(v) Increase GAIN adjust to maximum on power amplifiers.

(vi) Slowly increase VARIAC secondary voltage until $\Delta V = 0$.

(vii) Close SHORTING SWITCH.

(viii) Increase LEVEL adjust until line current is of correct value.

The procedure is reversed for stopping the model's operation. Rapid isolation of all equipment could be achieved by pressing the emergency stop button.

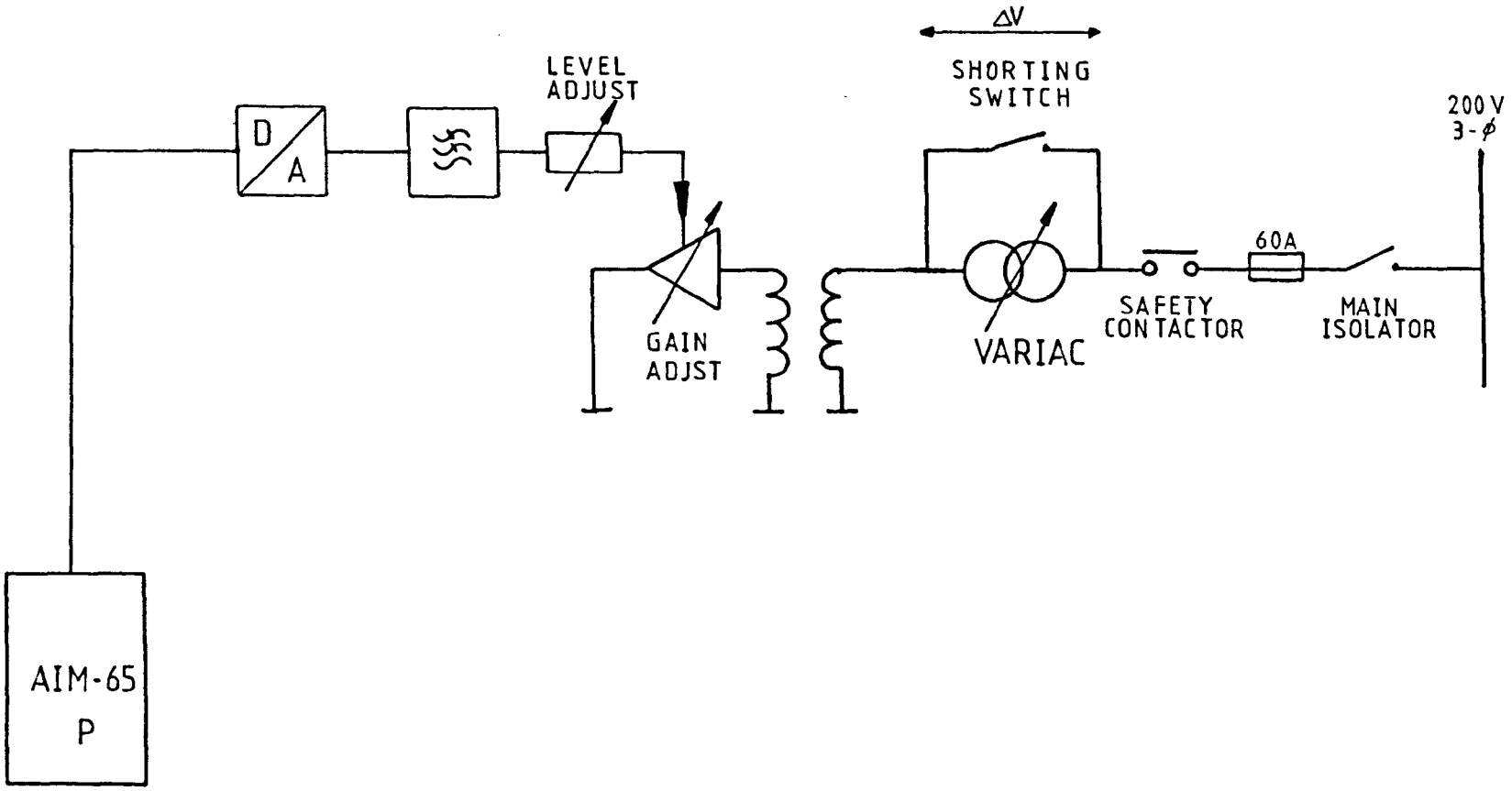

FIG. E1 : Laboratory model schematic

APPENDIX F

SIX-PULSE TCR CONTROL PROGRAM

F.I FireAsub.asm - Control Algorithm Compiler Listing

```
                                    NAME    thyristor_firing_routine
                                    NOLIST  CON

                                    GLOBAL  firAsub
                                    GLOBAL  CODEBASEQQ, DATABASEQQ, CONSTBASEQQ

                                    ASSUME DS:DATABASEQQ

                                    SECTION pascalprocedure, CLASS=INSTRQQ



                               ;XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
                               ;assembley routine to fire thyristors
                               ;called from main prog after voltage zero detected
                               ;algorithm subtracts sine value from measured value and integrates
                               ;testing value against a limit.Fires thy. when limit reached
                               ;
                               ;only outputs a short pulse for thyristor firing
                               ;
                               ;loop delay values set to values suitable for no1 compensator.Values
                               ;for the other two compensators must be set in RAM after download
                               ;
                               ;
                               ;positive half cycle
                               ;?
                               firAsub                       ;thyristor firing routine
00000000 8D360000 R            fire1   LEA SI, sine1         ;positive half cycle section
00000004 33DB                          XOR BX, BX
00000006 B509                          MOV CH, £09H
00000008 BA00F8                start1  MOV DX, £0F800H       ;load address of adc
0000000B EF                            OUT DX, AX            ;initiate conversion
0000000C B10F                          MOV CL, £0FH          ;conversion delay
0000000E D2E9                          SHR CL, CL
00000010 32E4                          XOR AH, AH            ;set ah to zero
00000012 EC                            IN AL, DX             ;input sample
00000013 B109                          MOV CL, £09H          ;loop delay to adjust sampling frequency
00000015 D2E9                          SHR CL, CL            ;sine curve based on 74 usecs sample time
00000017 80FD00                        CMP CH, £00H          ;test whether one of first nine samples
0000001A 7405                          JE tsta               ;jump to tsta if after nine samples
0000001C FECD                          DEC CH
0000001E E9                            JMP lab1
00000021 3C87                  tsta    CMP AL, £87H          ;test sample to check if near end of 1/2 cycle
00000023 72                            JB end1
00000025 8A0C                  lab1    MOV CL, [SI]          ;mov current value of sine curve from memory
00000027 3A                            CMP AL, CL            ;decide whether?sample < sine, jmp to neg1 - ?
00000029 7207                          JB neg1               ;-- if it is.
0000002B 2A                            SUB AL, CL            ;subtract sine from sample
0000002D 03D8                  add1    ADD BX, AX            ;add difference to summation store
0000002F E90C                          JMP con
00000032 2AC8                  neg1    SUB CL, AL            ;CL)AL , subtract AL from CL
00000034 8A                            MOV AL, CL            ;put difference into AL
```

```
                00006036 3BD8                   CMP BX,AX               ;test AX against BX--if AX)BX make AX=BX so
                0000003B 7702                   JA sub1                 ;that BX is set to zero in the subtraction
                0000003A 8BC3                   MOV AX,BX
                0000003C 2BD8           sub1    SUB BX,AX
                0000003E 81FE9A10       cont    CMP SI,£109AH           ;test SI for > 1/4 cycle
                00000042 7206                   JB  next                ;sample again if si < 1/4 cycle
                00000044 81FB0003               CMP BX,£0300H           ;test BX against limit
                00000048 7703                   JA firea                ;jump to firea when limit exeeded
                0000004A 46             next    INC SI                  ;update pointer to sine curve
                0000004B EBBB                   JMP start1
                0000004D BA00F0         firea   MOV DX,£0F000H          ;fire thyristor...one short pulse
                00000050 B001                   MOV AL,£01H
                00000052 EE                     OUT DX,AL
                00000053 B110                   MOV CL,£10H
                00000055 D2E9                   SHR CL,CL
                00000057 B000                   MOV AL,£00H
                00000059 EE                     OUT DX,AL
                0000005A BA00F8         end1    MOV DX,£0F800H          ;load adc address and input sample
                0000005D EF                     OUT DX,AX
                0000005E B10F                   MOV CL,£0FH
                00000060 D2E9                   SHR CL,CL
                00000062 EC                     IN AL,DX
                00000063 3C80                   CMP AL,£80H             ;check for zero crossing
                00000065 77F3                   JA end1
                00000067 8D368500 R     fire2   LEA SI,sine2    ;neg half cycle routine  Basically same as---
                0000006B 33DB                   XOR BX,BX               ;--positive half cycle routine except--
                0000006D B509                   MOV CH,£09H             ;--a positive contribution to summation--
                0000006F BA00F8         start2  MOV DX,£0F800H          ;--store results from AL being ----
                00000072 EF                     OUT DX,AX               ;--numerically smaller than sine curve--
                00000073 B10F                   MOV CL,£0FH             ;--to allow for fact that zero volts---
                00000075 D2E9                   SHR CL,CL               ;--corresponds to an adc output of 128.
                00000077 32E4                   XOR AH,AH
                00000079 EC                     IN AL,DX
                0000007A B108                   MOV CL,£08H             ;loop delay to adjust sampling freqency
                0000007C D2E9                   SHR CL,CL               ;sine curve based on 74usecs sample time
                0000007E 80FD00                 CMP CH,£00H
                00000081 7405                   JE test
                00000083 FECD                   DEC CH
                00000085 E90400                 JMP lab2
                00000088 3C73           test    CMP AL,£73H
                0000008A 7735                   JA end2
                0000008C 8A0C           lab2    MOV CL,[SI]
                0000008E 3AC1                   CMP AL,CL
                00000090 720D                   JB pos2
                00000092 2AC1                   SUB AL,CL
                00000094 3BD8                   CMP BX,AX
                00000096 7702                   JA sub2
                00000098 8BC3                   MOV AX,BX
                0000009A 2BD8           sub2    SUB BX,AX
                0000009C E90600                 JMP cont2
                0000009F 2AC8           pos2    SUB CL,AL
                000000A1 8AC1                   MOV AL,CL
```

```
105  000000A3 03D8          add2    ADD BX,AX
106  000000A5 81FE1F11      cont2   CMP SI,£111FH
107  000000A9 7206                  JB next2
108  000000AB 81FBC003              CMP BX,£003C0H
109  000000AF 7703                  JA fireb
110  000000B1 46            next2   INC SI
111  000000B2 EBBB                  JMP start2
112  000000B4 BA00F0        fireb   MOV DX,£0F000H          ;fire thyristor...one short pulse
113  000000B7 B002                  MOV AL,£02H
114  000000B9 EE                    OUT DX,AL
115  000000BA B110                  MOV CL,£10H
116  000000BC D2E9                  SHR CL,CL
117  000000BE B000                  MOV AL,£00H
118  000000C0 EE                    OUT DX,AL
119  000000C1 BA00F8        end2    MOV DX,£0F800H          ;load adc address and input sample
120  000000C4 EF                    OUT DX,AX
121  000000C5 B10F                  MOV CL,£0FH
122  000000C7 D2E9                  SHR CL,CL
123  000000C9 EC                    IN AL,DX
124  000000CA 3C80                  CMP AL,£80H             ;check for pos going zero crossing--
125  000000CC 72F3                  JB end2
126  000000CE E92FFF                JMP fire1               ;--cycle routine.
127  000000D1 C20400                RET £4
128
129
130
131
132                                 SECTION sdk88.const,CLASS=DATAQQ
133                                                         ; reference sine wave ...      zero = 127
134                                                         ;                          plus/minus  115
135                                                         ;                      first sample at 100us
136                                                         ;                      subsequent dt = 75us
137                                                         ;                   pt.s per 1/2 cyc = 132
138
139  00000000 8285888A      sine1           BYTE    130,133,136,138,141,143,146,148,151,154,156,159,161
                8D8F9294
                979A9C9F
                A1
149  0000000D A3A6A8AB              BYTE    163,166,168,171,173,175,178,180,182,184,187,189,191
                ADAFB2B4
                B6B8BBBD
                BF
41   0000001A C1C3C5C7              BYTE    193,195,197,199,201,203,205,207,208,210,212,213,215
                C9CBCDCF
                D0D2D4D5
                D7
42   00000027 D8DADBDD              BYTE    216,218,219,221,222,223,225,226,227,228,229,230,231
                DEDFE1E2
                E3E4E5E6
                E7
43   00000034 E8E8E9EA              BYTE    232,232,233,234,234,235,235,236,236,236,237,237,237
                EAEBEBEC
```

```
                        ECECEDED
                        ED
    144  00000041  EDEDEDED                        BYTE    237,237,237,237,237,236,236,236,235,235,234,234,233
                   EDECECEC
                   EBEBEAEA
                   E9
    145  0000004E  E8E7E6E6                        BYTE    232,231,230,230,229,228,227,225,224,223,222,220,219
                   E5E4E3E1
                   E0DFDEDC
                   DB
    146  0000005B  D9D8D6D5                        BYTE    217,216,214,213,211,210,208,206,204,202,200,198,196
                   D3D2D0CE
                   CCCAC8C6
                   C4
    147  00000068  C2C0BEBC                        BYTE    194,192,190,188,186,184,182,179,177,175,172,170,167
                   BAB8B6B3
                   B1AFACAA
                   A7
    148  00000075  A5A3A09E                        BYTE    165,163,160,158,155,153,150,148,145,142,140,137,135
                   9B999694
                   916E8C89
                   87
    149  00000082  84827F                          BYTE    132,130,127
    150
    151
    152  00000085  7C797674        sine2           BYTE    124,121,118,116,113,111,108,106,103,100,98,95,93,90
                   716F6C6A
                   6764625F
                   5D5A
    153  00000093  58565351                        BYTE    88,86,83,81,79,76,74,72,70,67,65,63,61
                   4F4C4A48
                   4643413F
                   3D
    154  000000A0  3B393735                        BYTE    59,57,55,53,51,49,47,46,44,42,41,39,38
                   33312F2E
                   2C2A2927
                   26
    155  000000AD  24232120                        BYTE    36,35,33,32,31,29,28,27,26,25,24,23,22
                   1F1D1C1B
                   1A191817
                   16
    156  000000BA  16151414                        BYTE    22,21,20,20,19,19,18,18,18,17,17,17,17
                   13131212
                   12111111
                   11
    157  000000C7  11111111                        BYTE    17,17,17,17,18,18,18,19,19,20,20,21,22
                   12121213
                   13141415
                   16
    158  000000D4  17181819                        BYTE    23,24,24,25,26,27,29,30,31,32,34,35,37
                   1A1B1D1E
                   1F202223
```

```
                    25
   159  000000E1 2628292B                BYTE    38,40,41,43,44,46,48,50,52,54,56,58,60
                 2C2E3032
                 3436383A
                 3C
   160  000000EE 3E404244                BYTE    62,64,66,68,70,72,75,77,79,82,84,87,89
                 46484B4D
                 4F525457
                 59
   161  000000FB 5B5E6063                BYTE    91,94,96,99,101,104,106,109,112,114,117,119,122
                 65686A6D
                 70727577
                 7A
   162  00000108 7C7F                    BYTE    124,127
   163
   164
   165
   166
   167                                   END
```

```
ASM       8086/8088 SYMBOL TABLE                                  Page    6
V01.18-38  (8560)                                        29-Sep-83 12:30:53

Section = SDK88.CONST, Class = DATAQQ, Aligned to 00000010, Size = 0000010A

SINE1-------------00000000     SINE2-------------00000085

Section = PASCALPROCEDURE, Class = INSTRQQ, Aligned to 00000010, Size = 000000D4

ADD1--------------0000002D     ADD2--------------000000A3     CONT--------------0000003E     CONT2-------------000000A5
END1--------------0000005A     END2--------------000000C1     FIRASUB-----------00000000 G   FIRE1-------------00000028
FIRE2-------------00000067     FIREA-------------0000004D     FIREB-------------000000B4     LAB1--------------00000025
LAB2--------------0000008C     NEG1--------------00000032     NEXT--------------0000004A     NEXT2-------------000000B1
POS2--------------0000009F     START1------------00000003     START2------------0000006F     SUB1--------------0000003C
SUB2--------------0000009A     TSTA--------------00000021     TSTB--------------00000088

Section = %FIREAOBJ, Aligned to 00000010, Size = EMPTY

Unbound Globals

CODEBASEQQ--------00000000     CONSTBASEQQ-------00000000     DATABASEQQ--------00000000

  167 Lines Read
  167 Lines Processed
    0 Errors
```

Sample No. dec.	Address hex.	V_R dec.	cont'd dec.	cont'd hex.	cont'd dec.	cont'd dec.	cont'd hex.	cont'd dec.	cont'd dec.	cont'd hex.	cont'd dec.
0	1058	130	35	107B	210	70	109E	236	105	10C1	192
1	1059	133	36	107C	212	71	109F	236	106	10C2	190
2	105A	136	37	107D	213	72	10A0	236	107	10C3	188
3	105B	138	38	107E	215	73	10A1	235	108	10C4	186
4	105C	141	39	107F	216	74	10A2	235	109	10C5	184
5	105D	143	40	1080	218	75	10A3	234	110	10C6	182
6	105E	146	41	1081	219	76	10A4	234	111	10C7	179
7	105F	148	42	1082	221	77	10A5	232	112	10C8	177
8	1060	151	43	1083	222	78	10A6	232	113	10C9	175
9	1061	154	44	1084	223	79	10A7	231	114	10CA	172
10	1062	156	45	1085	225	80	10A8	230	115	10CB	170
11	1063	159	46	1086	226	81	10A9	230	116	10CC	167
12	1064	161	47	1087	227	82	10AA	229	117	10CD	165
13	1065	163	48	1088	228	83	10AB	228	118	10CE	163
14	1066	166	49	1089	229	84	10AC	227	119	10CF	160
15	1067	168	50	108A	230	85	10AD	225	120	10D0	158
16	1068	171	51	108B	231	86	10AE	224	121	10D1	155
17	1069	173	52	108C	232	87	10AF	223	122	10D2	153
18	106A	175	53	108D	232	88	10B0	222	123	10D3	140
19	106B	178	54	108E	233	89	10B1	220	124	10D4	148
20	106C	180	55	108F	234	90	10B2	219	125	10D5	145
21	106D	182	56	1090	234	91	10B3	217	126	10D6	142
22	106E	184	57	1091	235	92	10B4	216	127	10D7	130
23	106F	187	58	1092	235	93	10B5	214	128	10D8	137
24	1070	189	59	1093	236	94	10B6	213	129	10D9	135
25	1071	191	60	1094	236	95	10B7	211	130	10DA	132
26	1072	193	61	1095	236	96	10B8	210	131	10DB	130
27	1073	195	62	1096	237	97	10B9	208	132	10DC	127
28	1074	197	63	1097	237	98	10BA	206			
29	1075	199	64	1098	237	99	10BB	204			
30	1076	201	65	1099	237	100	10BC	202			
31	1077	203	66	109A	237	101	10BD	200			
32	1078	205	67	109B	237	102	10BE	198			
33	1079	207	68	109C	237	103	10BF	196			
34	107A	208	69	109D	237	104	10C0	194			

F.II SINE1: Positive half-cycle reference sinusoid

Sample No. dec.	Address hex.	V_R dec.	cont'd dec.	cont'd hex.	cont'd dec.	cont'd dec.	cont'd hex.	cont'd dec.	cont'd dec.	cont'd hex.	cont'd dec.
0	10DD	124	35	1110	44	70	1133	18	105	1156	62
1	10DE	121	36	1111	42	71	1134	236	106	1157	64
2	10DF	118	37	1112	41	72	1135	236	107	1158	66
3	10E0	116	38	1113	39	73	1136	235	108	1159	68
4	10E1	113	39	1114	38	74	1137	235	109	115A	70
5	10E2	111	40	1115	36	75	1138	234	110	115B	72
6	10E3	108	41	1116	35	76	1139	234	111	115C	75
7	10E4	106	42	1117	33	77	113A	232	112	115D	77
8	10E5	103	43	1118	32	78	113B	232	113	115E	79
9	10E6	100	44	1119	31	79	113C	231	114	115F	82
10	10E7	98	45	111A	29	80	113D	230	115	1160	84
11	10E8	95	46	111B	28	81	113E	230	116	1161	87
12	10E9	93	47	111C	27	82	113F	229	117	1162	89
13	10EA	90	48	111D	26	83	1140	228	118	1163	91
14	10EB	88	49	111E	25	84	1141	227	119	1164	94
15	10EC	86	50	111F	24	85	1142	225	120	1165	96
16	10ED	83	51	1120	23	86	1143	224	121	1166	99
17	10EE	81	52	1121	22	87	1144	223	122	1167	101
18	10EF	79	53	1122	22	88	1145	222	123	1168	104
19	1100	76	54	1123	21	89	1146	220	124	1169	106
20	1101	74	55	1124	20	90	1147	219	125	116A	109
21	1102	72	56	1125	20	91	1148	217	126	116B	112
22	1103	70	57	1126	19	92	1149	216	127	116C	114
23	1104	67	58	1127	19	93	114A	214	128	116D	117
24	1105	65	59	1128	18	94	114B	213	129	116E	122
25	1106	63	60	1129	18	95	114C	211	130	116F	124
26	1107	61	61	112A	18	96	114D	210	131	1170	130
27	1108	59	62	112B	17	97	114E	208	132	1171	127
28	1109	57	63	112C	17	98	114F	206			
29	110A	55	64	112D	17	99	1150	204			
30	110B	53	65	112E	17	100	1151	202			
31	110C	51	66	112F	17	101	1152	200			
32	110D	49	67	1130	17	102	1153	198			
33	110E	47	68	1131	17	103	1154	196			
34	110F	46	69	1132	17	104	1155	194			

F.III SINE2: Negative half-cycle reference sinusoid

APPENDIX G

SPECAN.FORTRAN - A SPECTRUM ANALYSIS PACKAGE
PROGRAM LISTING

G.I Spectral Analysis Program Overview

The main SPECAN program is used for handling and manipulation of data to enable it to be used as a general program suited to input data with varying characteristics.

The number of time-series data samples was required to be 2^N, and an equivalent number of frequency blocks were returned from the FFT subroutine 'FRXFM' within the range 0 - F_sHz, where $F_s = 1/\Delta t$, the sampling frequency. Only the lower half of this frequency domain data could be used - that below the Nyquist frequency $F_N = 1/2\Delta t$.

The frequency range of power spectral density that could be studied was therefore simply a function of the input data sampling frequency F_s.

Δt for most of the data studied was fixed at 800 microseconds, giving $F_N = F_s/2 = 625$Hz.

The resolution into frequency blocks within this range was then a function of the total number of time series samples input to the program.

Table G1 shows how the output frequency range and resolution vary with input time series data sampling frequency F_s, and total number of samples 2^N.

2048 samples were always used, giving N = 11 and a resolution of 0.6Hz per block in the output frequency range to 625Hz.

Figure G1 shows how the main 'SPECAN' program utilised a run-time library of compiled subroutines 'FRXFM', 'BLOCK' and 'HAN'.

'BLOCK' rearranges the frequency components output from 'FRXFM' into their correct consecutive sequence.

	Hertz		
Sampling Frequency F_s	2500	1250	625
frequency span resulting	0 - 1250	0 - 625	0 - 312
Number of samples N_s			
1024	2.44	1.22	0.61
2048	1.22	0.61	0.31
4096	0.61	0.31	0.15
	Resolution bandwidth		

TABLE G1 : FFT output frequency range and resolution.

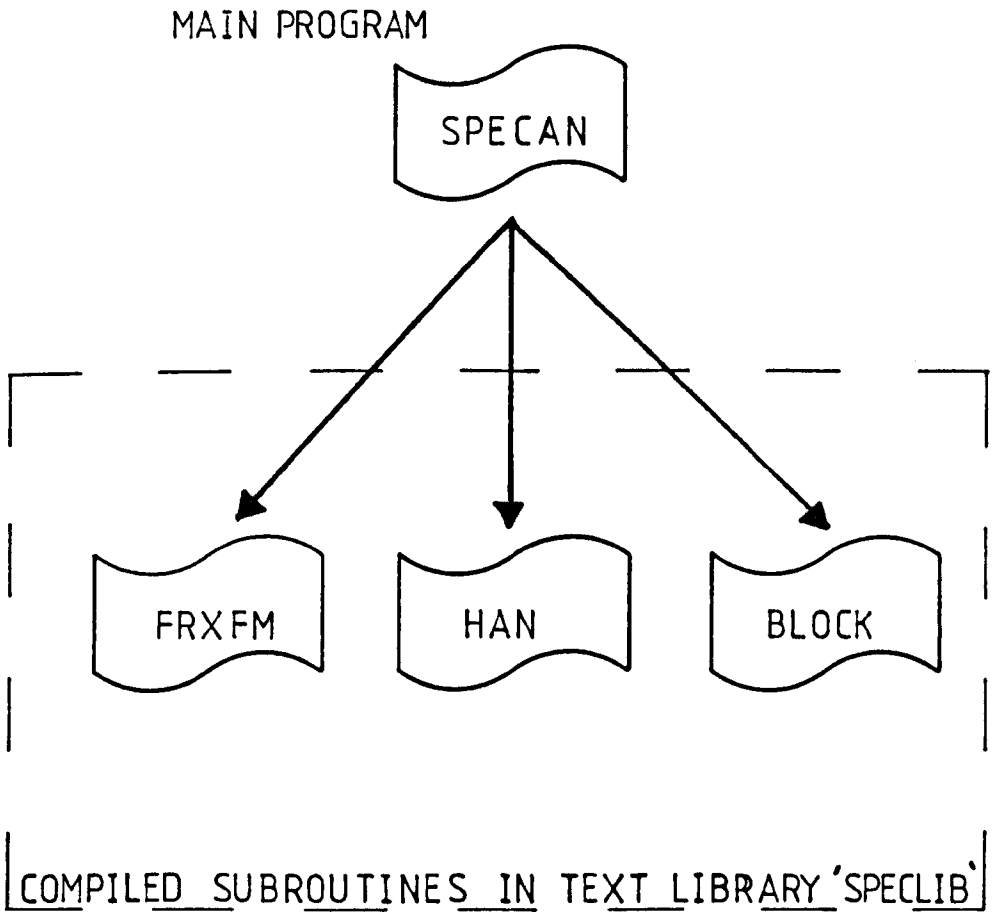

FIG. G1 : SPECTRUM ANALYSIS
PROGRAM STRUCTURE

'HAN' introduces a Hanning smoothing window which takes the form of a cosine 'half-bell' at each end of the data span. This reduces errors over the whole frequency span which may be caused by end-effects from the start and end of the time-series data.

The FORTRAN program listings for SPECAN, FRXFM, BLOCK and HAN are given in Sections G.II, G.III, G.IV and G.V respectively.

G.II 'SPECAN' Program Listing

```
      DIMENSION V(2048),T(2048),X(2048),Y(2048),XV(2048),YV(2048),      SPE00010
     + XHZ(20),YHZ(20),XDB(20),YDB(20),TITLE(8)                         SPE00020
      INTEGER I,J,K,K1,K2,LINES,IDB,NBLK,NBLK50,NBLKH,ENDBLK            SPE00030
      LOGICAL LIST,HANFIL                                               SPE00040
C     READ(5,100) N2TOT,N2SAM,NBLK,ITST,IDYN,IHAN,IPRINT,ISQ,IWAVE      SPE00050
C     WRITE(6,100) N2TOT,N2SAM,NBLK,ITST,IDYN,IHAN,IPRINT,ISQ,IWAVE     SPE00060
C                                                                       SPE00070
C.................THIS SPEC50 PROGRAM IS A MODIFICATION OF THE GENERAL  SPE00080
C                 SPECAN PROGRAM FOR SPECTRAL ANALYSIS.                 SPE00090
C                                                                       SPE00100
C                 THE MODIFICATIONS ONLY ALLOW ONE 'SEGMENT' TO BE      SPE00110
C                 PLOTTED FROM THE INPUT DATA.                          SPE00120
C                      THUS:                                            SPE00130
C                           'ITST' MUST BE 1 (TEST SEGMENT IS THE FIRST)SPE00140
C                           'ISQ'  NEED ONLY BE 1                       SPE00150
C                           'N2SAM'='N2TOT' (SAMPLES PER SEGMENT        SPE00160
C                                          = TOTAL NO. OF SAMPLES)      SPE00170
C                      ALSO:                                            SPE00180
C                           'NTOT' MUST BE 2048 DATA POINTS HERE        SPE00190
C                           'NBLK' IS SET SO THAT ALL SPECTRAL LINES ARESPE00200
C                                  CALCULATED - NO AVERAGING OCCURS     SPE00210
C                           'IDYN' IS SET TO 90 BECAUSE THIS APPLICATIONSPE00220
C                                  REQUIRES DETAILS DOWN TO -80DB       SPE00230
C                                                                       SPE00240
C                 THERE IS NO LONGER ANY FACILITY FOR PLOTTING THE      SPE00250
C                 INPUT TIME-SERIES DATA.                               SPE00260
C                                                                       SPE00270
      IDYN=90                                                           SPE00280
      N2TOT=11                                                          SPE00290
      N2SAM=11                                                          SPE00300
      NBLK=(2.0**N2SAM)/2.0                                             SPE00310
      ITST=1                                                            SPE00320
      ISQ=1                                                             SPE00330
      HANFIL=.TRUE.                                                     SPE00340
C                                                                       SPE00350
C.................THE RANGE OF FREQUENCY TO BE PRESENTED IS DEFINED    SPE00360
C                  BY SETTING THE NO. OF BLOCKS TO BE PLOTTED,          SPE00370
C                  REMEMBERING THAT (NO. OF SAMPLES X 0.5) WILL GIVE    SPE00380
C                  UP TO THE NYQUIST FREQUENCY.                         SPE00390
C                                                                       SPE00400
C                  THUS FOR 2048 SAMPLES AT 800US SAMPLING INTERVAL...  SPE00410
C                                82 BLOCKS GIVES 0 - 50 HZ              SPE00420
C                               983 BLOCKS GIVES 0 - 600 HZ.            SPE00430
C                                                                       SPE00440
C                                                                       SPE00450
      NBLK50=82                                                         SPE00460
      NBLKC=165                                                         SPE00470
      NBLKH=983                                                         SPE00480
      IDYN=IDYN-10                                                      SPE00490
      NTOT=2**N2TOT                                                     SPE00500
      NSAM=2**N2SAM                                                     SPE00510
      NSAM2=NSAM/2                                                      SPE00520
      FSAMSQ=FLOAT(NSAM)*FLOAT(NSAM)                                    SPE00530
      NSEG=NTOT/NSAM2 - 1                                               SPE00540
      NLPB=NSAM2/NBLK                                                   SPE00550
C                                                                       SPE00560
C.................READ ALPHANUMERIC DATA AT HEAD OF DATA FILE          SPE00570
C                                                                       SPE00580
      READ(5,111) TITLE                                                 SPE00590
C                                                                       SPE00600
C.................READ THE INPUT DATA AND ATTACH TO EACH POINT AN      SPE00610
C                  ARBITRARY TIME VALUE                                 SPE00620
C                                                                       SPE00630
      LINES=NTOT/8                                                      SPE00640
      IF(LIST)WRITE(6,104)                                              SPE00650
      DO 2 J=1,LINES                                                    SPE00660
            K1=J*8-7                                                    SPE00670
            K2=J*8                                                      SPE00680
            READ(5,102)(V(K),K=K1,K2,1)                                 SPE00690
            DO 1 K=K1,K2,1                                              SPE00700
                  T(K)=FLOAT(K)                                         SPE00710
                  IF(LIST) WRITE(6,105) K,T(K),V(K)                     SPE00720
    1       CONTINUE                                                    SPE00730
            IF(LIST) WRITE(6,110)                                       SPE00740
            IF(LIST) WRITE(6,102) (V(K),K=K1,K2,1)                      SPE00750
    2 CONTINUE                                                          SPE00760
C                                                                       SPE00770
C.................DRY RUN TO ESTIMATE MAX POWER                        SPE00780
C                                                                       SPE00790
      I1=(ITST-1)*NSAM2 + 1                                             SPE00800
      I2=(ITST+1)*NSAM2                                                 SPE00810
      DO 5 I=I1,I2                                                      SPE00820
            K=I-I1+1                                                    SPE00830
            X(K)=V(I)                                                   SPE00840
            Y(K)=0.0                                                    SPE00850
```

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    5 CONTINUE                                                          SPE00860
      CALL FRXFM(N2SAM,NSAM,X,Y)                                        SPE00870
      IF(.NOT.HANFIL) GO TO 6                                           SPE00880
      CALL HAN(NSAM,X,Y)                                                SPE00890
      SCALE=16.0/(3.0*FSAMSQ)                                           SPE00900
      GO TO 7                                                           SPE00910
    6 SCALE=2.0/FSAMSQ                                                  SPE00920
    7 X(1)=0.0                                                          SPE00930
      DO 8 I=2,NSAM2                                                    SPE00940
    8 X(I)=SCALE*(X(I)*X(I) + Y(I)*Y(I))                                SPE00950
      CALL BLOCK(X,Y,NSAM2,NBLK)                                        SPE00960
      XMX=X(1)                                                          SPE00970
      DO 9 I=2,NBLK                                                     SPE00980
    9 IF(X(I).GT.XMX) XMX=X(I)                                          SPE00990
C                                                                       SPE01000
C.................COMPUTE AND PLOT  SPECTRA                            SPE01010
C                                                                       SPE01020
C                                                                       SPE01030
C.................J IS INVARIENT BECAUSE THERE IS ONLY ONE SEGMENT     SPE01040
C                                                                       SPE01050
      J=1                                                               SPE01060
      I1=(J-1)*NSAM2+1                                                  SPE01070
      I2=(J+1)*NSAM2                                                    SPE01080
      DO 12 I=I1,I2                                                     SPE01090
      K=I-I1+1                                                          SPE01100
      X(K)=V(I)                                                         SPE01110
   12 Y(K)=0.0                                                          SPE01120
      CALL FRXFM(N2SAM,NSAM,X,Y)                                        SPE01130
      IF(LIST) WRITE(6,106)                                             SPE01140
      IF(LIST) WRITE(6,101) (I,X(I),Y(I),I=1,NSAM)                      SPE01150
      IF(.NOT.HANFIL) GO TO 13                                          SPE01160
      CALL HAN(NSAM,X,Y)                                                SPE01170
      IF(LIST) WRITE(6,107)                                             SPE01180
      IF(LIST) WRITE(6,101) (I,X(I),Y(I),I=1,NSAM)                      SPE01190
      IF(LIST) WRITE(6,109)                                             SPE01200
      SCALE=16.0/(3.0*FSAMSQ)                                           SPE01210
      GO TO 14                                                          SPE01220
   13 SCALE=2.0/FSAMSQ                                                  SPE01230
   14 X(1)=0.0                                                          SPE01240
      DO 16 I=2,NSAM2                                                   SPE01250
   16 X(I)=SCALE*(X(I)*X(I) + Y(I)*Y(I))                                SPE01260
      CALL BLOCK(X,Y,NSAM2,NBLK)                                        SPE01270
      IF(LIST) WRITE(6,108)                                             SPE01280
      IF(LIST)  WRITE(6,101)(I,X(I),Y(I), I=1,NBLK)                     SPE01290
C                                                                       SPE01300
C.................PLOTTING OF SPECTRUM FOLLOWS                         SPE01310
C                  XV,YV AT 34 CARRY OVERFLOW MARKERS                   SPE01320
C                                                                       SPE01330
   17 CONTINUE                                                          SPE01340
      ENDBLK=NBLKC                                                      SPE01350
      CALL PAPER(1)                                                     SPE01360
   18 CALL PSPACE(0.2,0.56,0.3,0.9)                                     SPE01370
      CALL CSPACE(0.0,0.0,0.0,0.0)                                      SPE01380
      ENDYM=0.5*(FLOAT(ENDBLK)/1024.0)                                  SPE01390
      WRITE(2,*) ENDBLK,ENDYM                                           SPE01400
      CALL MAP(-80.0,10.0,ENDYM,0.0)                                    SPE01410
      CALL CTRFNT(1)                                                    SPE01420
      CALL CTRMAG(10)                                                   SPE01430
C                                                                       SPE01440
C                                                                       SPE01450
C          THE FOLLOWING PRAMETERS SET THE MATHEMATICAL  SPACE FOR THE  SPE01460
C          POWER SPECTRUM PLOT.                                         SPE01470
C                                                                       SPE01480
C          YSM DICTATES THE RANGE OF NORMALISED FREQUENCY PLOTTED--ITS  SPE01490
C          MAXIMUM ALLOWABLE VALUE IS 0.5.   (NYQUIST LIMIT)            SPE01500
C                                                                       SPE01510
C                                                                       SPE01520
      XSM1=-FLOAT(80)                                                   SPE01530
      XSM2=10.0                                                         SPE01540
C     YSM1=0.5                                                          SPE01550
C     YSM1=0.5*(NBLK50/1024.0)                                          SPE01560
      YSM2=0.0                                                          SPE01570
      DEL=Y(2)-Y(1)                                                     SPE01580
      CALL POSITN(XSM1,0.0)                                             SPE01590
      MARK=0                                                            SPE01600
      XP=XSM1                                                           SPE01610
      IF(X(1).EQ.0.0) GO TO 19                                          SPE01620
      XP=10.0*ALOG10(X(1)/XMX)                                          SPE01630
   19 YP=0.0                                                            SPE01640
      IF(XP.LT.XSM2) GO TO 20                                           SPE01650
      MARK=MARK+1                                                       SPE01660
      XP=XSM2                                                           SPE01670
      YV(1)=Y(1)                                                        SPE01680
      XV(1)=XP                                                          SPE01690
      GO TO 22                                                          SPE01700
   20 IF(XP.GT.XSM1) GO TO 22                                           SPE01710
```

```
      MARK=MARK+1                                                       SPE01720
      XP=XSM1                                                           SPE01730
      YV(1)=Y(1)                                                        SPE01740
      XV(1)=XP                                                          SPE01750
   22 CALL JOIN(XP,YP)                                                  SPE01760
      YP=Y(1)+DEL/2.0                                                   SPE01770
      CALL JOIN(XP,YP)                                                  SPE01780
C                                                                       SPE01790
C           THE LOOP TO 30 PLOTS THE BLOCKS IN THE F-DOMAIN AFTER  THE  SPE01800
C           FIRST BLOCK.                                                SPE01810
C                                                                       SPE01820
C           USUALLY THE UPPER LIMIT WOULD BE SIMPLY NBLK--BUT FOR THIS  SPE01830
C           SPEC50 PROGRAM IT IS NBLKC  AS SET ABOVE.                   SPE01840
C                                                                       SPE01850
      DO 30 I=2,ENDBLK                                                  SPE01860
      IF(X(I).GT.0.0) GO TO 23                                          SPE01870
      XP=XSM1                                                           SPE01880
      GO TO 26                                                          SPE01890
   23 XP=10.0*ALOG10(X(I)/XMX)                                          SPE01900
      IF(XP.LT.XSM2) GO TO 24                                           SPE01910
      MARK=MARK+1                                                       SPE01920
      XP=XSM2                                                           SPE01930
      XV(MARK)=XP                                                       SPE01940
      YV(MARK)=Y(I)                                                     SPE01950
      GO TO 26                                                          SPE01960
   24 IF(XP.GT.XSM1) GO TO 26                                           SPE01970
      MARK=MARK+1                                                       SPE01980
      XP=XSM1                                                           SPE01990
      XV(MARK)=XP                                                       SPE02000
      YV(MARK)=Y(I)                                                     SPE02010
C  26 IF(MARK.GT.499) GO TO 34                                          SPE02020
   26 CONTINUE                                                          SPE02030
      IF(LIST) WRITE(6,103)XP,YP                                        SPE02040
      CALL JOIN(XP,YP)                                                  SPE02050
      YP=YP+DEL                                                         SPE02060
   30 CALL JOIN(XP,YP)                                                  SPE02070
      XP=XSM1                                                           SPE02080
      CALL JOIN(XP,YP)                                                  SPE02090
      IF(MARK.EQ.0) GO TO 40                                            SPE02100
C                                                                       SPE02110
C.............PLOT STARS WHERE XP IS 'OUT OF RANGE'                     SPE02120
C                                                                       SPE02130
   34 CALL PTPLOT(XV,YV,1,MARK,45)                                      SPE02140
   40 CONTINUE                                                          SPE02150
C                                                                       SPE02160
C              FOLLOWING SECTION LABELS AXES OF SPECTRUM PLOT           SPE02170
C              (ONLY IF J=1)                                            SPE02180
C                                                                       SPE02190
C                                                                       SPE02200
      IF(J.GT.1) GO TO 50                                               SPE02210
      CALL AXNOTA(0)                                                    SPE02220
      CALL XAXIS                                                        SPE02230
      DBMIN=-(IDYN)                                                     SPE02240
      DO 41 I=1,10,1                                                    SPE02250
          YHZ(I)=FLOAT(I)*(ENDYM/10.0)                                  SPE02260
          XHZ(I)=DBMIN                                                  SPE02270
   41 CONTINUE                                                          SPE02280
      IDB=IDYN/10+1                                                     SPE02290
      DO 42 I=1,IDB,1                                                   SPE02300
          XDB(I)=10.0-(I*10.0)                                          SPE02310
          YDB(I)=0.0                                                    SPE02320
   42 CONTINUE                                                          SPE02330
      CALL CTRMAG(20)                                                   SPE02340
      CALL PTPLOT(XHZ,YHZ,1,10,43)                                      SPE02350
      CALL PTPLOT(XDB,YDB,1,IDB,43)                                     SPE02360
      CALL POSITN(DBMIN,0.0)                                            SPE02370
      CALL JOIN(10.0,0.0)                                               SPE02380
      CALL POSITN(DBMIN,0.0)                                            SPE02390
      CALL JOIN(DBMIN,ENDYM)                                            SPE02400
      CALL CTRORI(270.0)                                                SPE02410
      CALL PSPACE(0.0,1.0,0.0,1.0)                                      SPE02420
      CALL CSPACE(0.0,0.0,0.0,0.0)                                      SPE02430
      CALL MAP(0.0,1.0,0.0,1.0)                                         SPE02440
      CALL CTRMAG(8)                                                    SPE02450
      CALL CTRORI(270.0)                                                SPE02460
      XCH=0.18                                                          SPE02470
      YCH=0.91                                                          SPE02480
      CALL PLOTCS(XCH,YCH,91H0.0     10.0     20.0     30.0     40.0    SPE02490
     +50.0     60.0     70.0     80.0     90.0    100.0,91)             SPE02500
      XCH=XCH-0.03                                                      SPE02510
      YCH=YCH-0.08                                                      SPE02520
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      CALL CTRMAG(10)                                                    SPE02530
      CALL PLOTCS(XCH,YCH,36H                    FREQUENCY ( HZ ),36)    SPE02540
      CALL PLOTCS(0.54,0.95,2HDB,2)                                      SPE02550
      CALL CTRMAG(10)                                                    SPE02560
      CALL PLOTCS(0.98,0.95,TITLE,64)                                    SPE02570
      CALL CTRMAG(20)                                                    SPE02580
      CALL PLOTCS(0.65,0.70,13HPOWER SPECTRA,13)                         SPE02590
      CALL CTRMAG(8)                                                     SPE02600
      CALL PLOTCS(0.560,0.95,5H 10.0,5)                                  SPE02610
      CALL PLOTCS(0.520,0.95,5H  0.0,5)                                  SPE02620
      CALL PLOTCS(0.480,0.95,5H-10.0,5)                                  SPE02630
      CALL PLOTCS(0.440,0.95,5H-20.0,5)                                  SPE02640
      CALL PLOTCS(0.400,0.95,5H-30.0,5)                                  SPE02650
      CALL PLOTCS(0.360,0.95,5H-40.0,5)                                  SPE02660
      CALL PLOTCS(0.320,0.95,5H-50.0,5)                                  SPE02670
      CALL PLOTCS(0.280,0.95,5H-60.0,5)                                  SPE02680
      CALL PLOTCS(0.240,0.95,5H-70.0,5)                                  SPE02690
      CALL PLOTCS(0.200,0.95,5H-80.0,5)                                  SPE02700
      CALL CTRORI(0.0)                                                   SPE02710
      CALL CTRMAG(10)                                                    SPE02720
   50 CONTINUE                                                           SPE02730
      CALL GREND                                                         SPE02740
C                                                                        SPE02750
C                                                                        SPE02760
C.................SECOND PLOTTING SECTION (BELOW) OUTPUTS 0 - 600HZ      SPE02770
C                 FOR HARMONIC ANALYSIS.                                 SPE02780
C                                                                        SPE02790
C                                                                        SPE02800
      ENDBLK=NBLKH                                                       SPE02810
      CALL PAPER(1)                                                      SPE02820
   68 CALL PSPACE(0.2,0.56,0.3,0.9)                                      SPE02830
      CALL CSPACE(0.0,0.0,0.0,0.0)                                       SPE02840
      ENDYM=0.5*(FLOAT(ENDBLK)/1024.0)                                   SPE02850
      WRITE(2,*) ENDBLK,ENDYM                                            SPE02860
      CALL MAP(-80.0,10.0,ENDYM,0.0)                                     SPE02870
      CALL CTRFNT(1)                                                     SPE02880
      CALL CTRMAG(10)                                                    SPE02890
C                                                                        SPE02900
C                                                                        SPE02910
C          THE FOLLOWING PRAMETERS SET THE MATHEMATICAL  SPACE FOR THE   SPE02920
C          POWER SPECTRUM PLOT.                                          SPE02930
C                                                                        SPE02940
C          YSM DICTATES THE RANGE OF NORMALISED FREQUENCY PLOTTED--ITS   SPE02950
C          MAXIMUM ALLOWABLE VALUE IS 0.5.   (NYQUIST LIMIT)             SPE02960
C                                                                        SPE02970
C                                                                        SPE02980
      XSM1=-FLOAT(80)                                                    SPE02990
      XSM2=10.0                                                          SPE03000
C     YSM1=0.5                                                           SPE03010
C     YSM1=0.5*(NBLK50/1024.0)                                           SPE03020
      YSM2=0.0                                                           SPE03030
      DEL=Y(2)-Y(1)                                                      SPE03040
      CALL POSITN(XSM1,0.0)                                              SPE03050
      MARK=0                                                             SPE03060
      XP=XSM1                                                            SPE03070
      IF(X(1).EQ.0.0) GO TO 69                                           SPE03080
      XP=10.0*ALOG10(X(1)/XMX)                                           SPE03090
   69 YP=0.0                                                             SPE03100
      IF(XP.LT.XSM2) GO TO 70                                            SPE03110
      MARK=MARK+1                                                        SPE03120
      XP=XSM2                                                            SPE03130
      YV(1)=Y(1)                                                         SPE03140
      XV(1)=XP                                                           SPE03150
      GO TO 72                                                           SPE03160
   70 IF(XP.GT.XSM1) GO TO 72                                            SPE03170
      MARK=MARK+1                                                        SPE03180
      XP=XSM1                                                            SPE03190
      YV(1)=Y(1)                                                         SPE03200
      XV(1)=XP                                                           SPE03210
   72 CALL JOIN(XP,YP)                                                   SPE03220
      YP=Y(1)+DEL/2.0                                                    SPE03230
      CALL JOIN(XP,YP)                                                   SPE03240
C                                                                        SPE03250
C          THE LOOP TO 80 PLOTS THE BLOCKS IN THE F-DOMAIN AFTER  THE    SPE03260
C          FIRST BLOCK.                                                  SPE03270
C                                                                        SPE03280
C          USUALLY THE UPPER LIMIT WOULD BE SIMPLY NBLK--BUT FOR THIS    SPE03290
C          PLOT IT IS NBLKH AS SET ABOVE.                                SPE03300
C                                                                        SPE03310
      DO 80 I=2,ENDBLK                                                   SPE03320
      IF(X(I).GT.0.0) GO TO 73                                           SPE03330
      XP=XSM1                                                            SPE03340
      GO TO 76                                                           SPE03350
   73 XP=10.0*ALOG10(X(I)/XMX)                                           SPE03360
      IF(XP.LT.XSM2) GO TO 74                                            SPE03370
      MARK=MARK+1                                                        SPE03380
      XP=XSM2                                                            SPE03390
      XV(MARK)=XP                                                        SPE03400
      YV(MARK)=Y(I)                                                      SPE03410
      GO TO 76                                                           SPE03420
   74 IF(XP.GT.XSM1) GO TO 76                                            SPE03430
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      MARK=MARK+1                                                       SPE03440
      XP=XSM1                                                           SPE03450
      XV(MARK)=XP                                                       SPE03460
      YV(MARK)=Y(I)                                                     SPE03470
C  76 IF(MARK.GT.499) GO TO 84                                          SPE03480
   76 CONTINUE                                                          SPE03490
      IF(LIST) WRITE(6,103)XP,YP                                        SPE03500
      CALL JOIN(XP,YP)                                                  SPE03510
      YP=YP+DEL                                                         SPE03520
   80 CALL JOIN(XP,YP)                                                  SPE03530
      XP=XSM1                                                           SPE03540
      CALL JOIN(XP,YP)                                                  SPE03550
      IF(MARK.EQ.0) GO TO 90                                            SPE03560
C                                                                       SPE03570
C.............PLOT STARS WHERE XP IS 'OUT OF RANGE'                     SPE03580
C                                                                       SPE03590
   84 CALL PTPLOT(XV,YV,1,MARK,45)                                      SPE03600
   90 CONTINUE                                                          SPE03610
C                                                                       SPE03620
C              FOLLOWING SECTION LABELS AXES OF SPECTRUM PLOT           SPE03630
C              (ONLY IF J=1)                                            SPE03640
C                                                                       SPE03650
C                                                                       SPE03660
      IF(J.GT.1) GO TO 99                                               SPE03670
      CALL AXNOTA(0)                                                    SPE03680
      CALL XAXIS                                                        SPE03690
      DBMIN=-(IDYN)                                                     SPE03700
      DO 91 I=1,12,1                                                    SPE03710
          YHZ(I)=FLOAT(I)*(ENDYM/12.0)                                  SPE03720
          XHZ(I)=DBMIN                                                  SPE03730
   91 CONTINUE                                                          SPE03740
      IDB=IDYN/10+1                                                     SPE03750
      DO 92 I=1,IDB,1                                                   SPE03760
          XDB(I)=10.0-(I*10.0)                                          SPE03770
          YDB(I)=0.0                                                    SPE03780
   92 CONTINUE                                                          SPE03790
      CALL CTRMAG(20)                                                   SPE03800
      CALL PTPLOT(XHZ,YHZ,1,10,43)                                      SPE03810
      CALL PTPLOT(XDB,YDB,1,IDB,43)                                     SPE03820
      CALL POSITN(DBMIN,0.0)                                            SPE03830
      CALL JOIN(10.0,0.0)                                               SPE03840
      CALL POSITN(DBMIN,0.0)                                            SPE03850
      CALL JOIN(DBMIN,ENDYM)                                            SPE03860
      CALL CTRORI(270.0)                                                SPE03870
      CALL PSPACE(0.0,1.0,0.0,1.0)                                      SPE03880
      CALL CSPACE(0.0,0.0,0.0,0.0)                                      SPE03890
      CALL MAP(0.0,1.0,0.0,1.0)                                         SPE03900
      CALL CTRMAG(8)                                                    SPE03910
      CALL CTRORI(270.0)                                                SPE03920
      XCH=0.18                                                          SPE03930
      YCH=0.91                                                          SPE03940
      CALL PLOTCS(XCH,YCH,91H 0              100             200        SPE03950
     + 300           400           500            600 ,91)              SPE03960
      XCH=XCH-0.03                                                      SPE03970
      YCH=YCH-0.08                                                      SPE03980
      CALL CTRMAG(10)                                                   SPE03990
      CALL PLOTCS(XCH,YCH,36H                    FREQUENCY ( HZ ),36)   SPE04000
      CALL PLOTCS(0.54,0.95,2HDB,2)                                     SPE04010
      CALL CTRMAG(8)                                                    SPE04020
      CALL PLOTCS(0.98,0.95,TITLE,64)                                   SPE04030
      CALL CTRMAG(20)                                                   SPE04040
      CALL PLOTCS(0.65,0.70,13HPOWER SPECTRA,13)                        SPE04050
      CALL CTRMAG(8)                                                    SPE04060
      CALL PLOTCS(0.560,0.95,5H 10.0,5)                                 SPE04070
      CALL PLOTCS(0.520,0.95,5H  0.0,5)                                 SPE04080
      CALL PLOTCS(0.480,0.95,5H-10.0,5)                                 SPE04090
      CALL PLOTCS(0.440,0.95,5H-20.0,5)                                 SPE04100
      CALL PLOTCS(0.400,0.95,5H-30.0,5)                                 SPE04110
      CALL PLOTCS(0.360,0.95,5H-40.0,5)                                 SPE04120
      CALL PLOTCS(0.320,0.95,5H-50.0,5)                                 SPE04130
      CALL PLOTCS(0.280,0.95,5H-60.0,5)                                 SPE04140
      CALL PLOTCS(0 240,0.95,5H-70.0,5)                                 SPE04150
      CALL PLOTCS(0.200,0.95,5H-80.0,5)                                 SPE04160
      CALL CTRORI(0.0)                                                  SPE04170
      CALL CTRMAG(10)                                                   SPE04180
   99 CONTINUE                                                          SPE04190
      CALL GREND                                                        SPE04200
  100 FORMAT(9I5)                                                       SPE04210
  101 FORMAT(//2(2X,I4,E11.4,E11.4,2X))                                 SPE04220
  102 FORMAT(1H ,8(1X,F8.4))                                            SPE04230
  103 FORMAT(1H ,2(2X,F10.5))                                           SPE04240
  104 FORMAT(///14H DATA DETAILS:,/,27H   K       T(K)        V(K),/)   SPE04250
  105 FORMAT(2X,I4,2X,F10.4,2X,F10.4)                                   SPE04260
  106 FORMAT(//25H X(I) & Y(I) AFTER FRXFM:,/)                          SPE04270
  107 FORMAT(//23H X(I) & Y(I) AFTER HAN:,/)                            SPE04280
  108 FORMAT(//25H X(I) & Y(I) AFTER BLOCK:,/)                          SPE04290
  109 FORMAT(//23H  POINTS TO BE PLOTTED:,/)                            SPE04300
  110 FORMAT(//19H CONTINUOUS V(K)...,/)                                SPE04310
  111 FORMAT(8A8)                                                       SPE04320
  895 FORMAT(//46H     &&&&&&&&& THIS IS THE TEST LINE &&&&&&&&&)       SPE04330
      STOP                                                              SPE04340
      END                                                               SPE04350
```

G.III 'FRXFM' Program Listing

FILE: FRXFM FORTRAN A1 (EE68)

```
      SUBROUTINE FRXFM(N2POW,NTHPOW,X,Y)                                FRX00010
      REAL X(NTHPOW), Y(NTHPOW), I,I1,I2,I3,I4                          FRX00020
      INTEGER PASS,SEQLOC,L(13)                                         FRX00030
      EQUIVALENCE (L13,L(1)),(L12,L(2)),(L11,L(3)),(L10,L(4)),          FRX00040
     1     (L9,L(5)),(L8,L(6)),(L7,L(7)),(L6,L(8)),(L5,L(9)),           FRX00050
     2     (L4,L(10)),(L3,L(11)),(L2,L(12)),(L1,L(13))                  FRX00060
      N4POW=N2POW/2                                                     FRX00070
      IF(N4POW.EQ.0) GO TO 3                                            FRX00080
      DO 2 PASS=1,N4POW                                                 FRX00090
      NXTLTH=2**(N2POW-2*PASS)                                          FRX00100
      LENGTH=4*NXTLTH                                                   FRX00110
      SCALE=6.283185307/FLOAT(LENGTH)                                   FRX00120
      DO 2 J=1,NXTLTH                                                   FRX00130
      ARG=FLOAT(J-1)*SCALE                                              FRX00140
      C1=COS(ARG)                                                       FRX00150
      S1=SIN(ARG)                                                       FRX00160
      C2=C1*C1-S1*S1                                                    FRX00170
      S2=C1*S1+C1*S1                                                    FRX00180
      C3=C1*C2-S1*S2                                                    FRX00190
      S3=C2*S1+S2*C1                                                    FRX00200
      DO 2 SEQLOC=LENGTH,NTHPOW,LENGTH                                  FRX00210
      J1=SEQLOC-LENGTH+J                                                FRX00220
      J2=J1+NXTLTH                                                      FRX00230
      J3=J2+NXTLTH                                                      FRX00240
      J4=J3+NXTLTH                                                      FRX00250
      R1=X(J1)+X(J3)                                                    FRX00260
      R2=X(J1)-X(J3)                                                    FRX00270
      R3=X(J2)+X(J4)                                                    FRX00280
      R4=X(J2)-X(J4)                                                    FRX00290
      I1=Y(J1)+Y(J3)                                                    FRX00300
      I2=Y(J1)-Y(J3)                                                    FRX00310
      I3=Y(J2)+Y(J4)                                                    FRX00320
      I4=Y(J2)-Y(J4)                                                    FRX00330
      X(J1)=R1+R3                                                       FRX00340
      Y(J1)=I1+I3                                                       FRX00350
      IF(J.EQ.1) GO TO 1                                                FRX00360
      X(J3)=C1*(R2-I4)-S1*(I2+R4)                                       FRX00370
      Y(J3)=S1*(R2-I4)+C1*(I2+R4)                                       FRX00380
      X(J2)=C2*(R1-R3)-S2*(I1-I3)                                       FRX00390
      Y(J2)=S2*(R1-R3)+C2*(I1-I3)                                       FRX00400
      X(J4)=C3*(R2+I4)-S3*(I2-R4)                                       FRX00410
      Y(J4)=S3*(R2+I4)+C3*(I2-R4)                                       FRX00420
      GO TO 2                                                           FRX00430
    1 X(J3)=R2-I4                                                       FRX00440
      Y(J3)=I2+R4                                                       FRX00450
      X(J2)=R1-R3                                                       FRX00460
      Y(J2)=I1-I3                                                       FRX00470
      X(J4)=R2+I4                                                       FRX00480
      Y(J4)=I2-R4                                                       FRX00490
    2 CONTINUE                                                          FRX00500
    3 IF(N2POW.EQ.2*N4POW) GO TO 5                                      FRX00510
      DO 4 J=1,NTHPOW,2                                                 FRX00520
      R=X(J)+X(J+1)                                                     FRX00530
      X(J+1)=X(J)-X(J+1)                                                FRX00540
      X(J)=R                                                            FRX00550
      I=Y(J)+Y(J+1)                                                     FRX00560
      Y(J+1)=Y(J)-Y(J+1)                                                FRX00570
    4 Y(J)=I                                                            FRX00580
    5 DO 6 J=1,13                                                       FRX00590
      L(J)=1                                                            FRX00600
    6 IF(J.LE.N2POW) L(J)=2**(N2POW+1-J)                                FRX00610
      IJ=1                                                              FRX00620
      DO 7 J1=1,L1                                                      FRX00630
      DO 7 J2=J1,L2,L1                                                  FRX00640
      DO 7 J3=J2,L3,L2                                                  FRX00650
      DO 7 J4=J3,L4,L3                                                  FRX00660
      DO 7 J5=J4,L5,L4                                                  FRX00670
      DO 7 J6=J5,L6,L5                                                  FRX00680
      DO 7 J7=J6,L7,L6                                                  FRX00690
      DO 7 J8=J7,L8,L7                                                  FRX00700
      DO 7 J9=J8,L9,L8                                                  FRX00710
      DO 7 J10=J9,L10,L9                                                FRX00720
      DO 7 J11=J10,L11,L10                                              FRX00730
      DO 7 J12=J11,L12,L11                                              FRX00740
      DO 7 JI=J12,L13,L12                                               FRX00750
      IF(IJ.GE.JI) GO TO 7                                              FRX00760
      R=X(IJ)                                                           FRX00770
      X(IJ)=X(JI)                                                       FRX00780
      X(JI)=R                                                           FRX00790
      I=Y(IJ)                                                           FRX00800
      Y(IJ)=Y(JI)                                                       FRX00810
      Y(JI)=I                                                           FRX00820
    7 IJ=IJ+1                                                           FRX00830
      RETURN                                                            FRX00840
      END                                                               FRX00850
```

G.IV 'BLOCK' Program Listing

```
      SUBROUTINE BLOCK(X,Y,N,NBLK)                                    BLO00010
C SPLITS ARRAY X, LENGTH N, INTO NBLK BLOCKS. X(1) IS SET TO          BLO00020
C ZERO AVERAGES OF X(I) IN EACH BLOCK ARE EVALUATED AND RETURNED      BLO00030
C IN THE FIRST NBLK POSITIONS OF X.                                   BLO00040
C FOR FRXFMS, THE FIRST NBLK POSITIONS OF Y CARRY MEAN BLOCK          BLO00050
C FREQUENCIES. N AND NBLK INTEGER POWERS OF TWO.                      BLO00060
      DIMENSION X(N), Y(N)                                            BLO00070
      NLPB=N/NBLK                                                     BLO00080
      KLST=N-NLPB+1                                                   BLO00090
      X(1)=0.0                                                        BLO00100
      NF=0                                                            BLO00110
      DO 1 K=1,KLST,NLPB                                              BLO00120
      NF=NF+1                                                         BLO00130
      Y(NF)=0.0                                                       BLO00140
      DO 1 J=1,NLPB                                                   BLO00150
      I=K+J-1                                                         BLO00160
    1 Y(NF)=Y(NF)+X(I)                                                BLO00170
      IF (NBLK.EQ.N) GO TO 3                                          BLO00180
      X(1)=Y(1)/FLOAT(NLPB-1)                                         BLO00190
      DO 2 K=2,NBLK                                                   BLO00200
    2 X(K)=Y(K)/FLOAT(NLPB)                                           BLO00210
      GO TO 5                                                         BLO00220
    3 DO 4 K=1,NBLK                                                   BLO00230
    4 X(K)=Y(K)                                                       BLO00240
    5 DO 6 K=1,NBLK                                                   BLO00250
    6 Y(K)=FLOAT((2*K-1)*NLPB-1)/FLOAT(4*N)                           BLO00260
      RETURN                                                          BLO00270
      END                                                             BLO00280
```

G.V 'HAN' Program Listing

```
      SUBROUTINE HAN(NTHPOW,X,Y)                                      HAN00010
C HANS FRXFM COEFFS IN ARRAYS X,Y GIVEN IN USUAL FORM ABOUT           HAN00020
C FOLDING FREQUENCY. SIGNAL POWER REDUCED BY 3/8.                     HAN00030
      DIMENSION X(NTHPOW), Y(NTHPOW)                                  HAN00040
      X1=0.5*(X(1)-X(2))                                              HAN00050
      Y1=0.5*Y(1)                                                     HAN00060
      XN=0.5*X(NTHPOW) - 0.25*(X(NTHPOW-1)+X(1))                      HAN00070
      YN=0.5*Y(NTHPOW) - 0.25*(Y(NTHPOW-1)+Y(1))                      HAN00080
      JLST=NTHPOW-1                                                   HAN00090
      XB=X(1)                                                         HAN00100
      YB=Y(1)                                                         HAN00110
      DO 1 J=2,JLST                                                   HAN00120
      XA=X(J)                                                         HAN00130
      YA=Y(J)                                                         HAN00140
      X(J)=0.5*X(J) - 0.25*(XB+X(J+1))                                HAN00150
      Y(J)=0.5*Y(J) - 0.25*(YB+Y(J+1))                                HAN00160
      XB=XA                                                           HAN00170
    1 YB=YA                                                           HAN00180
      X(1)=X1                                                         HAN00190
      Y(1)=Y1                                                         HAN00200
      X(NTHPOW)=XN                                                    HAN00210
      Y(NTHPOW)=YN                                                    HAN00220
      RETURN                                                          HAN00230
      END                                                             HAN00240
```

APPENDIX H

DATA LOGGING

H.I Twelve-Bit Data Logging

It was required that the mainframe computer could be used for storage and subsequent analysis of the test results obtained using the laboratory compensator. Section 4.2.2 showed that 8-bit digital sampling of voltage waveforms would not be able to accurately measure the small level of voltage disturbances that would just cause annoying lamp flicker.

To be able to measure the compensator's performance more effectively, a three channel data-logger incorporating three 12-bit ADCs was constructed. Sampling and immediate storage of data was controlled by an SDK-88 microprocessor development kit similar to that used in the TCR compensators (Part 4.2).

Data logging for any particular cycle of the arc furnace model's operation was initiated by the 10 microsecond synchronising pulse output from the AIM-65 microcomputer system.

A software sample loop delay time was incorporated into the controlling assembler language program 'sampsub', fixing the sampling interval for all three channels to 800 microseconds. The full program listing is given in H.II.

H.II 12-Bit ADC Sampling Program

```
                        ;NAME   synchronised_sampling_routine
                        NOLIST  INC

                        GLOBAL  sampsub
                        GLOBAL  CODEBASEQQ,DATABASEQQ,CONSTBASEQQ

                        ASSUME DS:DATABASEQQ

                        SECTION pascalprocedure,CLASS=INSTRQQ


;xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
;assembler routine to sample from 3 12-bit adcs at addresses FA00,FC00
;and FE00 . sampling is initiated by a 5v level on l.s.b. of PORT A of
;8255 PPI. the 5v level should last for at least 20us.
;
;the code for text strings is stored in the CONST  RAM segment so the
;results are offset from the beginning of this segment by 500 bytes.
;
;       pascal call :-  sampsub
;
;
;condition of stack on entry to this routine
;
;       RETURN ADDRESS          <--SP
;

sampsub
00000000 B400                   MOV AH,£00H             ;zero AH
00000002 B091                   MOV AL,£91H             ;
00000004 BA03F0                 MOV DX,£0F003H          ;set address of 8255 control port
00000007 EE                     OUT DX,AL               ;set ports as inputs
00000008 BA00F0                 MOV DX,£0F000H          ;set address of PORT A

idle
0000000B EC                     IN AL,DX                ;read byte from PORT A into AL
0000000C 3C00                   CMP AL,£00H             ;a '1' for any bit will initiate sampling
0000000E 74FB                   JE idle                 ;all bits zero perpetuates idle loop

00000010 B50F                   MOV CH,£0FH             ;set number of loops
00000012 BB0050                 MOV BX,£00050H          ;set start address for data storage
main
00000015 BA00FA                 MOV DX,£0FA00H          ;set address of adc1
00000018 EE                     OUT DX,AL               ;start conversion for 12-bit adc1
00000019 BA00FC                 MOV DX,£0FC00H          ;set address of adc2
0000001C EE                     OUT DX,AL               ;start conversion for 12-bit adc2
0000001D BA00FE                 MOV DX,£0FE00H          ;set address of adc3
00000020 EE                     OUT DX,AL               ;start conversion for 12 bit adc3

00000021 B12F                   MOV CL,£2FH             ;conversion delay 20us
00000023 D2E1                   SHR CL,CL
```

```
                        ;
00000025 BA00FA         MOV DX,£0FA00H          ;set address for high byte of 12-bit adc1
00000028 EC             IN AL,DX                ;read high byte of adc1
00000029 8807           MOV [BX],AL             ;store high byte
0000002B 42             INC DX                  ;set address for low nibble of 12-bit adc1
0000002C EC             IN AL,DX                ;read low nibble (left justified)
0000002D 43             INC BX                  ;next memory location for data storage
0000002E 8807           MOV [BX],AL             ;and store
                        ;
00000030 BA00FC         MOV DX,£0FC00H          ;repeat for adc2
00000033 EC             IN AL,DX                ;
00000034 43             INC BX                  ;
00000035 8807           MOV [BX],AL             ;
00000037 42             INC DX                  ;
00000038 EC             IN AL,DX                ;
00000039 43             INC BX                  ;
0000003A 8807           MOV [BX],AL             ;
                        ;
0000003C BA00FE         MOV DX,£0FE00H          ;repeat for adc3
0000003F EC             IN AL,DX                ;
00000040 43             INC BX                  ;
00000041 8807           MOV [BX],AL             ;
00000043 42             INC DX                  ;
00000044 EC             IN AL,DX                ;
00000045 43             INC BX                  ;
00000046 8807           MOV [BX],AL             ;
00000048 43             INC BX
                        ;
00000049 FECD           DEC CH                  ;decrement loop counter
0000004B 80FD00         CMP CH,£00H
0000004E 77E5 EA        JA again
00000050 C3             RET                     ;return to calling pascal program
                        ;
                        END
```

APPENDIX J

SYSMOD6.FORTRAN - COMPUTATIONAL ARC FURNACE MODEL PROGRAM LISTING

FILE: SYSMOD6 FORTRAN A1 (EE68)

```
C                                                                       SYS00010
C            SYSMOD6 FORTRAN..... SAME AS SYSMOD5 EXECPT CALLING        SYS00020
C            SUBROUTINES FROM TEXT LIBRARY 'SYSLIB'                     SYS00030
C                                                                       SYS00040
C                                                                       SYS00050
C                                                                       SYS00060
      EXTERNAL VZEROS,DEMOD,GRAF6,FOSPEC                                SYS00070
      REAL VR(2300),VY(2300),VB(2300),IB(2300),IR(2300),IY(2300),       SYS00080
     +   DIB(2300),DIR(2300),DIY(2300),                                 SYS00090
     +   I1(2300),I2(2300),I3(2300),DI1(2300),DI2(2300),DI3(2300),      SYS00100
     +   V1(2300),V2(2300),V3(2300),V4(2300),V5(2300),V6(2300),         SYS00110
     +   V7(2300),V8(2300),V9(2300),VSA(2300),VSB(2300),VSC(2300),      SYS00120
     +   MVRY(2300),MVYB(2300),MVBR(2300),                              SYS00130
     +   CVRY(2300),CVYB(2300),CVBR(2300),T(2300),                      SYS00140
     +   RTZERO(200),YTZERO(200),BTZERO(200),                           SYS00150
     +   CRTZ(200),CYTZ(200),CBTZ(200),                                 SYS00160
     +   VSPEAK,W,DELTA,PI,LLINE,LSYS,LSC,LTOT,RSC,RLINE,RSUM,RTOT,     SYS00170
     +   RERROR,YERROR,BERROR,RERSUM,YERSUM,BERSUM,AVSUM,AVFREQ,TUSED,  SYS00180
     +   RFREQ,YFREQ,BFREQ,CRFREQ,CYFREQ,CBFREQ,RADERR,DEGERR,LIMIT,    SYS00190
     +   DMVRY(2300),DMVYB(2300),DMVBR(2390),DCVRY(2300),DCVYB(2300),   SYS00200
     +   DCVBR(2300)                                                    SYS00210
      REAL TITLA(5),TITLB(5),TITLC(5),TITLD(5),TITLE(5),TITLF(5),       SYS00220
     +   TITLG(5),TITLH(5),                                             SYS00230
     +   GINFOB(4),                                                     SYS00240
     +   GINFO1(4),GINFO2(8),GINFO3(8),                                 SYS00250
     +   TITL1A(2),TITL2A(2),TITL3A(2),TITL4A(2),TITL5A(2),TITL6A(2),   SYS00260
     +   TITL1B(2),TITL2B(2),TITL3B(2),TITL4B(2),TITL5B(2),TITL6B(2),   SYS00270
     +   TITL1C(2),TITL2C(2),TITL3C(2),TITL4C(2),TITL5C(2),TITL6C(2),   SYS00280
     +   TITL1D(2),TITL2D(2),TITL3D(2),TITL4D(2),TITL5D(2),TITL6D(2),   SYS00290
     +   TITL1E(2),TITL2E(2),TITL3E(2),TITL4E(2),TITL5E(2),TITL6E(2),   SYS00300
     +   TITL1F(2),TITL2F(2),TITL3F(2),TITL4F(2),TITL5F(2),TITL6F(2),   SYS00310
     +   TITL1G(2),TITL2G(2),TITL3G(2),TITL4G(2),TITL5G(2),TITL6G(2),   SYS00320
     +   TITL1H(2),TITL2H(2),TITL3H(2),TITL4H(2),TITL5H(2),TITL6H(2),   SYS00330
C    +   FIRST(1),SECOND(1),THIRD(1),FOURTH(1),FIFTH(1),SIXTH(1),       SYS00340
     +   STRNG1(2),STRNG2(2),STRNG3(2),STRNG4(2),STRNG5(2),STRNG6(2)   SYS00350
      REAL SUM1,SUM2,SUM3,PLIM1,PLIM2,PLIM3,NLIM1,NLIM2,NLIM3,          SYS00360
     +HVSA,HVSB,HVSC,HIR,HIY,HIB,HDIR,HDIY,HDIB,                        SYS00370
     +LC,KL1,A1,A2,A3,B1,B2,B3,C1,C2,C3,D1,D2,D3,                       SYS00380
     +VLC1(2300),VLC2(2300),VLC3(2300),POSLIM,NEGLIM,                   SYS00390
     +ILC1(2300),ILC2(2300),ILC3(2300),                                 SYS00400
     +DILC1(2300),DILC2(2300),DILC3(2300),                              SYS00410
     +ILCR(2300),ILCY(2300),ILCB(2300),                                 SYS00420
     +DILCR(2300),DILCY(2300),DILCB(2300)                               SYS00430
      INTEGER I,J,K,L,M,N,POINTS,CHECK,LOOP,LOOPS,NPERSQ,               SYS00440
     +   RKROS(200),YKROS(200),BKROS(200),                              SYS00450
     +   CRKROS(200),CYKROS(200),CBKROS(200),                           SYS00460
     +   RCYCLS,YCYCLS,BCYCLS,CRCYCS,CYCYCS,CBCYCS,                     SYS00470
     +   RZEROS,YZEROS,BZEROS,CRZS,CYZS,CBZS                            SYS00480
      INTEGER ICON,ICOFF,K1,K2,K3,QCYC,QUART1,QUART2,QUART3             SYS00490
      LOGICAL PLOT,NOPLOT,LONG,DMOD,NODMOD,LIST,NOLIST,DMOD2,SPEC,SPEC3,SYS00500
     +CYC10                                                             SYS00510
      LOGICAL NOCOMP,COMPON,INT1P,INT2P,INT3P,INT1N,INT2N,INT3N,        SYS00520
     +ON1,ON2,ON3,NEGI1,NEGI2,NEGI3,POSI1,POSI2,POSI3                   SYS00530
      COMMON/COM1/LIST,NOLIST,POINTS/COM2/TSTEP,PI,ROOT2                SYS00540
C                                                                       SYS00550
C.....................READ THE LINES CONTAINING EXPLANATORY CHARACTERS  SYS00560
C                     AT THE BEGINNING OF THE 'OPTION' DATA FILE .      SYS00570
C                                                                       SYS00580
      READ(3,800)                                                       SYS00590
      READ(3,800)                                                       SYS00600
      READ(3,800)                                                       SYS00610
C                                                                       SYS00620
C.....................READ THE COMPENSATOR OPTIONS FOR THIS RUN OF THE  SYS00630
C                     PROGRAM:                                          SYS00640
C                             LC : VALUE IN HENRIES OF COMPENSATOR      SYS00650
C                                                   BRANCH INDUCTANCE   SYS00660
C                          POSLIM : INTEGRATION LIMIT FOR A +'VE HALF CYCLESYS00670
C                          NEGLIM : INTEGRATION LIMIT FOR A -'VE HALF CYCLESYS00680
C                            ICON : FIRST VALUE OF 'I' FOR COMPENSATOR 'ON'SYS00690
C                           ICOFF : LAST VALUE OF 'I' FOR COMPENSATOR 'ON' SYS00700
C                                                                       SYS00710
      READ(3,795) LC,POSLIM,NEGLIM,ICON,ICOFF                           SYS00720
      READ(3,794) GINFO2                                                SYS00730
      READ(3,794) GINFO3                                                SYS00740
```

```
C                                                                       SYS00750
C.....................READ THE LINES CONTAINING EXPLANATORY CHARACTERS   SYS00760
C                     AT THE BEGINNING OF THE 'OPTION' DATA FILE .      SYS00770
C                                                                       SYS00780
      READ(4,800)                                                       SYS00790
      READ(4,800)                                                       SYS00800
      READ(4,800)                                                       SYS00810
      READ(4,800)                                                       SYS00820
C                                                                       SYS00830
C.....................READ OPTIONS FOR THIS RUN OF THE PROGRAM.         SYS00840
C                     TSTEP : TIME INTERVAL BETWEEN SUCCESSIVE DATA PTS. SYS00850
C                     LIMIT : ERROR LIMIT FOR EVALUATING DELTA.         SYS00860
C                     LOOPS : MAX. NO. OF LOOPS TO TRY FOR 'LIMIT' ABOVE SYS00870
C                     LIST  : T/F  (T IF FULL LISTING REQUIRED IN O/P)  SYS00880
C                     PLOT  : T/F  (T IF PLOTTING IS REQUIRED)          SYS00890
C                     LONG  : T/F  (T IF LONG CALCOMP PLOTS WILL BE USED) SYS00900
C                     SPEC  : T/F  (T IF OUTPUT REQUIRED FOR SPECTRAL   SYS00910
C                                                          ANALYSIS)    SYS00920
C                     SPEC3 : T/F  (T IF OUTPUT FOR SPECTRAL ANALYSIS OF SYS00930
C                                                3 CHANNELS IS REQUIRED) SYS00940
C                     DMOD  : T/F  (T IF DEMODULATION IS REQUIRED)      SYS00950
C                     DMOD2 : T/F  (T FOR SAME SINE WAVE TO BE          SYS00960
C                                   SUBTRACTED FROM BOTH MEASURED       SYS00970
C                                   AND CALCULATED VOLTAGE WAVEFORMS)   SYS00980
C                                                                       SYS00990
C                                                                       SYS01000
C                     *** NOTE *** .....   DMOD.AND.DMOD2  IS ILLEGAL   SYS01010
C                                          SPEC.AND.SPEC3 = SPEC3       SYS01020
C                                                                       SYS01030
      READ(4,897)TSTEP,LIMIT,LOOPS,LIST,PLOT,LONG,SPEC,SPEC3,DMOD,DMOD2 SYS01040
C                                                                       SYS01050
C.....................THE OPTIONS USED ARE ALWAYS PRINTED               SYS01060
C                                                                       SYS01070
      WRITE(6,896)TSTEP,LIMIT,LOOPS,LIST,PLOT,LONG,SPEC,SPEC3,DMOD,DMOD2SYS01080
      WRITE(6,793) LC,POSLIM,NEGLIM,ICON,ICOFF                          SYS01090
      WRITE(6,792) (GINFO2(I),I=1,8),(GINFO3(I),I=1,8)                  SYS01100
C                                                                       SYS01110
C.....................CHECK FOR ILLEGAL INPUT COMBINATION               SYS01120
C                                                                       SYS01130
      IF(DMOD.AND.DMOD2) GOTO 160                                       SYS01140
C                                                                       SYS01150
C.....................USING INVERSE LOGICAL VARIABLES IMPROVES THE      SYS01160
C                     'READABILITY' OF THE PROGRAM.                     SYS01170
C                                                                       SYS01180
      NOLIST=.NOT.LIST                                                  SYS01190
      NOPLOT=.NOT.PLOT                                                  SYS01200
      NODMOD=.NOT.DMOD                                                  SYS01210
C                                                                       SYS01220
C.....................DEFINE CERTAIN CONSTANTS THAT ARE FREQUENTLY      SYS01230
C                     USED IN THE PROGRAM.                              SYS01240
C                                                                       SYS01250
      PI=3.1415926536                                                   SYS01260
      ROOT2=SQRT(2.0)                                                   SYS01270
      ROOT3=SQRT(3.0)                                                   SYS01280
C                                                                       SYS01290
C.....................THE SYSTEM PARAMETERS ARE SET HERE WHILE THEY     SYS01300
C                     ARE NOT LIKELY TO BE CHANGED.                     SYS01310
C                                                                       SYS01320
C                     ALL VALUES ARE IN OHMS.                           SYS01330
C                                                                       SYS01340
      RLINE=0.00218                                                     SYS01350
      XLINE=0.01089                                                     SYS01360
      XSYS=0.1307                                                       SYS01370
      XSC=2.595                                                         SYS01380
      RSC=0.0565                                                        SYS01390
      RTOT=RSC+RLINE                                                    SYS01400
      QCYC=7                                                            SYS01410
      VSPEAK=33.0*ROOT2                                                 SYS01420
C                                                                       SYS01430
C....CERTAIN VARIABLES ARE SET HERE TEMPORARILY INSTEAD OF BEING READ   SYS01440
C    FROM THE OPTIONS FILE                                              SYS01450
C                                                                       SYS01460
      NOCOMP=.FALSE.                                                    SYS01470
      PLIM1=POSLIM                                                      SYS01480
      PLIM2=POSLIM                                                      SYS01490
      PLIM3=POSLIM                                                      SYS01500
      NLIM1=NEGLIM                                                      SYS01510
      NLIM2=NEGLIM                                                      SYS01520
      NLIM3=NEGLIM                                                      SYS01530
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C                                                                       SYS01540
C.....................THE FOLLOWING ALPHNUMERIC STRINGS ARE USED        SYS01550
C                     TO IDENTIFY PRINTED OUTPUT PRODUCED FROM SEVERAL  SYS01560
C                     CALLS TO THE SAME SECTION                         SYS01570
C                                                                       SYS01580
C     DATA  FIRST/'  FIRST '/                                           SYS01590
C     DATA SECOND/' SECOND '/                                           SYS01600
C     DATA  THIRD/'  THIRD '/                                           SYS01610
C     DATA FOURTH/' FOURTH '/                                           SYS01620
C     DATA  FIFTH/'  FIFTH '/                                           SYS01630
C     DATA  SIXTH/'  SIXTH '/                                           SYS01640
C                                                                       SYS01650
C.....................'GINFO' ALPHANUMERIC INFORMATION IS FOR           SYS01660
C                      INCLUSION IN PLOTTED OUTPUT.                     SYS01670
C                                                                       SYS01680
      DATA GINFOB/'        ','        ','        ','        '/          SYS01690
      DATA GINFO1/'***  COM','MON  DEM','ODULATIO','N  ***  '/          SYS01700
C                                                                       SYS01710
C.....................'STRNG' ALPHANUMERIC DATA IS COMMON TO            SYS01720
C                      SEVERAL PLOTTING SUBROUTINES                     SYS01730
C                                                                       SYS01740
      DATA STRNG1/'  MEASUR','ED  VR  '/                                SYS01750
      DATA STRNG2/'  MEASUR','ED  VY  '/                                SYS01760
      DATA STRNG3/'  MEASUR','ED  VB  '/                                SYS01770
      DATA STRNG4/' CALCULA','TED  VR '/                                SYS01780
      DATA STRNG5/' CALCULA','TED  VY '/                                SYS01790
      DATA STRNG6/' CALCULA','TED  VB '/                                SYS01800
C                                                                       SYS01810
C.....................SKIP THE FIRST LINE OF THE DATA FILE             SYS01820
C                      (DESCRIPTIVE TEXT)                               SYS01830
C                                                                       SYS01840
      READ(5,800)                                                       SYS01850
C                                                                       SYS01860
C.....................THE FOLLOWING LOOP FOR 'I' READS DATA            SYS01870
C                      UNTIL A BLANK LINE IS ENCOUNTERED                SYS01880
C                                                                       SYS01890
      I=0                                                               SYS01900
   20 I=I+1                                                             SYS01910
      READ(5,999) VR(I),VY(I),VB(I),IB(I),IR(I),IY(I),DIB(I),           SYS01920
     +DIR(I),DIY(I)                                                     SYS01930
      T(I)=FLOAT(I)*TSTEP                                               SYS01940
      IF(I.LT.5)WRITE(6,998)VR(I),VY(I),VB(I),IB(I),IR(I),IY(I),        SYS01950
     +DIB(I),DIR(I),DIY(I)                                              SYS01960
      MVRY(I)=VR(I)-VY(I)                                               SYS01970
      MVYB(I)=VY(I)-VB(I)                                               SYS01980
      MVBR(I)=VB(I)-VR(I)                                               SYS01990
      IF(VR(I).NE.0.0.OR.VY(I).NE.0.0) GOTO 20                          SYS02000
      POINTS=I-1                                                        SYS02010
      CYC10=.TRUE.                                                      SYS02020
      IF(POINTS.GE.300) CYC10=.FALSE.                                   SYS02030
C                                                                       SYS02040
C.....................'POINTS' IS THE NUMBER OF LINES OF INPUT DATA.    SYS02050
C                                                                       SYS02060
      WRITE(6,992)POINTS                                                SYS02070
C                                                                       SYS02080
C.....................INITIALISE WHERE NECCESSARY                      SYS02090
C                                                                       SYS02100
      RERROR=0.0                                                        SYS02110
      RERSUM=0.0                                                        SYS02120
      YERROR=0.0                                                        SYS02130
      YERSUM=0.0                                                        SYS02140
      BERROR=0.0                                                        SYS02150
      BERSUM=0.0                                                        SYS02160
      AVSUM=0.0                                                         SYS02170
      AVFREQ=0.0                                                        SYS02180
      DEGERR=0.0                                                        SYS02190
      RADERR=0.0                                                        SYS02200
      DO 40 I=1,POINTS,1                                                SYS02210
          VLC1(I)=0.0                                                   SYS02220
          VLC2(I)=0.0                                                   SYS02230
          VLC3(I)=0.0                                                   SYS02240
          DILC1(I)=0.0                                                  SYS02250
          DILC2(I)=0.0                                                  SYS02260
          DILC3(I)=0.0                                                  SYS02270
   40 CONTINUE                                                          SYS02280
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      CALL VZEROS(POINTS,MVRY,T,RTZERO,RZEROS,RCYCLS,RFREQ,RKROS,VRRMS, SYS02290
     +CHECK,STRNG1)                                                    SYS02300
      IF(CHECK.EQ.0) WRITE(6,997)                                      SYS02310
      CALL VZEROS(POINTS,MVYB,T,YTZERO,YZEROS,YCYCLS,YFREQ,YKROS,VYRMS, SYS02320
     +CHECK,STRNG2)                                                    SYS02330
      IF(CHECK.EQ.0) WRITE(6,996)                                      SYS02340
      CALL VZEROS(POINTS,MVBR,T,BTZERO,BZEROS,BCYCLS,BFREQ,BKROS,VBRMS, SYS02350
     +CHECK,STRNG3)                                                    SYS02360
      IF(CHECK.EQ.0) WRITE(6,995)                                      SYS02370
      WRITE(6,993) RZEROS,YZEROS,BZEROS,RCYCLS,YCYCLS,BCYCLS,          SYS02380
     +             RFREQ,YFREQ,BFREQ                                   SYS02390
      RSUM=RLINE+RSC                                                   SYS02400
      W=2.0*PI*RFREQ                                                   SYS02410
      DELTA=-0.2                                                       SYS02420
      LOOP=0                                                           SYS02430
   50 LOOP=LOOP+1                                                      SYS02440
      IF(LOOP.GT.LOOPS)GOTO 140                                        SYS02450
      IF(CYC10) DELTA=DELTA-1.0*RADERR                                 SYS02460
      IF(.NOT.CYC10) DELTA=DELTA-0.1*RADERR                            SYS02470
      RERSUM=0.0                                                       SYS02480
      YERSUM=0.0                                                       SYS02490
      BERSUM=0.0                                                       SYS02500
   60 CONTINUE                                                         SYS02510
      LLINE=XLINE/W                                                    SYS02520
      LSYS=XSYS/W                                                      SYS02530
      LSC=XSC/W                                                        SYS02540
      LTOT=LSYS+LSC+LLINE                                              SYS02550
      KL1 = 1.0/(LC*(3.0*LTOT+LC))                                     SYS02560
      DO 100 I=1,POINTS,1                                              SYS02570
C                                                                      SYS02580
C.................EVALUATE PRIMARY CIRCUIT LINE CURRENTS              SYS02590
C                  FROM SECONDARY CIRCUIT LINE CURRENTS                SYS02600
C                      (CURRENT TRANSFORMATION)                        SYS02610
C                                                                      SYS02620
C                                                                      SYS02630
         I1(I)=(IB(I)-IR(I))/ROOT3                                     SYS02640
         I2(I)=(IR(I)-IY(I))/ROOT3                                     SYS02650
         I3(I)=(IB(I)-IB(I))/ROOT3                                     SYS02660
C                                                                      SYS02670
C.................SIMILARLY FOR CURRENT FIRST DERIVATIVES             SYS02680
C                      (CURRENT TRANSFORMATION)                        SYS02690
C                                                                      SYS02700
C                                                                      SYS02710
         DI1(I)=(DIB(I)-DIR(I))/ROOT3                                  SYS02720
         DI2(I)=(DIR(I)-DIY(I))/ROOT3                                  SYS02730
         DI3(I)=(DIY(I)-DIB(I))/ROOT3                                  SYS02740
   80    CONTINUE                                                      SYS02750
C                                                                      SYS02760
C.................SET-UP SYSTEM VOLTAGES,                             SYS02770
C                  THREE PHASE SINUSOIDAL ADVANCED BY PHASE ANGLE      SYS02780
C                  'DELTA'  WITH RESPECT TO VOLTAGES AT THE            SYS02790
C                  FURNACE BUSBAR (V7,V8,V9)                           SYS02800
C                                                                      SYS02810
         VSA(I)=VSPEAK*COS(W*T(I)+DELTA)                               SYS02820
         VSB(I)=VSPEAK*COS(W*T(I)-2.0*PI/3.0+DELTA)                    SYS02830
         VSC(I)=VSPEAK*COS(W*T(I)+2.0*PI/3.0+DELTA)                    SYS02840
C                                                                      SYS02850
C.................CALCULATE TRANSFORMER PRIMARY VOLTAGES              SYS02860
C                  USING VOLT-DROPS.                                   SYS02870
C                                                                      SYS02880
         V1(I)=VSA(I) - RSC*(I1(I)-I2(I)) - (LSYS+LSC)*(DI1(I)-DI2(I)) SYS02890
         V2(I)=VSB(I) - RSC*(I2(I)-I3(I)) - (LSYS+LSC)*(DI2(I)-DI3(I)) SYS02900
         V3(I)=VSC(I) - RSC*(I3(I)-I1(I)) - (LSYS+LSC)*(DI3(I)-DI1(I)) SYS02910
C                                                                      SYS02920
C.................PRIMARY TO SECONDARY                                SYS02930
C                  VOLTAGE TRANSFORMATION                              SYS02940
C                                                                      SYS02950
         V4(I)=(V1(I)-V2(I))/ROOT3                                     SYS02960
         V5(I)=(V2(I)-V3(I))/ROOT3                                     SYS02970
         V6(I)=(V3(I)-V1(I))/ROOT3                                     SYS02980
C                                                                      SYS02990
C.................ALLOW FOR CABLE VOLT-DROP                           SYS03000
C                                                                      SYS03010
         V7(I)=V4(I) - RLINE*(IR(I)-IY(I)) - LLINE*(DIR(I)-DIY(I))     SYS03020
         V8(I)=V5(I) - RLINE*(IY(I)-IB(I)) - LLINE*(DIY(I)-DIB(I))     SYS03030
         V9(I)=V6(I) - RLINE*(IB(I)-IR(I)) - LLINE*(DIB(I)-DIR(I))     SYS03040
         CVRY(I)=V7(I)                                                 SYS03050
         CVYB(I)=V8(I)                                                 SYS03060
         CVBR(I)=V9(I)                                                 SYS03070
         IF(LOOP.NE.LOOPS)GOTO 90                                      SYS03080
         IF(LIST) WRITE(6,994)VR(I),VY(I),VB(I),                       SYS03090
     +   CVRY(I),CVYB(I),CVBR(I)                                       SYS03100
   90    CONTINUE                                                      SYS03110
  100 CONTINUE                                                         SYS03120
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      IF(.NOT.LIST) GOTO 101                                            SYS03130
              WRITE(6,892)                                              SYS03140
              DO 101 I=1,15,1                                           SYS03150
                  WRITE(6,893) VR(I),VY(I),VB(I),                       SYS03160
     +                         IR(I),IY(I),IB(I),                       SYS03170
     +                         CVRY(I),CVYB(I),CVBR(I)                  SYS03180
  101 CONTINUE                                                          SYS03190
C                                                                       SYS03200
C.................USE VZEROS SUBROUTINE TO GET DETAILS OF              SYS03210
C                  ZERO CROSSING POINTS OF CALCULATED VOLTAGES          SYS03220
C                                                                       SYS03230
      CALL VZEROS(POINTS,CVRY,T,CRTZ,CRZS,CRCYCS,CRFREQ,CRKROS,CVRRMS,  SYS03240
     +CHECK,STRNG4)                                                     SYS03250
      CALL VZEROS(POINTS,CVYB,T,CYTZ,CYZS,CYCYCS,CYFREQ,CYKROS,CVYRMS,  SYS03260
     +CHECK,STRNG5)                                                     SYS03270
      CALL VZEROS(POINTS,CVBR,T,CBTZ,CBZS,CBCYCS,CBFREQ,CBKROS,CVBRMS,  SYS03280
     +CHECK,STRNG6)                                                     SYS03290
      IF(.NOT.LIST) GOTO 118                                            SYS03300
      WRITE(6,991)                                                      SYS03310
      WRITE(6,990)(J,RKROS(J),YKROS(J),BKROS(J),                        SYS03320
     +             CRKROS(J),CYKROS(J),CBKROS(J),J=1,YZEROS,1)          SYS03330
      WRITE(6,891)                                                      SYS03340
  118 CONTINUE                                                          SYS03350
C                                                                       SYS03360
C.................CALCULATE A SUM OF DIFFERENCES BETWEEN THE           SYS03370
C                  ZERO CROSSING POINTS OF                              SYS03380
C                  MEASURED AND CALCULATED VOLTAGES.                    SYS03390
C                                                                       SYS03400
      DO 120 J=1,YZEROS,1                                               SYS03410
           RERROR=RTZERO(J)-CRTZ(J)                                     SYS03420
           YERROR=YTZERO(J)-CYTZ(J)                                     SYS03430
           BERROR=BTZERO(J)-CBTZ(J)                                     SYS03440
           IF(LIST) WRITE(6,890) J,RTZERO(J),CRTZ(J),YTZERO(J),CYTZ(J), SYS03450
     +                           BTZERO(J),CBTZ(J)                    SYS03460
           RERSUM=RERSUM+RERROR                                         SYS03470
           YERSUM=YERSUM+YERROR                                         SYS03480
           BERSUM=BERSUM+BERROR                                         SYS03490
  120 CONTINUE                                                          SYS03500
      AVSUM=(RERSUM+YERSUM+BERSUM)/(3.0*YZEROS)                         SYS03510
      AVFREQ=(RFREQ+YFREQ+BFREQ)/3.0                                    SYS03520
C                                                                       SYS03530
C.................CALCULATE AN AVERAGE PHASE ERROR BETWEEN             SYS03540
C                  MEASURED AND CALCULATED VOLTAGES AND RETURN          SYS03550
C                  TO ADJUST 'DELTA' IF THE ERROR IS OUTSIDE            SYS03560
C                  THE PRESET LIMIT.                                    SYS03570
C                                                                       SYS03580
      DEGERR=AVSUM*AVFREQ*360.0                                         SYS03590
      RADERR=1.0*PI*DEGERR/180.0                                        SYS03600
      WRITE(6,899)LOOP,DELTA,RADERR,AVSUM                               SYS03610
      IF(RADERR.GT.LIMIT.OR.RADERR.LT.-LIMIT)GOTO 50                    SYS03620
C                                                                       SYS03630
C.................PRINT THE FIRST 25 VALUES OF EACH ARRAY              SYS03640
C                  TO AID FAULT FINDING                                 SYS03650
C                                                                       SYS03660
          WRITE(6,699)                                                  SYS03670
          WRITE(6,666) (I1(I),I2(I),I3(I), I=1,25,1)                    SYS03680
          WRITE(6,698)                                                  SYS03690
          WRITE(6,666) (DI1(I),DI2(I),DI3(I), I=1,25,1)                 SYS03700
          WRITE(6,697)                                                  SYS03710
          WRITE(6,666) (VSA(I),VSB(I),VSC(I), I=1,25,1)                 SYS03720
          WRITE(6,696)                                                  SYS03730
          WRITE(6,666) (V1(I),V2(I),V3(I), I=1,25,1)                    SYS03740
          WRITE(6,695)                                                  SYS03750
          WRITE(6,666) (V4(I),V5(I),V6(I), I=1,25,1)                    SYS03760
  699 FORMAT(///32H FIRST 25 PRIMARY LINE CURRENTS:/)                   SYS03770
  698 FORMAT(///32H FIRST 25 PRIMARY DI/DT'S      :/)                   SYS03780
  697 FORMAT(///32H FIRST 25 SYSTEM LINE VOLTAGES :/)                   SYS03790
  696 FORMAT(///32H FIRST 25 PRIMARY LINE VOLTAGES:/)                   SYS03800
  695 FORMAT(///32H FIRST 25 SECONDARY LINE VOLTS :/)                   SYS03810
  666 FORMAT(3(F12.4,5X))                                               SYS03820
```

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CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C                                                                       C
C                                                                       C
C                                                                       C
C                                                                       C
C.................A REPRESENTATION OF A DELTA-CONNECTED COMPENSATOR     C
C                 FOLLOWS FROM THIS POINT.                              C
C                                                                       C
C                                                                       C
C                                                                       C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      I=0
      IF(NOCOMP) GOTO 520
  200 I=I+1
      IF(I.LT.ICON) GOTO 200
      COMPON=.FALSE.
C
C.................FOR THE FIRST VALUE OF 'I' FOR WHICH THE COMPENSATOR
C                 IS 'ON' , VALUES OF V7, V8, V9  ARE USED
C                 AS THE VOLTAGE ACROSS EACH BRANCH OF THE COMPENSATOR
C
C
      VLC1(I-1)=V7(I-1)
      VLC2(I-1)=V8(I-1)
      VLC3(I-1)=V9(I-1)
      VLC1(I)=V7(I)
      VLC2(I)=V8(I)
      VLC3(I)=V9(I)
  210 CONTINUE
      WRITE(6,212) I
  212 FORMAT(//5H  I =,I3)
C
C...............IF COMPON IS .FALSE. NO FURTHER INTEGRATION OR
C               SWITCHING ON CAN TAKE PLACE BUT CURRENT IN CONDUCTING
C               BRANCHES IS ALLOWED TO FLOW UNTIL A CURRENT ZERO
C
      IF(.NOT.COMPON) GOTO 310
C
C...............FOR INCREMENT OF 'I' FLAGS ARE SET SHOWING WHAT STAGE
C               CALCULATIONS ARE AT FOR EACH BRANCH OF THE COMPENSATOR
C
C               'INT1P' TRUE MEANS INTEGRATION FOR RED BRANCH IN POS.
C               'INT1N' TRUE MEANS INTEGRATION FOR RED BRANCH IN NEG.
C                                  ---         -         -
C                                                        HALF CYCLES
C
C               'SUM1' WILL CONTAIN THE CUMULATIVE INTEGRATION VALUE
C
C
      IF(INT1P.OR.INT1N) GOTO 230
      IF(VLC1(I).GT.0.0.AND.VLC1(I-1).LE.0.0) GOTO 215
      INT1P=.FALSE.
      GOTO 220
  215 INT1P=.TRUE.
      SUM1=0.0
      QUART1=0
  220 IF(VLC1(I).LT.0.0.AND.VLC1(I-1).GE.0.0) GOTO 225
      INT1N=.FALSE.
      GOTO 230
  225 INT1N=.TRUE.
      SUM1=0.0
      QUART1=0
C
C...............SIMILARLY FOR YELLOW BRANCH
C
  230 IF(INT2P.OR.INT2N) GOTO 250
      IF(VLC2(I).GT.0.0.AND.VLC2(I-1).LE.0.0) GOTO 235
      INT2P=.FALSE.
      GOTO 240
  235 INT2P=.TRUE.
      SUM2=0.0
      QUART2=0
  240 IF(VLC2(I).LT.0.0.AND.VLC2(I-1).GE.0.0) GOTO 245
      INT2N=.FALSE.
      GOTO 250
  245 INT2N=.TRUE.
      SUM2=0.0
      QUART2=0
```

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C                                                                       SYS04610
C.................SIMILARLY FOR BLUE BRANCH                            SYS04620
C                                                                       SYS04630
  250 IF(INT3P.OR.INT3N) GOTO 270                                       SYS04640
      IF(VLC3(I).GT.0.0.AND.VLC3(I-1).LE.0.0) GOTO 255                  SYS04650
      INT3P=.FALSE.                                                     SYS04660
      GOTO 260                                                          SYS04670
  255 INT3P=.TRUE.                                                      SYS04680
      SUM3=0.0                                                          SYS04690
      QUART3=0                                                          SYS04700
  260 IF(VLC3(I).LT.0.0.AND.VLC3(I-1).GE.0.0) GOTO 265                  SYS04710
      INT3N=.FALSE.                                                     SYS04720
      GOTO 270                                                          SYS04730
  265 INT3N=.TRUE.                                                      SYS04740
      SUM3=0.0                                                          SYS04750
      QUART3=0                                                          SYS04760
  270 CONTINUE                                                          SYS04770
      WRITE(6,796) ON1,ON2,ON3,POSI1,POSI2,POSI3,INT1N,INT2N,INT3N,     SYS04780
     +NEGI1,NEGI2,NEGI3,INT1P,INT2P,INT3P                               SYS04790
C                                                                       SYS04800
C.................CHECK FOR ATTEMPTED POS. & NEG. INTEGRATION          SYS04810
C                                                                       SYS04820
      IF(INT1P.AND.INT1N) GOTO 150                                      SYS04830
      IF(INT2P.AND.INT2N) GOTO 150                                      SYS04840
      IF(INT3P.AND.INT3N) GOTO 150                                      SYS04850
C                                                                       SYS04860
C.................INTEGRATION CAN ONLY PROCEED IF THE SIGN OF THE      SYS04870
C                 MEASURED POINTS REMAINS IN THE CORRECT SENSE          SYS04880
C                 ( CHECKING FOR END OF HALF CYCLE)                     SYS04890
C                 OTHERWISE THE INTEGRATION IS ABANDONED                SYS04900
C                                                                       SYS04910
C.................FOR RED BRANCH                                       SYS04920
C                                                                       SYS04930
C                                                                       SYS04940
      IF(INT1P) GOTO 271                                                SYS04950
      IF(INT1N) GOTO 272                                                SYS04960
      GOTO 274                                                          SYS04970
  271 IF(VLC1(I).GT.0.0) GOTO 273                                       SYS04980
          INT1P=.FALSE.                                                 SYS04990
          SUM1=0.0                                                      SYS05000
          QUART1=0                                                      SYS05010
          GOTO 275                                                      SYS05020
  272 IF(VLC1(I).LT.0.0) GOTO 273                                       SYS05030
          INT1N=.FALSE.                                                 SYS05040
          SUM1=0.0                                                      SYS05050
          QUART1=0                                                      SYS05060
          GOTO 274                                                      SYS05070
  273 CONTINUE                                                          SYS05080
      SUM1=SUM1+VLC1(I)                                                 SYS05090
      QUART1=QUART1+1                                                   SYS05100
  274 CONTINUE                                                          SYS05110
C                                                                       SYS05120
C.................FOR YELLOW BRANCH                                    SYS05130
C                                                                       SYS05140
      IF(INT2P) GOTO 275                                                SYS05150
      IF(INT2N) GOTO 276                                                SYS05160
      GOTO 278                                                          SYS05170
  275 IF(VLC2(I).GT.0.0) GOTO 277                                       SYS05180
          INT2P=.FALSE.                                                 SYS05190
          SUM2=0.0                                                      SYS05200
          QUART2=0                                                      SYS05210
          GOTO 278                                                      SYS05220
  276 IF(VLC2(I).LT.0.0) GOTO 277                                       SYS05230
          INT2N=.FALSE.                                                 SYS05240
          SUM2=0.0                                                      SYS05250
          QUART2=0                                                      SYS05260
          GOTO 278                                                      SYS05270
  277 CONTINUE                                                          SYS05280
      SUM2=SUM2+VLC2(I)                                                 SYS05290
      QUART2=QUART2+1                                                   SYS05300
  278 CONTINUE                                                          SYS05310
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C                                                                       SYS05320
C.....................FOR BLUE BRANCH                                   SYS05330
C                                                                       SYS05340
      IF(INT3P) GOTO 279                                                SYS05350
      IF(INT3N) GOTO 280                                                SYS05360
      GOTO 282                                                          SYS05370
  279 IF(VLC3(I).GT.0.0) GOTO 281                                       SYS05380
          INT3P=.FALSE.                                                 SYS05390
          SUM3=0.0                                                      SYS05400
          QUART3=0                                                      SYS05410
          GOTO 282                                                      SYS05420
  280 IF(VLC3(I).LT.0.0) GOTO 281                                       SYS05430
          INT3N=.FALSE.                                                 SYS05440
          SUM3=0.0                                                      SYS05450
          QUART3=0                                                      SYS05460
          GOTO 282                                                      SYS05470
  281 CONTINUE                                                          SYS05480
      SUM3=SUM3+VLC3(I)                                                 SYS05490
      QUART3=QUART3+1                                                   SYS05500
  282 CONTINUE                                                          SYS05510
C                                                                       SYS05520
      WRITE(6,797) SUM1,SUM2,SUM3,QUART1,QUART2,QUART3                  SYS05530
C                                                                       SYS05540
C.................SET FURTHER FLAGS IF THE INTEGRATION LIMITS ARE REACHEDSYS05550
C                ( UNLESS THE INTEGRATION LIMITS ARE SO SMALL THAT      SYS05560
C                  CONDUCTION WOULD START BEFORE THE 1/4 CYCLE POINT )  SYS05570
C                                                                       SYS05580
C                 'POSI1' INDICATES ALLOWANCE OF CURRENT FLOW IN RED    SYS05590
C                         BRANCH OF COMPENSATOR AS RESULT OF INTEGRATIONSYS05600
C                         IN POSITIVE HALF-CYCLE OF 'VLCR'.           SYS05610
C                                                                       SYS05620
C                 'ON1'   RED BRANCH ON                                 SYS05630
C                                                                       SYS05640
C                                                                       SYS05650
      IF(QUART1.LT.QCYC) GOTO 285                                       SYS05660
      IF(SUM1.LT.PLIM1) GOTO 284                                        SYS05670
      IF(NEGI1) GOTO 285                                                SYS05680
      ON1=.TRUE.                                                        SYS05690
      POSI1=.TRUE.                                                      SYS05700
      INT1P=.FALSE.                                                     SYS05710
      SUM1=0.0                                                          SYS05720
      QUART1=0                                                          SYS05730
  284 IF(SUM1.GT.NLIM1) GOTO 285                                        SYS05740
      IF(POSI1) GOTO 285                                                SYS05750
      ON1=.TRUE.                                                        SYS05760
      NEGI1=.TRUE.                                                      SYS05770
      INT1N=.FALSE.                                                     SYS05780
      SUM1=0.0                                                          SYS05790
      QUART1=0                                                          SYS05800
C                                                                       SYS05810
C.................SIMILARLY FOR YELLOW BRANCH                          SYS05820
C                                                                       SYS05830
  285 IF(QUART2.LT.QCYC) GOTO 295                                       SYS05840
      IF(SUM2.LT.PLIM2) GOTO 290                                        SYS05850
      IF(NEGI2) GOTO 295                                                SYS05860
      ON2=.TRUE.                                                        SYS05870
      POSI2=.TRUE.                                                      SYS05880
      INT2P=.FALSE.                                                     SYS05890
      SUM2=0.0                                                          SYS05900
      QUART2=0                                                          SYS05910
  290 IF(SUM2.GT.NLIM2) GOTO 295                                        SYS05920
      IF(POSI2) GOTO 295                                                SYS05930
      ON2=.TRUE.                                                        SYS05940
      NEGI2=.TRUE.                                                      SYS05950
      INT2N=.FALSE.                                                     SYS05960
      SUM2=0.0                                                          SYS05970
      QUART2=0                                                          SYS05980
C                                                                       SYS05990
C.................SIMILARLY FOR BLUE BRANCH                            SYS06000
C                                                                       SYS06010
  295 IF(QUART3.LT.QCYC) GOTO 305                                       SYS06020
      IF(SUM3.LT.PLIM3) GOTO 300                                        SYS06030
      IF(NEGI3) GOTO 305                                                SYS06040
      ON3=.TRUE.                                                        SYS06050
      POSI3=.TRUE.                                                      SYS06060
      INT3P=.FALSE.                                                     SYS06070
      SUM3=0.0                                                          SYS06080
      QUART3=0                                                          SYS06090
  300 IF(SUM3.GT.NLIM3) GOTO 305                                        SYS06100
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      IF(POSI3) GOTO 305                                                SYS06110
      ON3=.TRUE.                                                        SYS06120
      NEGI3=.TRUE.                                                      SYS06130
      INT3N=.FALSE.                                                     SYS06140
      SUM3=0.0                                                          SYS06150
      QUART3=0                                                          SYS06160
  305 CONTINUE                                                          SYS06170
      WRITE(6,796) ON1,ON2,ON3,POSI1,POSI2,POSI3,INT1N,INT2N,INT3N,     SYS06180
     +NEGI1,NEGI2,NEGI3,INT1P,INT2P,INT3P                               SYS06190
      IF(POSI1.AND.NEGI1) GOTO 150                                      SYS06200
      IF(POSI2.AND.NEGI2) GOTO 150                                      SYS06210
      IF(POSI3.AND.NEGI3) GOTO 150                                      SYS06220
  310 CONTINUE                                                          SYS06230
C                                                                       SYS06240
C.................CALCULATE THE 'HALF STEP' VALUES NEEDED FOR          SYS06250
C                 THE RUNGE-KUTTA PROCESS                               SYS06260
C                                                                       SYS06270
C                 SIMPLE LINEAR INTERPOLATION IS USED                   SYS06280
C                                                                       SYS06290
C                                                                       SYS06300
C.................SYSTEM VOLTAGE                                       SYS06310
C                                                                       SYS06320
      HVSA= VSA(I) + ((VSA(I+1) + VSA(I))/2.0)                          SYS06330
      HVSB= VSB(I) + ((VSB(I+1) + VSB(I))/2.0)                          SYS06340
      HVSC= VSC(I) + ((VSC(I+1) + VSC(I))/2.0)                          SYS06350
C                                                                       SYS06360
C.................PER-UNIT FURNACE CURRENT                             SYS06370
C                                                                       SYS06380
      HIR= IR(I) + ((IR(I+1) + IR(I))/2.0)                              SYS06390
      HIY= IY(I) + ((IY(I+1) + IY(I))/2.0)                              SYS06400
      HIB= IB(I) + ((IB(I+1) + IB(I))/2.0)                              SYS06410
C                                                                       SYS06420
C.................PER-UNIT FURNACE CURRENT GRADIENT                    SYS06430
C                                                                       SYS06440
      HDIR= DIR(I) + ((DIR(I+1) + DIR(I))/2.0)                          SYS06450
      HDIY= DIY(I) + ((DIY(I+1) + DIY(I))/2.0)                          SYS06460
      HDIB= DIB(I) + ((DIB(I+1) + DIB(I))/2.0)                          SYS06470
C                                                                       SYS06480
C.................SET ZERO VALUES FOR RED BRANCH CURRENT  ILC1         SYS06490
C                                    &  RED BRANCH DI/DT    DILC1       SYS06500
C                 IF THE BRANCH IS 'OFF' OR IF THIS IS THE FIRST STEP   SYS06510
C                 FOR THE 'ON' COMPENSATOR.                             SYS06520
C                                                                       SYS06530
      IF(ON1) GOTO 315                                                  SYS06540
          DILC1(I)=0.0                                                  SYS06550
          ILC1(I)=0.0                                                   SYS06560
          GOTO 320                                                      SYS06570
  315 K1=K1+1                                                           SYS06580
      IF(K1.EQ.1) ILC1(I)=0.0                                           SYS06590
  320 CONTINUE                                                          SYS06600
C                                                                       SYS06610
C.................SIMILARLY FOR YELLOW                                 SYS06620
C                                                                       SYS06630
      IF(ON2) GOTO 325                                                  SYS06640
          DILC2(I)=0.0                                                  SYS06650
          ILC2(I)=0.0                                                   SYS06660
          GOTO 330                                                      SYS06670
  325 K2=K2+1                                                           SYS06680
      IF(K2.EQ.1) ILC2(I)=0.0                                           SYS06690
C     WRITE(6,895)                                                      SYS06700
C     WRITE(6,777) LC,I,VLC2(I),DILC2(I),ILC2(I)                        SYS06710
C 777 FORMAT(5H  LC=,F8.6,9H & FOR I=,I3,6H VLCY=,F8.5,7H DILC2=,F8.5,  SYS06720
C    +6H ILC2=,F8.5)                                                    SYS06730
  330 CONTINUE                                                          SYS06740
C                                                                       SYS06750
C.................SIMILARLY FOR BLUE                                   SYS06760
C                                                                       SYS06770
      IF(ON3) GOTO 335                                                  SYS06780
          DILC3(I)=0.0                                                  SYS06790
          ILC3(I)=0.0                                                   SYS06800
          GOTO 340                                                      SYS06810
  335 K3=K3+1                                                           SYS06820
      IF(K3.EQ.1) ILC3(I)=0.0                                           SYS06830
  340 CONTINUE                                                          SYS06840
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C                                                                       SYS06850
C.................CALCULATE VALUE FOR COMPENSATOR DI/DT IF THIS IS      SYS06860
C                 THE FIRST STEP FOR CURRENT CONDUCTION                 SYS06870
C                                                                       SYS06880
C.................FOR BRANCH ONE                                       SYS06890
C                                                                       SYS06900
      IF(.NOT.ON1) GOTO 341                                             SYS06910
      DILC1(I)= KL1*(VSA(I)                                             SYS06920
     + - RTOT*(IR(I)-IY(I)+2.0*ILC1(I)-ILC2(I)-ILC3(I))                 SYS06930
     + - LTOT*(DIR(I)-DIY(I)))                                          SYS06940
  341 CONTINUE                                                          SYS06950
C                                                                       SYS06960
C.................FOR BRANCH TWO                                       SYS06970
C                                                                       SYS06980
      IF(.NOT.ON2) GOTO 342                                             SYS06990
      DILC2(I)= KL1*(VSB(I)                                             SYS07000
     + - RTOT*(IY(I)-IB(I)-ILC1(I)+2.0*ILC2(I)-ILC3(I))                 SYS07010
     + - LTOT*(DIY(I)-DIB(I)))                                          SYS07020
  342 CONTINUE                                                          SYS07030
C                                                                       SYS07040
C.................FOR BRANCH THREE                                     SYS07050
C                                                                       SYS07060
      IF(.NOT.ON3) GOTO 343                                             SYS07070
      DILC3(I)= KL1*(VSC(I)                                             SYS07080
     + - RTOT*(IB(I)-IR(I)-ILC1(I)-ILC2(I)+2.0*ILC3(I))                 SYS07090
     + - LTOT*(DIB(I)-DIR(I)))                                          SYS07100
  343 CONTINUE                                                          SYS07110
C                                                                       SYS07120
C.................CALCULATE VALUES FOR V7,V8 & V9 SINCE DILC1,2,3      SYS07130
C                 & ILC1,2,3  ARE NOW KNOWN FOR THIS VALUE OF 'I'       SYS07140
C                                                                       SYS07150
C                                                                       SYS07160
      IF(I.EQ.ICON) GOTO 345                                            SYS07170
      VLC1(I) = VSA(I)-RTOT*(IR(I)-IY(I)                                SYS07180
     +                     + 2.0* ILC1(I) -  ILC2(I) -  ILC3(I))        SYS07190
     +               -LTOT*(DIR(I)-DIY(I)                               SYS07200
     +                     + 2.0*DILC1(I) - DILC2(I) - DILC3(I))        SYS07210
C                                                                       SYS07220
C                                                                       SYS07230
C                                                                       SYS07240
      VLC2(I) = VSB(I)-RTOT*(IY(I)-IB(I)                                SYS07250
     +                     -  ILC1(I) + 2.0* ILC2(I) -  ILC3(I))        SYS07260
     +               -LTOT*(DIY(I)-DIB(I)                               SYS07270
     +                     - DILC1(I) + 2.0*DILC2(I) - DILC3(I))        SYS07280
C                                                                       SYS07290
C                                                                       SYS07300
C                                                                       SYS07310
      VLC3(I) = VSC(I)-RTOT*(IB(I)-IR(I)                                SYS07320
     +                     -  ILC1(I) -  ILC2(I) + 2.0* ILC3(I))        SYS07330
     +               -LTOT*(DIB(I)-DIR(I)                               SYS07340
     +                     - DILC1(I) - DILC2(I) + 2.0*DILC3(I))        SYS07350
C                                                                       SYS07360
C                                                                       SYS07370
C                                                                       SYS07380
C                                                                       SYS07390
C.................CALCULATE THE CONSTANT A,B,C,D FOR THE RUNGE-KUTTA   SYS07400
C                 PROCESS WHICH CALCULATES ILC FROM D ILC/DT.           SYS07410
C                                                                       SYS07420
C                 FIRST SET CALCULATED VARIABLES TO ZERO                SYS07430
C                                                                       SYS07440
  345 CONTINUE                                                          SYS07450
      A1=0.0                                                            SYS07460
      A2=0.0                                                            SYS07470
      A3=0.0                                                            SYS07480
      B1=0.0                                                            SYS07490
      B2=0.0                                                            SYS07500
      B3=0.0                                                            SYS07510
      C1=0.0                                                            SYS07520
      C2=0.0                                                            SYS07530
      C3=0.0                                                            SYS07540
      D1=0.0                                                            SYS07550
      D2=0.0                                                            SYS07560
      D3=0.0                                                            SYS07570
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      A1=TSTEP*DILC1(I)                                                 SYS07580
      A2=TSTEP*DILC2(I)                                                 SYS07590
      A3=TSTEP*DILC3(I)                                                 SYS07600
C                                                                       SYS07610
      IF(.NOT.ON1) GOTO 350                                             SYS07620
      B1 = TSTEP* KL1*(HVSA                                             SYS07630
     +                -RTOT*(HIR-HIY                                   SYS07640
     + +2.0*(ILC1(I)+A1/2.0) - (ILC2(I)+A2/2.0) - (ILC3(I)+A3/3.0))     SYS07650
     +                -LTOT*(HDIR-HDIY))                               SYS07660
      GOTO 355                                                          SYS07670
  350 B1 = 0.0                                                          SYS07680
  355 CONTINUE                                                          SYS07690
C                                                                       SYS07700
      IF(.NOT.ON2) GOTO 360                                             SYS07710
      B2 = TSTEP* KL1*(HVSB                                             SYS07720
     +                -RTOT*(HIY-HIB                                   SYS07730
     + -(ILC1(I)+A1/2.0) +2.0*(ILC2(I)+A2/2.0) - (ILC3(I)+A3/3.0))     SYS07740
     +                -LTOT*(HDIY-HDIB))                               SYS07750
      GOTO 365                                                          SYS07760
  360 B2 = 0.0                                                          SYS07770
  365 CONTINUE                                                          SYS07780
C                                                                       SYS07790
      IF(.NOT.ON3) GOTO 370                                             SYS07800
      B3 = TSTEP* KL1*(HVSC                                             SYS07810
     +                -RTOT*(HIB-HIR                                   SYS07820
     + -(ILC1(I)+A1/2.0) - (ILC2(I)+A2/2.0) +2.0*(ILC3(I)+A3/3.0))     SYS07830
     +                -LTOT*(HDIB-HDIR))                               SYS07840
      GOTO 375                                                          SYS07850
  370 B3 = 0.0                                                          SYS07860
  375 CONTINUE                                                          SYS07870
C                                                                       SYS07880
C                                                                       SYS07890
C                                                                       SYS07900
C                                                                       SYS07910
      IF(.NOT.ON1) GOTO 380                                             SYS07920
      C1 = TSTEP* KL1*(HVSA                                             SYS07930
     +                -RTOT*(HIR-HIY                                   SYS07940
     + +2.0*(ILC1(I)+B1/2.0) - (ILC2(I)+B2/2.0) - (ILC3(I)+B3/3.0))     SYS07950
     +                -LTOT*(HDIR-HDIY))                               SYS07960
      GOTO 385                                                          SYS07970
  380 C1 = 0.0                                                          SYS07980
  385 CONTINUE                                                          SYS07990
C                                                                       SYS08000
      IF(.NOT.ON2) GOTO 390                                             SYS08010
      C2 = TSTEP* KL1*(HVSB                                             SYS08020
     +                -RTOT*(HIY-HIB                                   SYS08030
     + -(ILC1(I)+B1/2.0) +2.0*(ILC2(I)+B2/2.0) - (ILC3(I)+B3/3.0))     SYS08040
     +                -LTOT*(HDIY-HDIB))                               SYS08050
      GOTO 395                                                          SYS08060
  390 C2 = 0.0                                                          SYS08070
  395 CONTINUE                                                          SYS08080
C                                                                       SYS08090
      IF(.NOT.ON3) GOTO 400                                             SYS08100
      C3 = TSTEP* KL1*(HVSC                                             SYS08110
     +                -RTOT*(HIB-HIR                                   SYS08120
     + -(ILC1(I)+B1/2.0) - (ILC2(I)+B2/2.0) +2.0*(ILC3(I)+B3/3.0))     SYS08130
     +                -LTOT*(HDIB-HDIR))                               SYS08140
      GOTO 405                                                          SYS08150
  400 C3 = 0.0                                                          SYS08160
  405 CONTINUE                                                          SYS08170
C                                                                       SYS08180
C                                                                       SYS08190
C                                                                       SYS08200
C                                                                       SYS08210
      IF(.NOT.ON1) GOTO 410                                             SYS08220
      D1 = TSTEP* KL1*(VSA(I+1)                                         SYS08230
     +                -RTOT*(IR(I+1)-IY(I+1)                           SYS08240
     + +2.0*(ILC1(I)+C1) - (ILC2(I)+C2) - (ILC3(I)+C3))                 SYS08250
     +                -LTOT*(DIR(I+1)-DIY(I+1)))                       SYS08260
      GOTO 415                                                          SYS08270
  410 D1 = 0.0                                                          SYS08280
  415 CONTINUE                                                          SYS08290
C                                                                       SYS08300
      IF(.NOT.ON2) GOTO 420                                             SYS08310
      D2 = TSTEP* KL1*(VSB(I+1)                                         SYS08320
     +                -RTOT*(IY(I+1)-IB(I+1)                           SYS08330
     + -(ILC1(I)+C1) +2.0*(ILC2(I)+C2) - (ILC3(I)+C3))                 SYS08340
     +                -LTOT*(DIY(I+1)-DIB(I+1)))                       SYS08350
      GOTO 425                                                          SYS08360
  420 D2 = 0.0                                                          SYS08370
  425 CONTINUE                                                          SYS08380
C                                                                       SYS08390
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      IF(.NOT.ON3) GOTO 430                                              SYS08400
      D3 = TSTEP* KL1*(VSC(I+1)                                          SYS08410
     +                -RTOT*(IB(I+1)-IR(I+1)                              SYS08420
     + -(ILC1(I)+C1) - (ILC2(I)+C2) +2.0*(ILC3(I)+C3))                    SYS08430
     +                -LTOT*(DIB(I+1)-DIR(I+1)))                          SYS08440
      GOTO 435                                                           SYS08450
  430 D3 = 0.0                                                           SYS08460
  435 CONTINUE                                                           SYS08470
C                                                                        SYS08480
C                                                                        SYS08490
C                                                                        SYS08500
C                                                                        SYS08510
C.................CALCULATE THE NEXT COMPENSATOR BRANCH CURRENTS        SYS08520
C                      (RUNGE-KUTTA)                                     SYS08530
C                                                                        SYS08540
      ILC1(I+1)= ILC1(I) + (A1 + 2.0*B1 + 2.0*C1 + D1)/6.0               SYS08550
      ILC2(I+1)= ILC2(I) + (A2 + 2.0*B2 + 2.0*C2 + D2)/6.0               SYS08560
      ILC3(I+1)= ILC3(I) + (A3 + 2.0*B3 + 2.0*C3 + D3)/6.0               SYS08570
C                                                                        SYS08580
C.................CHECK THAT BRANCH CURRENTS ARE ZERO WHEN               SYS08590
C                 FLAGS INDICATE SO                                      SYS08600
C                                                                        SYS08610
      IF(ON1) GOTO 440                                                   SYS08620
      IF(ILC1(I+1).NE.0.0) GOTO 150                                      SYS08630
  440 IF(ON2) GOTO 445                                                   SYS08640
      IF(ILC2(I+1).NE.0.0) GOTO 150                                      SYS08650
  445 IF(ON3) GOTO 450                                                   SYS08660
      IF(ILC3(I+1).NE.0.0) GOTO 150                                      SYS08670
  450 CONTINUE                                                           SYS08680
C                                                                        SYS08690
C.................CALCULATE LINE COMPENSATOR CURRENT VALUES FROM        SYS08700
C                 THE DELTA-CONNECTED BRANCH VALUES                      SYS08710
C                                                                        SYS08720
      ILCR(I+1) = ILC1(I+1) - ILC3(I+1)                                  SYS08730
      ILCY(I+1) = ILC2(I+1) - ILC1(I+1)                                  SYS08740
      ILCB(I+1) = ILC3(I+1) - ILC2(I+1)                                  SYS08750
C                                                                        SYS08760
C.................ALTER FLAGS IF CURRENT ZERO CROSSINGS ARE DETECTED    SYS08770
C                 ( ALSO IF FIRST 'ON' POINT IS THE LAST POINT IN A      SYS08780
C                   HALF CYCLE LEADING TO CONDUCTION IN ALL OF NEXT      SYS08790
C                   HALF CYCLE )                                         SYS08800
C                                                                        SYS08810
      IF(POSI1) GOTO 460                                                 SYS08820
      IF(ILC1(I).LE.0.0.AND.ILC1(I+1).GE.0.0) GOTO 455                   SYS08830
      GOTO 470                                                           SYS08840
  455 NEGI1=.FALSE.                                                      SYS08850
      ON1=.FALSE.                                                        SYS08860
      K1=0                                                               SYS08870
      GOTO 470                                                           SYS08880
  460 IF(ILC1(I).GE.0.0.AND.ILC1(I+1).LE.0.0) GOTO 465                   SYS08890
      GOTO 470                                                           SYS08900
  465 POSI1=.FALSE.                                                      SYS08910
      ON1=.FALSE.                                                        SYS08920
      K1=0                                                               SYS08930
  470 CONTINUE                                                           SYS08940
C                                                                        SYS08950
      IF(POSI2) GOTO 480                                                 SYS08960
      IF(ILC2(I).LE.0.0.AND.ILC2(I+1).GE.0.0) GOTO 475                   SYS08970
      GOTO 490                                                           SYS08980
  475 NEGI2=.FALSE.                                                      SYS08990
      ON2=.FALSE.                                                        SYS09000
      K2=0                                                               SYS09010
      GOTO 490                                                           SYS09020
  480 IF(ILC2(I).GE.0.0.AND.ILC2(I+1).LE.0.0) GOTO 485                   SYS09030
      GOTO 490                                                           SYS09040
  485 POSI2=.FALSE.                                                      SYS09050
      ON2=.FALSE.                                                        SYS09060
      K2=0                                                               SYS09070
  490 CONTINUE                                                           SYS09080
C                                                                        SYS09090
      IF(POSI3) GOTO 500                                                 SYS09100
      IF(ILC3(I).LE.0.0.AND.ILC3(I+1).GE.0.0) GOTO 495                   SYS09110
      GOTO 510                                                           SYS09120
  495 NEGI3=.FALSE.                                                      SYS09130
      ON3=.FALSE.                                                        SYS09140
      K3=0                                                               SYS09150
      GOTO 510                                                           SYS09160
  500 IF(ILC3(I).GE.0.0.AND.ILC3(I+1).LE.0.0) GOTO 505                   SYS09170
      GOTO 510                                                           SYS09180
  505 POSI3=.FALSE.                                                      SYS09190
      ON3=.FALSE.                                                        SYS09200
      K3=0                                                               SYS09210
  510 CONTINUE                                                           SYS09220
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C                                                                       SYS09230
C.................CALCULATE DI/DT FOR THE COMPENSATOR BRANCH CURRENTS.  SYS09240
C                 THESE ARE NECCESSARY FOR THE NEXT RUNGE-KUTTA STEP    SYS09250
C                 ( SINCE  A= TSTEP * DI/DT   ETC. )                    SYS09260
C                 AND THEY ARE NEEDED FOR THE CALCULATION OF VOLTAGES   SYS09270
C                 --- DI/DT(I+1) NOW                                    SYS09280
C                     IS USED AS  DI/DT(I) IN THENEXT RUN THROUGH THE   SYS09290
C                     COMPENSATOR LOOP.                                 SYS09300
C                                                                       SYS09310
C                                                                       SYS09320
  512 CONTINUE                                                          SYS09330
      DILC1(I+1) = KL1*(VSA(I+1)                                        SYS09340
     +                 -RTOT*(  IR(I+1) -  IY(I+1)                    SYS09350
     +                       + 2.0*ILC1(I+1) - ILC2(I+1) - ILC3(I+1))) SYS09360
     +                 -LTOT*( DIR(I+1) - DIY(I+1)))                  SYS09370
C                                                                       SYS09380
C                                                                       SYS09390
      DILC2(I+1) = KL1*(VSB(I+1)                                        SYS09400
     +                 -RTOT*(  IY(I+1) -  IB(I+1)                    SYS09410
     +                       - ILC1(I+1) +2.0*ILC2(I+1) - ILC3(I+1))  SYS09420
     +                 -LTOT*( DIY(I+1) - DIB(I+1)))                  SYS09430
C                                                                       SYS09440
C                                                                       SYS09450
      DILC3(I+1) = KL1*(VSC(I+1)                                        SYS09460
     +                 -RTOT*(  IB(I+1) -  IR(I+1)                    SYS09470
     +                       - ILC1(I+1) - ILC2(I+1) +2.0*ILC3(I+1))  SYS09480
     +                 -LTOT*( DIB(I+1) - DIR(I+1)))                  SYS09490
C                                                                       SYS09500
C                                                                       SYS09510
C.................CALCULATE LINE VALUES FROM BRANCH DI/DT S            SYS09520
C                                                                       SYS09530
C                                                                       SYS09540
      DILCR(I+1) = DILC1(I+1) - DILC3(I+1)                              SYS09550
      DILCY(I+1) = DILC2(I+1) - DILC1(I+1)                              SYS09560
      DILCB(I+1) = DILC3(I+1) - DILC2(I+1)                              SYS09570
C                                                                       SYS09580
C                                                                       SYS09590
      IF(ON1.OR.ON2.OR.ON3) WRITE(6,798) VLC1(I),VLC2(I),VLC3(I),       SYS09600
     +ILC1(I),ILC2(I),ILC3(I),DILC1(I),DILC2(I),DILC3(I)                SYS09610
C                                                                       SYS09620
C                                                                       SYS09630
C.................CALCULATE THE LINE VOLTAGES FOR THE NEXT STEP OF 'I' SYS09640
C                 THIS IS POSSIBLE NOW THAT   ILC(I+1)   &   DILC(I+1) SYS09650
C                 ARE KNOWN.                                            SYS09660
C                                                                       SYS09670
C                                                                       SYS09680
      VLC1(I+1) = VSA(I+1)-RTOT*(IR(I+1)-IY(I+1)                        SYS09690
     +                       + 2.0* ILC1(I+1) -  ILC2(I+1) -  ILC3(I+1)) SYS09700
     +                -LTOT*(DIR(I+1)-DIY(I+1)                         SYS09710
     +                       + 2.0*DILC1(I+1) - DILC2(I+1) - DILC3(I+1)) SYS09720
C                                                                       SYS09730
C                                                                       SYS09740
C                                                                       SYS09750
      VLC2(I+1) = VSB(I+1)-RTOT*(IY(I+1)-IB(I+1)                        SYS09760
     +                       -  ILC1(I+1) + 2.0* ILC2(I+1) -  ILC3(I+1)) SYS09770
     +                -LTOT*(DIY(I+1)-DIB(I+1)                         SYS09780
     +                       - DILC1(I+1) + 2.0*DILC2(I+1) - DILC3(I+1)) SYS09790
C                                                                       SYS09800
C                                                                       SYS09810
C                                                                       SYS09820
      VLC3(I+1) = VSC(I+1)-RTOT*(IB(I+1)-IR(I+1)                        SYS09830
     +                       -  ILC1(I+1) -  ILC2(I+1) + 2.0* ILC3(I+1)) SYS09840
     +                -LTOT*(DIB(I+1)-DIR(I+1)                         SYS09850
     +                       - DILC1(I+1) - DILC2(I+1) + 2.0*DILC3(I+1)) SYS09860
C                                                                       SYS09870
C                                                                       SYS09880
C.................INCREMENT I                                          SYS09890
C                                                                       SYS09900
C                                                                       SYS09910
      I=I+1                                                             SYS09920
C                                                                       SYS09930
C.................CHECK IF 'I' GREATER THAN THE LAST VALUE OF 'I'      SYS09940
C                 PREVIOUSLY SET FOR COMPENSATOR OPERATION              SYS09950
C                                                                       SYS09960
      IF(I.LT.ICOFF) GOTO  515                                          SYS09970
      COMPON = .FALSE.                                                  SYS09980
  515 CONTINUE                                                          SYS09990
      IF(I.LT.POINTS) GOTO 210                                          SYS10000
  520 CONTINUE                                                          SYS10010
```

```
C                                                                       SYS10020
C                                                                       SYS10030
C                                                                       SYS10040
C.................ANALYSIS SECTION                                     SYS10050
C                                                                       SYS10060
C                                                                       SYS10070
C                                                                       SYS10080
C                                                                       SYS10090
      IF(SPEC.OR.SPEC3) CALL FOSPEC(POINTS,1,2048,CVRY)                 SYS10100
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,CVYB)                         SYS10110
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,CVBR)                         SYS10120
      IF(SPEC.OR.SPEC3) CALL FOSPEC(POINTS,1,2048,MVRY)                 SYS10130
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,MVYB)                         SYS10140
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,MVBR)                         SYS10150
      IF(NOPLOT) GOTO 125                                               SYS10160
C                                                                       SYS10170
C.................NPERSQ IS THE NO. OF CYCLES PER PLOTTING SQUARE      SYS10180
C                 IF A LONG PLOT IS OUTPUT.                             SYS10190
C                                                                       SYS10200
      NPERSQ=5                                                          SYS10210
C     LONG=.TRUE.                                                       SYS10220
C                                                                       SYS10230
C                                                                       SYS10240
C                 ********   ********   ********   ********   ********  SYS10250
      DATA TITLA/'FURNACE ','& COMPEN','SATOR LI','NE CURRE','NTS     '/SYS10260
      DATA TITL1A/'IR (KA)','         '/                               SYS10270
      DATA TITL2A/'IY (KA)','         '/                               SYS10280
      DATA TITL3A/'IB (KA)','         '/                               SYS10290
      DATA TITL4A/'ILCR (K','A)       '/                               SYS10300
      DATA TITL5A/'ILCY (K','A)       '/                               SYS10310
      DATA TITL6A/'ILCB (K','A)       '/                               SYS10320
      CALL GRAF6(POINTS,6,IR,IY,IB,ILCR,ILCY,ILCB,                      SYS10330
     +TITLA,TITL1A,TITL2A,TITL3A,TITL4A,TITL5A,TITL6A,LONG,NPERSQ,      SYS10340
     +GINFOB,GINFO2,GINFO3,1.75,1.75,1.75,0.00,0.00,0.00)               SYS10350
C                                                                       SYS10360
C                                                                       SYS10370
C                 ********   ********   ********   ********   ********  SYS10380
      DATA TITLF/'MEASURED',' AND CAL','CULATED ','LINE VOL','TAGES   '/SYS10390
      DATA TITL1F/'VRY M (','KV)      '/                                SYS10400
      DATA TITL2F/'VYB M (','KV)      '/                                SYS10410
      DATA TITL3F/'VBR M (','KV)      '/                                SYS10420
      DATA TITL4F/'VRY C (','KV)      '/                                SYS10430
      DATA TITL5F/'VYB C (','KV)      '/                                SYS10440
      DATA TITL6F/'VBR C (','KV)      '/                                SYS10450
      CALL GRAF6(POINTS,6,MVRY,MVYB,MVBR,CVRY,CVYB,CVBR,                SYS10460
     +TITLF,TITL1F,TITL2F,TITL3F,TITL4F,TITL5F,TITL6F,LONG,NPERSQ,      SYS10470
     +GINFOB,GINFO2,GINFO3,55.0,55.0,55.0,55.0,55.0,55.0)               SYS10480
C                                                                       SYS10490
C                                                                       SYS10500
C                 ********   ********   ********   ********   ********  SYS10510
      DATA TITLE/'COMPENSA','TOR BRAN','CH VOLTA','GES AND ','CURRENTS'/SYS10520
      DATA TITL1E/'VLC1   ','(KV)     '/                               SYS10530
      DATA TITL2E/'VLC2   ','(KV)     '/                               SYS10540
      DATA TITL3E/'VLC3   ','(KV)     '/                               SYS10550
      DATA TITL4E/'ILC1   ','(KA)     '/                               SYS10560
      DATA TITL5E/'ILC2   ','(KA)     '/                               SYS10570
      DATA TITL6E/'ILC3   ','(KA)     '/                               SYS10580
      LONG=.FALSE.                                                      SYS10590
      CALL GRAF6(POINTS,6,VLC1,VLC2,VLC3,ILC1,ILC2,ILC3,                SYS10600
     +TITLE,TITL1E,TITL2E,TITL3E,TITL4E,TITL5E,TITL6E,LONG,NPERSQ,      SYS10610
     +GINFOB,GINFO2,GINFO3,55.0,55.0,55.0,0.00,0.00,0.00)               SYS10620
  125 CONTINUE                                                          SYS10630
C                                                                       SYS10640
C                                                                       SYS10650
```

```
C                                                                       SYS10660
C.............THE FOLLOWING SECTION USES CALLS TO SUBPROGRAM  'DEMOD' .SYS10670
C             THIS SUBPROGRAM USES PREVIOUSLY CALCULATED VALUES OF      SYS10680
C             FREQUENCY AND RMS VALUE TO FIT A TRUE SINUSOID TO THE     SYS10690
C             ARRAY OF TIME-SERIES DATA GIVEN AS THE FIRST PARAMETER.   SYS10700
C                 THE FOURTH PARAMETER SHOULD BE AN ARRAY OF ZEROS ON   SYS10710
C             ENTRY & ON EXIT SHOULD CONTAIN THE 'DEMODULATED' DATA.    SYS10720
C                THE FIFTH PARAMETER SHOULD BE ZERO ON ENTRY & ON EXITSYS10730
C             SHOULD CONTAIN A TIME VALUE USED TO GIVE SYNCHONIISATION.SYS10740
C                                                                       SYS10750
C                                                                       SYS10760
      IF(NODMOD) GOTO 140                                               SYS10770
      TUSED=0.0                                                         SYS10780
      CALL DEMOD(POINTS,MVRY,AVFREQ,VRRMS,DMVRY,TUSED)                  SYS10790
      IF(.NOT.DMOD2) TUSED=0.0                                          SYS10800
      CALL DEMOD(POINTS,CVRY,AVFREQ,CVRRMS,DCVRY,TUSED)                 SYS10810
      TUSED=0.0                                                         SYS10820
      CALL DEMOD(POINTS,MVYB,AVFREQ,VYRMS,DMVYB,TUSED)                  SYS10830
      IF(.NOT.DMOD2) TUSED=0.0                                          SYS10840
      CALL DEMOD(POINTS,CVYB,AVFREQ,CVYRMS,DCVYB,TUSED)                 SYS10850
      TUSED=0.0                                                         SYS10860
      CALL DEMOD(POINTS,MVBR,AVFREQ,VBRMS,DMVBR,TUSED)                  SYS10870
      IF(.NOT.DMOD2) TUSED=0.0                                          SYS10880
      CALL DEMOD(POINTS,CVBR,AVFREQ,CVBRMS,DCVBR,TUSED)                 SYS10890
      IF(SPEC.OR.SPEC3) CALL FOSPEC(POINTS,1,2048,DCVRY)                SYS10900
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,DCVYB)                        SYS10910
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,DCVBR)                        SYS10920
      IF(SPEC.OR.SPEC3) CALL FOSPEC(POINTS,1,2048,DMVRY)                SYS10930
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,DMVYB)                        SYS10940
      IF(SPEC3) CALL FOSPEC(POINTS,1,2048,DMVBR)                        SYS10950
  130 CONTINUE                                                          SYS10960
      IF(NOPLOT) GOTO 140                                               SYS10970
C                                                                       SYS10980
C                                                                       SYS10990
C                 ********   ********   ********   ********   ********  SYS11000
      DATA TITLB/'MEASURED',' AND DEM','ODULATED',' WAVEFOR','MS      '/SYS11010
      DATA TITL1B/'VRY (KV',')       '/                                 SYS11020
      DATA TITL2B/'VYB (KV',')       '/                                 SYS11030
      DATA TITL3B/'VBR (KV',')       '/                                 SYS11040
      DATA TITL4B/'DVRY (K','V)      '/                                 SYS11050
      DATA TITL5B/'DVYB (K','V)      '/                                 SYS11060
      DATA TITL6B/'DVBR (K','V)      '/                                 SYS11070
C     LONG=.TRUE.                                                       SYS11080
      IF(DMOD2) CALL GRAF6(POINTS,6,MVRY,MVYB,MVBR,DMVRY,DMVYB,DMVBR,   SYS11090
     +TITLB,TITL1B,TITL2B,TITL3B,TITL4B,TITL5B,TITL6B,LONG,NPERSQ,      SYS11100
     +GINFO1,GINFO2,GINFO3,55.0,55.0,55.0,15.0,15.0,15.0)               SYS11110
      IF(.NOT.DMOD2) CALL GRAF6(POINTS,6,MVRY,MVYB,MVBR,DMVRY,DMVYB,    SYS11120
     +DMVBR,TITLB,TITL1B,TITL2B,TITL3B,TITL4B,TITL5B,TITL6B,LONG,NPERSQ,SYS11130
     +GINFOB,GINFO2,GINFO3,55.0,55.0,55.0,15.0,15.0,15.0)               SYS11140
C                                                                       SYS11150
C                                                                       SYS11160
C                 ********   ********   ********   ********   ********  SYS11170
      DATA TITLC/'CALCULAT','ED  AND ','DEMODULA','TED WAVE','FORMS   '/SYS11180
      DATA TITL1C/'CVRY    ','(KV)    '/                                SYS11190
      DATA TITL2C/'CVYB  .','(KV)    '/                                SYS11200
      DATA TITL3C/'CVBR    ','(KV)    '/                                SYS11210
      DATA TITL4C/'DCVRY   ','(KV)    '/                                SYS11220
      DATA TITL5C/'DCVYB   ','(KV)    '/                                SYS11230
      DATA TITL6C/'DCVBR   ','(KV)    '/                                SYS11240
C     LONG=.TRUE.                                                       SYS11250
      IF(DMOD2) CALL GRAF6(POINTS,6,CVRY,CVYB,CVBR,DCVRY,DCVYB,DCVBR,   SYS11260
     +TITLC,TITL1C,TITL2C,TITL3C,TITL4C,TITL5C,TITL6C,LONG,NPERSQ,      SYS11270
     +GINFO1,GINFO2,GINFO3,55.0,55.0,55.0,15.0,15.0,15.0)               SYS11280
      IF(.NOT.DMOD2) CALL GRAF6(POINTS,6,CVRY,CVYB,CVBR,DCVRY,DCVYB,    SYS11290
     +DCVBR,TITLC,TITL1C,TITL2C,TITL3C,TITL4C,TITL5C,TITL6C,LONG,NPERSQ,SYS11300
     +GINFOB,GINFO2,GINFO3,55.0,55.0,55.0,15.0,15.0,15.0)               SYS11310
C                                                                       SYS11320
C                                                                       SYS11330
C                 ********   ********   ********   ********   ********  SYS11340
      DATA TITLD/'BOTH DEM','ODULATED',' WAVEFOR','MS      ',','       '/SYS11350
      DATA TITL1D/'DMVRY   ','(KV)    '/                                SYS11360
      DATA TITL2D/'DMVYB   ','(KV)    '/                                SYS11370
      DATA TITL3D/'DMVBR   ','(KV)    '/                                SYS11380
      DATA TITL4D/'DCVRY   ','(KV)    '/                                SYS11390
      DATA TITL5D/'DCVYB   ','(KV)    '/                                SYS11400
      DATA TITL6D/'DCVBR   ','(KV)    '/                                SYS11410
C     LONG=.TRUE.                                                       SYS11420
      IF(.NOT.DMOD2) CALL GRAF6(POINTS,6,DMVRY,DMVYB,DMVBR,DCVRY,DCVYB, SYS11430
     +DCVBR,TITLD,TITL1D,TITL2D,TITL3D,TITL4D,TITL5D,TITL6D,LONG,NPERSQ,SYS11440
     +GINFOB,GINFO2,GINFO3,15.0,15.0,15.0,15.0,15.0,15.0)               SYS11450
      IF(DMOD2) CALL GRAF6(POINTS,6,DMVRY,DMVYB,DMVBR,DCVRY,DCVYB,DCVBR,SYS11460
     +TITLD,TITL1D,TITL2D,TITL3D,TITL4D,TITL5D,TITL6D,LONG,NPERSQ,      SYS11470
     +GINFO1,GINFO2,GINFO3,15.0,15.0,15.0,15.0,15.0,15.0)               SYS11480
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C                                                                       SYS11490
C.................CALLS TO GRAF6 BELOW OUTPUT MANY MORE CYCLES          SYS11500
C                 THAN CAN BE PLOTTED ON THE 'IMLAC' SYSTEM.            SYS11510
C                                                                       SYS11520
C                 THE PLOT CODE MUST BE SENT TO THE DRUM PLOTTER        SYS11530
C                                                                       SYS11540
      GOTO 140                                                          SYS11550
  135 NPERSQ=25                                                         SYS11560
      LONG=.TRUE.                                                       SYS11570
C                                                                       SYS11580
C                                                                       SYS11590
C               ********   ********   ********   ********   ********  SYS11600
      DATA TITLG/'MEASURED',' AND CAL','CULATED ','LINE VOL','TAGES   '/SYS11610
      DATA TITL1G/'VRY M (','KV)     '/                                 SYS11620
      DATA TITL2G/'VRY C (','KV)     '/                                 SYS11630
      DATA TITL3G/'VRY M (','KV)     '/                                 SYS11640
      DATA TITL4G/'VRY C (','KV)     '/                                 SYS11650
      DATA TITL5G/'VRY M (','KV)     '/                                 SYS11660
      DATA TITL6G/'VRY C (','KV)     '/                                 SYS11670
      CALL GRAF6(POINTS,2,MVRY,CVRY,MVRY,CVRY,MVRY,CVRY,                SYS11680
     +TITLG,TITL1G,TITL2G,TITL3G,TITL4G,TITL5G,TITL6G,LONG,NPERSQ,      SYS11690
     +GINFOB,GINFO2,GINFO3,55.0,55.0,55.0,55.0,55.0,55.0)               SYS11700
C                                                                       SYS11710
C                                                                       SYS11720
C               ********   ********   ********   ********   ********  SYS11730
      DATA TITLH/'DEMODULA','TED LINE','VOLTAGES','        ','        '/SYS11740
      DATA TITL1H/'DMVRY (','KV)     '/                                 SYS11750
      DATA TITL2H/'DCVRY (','KV)     '/                                 SYS11760
      DATA TITL3H/'DMVRY (','KV)     '/                                 SYS11770
      DATA TITL4H/'DCVRY (','KV)     '/                                 SYS11780
      DATA TITL5H/'DMVRY (','KV)     '/                                 SYS11790
      DATA TITL6H/'DCVRY (','KV)     '/                                 SYS11800
      CALL GRAF6(POINTS,2,DMVRY,DCVRY,DMVRY,DCVRY,DMVRY,DCVRY,          SYS11810
     +TITLH,TITL1H,TITL2H,TITL3H,TITL4H,TITL5H,TITL6H,LONG,NPERSQ,      SYS11820
     +GINFOB,GINFO2,GINFO3,15.0,15.0,15.0,15.0,15.0,15.0)               SYS11830
C                                                                       SYS11840
C                                                                       SYS11850
C.................END OF MAIN PROGRAM EXEPT FOR FORMAT STATEMENTS       SYS11860
C                                                                       SYS11870
C                                                                       SYS11880
      GOTO 140                                                          SYS11890
  160 WRITE(6,791)                                                      SYS11900
      GOTO 140                                                          SYS11910
  150 WRITE(6,799)                                                      SYS11920
  140 CONTINUE                                                          SYS11930
  999 FORMAT(1H ,3(F10.6,1X),2X,3(F10.7,1X),2X,3(F10.4,1X))             SYS11940
  998 FORMAT(1H ,3(F7.3,1X),1X,3(F7.4,1X),3(1X,F8.3))                   SYS11950
  997 FORMAT(//52H****** CHECK=0 ON EXIT FROM 'VZEROS' -CHANNEL 1 ******) SYS11960
  996 FORMAT(//52H****** CHECK=0 ON EXIT FROM 'VZEROS' -CHANNEL 2 ******) SYS11970
  995 FORMAT(//52H****** CHECK=0 ON EXIT FROM 'VZEROS' -CHANNEL 3 ******) SYS11980
  994 FORMAT(1H ,6(F8.3,2X))                                            SYS11990
  993 FORMAT(///20H  INPUT DATA DETAILS,                                SYS12000
     +/22H -------------------- ,                                       SYS12010
     +/22H -------------------- ,                                       SYS12020
     +///49H                     RED       YELLOW       BLUE ,         SYS12030
     +/50H                  ----------  ----------  ----------,        SYS12040
     +//16H NO. OF ZEROS   ,3(I10,2X),                                  SYS12050
     +//16H NO. OF CYCLES  ,3(I10,2X),                                  SYS12060
     +//16H     FREQUENCY  ,3(F10.2,2X),///)                           SYS12070
  992 FORMAT(//13H     POINTS =,I5,//)                                  SYS12080
  991 FORMAT(//46H   SENSE OF CROSSING POINTS...+1 = +'VE GRADT.,       SYS12090
     +/46H  ------------------------    0 = UNDEFINED  ,               SYS12100
     +/46H                             -1 = -'VE GRADT ,               SYS12110
     +//59H         ----------DATA---------     ----------CALC---------, SYS12120
     +/55H  J         R      Y      B             R      Y      B,/)   SYS12130
  990 FORMAT(1H ,I2,8X,I2,5X,I2,5X,I2,12X,I2,5X,I2,5X,I2)               SYS12140
  899 FORMAT(/////////9H LOOP NO.,I2,11H    DELTA =,F8.4,5H RADS,       SYS12150
     +/21H ----------    ERROR=,F9.5,17H RADS AND AVSUM =,F10.5)        SYS12160
  898 FORMAT(1H ,I4,5(F9.5))                                            SYS12170
```

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897 FORMAT(1H ,F6.4,4X,F7.5,4X,I2,7(5X,L1))                                    SYS12180
896 FORMAT(//30X,25H     **********,                                           SYS12190
   +/30X,25H     **********,                                                  SYS12200
   +/30X,25H     * PROGRAM RUN FOR  *,                                        SYS12210
   +/30X,25H     *                  *,                                        SYS12220
   +/30X,15H     *  TSTEP =,F7.5,3H  *,                                       SYS12230
   +/30X,15H     *  LIMIT =,F7.5,3H  *,                                       SYS12240
   +/30X,15H     *  LOOPS =,I3,7H      *,                                     SYS12250
   +/30X,16H     *   LIST = ,L1,8H       *,                                   SYS12260
   +/30X,16H     *   PLOT = ,L1,8H       *,                                   SYS12270
   +/30X,16H     *   LONG = ,L1,8H       *,                                   SYS12280
   +/30X,16H     *   SPEC = ,L1,8H       *,                                   SYS12290
   +/30X,16H     *  SPEC3 = ,L1,8H       *,                                   SYS12300
   +/30X,16H     *   DMOD = ,L1,8H       *,                                   SYS12310
   +/30X,16H     *   DMOD2= ,L1,8H       *,                                   SYS12320
   +/30X,25H     *                  *,                                        SYS12330
   +/30X,25H     *                  *)                                        SYS12340
895 FORMAT(//48H   THIS IS THE TEST LINE $$$$$$$$$$ $$$$$$$$$$)               SYS12350
894 FORMAT(//23H   $$$$$$$$$$$$  LABEL ,I4,15H  $$$$$$$$$$$$$)                SYS12360
893 FORMAT(//1H ,6(F10.4,2X),/15X,3(F10.4,5X))                                 SYS12370
892 FORMAT(//1H ,2X,2HVR,12X,2HVY,12X,2HVB,12X,2HIR,12X,2HIY,12X,2HIB,         SYS12380
   +/53H                    V7             V8             V9 )               SYS12390
891 FORMAT(//53HJ & ZERO CROSSING TIMES ..... R,RCALC,Y,YCALC,B,BCALC)         SYS12400
890 FORMAT(1H ,I2,4X,3(F9.5,2X,F9.5,4X))                                       SYS12410
800 FORMAT(72X)                                                                SYS12420
799 FORMAT(52H   ******* FLAG ERROR IN COMPENSATOR SECTION *******)            SYS12430
798 FORMAT(1H ,3(F9.4,3X),3(F9.4,2X),/37X,3(F9.4,2X))                          SYS12440
797 FORMAT(6H SUM1=,F9.3,6H SUM2=,F9.3,6H SUM3=,F9.3,                          SYS12450
   +10H   QUART1=,I2,8H QUART2=,I2,8H QUART3=,I2)                              SYS12460
796 FORMAT(10H    ON1 = ,L1,10H    ON2 = ,L1,10H    ON3 = ,L1,                 SYS12470
   +3X,10H  POSI1 = ,L1,10H  POSI2 = ,L1,10H  POSI3 = ,L1,                     SYS12480
   +/10H  INT1N = ,L1,10H  INT2N = ,L1,10H  INT3N = ,L1,                       SYS12490
   +3X,10H  NEGI1 = ,L1,10H  NEGI2 = ,L1,10H  NEGI3 = ,L1,                     SYS12500
   +/10H  INT1P = ,L1,10H  INT2P = ,L1,10H  INT3P = ,L1)                       SYS12510
795 FORMAT(1H ,F7.5,4X,F7.1,4X,F7.1,4X,I5,4X,I5)                               SYS12520
794 FORMAT(1H ,8A8)                                                            SYS12530
793 FORMAT(30X,25H     *  COMPENSATOR     *,                                   SYS12540
   +/30X,25H     *     DETAILS:     *,                                        SYS12550
   +/30X,25H     *                  *,                                        SYS12560
   +/30X,16H     *    LC  = ,F7.5,3H  *,                                      SYS12570
   +/30X,16H     *  POSLIM= ,F7.1,3H  *,                                      SYS12580
   +/30X,16H     *  NEGLIM= ,F7.1,3H  *,                                      SYS12590
   +/30X,16H     *   ICON = ,I5,5H    *,                                     SYS12600
   +/30X,16H     *   ICOFF= ,I5,5H    *,                                     SYS12610
   +/30X,25H     **********,                                                  SYS12620
   +/30X,25H     **********///)                                               SYS12630
792 FORMAT(//' GINFO2 : ',8A8/' GINFO3 : ',8A8//)                              SYS12640
791 FORMAT(//50H  ******  ILLEGAL INPUT OPTION COMBINATION  ******)            SYS12650
    STOP                                                                       SYS12660
    END                                                                        SYS12670
```

APPENDIX K

TWELVE-PULSE TCR CONTROL PROGRAM LISTING

```
                        NAME    thyristor_firing_routine
                        NOLIST  CON

                        GLOBAL  firBsub
                        GLOBAL  CODEBASEGG, DATABASEGG, CONSTBASEGG

                        ASSUME DS:DATABASEGG

                        SECTION pascalprocedure, CLASS=INSTRGG


                ;xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
                ;assembley routine to fire thyristors..... 12-pulse
                ;called from main prog after voltage zero detected
                ;algorithm subtracts sine value from measured value and integrates
                ;testing value against a limit.Fires thy. when limit reached
                ;
                ;only outputs a short pulse for thyristor firing
                ;
                ;loop delay values set to values suitable ror no1 compensator.Values
                ;for the other two compensators must be set in RAM after download
                ;
                ;
                ;positive half cycle
                ;?
                firBsub                         ;12-pulse thyristor firing routine
00000000 8D360000 R     fire1   LEA SI, sine1   ;positive half cycle section
00000004 33DB                   XOR BX, BX
00000006 B507                   MOV CH, £07H
00000008 BA00F8         start1  MOV DX, £0F800H ;load address of adc
0000000B EF                     OUT DX, AX      ;initiate conversion
0000000C B10F                   MOV CL, £0FH    ;conversion delay
0000000E D2E9                   SHR CL, CL
00000010 32E4                   XOR AH, AH      ;set ah to zero
00000012 EC                     IN AL, DX       ;input sample
00000013 B109                   MOV CL, £09H    ;loop delay to adjust sampling frequency
00000015 D2E9                   SHR CL, CL      ;sine curve based on 74 usecs sample time
00000017 80FD00                 CMP CH, £00H    ;test whether one of first nine samples
0000001A 7402                   JE lab1         ;jump to lab1 if after nine samples
0000001C FECD                   DEC CH
0000001E 8A0C           lab1    MOV CL, [SI]    ;mov current value of sine curve from memory
00000020 3AC1                   CMP AL, CL      ;decide whether?sample ( sine, jmp to neg1--;
00000022 7207                   JB neg1         ;  -- if it is.
00000024 2AC1                   SUB AL, CL      ;subtract sine from sample
00000026 03D8           add1    ADD BX, AX      ;add difference to summation store
00000028 E90C00                 JMP con1
0000002B 2AC8           neg1    SUB CL, AL      ;CL)AL , subtract AL from CL
0000002D 8AC1                   MOV AL, CL      ;put difference into AL
0000002F 3BD8                   CMP BX, AX      ;test AX against BX--if AX)BX make AX=BX so
00000031 7702                   JA sub1         ;that BX is set to zero in the subtraction
00000033 8BC3                   MOV AX, BX
```

```
 53  00000035 2BD8          sub1    SUB BX,AX
 54  00000037 81FE7C10      cont    CMP SI,£107CH           ;test SI for >  60 degrees
 55  0000003B 7208                  JB  next                ;sample again if SI <  60 degrees
 56  0000003D 81FEBF10              CMP SI,£10BFH           ;test SI for < 150 degrees
 57  00000041 7716                  JA lab2                 ;if > 150 degrees disallow 1st pulse
 58  00000043 81FB0001              CMP BX,£0100H           ;test BX against first limit
 59  00000047 7703                  JA firea                ;jump to firea when limit exeeded
 60  00000049 46            next    INC SI                  ;update pointer to sine curve
 61  0000004A EBBC                  JMP start1
 62  0000004C BA00F0        firea   MOV DX,£0F000H          ;fire thyristor...one short pulse
 63  0000004F B001                  MOV AL,£01H
 64  00000051 EE                    OUT DX,AL
 65  00000052 B110                  MOV CL,£10H
 66  00000054 D2E9                  SHR CL,CL
 67  00000056 B000                  MOV AL,£00H
 68  00000058 EE                    OUT DX,AL
 69
 70                                                     ;continue the integration process until a
 71                                                     ;2nd limit gives a 2nd firing pulse
 72
 73  00000059 BA00F8        lab2    MOV DX,£0F800H          ;get next sample
 74  0000005C EF                    OUT DX,AX               ;
 75  0000005D B10F                  MOV CL,£0FH             ;
 76  0000005F D2E9                  SHR CL,CL               ;
 77  00000061 32E4                  XOR AH,AH               ;
 78  00000063 EC                    IN AL,DX                ;
 79  00000064 B109                  MOV CL,£09H             ;sample loop delay
 80  00000066 D2E9                  SHR CL,CL               ;
 81  00000068 3C87                  CMP AL,£87H             ;test for end of half-cycle
 82  0000006A 7235                  JB end1                 ;
 83  0000006C 8A0C                  MOV CL,[SI]             ;mov current value of sine curve from memory
 84  0000006E 3AC1                  CMP AL,CL               ;if?sample < sine, jmp to neg1
 85  00000070 7207                  JB neg2                 ;
 86  00000072 2AC1                  SUB AL,CL               ;subtract sine from sample
 87  00000074 03D8          add2    ADD BX,AX               ;add difference to summation store
 88  00000076 E90C00                JMP cont2
 89  00000079 2AC8          neg2    SUB CL,AL               ;CL>AL , subtract AL from CL
 90  0000007B 8AC1                  MOV AL,CL               ;put difference into AL
 91  0000007D 3BD8                  CMP BX,AX               ;test AX against BX--if AX>BX make AX=BX so
 92  0000007F 7702                  JA sub2                 ;that BX is set to zero in the subtraction
 93  00000081 8BC3                  MOV AX,BX
 94  00000083 2BD8          sub2    SUB BX,AX
 95  00000085 81FE9310      cont2   CMP SI,£1093H           ;test SI for >  90 degrees
 96  00000089 7206                  JB  next2               ;sample again if SI <  90 degrees
 97  0000008B 81FB0002              CMP BX,£0200H           ;test BX against second limit
 98  0000008F 7703                  JA fireb                ;jump to fireb when 2nd limit exeeded
 99  00000091 46            next2   INC SI                  ;update pointer to sine curve
100  00000092 EBC5                  JMP lab
101  00000094 BA00F0        fireb   MOV DX,£0F000H          ;fire thyristor...one short pulse
102  00000097 B004                  MOV AL,£04H
103  00000099 EE                    OUT DX,AL
104  0000009A B110                  MOV CL,£10H
```

```
105  0000009C D2E9                    SHR CL,CL
106  0000009E B000                    MOV AL,£00H
107  000000A0 EE                      OUT DX,AL
108
109  000000A1 BA00F8          end1    MOV DX,£0F800H          ;load adc address and input sample
110  000000A4 EF                      OUT DX,AX
111  000000A5 B10F                    MOV CL,£0FH
112  000000A7 D2E9                    SHR CL,CL
113  000000A9 EC                      IN AL,DX
114  000000AA 3C80                    CMP AL,£80H             ;check for zero crossing
115  000000AC 77F3                    JA end1
116
117
118                                   ;same integration process is followed
119                                   ;for the negetive half cycle
120
121
122  000000AE 8D368500 R      fire3   LEA SI,sine2            ;neg half cycle routine  Basically same as---
123  000000B2 33DB                    XOR BX,BX               ;--positive half cycle routine except---
124  000000B4 B509                    MOV CH,£09H             ;--a positive contribution to summation--
125  000000B6 BA00F8          start3  MOV DX,£0F800H          ;--store results from AL being ----
126  000000B9 EF                      OUT DX,AX               ;--numerically smaller than sine curve--
127  000000BA B10F                    MOV CL,£0FH             ;--to allow for fact that zero volts---
128  000000BC D2E9                    SHR CL,CL               ;--corresponds to an adc output of 128.
129  000000BE 32E4                    XOR AH,AH
130  000000C0 EC                      IN AL,DX
131  000000C1 B108                    MOV CL,£08H             ;loop delay to adjust sampling freqency
132  000000C3 D2E9                    SHR CL,CL               ;sine curve based on 74usecs sample time
133  000000C5 80FD00                  CMP CH,£00H
134  000000C8 7402                    JE lab3
135  000000CA FECD                    DEC CH
136  000000CC 8AC8            lab3    MOV CL,[SI]
137  000000CE 3AC1                    CMP AL,CL
138  000000D0 7208                    JB pos3
139  000000D2 2AC1                    SUB AL,CL
140  000000D4 3BD8                    CMP BX,AX
141  000000D6 7702                    JA sub3
142  000000D8 8BC3                    MOV AX,BX
143  000000DA 2BD8            sub3    SUB BX,AX
144  000000DC E90600                  JMP cont3
145  000000DF 2AC8            pos3    SUB CL,AL
146  000000E1 8AC1                    MOV AL,CL
147  000000E3 03D8            add3    ADD BX,AX
148  000000E5 81FE0111        cont3   CMP SI,£110H            ;past 240 degrees
149  000000E9 720C                    JB next3
150  000000EB 81FE3D01                CMP SI,£13DH            ;before 330 degrees
151  000000EF 7716                    JA lab4
152  000000F1 81FB0001                CMP BX,£0100            ;test BX against first limit
153  000000F5 7703                    JA fire
154  000000F7 46              next3   INC SI
155  000000F8 EBBC                    JMP start3
156  000000FA BA00F0          fire    MOV DX,£0F000H          ;fire thyristor...one short pulse
```

```
157  000000FD B002                MOV AL,£02H
158  000000FF EE                  OUT DX,AL
159  00000100 B110                MOV CL,£10H
160  00000102 D2E9                SHR CL,CL
161  00000104 B000                MOV AL,£00H
162  00000106 EE                  OUT DX,AL
163
164                                                    ;integration can continue for 2nd pulse
165                                                    ;in negative half-cycle
166
167  00000107 BA00F8      lab4    MOV DX,£0F800H      ;--store results from AL being ----
168  0000010A EF                  OUT DX,AX           ;--numerically smaller than sine curve--
169  0000010B B10F                MOV CL,£0FH         ;--to allow for fact that zero volts---
170  0000010D D2E9                SHR CL,CL           ;--corresponds to an adc output of 128.
171  0000010F 32E4                XOR AH,AH
172  00000111 EC                  IN AL,DX
173  00000112 B108                MOV CL,£08H         ;loop delay to adjust sampling freqency
174  00000114 D2E9                SHR CL,CL           ;sine curve based on 74usecs sample time
175  00000116 3C73                CMP AL,£73H         ;
176  00000118 7735                JA end3             ;check for end of half-cycle
177  0000011A 8A0C                MOV CL,[SI]
178  0000011C 3AC1                CMP AL,CL
179  0000011E 720D                JB pos4
180  00000120 2AC1                SUB AL,CL
181  00000122 3BD8                CMP BX,AX
182  00000124 7702                JA sub4
183  00000126 8BC3                MOV AX,BX
184  00000128 2BD8      sub4      SUB BX,AX
185  0000012A E90600              JMP cont4
186  0000012D 2AC8      pos4      SUB CL,AL
187  0000012F 8AC1                MOV AL,CL
188  00000131 03D8      add4      ADD BX,AX
189  00000133 81FE1811  cont4     CMP SI,£1118H       ;past 270 degrees ?
190  00000137 7206                JB next4
191  00000139 81FB0002            CMP BX,£0200H       ;test BX against second limit
192  0000013D 7705                JA fired
193  0000013F 46        next4     INC SI
194  00000140 EBC5                JMP lab4
195  00000142 BA00F0    fired     MOV DX,£0F000H      ;fire thyristor...one short pulse
196  00000145 B000                MOV AL,£00H
197  00000147 EE                  OUT DX,AL
198  00000148 B110                MOV CL,£10H
199  0000014A D2E9                SHR CL,CL
200  0000014C B000                MOV AL,£00H
201  0000014E EE                  OUT DX,AL
202
203
204  0000014F BA00F8    end3      MOV DX,£0F800H      ;load adc address and input sample
205  00000152 EC                  OUT DX,AX
206  00000153 B10F                MOV CL,£0FH
207  00000155 D2E9                SHR CL,CL
208  00000157 EC                  IN AL,DX
```

```
   209  00000158 3C80              CMP AL,£80H             ;check for pos going zero crossing
   210  0000015A 72F3              JB end3
   211  0000015C E9A1FE            JMP firel               ;--cycle routine.
   212  0000015F C20400            RET £4
   213
   214
   215
   216
   217                            SECTION sdk88.const,CLASS=DATA@@
   218
   219                                                    ; reference sine wave ...      zero = 127
   220                                                    ;                          plus/minus  105
   221                                                    ;                       first sample at 100us
   222                                                    ;                       subsequent dt = 75us
   223                                                    ;                    pts per 1/2 cyc = 132
   224
   225  00000000 82848789          sine1           BYTE    130,132,135,137,140,142,144,147,149,151,153,156,158
                 8C8E9093
                 9597999C
                 9E
   226  0000000D A0A2A5A7          BYTE    160,162,165,167,169,171,173,175,177,179,181,183,185
                 A9ABADAF
                 B1B3B5B7
                 B9
   227  0000001A BBBDBFC1          BYTE    187,189,191,193,194,196,198,199,201,203,204,206,207
                 C2C4C6C7
                 C9CBCCCE
                 CF
   228  00000027 D0D2D3D4          BYTE    208,210,211,212,213,215,216,217,218,219,220,221,221
                 D5D7D8D9
                 DADBDCDD
                 DD
   229  00000034 DEDFDFE0          BYTE    222,223,223,224,225,225,226,226,226,236,227,227,227
                 E1E1E2E3
                 E3ECE3E3
                 E3
   230  00000041 E3E3E3E3          BYTE    227,227,227,227,227,226,226,226,225,225,224,224,223
                 E3E2E2E2
                 E1E1E0E0
                 DF
   231  0000004E DFDEDDDC          BYTE    223,222,221,220,219,218,217,216,215,214,213,212,211
                 DBDAD9D8
                 D7D6D5D4
                 D3
   232  0000005B D1D0CECD          BYTE    209,208,206,205,204,202,200,199,197,195,194,192,190
                 CCCACBC9
                 C8C6C2C0
                 BE
   233  00000068 BCBAB9B7          BYTE    188,186,185,183,181,179,177,174,172,170,168,166,164
                 B5B3B1AF
                 ACAAA8A6
                 A4
```

actually 100

```
234  00000075 A29F9D9B                    BYTE    162, 159, 157, 155, 153, 150, 148, 146, 143, 141, 139, 136, 134
                  99969493
                  8F8D8B88
                  86
235  00000082 84817F                      BYTE    132, 129, 127
236
237
238  00000085 7C7A7775        sine2       BYTE    124, 122, 119, 117, 114, 112, 110, 107, 105, 103, 101, 98, 96
                  72706E6B
                  69676562
                  60
239  00000092 5E5C5957                    BYTE    94, 92, 89, 87, 85, 83, 81, 79, 77, 75, 73, 71, 69
                  5553514F
                  4D4B4947
                  45
240  0000009F 43413F3D                    BYTE    67, 65, 63, 61, 60, 58, 56, 55, 53, 51, 50, 48, 47
                  3C3A3837
                  35333230
                  2F
241  000000AC 2E2C2B2A                    BYTE    46, 44, 43, 42, 41, 39, 38, 37, 36, 35, 34, 33, 33
                  29272625
                  24232221
                  21
242  000000B9 201F1F1E                    BYTE    32, 31, 31, 30, 29, 29, 28, 28, 28, 28, 27, 27, 27
                  1D1D1C1C
                  1C1C1B1B
                  1B
243  000000C6 1B1B1B1B                    BYTE    27, 27, 27, 27, 27, 28, 28, 28, 29, 29, 30, 30, 31
                  1B1C1C1C
                  1D1D1E1E
                  1F
244  000000D3 1F202122                    BYTE    31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43
                  23242526
                  2728292A
                  2B
245  000000E0 2D2E3031                    BYTE    45, 46, 48, 49, 50, 52, 54, 55, 57, 59, 60, 62, 64
                  32343637
                  3938B3C3E
                  40
246  000000ED 42444547                    BYTE    66, 68, 69, 71, 73, 75, 77, 80, 82, 84, 86, 88, 90
                  494B4D50
                  52545658
                  5A
247  000000FA 5C5F6163                    BYTE    92, 95, 97, 99, 101, 104, 106, 108, 111, 113, 115, 118, 120
                  65686A6D
                  6F717376
                  78
248  00000107 7A7D7F                      BYTE    122, 125, 127
249
250
251 ;
```

```
Section = SDK88.CONST, Class = DATAQQ, Aligned to 00000010, Size = 0000010A

SINE1------------00000000     SINE2------------00000085

Section = PASCALPROCEDURE, Class = INSTRQQ, Aligned to 00000010, Size = 00000162

ADD1-------------00000026     ADD2-------------00000074     ADD3-------------000000E3     ADD4-------------00000131
CONT-------------00000037     CONT2------------00000085     CONT3------------000000E5     CONT4------------00000133
END1-------------000000A1     END3-------------0000014F     FIRBSUB----------00000000 G   FIRE1------------00000000
FIRE3------------000000AE     FIREA------------0000004C     FIREB------------00000074     FIREC------------000000FA
FIRED------------00000142     LAB1-------------0000001E     LAB2-------------00000059     LAB3-------------000000CC
LAB4-------------00000107     NEG1-------------0000002B     NEG2-------------00000079     NEXT-------------00000049
NEXT2------------00000091     NEXT3------------000000F7     NEXT4------------0000013F     POS3-------------000000DF
POS4-------------00000120     START1-----------00000000     START3-----------000000B6     SUB1-------------00000035
SUB2-------------00000083     SUB3-------------000000DA     SUB4-------------00000128

Section = %FIREBOBJ, Aligned to 00000010, Size = EMPTY



Unbound Globals

CODEBASEQQ-------00000000     CONSTBASEQQ------00000000     DATABASEQQ-------00000000


  251 Lines Read
  251 Lines Processed
    0 Errors
```

APPENDIX L

PUBLISHED PAPERS

L.I Reference [66]

MODELLING OF AN ELECTRIC ARC FURNACE

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INTRODUCTION

Electric arc furnaces provide a clean and efficient way of melting scrap metal for the production of steel, but they are well known for the effects that they can have on the supply system, particularly voltage fluctuations and consequent tungsten filament lamp flicker. There is considerable interest in the use of shunt compensators for the control of these voltage variations, and a number of methods such as saturated reactors and thyristor controlled devices have been employed. One of the requirements of such equipment is that it should have a good speed of response[1],[2] and the work on modelling described in this paper is part of an investigation of the advantages to be gained by the use of increased phase numbers for thyristor controlled shunt reactors.

It is naturally desirable in such a programme to be able to model the furnace and supply system, both experimentally and theoretically, in order to assess the merits of the different control configurations, but the random nature of the arc currents makes this a difficult task. Whilst a number of authors have described theoretical models[3], very little is reported in the literature on the experimental modelling. Dugan[4] describes a model using a transient network analyser with a harmonic current source to represent the furnace. However, as the author indicates this model does not attempt to incorporate the random nature of the current variations. Investigations by Dixon[5] and others suggest that the pattern of variations produced by arc furnaces is almost independent of rating, which implies that results based on one particular furnace are likely to be applicable to others.

The model described in this paper makes use of the recorded current waveforms of a working furnace, thus introducing the necessary random current variations which are needed to judge the compensator performance.

Nature of the experimental model

The basic concept on which the model is based is that the furnace be represented by a current sink which has a terminal current characteristic similar to that of a working furnace, whilst the electrical supply is represented by a constant voltage in series with a lumped parameter system impedance. The presence of transformers in the supply network, particularly those with star-delta connections, generates a coupling[6] between phases which, whilst it can be ignored for balanced sinusoidal operation, is important for the unbalanced non sinusoidal currents of the arc furnace. This is a topic for which there appears to be little information available and one which needs further work. It is incorporated into the model by the use of a star-delta connected transformer in the supply system, although it is recognised that the transformer used may well not be an accurate representation of the full sized device. This coupling between phases means that the furnace and system must be modelled as a three phase unit rather than one single phase model. The ratio of reactance to resistance of a typical supply network (Q factor) is high and the requirement to achieve a similarly high value of Q in the model demands the use of linear iron cored inductors and suitable values of base current and voltage. These base values impose constraints on the choice of current sink, but the availability of high power electronic amplifiers, such as those used in electro-mechanical vibrators, means that these requirements can be achieved, making direct coupled electronic amplifiers the most convenient form of current sink. The driving or input signal to the amplifiers could be derived in a number of ways. For example the current waveform of a furnace could be subjected to a spectral analysis and the input signal then synthesised using a random but weighted combination of the frequencies found in the waveform spectrum. The approach adopted for this work is to use waveforms recorded on a working furnace as the driving signal, and to this end records made by the CEGB with the co-operation of the steel makers have been made available to the authors, in the form of digitised data on magnetic tape. The information has been transferred to a main frame computer, enabling short sections to be chosen at will and transferred to the bench top model, described in detail in the next section. This form of data handling has been used, since it also allows computational analysis of the recorded data and easy access for comparison with the results of a computational model, work which is progressing in parallel with the experimental modelling.

The nature of this current sink means that whatever one does to the system voltage or impedance the current at the terminals of the furnace model will always be an exact copy of the recorded current. Thus when a compensator is connected to the model the arc furnace currents will remain unchanged. Since the recorded data is that of a furnace operating without a compensator this approach will neglect the small changes that will arise in furnace current due to the action of the compensator. However, the random nature of the furnace currents means that it is doubtful whether these changes could be quantified, but naturally the currents seen by the supply system, and consequently the system voltages, will change when a compensator is fitted.

Details of the model

The model is based on the Templeborough Plant of British Steel Ltd., figure 1 shows the salient features of the supply system. The recordings of phase voltage and current were taken at the 33k bus bar by the CEGB using their D.R.F.A.M.[2] equipment and for the recordings used in this paper furnace 2 was in operation. Following transfer of this data to the main frame computer at Liverpool short sections of recording can be selected at will and transferred to the model by paper tape, where it is held in RAM (figure 2). The time span of data held in the model is dependent upon the size of the memory, and at present is limited to 10 cycles, but it is intended to extend this soon. In addition to the three phase currents one of the voltages is also held in the memory and this

can be displayed for comparison with the measured model voltage.

Synchronisation of the currents to the voltage is achieved in two stages, whilst selecting the data in the mainframe computer the values of current at the instant of red phase voltage zero are identified and subsequently loaded into known memory location in the RAM.

The phase locked loop (fig. 2) circuit generates two interrupt signals, one of which is at 50Hz and coincides with the zero crossing of the red phase voltage. This is used to output the appropriate values of phase currents. The 5KHz interrupt signal is used to output the current values between zero crossing points, giving 100 samples per cycle. The digital values of current are passed to the voltage controlled current feedback amplifiers via three digital to analogue converters. The control of the system can be arranged to give either a single shot or repetative mode of operation.

The base voltage of the model is 100 V line, and the amplifiers are capable of sinking currents in excess of 3A. The results presented in the next section were taken when the model was initially constructed to demonstrate the feasibility of the approach. At this time the star-delta transformer was not specifically designed for the task, its impedance was such to limit the base current to a value of 1.4 A, and it does not represent the variation of system impedance with frequency (or rate of change of current). Similarly the variation of line impedance with frequency is not represented, however in this case the system impedance is dominated by the super grid transformer. The model is currently being rebuilt with components to give a base value current of 5A and a better representation of the system impedances including frequency variation.

As indicated in the introduction the model is part of an investigation of the advantages to be gained by the use of increased phase numbers for thyristor controlled shunt reactors. Such a device would normally be connected to the 33 KV bus of the supply system and it is the authors' intention to connect a compensator to the model at the terminals of the amplifiers representing the arc furnace. In order that different control strategies can be readily implemented it is intended to make full use of mode in digital techniques in the compensator control system, which provide the facility for rapid reprogramming of the control algorithms. A number of different techniques have been described[7] in the literature for assessing the flicker level of voltage variations and it is proposed to implement these techniques digitally, applying them to the voltage waveforms measured on the model once these have been transferred back to the main frame computer.

Results

In order to check the suitability of the amplifiers as currents sinks the model was initially run in single phase mode using one of the recorded phase currents. Figure 3(b) shows the recorded phase current used as input to the amplifier whilst figure 3(a) shows the current waveform recorded on the model, over 5 cycles, and it is seen that they are in good agreement.

The model was then developed into the three phase form, and figure 4 and 5 show two phase currents both measured (upper trace a) and recorded (lower trace b) and again it is seen that the agreement between the two is good

Figure 6 shows one of the phase voltages, the upper trace again being the measured value from the model and the lower trace the recorded value. This latter was derived from the output of one of three voltages transformers connected in star at the 33 KV bus, whilst the former was recorded across one of three balanced resistors connected in star to the amplifier terminals. The distortions to the waveforms are evident and considering that the star-delta transformers in use when these recordings were made was not an exact representation of the super grid transformer supplying the furnace (SGT4, figure 1) the agreement between the two is encouraging.

REFERENCES

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ACKNOWLEDGMENTS

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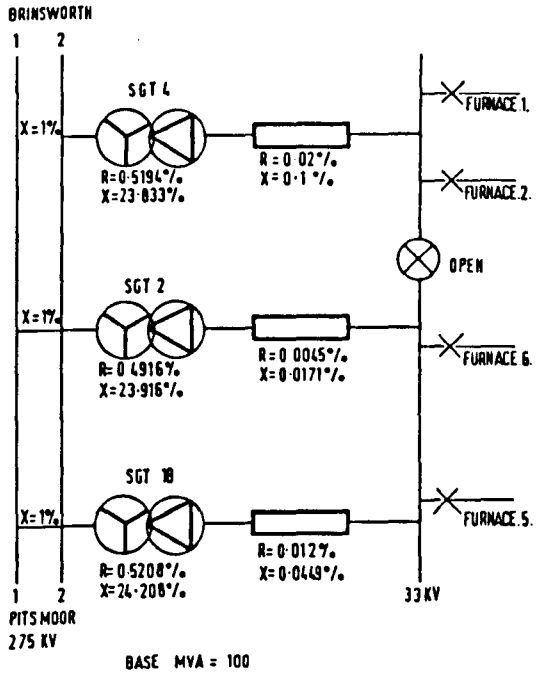


Figure 1 Supply to Templeborough Furnaces

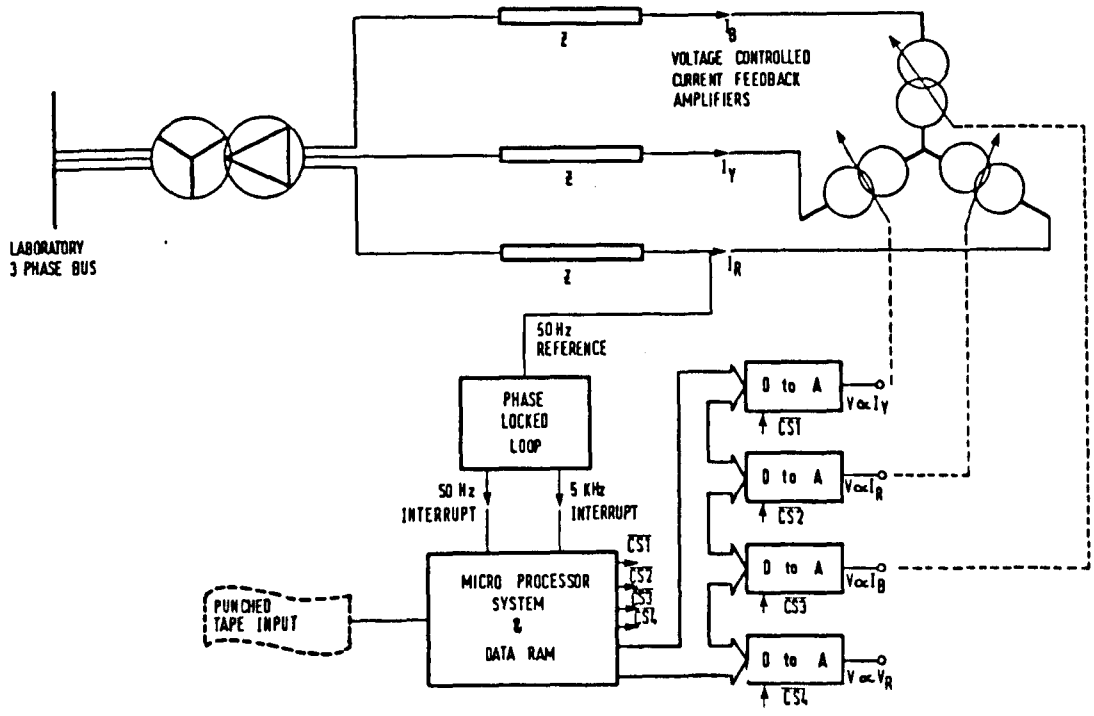
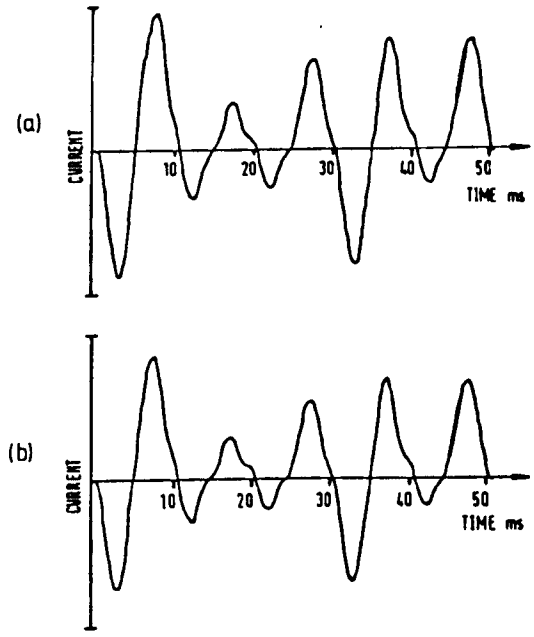
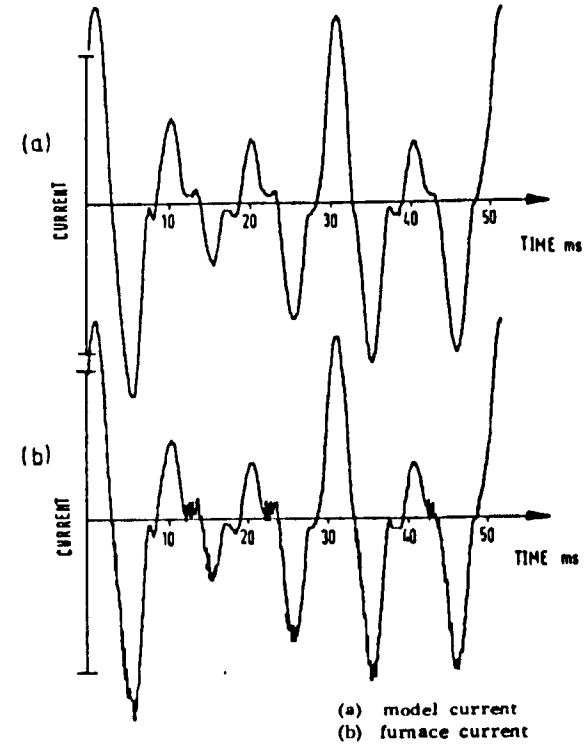


Figure 2 Block diagram of experimental model



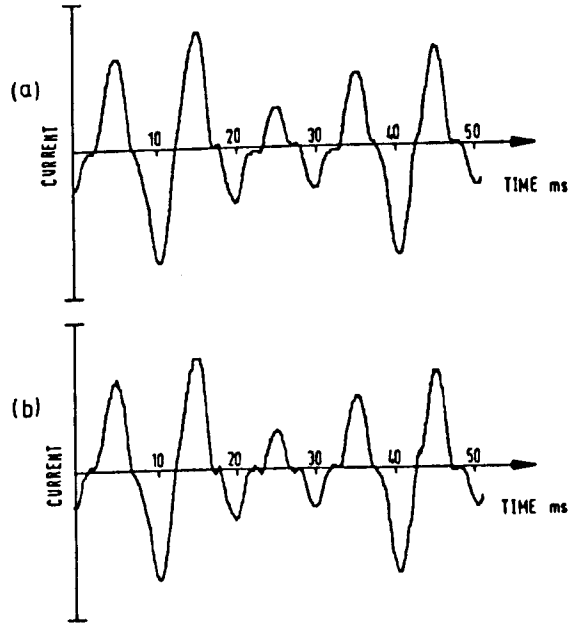
(a) model current
(b) furnace current

Figure 3 Current waveforms, single phase mode



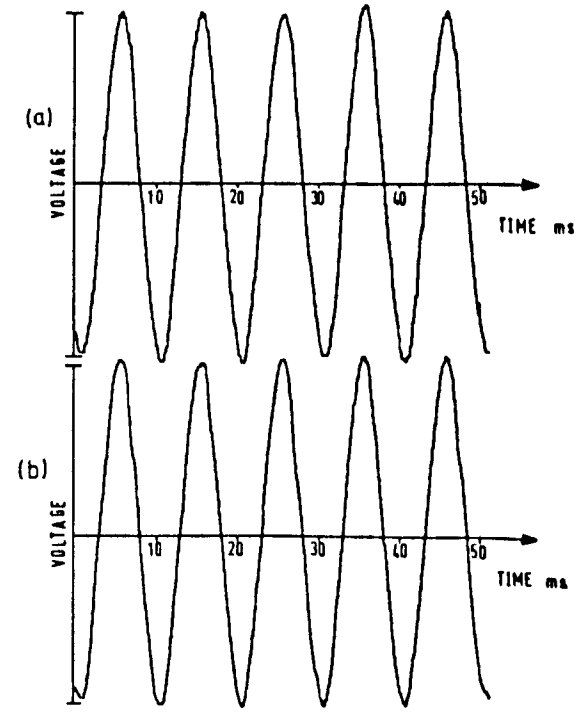
(a) model current
(b) furnace current

Figure 5 Yellow phase current waveforms, three phase model



(a) model current
(b) furnace current

Figure 4 Red phase current waveforms, three phase model



(a) model voltage
(b) furnace voltage

Figure 6 Red phase voltage waveforms, three phase model

L.II Reference [77]

The Computational Modelling of an Electric Arc Furnace

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Introduction

Residents of steel towns are frequently aware of the effects of electric arc furnaces on the supply system voltage level - as witnessed by the flicker of tungsten filament lamps. However, for certain steel making processes, this type of furnace represents the best production method, and thus there is considerable interest in possible methods of controlling voltage fluctuations. Control of voltage by shunt reactive compensators - particularly for relatively slow voltage changes, has been employed by power system authorities for some time, and following advances in solid state technology thyristor controlled static var compensators have been available for system voltage control [1]. Along with saturated reactor compensators [2], thyristor controlled equipment [3] has been used by a number of installations to provide voltage and flicker control at arc furnace sites. One of the requirements of equipment used for this purpose is that it should have a fast speed of response. For thyristor controlled reactors, one possible way to reduce the response time is to increase the phase number, and the work described in this paper is part of a study of thyristor controlled reactors (T.C.R's) with higher phase numbers.

To evaluate the performance of such equipment in the laboratory it is necessary to model, either computationally or experimentally the furnace and supply system. Both methods are being used by the authors, the experimental model is described elsewhere [5], and both use a similar approach to the problem of the random nature of the furnace currents.

A number of workers have approached the modelling of arc furnaces in different ways. Granstrom [6] uses a value of arc resistance or current which is a function of time, using sinusoidal, square and random functions alone or in combination. Dugan [7] describes the use of a transient network analyser with harmonic current sources to represent the furnace, but comments that this does not represent the random nature of the furnace currents. The method described in this paper makes use of recorded values of furnace currents as the input to the model, which represents the supply system by constant resistance and inductance. Macedo [8] has shown that the system is a dynamic one and that the impedance changes with time, and it is well known that the system impedance is a more complex function of frequency than $(R + jwL)$ due to the capacitance of the system as well as the nature of other loads. Both these effects are ignored in the work presented in this paper but the model is to be extended to include system capacitance.

Description of the Model

Figure 1 shows the supply system to the Templeborough Plant of British Steel upon which both the computational and experimental models are based. The C.E.G.B. with the co-operation of the steel makers have recorded furnace currents and voltages at the 33 kV busbars and these records have been made available to the authors, figure 2 shows a few cycles of one phase current for the start up of a

56 MVA furnace. The aim of the model is to calculate the voltage at the 33 kV busbars given the furnace currents, thus these form an 'input' to the computer model.

Looking at figure 1, it is seen that the 33 kV busbar is supplied by star-delta transformers, and for the non-sinusoidal, unbalanced currents the delta connection introduces a coupling between phases, a topic which does not yet seem to have been considered in detail. For three phase transformers constructed on a single three limbed core there are mutual inductances between the phases which act as another source of coupling important to unbalanced operation, but these are ignored in the results presented here.

For a star-delta transformer shown in figure 3 the line currents on the delta side can be expressed simply in terms of the branch currents by the relationship:

$$[I_{\Delta L}] = [C] \cdot [I_{\Delta B}] \quad \text{where } [C] = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

C is a singular matrix thus its inverse does not exist, physically this means that the branch currents $[I_{\Delta B}]$ cannot be expressed in terms of $[I_{\Delta L}]$ unless there is some additional condition, since any circulating current in the delta has no effect on the line currents. It is essential however that a relationship be derived in order to evaluate the line currents on the high voltage side of the Transformer since $[I_{\Delta L}]$ are the "driving function" of the model. It was expected that the instantaneous sum of the furnace currents would be zero and inspection of the recorded current waveforms showed this to be so within experimental error, further any circulating currents in the delta must be due to zero sequence currents flowing on the high voltage star side of the transformer, and these are most likely to be sinusoidal in nature. Thus assuming that the circulating current is zero yields:

$$[I_{\Delta B}] = \frac{1}{3} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \cdot [I_{\Delta L}] \qquad (1)$$

The line currents on the star side $[I_Y]$ are related to the branch currents on the delta side $[I_{\Delta B}]$ by the transformer turns ratio.

The voltages measured at the 33kV busbars are phase values determined by three star connected voltage transformers. Assuming that these are identical and that the sum of the currents at the star point is zero then

$$[V_{\Delta p}] = \frac{1}{3} \cdot \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} [V_{\Delta L}] \qquad (2)$$

and it is noted that this transformation is the transpose of that for the currents, equation (1).

Using a step-by-step technique with the furnace currents of the 33kV busbars and their rates of change specified, the currents $[I_Y]$ can be determined by equation (1), thus referring to figure 4

$$[V_Y] = [V_B] - L_s \cdot \frac{d}{dt} \cdot [I_Y] \qquad (3)$$

$[V_{\Delta L}]$ and $[V_Y]$ are related by the transformer turns ratio, thus from $[V_{\Delta L}]$ using equation (2) the voltages $[V_{\Delta p}]$ are found and then

$$[V_f] = [V_{\Delta p}] - (L_r + L_l) \frac{d}{dt} [I_f] - (R_t + R_l)[I_f]$$

As the computation continues the variation of $[V_f]$ with time is determined. It is necessary to achieve the correct phase relationship between the busbar voltage and the furnace currents. This is achieved by labelling the current values which occur at the points of measured busbar voltage zero crossing and ensuring that these coincide with the calculated voltage zero crossings by adjusting the phase of the voltage $[V_B]$.

Results

Figures 5 (a) and (b) show the predicted and measured phase voltages for the red and blue phases over 5½ cycles, and the distortion of the voltage waveform is clearly seen. It is seen that whilst the magnitudes of the measured and predicted voltages are in reasonable agreement there is some discrepancy in the detailed shape of the waveforms, due to the limitations of the model mentioned earlier, this is obviously a topic which needs further investigation.

Acknowledgment

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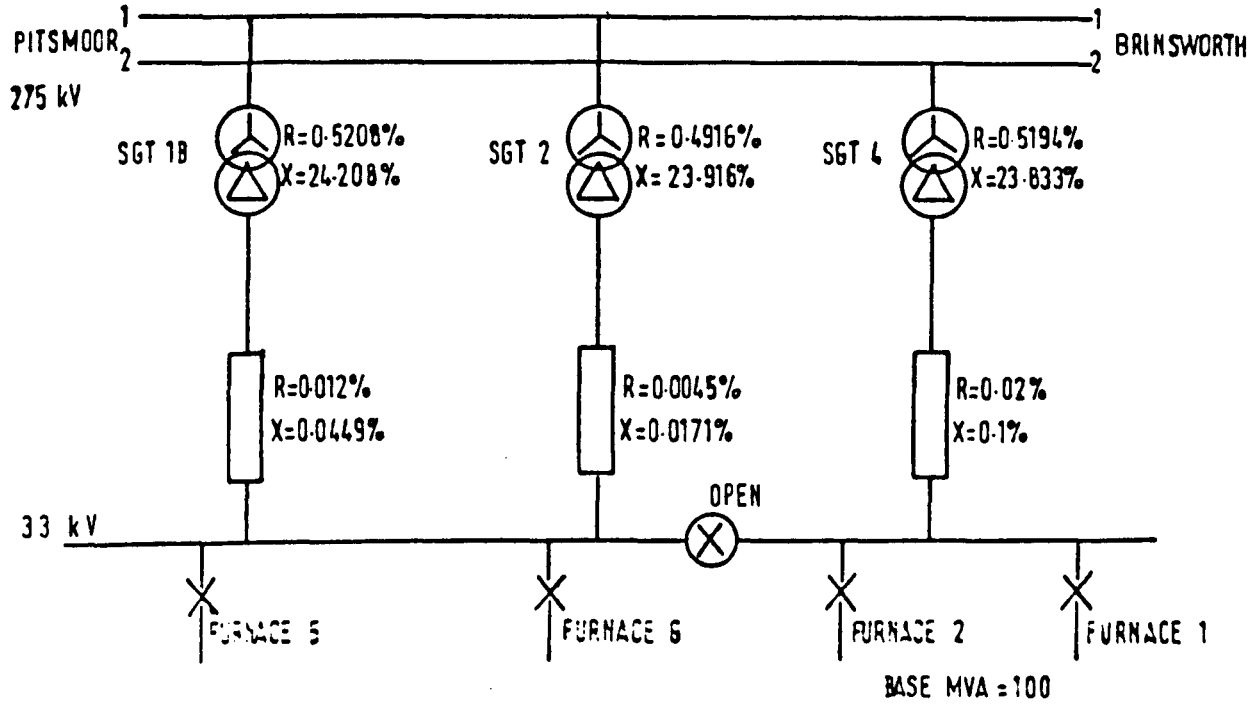


Figure 1 Supply to Templeborough Furnaces

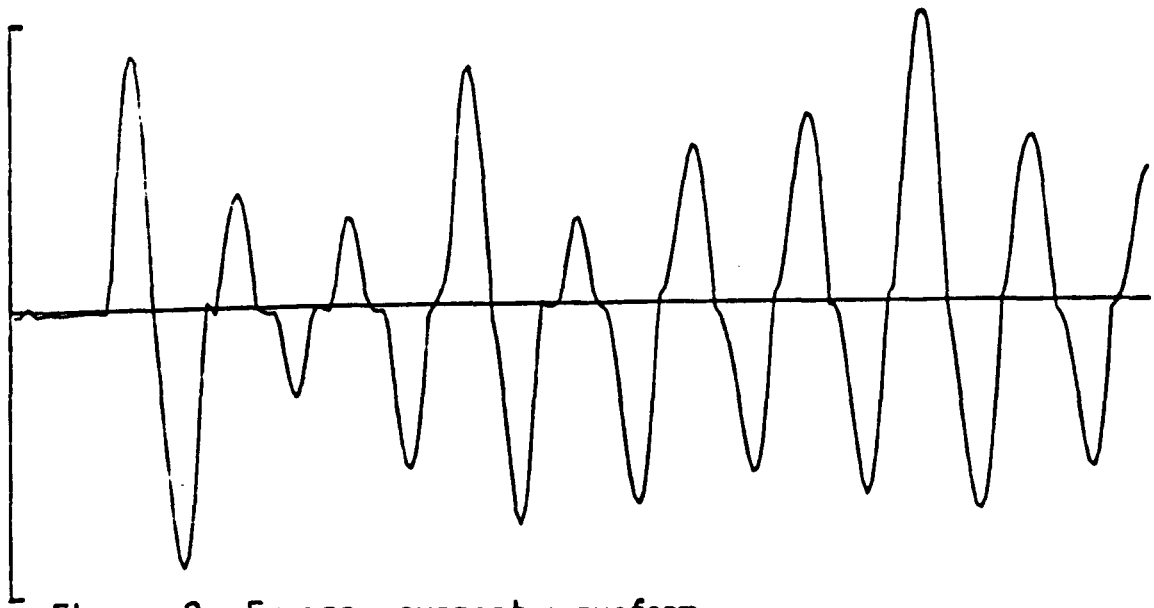


Figure 2 Furnace current waveform

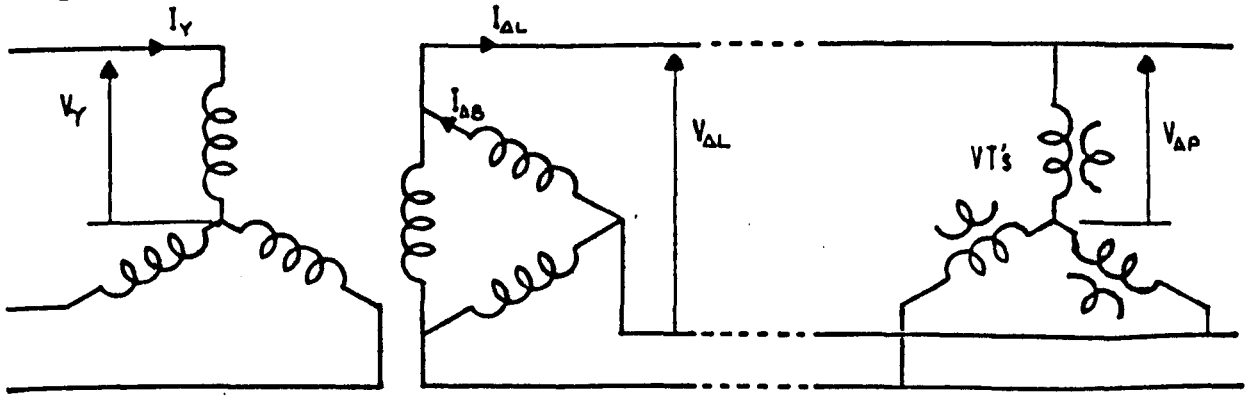


Figure 3 Star-Delta Transformer and derivation of secondary phase voltage

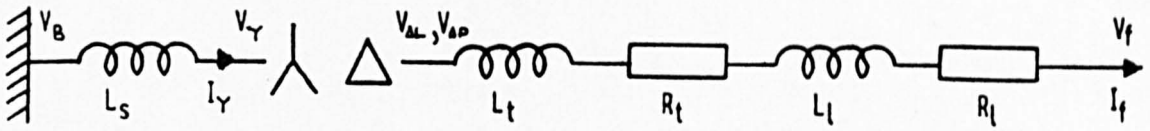
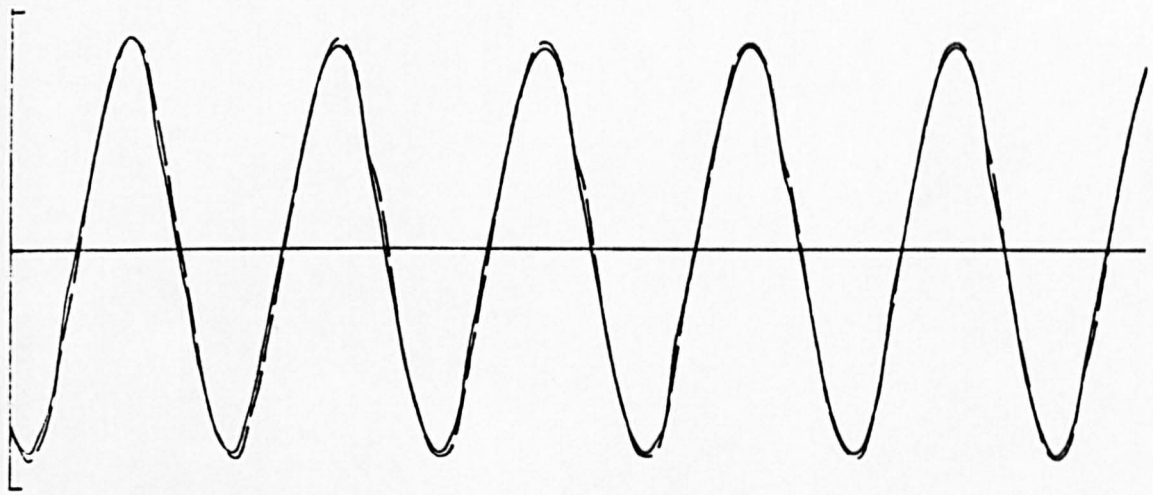


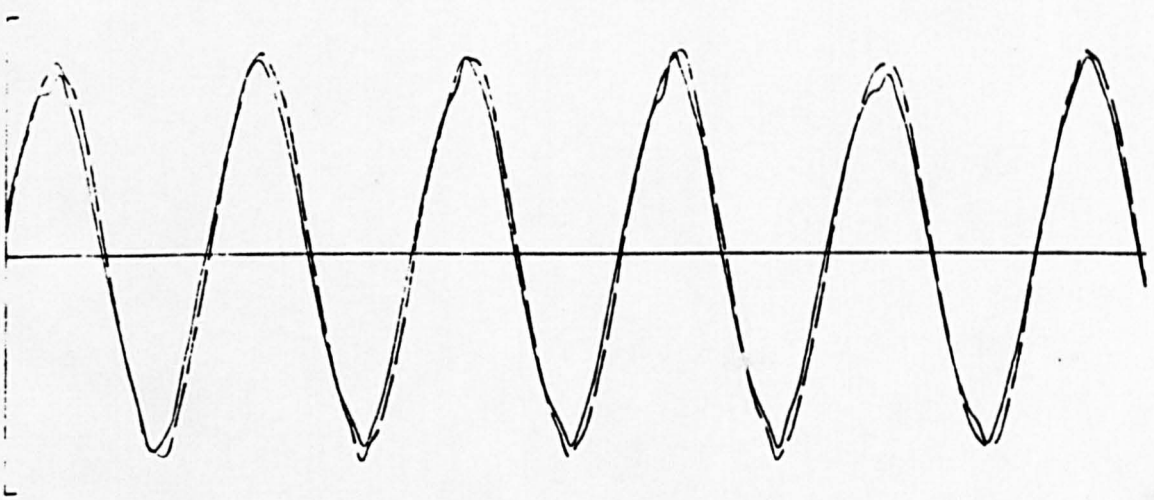
Figure 4 Equivalent Circuit



(a) Red Phase

— — recorded

——— calculated



(b) Blue Phase

— — recorded

——— calculated

Figure 5 Predicted and Measured Phase Voltage ——— 33kV Busbar