THE UNIVERSITY *of* LIVERPOOL

A STUDY OF THE ELECTRICAL PROPERTIES OF HYDROGENATED AMORPHOUS SILICON AND ITS APPLICATION IN THIN-FILM TRANSISTORS

by

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To my wife and my son

for their patience, understanding,

encouragement, and support.

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ABSTRACT

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) are widely used as switching elements in active matrix liquid crystal displays (AMLCDs). The density of states (DOS) in the mobility gap of a-Si:H has an essential role in the characteristics of thin-film transistors and other devices made in this material. The quality of a-Si:H film depends on the method and conditions of deposition and is variable from sample to sample. In this work some electrical properties of a-Si:H, with the idea of a thin-film transistor application, are studied. The steady-state space-charge limited current (SCLC) method is used to investigate the density of states in the mobility gap of a-Si:H. The field effect mobility of electrons is measured and the metal a-Si:H contacts are studied. The work also consists of computer simulation of both vertical thin-film transistor (VTFT), and space-charge limited currents.

The work includes a review of amorphous silicon, its history, electronic structure, methods of preparation, and applications, and a review of thin film transistors, including history, materials, and structures. The properties and processing steps of a vertical thin-film transistor (VTFT) are demonstrated.

The theory of space-charge limited current for multiple trap levels is established. The steady-state SCLC of a-Si:H is simulated using the Medici device simulation package. The effect of single and multiple traps, film thickness, temperature, etc. on the current-voltage characteristics is also studied.

The *I-V* characteristics of intrinsic a-Si:H deposited on *n*-type crystalline silicon was measured at room temperature and at low temperatures in a nitrogen cryostat

using different metal contacts. The intrinsic a-Si:H makes rectifying contacts with most of metals. The forward current is space-charge limited, and the thermionic emission conduction process is dominant under the reverse bias. The steady-state SCLC is used to investigate the density of states in the mobility gap of a-Si:H by different methods. The barrier height at the metal a-Si:H contact is calculated using the reverse current.

The field effect mobility of electrons in a-Si:H was measured using a structure similar to that of an inverted-staggered TFT. The variation of field effect mobility with gate voltage is studied. The field effect mobility has also been calculated from the frequency dependence of drain current.

A vertical a-Si:H TFT was simulated using the Medici simulation package. Different sets of traps derived from SCLC measurement were used in a-Si:H and the effect of traps, channel length, thickness of gate oxide, and thickness of semiconductor etc. on device characteristics were studied.

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Chapter One

INTRODUCTION

In 1947 amorphous silicon (a-Si) was first reported by Haas [1], and in 1969 Chittick, Alexander, and Sterling made hydrogenated amorphous silicon (a-Si:H) for the first time [2]. A-Si:H has become the favoured material for the thin-film transistors (TFTs). Because of high defect states, unhydrogenated a-Si does not have the more desirable characteristics of a useful semiconductor. It was shown that introducing hydrogen in amorphous silicon reduces the defect states by removing dangling bonds, resulting in a material with high photoconductivity, good electrical transport properties, and with the possibility of doping [3, 4]. The means of doping the material was recognized by Spear and Le Comber [5], and this made possible the use of a-Si:H in the electronic devices, rapidly increasing the interest in this material.

The density of states (DOS) in the mobility gap of a-Si:H has an important role in the operation of a-Si:H devices. Many researchers have investigated the DOS in the bandgap of a-Si:H by different methods, such as deep level transient spectroscopy (DLTS) [6, 7], field effect (FE) [8-10], space-charge limited current (SCLC) [11-27], and some other methods such as capacitance-voltage, capacitance-frequency,

and capacitance-temperature measurements, etc. [24, 28]. The steady-state SCLC method is less dependent on the surface states and is more suitable for determination of the bulk density of states in intrinsic a-Si:H [29].

The first application of a-Si:H was in photovoltaic devices [30]. Just few years later, the first a-Si:H thin-film transistor was fabricated and was used as a switching element in the active matrix liquid crystal displays (AMLCD) [31]. Before that, CdSe was the main material used in thin-film transistor technology [32, 33]. CdSe TFTs present high electron mobility, and as a result, high operation speed, but it encountered some serious problems such as stability and toxicity problems [34]. Polycrystalline silicon or polysilicon (poly-Si) is another important semiconductor material for TFTs. It has the advantage of high carrier mobility, however, the high leakage current of poly-Si TFTs is a serious problem in their usage as pixel elements in AMLCDs [35-39]. Despite its low carrier mobility, a-Si:H is used to produce the pixel TFT in active matrix displays. This is because of its low leakage current and the fact that it can be deposited over large areas at low temperatures.

The switching speed of ideal TFTs is proportional to μ/L^2, where μ is the carrier mobility and L is the channel length. There are two simultaneous efforts to improve the speed of a-Si:H TFTs. One effort is to increase the field effect mobility by improving the quality of semiconductor material and insulator interface. Electron field effect mobility as high as 5.1 $cm^2V^{-1}s^{-1}$ has been reported [40]. Another and more effective method is to reduce the channel length by improving the lithography techniques. Introducing vertical TFTs (VTFT) is an efficient way to overcome the lithography limitations, in which the channel length can be reduced to submicron measures, independent of the accuracy of lithography equipment. It also reduces the active capacitances.

Among the methods of deposition of a-Si:H, plasma enhanced chemical vapour deposition (PECVD) or glow discharge (GD) decomposition of silane gas is the most common. As deposition takes place at rather low temperatures, a-Si:H can be deposited on cheap glass substrates. This is one of the main advantages of a-Si:H TFTs compared to their poly-Si counterparts. The inverted-staggered structure with silicon nitride as insulator is the most common planar structure used for a-Si:H TFTs.

This structure allows silicon nitride, intrinsic a-Si:H film, and n^+ a-Si:H contact layers to be deposited successively in the same chamber.

The work presented in this thesis details the investigation of some major properties of a-Si:H, such as density of states, free electron mobility, field effect mobility, etc. that have essential roles in a-Si:H TFTs. The data so derived are then used in computer modelling of a vertical a-Si:H TFT, to achieve a better understanding of the device operation. Steady-state SCLC is the method used in this work to investigate the density of states. The SCLC of a-Si:H was simulated as an evaluation of validity of methods.

1.1 Motivation and Thesis Organization

The material and the structure are two key issues in any electronic device. Although about half a century has passed since the first arrival of amorphous silicon, this material and its application in electronic devices have always been of central interest. Therefore, it is appropriate to provide a brief description of a-Si:H and its applications. Chapter 2 deals with a review of a-Si:H, its electronic structure, methods of preparation, and its application, especially in thin-film transistors.

The steady-state space-charge limited current has extensively been used to investigate the density of states in the mobility gap of amorphous silicon. The methods of investigation are based on the shape of the logarithmic plot of *J-V* characteristics. The theory of steady-state SCLC [41, 42] has been extended to the case of multiple traps. An a-Si:H specimen has been simulated and the effect of density and energy level of traps, temperature, etc. on the *J-V* characteristics is analyzed in chapter 3.

It is shown that the dominant conduction process in the bulk of a-Si:H is space-charge limited. In chapter 4, the *J-V* characteristics of a-Si:H, measured at different temperatures, are analyzed using different methods. The experimental data are also compared to the simulation results presented in chapter 3.

Metal-semiconductor contacts are among the important issues in a-Si:H devices. They have important potential for drain and source contacts in thin-film

transistors. Due to surface states, intrinsic a-Si:H makes a rectifying contact with nearly all metals [43-46]. Chapter 5 addresses this issue. The *J-V* characteristics of metal a-Si:H contact are measured using different metals and at different temperatures. The results show that the space-charge limited current is the dominant in forward bias, while in the reverse the dominant conduction process is thermionic emission.

The drain current in thin-film transistors is proportional to field effect mobility. The presence of surface states means that this quantity is usually smaller than the bulk free carrier mobility. Using an a-Si:H structure similar to the inverted-staggered TFT, the field effect mobility is calculated from the measured characteristics. The methods and results are discussed in chapter 6.

Computer simulation prior to the fabrication of device is a useful method in which the effect of various parameters on the device characteristics can be traced and analyzed. In chapter 7, a vertical a-Si:H TFT is simulated using the Medici device simulation package. The traps derived from the SCLC of a-Si:H discussed in chapter 4 are used in the model. The effect of different parameters such as density and energy level of traps, channel length, thickness of gate oxide, etc. on the characteristics of a device is investigated.

The last chapter, chapter 8, is dedicated to conclusions obtained from this work and gives suggestions for further work.

1.2 Experimental Techniques Used in This Work

Various equipment and experimental tools have been used in this work. The a-Si:H samples were prepared in a glow discharge cavity in Cambridge University. Silicon dioxide was grown in a high temperature furnace in the presence of oxygen. Metal contacts were deposited using a high vacuum evaporator and were annealed in a furnace in the presence of forming gas. Conventional photolithography techniques, lift-off process and wet etching were used in fabrication of field effect samples.

The TFT characteristics were measured using a pc-controlled Keithly MOS measurement rig. A nitrogen cryostat linked to a pc-controlled Keithly *IV* rig was

used for temperature dependent SCLC measurement. The pc-controlled Keithly *IV* rig was used for other SCLC measurements. A Fluke 410B high voltage power supply, a Tektronix 2430A digital storage oscilloscope, and an ordinary signal generator were used for ac field effect measurements.

The computer simulation of SCLC and the vertical TFT was performed using the TMA Medici version 2.0.2, two-dimensional device simulation package on Sun-Unix workstation. The masks for field effect devices were designed using Cadence on Sun workstation.

1.3 CONTRIBUTIONS

The following contributions were revealed in this thesis:

- The Steady-state SCLC theory proposed by Lampert and Mark [42] for single trap level was extended to multiple trap case. The resulting theory can be used to calculate the density of discrete traps.

- The steady-state SCLC regime was simulated using the Medici device simulation package. The effect of traps and other parameters on the SCLC *IV* plots was investigated and analyzed.

- The SCLC measurements were applied to very thin a-Si:H films (0.2-0.3 μm) and different methods were used to investigate the density of states in the mobility gap of a-Si:H. The results obtained from different methods were compared and analyzed.

- A new structure consisting of an intrinsic a-Si:H film on crystalline silicon (c-Si) substrate, without any n^+ contact layer was used for SCLC and Schottky contact measurements.

- The *IV* characteristics of metal contact with a-Si:H were measured. It was found that intrinsic a-Si:H makes Schottky contact with all metals used in the experiments. The Schottky barrier height was calculated by different methods from the experimental data. It was concluded that the barrier height is nearly independent of metal work function and depends mainly on the surface states.

- A vertical a-Si:H TFT was modelled using the Medici simulation package. The traps found from the SCLC measurements were applied to a-Si:H in this device. The effect of traps and other device parameters on the device characteristics were investigated.

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CHAPTER TWO

HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTORS, A REVIEW

2.1 INTRODUCTION

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFT) are widely used in various applications, especially in large area active matrix liquid crystal displays (AMLCD). The low cost and ability to deposit on large areas at low temperature, makes a-Si:H the most popular material for thin-film transistors. Despite its low carrier mobility, the a-Si:H TFT has the advantage of lower leakage current, comparing to its main counterpart in polycrystalline silicon, the polysilicon (poly-Si) TFT, providing a higher on-off ratio.

In this chapter, the properties of a-Si:H and its applications are reviewed, with emphasis on the application to thin-film transistor manufacture. In the following

section, the properties of a-Si:H are described, including the historical background, its structure, conduction mechanisms, methods of preparation, and applications. The thin-film transistor is reviewed next. In this review, after a brief history, the general features of thin-film transistors, the basic materials used in TFTs, their application, and their structure are described, with emphasis on vertical structures.

2.2 Properties and Applications of Hydrogenated Amorphous Silicon

2.2.1 Historical Background

The first amorphous semiconductors which were studied were chalcogenides. These materials, glasses formed from the melt by cooling, contain the elements sulphur, selenium, and tellurium and include As_2Se_3, GeS_2, etc. Their structure is similar to the oxides, but they have a smaller band gap [1]. The study of chalcogenides led to introduction of xerographic copying machines. The first successful copying machine was made in 1956, using selenium as the photoconductive material [1]. In 1968, S. R. Ovshinsky used chalcogenides for electronic switching [2].

Pure amorphous silicon was first reported by Haas in 1947 [3]. In 1958, Richter and Breitling found that, due to the strong covalent bonding force, amorphous silicon has almost the same tetrahedral short-range order as the crystalline phase [4]. Because of very high defect density, pure amorphous silicon did not have the characteristics required for a useful semiconductor, and this led to introduction of the hydrogenated amorphous silicon [1].

Hydrogenated amorphous silicon was first made by Chittick and coworkers in UK in 1969, when preparing a-Si by plasma-enhanced decomposition of silane gas [5]. Later, Spear's group at the University of Dundee, using field effect experiments, found out that the density of states (DOS) in the forbidden band of a-Si:H made by glow discharge (GD) deposition technique was reduced [6-8]. The material had fairly high carrier mobility [9] and strong photoconductivity [10]. Paul and coworkers at Harvard were the first to recognize the role of hydrogen in amorphous

silicon [11, 12]. They found out that adding hydrogen to the sputtering system could significantly reduce dangling bonds and, as a result, also the defect density in the forbidden band of amorphous silicon. It was found that the hydrogen gives a similar improvement in material properties for glow discharge a-Si:H [1].

N and *p*-type hydrogenated amorphous silicon were developed by Spear and coworkers by addition of phosphine and diborane to the deposition gas [13]. The doping possibility, which can affect the electrical properties of hydrogenated amorphous silicon over a wide range, resulted in huge increase in both basic research and application development based on this material [6].

The first research on a-Si:H devices was in 1976 by Carlson and Wronski at RCA laboratories who reported the first solar cell using a-Si:H [14]. In this year, Spear and coworkers made the first a-Si:H *p-n* junction [15]. The first a-Si:H thin film transistor and its application to active matrix liquid crystal displays (AMLCD) was first reported by Le Comber, Spear, and Gaith in 1979 [16]. The ability to deposit and process a-Si:H over large areas is the main advantage of these devices. Research on large area electronic arrays of a-Si:H devices started in 1981 by the Dundee group [17]. Applications include liquid crystal displays, optical scanners, and radiation imagers [1]. The application of a-Si:H thin film transistors in memory devices was reported in 1982 [18].

2.2.2 Electronic Structure of Amorphous Silicon

The main difference between amorphous and crystalline semiconductors is the disorder of atomic structure [1]. In a crystal, atoms are located in a periodic structure and each atom has a covalent bond with its nearest neighbour with a specific bond length and bond angle. So crystals are ordered both over short and long distances (short range order and long range order, respectively). Crystals have an electronic structure with abrupt band edges, and in the absence of defects, there are no states in the forbidden band. The defects in crystal are mainly due to displacement of atoms from crystalline structure such as vacancies and interstitials, or structural defects. These defects introduce some states in the band gap. In practical crystalline

semiconductors, the defect states are so few that have virtually no effect on the conduction mechanisms of semiconductors.

Amorphous semiconductors are not completely disordered. In amorphous materials, there are the same covalent bonds between atoms, the same number of neighbours, and the same average bond length and bond angle as in single crystals. They have almost the same short range order as single crystals, but do not have long range order [1]. A chemical bonding picture of interactions among atoms indicates that only the arrangement of nearby atoms (the short range order) will dominate the formation of electronic states in the material and its electronic structure [19]. Because the electronic structure of amorphous semiconductors are nearly the same as their crystalline counterpart, they have a considerable band gap.

Due to variations of length and angle of bonds arising from long range disorder, there are some localized states close to the conduction and valence bands of amorphous semiconductors that form band tails. So the abrupt band edges in crystalline semiconductors are replaced by broadened band tails. In spite of relatively low concentration of states in band tails, they have an important role in conduction, because electronic transport usually occurs at band edges [1].

The localized states in band tails and the extended states in the middle of conduction or valence bands are separated by a so-called mobility edge (E_C and E_V). It has been named the mobility edge because at absolute zero temperature only electrons above E_C (or holes below E_V) are mobile and can take part in conduction.

In crystalline semiconductors, the band gap E_G is defined as the separation of the conduction and valence band edges E_C and E_V:

$$E_G = E_C - E_V . \tag{2.1}$$

Because there are not such abrupt band edges in amorphous semiconductors, the definition of band gap is not so straightforward. There are different definitions for the band gap or the optical gap in amorphous semiconductors. One definition is the separation of the conduction band minimum and the valence band maximum with the addition of a correction term called the exciton binding energy [20]

$$E_G = E_T - \text{VBM} + E_{xc}, \tag{2.2}$$

where the threshold energy E_T is the point of maximum slope in the yield spectrum, VBM (valence band maximum) is the extrapolation of the steepest descent of the leading edge of the valence band spectrum, and E_{xc} is the core level exciton binding energy [20]. The valence band maximum (VBM) and the threshold E_T are usually measured using photoelectron spectroscopy (or photoemission) techniques [20]. Reichardt, Ley, and Johnson have measured VBM and E_T using synchrotron radiation [21]. The band gap calculated by them is 0.75 eV for unhydrogenated a-Si and 0.85 eV, 1.40 eV, and 1.65 eV for a-Si:H with hydrogen content of 10, 17, and 50 %, respectively. They have used the value of 150 meV for the core level exciton binding energy.

Another technique to derive the optical gap introduced by Tauc, Grigorovici, and Vancu, is optical spectroscopy [22]. The value of optical gap derived from absorption edge spectrum of a glow discharge a-Si:H sample prepared at 370 °C is between 1.6 to 1.85 eV, depending on the region used for linear extrapolation of the Tauc plot [23, 24]. For specimens evaporated or sputtered in the absence of hydrogen, values of optical gap between 1.2 eV and 1.5 eV have been observed [25-30].

The term mobility gap, the separation of the conduction and valence mobility edges ($E_G = E_C - E_V$), is widely used in amorphous materials. The mobility gap can be measured from the activation energy of the dc conductivity measurements when the Fermi level is at midgap [31]. Beyer *et al.* have measured the mobility gap using this technique by studying the conductivity and thermoelectric power in a series of compensated a-Si:H films with different Fermi level positions [32]. The mobility gap measured by this technique is 1.74 eV which is in close agreement with the optical gap of 1.71 eV derived from the Tauc plot, extrapolated at zero temperature [33]. This close agreement between the optical gap and the mobility gap suggests that the localized state distributions near the mobility edges are relatively narrow ($\leq$ 0.1 eV).

In a-Si:H, the hydrogen content is the main source of variation in the optical band-gap. Cody *et al.* have derived a linear relationship between optical band-gap

and hydrogen concentration of 10 to 30% in specimens prepared by RF glow discharge or sputtering:

$$E_G = 1.5 + 0.015c_{\rm H}, \tag{2.3}$$

where E_G is the optical gap in eV and $c_{\rm H}$ is hydrogen concentration in per cent [24]. Matsuda *et al.* have obtained a similar linear relationship between E_G and $c_{\rm H}$ for variety of films prepared by reactive sputtering or glow discharge at deposition temperature of 300 °C with hydrogen concentration of 2 to 17% [34]:

$$E_G = 1.48 + 0.019c_{\rm H}, \tag{2.4}$$

that agrees well with the relationship derived by Cody *et al.*

The optical gap is affected by annealing temperature in two ways: the loss of hydrogen with increasing the annealing temperature tends to a lowering of the optical gap, while the relaxation of the network lowers the absorption tails that are due to defects and thus increases the optical gap [20]. For samples prepared at deposition temperature $T_D \leq 200$ °C or at high deposition rates, due to high defect density, the defect density decreases with annealing by several orders of magnitude and E_G increases [35-37]. At an annealing temperature of $T_A \approx 300$ °C the increase is dominated by the decrease in E_G due to the loss of hydrogen [37, 38]. For samples prepared at high deposition temperatures ($T_D \geq 200$ °C), there is no change in E_G with annealing temperatures below 350 °C, and E_G decreases as hydrogen begins to evolve above $T_A \approx 350$ °C [35, 39]. The temperature coefficient of the optical gap is 4.3×10^{4} eV/K [40].

In amorphous semiconductors, atoms are situated in a random network and each atom has a specific number of bonds with its nearest neighbour, which is called coordination [1]. The most important defect in amorphous semiconductors is the coordination defect, which an atom has too many or too few bonds (Fig. 2.1). This kind of defects introduces some states in the middle of mobility gap (Fig. 2.2).

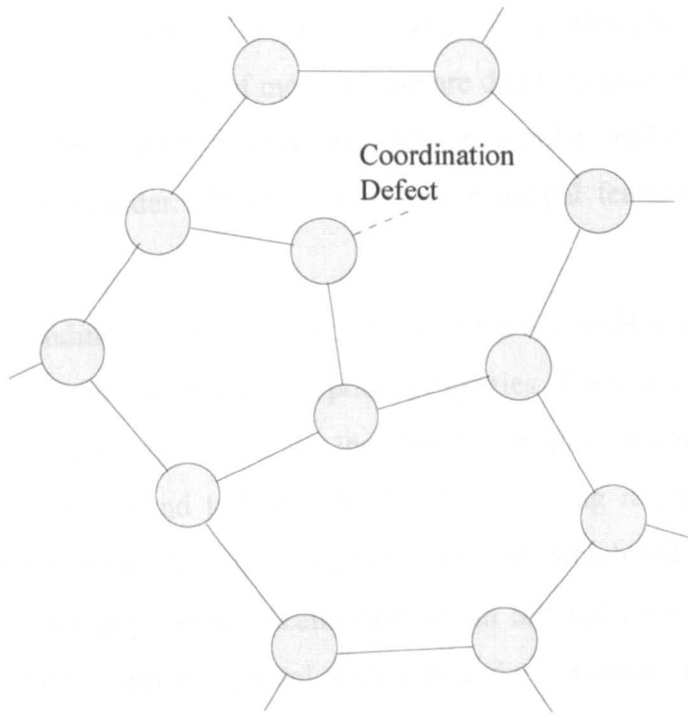


Figure 2.1 Coordination defect in amorphous semiconductors (after Street [1]*).*

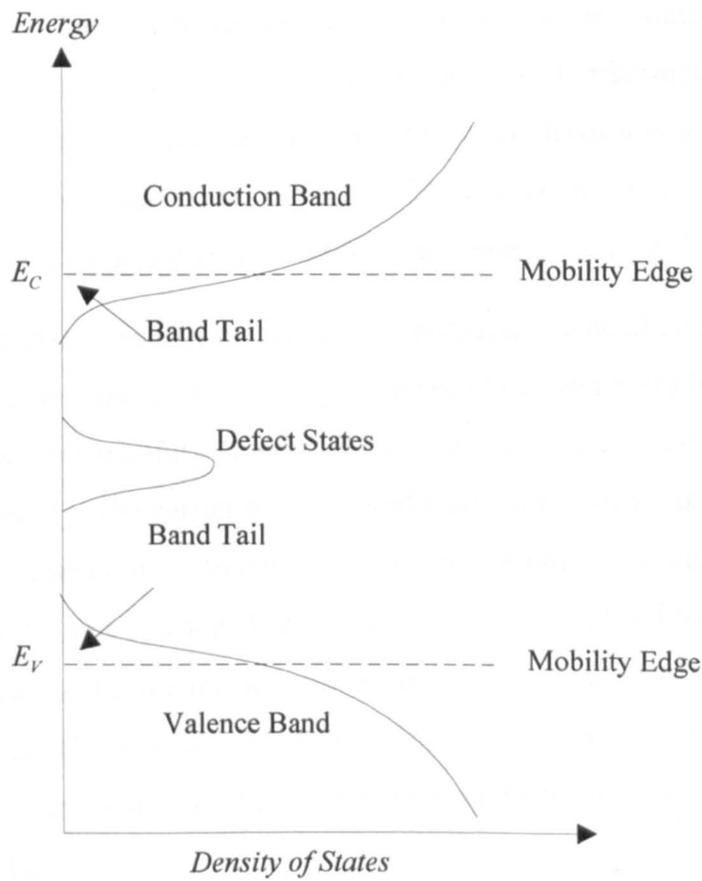


Figure 2.2 The electronic structure of a typical amorphous semiconductor (after Street [1]*).*

The electronic structure of a typical amorphous semiconductor is shown in Fig. 2.2. The states in the middle of mobility gap are due to coordination defects, the presence of a forbidden band is because of short range order, and band tails are because of long range disorder. These are the three principal features of amorphous semiconductors.

An understanding of the band tail and gap states in a-Si:H is essential in order to understand and control transport and optical properties. There is clear evidence for band tails and reasonable agreement for the distribution of states within the tail (at least for the conduction band tail) in a-Si:H [40]. The long range disorder of the atoms in a-Si:H introduces first strong carrier scattering, which reduces the mobility of carriers, and eventually causes localization. In an ordered crystal, the electronic states "extend" throughout the crystal with a periodic potential energy. There is a constant phase relation between the wavefunction at different lattice sites and the wavefunction has a well defined momentum [1]. Therefore, these states are called "extended" states. In an amorphous semiconductor, however, the disordering effect is strong enough to cause such frequent scattering that the wavefunction loses phase coherence over a distance of one or two atomic spacings. Furthermore, in some states close to the band edge there is zero probability for an electron in a particular site to diffuse away and these states are "localized" through the material. The extended and localized states are separated by a mobility edge at energy E_C (Fig. 2.3) [1].

In addition to creating the distinction between extended and localized states, the disorder also influences the mobility of the electrons and holes beyond the mobility edge. The carrier mobility is reduced by scattering, which increases with the degree of disorder [1]. The carrier mobility under conditions of weak scattering is proportional to the carrier mean free path, and the minimum of the latter in a disordered solid is the interatomic spacing. The electron mobility calculated for a-Si:H using the interatomic spacing for the mean free path is about 2-5 $cm^2 V^{-1}s^{-1}$, which is close to the actual value [1]. However, the simple transport equations do not apply to strong disorder and the calculation of the mobility and conductivity near the mobility edge is complicated [1].

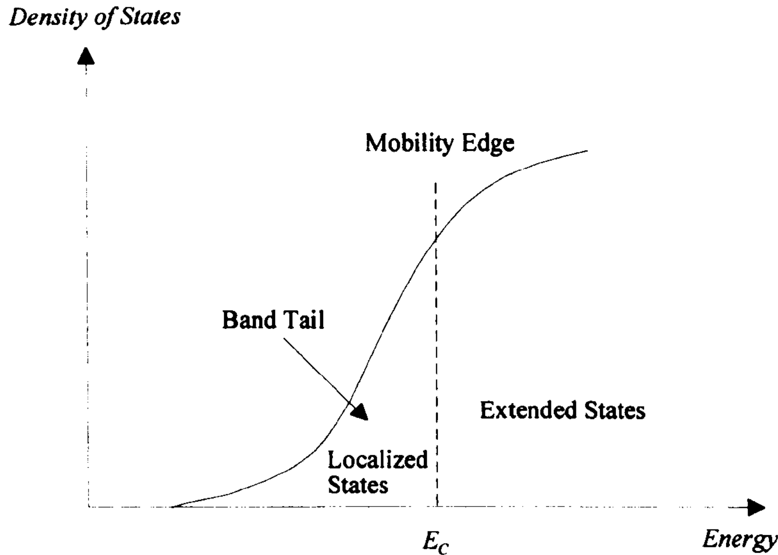


Figure 2.3 The density of states distribution near the band edge of an amorphous semiconductor. (after Street [1]).

Adler is against the band-tail interpretation and has argued that a defect related band of states near the band edge is more likely [42].

Cohen, Harbison, and Wecht identified a band of defect states just above midgap (0.85 eV below the conduction band) as the second electron bound to the dangling bond defect [43]. Two peaks in density of states $N(E)$ were found at 0.4 and 1.2 eV below the conduction band edge using field effect measurements, where the lower energy peak is larger by an order of magnitude[44-46]. However, deep-level transient spectroscopy (DLTS) measurements indicate a much lower $N(E)$ in the gap [47-51], suggesting that the field effect measurements may be influenced by surface states [19]. Lang, Cohen, and Harbison found a deep minimum in $N(E)$ between 0.3 and 0.6 eV from the conduction band edge and a broad shoulder of states extending from the valence band edge up to midgap[49]. Photoemission results [52-54] and a correlation of conductivity, photoconductivity, and photoluminescence [55] are also consistent with a large population of hole-trap states in the lower half of the gap. Photoluminescence experiments shows a dominant peak near 1.4 eV below the conduction band [56, 59].

In a-Si:H, because of very low defect states, the surface states play an important role. The depletion layer width in a-Si:H is in order of 1 μm, which is around or

greater than the typical sample thickness. So, good control of surface is essential for an understanding of the electrical properties [41].

There are two significant types of surface states in a-Si:H [41]. One of these is a fixed charge that can be introduced on the surface, giving strong band bending. One source of this fixed charge is adsorbed gas molecules, particularly water vapour or NH_3 [41]. These surface states can change the conductivity by several orders of magnitude [60]. Annealing to 150 °C can drive off the adsorbed gas and so remove the surface states produced by them [41]. The second type of surface state is a localized level within the band gap originating from an a-Si:H defect at the surface or interface. This kind of surface states is very important because of their influence on the field effect results. The field effect is very sensitive to the way the interface to the insulator was prepared, and this is attributed as being due to surface states [41].

The position of the Fermi level E_F within the band gap depends on the density of states, doping, and temperature. In the intrinsic a-Si:H the Fermi level is not situated in the middle of the band gap, because of the difference between the DOS below and above E_F. The Fermi level varies with temperature when it falls in a range of nonuniform DOS. In this case, as temperature changes, the number of states filled above E_F differs from the number of emptied states below E_F, according to the Fermi-Dirac statistics. Therefore, by increasing the temperature, the Fermi level moves in the direction of decreasing DOS. This is referred as the statistic shift [20]. The shift of the Fermi level with temperature depends on the change in DOS. For a DOS that varies linearly in the neighborhood of the Fermi level as

$$N(E) = N\left(E_F^0\right) + m\left(E - E_F^0\right) \tag{2.5}$$

the shift in E_F is approximately given by [20]

$$E_F(T) - E_F^0 = -\frac{1}{6}\frac{m(2kT)^2}{N\left(E_F^0\right) - mE_F^0 + \frac{1}{2}m\left(E_F^0 + E_F\right)} \tag{2.6}$$

where E is energy, $N(E)$ is density of states, $E_F^0 = E_F(0)$ is the Fermi energy level at 0 K, m is a constant, T is temperature, and $k = 8.63\times10^{-5}$ eV K^{-1} is the Boltzmann

constant. For a density of states that increases by a factor of 100 over 100 meV (4 kT), the shift in E_F between 0 K and room temperature is only about 40 meV [20]. An implicit assumption usually made is that E_F shifts linearly with T [20, 61]:

$$E_F(T) = E_F^0 - \beta T \tag{2.7}$$

where $\beta = 2.2\times10^{-4}$ eV/K [31].

2.2.3 Role of Hydrogen in Hydrogenated Amorphous Silicon

As seen in electron spin resonance (ESR) experiments, a-Si produced by sputtering or evaporation, without hydrogen, contains a large number (~ 10^{20} cm^{-3}) of dangling bonds [19]. Gap states associated with dangling bonds make a-Si insensitive to dopants. When hydrogen is added, hydrogen bonding to the dangling bonds removes the singly occupied states from the gap. In terms of the short range chemical picture, strong Si–H bonds replace weak Si–Si bonds and terminate dangling bonds and thus remove states from the gap [41]. Consequently, the optical gap increases with hydrogen content from about 1.5 eV in a-Si to around 2.0 eV at 30% hydrogen [56, 57].

The photoemission experiments [62, 63] and theoretical work [64] suggested that addition of hydrogen to the a-Si would remove states from the top of the valence band that causes widening of the gap. Increasing the hydrogen content yields to further widening of the gap by removal of states from the valence band edge [65]. This suggestion has been confirmed theoretically by comparison of the densities of states for structures that contain increasing amounts of hydrogen [66-68]. As hydrogen is added, the gap widens by receding the valence band edge as Si–Si bonds are replaced by stronger Si–H bonds, but the conduction band edge remains the same. This difference may explain the large asymmetry in electron and hole mobilities, and also other observations which indicate a high concentration of states near the valence band edge [20].

2.2.4 Conduction Mechanisms in Amorphous Silicon

Because of the high density of states in the band tails, it is not possible to move the Fermi level beyond the mobility edge of amorphous semiconductors. In the doped a-Si:H the Fermi level moves into the band tails, but never closer than 0.1 eV from the mobility edge. So, there is no metallic conduction in amorphous material. There are three conduction mechanisms in the amorphous silicon:

2.2.4.1 Extended states conduction

This conduction mechanism is related to the thermally activated carriers in the extended states beyond the mobility edge (free carriers). The relationship for the conductivity in this case, in the absence of the space charge, uses the same Fermi-Dirac statistics as the crystalline semiconductors:

$$\sigma_{ext} = \sigma_{oe} \exp\left[-\left(E_C - E_F\right)/kT\right] \tag{2.8}$$

where σ_{oe} is the average conductivity beyond the mobility edge [1].

2.2.4.2 Band tail conduction

At zero temperature, there is no conduction in localized states. However, at higher temperatures tunnelling transitions occur between neighbouring localized states due to the spatial extent of the wavefunction. Hopping conduction in the band tail is given by

$$\sigma_{tail} = \sigma_{ot} \exp\left[-\left(E_{CT} - E_F\right)/kT\right] \tag{2.9}$$

where E_{CT} is the average energy of the band tail conduction path and is closer to E_F than is E_C. The prefactor σ_{ot} depends on the density of states and the overlap of the wavefunction and is smaller than σ_{oe}. However, the band tail conduction is significant, particularly at low temperatures where the larger exponential term has more effect than the smaller prefactor [1].

2.2.4.3 Hopping conduction at the Fermi level

Conduction at the Fermi energy level occurs by hopping from site to site when the density of states is large enough for significant tunnelling of electrons. The

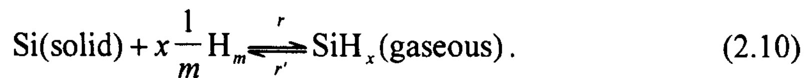
conductivity is small but weakly temperature-dependent and consequently this mechanism is dominant at lower temperatures. The conductivity is dependent on the defect states at the Fermi level and in a-Si:H where the density of states in the middle of the bandgap is very low, hopping conduction is virtually suppressed [1].

2.2.5 Preparation of a-Si:H

There are different methods for preparing a-Si:H among which the glow discharge (GD) decomposition of silane gas is the most common method. These methods can be divided in two categories: chemical vapour deposition (CVD) and physical vapour deposition (PVD).

2.2.5.1 Chemical Vapour Deposition

All CVD methods for the preparation of amorphous silicon are based on the decomposition of a silicon-hydrogen compound from gaseous phase. The following equation shows this reaction [6]:



$$\mathrm{Si(solid)} + x\frac{1}{m}\mathrm{H}_m \underset{r'}{\overset{r}{\rightleftharpoons}} \mathrm{SiH}_x\mathrm{(gaseous)}. \qquad (2.10)$$

The reaction is not only in the direction of deposition (decomposition of the gaseous phase) but also in the direction of etching of the solid (formation of the gaseous phase). The reaction factors r and r' are influenced by the temperature of the solid or gaseous phase, gas pressure, gas flux, etc. [69, 70].

The simplest CVD method is the thermal decomposition of silane gas. This method is used at high temperatures (above 850 °C) to make polycrystalline or epitaxial silicon [1]. Amorphous films can be grown in this way if the temperature is less than about 550 °C, but these films are mostly of low quality because the temperature is too high to retain the hydrogen [1]. However, to obtain a sufficient deposition rate a substrate temperature more than 500 °C must be used [71]. At this temperature at most a few percents of hydrogen will be incorporated and a high defect a-Si (at higher temperatures also c-Si) will be deposited [6]. To enhance quality, post-hydrogenation is necessary [72], but the quality of these films is much

lower than GD material. Scott, Plecenik, and Simonyi in a method called homogeneous CVD (HOMCVD) used separate thermal decomposition and deposition steps at about 650 °C and 300 °C respectively [73, 74]. The quality of a-Si:H obtained in this way is reasonable but the deposition rate is very low (0.1 $\mu m\ hr^{-1}$).

The usual method of depositing a-Si:H is the so-called plasma-enhanced CVD (PECVD). In this process the plasma is the source of energy to dissociate the silane molecule instead of the thermal energy, and so, the deposition can be performed at lower temperatures. The first plasma deposition system for amorphous silicon was developed by Chittick, Alexander, and Sterling, in which a radio frequency (RF) induction coil outside a quartz chamber was used to create the plasma [5]. Although different plasma techniques have been used, the decomposition of silane in an RF GD is the most commonly used method [5, 75, 76]. The RF power can be supplied by capacitive or inductive coupling to the reactor chamber. For large area deposition, a capacitively coupled system is more suitable [6]. The deposition of the films takes place on both electrodes, however, the a-Si:H films obtained on the grounded anode have better quality [6]. There are many parameters in the deposition process which must be controlled to give good material, such as the reactor design, the process gas purity, the gas pressure, the gas flow rate, the RF power, and the temperature of the substrate [1, 6]. The deposition rate ranges from about 0.1 – 1 $nm\ s^{-1}$ and is approximately proportional to the RF power. The hydrogen content ranges from 8 to 40% and decreases as the substrate temperature is raised. The hydrogen content also depends on the RF power and the composition of the gas. The defect density also depends on the substrate temperature and the RF power and can vary by more than 3 orders of magnitude. The lowest defect density is obtained with the substrate temperature between 200 and 300 °C and at low powers [1].

The energy needed for the dissociation of disilane or higher silane gases can also be supplied by ultra violet (UV) light or laser illumination in a process called photochemical vapour deposition (photo-CVD) [1, 6]. UV light can be used for the initial dissociation of the silane gas, which either excites the silane directly [1], or by energy transfer from mercury vapour introduced in the chamber [77-79].

Subsequently laser excitation was used in the technique called laser-induced CVD (LiCVD) [80-82]. LiCVD has similarities to HOMOCVD [73, 74], however, the process gas is directly heated by laser beam absorption in front of the substrate. The advantages of photo-CVD and LiCVD are the absence of high energy particles, the bombardment of the growing film by ions from the plasma, and the selected excitation [1, 6]. However, they have the disadvantage of the low rate deposition and the complicated experimental arrangement. For this reason, these methods are only used for special very thin device layers [6].

2.2.5.2 Physical Vapour Deposition

In the physical vapour deposition (PVD) methods, the amorphous silicon film is produced by a sputter or evaporation process. It is very simple to produce a-Si films with high deposition rate by these methods. However, obtaining a low defect a-Si:H material is not completely straightforward and needs further reactive processes, usually in the presence of a plasma [6].

In the reactive sputtering (SP) method of depositing a-Si:H, a silicon target is sputtered, usually with argon ions, in the presence of hydrogen. The sputtered silicon reacts with the atomic hydrogen in the plasma, forming SiH_x radicals from which deposition takes place. The deposition process is very similar to glow discharge and the sputtered films have essentially the same properties as the plasma deposited materials, however, the ion bombardment damage may be more because of higher energy of the ions reaching the surface [1]. Although the SP a-Si:H material has the same application potential as GD a-Si:H, the former suffers from more surface or interface problem. If the same material and device quality can be obtained, the dc sputtering technique would be favourable for large area applications as less energy, less poisonous gas and no explosive gas are needed [6]. The properties of the SP a-Si:H films are sensitively dependent on the following parameters: argon and hydrogen partial pressure, base pressure, substrate temperature, target-substrate distance, and rf power [83].

Evaporation techniques (EV) have often been used for the preparation of a-Si and it is very difficult to grow a-Si:H by this method [6]. The deposition of a-Si:H

needs a reactive evaporation with an atomic hydrogen treatment [84, 85], however, the defect density in evaporated a-Si can be reduced by a hydrogen plasma annealing treatment [86] or by reactive evaporation in a hydrogen atmosphere [87].

2.2.6 Applications of a-Si:H

The a-Si:H-based solid state devices are not comparable with their crystalline counterparts, regarding to precision, speed and power density. However, because of low cost fabrication, low temperature processing, and large area production, a-Si:H has a large number of applications. These applications range form photovoltaic devices or solar cells, photoreceptors, photoconductors, image sensors, optical recording, charge-coupled devices (CCD), and memory switches, to widely used TFTs in displays and high voltage TFTs used in printers [6, 88-90], among which the solar cells and thin-film transistors (TFT) have more importance.

The first and one of the most important applications of a-Si:H is in solar cells because of its large absorption coefficient, high conversion efficiency, low cost, and its ability to be deposited over large areas by mass production [6, 15]. To obtain high conversion efficiency it is necessary to have a low DOS in the mobility gap and as a result a large mobility-lifetime product [6]. Different device structures have been used for the single junction solar cells, however, they can be classified into three main types, namely p-i-n, MIS, and Schottky barrier cells [6]. The higher conversion efficiency has been achieved from large area interconnected single-junction modules [91]. Even much higher conversion efficiency is attainable using tandem or multigap solar cells by depositing stacked solar cells with different optical gaps which enables a selective absorption of the sunlight [6].

Another important application of a-Si:H is in thin-film transistors (TFT) which are widely used in the active matrix liquid crystal displays (AMLCD). In the next section, the various aspects of the TFTs are described in more details.

2.3 THIN-FILM TRANSISTORS

2.3.1 Historical Background

The first thin film transistor was invented by Lilienfield [92-94] in 1925, many years before the invention of bipolar and field effect transistors [95]. Lilienfield's devices would not have worked, but Heil [96] made an apparently independent patent application in 1935, describing a thin film field effect transistor [95, 97]. Heil proposed the use of tellurium, cuprous oxide, vanadium pentoxide and other similar materials, and may have built the first solid state amplifier [97]. In 1961 Weimer described the first successful vacuum deposited thin film field effect transistor using CdS as the semiconductor [98]. Weimer and his group in RCA continued to work on the TFTs [99-101]. In 1967, Brody and Page in Westinghouse made Tellurium TFTs on paper, aluminium foil, and other flexible substrates [102-104]. A successful 180-stage thin film integrated circuit using CdSe TFTs was reported by Weimer in 1966 [105]. In 1979, Le Comber *et al.* proposed amorphous silicon thin-film transistors for device applications [106].

2.3.2 Materials Used in Thin-Film Transistors

Although different materials such as tellurium and CdSe have been used in thin-film transistors [96], the main stream of the TFT technology is a-Si:H and polycrystalline silicon, because of their low cost, ability to be deposited on large areas, and better electrical properties [107]. Polycrystalline silicon has the advantage of higher carrier mobility. However, it suffers from high leakage current [108-112]. Hydrogenated amorphous silicon has much lower carrier mobility than polycrystalline silicon, but the leakage current of a-Si:H TFTs is lower and they provide higher on-off current [113]. Since a-Si:H deposition is performed at lower temperatures, it can be deposited on ordinary glass, making the device process cheaper [114]. There are some efforts to improve the carrier mobility of a-Si:H, and a parallel effort to reduce the leakage current of polysilicon TFTs. However, a-Si:H is the dominant material used in the pixel drive TFTs in liquid crystal displays, while polysilicon TFTs are mostly used in peripheral circuitry [115, 116].

In the last decade, there has been a great interest in using organic semiconductors in thin-film transistors [117-121]. However, because of the low carrier mobility in these materials, more research on their quality is still needed to make the application of the organic TFTs as widespread as their a-Si:H counterparts.

2.3.4 Applications of Thin-Film Transistors.

The main application of thin-film transistors is as switch elements in the active matrix of liquid crystal displays. The other important applications are in large area electonics such as image sensors and printers, fundamental logic circuits [122-126], and load device in static random access memories (SRAMs) [109, 127, 128]. The important applications of organic TFTs are in smart cards, flexible displays, and radio frequency identification tags [129].

2.3.5 Thin-Film Transistor Structures

A wide variety of structures have been use for thin-film transistors. These structures can be divided to two main categories, planar and vertical structures. In the planar structures, the semiconductor film is in parallel with the substrate, while in vertical structures it is perpendicular to the substrate. There are different structures in each category that are described briefly in the following sections.

2.3.5.1 Planar Structures

Basically, there are four types of planar structures depending on the order of deposition of the semiconductor layer, the gate insulator layer, the source and drain contacts, and the gate electrodes [130]. In the coplanar structures, all the gate and drain/source electrodes are situated in the same side of the semiconductor, while with staggered structures, the gate is in one side and drain and source contacts are located on the opposite side. In the inverted structure, the gate is underneath the insulating layer. The four different planar structures of thin-film transistors are shown in Fig. 2.4. For each structure there are still many different TFT technologies [130]. The inverted-staggered is the most popular structure for a-Si:H TFTs [130].

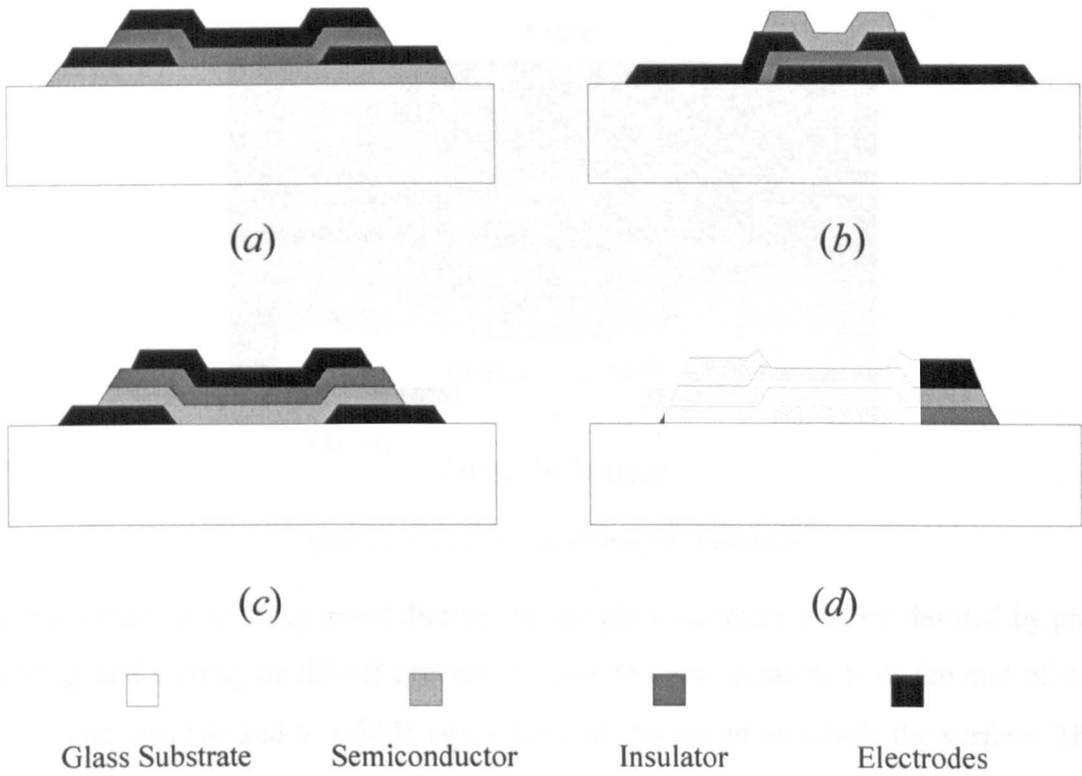


Figure 2.4 Different planar TFT structures, (a) coplanar, (b) inverted-coplanar, (c) staggered, and (d) inverted-staggered. (after Powell [130]).

2.3.5.2 Vertical Structures

The speed of TFTs in a circuit is proportional to μ/L^2 for zero gate overlap, where μ is the carrier mobility and L is the channel length. The a-Si:H suffers from low carrier mobility and one method to increase the speed of a-Si:H TFTs is by reducing the channel length. However, the reduction in channel length is limited by lithography. The vertical TFT (VTFT) structure can overcome this limitation, because the a-Si:H film is deposited vertically relative to the substrate. Therefore, the channel length is independent of lithography process.

From the author's knowledge, the first a-Si:H vertical TFT was reported by Uchida *et al.* in 1984 [131]. Since then, different vertical structures have been published for both a-Si:H and polysilicon TFTs [132-137].

2.3.6 Demonstration of a Vertical a-Si:H TFT

As an example, a vertical structure proposed by Prof. W. Eccleston for a-Si:H TFT is presented in this section. The structure is shown in Fig. 2.5. The drain and

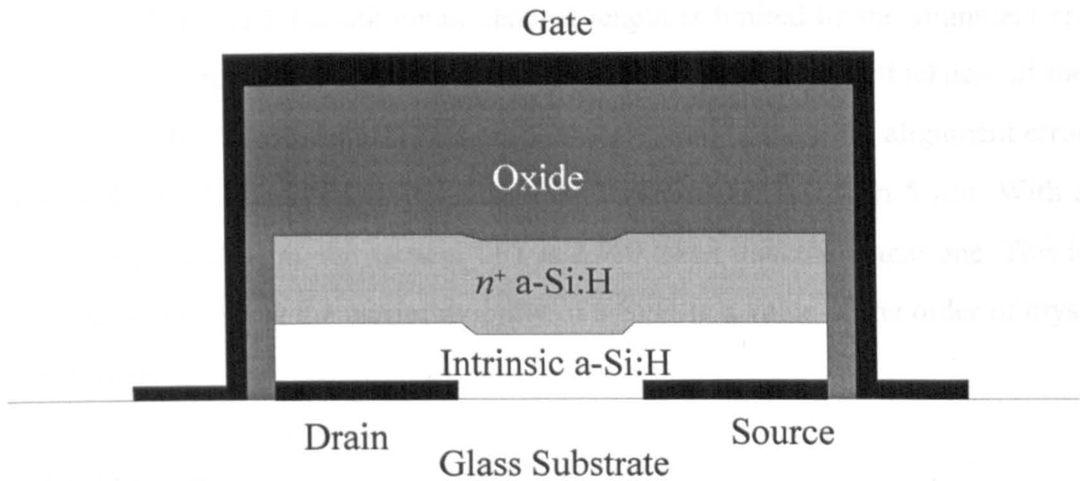


Figure 2.5 A vertical a-Si:H thin-film transistor.

source contacts are evaporated directly on the glass substrate and are defined by patterning and etching or lift-off process. Access to these contacts is at the end of device. The intrinsic and n^+ a-Si:H layers then are deposited on whole the surface. The top oxide can be deposited on the n^+ layer or grown by thermal oxidation. In the next step, the oxide, n^+ and intrinsic a-Si:H, and drain and source metals in unwanted areas are etched dawn to glass substrate, successively. A thin layer of gate oxide is grown by plasma oxidation. The gate metal is then evaporated on the entire device, with overlaps to the glass substrates.

They also provide heat sinks adjacent to the channel to prevent overheating due to lack of substrate connection. The channel consists of two parts, connected in series by the relatively thick n^+ bridge. Therefore, two combined channels appear as a single channel. The junction between the n^+ bridge and intrinsic channels inhibits the hole current when the transistor is turned off. The capacitance between gate and drain/source contacts depends on the thickness of drain/source contacts, and therefore is very small. The thick layer of top oxide reduces the capacitance between gate and n^+ bridge. The capacitance between gate and channel is very small when the channel is short.

There may be a large leakage current through the bulk in the wide areas between drain/source contacts and n^+ bridge. To reduce this leakage current, the width of drain/source contacts should be decreased to minimum feature size.

In a planar TFT the minimum channel length is limited by the alignment error, while in a vertical structure the channel length is determined by thickness of the a-Si:H layer. The speed of the TFT is proportional to $1/L^2$. If a 5 μm alignment error is assumed, the channel length in a planar TFT can not be less than 5 μm. With a channel length of 0.1 μm, the vertical TFT is 2,500 faster than the planar one. This is equivalent to increasing the carrier mobility of a-Si:H to a value of the order of crystalline silicon.

2.4 SUMMARY

The properties of hydrogenated amorphous silicon and a-Si:H thin-film transistors have been reviewed. Pure amorphous silicon was reported first by Haas in 1947, and a-Si:H was prepared by Chittick *et al.* in 1969. The first a-Si:H TFT was made by Le Comber, Spear, and Gaith in 1979.

The atoms in a-Si:H have the same short range order as in crystalline silicon. Therfore, a-Si:H has a considerable bandgap. the long range disorder of atoms in a-Si:H introduces broadened band tails in the mobility gap, and the states in the middle of the mobility gap are produced by coordination defects.

Introducing hydrogen into a-Si:H reduces the defect states in the middle of mobility gap by removing dangling bonds. The mobility gap is increased by incresing the hydrogen in the film.

There are three different conduction processes in a-Si:H; conduction in the extended states, hopping conduction in localized states in band tails, and hopping in the states in the middle of mobility gap.

There are different methods for preparing a-Si:H that can be divided in two categories; chemical vapour deposition (CVD), and physical vapour deposition (PVD). The most common method to prepare a-Si:H is glow discharge (GD) or plasma enhanced chemical vapour deposition (PECVD), which provides the best quality material.

The main application of a-Si:H is in thin-film transistors. There are many other applications and the most important of them are solar cells.

The first thin-film transistor was invented by Lilienfield in 1925. The first a-Si:H TFT was proposed by Le Comber *et al.* in 1979.

Polysilicon and a-Si:H are the main materials in thin-film transistors. In recent years there has been some interest in using organic semiconductors in TFTs.

The main application of thin-film transistors is as a switching element in active matrix crystal displays (AMLCDs). Some other important applications are image sensors and printers.

Coplanar, inverted-coplanar, staggered, and inverted-staggered are four structures used in coplanar TFTs, among which the inverted-staggered structure is the most popular. Vertical TFT structures can provide submicron channel lengths, without any limitation due to the lithography process.

The properties and process of a vertical a-Si:H thin-film transistor have been explained.

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CHAPTER THREE

MODELLING OF THE STEADY-STATE SPACE-CHARGE-LIMITED CURRENT IN HYDROGENATED AMORPHOUS SILICON

3.1 INTRODUCTION

The current-voltage measurements can be used to provide useful information about the properties of the hydrogenated amorphous silicon (a-Si:H) and its interface to the other materials. The experimental results, described in Chapter 4, suggest that the dominant conduction mechanism in the bulk of a-Si:H is space-charge-limited current (SCLC). The steady-state SCLC is a reliable method to investigate the density of states in the mobility gap of a-Si:H. The density of states is important in characterizing the quality of material grown by various methods and is a basis for understanding electronic devices. An understanding of the effect of the density and energy level of the trap states and the other parameters such as film thickness, metal

contacts, temperature, etc. on the current-voltage characteristics can help to solve the reverse problem, i.e. determining the density of states from the *I-V* plot. This chapter deals with the modelling of a device, similar to the one used in the experimental work to measure the *J-V* characteristics (chap. 4), using the Medici™ device simulation program.

The steady state space-charge-limited current measurement has extensively been used in a-Si:H to provide information about the bulk density of states (DOS) in the mobility gap [1-17]. The method was first applied by den Böer, on glow-discharge (GD) deposited samples with an n^{+}-i-n^{+} sandwich structure [1]. Later, the method was used by the other workers, mostly on the glow-discharge samples [2-14] and also on evaporated [15, 16] and sputtered [16, 17] samples to determine the DOS in the mobility gap.

The basis of the SCLC method was established by the work of Rose [18] and Lampert and Mark [19, 20]. These authors have shown that the plot of current-voltage (*I-V*) characteristics reflects the distribution of trap levels and so, in principle, the trap parameters can be extracted from the non-linearities of this plot. Any distribution of traps in the mobility gap can produce a unique plot of *I-V* characteristics, however, deriving the exact distribution of trap states from this plot is not straightforward. All the methods of determining the density of states from the SCLC plot are based on some assumptions and a prior knowledge of the shape of energy distribution of traps [14]. In addition, mapping from the *I-V* characteristics to the density of states-energy plot is not unique, i.e. many distributions of traps may produce the same plot. Nešpurek and Sworakowski have shown that discrete trap levels can be reproduced as bell-shaped distributions with half-widths of 3.5 kT [21]. One can expect that this distribution produces the same *J-V* characteristics as does a discrete trap. The SCLC method has some other limitations that will be discussed in more detail in the present chapter, however, it is more appropriate for determining the bulk density of states in the intrinsic a-Si:H than other methods such as deep level transient spectroscopy (DLTS) or the field-effect (FE) [22]. The latter is rather insensitive to the variations in the distribution function [23] and measures both bulk and

surface (interface) states [24]. The former is better suited to measuring doped material [22].

The SCLC measurements are mostly made on sandwich structures of metal-n^+-i-n^+-metal [1-3, 7, 9, 12-14, 21] or metal-p^+-i-p^+-metal [10, 13] type. The heavily doped layers provide Ohmic contacts to improve the injection of electrons (n^+-i-n^+) or holes (p^+-i-p^+) into the intrinsic layer. Voltage applied to such structures establishes a one-carrier current, which is the case in nearly all the investigations, since the analysis of two-carrier injection is more complicated. In the case of the n^+-i-n^+ structure, the electrons are injected from the n^+ layer (injecting contact) into the intrinsic region and the counter n^+ layer blocks the injection of holes (and vice versa for a p^+-i-p^+ structure). In most of the investigations, the space-charge-limited current was obtained using n^+-i-n^+ structures where at sufficiently high voltages, the electrons injected from the Ohmic contacts and trapped in the states above midgap raise the electron Fermi level. Dawson *et al.* [10], and Nebel and Street [13] have used p^+-i-p^+ structures in which the density and energy distribution of gap states below midgap in intrinsic a-Si:H are obtained from the SLSC of holes. Krühler *et al.* [25] observed SCLC in a-Si:H using lightly doped materials in the form of p-π-p structures. However, since even light boron doping of a-Si:H introduces a large number of midgap defect states [26], the DOS determined using these structures does not correspond to that in intrinsic a-Si:H. Some of workers have used metal-semiconductor-metal structures without heavily doped contact layers [6, 16], but providing a good Ohmic contact between metal and intrinsic semiconductor is not always possible, and these structures are usually used only in the case of doped materials. Gangopadhyay *et al.* [16] have used a Cr/a-Si/a-Si:H/a-Si/Cr configuration. They have claimed that the deposition of unhydrogenated amorphous silicon layers between the a-Si:H and chromium contacts has provided a good Ohmic contact without any phosphorous cross-contamination that can easily occur after deposition of highly phosphorous doped n^+ layers in the same chamber. Weisfield [6] has also used an unhydrogenated a-Si layer on nichrome coated glass as a conducting back contact. Soh *et al.* [11] have used a-Si:H TFTs to measure SCLC in low gate voltages.

Throughout this text, only one-carrier (electron) injection will be discussed, as the experiments have been performed on the SCLC of electrons. The SCLC of holes can be performed by a similar manner. The two-carrier injection has rarely been used because recombination should also be considered making the problem more complicated.

3.2 OUTLINE OF THE STEADY-STATE SCLC

Space-charge-limited current arises from the situations where the injected charge carriers build up a non-uniform distribution of excess charge between the contacts or plates due to something such as low mobility or a high density of traps. This excess space charge results in a nonlinear electrical field across the sample, which produce a nonlinear relationship between voltage and current instead of a linear, Ohmic relationship.

At low applied voltages the excess space-charge (and consequently the Fermi level shift) is negligible compared to the thermally-generated free electrons, and therefore there is an Ohmic relationship between current and voltage, or there is a slope of one in a log$J$-log$V$ plot (region a in Fig. 3.1). At higher voltages the injected electrons dominate the thermally-generated free electrons and the current becomes space-charge-limited and is proportional to V^2. Therefore, the log$J$-log$V$ plot has a slope of two in the SCLC region. In the presence of traps, when the Fermi level lies below the trap energy level (shallow trap), some of the injected electrons occupy the trap states and the space-charge consists of both free and trapped electrons. However, the concentration of trapped electrons is usually much higher than that of free electrons and the current is mostly determined by the SCLC of trapped electrons (region b in Fig. 3.1).

By increasing the applied voltage, the Fermi level shifts towards the conduction band mobility edge E_c and the concentration of both free and trapped electrons increases by nearly the same rate. However, when the Fermi level is very close to the trap energy level (Fermi pinning) or higher than the trap energy level (deep trap), the free electron concentration increases with a higher rate than that of trapped electrons.

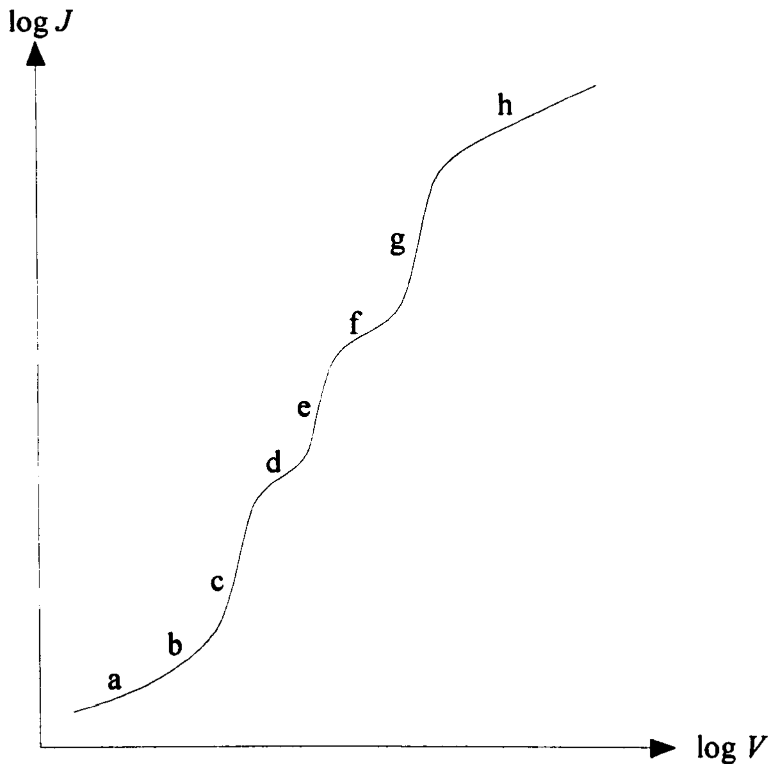


Figure 3.1 A typical log-log plot of current density versus applied voltage in the case of space-charge-limited current.

This causes the current to increase more rapidly with applied voltage, resulting in a rise in the slope of the curve in the log$J$-log$V$ plot. In this case, the trap is virtually full, the trapped electron concentration is nearly constant, and increasing the applied voltage causes only the free electron concentration to be increased. This is called the trap-filled-limit (TFL) situation (region c in Fig. 3.1).

In the case of multiple discrete trap levels, when the Fermi level approaches to the next trap level, the injected electrons occupy the new trap states and current will be space-charge-limited again (regions d and f in Fig. 3.1), and there will be a trap-filled-limit region after each SCLC region (regions e and g in Fig. 3.1).

When the Fermi level is above the highest trap level, all trap states are virtually filled, and by increasing the applied voltage only the free electron concentration increases. Above a certain point, the free electron concentration is much more than the concentration of total trapped electrons concentration, and the situation is similar to the space-charge-limited current with no traps. Hence, this region is called trap-free region (region h in Fig. 3.1).

3.3 THEORY OF SCLC

The theory of SCLC is based on the work of Rose [18] and Lampert and Mark [19] and has been described in full detail by Lambert and Mark [20]. To study the conduction mechanism in different cases, a specimen is of thickness d is assumed to exist between two parallel electrodes with very large dimensions compared to d. Both contacts between electrodes and the specimen are assumed Ohmic. In the beginning, we consider the simplest case, a material with high conductivity and without any traps.

3.3.1 A Trap-Free Material with High Conductivity

A very conductive material is one with high concentration of free carriers and high mobility, like a metal or a doped semiconductor. Before applying any voltage, the thermally generated free carriers, for example free electrons, with concentration n_0 are uniformly distributed throughout the material. By applying an external voltage, electrons will inject from cathode to the material and will produce a space-charge region. The width of the space-charge region is inversely proportional to the conductivity of the material [20], and so there will be a very narrow space-charge region in the vicinity of the cathode electrode. In the rest of the specimen the concentration of the excess electrons is negligible compared to that of thermally generated free electrons, so the concentration of free electrons and consequently the position of Fermi level remain nearly unchanged. There is no significant diffusion current and the only current mechanism in the material is drift

$$J = n_0 q\mu_0 \mathcal{E} = n_0 q\mu_0 (V/d), \tag{3.1}$$

where J is the current density, $q = 1.6 \times 10^{-19}\,\mathrm{C}$ is the electronic charge, μ_0 is the mobility of free electrons, $\mathcal{E}$ is the electric field intensity, V is the applied voltage, and d is the thickness of the specimen. Since n_0 is nearly constant, the current density is proportional to the electric field density and $\mathcal{E}$ is constant throughout the material (Ohm's law).

3.3.1 The Perfect Insulator

In the next step, we consider a perfect insulator with no traps and negligible thermally generated free carriers. When a voltage is applied across the sample, electrons are injected form cathode to the conduction band of the material and build up a space-charge region. The injected electrons are the only carriers that contribute to the current, because the thermal-free electrons are assumed negligible. The concentration of the injected electrons is maximum near the cathode and decreases with the distance from cathode to anode. Hence, the free electron concentration n_f and electric field density $\mathcal{E}$ are both functions of the distance from cathode to anode x. In the theory of SCLC the diffusion currents have always been neglected and only pure drift current has been used as total current. Diffusion currents have considerable values only in the immediate neighbourhood of the contacts and neglecting them does not have an essential role in deriving the bulk current [20]. With this assumption the current density can be written as

$$J = n_f(x) q\mu_0 \mathcal{E}(x) = \text{constant}. \tag{3.2}$$

The electron concentration n_f can be found using Poisson's equation

$$n_f(x) = \frac{\varepsilon}{q}\frac{\partial^2 V(x)}{\partial x^2} = \frac{\varepsilon}{q}\frac{\partial \mathcal{E}(x)}{\partial x}, \tag{3.3}$$

where $\varepsilon = \varepsilon_r \varepsilon_0$ is the permitivity of the material, $\varepsilon_0 = 8.85\times10^{-14}$ F/cm is the permitivity of the vacuum, and ε_r is the dielectric constant. By substituting (3.3) into (3.2)

$$J = \varepsilon\mu_0 \mathcal{E}(x)\frac{\partial \mathcal{E}(x)}{\partial x}, \tag{3.4}$$

$\mathcal{E}$ can be found by integrating both sides of the equation

$$\mathcal{E}(x) = \frac{\partial V(x)}{\partial x} = \left(2J/\varepsilon\mu_0\right)^{1/2} x^{1/2}, \tag{3.5}$$

and $V(x)$ can be found by integrating (3.5)

$$V(x) = \frac{2}{3}\left(2J/\varepsilon\mu_0\right)^{1/2} x^{3/2}. \tag{3.6}$$

If d is the thickness of material, or the separation between cathode and anode, the voltage difference between anode at $x = d$ and cathode at $x = 0$ equals the applied voltage V, and so

$$J = \frac{9}{8}\varepsilon \mu_0 \frac{V^2}{d^3}. \tag{3.7}$$

Equation (3.7) is the famous Child's law for a perfect insulator and indicates that in the SCLC regime, current is proportional to the applied voltage squared and log$J$-log$V$ plot has a slope of two.

Using (3.3) and (3.5), the variation of the free electron concentration with x can be found

$$n_f = \left(\varepsilon J / 2q^2 \mu_0\right) x^{-1/2}. \tag{3.8}$$

In the above equations, as we have just been concerned about the absolute value of the variables, their polarity has been omitted. In Eqn. (3.8) the concentration of free electrons at $x = 0$ is equal to infinity, however n_f has a limited maximum value that depends on the concentration of thermal-free electrons in the cathode contact. In Fig. 3.2, Electrical field intensity, voltage, and free electron concentration are plotted

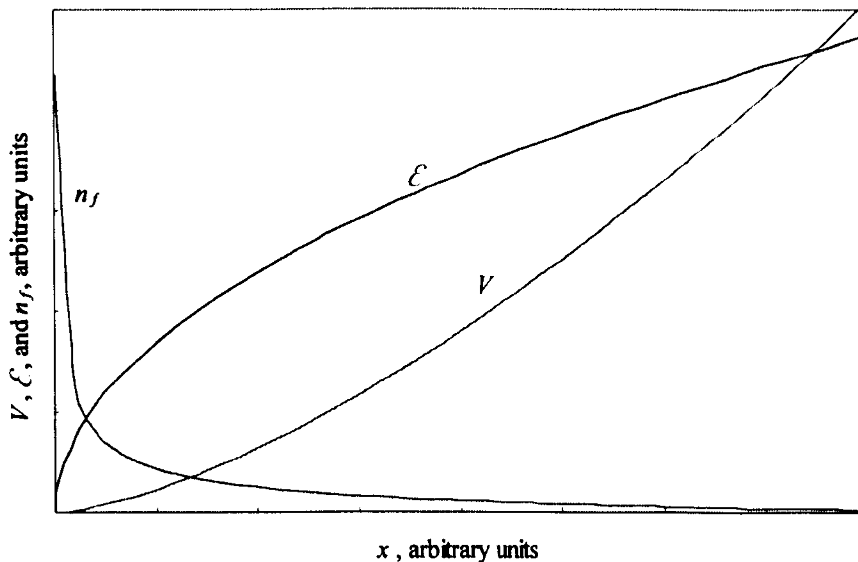


Figure 3.2 Voltage V, electric field intensity $\mathcal{E}$ and free electron concentration n_f as a function of distance x in a perfect insulator.

as a function of x. It can be seen that n_f has a very steep slope only in the area close to the cathode contact, and so, neglecting the diffusion current does not have a significant effect on the bulk current.

3.3.2 The Trap-Free Material with Thermal-Free Electrons

Now we include the thermally generated free electrons with concentration n_0 in the problem. The space charge in this situation is the excess injected electrons, or the difference between the total free electrons n_f and the thermally generated free electrons n_0. The concentration of excess free electrons is maximum at $x = 0$ and approaches zero as x increases. Poisson's equation in this case can be written as

$$n_f(x) - n_0 = \frac{\varepsilon}{q}\frac{\partial^2 V(x)}{\partial x^2} = \frac{\varepsilon}{q}\frac{\partial \mathcal{E}(x)}{\partial x}. \qquad (3.9)$$

It is impossible to find an exact analytical relation between current density and applied voltage, instead they can both be expressed as functions of the parameter $n_0/n_f(x)$ [20]. Lampert and Mark [20] have used a regional approximation to find such a relationship. A schematic plot of the concentration of total and excess free electrons is shown if Fig. 3.3 for a rather low applied voltage. For any value of current density

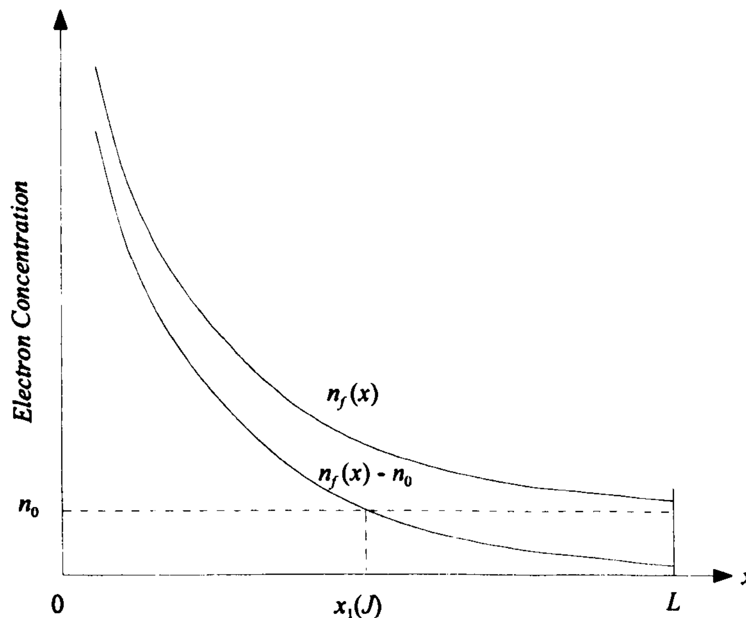


Figure3.3 The variation of excess injected electrons concentration and total electrons concentration between cathode and anode. (after Lampert and Mark [20]*).*

J, there is a plane at $x = x_1$ between cathode and anode that the concentration of injected electrons is equal to the concentration of thermal-free electrons n_0. At $x << x_1$, the concentration of thermal-free electrons n_0 is much lower than that of injected electrons and can be neglected. The injected electrons concentration can be approximated to the total electrons concentration and the Poisson equation (3.9) changes to (3.3). At the other extreme, at $x_1 << x < d$, the concentration of injected electrons compared to n_0 is so low that the space-charge in this region can be neglected and Ohm's law can be applied.

The current, in general, is neither pure space-charge-limited nor Ohmic, however using the regional approximation, relationships between current and voltage can be found for two ranges of low and high applied voltages. Lampert and Mark [20] have calculated the distance x_1 as a linear function of current density

$$x_1 = \varepsilon J / 2q^2 n_0^2 \mu_0 \,. \tag{3.10}$$

At low applied voltages, the current is very low, the space-charge region is very narrow, and the concentration of free electrons in most of the film is approximately equal to constant value n_0. So, by neglecting this small region and small voltage drop across it, an Ohmic relationship between current and voltage can be found. By increasing the applied voltage the space-charge region extends towards the anode and at a specific value of applied voltage the concentration of the excess injected free electrons becomes equal to n_0 (or $x_1 = d$). At higher voltages, the concentration of injected free electrons may be so much higher than n_0 that the latter can be neglected. This situation is similar to the perfect insulator with negligible thermal-free electrons and the current becomes space-charge-limited.

By equating the right hand sides of equations (3.1) and (3.7), voltage V_X, the intercept of the Ohmic and SCL regions, will be found that can be considered as the onset of the SCL region

$$V_X = \frac{8}{9}\frac{q n_0 d^2}{\varepsilon} \,. \tag{3.11}$$

Lampert and Mark [20] have calculated a critical voltage and current at which the concentration of excess free electrons at the anode becomes equal to the concentration of thermally generated free electrons (or $x_1 = d$)

$$V_{cr} = \frac{4}{3}\frac{qn_0 d^2}{\varepsilon}, \tag{3.12a}$$

$$J_{cr} = 2q^2 n_0^2 \mu_0 d/\varepsilon. \tag{3.12b}$$

The critical voltage is very close to V_X in equation (3.11). This is expected since they have the same physical significance.

In section 3.3.1 it was mentioned that in a material with high conductivity the effect of space charge can be ignored. Eqn. (3.10) shows that when conductivity ($\sim n_0\,\mu_0$) is very high, even at high currents x_1 remains small enough to neglect the effect of space-charge, and current-voltage relationship is Ohmic at any current level.

3.3.3 The Material with a Single Set of Shallow Traps

In the next step we include a single set of traps with density of N_t at the energy level E_t, well above the Fermi level (shallow trap). When no voltage is applied, some of the trap states are occupied with thermally generated free electrons. In the thermal equilibrium condition, the concentration of free electrons n_0 can be expressed by Boltzmann statistics

$$n_0 = N_c \exp\left[-\left(E_c - E_{F0}\right)/kT\right], \tag{3.13}$$

where N_c is the effective density of states at the conduction band mobility edge E_c, E_{F0} is the Fermi level for electrons, $k = 1.38\times10^{-23}$ J/K is the Boltzmann constant, and T is the temperature in Kelvin. The concentration of occupied traps (trapped electrons) in thermal equilibrium n_{t0} is given by the Fermi-Dirac expression

$$n_{t0} = \frac{N_t}{1+\left(1/g\right)\exp\left[\left(E_t - E_{F0}\right)/kT\right]}, \tag{3.14}$$

where g is degeneracy factor (statistical weight) for the traps. Lampert and Mark [20], throughout their text have assumed $g = 2$, while in the other publications about SCLC in a-Si:H, g has not appeared; it has been assumed equal to 1 or has been ignored. However, it can simply be shown that the difference between two values of g makes a difference equal to $kT \ln 2 \approx 0.7\ kT$ in $E_t - E_{F0}$ which at 300 K is less than 0.02 eV. Hence, throughout the present text, g is assumed equal to 1.

When a voltage is applied, some of the injected electrons are captured by traps and the others remain in the conduction band. The density of total free electrons n_f and total trapped electrons n_t can be expressed by

$$n_f = N_c \exp\left[-\left(E_c - E_F\right)/kT\right], \tag{3.15}$$

$$n_t = \frac{N_t}{1+\exp\left[\left(E_t - E_F\right)/kT\right]}, \tag{3.16}$$

where n_f, n_t, and E_F are functions of distance x. The uncompensated space-charge in this case is the difference between the total concentration of free and trapped electrons, $n_f + n_t$, and the total concentration of free and trapped electrons in thermal equilibrium prior to the application of voltage, $n_0 + n_{t0}$. The Poisson's equation can be written as

$$\left(n_f - n_0\right) + \left(n_t - n_{t0}\right) = \frac{\varepsilon}{q}\frac{\partial^2 V(x)}{\partial x^2} = \frac{\varepsilon}{q}\frac{\partial \mathcal{E}(x)}{\partial x}. \tag{3.17}$$

The energy band diagram of the specimen at a rather low applied voltage is shown in Fig. 3.4*a*. The shape of energy band diagram depends on both the external field, due to the applied voltage, and the internal field, due to the space charge. The former bends the entire energy band, while the latter affects the position of the Fermi level relative to the conduction and valence bands. As we are concerned about the position of Fermi level, the energy band diagram has been redrawn in Fig. 3.4*b* with a flat Fermi level and band bending due to the external field has been omitted.

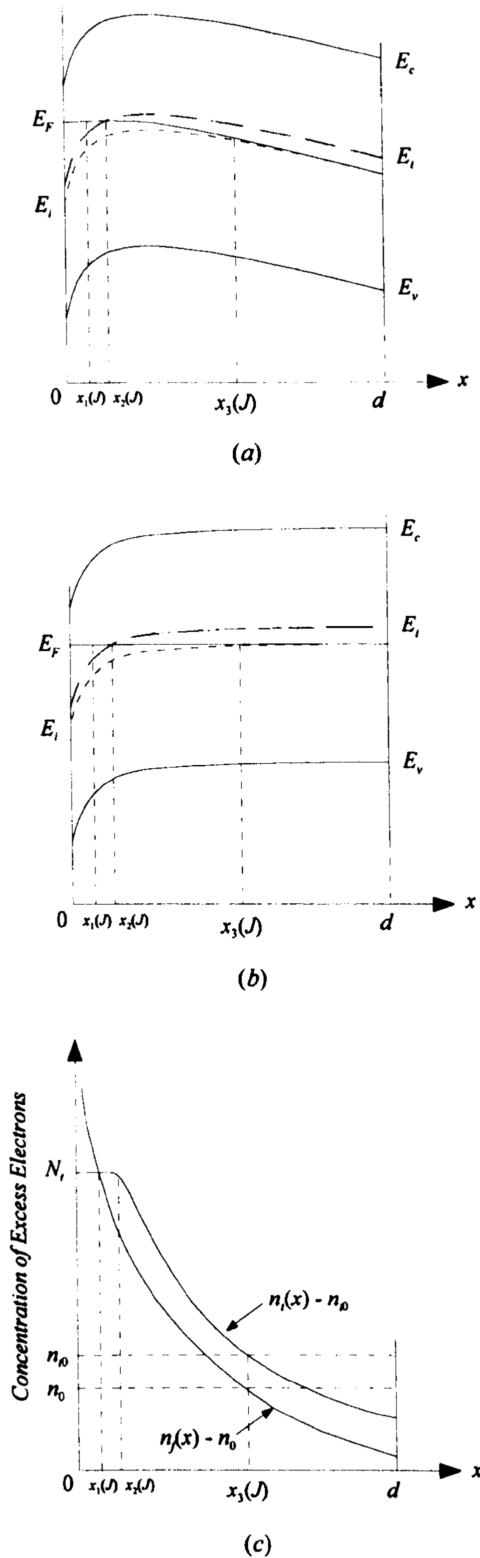


Figure 3.4 (a) Energy band diagram of a specimen with a single set of traps at a fairly low applied voltage, (b) Energy band diagram of (a) with flat Fermi level, (c) The concentration of free and trapped electrons versus distance between cathode and anode.

To find the current-voltage relationship, the regional approximation [20] can be used as in the trap-free case. At low applied voltages, for any value of current density J there is a plane at $x = x_3$ between cathode and anode, in which the concentration of injected excess free electrons $n_f - n_0$ is equal to the concentration of thermal-free electrons n_0 (Fig.3.4c). The Fermi level at this point is very close to the one in thermal equilibrium prior to applying voltage, and so well below the trap energy level (shallow trap). For shallow traps, the Fermi-Dirac expression for concentration of occupied states, Eqn. (3.16), can be approximated by Boltzmann statistics

$$n_t \approx N_t \exp\left[-\left(E_t - E_F\right)/kT\right]. \tag{3.18}$$

It can easily be shown that at $x = x_3$, the concentration of excess injected electrons captured by traps, $n_t - n_{t0}$, is equal to n_{t0}, the concentration of trapped electrons before applying voltage. In the region $x_3 < x < d$, $n_f - n_0 < n_0$ and $n_t - n_{t0} < n_{t0}$, and $n_f - n_0$ and $n_t - n_{t0}$ can be neglected. Therefore the space charge in this region is negligible and Ohm's law can be applied. For $x < x_3$, n_0 and n_{t0} are much smaller than n_f and n_t respectively, and can be neglected. So

$$\left(n_f - n_0\right) + \left(n_t - n_{t0}\right) \approx n_f + n_t = n_f\left(1 + n_t/n_f\right) = n_f/\theta, \tag{3.19}$$

in which

$$\theta = \frac{n_f}{n_f + n_t} \tag{3.20}$$

is the ratio of the free electron to total electron concentration.

There is a plane at $x = x_2$ in which the Fermi level passes through the trap energy level. From (3.16) it can be found that $n_t(x_2) = N_t/2$. For x sufficiently larger than x_2, when the Fermi level is a few kT's below the trap energy level, the exponential term in Eqn. (3.16) is much greater than one, and Boltzmann statistics, Eqn. (3.18) can be used. By substituting (3.15) and (3.18) in (3.20) θ can be calculated

$$\theta = \frac{1}{1 + \frac{N_t}{N_c}\exp\left[\left(E_c - E_t\right)/kT\right]}. \tag{3.21}$$

It can be seen that as long as the trap remains shallow, θ is independent of the position of the Fermi level or applied voltage, and is constant at a constant temperature. Further, if $\frac{N_t}{N_c}\exp\left[\left(E_c - E_t\right)/kT\right] >> 1$, Eqn. (3.21) can be simplified as

$$\theta \approx \frac{N_c}{N_t}\exp\left[-\left(E_c - E_t\right)/kT\right]. \tag{3.22}$$

This is true in many real cases when the trap level is not very close to the conduction band mobility edge and the trap density is comparable with the effective density of states at the conduction band mobility edge.

In the region between x_2 and x_3, the current is space-charge-limited mostly by the trapped electrons with n_f/θ instead of n_f in the Poisson's equation. However, for $x < x_2$, the Fermi level is above the trap energy level and the exponential term in Eqn. (3.16) is smaller than one. So, the Boltzmann approximation is not valid anymore and exact Fermi-Dirac statistics should be used. By decreasing x, n_t - $n_{t0} \approx n_t$ changes between n_t (x_2) = N_t /2 and n_t (0) = N_t, while $n_f - n_0$ increases exponentially. Not far from x_2, when the Fermi level is just 3 kT above the trap energy level, about 95% of trap states are occupied by electrons and the trap is virtually full. So n_t increases at a much lower rate than n_f and saturates at $N_t - n_{t0} \approx N_t$. Therefore θ is no longer constant and increases greatly by decreasing x.

There is a plane at $x = x_1$ in which $n_f - n_0 = N_t$. At this point the trap is virtually full and $n_t - n_{t0} \approx n_t \approx N_t$. The region between x_1 and x_2 in which the trap is virtually full is called the trap-filled region. For x sufficiently smaller than x_1, N_t is much smaller than $n_f - n_0$ and can be neglected, or $\theta \approx 1$. The current in this region is space-charge-limited by the free electrons and the effect of trapped electrons is negligible. This is similar to the space-charge-limited current in the trap-free material and so the region is called the trap-free region.

From Lampert and Mark [20], x_1, x_2, and x_3 can be calculated

$$x_1(J) = \frac{\varepsilon J}{2q^2 N_t^2 \mu_0}, \tag{3.23a}$$

$$x_2(J) = \frac{\varepsilon J n_{t0}}{q^2 n_0 N_t^{\,2} \mu_0} \approx \frac{\varepsilon J}{\theta q^2 N_t^{\,2} \mu_0}, \tag{3.23b}$$

$$x_3(J) = \frac{\theta \varepsilon J}{2q^2 n_0^{\,2} \mu_0} \approx \frac{\varepsilon J}{2q^2 n_0 n_{t0} \mu_0}. \tag{3.23c}$$

where the minimum constant θ at $x > x_2$ should be used. The relationship for x_3 in Eqn. (3.23c) is similar to that for x_1 in Eqn. (3.10) multiplied by θ. From (3.23) it can be found that $x_1 / x_2 = n_0 / 2n_{t0} \approx \theta / 2 << 1$ and $x_2 / x_3 = 2n_{t0}^2 / N_t^2 << 1$, or $x_1 << x_2 << x_3$ [20]. At low applied voltages, all the four regions described above exist in the material. However, since $x_2 << x_3 < d$ the contribution of trap-filled and trap-free regions ($x < x_2$) in the current is negligible and only two regions at $x > x_2$ are important.

At very low applied voltages, the current is very low and from (3.23c), $x_3 << d$. The space-charge is mostly in the region very close to the cathode and is negligible in most of the film. The current is carried out only by thermal-free electrons $n_0 - n_{t0}$ and can be expressed by the Ohm's law. By increasing the applied voltage x_3 is increased and at a critical voltage becomes equal to d. Beyond this point the contribution of the Ohmic regime in the current is negligible and the current is dominated by the space charge described by Eqn. (3.19). Since $x_1 << x_2 << x_3$, neglecting the narrow region at $x < x_2$, the shallow trap approximation can be used and θ can be considered constant. The current density can be calculated by solving the Poisson's equation similar to the trap-free case, using n_f / θ instead of n_f, resulting in

$$J = \frac{9}{8} \theta \varepsilon \mu_0 \frac{V^2}{d^3}, \tag{3.24}$$

which is the Child's law with the presence of trap(s).

Here it would be useful to define the effective drift mobility

$$\mu_d = \theta \mu_0 = \frac{n_f}{n_t + n_f} \mu_0. \tag{3.25}$$

So Child's law, Eqn. (2.7) can be modified as

$$J = \frac{9}{8} \varepsilon \mu_d \frac{V^2}{d^3}. \tag{3.26}$$

By increasing the applied voltage, x_2 approaches to d, and at a critical voltage x_2 becomes equal to d. Beyond this point, where the Fermi level is above the trap energy level, the Boltzmann approximation for n_t is no more valid and the exact Fermi-Dirac statistics should be applied. As stated above, with the Fermi level above the trap energy level, trap states are virtually full and n_t approaches the maximum value N_t, the density of traps (deep trap). The free electron concentration, however, changes significantly by a slight shift of Fermi level. This results in a higher increase in current, or a steeper slope in the J-V plot, which is called trap-filled limit (TFL) region. In deriving Eqn. (3.26) it was assumed that θ is constant at a constant temperature, while in this case θ is no longer constant and (3.26) is not valid. Finding a relationship between current and voltage in the TFL region is not possible [20]. However, it is known that the slope of the log-log J-V plot is a function of N_t / N_c and the energy level of the trap [20].

With further increase of the applied voltage, there is a situation that x_1 becomes equal to d, or the concentration of free electrons in all the film is more than N_t. So, the trapped electrons are negligible and only free electrons contribute to the space-charge, or θ approaches to one and drift mobility approaches to the conduction band mobility μ_0. The current is space-charge-limited similar to the trap-free material, and so this region is called the trap-free region. A logarithmic plot of current density versus applied voltage for a material with a single set of traps is shown in Fig. 3.5, indicating four different regions.

The intercept of the Ohmic and SCL regions or the onset of SCL regime can be found by equating the right hand sides of Eqns. (3.1) and (3.24)

$$V_1 = \frac{8}{9} \frac{q n_0 d^2}{\theta \varepsilon}. \tag{3.27}$$

Lambert and Mark, using the regional approximation [20], have derived relationships for current and voltage at some critical points that can be considered as the intercepts of the different regions. These are

$$J_{cr1} = \frac{2q^2 n_0^{\,2} \mu_0 d}{\theta\varepsilon}, \tag{3.28a}$$

$$V_{cr1} = \frac{4}{3}\frac{q n_0 d^2}{\theta\varepsilon}, \tag{3.28b}$$

for the intercept of the Ohmic and SCL regions, which is very close to V_1 in (3.27),

$$J_{cr2} = \frac{\theta q^2 N_t^{\,2} \mu_0 d}{\varepsilon}, \tag{3.29a}$$

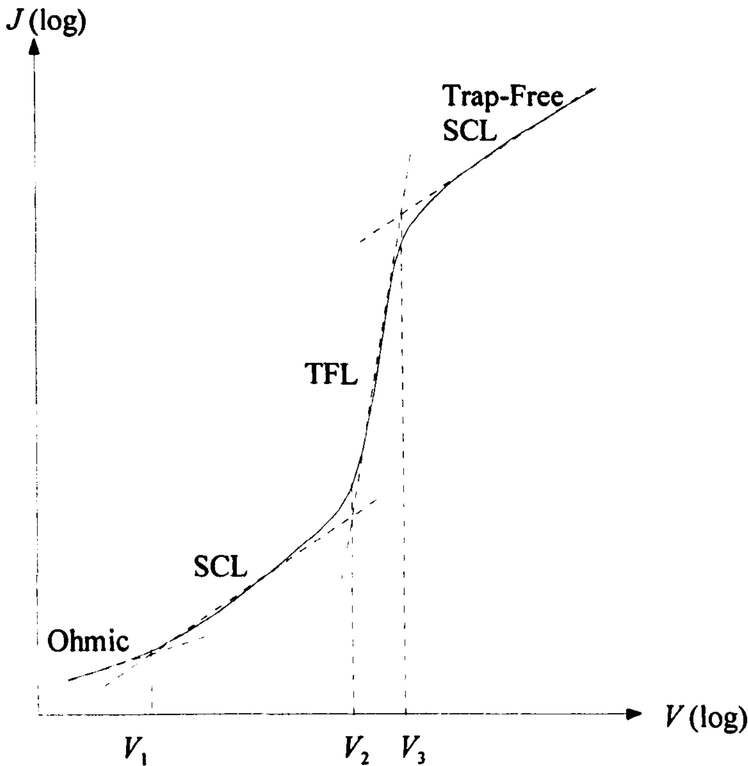


Figure 3.5 A schematic log-log plot of current density versus applied voltage for a material with a single set of shallow traps. The different regions and their intercept are indicated in the figure.

$$V_{\mathrm{cr2}} = \frac{qN_t d^2}{2\varepsilon}, \tag{3.29b}$$

for the intercept of the SCL and TFL regions, and

$$J_{\mathrm{cr3}} = \frac{2q^2 N_t^{\,2} \mu_0 d}{\varepsilon}, \tag{3.30a}$$

$$V_{\mathrm{cr3}} = \frac{4}{3}\frac{qN_t d^2}{\varepsilon}, \tag{3.30b}$$

for the intercept of the TFL and trap-free SCL regions. The current and voltage at the intercept of the Ohmic and SCL regions, equations (3.27) and (3.28) above, are similar to equations (3.11) and (3.12) derived for the trap-free case, with their right-hand side multiplied by $1/\theta$. Lampert and mark suggest that the presence of shallow trapping delays the critical voltage and current corresponding to departure form Ohm's law by the factor of $1/\theta$ [20]. However, some care should be taken since n_0 in the material with traps differs highly from that in the trap-free material.

3.3.4 The Material with Deep Traps

Another possible situation is a material with one or more sets of electron traps well below the Fermi level (deep traps) prior to the application of voltage. Since the traps are virtually filled initially with thermally generated electrons, the Ohmic region joins directly to the steep TFL region without a square law SCL region. After that, like the previous situation, there will be a trap-free SCL region. The current and voltage of the critical points for a single set of deep traps are

$$J_{\mathrm{cr1}} = \frac{q^2 n_0 N_t \exp\left[\left(E_t - E_{F0}\right)/kT\right]\mu_0 d}{\varepsilon} \approx \frac{q^2 n_0 \left(N_t - n_{t0}\right)\mu_0 d}{\varepsilon}, \tag{3.31a}$$

$$V_{\mathrm{cr1}} = \frac{qN_t \exp\left[\left(E_t - E_{F0}\right)/kT\right]d^2}{2\varepsilon} \approx \frac{q\left(N_t - n_{t0}\right)d^2}{2\varepsilon}, \tag{3.31b}$$

for the intercept of Ohmic and TFL regions, and

$$J_{\mathrm{cr2}} = \frac{2q^2 N_t^2 \exp\left[2\left(E_t - E_{F0}\right)/kT\right]\mu_0 d}{\varepsilon} \approx \frac{2q^2\left(N_t - n_{t0}\right)^2 \mu_0 d}{\varepsilon}, \tag{3.32a}$$

$$V_{cr2} = \frac{4qN_t \exp[(E_t - E_{F0})/kT]d^2}{3\varepsilon} \approx \frac{4q(N_t - n_{t0})d^2}{3\varepsilon}, \quad (3.32b)$$

for the intercept of TFL and trap-free SCL regions [20]. In the above equations, the term $N_t - n_{t0}$ is the empty trap states or the concentration of traps not occupied by the electrons. In the case of multiple deep traps, the sum of all empty trap states, or $\sum_i (N_{ti} - n_{ti0})$ should be used instead of $N_t - n_{t0}$.

3.3.5 The Material with Multiple Traps

In the case of multiple discrete trap levels, because the electrons occupy the vacant states in all trap levels, the problem is more complicated. If there are n traps with densities N_{t1}, N_{t2}, N_{t3}, ..., N_{tn}, at energy levels E_{t1}, E_{t2}, E_{t3}, ..., E_{tn}, and all traps are shallow, the concentration of trapped electrons at a distance x from cathode can be expressed by

$$\begin{aligned} n_t(x) &= n_{t1}(x) + n_{t2}(x) + \cdots \\ &= N_{t1} \exp[-(E_{t1} - E_F)/kT] + N_{t2} \exp[-(E_{t2} - E_F)/kT] + \cdots \\ &= \sum_n N_{ti} \exp[-(E_{ti} - E_F)/kT], \end{aligned} \quad (3.33)$$

where n_{tl}, n_{t2}, ... are the concentration of electrons trapped in the first, second, ... trap, respectively. By application of voltage, the injected electrons from cathode make a space charge whose density decreases by increasing x. Some of the injected electrons occupy the trap states, while others stay in the conduction band. Finding a universal relationship between current and voltage in general is not possible and the regional approximation in general is not applicable. The injected electrons occupy the states in all traps. Even when all traps are shallow, θ is not constant and Poisson's equation can not simply be solved. The problem is more complicated in the regions where the Fermi level is above some trap energy levels (deep traps) and below some others (shallow traps). The lower traps are virtually full with a constant concentration of trapped electrons, while the concentration of electrons in the higher traps is varied by changing the position of Fermi level. At very low applied voltages, the space

charge is negligible and there is an Ohmic conduction. On the other hand, at a certain voltage all the trap states are filled with electrons and there is a trap-free square-low SCL current. Between the linear Ohmic region and square-low trap-free regions, the log-log current-voltage plot has a varying slope that is a function of the density and the energy level of all traps, the relative density of traps, the separation of trap levels, and the film thickness d.

However, the regional approximation still can be used in an idealized case, by adding two other assumptions:

1. The trap levels are widely separated or the difference between energy levels of two successive traps is much more than kT. In this case when the Fermi level is close to a particular trap, the concentration of electrons in the higher traps is negligible. The best condition for this assumption is at very low temperatures where the zero temperature approximation can be used. From Fermi-Dirac statistics, Eqn. (3.14), at zero temperature a trap is completely full when the Fermi level is above the trap energy level, and is completely empty when the Fermi level is below the trap level.

2. The density of traps is greatly increased by increasing the trap energy level, i.e. the density of a trap is much (many orders) greater than that of the immediate trap below it. In this case, when the Fermi level is close to a particular trap, the electrons occupied in the lower traps can be neglected.

With these assumptions, the traps can be treated individually, i.e. when a trap is active, the effect of other traps is negligible and the problem is similar to the single-trap case. The regional approximation can effectively be used in the case of multiple traps. At a rather low applied voltage, in a region close to the anode, where $n_f(x) - n_0 > n_0$, the excess free and trapped electrons are negligible in comparison with n_0 and n_{t0} and the conduction is mainly due to the thermal-free electrons n_0. In the other regions, n_0 and n_{t0} do not have a significant effect and the excess free and trapped electrons forming space charge control the current.

In a region adjacent to the Ohmic region where the Fermi level is below the first trap level, or $E_F(x) < E_{t1}$, all the traps are shallow and the current becomes space-charge-limited. The space charge in this region equals

$n_f + n_t = n_f + n_{t1} + n_{t2} + \cdots = n_f + \sum_n n_{ti} = n_f / \theta$ that according to the first assumption is nearly equal to $n_f + n_{t1} = n_f/\theta_1$, in which $\theta_1 = n_f/(n_f + n_{t1})$ is nearly constant in a constant temperature. Next there is a TFL region where the Fermi level is above the first trap energy level and $n_{t2} < N_{t1}$ (after that the n_{t2} is dominant and the SCL region of the second trap begins). In this region, the trap is virtually full and the effect of next traps is negligible. The space charge in this region equals $n_f + n_{t1} + n_{t2} + \ldots \approx n_f + N_{t1} + n_{t2} + \ldots \approx n_f + N_{t1}$.

There are two regions associated with each trap; the SCL region when the trap is shallow, and the TFL region when the trap is filled with electrons. For any trap i, the boundary between the SCL and TFL regions associated with that trap is where the Fermi level passes through the particular trap energy level, or $E_F(x) = E_{ti}$. At this point $n_{ti}(x) = N_{ti}/2$. The boundary between the SCL region of trap i and the TFL region of trap $i - 1$ is where the concentration of electrons in trap i is comparable with the concentration of electrons in all deep traps, or $n_{ti}(x) = \sum_{i-1} N_{tj} \approx N_{t(i-1)}$. At this point, $n_f(x) \approx \theta_i n_{ti}(x) \approx \theta_i N_{t(i-1)}$. Similarly, the boundary between the TFL region of trap i and the SCL of trap $i + 1$ is where the concentration of electrons in trap $i + 1$ is comparable with that of electrons in all traps below the trap $i + 1$. The space charge in the SCL region approximately equals to $n_f + n_{ti} = n_f / \theta_i$, where $\theta_i = n_f/(n_f + n_{ti})$ is nearly constant at a constant temperature. In the TFL region, however, the space charge is approximately equal to $n_f + N_{ti}$ and so, there is no constant θ.

In the region $x < x_1$ close to the cathode, where $n_f(x_1) = \sum_n N_{ti}$, all the traps are full and the concentration of free electrons is more than that of total trapped electrons and the region is virtually trap free. This is like the trap-free SCL region in the single-trap case and x_1 can be found from Eqn. (3.23a) by substituting N_t with sum of the densities of all traps, or

$$x_1(J) = \frac{\varepsilon J}{2q^2 \sum_n N_{tj}^2 \mu_0} = \frac{\varepsilon J}{2q^2 N_t^2 \mu_0} \approx \frac{\varepsilon J}{2q^2 N_{tn}^2 \mu_0}, \tag{3.34}$$

in which $N_t = \sum_n N_{tj}$. The region $x_1 < x < x_2$, where $E_F(x_2) = E_{tn}$, is the TFL region associated with the nth trap. The distance x_2 can be calculated as

$$x_2(J) \approx \frac{\varepsilon J}{\theta_n q^2 N_{tn} N_t \mu_0} \approx \frac{\varepsilon J}{\theta_n q^2 N_{tn}^2 \mu_0}, \tag{3.35}$$

with N_t defined as above, and $\theta_n = n_f / (n_f + n_{tn})$ is the constant θ in the SCL region of the nth trap. The SCL region associated to the nth trap is between $x_2 < x < x_3$, where $n_{tn}(x_3) = \sum_{n-1} N_{tj} \approx N_{t(n-1)}$ and

$$x_3(J) \approx \frac{\varepsilon J}{2\theta_n q^2 \left(\sum_{n-1} N_{tj}\right)^2 \mu_0} \approx \frac{\varepsilon J}{2\theta_n q^2 N_{t(n-1)}^2 \mu_0}. \tag{3.36}$$

In the same way, the width of TFL and SCL regions associated with each trap can be calculated. For the ith trap these regions are

$$w_{\mathrm{TFL}i}(J) \approx \frac{\varepsilon J}{\theta_i q^2 N_{ti} \sum_i N_{tj} \mu_0} \approx \frac{\varepsilon J}{\theta_i q^2 N_{ti}^2 \mu_0}, \tag{3.37}$$

and

$$w_{\mathrm{SCL}i}(J) \approx \frac{\varepsilon J}{2\theta_i q^2 \left(\sum_{i-1} N_{tj}\right)^2 \mu_0} \approx \frac{\varepsilon J}{2\theta_i q^2 N_{t(i-1)}^2 \mu_0}. \tag{3.38}$$

where $\theta_i = n_f / (n_f + n_{ti})$ is the constant θ in the SCL region of the ith trap. The width of SCL region for the lowest trap is

$$w_{\mathrm{SCL}1}(J) \approx \frac{\theta_1 \varepsilon J}{2q^2 n_0^2 \mu_0}. \tag{3.39}$$

The important conclusion from the above equations is that $w_{\mathrm{SCL}i} >> w_{\mathrm{TFL}i}$ and the widths of the SCL and TFL regions associated with each trap are much bigger than those associated with the higher traps. When the right boundary of the SCL region for the lowest trap reaches the anode, the width of the other regions are so small compared with this region that their effect can be neglected. The current is

space-charge-limited and depends only on the parameters of the lowest trap. By increasing the applied voltage, when the right boundary of the TFL region for the lowest trap reaches to the anode, this region is dominant, and so on for the other traps. Therefore, each trap produces a square-law SCL region and a steep TFL region in the *J-V* characteristics similar to Fig. 3.1.

Lampert and Mark [20] have calculated the voltage and current of some critical points which are the intercepts of the different regions in the case of single trap. By the same method and using Eqns. 3.24 and 3.34 - 3.39, the current and voltage of these turning points can be calculated for the multiple-trap situation. In the following equations, J_{SCL1} and V_{SCL1} are the current and voltage of the intercept of the Ohmic region and the SCL region, or the onset of the SCL region associated to the lowest trap level, $J_{\mathrm{SCL}i}$ and $V_{\mathrm{SCL}i}$ are for the onset of the SCL region associated to the ith trap level, $J_{\mathrm{TFL}i}$ and $V_{\mathrm{TFL}i}$ for the onset of the TFL region associated to the ith trap level, and J_{TF} and V_{TF} are the current and voltage of the onset of trap-free square-law region.

$$J_{\mathrm{SCL1}} = \frac{2q^2 n_0{}^2 \mu_0 d}{\theta_1 \varepsilon}, \tag{3.40a}$$

$$V_{\mathrm{SCL1}} = \frac{4qn_0 d^2}{3\theta_1 \varepsilon}. \tag{3.40b}$$

$$J_{\mathrm{SCL}i} = \frac{2\theta_i q^2 \mu_0 \left(\sum_{i-1} N_{tj}\right)^2 d}{\varepsilon} \approx \frac{2\theta_i q^2 \mu_0 N_{t(i-1)}^2 d}{\varepsilon}, \tag{3.41a}$$

$$V_{\mathrm{SCL}i} = \frac{4q\sum_{i-1} N_{tj} d^2}{3\varepsilon} \approx \frac{4qN_{t(i-1)} d^2}{3\varepsilon}. \tag{3.41b}$$

$$J_{\mathrm{TFL}i} = \frac{\theta_i q^2 \mu_0 N_{ti} \sum_i N_{tj} d}{\varepsilon} \approx \frac{\theta_i q^2 \mu_0 N_{ti}^2 d}{\varepsilon}, \tag{3.42a}$$

$$V_{\mathrm{TFL}i} = \frac{q\left(N_{ti}\sum_i N_{tj}\right)^{1/2} d^2}{2\varepsilon} \approx \frac{qN_{ti} d^2}{2\varepsilon}. \tag{3.42b}$$

$$J_{\rm TF} = \frac{2q^2\mu_0 N_t^2 d}{\varepsilon} \approx \frac{2q^2\mu_0 N_{tn}^2 d}{\varepsilon}, \tag{3.43a}$$

$$V_{\rm TF} = \frac{4qN_t d^2}{3\varepsilon} \approx \frac{4qN_{tn} d^2}{3\varepsilon}. \tag{3.43b}$$

The above assumptions are not generally satisfied in the real cases. For instance, the energy level of two or more traps may be so close that the number of electrons captured by each trap is comparable. Hence, the *J-V* characteristics do not obey the square law in the SCLC region and the slope of its plot is more than two. There may be a case that no TFL region can be observed between two SCLC regions on the *J-V* plot, and two traps have the effect of a single trap. Even when the trap levels are widely separated, the density of higher traps may be so high that the concentration of electrons captured by these traps becomes comparable or even more than that in the first trap. If the density of a lower trap is not much smaller than that of higher trap, it can not be neglected in calculation of SCLC for the second trap, resulting in a slope of higher than two in the *J-V* plot. At the other extreme, if a higher trap has smaller density than the lower one, when the first trap is filled (TFL region) and the Fermi level approaches the next trap, there may be a slight decrease in the slope of the *J-V* plot and an increase in the slope afterwards, corresponding to the TFL region after the second trap is filled. In some cases, the change of slope may not be observable in the *J-V* plot. Therefore, the information about the second trap can not be investigated from the SCLC plot.

3.3.6 The Material with a Continuous Distribution of Traps

When there is a continuous distribution of traps, the problem is more complicated. Because the trap levels are very close together, traps with different energy levels are being filled simultaneously and there is a continuous distribution of filled trap states below the Fermi level. Therefore, the *J-V* curve at each particular point has a slope that can not be treated as simple space-charge limited or trap-filled limit situations. In most experimental SCLC results reported for a-Si:H, no slope of two corresponding to the space-charge limited region can be observed, except the

SCLC region after the Ohmic region. In many of them, there is not even an apparent decrease in the slope.

The variation of the current density with the applied voltage depends on the trap distribution function and deriving a relationship between current and voltage is not possible for any distribution function. Some authors have derived such expressions for special distributions of traps. Lampert and mark have derived expressions for the exponential and uniform distributions of traps [20]. For an exponential distribution of traps in the form of

$$N_t(E) = N_0 \exp\left[-\left(E_c - E\right)/kT_c\right], \tag{3.44}$$

they have derived

$$J = q\mu N_c \left[\frac{\varepsilon l}{qN_0 kT_c(l+1)}\right]^l \left(\frac{2l+1}{l+1}\right)^{l+1} \frac{V^{l+1}}{d^{2l+1}} \approx q\mu_0 N_c \left(\frac{\varepsilon}{qN_0 kT_c}\right)^l \frac{V^{l+1}}{d^{2l+1}},$$

with $\quad l = T_c/T, \qquad (3.45)$

where N_0 in cm^{-3} eV^{-1} is the density of states at the conduction band mobility edge, and T_c is a temperature parameter characterizing the trap distribution. The physical significance of parameter T_c is not exactly clear. Possibly, it corresponds to that temperature in the final cooling-down stage of the sample preparation at which annealing effectively ceases [20]. The crossover voltages with the Ohm's law, V_{cr1}, and with the trap-free square law, V_{cr2}, are given by (2.46) and (2.47), respectively [20]

$$V_{cr1} = \frac{qn_0 d^2}{\varepsilon}\left(\frac{l+1}{2l+1}\right)^{(l+1)/l} \frac{\Gamma(l+1)}{l}, \tag{3.46}$$

$$V_{cr2} = \frac{qn_0 d^2}{\varepsilon}\Gamma^l \left[\frac{9}{8}\left(\frac{l+1}{l}\right)^l \left(\frac{l+1}{2l+1}\right)^{l+1}\right]^{l/(l-1)}, \tag{3.47}$$

in which

$$\Gamma = \left(N_0 kT_c/n_0\right)\left(n_0/N_c\right)^{1/l}. \tag{3.48}$$

For a uniform distribution of traps in the form of

$$N_t(E) = N_0 = \text{constant}, \tag{3.49}$$

Lampert and Mark [20] have given

$$J = 2q\mu_0 n_0 (V/d)\exp(2\alpha V/Td^2), \quad \text{with} \quad \alpha = \varepsilon/qN_0 k. \tag{3.50}$$

Orton and Powell [22] have presented the same expression for the uniform distribution of traps. For the exponential distribution of traps they have given

$$J = qN_c\mu_0 \frac{V}{d}\left(1 + \frac{\alpha' V}{l}\right)^l, \quad \text{with} \quad \alpha' = \varepsilon/qd^2 N_0 kT, \text{ and } l = T_c/T, \tag{3.51}$$

and ignoring 1 in the parentheses, it is the same as (3.45).

3.3.7 The Scaling Law

Lampert and Mark [20] have shown that as long as the diffusion current is negligible, the *J-V* characteristics of the material, in any region and for any distribution of traps, follows the scaling law in the form of

$$J/d = f(V/d^2), \tag{3.53}$$

for fixed values of material constants. For instance, the *J-V* characteristics in the Ohmic region, trap-free square law region, and the SCLC region for single trap, exponential distribution and uniform distribution, Eqn. (3.1), (3.7), (3.24), (3.45), and (3.50), all are in agreement with the scaling law.

At low fields, the drift velocity is proportional to the applied field

$$v_d = \mu_0 \mathcal{E}, \tag{3.54}$$

and μ_0 is constant and independent of the applied field. However, above a critical field intensity $\mathcal{E}_1$, the acoustic phonon scattering is dominant and the drift velocity v_d varies with the square-root of the applied field [20]

$$v_d = \mu_0 (\mathcal{E}_1/\mathcal{E})^{1/2} \quad \text{for} \quad \mathcal{E} > \mathcal{E}_1. \tag{3.55}$$

At even higher fields, when the applied field is much greater than the critical field $\mathcal{E}_1$, the electrons are heated up by the field to optical phonon energy and the drift velocity is saturated at the value v_s

$$v_d = v_s \qquad \text{for} \qquad \mathcal{E} >> \mathcal{E}_1. \tag{3.56}$$

In general, the relationship between drift velocity and the applied field can be written as

$$v_d = \mu_0 \mathcal{E}_{cr}^{1-\alpha} \mathcal{E}^{\alpha}. \tag{3.57}$$

With $\alpha = 1$, 1/2, and 0, (3.57) is consistent with the equations (3.54-3.56) for low field, high field, and very high field (velocity saturation) respectively.

It would useful to define a field dependent mobility

$$\tilde{\mu} = \frac{v_d}{\mathcal{E}} = \mu_0 \mathcal{E}_1^{1-\alpha} \mathcal{E}^{\alpha-1}, \tag{3.58}$$

which is equal to μ_0 at low fields, $\mu_0 \mathcal{E}_1^{1/2} \mathcal{E}^{-1/2}$ at high fields, and $\mu_0 \mathcal{E}_1 \mathcal{E}^{-1} = v_s / \mathcal{E}$ at very high fields.

If the current-voltage characteristics at low fields is indicated by

$$J = f(V) \qquad \text{for} \qquad \mathcal{E} < \mathcal{E}_1, \tag{3.59}$$

and if the thermal relationship between free and trapped electrons is not strongly varied by the heating of the electrons, then the current-voltage characteristics at high fields for any trap model can be found [20] from the low-filled *J-V* characteristics simply by multiplying the latter by $(\mathcal{E}_1 d/V)^{1/2}$ for acoustic phonon scattering, and by $(v_s d/\mu_0 V)$ for velocity saturation

$$J = (\mathcal{E}_1 d/V)^{1/2} f(V) \qquad \text{for} \qquad \mathcal{E} > \mathcal{E}_1, \tag{3.60}$$

$$J = (v_s d/\mu_0 V) f(V) \qquad \text{for} \qquad \mathcal{E} >> \mathcal{E}_1, \tag{3.61}$$

In the other words, by substituting μ_0 with the field dependent mobility $\tilde{\mu}$ in the current-voltage relationship, and using $\mathcal{E} = V / d$ in (3.58), a universal *J-V* relationship

can be found which is valid for any applied field. The scaling law in this case can be written as

$$J/d^{\alpha} = f\left(V/d^{2}\right). \tag{3.62}$$

3.4 SIMULATION

Device simulation is a useful tool to study the characteristics and behaviour of a device or the material used in it. Although it is not possible to predict and include all the parameters of a real device in the model used in the simulation, however, the simulation can provide useful information if a proper model is defined. The simulation would be more effective especially when it is used in conjunction with the experimental results.

3.4.1 The Structure

The structure of the device used in the simulation is shown in Fig. 3.6a, which is similar to the experimental structure described in chapter three. The structure simply consists of an intrinsic a-Si:H film deposited on top of the *n*-type crystalline silicon, with metal contacts provided on top and on the bottom. The width of the device is 200 μm and the thickness of 200 nm has chosen for the *n*-type crystalline silicon layer to reduce the number of nodes. The thickness of a-Si:H layer is variable. The device simulation is two dimensional and current is calculated per unit depth. A nonlinear rectangular mesh has been defined with denser grids close to the junctions. Except stated otherwise, the parameters given in Table 3.1 have been used for all the simulations throughout this chapter. The concentration of donor atoms in the *n*-type crystalline silicon equals to 1×10^{18} cm^{-3}. For the parameters not specified in this table, the default values in Medici have been used.

3.4.2 Simulation Results

The device has been simulated and the effect of various parameters such as film thickness, position and density of traps, temperature, work function of metal

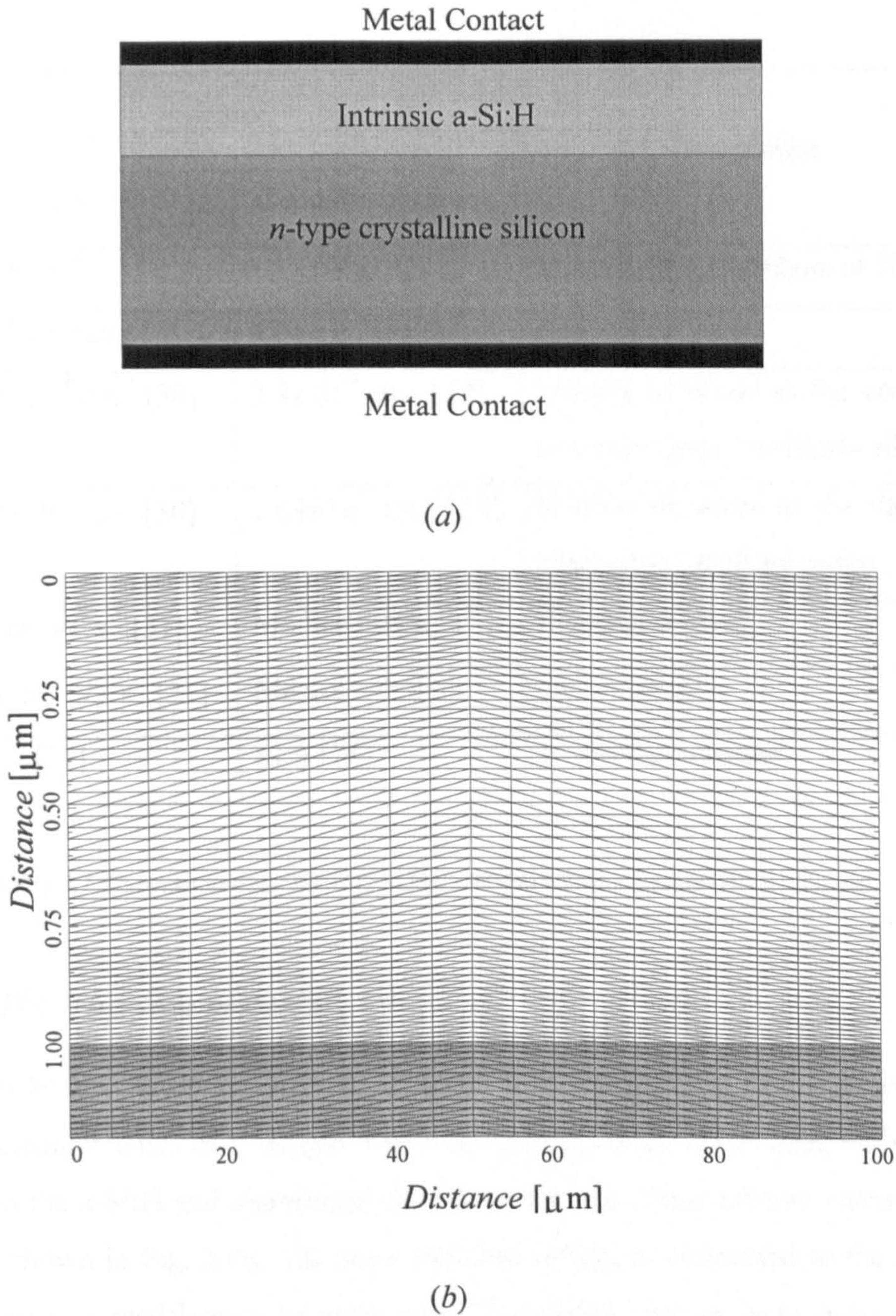


Figure. 3.6 The structure of the device (a) and the mesh (b) used in the SCLC simulation.

contact, and the doping level of *n*-type crystalline silicon on the *J-V* characteristics of the device are studied.

Parameter	Value		Description
	a-Si:H	Crystalline Silicon	
E_g	1.75 eV [27]	1.15 eV [28]	Mobility gap /Bandgap at 300 K
χ	3.93 eV [29]	4.01 eV [29]	Electron affinity
N_C	7.9×10^{18} cm^{-3} [30]	2.8×10^{19} cm^{-3} [28]	Density of states at the conduction band edge / mobility edge.
N_V	8.2×10^{18} cm^{-3} [30]	1.04×10^{19} cm^{-3} [28]	Density of states at the valence band edge / mobility edge.
μ_n	1 cm^2 V^{-1} s^{-1} [31]	Medici's default	Electron mobility
μ_p	0.1 cm^2 V^{-1} s^{-1} [31]	Medici's default	Hole mobility
ε_r	11.7 [31]	11.9 [28]	Dielectric constant

Table 3.1 The parameters of a-Si:H and crystalline silicon used in the simulation.

3.4.2.1 The trap-free material

To better understand the role of traps, first the trap-free case is considered. The *J-V* characteristics of a sample with a 0.3 μm trap-free a-Si:H film, with a gold contact on the a-Si:H and aluminium contact on the crystalline silicon, calculated at 300 K is shown in Fig. 3.7a. The more positive voltage is connected to the a- Si:H side. There is a rectification of more than 17 decades, due to large barrier at the a-Si:H and gold contact. The same characteristics with aluminium contact with both contacts aluminium is shown in Fig. 3.7b. The rectification is less than one decade, because of the very low barrier between aluminium and a-Si:H, neglecting the surface states. The device acts as a Schottky barrier diode, which is in forward bias when the more positive voltage is connected to the a-Si:H contact. The *n*-type crystalline silicon provides electrons to inject in the a-Si:H layer, when it is in a forward biased, and the Schottky barrier blocks the electrons in the reverse direction.

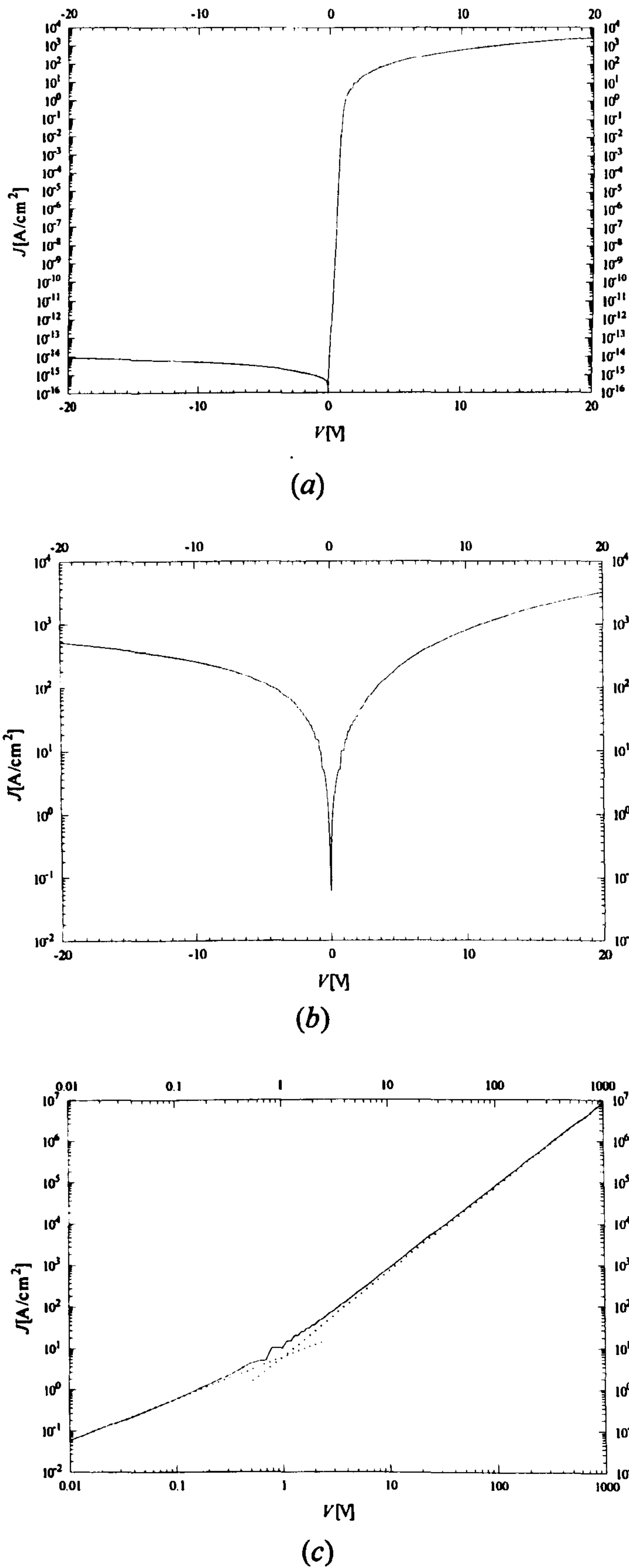


Figure. 3.7 The J-V characteristics of a 0.3 μm a-Si:H film without traps with (a) gold and (b) aluminium contact, and (c) the log-log plot of J-V characteristics of the device with aluminium contact at positive applied voltages.

The log-log plot of current density versus voltage for the device of Fig. 3.7b, at positive applied voltages is shown in Fig. 3.7c. The curve shows a trap-free SCLC behaviour, with a slope one, Ohmic region, followed by an SCL square law region. The intercept of the Ohmic and SCL regions is approximately 1 V, from which using Equation (3.11), $n_0 = 8.09\times10^{15}$ cm^{-3} can be found. Using (3.12b) the mobility of free electrons is equal to μ_0 = 0.10 cm^2 V^{-1}s^{-1}. The mobility of free electrons can also be found using (3.1) in the Ohmic region, and (3.7) in the SCL region, to be equal to 0.14 cm^2 V^{-1}s^{-1} and 0.19 cm^2 V^{-1}s^{-1}, respectively. These values, although very close, are less than 1 cm^2 V^{-1}s^{-1}, the value of mobility that has been set up in the program. The reason for this difference and also for very high electron concentration will be explained shortly in this section.

The energy band diagram of a trap-free sample with infinite thickness of a-Si:H layer is shown in Fig. 3.8. In the Fermi equilibrium, the free electrons from the n-type layer have diffused to the amorphous silicon. So, there is an accumulation layer in the a-Si:H layer near the heterojunction with the n-type silicon. The width of the accumulation layer is proportional to the Debye length defined as [32]

$$L_D = \left(\varepsilon kT/2q^2 n_i\right)^{\frac{1}{2}} \tag{3.63}$$

in which n_i is the intrinsic carrier concentration. For intrinsic a-Si:H without traps, L_D = 2.07 cm. Therefore, for a practical film thickness the accumulation layer extends through whole the film and the Fermi level for electrons moves towards the conduction band. Only for films with thickness of more than few centimeters can the Fermi level lie at the intrinsic Fermi level. The same thing happens in the region close to the a-Si:H and metal contact, however the band bending could be upward or downward depending on the work function of the metal (Fig. 3.8).

The energy band diagrams of the sample with thickness of a-Si:H layer equal to 0.3 μm, 10 μm, 1 mm, and 80 mm are shown in Fig. 3.9. Although some of these values are impractical, they can provide a better feeling about the effect of the Debye length in an intrinsic material. By increasing the thickness of the a-Si:H layer, the electrons Fermi level approaches the intrinsic Fermi level. However, even with a

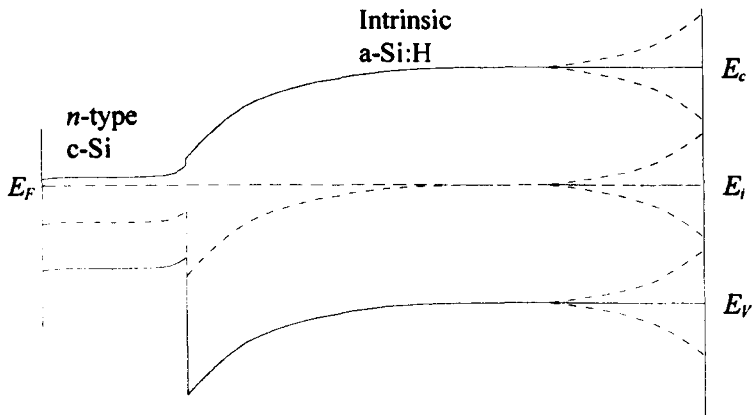


Figure 3.8 The energy band diagram of a sample with infinite thickness of a-Si:H layer.

thickness of 80 mm the Fermi level is still above midgap and the material can not be considered as intrinsic. Hence, the concentration of free electrons is much higher than the intrinsic carrier concentration and the material is virtually *n*-type.

The low free electron mobility calculated from the simulation results can be related to this huge concentration of excess injected electrons. In the theory of SCLC,

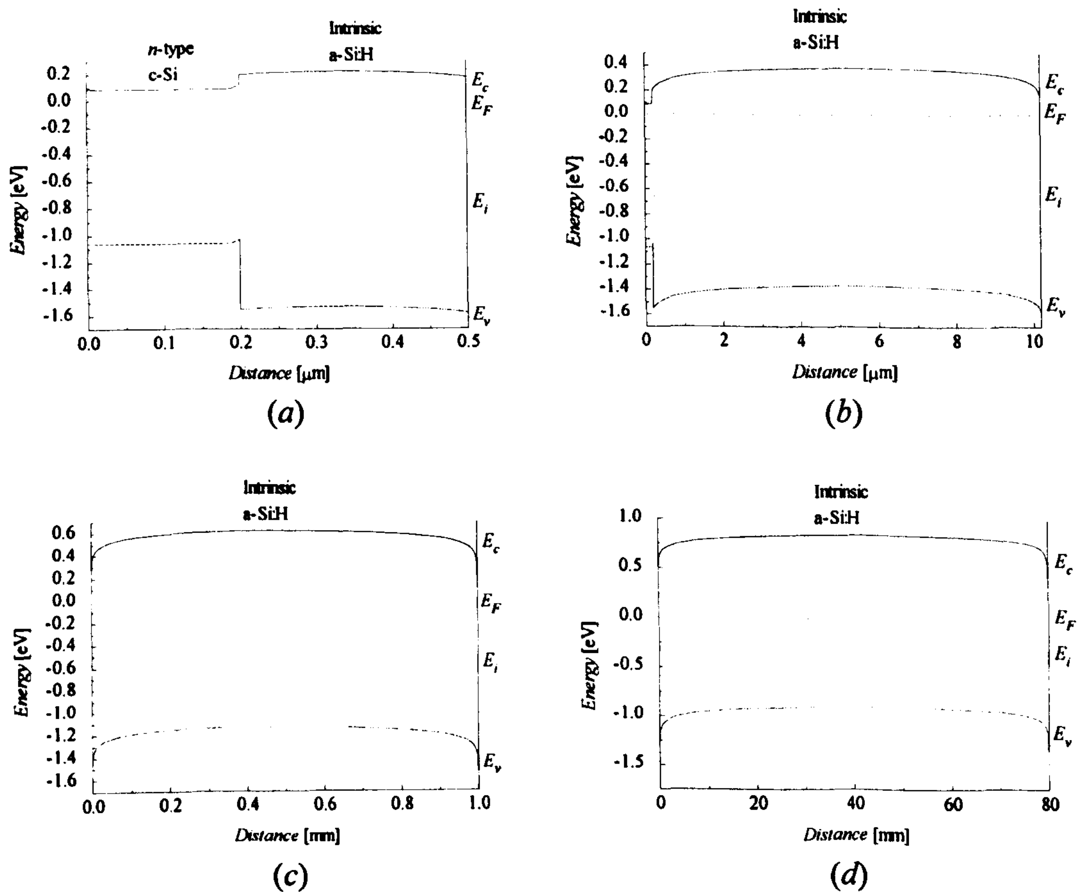


Figure 3.9 The energy band diagram of the sample with thickness of a-Si:H layer equal to (a) 0.3 μm, *(b)* 1 μm, *(c)* 1 mm, *and (d)* 80 mm.

it is assumed that the diffusion current is negligible, while in this case the large variation of electron concentration over a small distance produces a very large *dn/dx* so that the diffusion current may be effective. By increasing the film thickness, the electron concentration, and consequently *dn/dx* are reduced, which results in the reduction of the effect of diffusion current. For films with thickness of 0.1, 0.3, 1, 10, and 100 μm, the free electrons mobility was calculated in the SCL region of *J-V* results as 0.09, 0.15, 0.32, 0.43, and 0.52 $cm^2V^{-1}s^{-1}$. By increasing the film thickness, the mobility approaches the set-up value of 1 $cm^2V^{-1}s^{-1}$, which is in agreement with the above explanation.

Variation with Film Thickness

The log-log plots of *J-V* characteristics of the device for a-Si:H films with thickness of 0.1, 0.3, 1, 5, 50, and 500 μm are shown in Fig. 3.10. All the curves have a slope one Ohmic region followed by a square law SCL region. The intercept of Ohmic and SCL regions, V_X, equals to 0.5 V for the film with d = 0.1 μm, 1 V for d = 0.3 μm, and then saturates to about 1.3 V for the other films. From (3.11) and (3.63), it can be seen that for the films thicker than about 1 μm, the value of $n_0\ d^2$ is

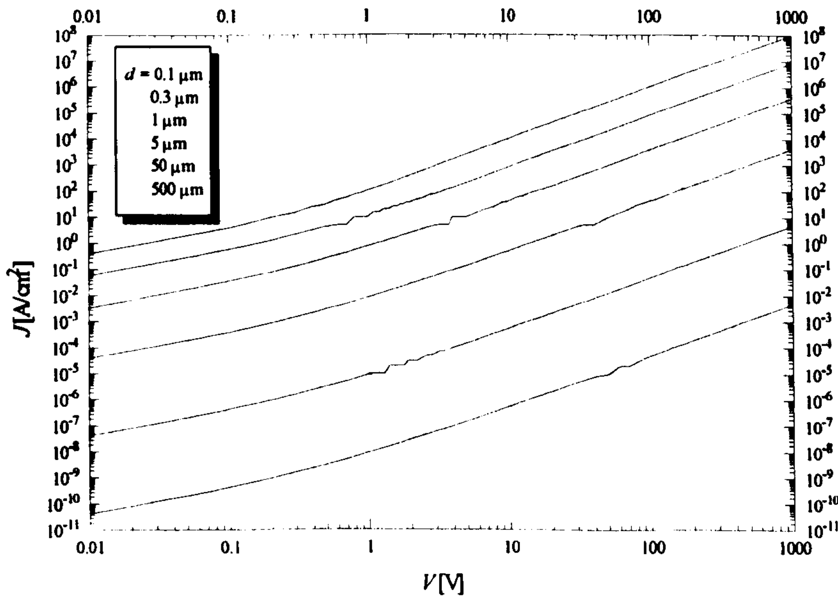


Figure 3.10 The J-V characteristics of the device for a-Si:H film thickness of 0.1 μm, 0.3 μm, 1 μm, 5 μm, 50 μm, *and* 500 μm.

nearly constant and is proportional to $n_i L_D^2$.

The variation of J/d versus V/d^2 is shown in Fig. 3.11. The SCL regions lie on the same line and agree with the scaling law, especially for thick films. However, as expected, the Ohmic regions do not follow the scaling law due to variation of free electron concentration with film thickness.

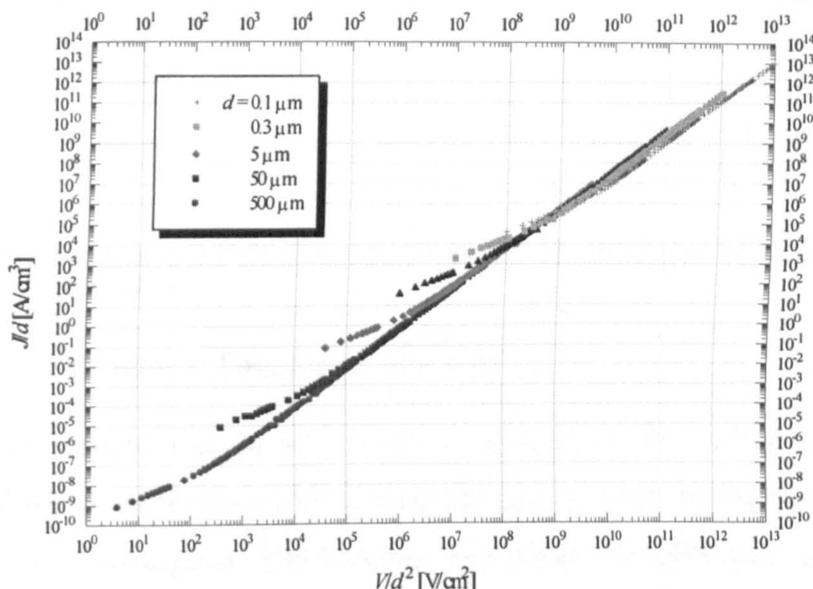


Figure 3.11 The variation of J/d versus V/d^2 for a-Si:H films with thickness of 0.1 μm, 0.3 μm, 1 μm, 5 μm, 50 μm, *and* 500 μm.

Effect of Doping Level of Crystalline Silicon

In the theory of SCLC, the electrodes are assumed as infinite reservoirs of carriers, and n^+ layers are usually used to provide a high level of carrier injection. The effect of doping level, or concentration of donor atoms in the *n*-type crystalline silicon is shown in Fig. 3.12. The thickness of a-Si:H is 0.3μm and both contacts are aluminium. The concentration of donor atoms in the crystalline silicon, N_D, is changed between 1×10^{14} to 1×10^{22} cm^{-3}. The doping level does not have a significant effect on the SCL region, and the change of current in the Ohmic region is around one order of magnitude. However, at very low concentrations (1×10^{14} and 1×10^{16} cm^{-3}) the characteristics are slightly away from the standard SCLC characteristics between applied voltages of 0.2 V and about 10 V.

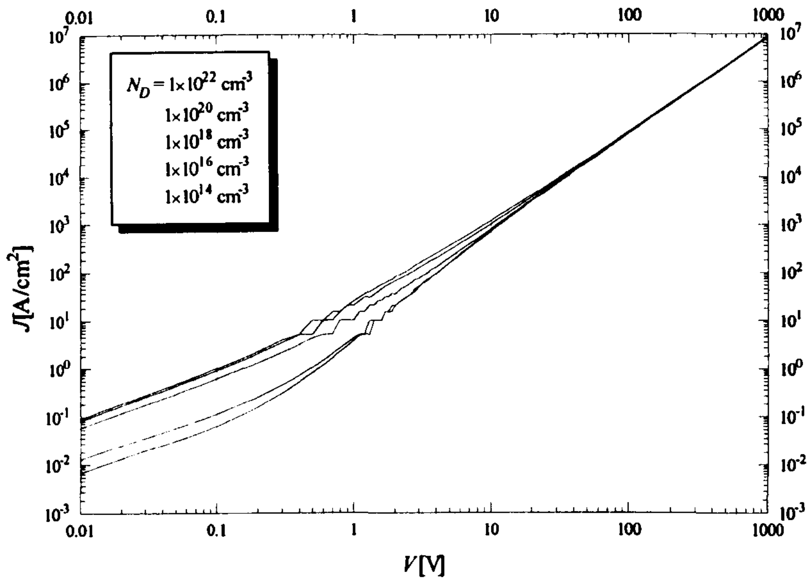


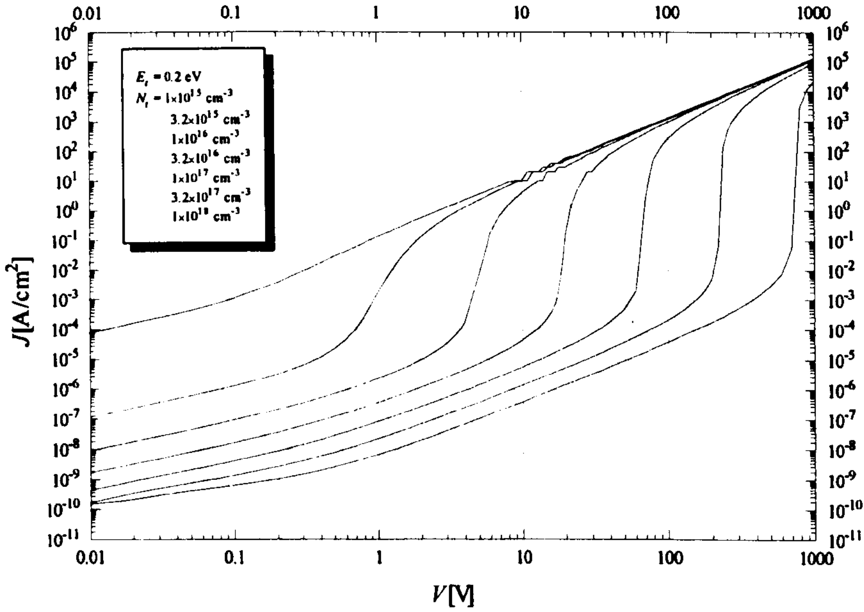
Figure 3.12 Variation of J-V characteristic with the concentration of donor atoms in crystalline silicon.

3.4.2.2 Material with a Single Set of Traps

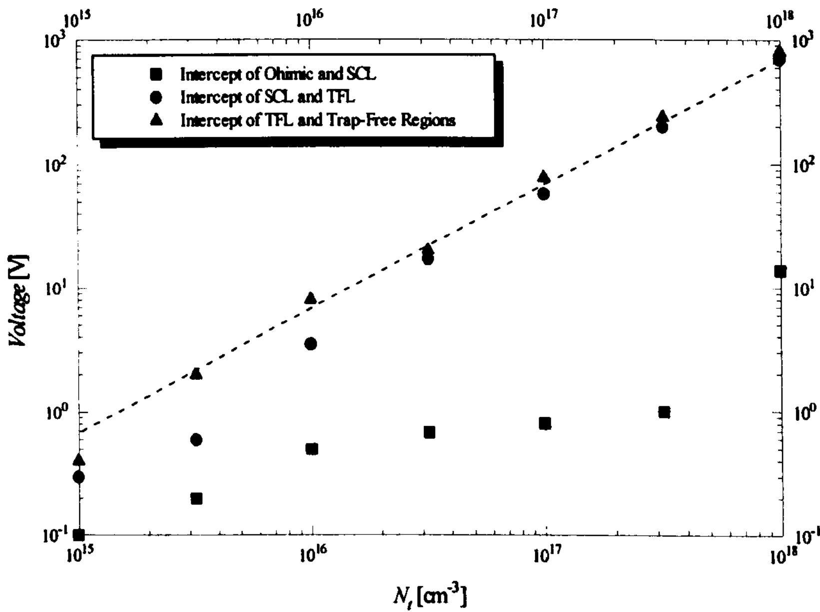
In this section, a single set of traps is included in the a-Si:H layer and the variation of *J-V* characteristics with density and energy level of traps and also with temperature was investigated. The thickness and width of a-Si:H film are 1 μm and 100 μm, respectively. The mobility was set equal to 0.1 $cm^2V^{-1}s^{-1}$ for free electrons and 0.01 $cm^2V^{-1}s^{-1}$ for holes. For each set of donor-like or electron traps above the intrinsic Fermi level, one set of acceptor-like or hole traps was set below the intrinsic Fermi level, with the same density and energy difference. The intrinsic Fermi level is used as zero energy. The simulation was performed at 300 K.

Variation with Density of Traps

A set of traps was set at the energy level of 0.2 eV, and its density was varied between 1×10^{15} to 1×10^{18} cm^{-3}. The calculated *J-V* characteristics are shown in Fig. 3.13a. Four different regions of the single trap SCLS, or the Ohmic, SCL, TFL, and trap-free regions can be observed on all curves, especially on those with a higher density of traps. The free electron mobility was checked in the free-trap region and the SCL regions of different graphs, which was very close to the set value of mobility in the program.



(a)



(b)

Figure 3.13 (a) The variation of J-V characteristics of a-Si:H with density of a single set of traps positioned at the energy level of 0.2 eV, *and (b) the variation of voltage of the intercept points with trap density.*

The intercept voltage of different regions, calculated from Eqns. (3.28b), (3.29b), and (3.30b) are shown in Fig. 3.13b. The onset voltages of both TFL and trap-free regions are proportional to the trap density. It can be shown that the slope of TFL region is proportional to log θ, and therefore increases with increasing the trap

density. From Fig. 3.13b, it can be seen that the onset of the trap-free region at all points is proportional to the trap density, while the onset of the TFL region is far away from theory at low trap densities.

The energy band diagram of the a-Si:H layer is shown if Fig. 3.14 for four different trap densities. The injected electrons accumulate in the area near the contacts and build up a space charge layer. These electrons are mostly captured by traps. Due to the space charge layer, there is a band bending η, in electron volts, in a distance W from contacts, after which the energy bands reach their bulk, neutral position (Fig. 3.14d). Lampert and Mark [20] have derived W as

$$W = \left(\frac{2\varepsilon\eta}{qN_t} \right)^{1/2} \tag{3.64}$$

With $\eta = E_g / 2 = 0.875$ eV, $W = 0.034$ μm for the highest trap density of $N_t = 1\times10^{18}$ cm^{-3}. However, for $N_t = 4.6\times10^{15}$ cm^{-3} the value of W is equal to 0.5 μm,

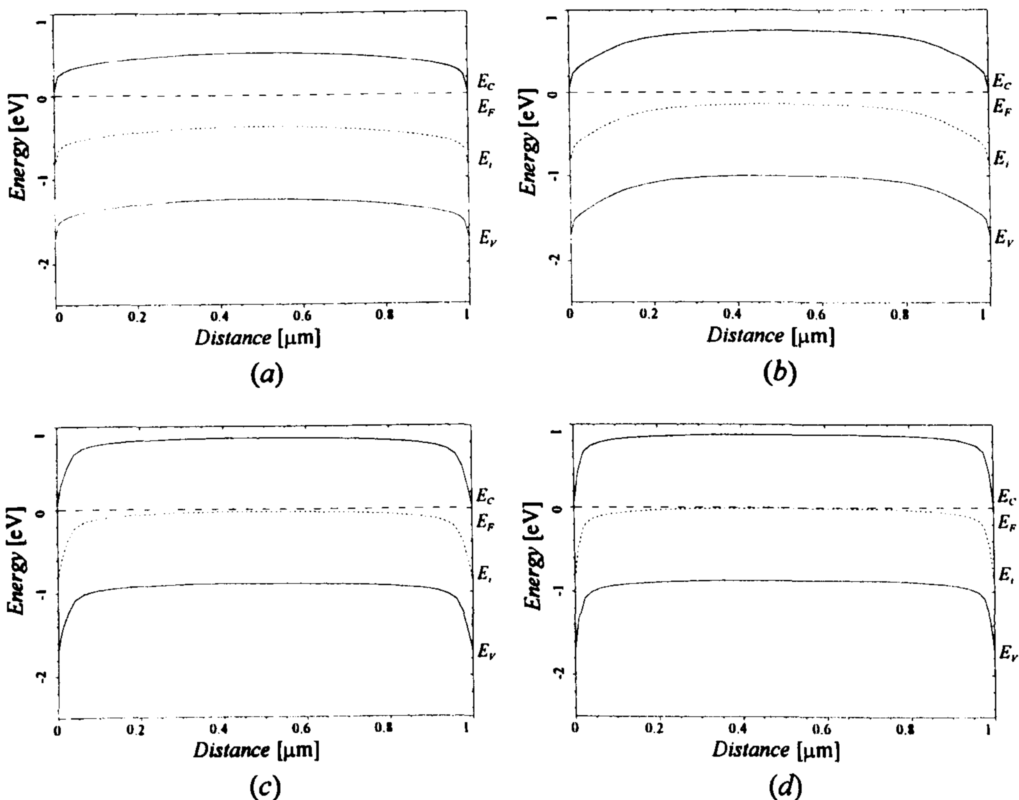


Figure 3.14 The energy band diagram of the a-Si:H film with a single set of traps at the energy level of 0.2 eV, *and densities of (a)* 1×10^{15} cm^{-3}, *(b)* 3.2×10^{15} cm^{-3}, *(c)* 3.2×10^{16} cm^{-3}, *and (d)* 1×10^{18} cm^{-3}.

or half of the film thickness, and for trap densities less than this amount the space charge regions overlap (Fig. 3.14a, b). The simplified theory of regional approximation is valid only if W is less than half of the film thickness [20]. With very low trap densities, the Fermi level is above the trap level throughout the film and all the trap states are virtually filled by the injected electrons (Fig. 3.14a). Therefore, the trap should be considered as a deep trap. Actually, a slope of two SCL regions can hardly be observed on the *J-V* curve corresponding to this trap density. It cab be seen that except for high trap densities, the Fermi level, prior to the application of voltage, is above midgap. Therefore, the condition at low trap densities is far away from assumptions in the regional approximation, and there is an error in applying Eqns. (3.29) and (3.30).

From (3.28b), the voltage at the intercept of Ohmic and SCL regions is proportional to $n_0 / \theta = n_t + n_0$. Both values of n_t and n_0 depend on the position of Fermi level, which is influenced by many parameters, such as density and energy level of traps, and thickness of film, and therefore finding a trend for variation of the intercept voltage with trap density is very complicated. The variation of the onset voltage of SCL region versus trap density is shown in Fig. 3.13b.

Variation with Trap Energy Level

The *J-V* characteristics of a sample with a single set of traps with density of 2×10^{17} cm^{-3} positioned at energy levels of 0, 0.1, 0.2, ..., and 0.8 eV is shown in Fig. 3.15. The four different regions can be seen on most curves. For E_t = 0.7 eV and E_t = 0.8 eV the Ohmic region joins directly to the trap-free region like a trap-free case. In the other words, traps very close to the conduction band have less effect on the *J-V* characteristics, except when their density is comparable to the density of states at the conduction band mobility edge.

The voltage at onsets of TFL and trap-free regions are about 100 V and 120 V respectively, which differ with a factor of two less than the 150 V and 200 V calculated from (3.29b) and (3.30b).

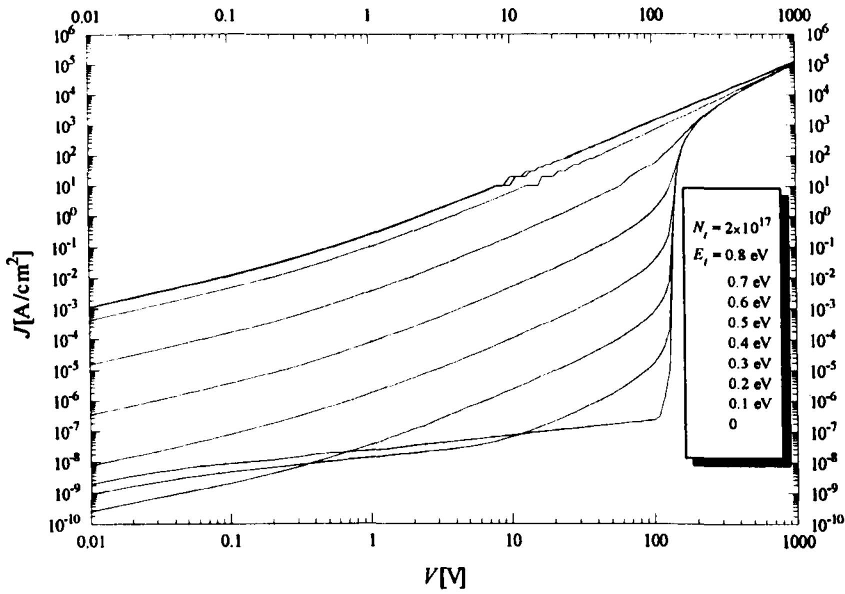


Figure 3.15 The variation of J-V characteristics of a-Si:H with the energy level of single set of traps with density of 2×10^{17} cm^{-3}.

For $E_t = 0$ and $E_t = 0.1$ eV, there is a reduction of slope after the Ohmic region, the reason of which is not well understood. One possible reason is that these traps act as recombination centers, which can reduce the concentration of free carriers and hence the current.

Variation with Temperature

The variation of *J-V* characteristics with temperature is shown in Fig. 3.16. A single set of traps with density of 1×10^{17} cm^{-3} positioned at energy level of 0.2 eV is used in this simulation and the temperature is varied between 250 K and 500 K. By increasing the temperature, the values of n_0, n_t, and θ will increase, resulting in an increase in current in the Ohmic and SCL regions. All the curves merge in the trap-free region, in which the current-voltage relationship is independent of temperature.

At high temperatures, there is again a reduction in the slope of the *J-V* curves between the Ohmic and SCL regions, which is not well understood.

3.4.2.3 Material with Multiple Sets of Traps

In this part multiple sets of discrete traps are set in the a-Si:H and the simulation results under different conditions are discussed. At the first stage two sets of

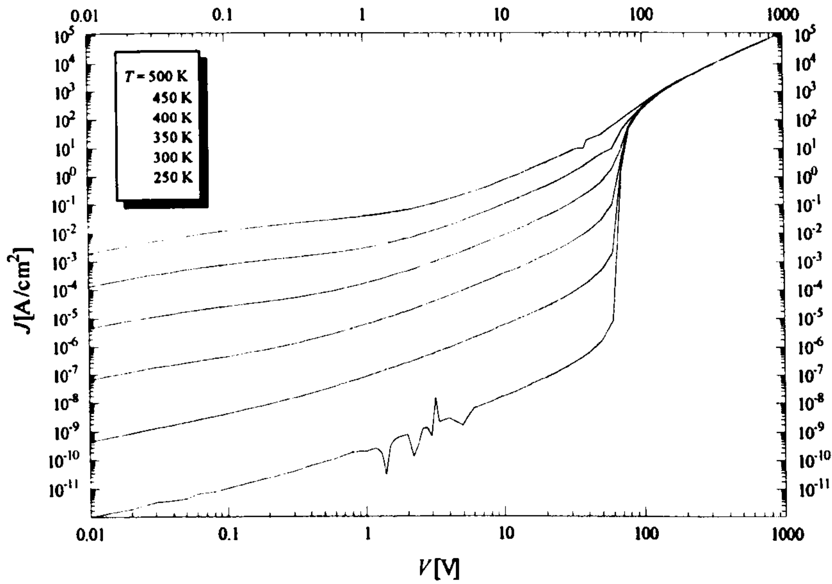


Figure 3.16 Variation of J-V characteristics of a-Si:H with temperature. A single set of trap with density of 1×10^{17} cm^{-3} *positioned at energy level of* 0.2 eV *is set.*

traps are set in the program, one with constant density of 1.2×10^{17} cm^{-3} at zero energy level, or the middle of bandgap, and the density and energy level of the other traps is varied. The thickness and width of film are 0.2 μm and 2 mm, respectively, and both contacts are aluminium. The mobility of electrons is set to 0.1 cm^2 V^{-1} s^{-1} and that of holes is 0.01 cm^2 V^{-1} s^{-1}. The simulation is performed at temperature of 250 K.

The resulted *J-V* characteristics for N_{t2} = 1×10^{16} cm^{-3}, 3×10^{16} cm^{-3}, 9×10^{16} cm^{-3}, 2.7×10^{17} cm^{-3}, 8.1×10^{17} cm^{-3}, 2.4×10^{18} cm^{-3}, 7.3×10^{18} cm^{-3}, and 2.2×10^{19} cm^{-3}, are shown in Fig. 3.17a-f for energy levels of E_{t2} = 0.1 – 0.6 eV. When the energy level of the second trap is very close to that of the first one (Fig. 3.17a), both traps act like a single trap and the characteristics are like the single trap case. For higher energy levels, the effect of both traps is visible in the characteristics (Fig. 3.17b-e). However, by increasing the energy level of the second trap, its effect becomes less and less, and for energy levels more than 0.6 eV, the second trap has no effect on the characteristics (Fig. 3.17f), except when its concentration is very high (not included in the simulation). The first trap introduces an SCL region with slope of two only if its energy level is well separated from that of the second trap and

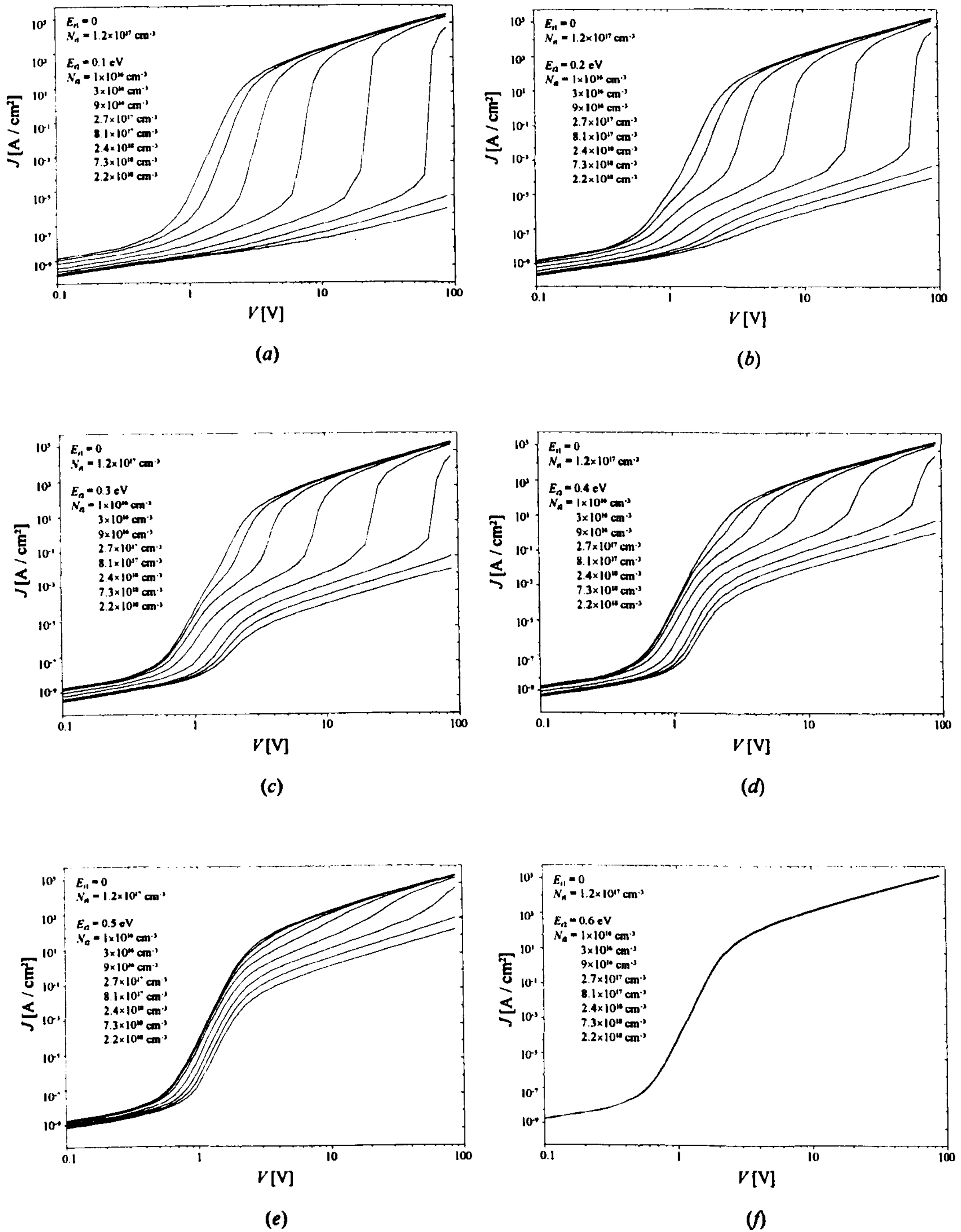


Figure 3.17 The J-V characteristics of a-Si:H with two sets of discrete traps. The first set with density of 1.2×10^{17} cm^{-3} *at the center of the bandgap, second set at energy level of (a)* 0.1 eV, *(b)* 0.2 eV, *(c)* 0.3 eV, *(d)* 0.4 eV, *(e)* 0.5 eV, *and (f)* 0.6 eV.

has much lower density than the other does. Otherwise, there is a slope of more than two in the SCL region corresponding to this trap.

The critical voltages, the onsets of SCL, TFL, and trap-free regions for the higher trap, are with a factor of less that three smaller than the values calculated from

(3.41b), (3.42b), and (3.43b), while the values corresponding to the first trap differ with a factor between 4-10 from the theoretical values. The value of mobility calculated from (3.7) in the trap-free region at $V = 1000$ V is equal to 0.10 cm^2 V^{-1}s^{-1}, which is exactly equal to the value set in the program.

The *J-V* characteristics of an a-Si:H film with one, two, three, and four sets of discrete traps are shown in Fig. 3.18. The uppermost curve corresponds to a single set of traps with density of 2.7×10^{18} cm^{-3} positioned at energy level of 0.74 eV. For the next lower one another trap with density of 1.2×10^{17} cm^{-3} is added. In the third one another trap with density of 2.4×10^{17} cm^{-3} at 0.15 eV, and for the most lower one a trap with density of 1.7×10^{17} cm^{-3} at energy level of zero are added. The trap densities and energy levels are chosen so that the effect of each trap can be seen individually on the *J-V* characteristics. The simulation was performed at a temperature of 250 K. There is an SCL region and a TFL region for each trap, however, the slope of the SCL region is more that two as explained in section 3.3.5. The applied voltage has not been enough to reach the trap-free region, which begins at about 200 V.

The effect of Temperature

The *J-V* characteristics of a-Si:H with four traps as described in previous

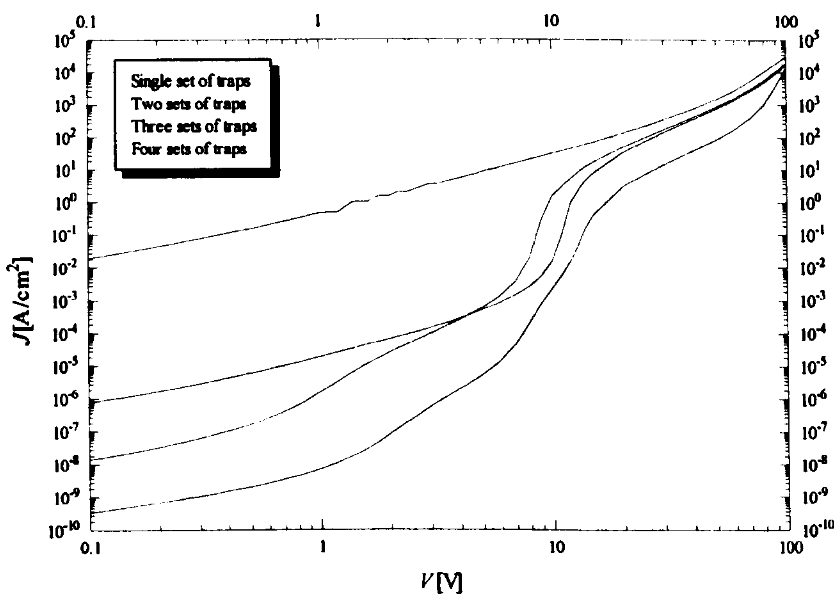


Figure 3.18 Variation of J-V characteristics of a-Si:H with different sets of traps.

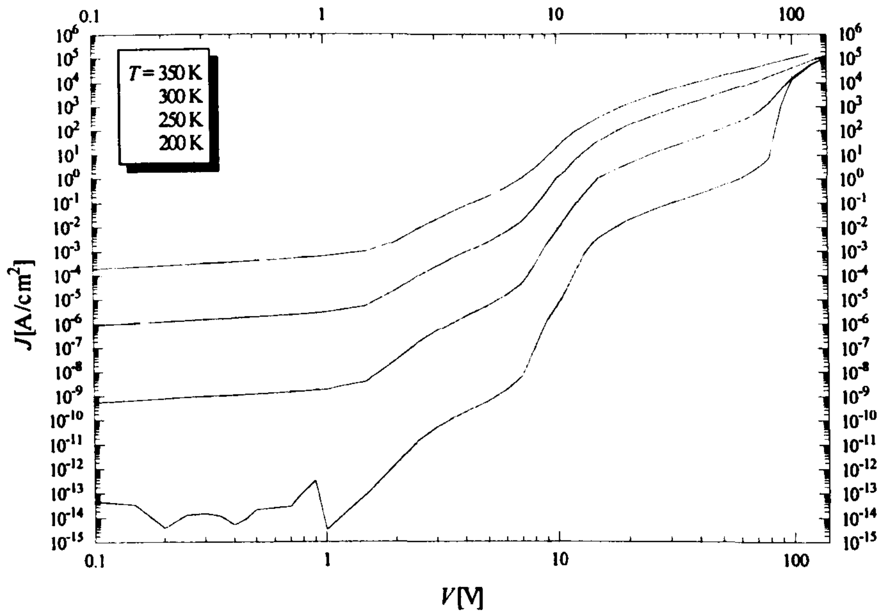


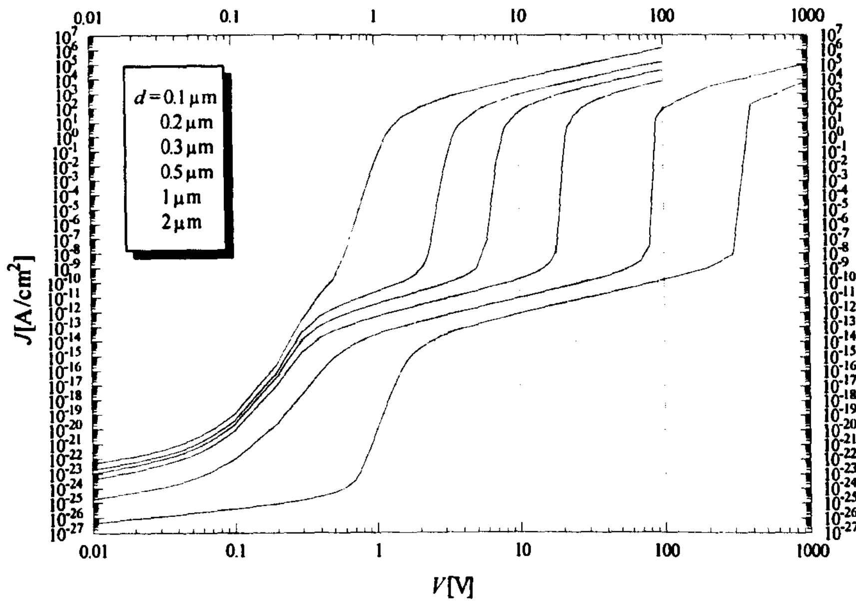
Figure 3.19 Variation of J-V characteristics of a-Si:H with four sets of discrete traps with temperature.

simulation, are shown in Fig. 3.19 calculated at four temperatures between 200 K and 350 K. The effect of each trap is more noticeable on the curves at low temperatures. All curves merge in the trap-free region for which the current-voltage relationship is independent of temperature.

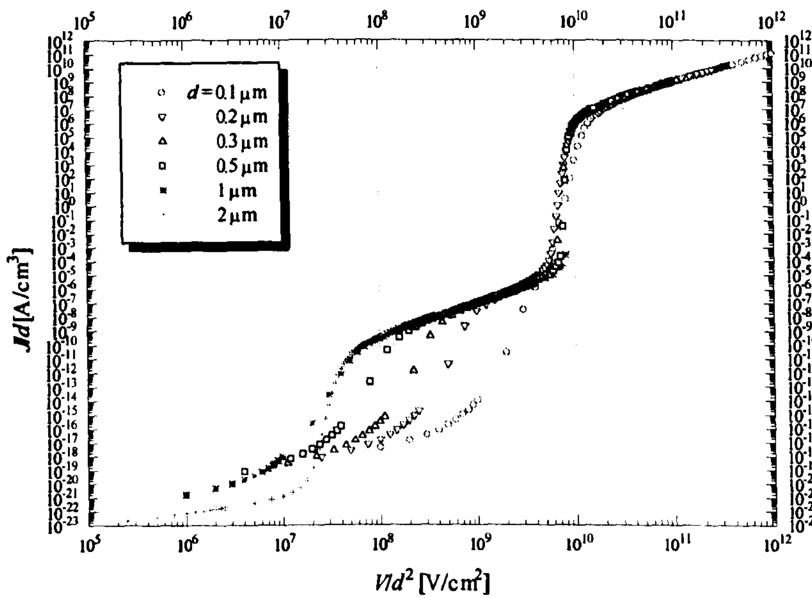
The Scaling Law

In Fig. 3.20a the *J-V* characteristics of a-Si:H are shown with two sets of discrete traps with densities of 2×10^{15} cm^{-3} and 2.18×10^{16} cm^{-3} positioned at 0.6 eV and 0.51 eV below the conduction band mobility edge, respectively. The thickness of a-Si:H film has changed between 0.1 μm and 2 μm and the simulation was performed at a temperature of 150 K. It can be seen that for thick films the effect of each trap is completely distinguishable, while for a film with the thickness of less than 0.3μm, the slope of the SCL region corresponding to the lower trap is more than two.

The variation of J/d versus V/d^2 for the films with different thickness is shown in Fig. 3.20b. In the trap-free region and TFL region of the higher trap all curves are in good agreement with scaling law. However, in the other regions, separation between curves is noticeable. The reason is that in very thin films, many of the trap states are filled by injected electrons and the Fermi level is above the



(a)



(b)

Figure 3.20 Variation of (a) J-V characteristics and (b) J/d versus V/d² of a-Si:H films with thickness.

center of bandgap. All the curves, except the curve for thickness of 2 μm, merge in the Ohmic region.

3.5 CONCLUSION

The steady state space-charge limited current in a-Si:H was described and the theory of regional approximation proposed by Lampert and Mark [20] for a single trap was extended to multiple discrete traps. To gain a better understanding of space-charge limited currents in a-Si:H, especially in analyzing the experimental results, simulations were performed on the SCLC of a-Si:H in the presence of single and multiples traps. The variation of current-voltage characteristics with different parameters such as density and energy level of traps, film thickness, temperature, etc. was investigated.

In the case of multiple traps, when the trap energy levels are well separated and the density of higher traps is much more than that of lower traps, the effect of each trap is distinguishable, otherwise each region is influenced by the action of more than one trap.

The traps that are close to the conduction mobility edge may have an effect only if their density would be enough high compared to the density of states in the conduction band mobility edge.

The regional approximation and the other methods used in analyzing space-charge limited current are valid only if the diffusion current can be neglected. For that purpose it is necessary that the width of space charge region close to the contacts in a-Si:H is much smaller than film thickness. However, even in the worst case the error using a regional approximation is less than a factor of ten.

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CHAPTER FOUR

IV CHARACTERISTICS OF HYDROGENATED AMORPHOUS SILICON

4.1 INTRODUCTION

Current-voltage measurement provides useful information about the electrical properties of hydrogenated amorphous silicon (a-Si:H). The dominant conduction mechanism in a-Si:H is space-charge limited current, which is a useful method to investigate the density of states in the mobility gap of a-Si:H[1-17]. As mentioned in Chapter 3, most researchers have used a sandwich structure of n^+-i-n^+ (p^+-i-p^+) [1-3, 7, 9, 10, 12-14, 18], to measure the current-voltage characteristics. This structure needs many processing steps and there is the risk of dopant contamination remained in the chamber after deposition of highly doped n^+ or p^+ layers [19]. In the present work, a very simple structure has been used that needs only two process steps without any doped layer.

The steady-state SCLC has been used by many researchers to investigate the density of states (DOS) in the mobility gap of a-Si:H. However, since the property of material is highly dependent on the deposition and preparation conditions, the results may be different from one sample to another. Most researchers have used rather thick a-Si:H films (> 0.5 μm) to eliminate the effect of diffusion current [2, 3, 6, 9, 10, 13, 17]. However, there has been a great interest in using very short channel lengths in a-Si:H thin-film transistors, especially in vertical TFTs, to increase the speed of device [20-24]. The leakage current in a-Si:H thin-film transistors is mainly bulk dependent, and study of steady state SCLC which provides information about the bulk of a-Si:H would be beneficial for very short channel devices. In this work a-Si:H films with thickness of 0.2 and 0.3 μm have been used and the validity of different methods for very thin a-Si:H films is investigated.

In this chapter, after describing the experimental process, the measurement results will be presented. The steady-state space-charge limited current is used to investigate the density of states in the mobility gap of a-Si:H, and different methods of determining DOS will be studied. The experimental results will be analyzed using different methods.

4.2 EXPERIMENTAL

The structure used for these measurements is shown if Fig. 4.1. Films of in-

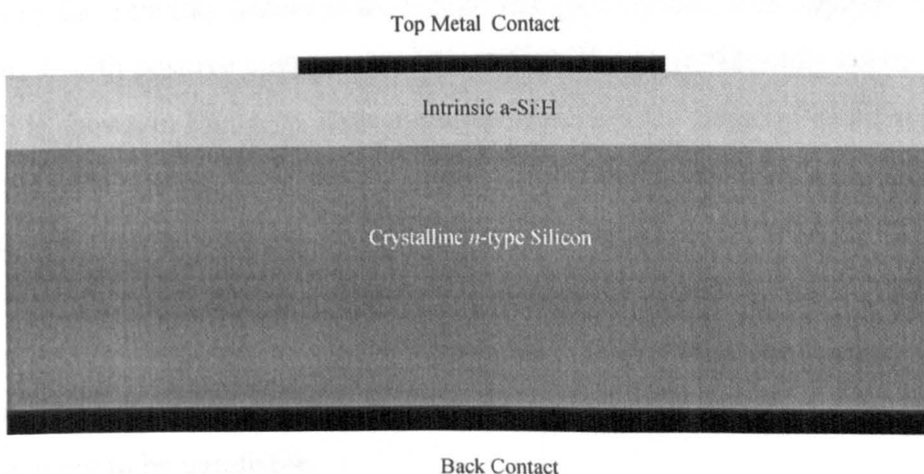

Figure4.1 The device used for IV measurement.

trinsic a-Si:H with thickness of 0.2 and 0.3 μm were deposited on top of the *n*-type crystalline silicon wafers with resistivity of 2-3 Ωcm, and then, aluminium, gold, titanium, and chromium dots were evaporated as top metal contacts on different samples. In most samples aluminium was evaporated on the back of the substrate as a back contact, but because of large contact area, there was no difference between the *I-V* characteristics of samples with and without aluminium back contacts. Although the contact between top metal and intrinsic a-Si:H film is usually rectifying, the *n*-type crystalline silicon can inject substantial number of electrons into the film when a more negative voltage is applied to the bottom contact. This structure simplifies the process, eliminating two deposition steps for doped layers.

A ramp voltage was applied to the samples using a Keithly 230 programmable voltage source and the current was measured by a Keithly 617 programmable electrometer. The measurements were performed at room temperature (295 K). One sample was measured at different temperatures, cooled by a liquid nitrogen cryostat and heated by electric heater, and at pressure of 0.1 mbar.

4.3 RESULTS

The current density versus voltage for a sample, with 0.2 μm a-Si:H and gold circular dots as top contact, measured at room temperature is shown in Fig. 4.2a. The more positive voltage is applied to the a-Si:H side (top contact). The characteristics show about six orders of magnitude rectification at applied voltage of 15 V, which is caused by the Schottky barrier at the a-Si:H and gold contact. The logarithmic plot of J versus V with positive voltage applied to the gold contact (Schottky barrier forward biased) is shown in Fig. 4.2b. The characteristics have the shape of multi-trap space-charge limited current, with an Ohmic region followed by an SCL region with slope of two, and then a combination of TFL and SCL regions with varying slopes. The applied voltage has not been enough to reach to the trap-free region, because the current on the measurement system was limited to 20 mA. Even if the current was not limited, the high power dissipation at higher currents would cause the measurement to be unreliable.

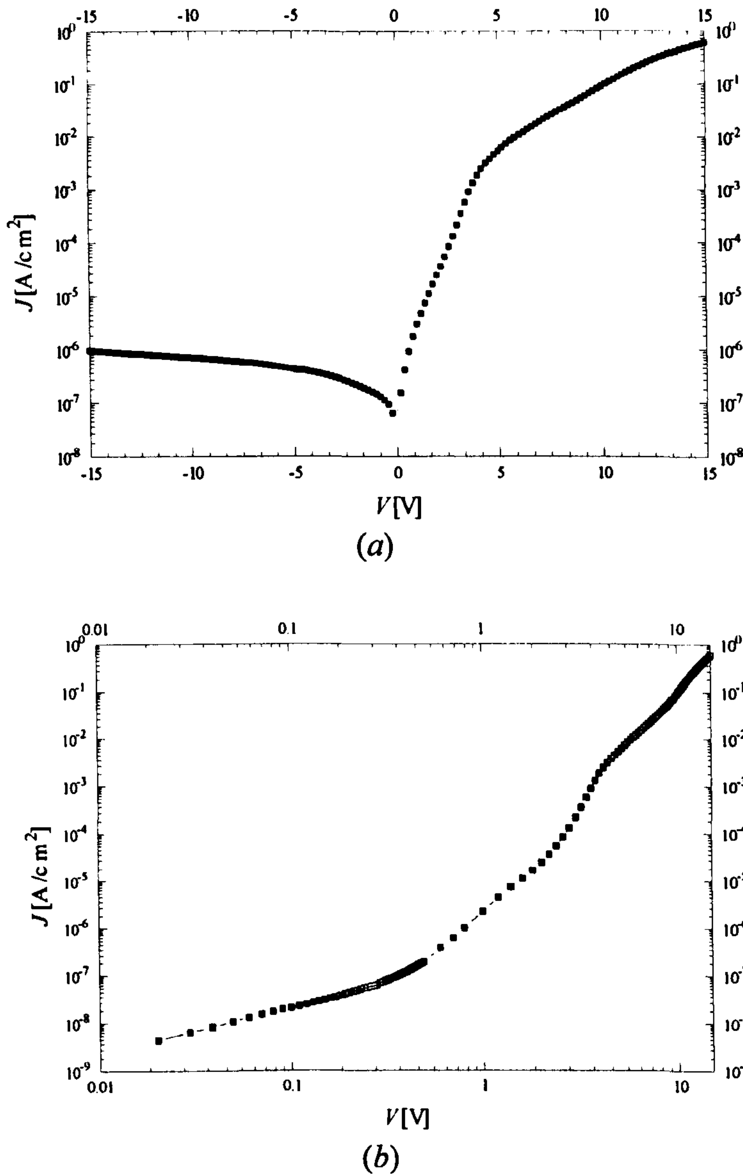

Figure 4.2 (a) Current density versus voltage for a sample with 0.2 μm *a-Si:H and gold contact, and (b) the log-log plot in the forward bias.*

4.3.1 Variation with Temperature

The current-voltage characteristics of a sample with 0.2 μm a-Si:H and gold contacts were measured at temperature range between 139 K and 376 K using a nitrogen cryostat and electric heater under a pressure of 0.1 mbar. The characteristics are shown if Fig. 4.3. The curves at lower temperatures have more variation than those at higher temperatures, as more trap states are filled simultaneously in the latter case. Although most researchers have reported a continuous distribution of traps in

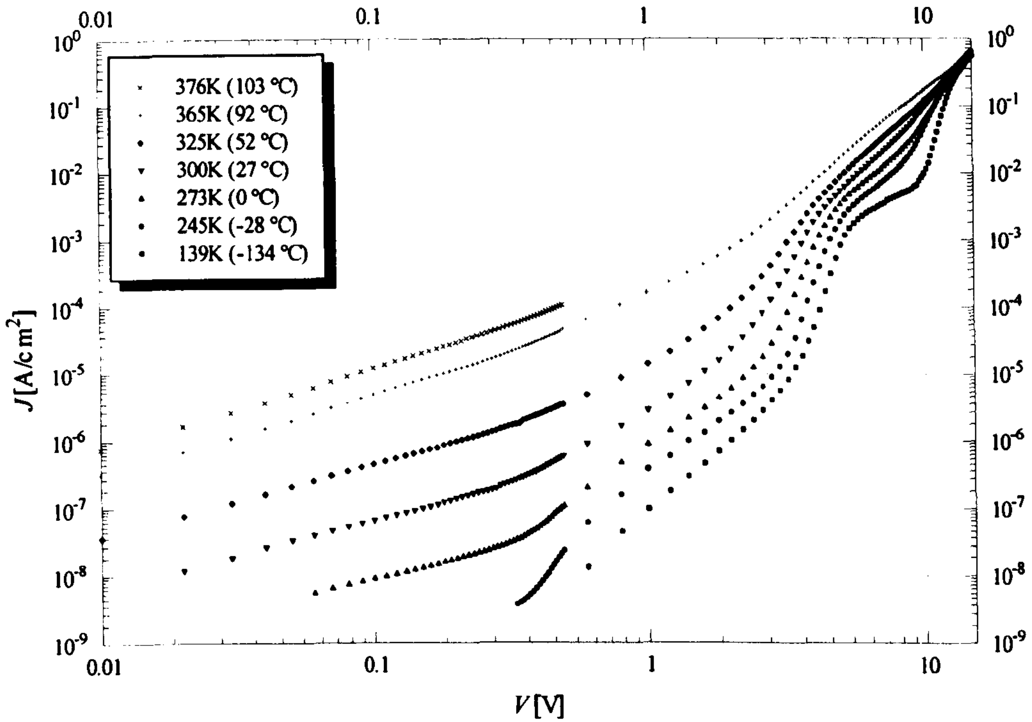

Figure 4.3 Variation of the J-V characteristics of a-Si:H with temperature.

the mobility gap of a-Si:H, the curves, especially at low temperatures, are very similar to that corresponding to multiple discrete traps. In fact, many trap distributions may produce similar SCLC characteristics.

All curves at different temperatures merge at applied voltage of about 12 V. Theoretically, the curves should merge only in the trap-free region, that is the only region in which the current-voltage relationship is independent of temperature. This region is far below the trap-free region as the slope of curves is between 3 and 5. One reason that the curves merge at this voltage could be the presence of a high density of trap states very close to the conduction band mobility edge. From Eqn. (3.21) it can be seen that when the energy level of traps is very close to the conduction band mobility edge, the variation of θ with temperature is small. The presence of a high trap density close to the conduction band is in agreement with the theory of band tails.

Another possibility is that the quasi-Fermi level has reached an exponential band tail. For an exponential distribution of traps, from (3.45), the slope of the J-V plot is inversely proportional to T. However, variation of the value of J with

temperature depends on both applied voltage and trap density. For any value of trap density, there is a voltage below which the current increases with temperature, while it decreases above that voltage. Therefore, in the presence of an exponential distribution of traps, the curves corresponding to different temperatures may meet at a point and diverge afterwards. In Fig. 4.3, it can be seen that at voltages above 12 V, the current at some lower temperatures is more than the current at higher temperatures, in agreement with the above discussion.

The full analysis of the results is given in section 4.5 of the present chapter.

4.4 Methods of Determining the DOS from the SCLC Measurements

The SCLC curves contain useful information about the density of traps in the mobility gap of the material. However, the methods used to determine the density of states or the density of discrete trap levels in the mobility gap are not always accurate. The methods are usually based on some assumptions, so that there may be a large error in the results obtained when these assumptions are not satisfied. The following are the general assumptions used in all the SCLC methods [14]:

- the free electron mobility is field independent,
- diffusion currents are negligible,
- there is an infinite reservoir of free electrons at the injecting contact, and
- there is a spatially homogeneous trap distribution throughout the intrinsic layer.

However, Lampert and Mark has shown that the absence of these assumptions leads to densities of states that are overestimated by less than a factor or two [25]. The SCLC curve is a function of all the traps distributed in the mobility gap. This function is not a unique function. In the other words, materials with different DOS may have similar SCLC curve. Nešpůrek and Sworakowski have shown that the SCLC curve obtained from a single discrete trap has reproduced a bell shape distribution, using the differential method [18].

The methods for determining the DOS from the SCLC measurements can be classified into two categories, depending on the assumptions made about the distribution of traps in the mobility gap:

1. Discrete trap levels or discrete sets of traps,
2. Continuous distribution of traps.

The following briefly explains the methods. The methods for discrete traps are discussed first, and the methods for continuous trap distributions are explained afterwards.

4.4.1 Using the Intercept of the Different Regions

In chapter 3, the currents and voltages of the intercepts of different regions are derived in Eqns. (3.40) to (3.43), for the case of n discrete sets of traps. The density of trap states can be found from the relations for current or voltage of the intercept points. These equations are based on some assumptions (section 3.3.5) that are not satisfied in all practical situations. They can give an overestimate of the density of states but are, on the whole, accurate if the measurements are performed at low temperatures.

4.4.2 Using Gauss's Law

The trap density can also be estimated using Gauss's law in the space-charge-limited region [26]. In this region, the total trapped charge in a specific set of traps is proportional to the change of voltage in this region

$$Q_t = qn_t d = C_0 \Delta V = \frac{\varepsilon}{d} \Delta V, \tag{4.1}$$

and

$$n_t = \frac{\varepsilon \Delta V}{qd^2}, \tag{4.2}$$

where Q_t is the total trapped charge per unit area in a specific set of traps, C_0 is capacitance per unit area, and ΔV is the change of voltage between the beginning and end of the space-charge-limited region.

In the entire space-charge-limited region, the Fermi level is below the trap energy level. If the Fermi level is assumed to be very close to the trap energy level, E_t - E_F in (3.16) can be approximated to zero and this equation can be written as $n_t \approx N_t/2$. So,

$$N_t \approx \frac{2\varepsilon \Delta V}{qd^2}. \tag{4.3}$$

It should be noted again that in this equation is true only if the effect of electrons trapped in the higher states can be neglected. In addition, in this case the value of N_t is an underestimate of the density of traps.

4.4.3 The Temperature Dependency of J-V Characteristics

In the methods mentioned earlier, only the density of traps can be determined from the *J-V* characteristics, and the energy level of traps must be found by the results obtained from the other measurements. From the steady-state SCLC measurements at different temperatures, both the density and energy level of traps can be extracted [27].

In the Ohmic region, the current can be expressed by Ohm's law, Eqn. (3.1), and the concentration of free electrons can be expressed by Boltzmann statistics, Eqn. (3.13). By substituting (3.13) in (3.1) the temperature dependency of current in the Ohmic region can be found

$$J = N_c q \mu_0 \frac{V}{d} \exp\left[-\left(E_c - E_F\right)/kT\right]. \tag{4.4}$$

The current density is proportional to exp [$1/T$], therefore, assuming that the free carrier mobility does not change with temperature, the logarithmic plot of J versus $1/T$ at a constant applied voltage would be a straight line. The slope of this line is

proportional to $E_c - E_F$ and its intercept with the current density axis is proportional to $N_c q\mu_0 \frac{V}{d}$.

In the space-charge-limited current region, the current voltage relationship can be expressed by the Child's law, Eqn. (3.24). By substituting (3.22) in (3.24) the relationship for current versus temperature in the SCLC region can be found

$$J = \frac{9}{8}\frac{N_c}{N_t}\varepsilon\mu_0\frac{V^2}{d^3}\exp[-(E_c - E_t)/kT]. \tag{4.5}$$

As in the Ohmic Region, the current density is proportional to exp $[1/T]$, therefore, the logarithmic plot of J versus $1/T$ at a constant applied voltage would be a straight line. The slope of this line is proportional to $E_c - E_t$ and its intercept with the current density axis is proportional to $\frac{N_c}{N_t}\varepsilon\mu_0\frac{V^2}{d^3}$. By using the slope of this line the trap energy level, and by using its intercept the density of traps can be calculated. The value of $N_c\,\mu_0$ can be found directly from the Ohmic region.

4.4.4 Step by Step (den Böer) Method

This comparatively simple approach was adopted by den Böer [1] and relates the charge injected in a small interval of the applied voltage to the density of states. By changing the applied voltage from V_1 to V_2, the quasi-Fermi level shifts from E_{F1} to E_{F2} resulting in a change in the current density from J_1 to J_2 (Fig. 4.4). Using the den Böer relations

$$\Delta E_F = E_{F2} - E_{F1} = kT\ln\left(\frac{J_2/V_2}{J_1/V_1}\right), \tag{4.6}$$

and

$$N_t(E_F) = \chi\frac{\varepsilon\Delta V}{qd^2\Delta E_F}, \tag{4.7}$$

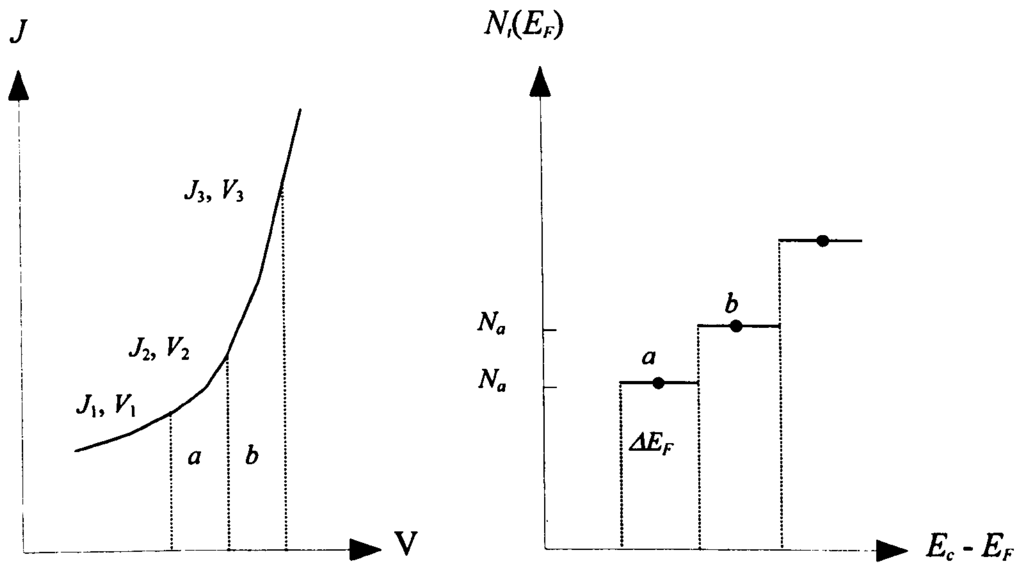

Figure 4.4 Schematic J-V and $N_t(E_F)$ diagrams to illustrate the step-by-step method of analysis (after Mackenzie et al. [2]).

the density of states can be traced out in a step-by-step process (Fig. 4.4). In the above equations, χ, lying between 1 and 3 is a factor accounting for the non-uniformity of the internal space-charge field, and $\Delta V = V_2 - V_1$. The starting position of the Fermi level can be obtained from the Ohmic part of the *J-V* characteristics, Eqn. (4.4).

In the derivation of the above equations, in addition to the general assumptions indicated at the beginning of this section, the density of states is assumed to change smoothly and continuously.

4.4.5 The Differential Method

This more elaborate method of analysis was introduced by Nešpůrek and Sworakowski [18]. It requires an accurate knowledge of the slope of the *J-V* curve as a function of *V*, as $m(V) = d(\ln J)/d(\ln V)$. The density of states and the energy level are then given by

$$N_t\left(E_F\right) = \frac{\varepsilon \kappa_1 \kappa_2}{2qd^2 kT} \frac{V}{m(V) - 1}, \tag{4.8}$$

and

$$E_c - E_F = kT\ln\left(\frac{\kappa_1 q N_c \mu_0}{d}\right) + kT\ln\left(\frac{V}{J}\right), \tag{4.9}$$

where $1 \le \kappa_1 \le 2$ and $\frac{1}{2} \le \kappa_2 \le 1$ are correction factors for the non-uniformity of the internal field and the carrier density.

Further to the general assumptions described before, it is assumed in this method that [18]: quasi-equilibrium conditions are reached at any injection rate, and the occupancy of traps is determined by the position of a common quasi-steady-state Fermi level; the temperature is low enough to consider the quasi-Fermi level as a sharp demarcation line between filled and empty traps, and the density of states varies smoothly and continuously.

4.4.6 Stöcksmann's Method

Both the step-by-step and differential methods have limitations in dealing with the spatial variations of the trapped and free electron densities and the field profile across the thickness of the film [14]. In the differential method, its validity rests on the assumption that the parameters κ_1, κ_2, and m are slowly varying functions of V. κ_1 and κ_2 are not constants and their change with respect to V should be accounted for. In addition, the expression for $N_t(E)$ is not well behaved as m approaches unity, i.e., the derivation breaks down for data close to the Ohmic regime [14].

Stöckmann [28] and later Wiesfield [6] have introduced an exact and more sophisticated method that uses the first, second, and third derivatives of the J-V characteristics. The only limitation is this method is that the variation of the density of states should be smooth and continuous. Stöckmann's relations are described as

$$N_t(E_F) = \left[\frac{(2\gamma - 3)\delta + \zeta}{(2-\gamma)(1-\gamma)+\delta} + \gamma\right](2-\gamma)\frac{\varepsilon}{qd^2kT}V , \tag{4.10}$$

$$E_c - E_F = kT\ln\left(\frac{d}{qN_c\mu_0(2-\gamma)}\frac{J}{V}\right), \tag{4.11}$$

where

$$\gamma = \frac{d[\ln(V/V_0)]}{d[\ln(J/J_0)]}, \qquad \delta = \frac{d\gamma}{d[\ln(J/J_0)]}, \qquad \zeta = \frac{d\delta}{d[\ln(J/J_0)]}. \qquad (4.12)$$

Constants J_0 and V_0 are introduced to ensure the quantities are dimensionless. The only limitation in the above equations is that the density of states should not vary rapidly with energy.

4.4.7 Exponential distribution

In his original paper, Rose [29] discussed the case of an exponential distribution of trapping states, which can be related analytically to the *J-V* characteristics. A more detailed treatment was given by Mark and Helfrich [30]. They showed that a distribution of the form

$$N_t(E) = \frac{N_t}{kT_c}\exp\left[-(E_c - E)/kT_c\right], \qquad (4.13)$$

leads to the *J-V* relation in the SCLC regime

$$J_{SC} = KV^{\nu}, \qquad (4.14)$$

where N_t is the total density of states involved. These are the same equations as Eqns. (3.44) and (3.45) presented by Lampert and Mark [25], described in chapter 3. Comparing (3.45) and (4.14), it is obvious that both N_t and T_c can be determined from the coefficient K and from ν in Eqn. (4.14). This method is particularly suitable at the higher injection levels, where many authors suggested an exponential tail, and the *J-V* characteristics can be represented by a single value of ν.

4.5 Analysis and Discussion

The defect states in the mobility gap of a-Si:H are broadened rather than discrete [31], therefore the SCLC of a-Si:H should be analyzed using the methods based on the continuous trap distribution. However, there are some peaks or maximum points in the density of states distribution that can behave similarly to discrete traps. Therefore, using methods based on discrete traps can provide a good feeling for the peaks in the density of states distribution and their total density and position in the

mobility gap. In this section, the methods based on both discrete and continuous trap states are used to analyze the experimental data and the results from different methods are compared.

4.5.1 Analysis Based on Discrete Trap Methods

The curves in Fig. 4.3, especially at low temperatures, have a shape very similar to the SCLC curves with multiple discrete traps. The Ohmic region, three SCL and three TFL regions can clearly be seen on the curves at low temperatures, and it seems that there is an SCL region after 15 V. The curves at higher temperatures change more smoothly, since the number of electrons captured by the trap states at higher energy levels is not negligible, even at low applied voltages.

The current density J on a logarithmic scale versus $1000/T$ for $V = 0.02$ V and $V = 0.1$ V in the Ohmic region is shown in Fig. 4.5. The data points approximately lie on straight lines, which are consistent with Eqn. (4.4). From the slope of the line corresponding to $V = 0.02$ V, and its intercept with the vertical axis, $E_c - E_F = 0.64$ eV and $N_c\mu_0 = 2.3\times10^{18}\mathrm{V^{-1}s^{-1}cm^{-1}}$ can be found. The values of both N_c and μ_0 depend on the process condition and vary from sample to sample. Spear and Le Comber [32] have reported the value of $N_c\mu_0 = 1\times10^{20}\mathrm{V^{-1}s^{-1}cm^{-1}}$, while Gangopadhyay *et al.* [16] have reported $N_c\mu_0 = 1\times10^{22}\mathrm{V^{-1}s^{-1}cm^{-1}}$ which differs by two orders of magnitude

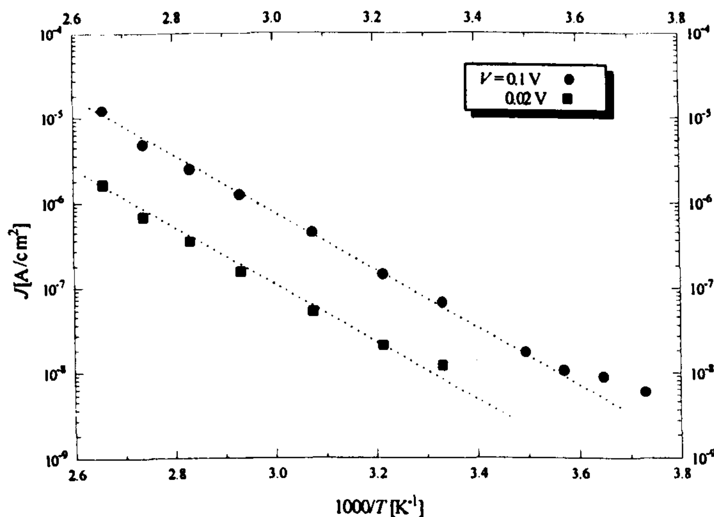

Figure 4.5 Current density versus 1000/*T in the Ohmic region.*

from the former value. Rubinelli has reported $N_c = 7.9\times10^{18}$ cm^{-3} [33] and using this value, $\mu_0 = 0.29$ cm^2 V^{-1}s^{-1} can be found.

The line corresponding to $V = 0.1$ V has nearly the same slope, giving an activation energy of 0.63 eV, and gives the same value for $N_c\,\mu_0$.

The mobility gap of a-Si:H depends on the preparation condition and atomic percent of incorporated hydrogen [34, 35], and varies from material to material. The reported values of mobility gap ranges from 1.5 eV to 1.75 eV [31, 34, 36]. As the material used in the measurement is intrinsic, in the first instant, it was expected that the quasi-Fermi level would lie on the intrinsic Fermi level, which is usually assumed in the middle of mobility gap. However, the activation energy obtained from temperature dependence in the Ohmic region is less than half of the minimum value for the mobility gap. The density of states above and below the midgap is not symmetrical, in either extended or localized states. The intrinsic Fermi level is not, therefore, necessarily in the middle of mobility gap. Its exact position depends on the density of states profile of the material. In chapter 3, section 3.4.2.2, it was explained that when electrons are injected into a film of small thickness, they occupy the trap states close to the intrinsic Fermi level, resulting in a rise in the position of Fermi level. Orton and Powell also found the activation energy of 0.6 eV in SCLC measurements [37].

The current density versus $1000/T$ for some other voltages is shown in Fig. 4.6. The data points for each applied voltage lie on a straight line except for two points corresponding to the two lowest temperatures. By measuring the slope of each line and its intercept with the current axis at voltages in the SCL region, and using (4.5) the energy level and density of traps can be found, respectively. The results are shown in Table 4.1. The energy level of the first trap is 0.63 eV below the mobility edge and very close to the activation energy in the Ohmic region. Therefore, it can be said that, prior to application of voltage, the quasi-Fermi level is pinned to the first trap.

The density of traps calculated using the intercept points and Gauss's law are also given in Table 4.1. It can be seen that in low applied voltages, corresponding to low trap energy levels, the trap densities obtained from different methods are in the

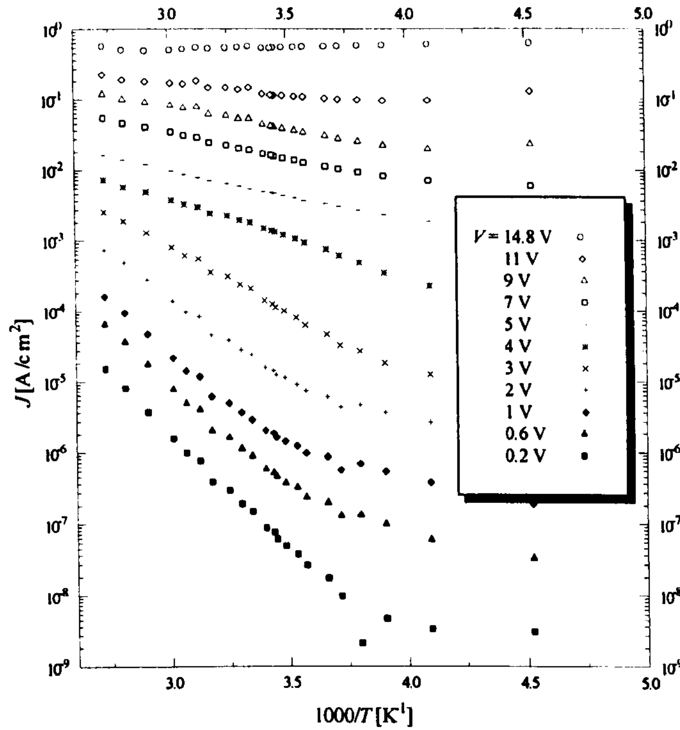

Figure 4.6 Current density versus 1000/T for different applied voltages.

same order. While at higher trap energy levels, the values found from temperature dependence method differ by many orders of magnitude from the values obtained from the other methods. This may be because the quasi-Fermi level is close to the exponential tail, where the temperature dependence of current on voltage differs from that of single trap.

Trap Set	$E_c - E_F$ [eV]	N_t [cm^{-3}]			
		Temperature Dependence	Onset of SCL Regions	Onset of TFL Regions	Gauss's Law
1st.	0.63	2.19×10^{15}	1.11×10^{16}	1.35×10^{16}	2.96×10^{15}
2nd.	0.57	4.39×10^{16}	2.72×10^{17}	1.32×10^{17}	1.02×10^{17}
3rd.	0.14	3.62×10^{21}	7.40×10^{17}	3.29×10^{17}	1.48×10^{17}
4th.	0.07	1.42×10^{22}	-	-	-

Table 4.1 Density of traps obtained by different methods of investigation.

As mentioned before, this analysis does not mean that there are discrete trap states in the mobility gap of a-Si:H. However, rather that there are some peaks or maximum points in the density of states distribution at energy levels of 0.63, 0.57, and 0.14 eV below the conduction band mobility edge, and an exponential tail at 0.07 eV below that.

4.5.2 Analysis Based on Continuous DOS Methods

The density of states distribution, for four different temperatures, derived from the characteristics of Fig. 4.3 using the step-by-step method is shown in Fig. 4.7. The value of χ in Eqn. 4.7 has been assumed equal to one. All curves have two apparent peaks. However their position in the gap and the densities of states at these points, change with temperature. The step-by-step method cannot be used in the Ohmic region, as ΔE_F is zero. The high density at the energy levels between 0.63 and 0.64 eV below the conduction band is not realistic and is a result of the small values of ΔE_F near the Ohmic region. The actual value for density of states is much smaller. The density of states distribution increases at energy levels more than about 0.3 eV below the conduction band. It may approach another peak, or may join to the

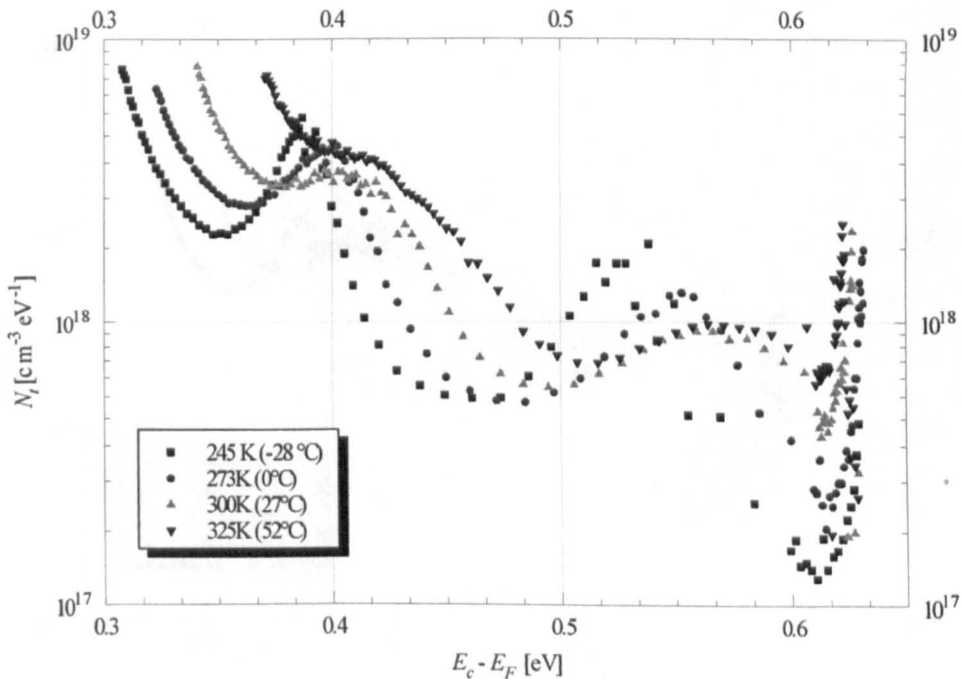

Figure 4.7 The density of states distribution obtained by the step-by-step method.

expnoential tail.

The curves at lower temperatures are more broadened in energy and indicate slightly higher densities. In all methods based on the assumption of continuous density of states, zero temperature statistics are assumed, and the methods are valid only when the temperature is low enough to consider the quasi-Fermi level as a sharp demarcation between filled and empty traps [14]. The DOS obtained from the curves corresponding to lower temperatures seem to be closer, therefore, to the exact trap distribution. On the other hand, it has been assumed that the density of states distribution changes smoothly, while at low temperatures both *J-V* characteristics and the density of states have sharper changes that can produce further error.

The density of states distribution, for four different temperatures derived by the differential method is shown if Fig. 4.8. The values of κ_1 and κ_2 in Eqns. (4.8) and (4.9) are assumed to be equal to one. The curves have the same shape as those derived from the step-by-step method, but are more broadened at higher energies and have much smaller densities, by more than one order of magnitude. Čech has derived the density of states using a differential method which is larger than the value obtained by the step-by-step method, by a factor of four [14]. However, instead of

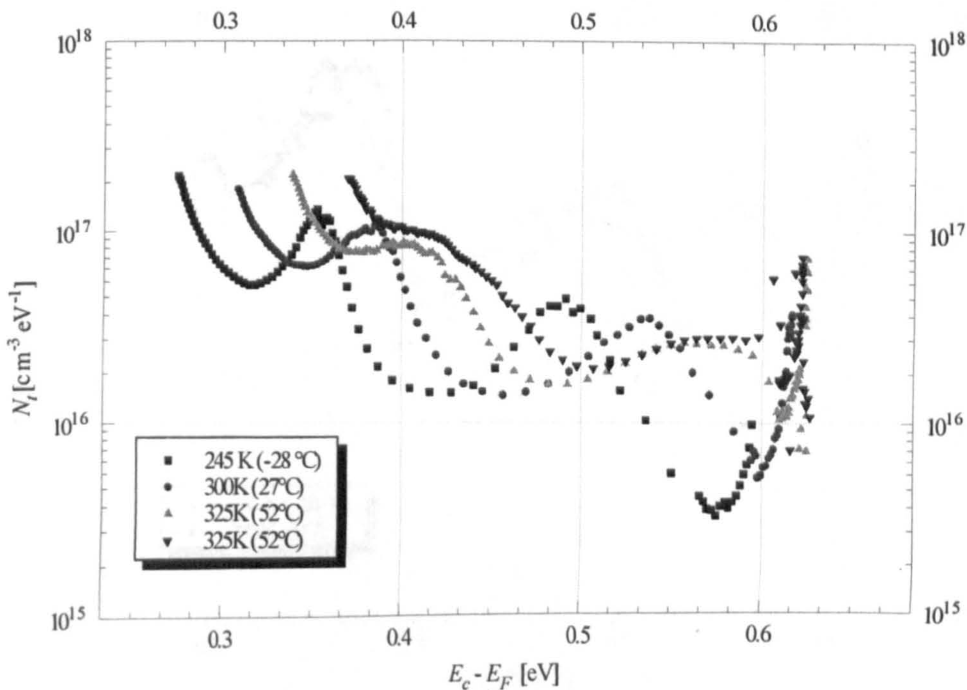

Figure 4.8 The density of states distribution obtained by the differential method.

using the slope of the *J-V* curve for *m* in Eqn. (4.9), he has used the slope of a line connecting each point in the *J-V* characteristics to a fixed point in the Ohmic region. The latter has a smaller slope than the *J-V* curve, resulting in a higher density. Although Nešpurek and Sworakowsky in their original paper [18] on the differential method have defined *m* as the slope of *J-V* curve, however, the *m* used by Čech gives a density of states closer to those obtained by the step-by-step method.

The differential method is not applicable in the Ohmic region, since *m* cannot be equal to one in Eqn. (43.9). The high density of states at energy levels less than 0.6 eV below the conduction band are due to error encountered in the transition region between Ohmic and SCL regions, in which *m* is very close to one.

Stöckmann's method is very sensitive to the measurement noise, because in this method in addition to the slope of the *J-V* curve, its second and third derivatives have also been used. A very small noise in the *J-V* curve can produce a huge change in the derivatives, especially on the second and third derivative, and consequently on derived DOS. The density of states distribution obtained by this method for two different temperatures are shown in Fig. 4.9. A polynomial smoothing algorithm has been applied to the experimental data before analyzing, however the results are still

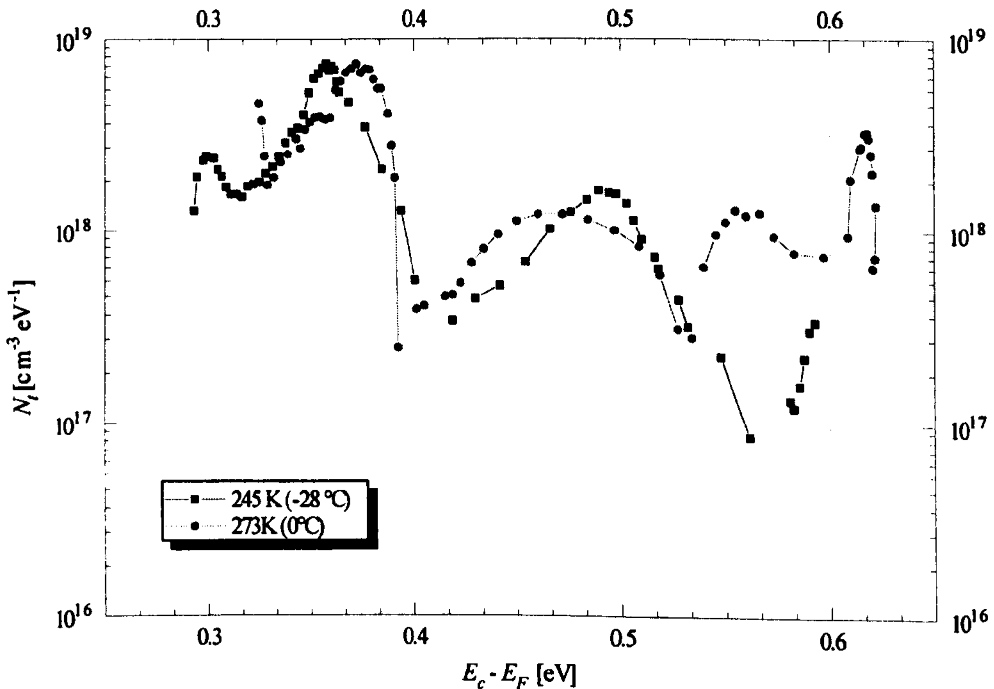

Figure 4.9 The density of states distribution obtained by Stöckmann's method.

very noisy. Applying higher degrees of smoothing or multi-step smoothing may cause the information in the original data to be lost.

This method provides more detailed information about the density of states distribution, although many of these variations could be because of the enlargement of measurement noise. The values of the density of states distribution are very close to those in step-by-step method, and the energy levels are closer to the conduction band.

The density of states distribution obtained from different methods at temperature of 273 K are shown in Fig. 4.10. The results of step-by-step and Stöckmann'n methods are closer, and have higher densities and are in deeper energies. This is in agreement with the results of Čech [14]. He has claimed that only Stöckmann's method can provide a true DOS from SCLC characteristics. However, since it is very sensitive to measurement noise and sharp changes in the *J-V* curve, and the density of states obtained by this method are very close to step-by-step method, the latter would be enough accurate for many investigations.

The trap densities calculated from the intercept of different regions, assuming discrete traps, are very close to the integral of DOS distribution derived by the

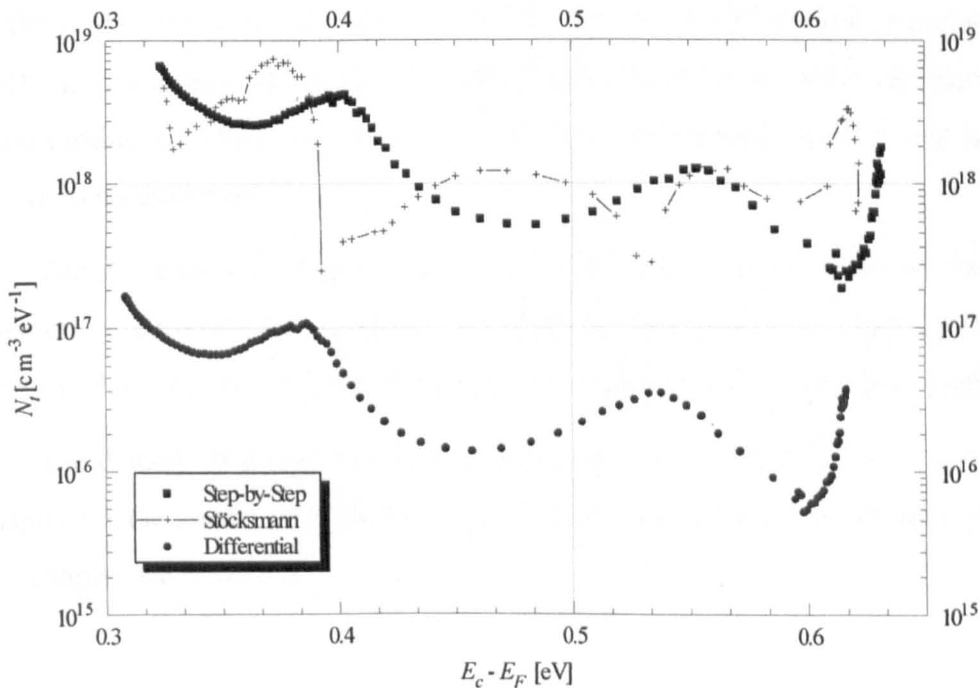

Figure 4.10 The comparison of density of states distribution obtained by different methods.

step-by-step method, around the maximum points. The values obtained for higher traps using temperature dependence are too high to be realistic. The energy levels of the two lower traps obtained from temperature dependence method are nearly close to the maximum points in the density of states distribution. However, the energy levels of higher traps are far away from the energy level of the maximum points in density of states distribution.

4.6 CONCLUSION

The steady-state space-charge limited current methods were used to investigate the density of states in very thin a-Si:H films. A simple structure using *n*-type crystalline silicon as the substrate, and different metal contacts was used. Different methods were applied to derive the density of states from the measured *J-V* characteristics.

The shape of the *J-V* characteristics suggests that there are some peaks or maximum points in the density of states distribution, that can be treated as discrete traps. The densities of traps obtained from the intercept of different regions and from Gauss's law are close to the integral of DOS distribution around maximum points.

The DOS distributions obtained from step-by-step and differential methods have the same general shape. However, the former is a few kT deeper in energy and its DOS is more than one order of magnitude higher than the latter. Stöckmann's method produces a DOS with a value close to the step-by-step method, but is very sensitive to measurement noise.

The *J-V* characteristics measured at low temperatures better satisfy the zero temperature approximation. However, for characteristics that have sharp variations the error in deriving the DOS distribution at low temperatures is more accountable.

The density of states distribution can be used in modelling of a-Si:H devices. In chapter six the results of modelling a vertical TFT using the trap densities obtained in this chapter are presented.

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CHAPTER FIVE

THE METAL-AMORPHOUS SILICON CONTACT

5.1 INTRODUCTION

There has been a great interest in investigating the metal-a-Si:H contacts [1-10]. The contact to a-Si:H has significant importance both in a-Si:H Schottky diodes and in other devices, the most important of which are a-Si:H thin-film transistors. Wronski and Carlson have shown that there are similarities in barrier formation between a-Si:H and crystalline silicon [10]. It is found that the interface states, mainly due to the oxide layer formed on a-Si:H have the main role in the barrier formation [1, 2]. The main conduction mechanisms in a-Si:H Schottky contacts, especially at low voltages are thermionic emission across the barrier and drift/diffusion. However, tunnelling through the potential barrier by both field emission or thermally assisted field emission have been observed in a-Si:H at high electric fields [2, 4].

The Schottky barrier is usually studied on n^+-a-Si:H-metal structures [2-4]. However, some researchers have used metal-a-Si:H-metal sandwich structures with different front and back metal contacts [1]. In the present work a simple structure

using intrinsic a-Si:H on top of an *n*-type crystalline silicon as a substrate has been used. The metal evaporated onto the a-Si:H layer provides a rectifying contact with intrinsic a-Si:H. The current-voltage characteristics were measured in both directions with different metals and the reverse current has been used to analyze the contact properties. The dominant conduction mechanism in reverse bias has been found to be thermionic emission, and using Richardson's theory the potential barrier height with different metals have been calculated. The temperature dependence of the reverse current and the effect of annealing on chromium contacts with a-Si:H have also been investigated.

5.2 THEORY

When a metal is making contact with a semiconductor, because the Fermi levels in the two materials must align in thermal equilibrium, a barrier will be formed at the interface of the metal and semiconductor. This barrier prevents electrons (holes) with low (high) energy from entering the semiconductor, while the carriers can move easily from semiconductor to the metal, resulting in a rectifying behaviour at the contact.

The current-voltage relationship, in general, can be described as [11]

$$J = J_0[\exp(qV/\eta kT) - 1], \tag{5.1}$$

where J_0 is the saturation current density, $q = 1.6\times10^{-19}$ C is the electronic charge, η is the ideality factor, $k = 1.38\times10^{-23}$ J/K = 8.63×10^{-5} eV/K is Boltzmann constant, and T is temperature in Kelvin. The saturation current depends on the barrier height and the conduction mechanism and is generally a function of temperature and applied voltage or electrical field

$$J_0 = J_{00}(V,T)\exp(-q\phi_b/kT), \tag{5.2}$$

where ϕ_b is the barrier height and the prefactor J_{00} depends on the conduction process.

The most common conduction process, especially at low electric fields in high mobility semiconductors is thermionic emission or Schottky emission, in which

the transport of electrons takes place over the potential barrier. The saturation current density in this case is given by [11]

$$J_0 = A^* T^2 \exp(-q\phi_b / kT), \tag{5.3}$$

where A^* is the effective Richardson constant for thermionic emission. The barrier height ϕ_b is reduced with increasing reverse voltage by image-force barrier lowering or the Schottky effect. If the image-force barrier lowering is considered, (5.3) changes to [11]

$$J_0 = A^* T^2 \exp\left[\frac{-q(\phi_b - \Delta\phi_b)}{kT}\right] = A^* T^2 \exp\left[\frac{-q\left(\phi_b - \sqrt{q\mathcal{E}/4\pi\varepsilon_s}\right)}{kT}\right], \tag{5.4}$$

where $\mathcal{E}$ is the electric field and ε_s is the permittivity of semiconductor. A logarithmic plot of J_0/A^*T^2 versus $1/T$ at any reverse voltage yields a straight line whose slope is proportional to the effective barrier height.

In a-Si:H the space-charge mainly originates from the trapped electrons in the surface states or bulk states close to the interface. The excess charge density is equal to

$$\rho = q[(n_f - n_0) + (n_t - n_{t0})] \approx q(n_f + n_t) \approx q\frac{n_f}{\theta} \approx qn_t, \tag{5.5}$$

where n_f is the free electron concentration, n_t is the concentration of trapped electrons, n_0 and n_{t0} are the bulk concentrations of free and trapped electrons, respectively, and θ is the ratio of free electron to total electron concentrations.

The space-charge can be approximated by $\rho \approx qN_t$ for $x < W$, and $\rho \approx 0$ and $dV/dx \approx 0$ for $x > W$, where N_t is the total density of traps and W is the depletion width. Solving the Poisson equation and using the boundary conditions yield

$$|\mathcal{E}(x)| = \mathcal{E}_m - \frac{qN_t}{\varepsilon_s}x, \tag{5.6}$$

$$V(x) = \frac{qN_t}{\varepsilon_s}\left(Wx - \frac{1}{2}x^2\right) - \phi_b, \tag{5.7}$$

$$W=\sqrt{\frac{2\varepsilon_s}{qN_t}\left(V_{bi}-V-\frac{kT}{q}\right)},\tag{5.8}$$

where

$$\mathcal{E}_m=\mathcal{E}(0)=\sqrt{\frac{2qN_t}{\varepsilon_s}\left(V_{bi}-V-\frac{kT}{q}\right)},\tag{5.9}$$

is the maximum electric field at the interface, V_{bi} is the built-in potential, and V is the applied voltage. The maximum electric field is responsible for barrier lowering, since it takes place at the interface. Substituting $\mathcal{E}$ in (4.4) by $\mathcal{E}_m$ in (5.9) yields

$$J_0=A^*T^2\exp\left(\frac{-q\phi_b}{kT}\right)\exp\left\{\frac{q}{kT}\left[\frac{q^3N_t(V_{bi}-V-kT/q)}{8\pi^2\varepsilon_s^{\;3}}\right]^{1/4}\right\}.\tag{5.10}$$

At reverse voltages of more than a few tenths of a volt, the terms V_{bi} and kT/q are negligible and $\ln J_0$ is proportional to $V^{1/4}$. A logarithmic plot of J_0 versus $V^{1/4}$ yields a straight line whose intercept with the vertical axis can give an estimate of barrier height.

Another conduction process is the drift and diffusion of electrons through the space-charge region, and the saturation current can be described by [11]

$$J_0=qN_cv_D\exp\left(-\frac{q\phi_b}{kT}\right)\approx qN_c\mu_0\mathcal{E}\exp\left(-\frac{q\phi_b}{kT}\right),\tag{5.11}$$

where v_D is the effective diffusion velocity and μ_0 is the electron mobility. Considering image-force barrier lowering, (5.11) changes to

$$J_0\approx qN_c\mu_0\mathcal{E}\exp\left[-\frac{q\left(\phi_b-\sqrt{q\mathcal{E}/4\pi\varepsilon_s}\right)}{kT}\right].\tag{5.12}$$

When both thermionic emission and drift/diffusion conduction processes are present, the saturation current can be described as [11]

$$J_0=q\left(\frac{v_R}{1+v_R/v_D}\right)N_c\exp\left(-\frac{q\phi_b}{kT}\right),\tag{5.13}$$

where

$$v_R = A^* T^2 / q N_c \tag{5.14}$$

is the effective surface recombination velocity. If $v_R << v_D$ the thermionic emission is dominant and (5.13) changes to the Richardson equation (5.3), and if $v_D << v_R$ the drift/diffusion process is dominant and (5.3) changes to (5.11).

At higher electric fields, the conduction can occur by electrons tunnelling through the potential barrier, especially for highly doped semiconductors. The tunnelling or field emission is expressed by the Fowler-Nordheim equation [11, 12]

$$J_0 = \frac{q^3 \mathcal{E}^2}{16\pi^2 \hbar \phi_b} \exp\left[-\frac{4\sqrt{2m^*}(q\phi_b)^{3/2}}{3q\hbar\mathcal{E}}\right], \tag{5.15}$$

where $\hbar = 1.05\times10^{-34}$ Js is the reduced Plank constant and m^* is the electron effective mass. The probability of tunnelling can be characterized by parameter [4]

$$E_{00} = (\hbar/2)\sqrt{N/m^* \varepsilon_s}\,, \tag{5.16}$$

where N is the space-charge density. For a doped material N is the impurity concentration, but for intrinsic a-Si:H it could, for example be the total density of traps. E_{00} is the energy below ϕ_b where the tunnelling probability is e^{-1} [4]. If $E_{00} << kT$ thermionic emission dominates, and if $E_{00} >> kT$ field emission dominates. In the intermediate range where E_{00} is in the same range as kT, thermionic field emission or tunnelling enhanced thermionic emission is the dominant process [4].

Another conduction mechanism is the generation-recombination of carriers through midgap states at the metal semiconductor interface or in the bulk states near the interface. This conduction mechanism may have an important role for very high surface or midgap density of states and for high barrier heights where tunnelling is not important [4].

5.3 Experimental

The measurements are performed on the same structure shown in Fig. 4.1 and described in chapter three. There is a Schottky contact at the interface of the a-Si:H

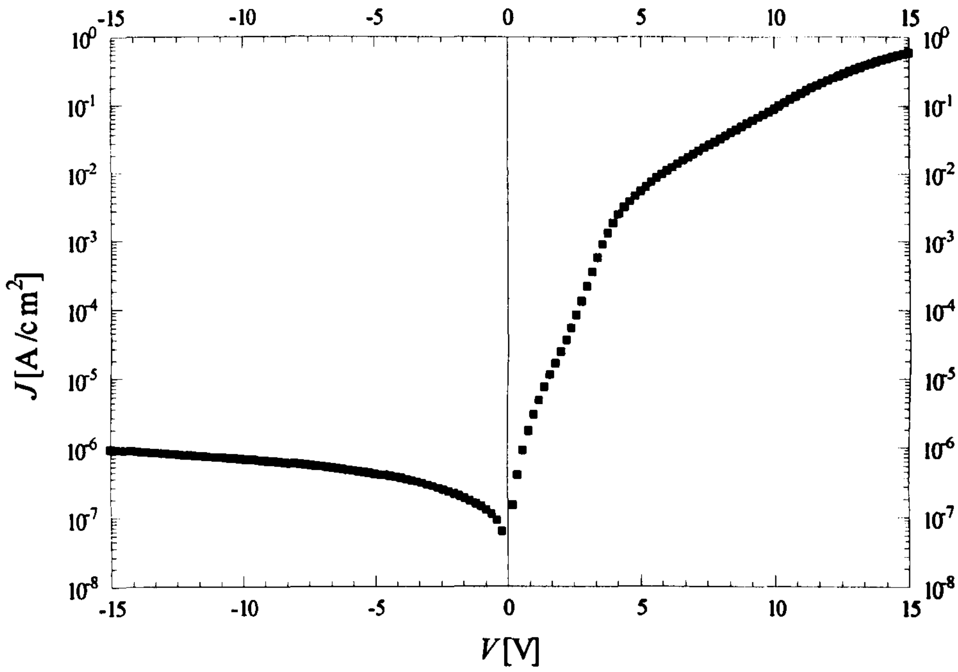
film and top metal. The current versus voltage was measured using a Keithly 230 programmable voltage source and a Keithly 617 programmable electrometer, both in forward and reverse directions. The measurements was performed at room temperature (295 K), and one sample was measured at different temperatures, cooled by a liquid nitrogen cryostat and heated by an electric heater, at the pressure of 0.1 mbar. Aluminium, gold, titanium, and chromium were used as metal contacts. The samples were annealed at 200 °C for one hour in the presence of forming gas, after metal evaporation.

5.4 RESULTS AND DISCUSSION

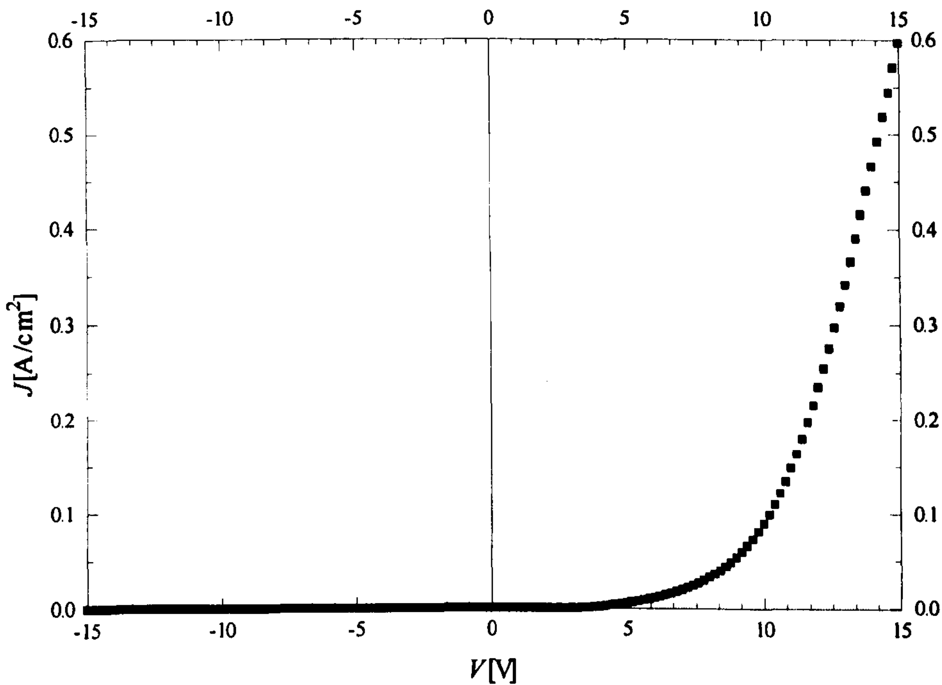
The linear and logarithmic plots of J-V characteristics of a sample with 0.2 μm a-Si:H and a gold contact, measured at 300 K are shown in Fig. 5.1a, b. The dominant conduction mechanism in forward bias, as explained in chapter three, is space-charge limited current. However, in the reverse bias the current is limited by the Schottky barrier, which is discussed in this chapter.

The variation of J versus $V^{1/4}$ is shown in Fig. 5.2 where V is the reverse applied voltage. For V greater than a few kT, the exponential term in (5.1) approaches to zero and $J \approx J_0$. The graph has a good fit with a straight line for voltages above 0.4 V, in agreement with thermionic conduction process, Eqn. (5.10). For this range of voltage, the terms V_{bi} and kT/q in (5.10) are negligible.

An estimate of barrier height can be found by interpolating the plot of J versus $V^{1/4}$ (Fig. 5.2) at $V = 0$ and using Eqn. (5.10). Unfortunately, there is no *a priori* theoretical knowledge about Richardson's constant in a-Si:H. The value of A^* for electrons in free space is 120 A cm^{-2} K^{-2} [13]. For crystalline silicon it is 79 A cm^{-2} K^{-2} for holes and 250-265 A cm^{-2} K^{-2} for electrons [11]. Anderson and Guo have found $A^* = 223$ A cm^{-2} K^{-2} for holes in a-Si:H from IV measurements [1]. Andrews and Lepselter propose that the value of A^* for electrons in a-Si:H is approximately four times that for holes [14], and Anderson and Guo [1] have assumed $A^* = 900$ A cm^{-2} K^{-2} for electrons based on this suggestion. The barrier height found from the intercept point is not very sensitive to Richardson's constant.



(a)



(b)

Figure 5.1(a) The logarithmic and (b) linear J-V characteristics of gold-a-Si:H contact.

For $A^* = 900$ A cm^{-2} K^{-2} and $A^* = 500$ A cm^{-2} K^{-2} barrier heights of 0.93 eV and 0.92 eV were found, respectively, with a difference about 0.01 eV. For $A^* = 120$ A cm^{-2} K^{-2}, the value for electrons in free space, the barrier height is 0.88 eV. In the absence of

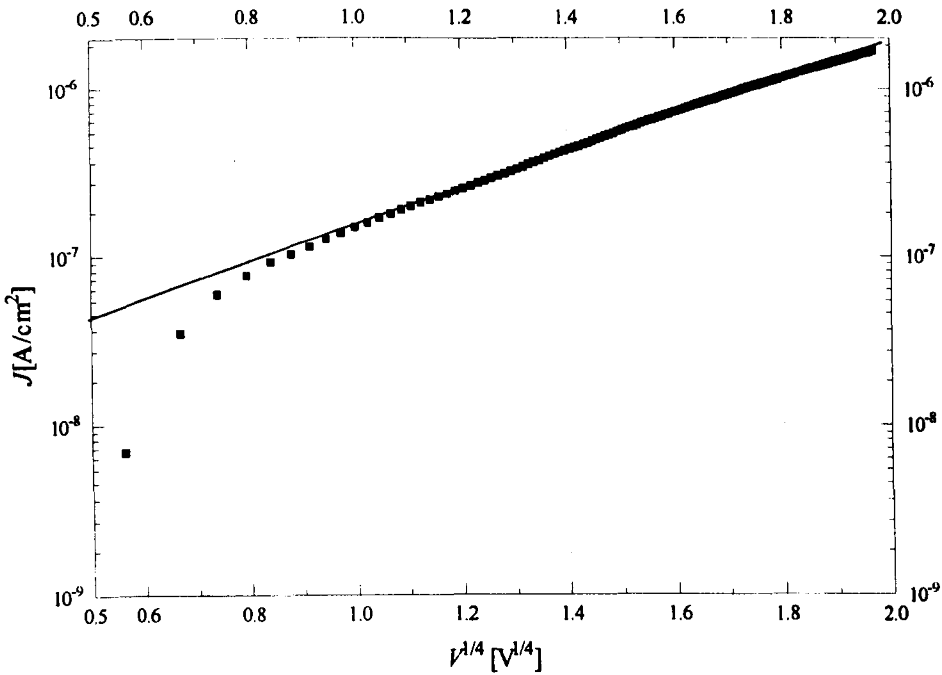


Figure 5.2 Variation of reverse current density versus $V^{1/4}$ for gold-a-Si:H contact.

trap states, the barrier height $q\phi_b$ can be related to the work function of metal $q\phi_m$ and electron affinity of semiconductor $q\chi$ by [11]

$$q\phi_b = q(\phi_m - \chi) - q\Delta\phi \tag{5.17}$$

where $q\Delta\phi$ is the change in the barrier height by image-force barrier lowering. With $q\varphi_m$ = 5.1 eV [11] for gold and $q\chi$ = 3.93 eV for a-Si:H [15], the barrier height of 1.17 eV was found, neglecting the barrier lowering. In the presence of interface traps, the barrier height depends mostly on the density of trap states, and the work function of the metal has little influence on the barrier height.

In chapter 4, the activation energy of 0.63 eV was found for electrons in a-Si:H at zero bias. Using this value, the band bending at the interface of metal and a-Si:H is around 0.25-0.3 eV upwards. Aker *et al.* reported an upward band bending of about 0.2 eV, caused by the surface oxide due to negative charge in the oxide [16]. The direction of band bending is in agreement with results of Aker *et al.* [16] and also Anderson and Guo [1]. Anderson and Guo have found the barrier height of 1.14 eV for a gold contact on *p*-type a-Si:H [1]. Drazin [17] has found the value of 1.1 eV and Hara *et al.* [18] reported 1.07-1.1 eV for the barrier height of gold on

intrinsic a-Si:H. The barrier height obtained in the present work is about 0.2 eV less than the value for a clean surface. It suggests that the barrier height is more affected by interface states.

The value of N_t, the total density of trap states close to the interface incorporating in the space-charge, can be found from the slope of J versus $V^{1/4}$ (Fig. 5.2), using Eqn. (5.10). The value of $N_t = 4.13\times10^{17}$ cm^{-3} was calculated from (5.10) and is close to the total density of the first three traps found in chapter 4 (Table 4.1) using SCLC measurement.

5.4.1 Variation with the Work Function of Metal

The current density versus reverse voltage for a-Si:H with aluminium, gold, titanium, and chromium contacts is shown if Fig. 5.3. The characteristics are nearly the same, except for the sample with chromium contact that has higher current at low voltages but a lower rate of increase. The current density versus $V^{1/4}$ corresponding to the previously mentioned graphs is shown in Fig. 5.4. It can be seen that all curves fit well with straight line, in agreement with thermionic conduction process.

The values of barrier height calculated from the intercept of fitting lines with

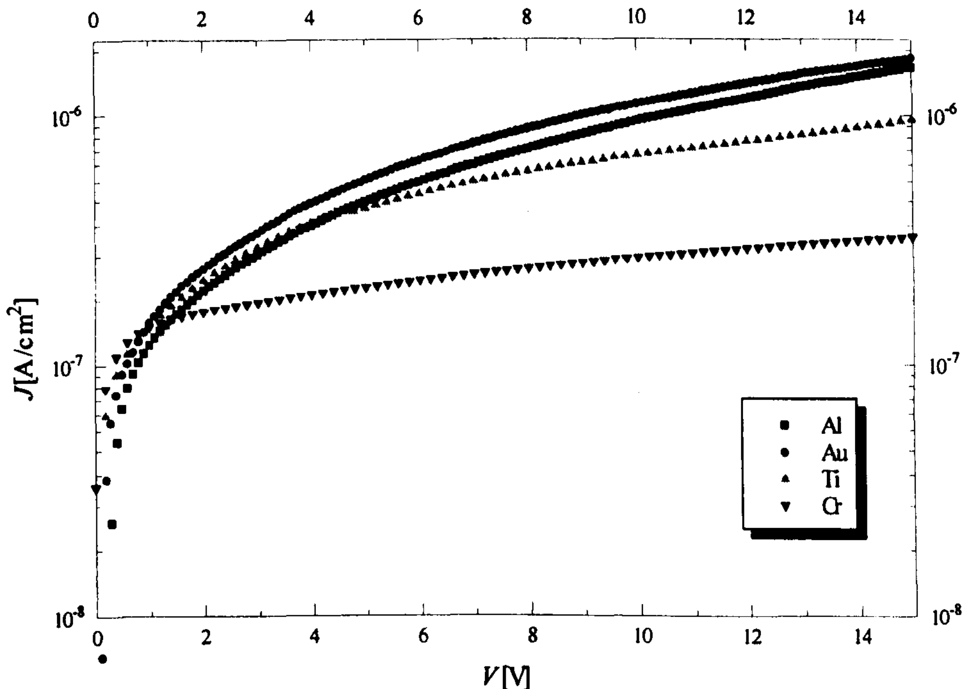


Figure 5.3 The reverse J-V characteristics of a-Si:H contact with different metals.

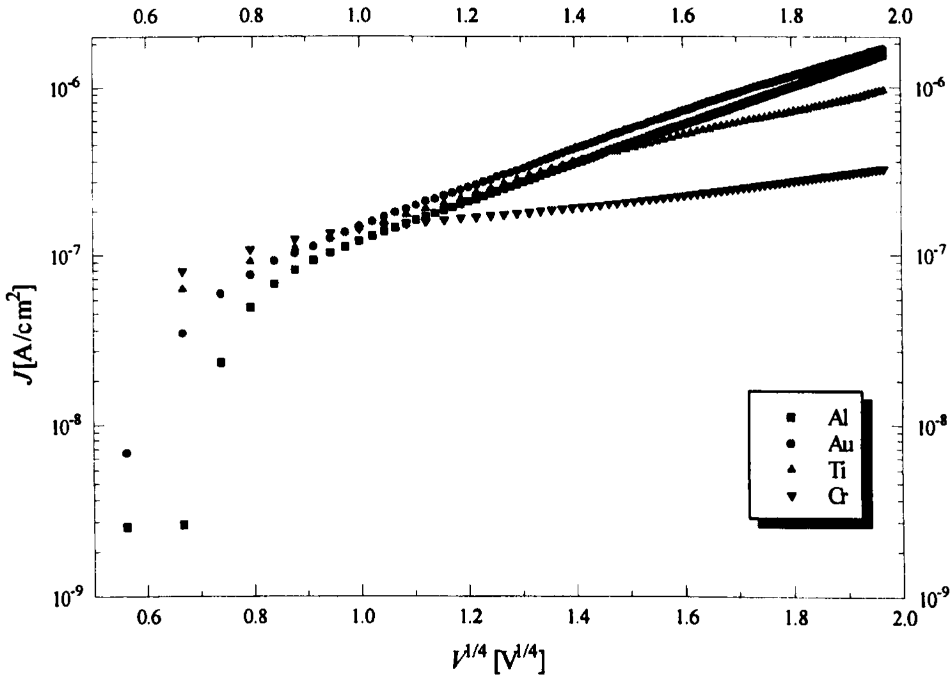


Figure 5.4 The variation of J versus $V^{1/4}$ for a-Si:H contact with different metals.

J axis, assuming $A^* = 500$ A cm^{-2} K^{-2}, are 0.92 eV, 0.92 eV, 0.91 eV, and 0.87 eV for gold, aluminium, titanium, and chromium, respectively. The barrier heights for all metals are nearly the same, except for chromium that is slightly lower. The barrier height for chromium is close to the values 0.83 eV reported by Nieuwesteeg *et al.* [3] and Wronski *et al.* [19], and 0.84 eV reported by Nemanich *et al.* [20].

In the presence of surface states, the relationship between barrier height and the work function of metal can be written as [11]

$$\phi_b = c(\phi_m - \chi) + (1-c)\left(\frac{E_g}{q} - \phi_0\right) - \Delta\phi , \tag{5.18}$$

where

$$c = \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta N_s}, \tag{5.19}$$

and ϕ_0 is the potential difference between Fermi level and valence band at the surface before the metal semiconductor contact was formed, $\Delta\phi$ is the image force barrier lowering, N_s is the density of surface states, and ε_i and δ are the permittivity and thickness of interfacial layer, respectively. Without surface states, c = 1 and (5.18)

reduces to (5.17). With a very high density of surface states, $c \rightarrow 0$ and therefore the barrier height is independent of the work function of metal.

For metal on *n*-type crystalline silicon, Sze [11] has found

$$\phi_b = 0.27\phi_m - 0.55 \tag{5.20}$$

from experimental results. For a-Si:H, Street [13] has quoted

$$\phi_b = 0.28\phi_m - 0.44 \tag{5.21}$$

and Wronski and Carlson [10] have reported

$$\phi_b = 0.25\phi_m - 0.33 \tag{5.22}$$

for electron barriers. However, Nieuwesteeg *et al.* [2] have found

$$\phi_b = 0.10\phi_m + 0.48 \tag{5.23}$$

which is completely different from (5.21) and (5.22). In the present work, the barrier height, except for chromium is independent of the work function of the metal and it seems that only the surface states are responsible for its value. Chromium is known to diffuse through the interface oxide layer [1] and makes a better metallic contact with a-Si:H. Therefore, a lower barrier height for chromium contact can be related to this effect. In Fig. 5.4, it can be seen that the curve for chromium has a lower slope than the others. From Eqn. (5.10) it can be concluded that the density of trap states incorporated in the space-charge is lower in this case. This may also be associated to diffusion of chromium atoms through the interfacial oxide layer.

5.4.2 Effect of Annealing

Annealing the sample after metal evaporation has been found to stabilize the film characteristics. Anderson and Guo [1] have claimed that extensively annealing the samples with chromium contact can provide good metallic contact for near intrinsic a-Si:H. The effect of annealing on a-Si:H sample with a chromium contact is investigated in this section. Successive annealing process steps were performed on a sample with 0.3 μm intrinsic a-Si:H and a chromium contact. Each process step

consists of 2 hours annealing at 200 °C in presence of forming gas, cooling at room temperature, and annealing again for one hour at 200 °C.

The *J-V* characteristics of the sample at different annealing steps are shown in Fig. 5.5a. It can be seen that the reverse current changes extensively with annealing, as the current increases about four orders of magnitude after 12 hours annealing. The current density versus $V^{1/4}$ is plotted in Fig. 5.5b. All the curves have a fairly good fit to a straight line, indicating a thermionic conduction process. The two lower curves have an increase in slope after a voltage of about 5 V, which possibly is because the value of drift-diffusion current has been significant at higher electric fields. This increase is not seen at the next curve, since the electric field in this case is not as strong as the previous, due to lower barrier height. The higher curve has a completely different shape, with a drastically higher slope that decreases at higher voltages. As the current level in this case is relatively high, the contact does not limit the current, and the bulk property may also affect the current.

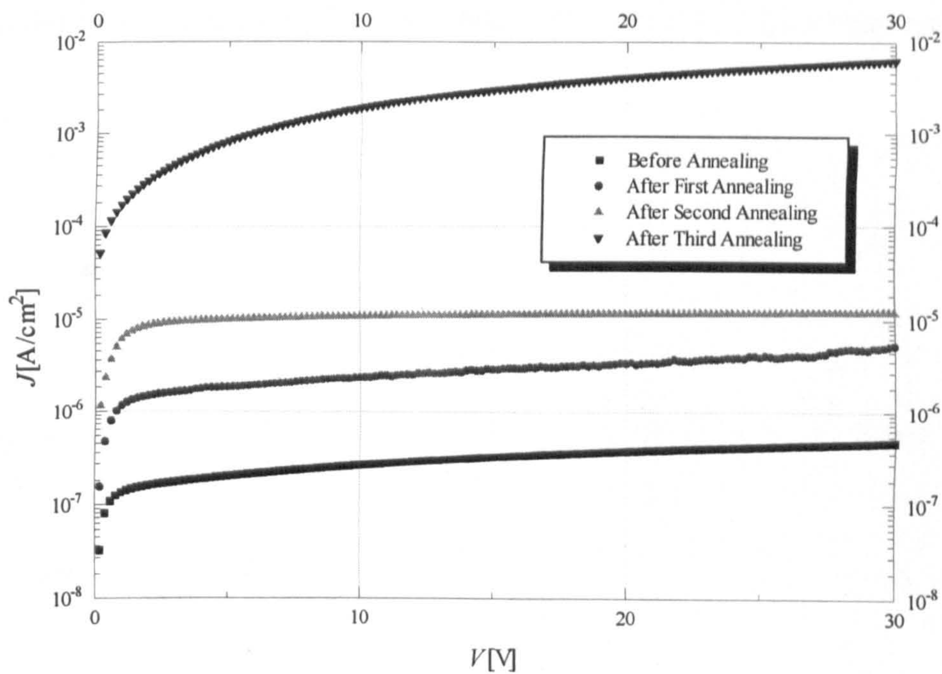
The variation of barrier height, calculated from the intercept of fitting lines with current density axis, versus annealing time is shown if Fig. 5.6, in which the barrier height decreases monotonically with annealing time. However, even with extensive annealing there is a noticeable barrier height and the contact is still rectifying.

The slope of the curves is lower than that of other metals (Fig. 5.4) and, except for the higher curve, decreases with annealing time. It suggests that the density of trap states incorporating in the space-charge reduces with annealing.

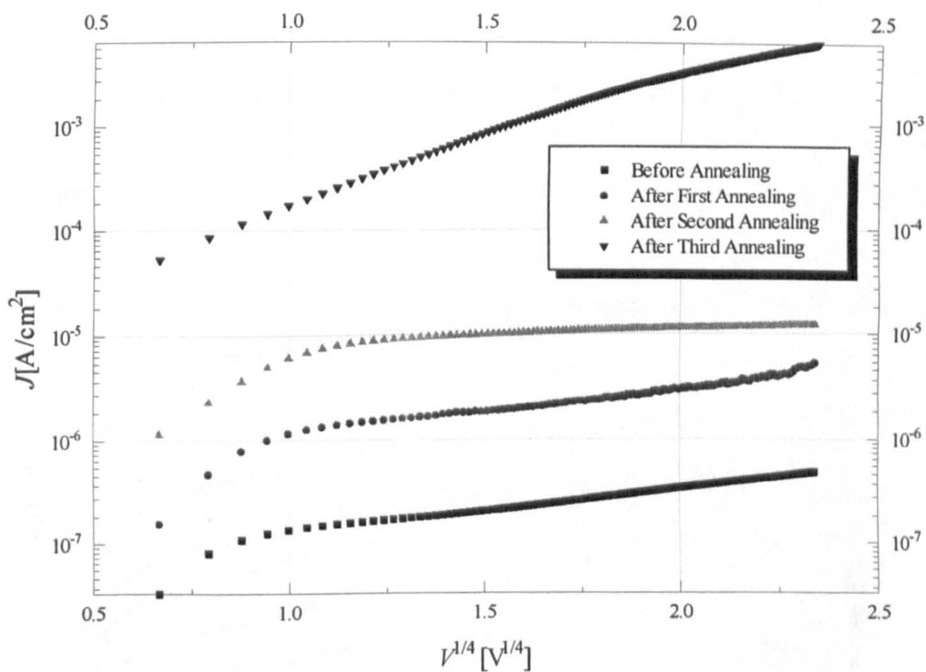
5.4.3 Temperature Dependence

In the thermionic conduction process, Eqn. (5.3), the current is dependent on temperature because of the term T^2 in the prefactor and $1/T$ in the exponential term. A graph of J/T^2 versus $1/T$ therefore, should be a straight line whose slope is proportional to the barrier height.

The reverse *J-V* characteristics for an a-Si:H sample with a gold contact, for some selected temperatures are shown in Fig. 5.7, and the variation of J/T^2 versus $1/T$ for some applied voltages are shown in Fig. 5.8. The data points do not have a



(a)



(b)

Figure 5.5 The variation of (a) J-V characteristics and (b) J versus $V^{1/4}$ with annealing.

perfect fit to a straight line. Instead, they can be fitted on two straight lines at high and low temperatures, and the line at low temperatures has a slightly smaller slope.

The barrier height calculated from the slope of the line at higher temperatures is

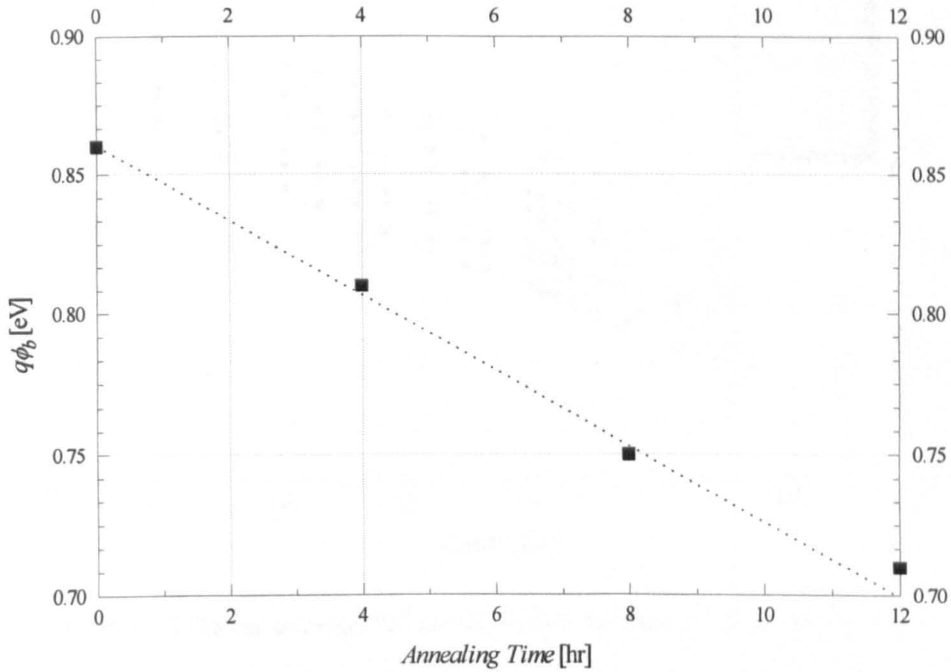


Figure 5.6 The variation of barrier height versus annealing time.

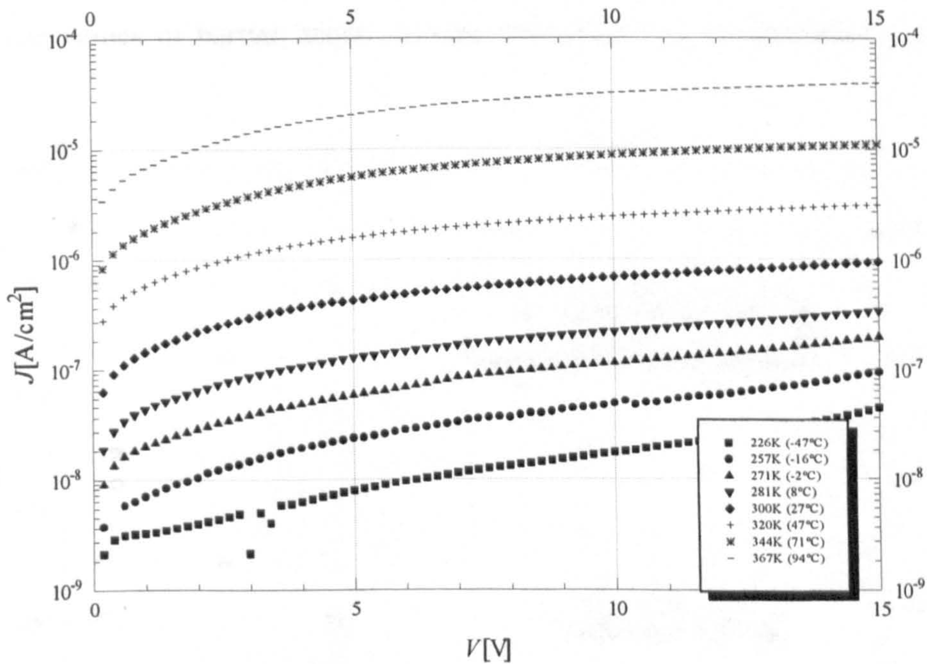


Figure 5.7 The variation of reverse current of gold-a-Si:H contact with temperature.

0.61 eV at applied voltage of 0.2 V, and reduces to 0.53 eV at voltage of 15 V. The variation of barrier height and change of barrier height with voltage are shown in

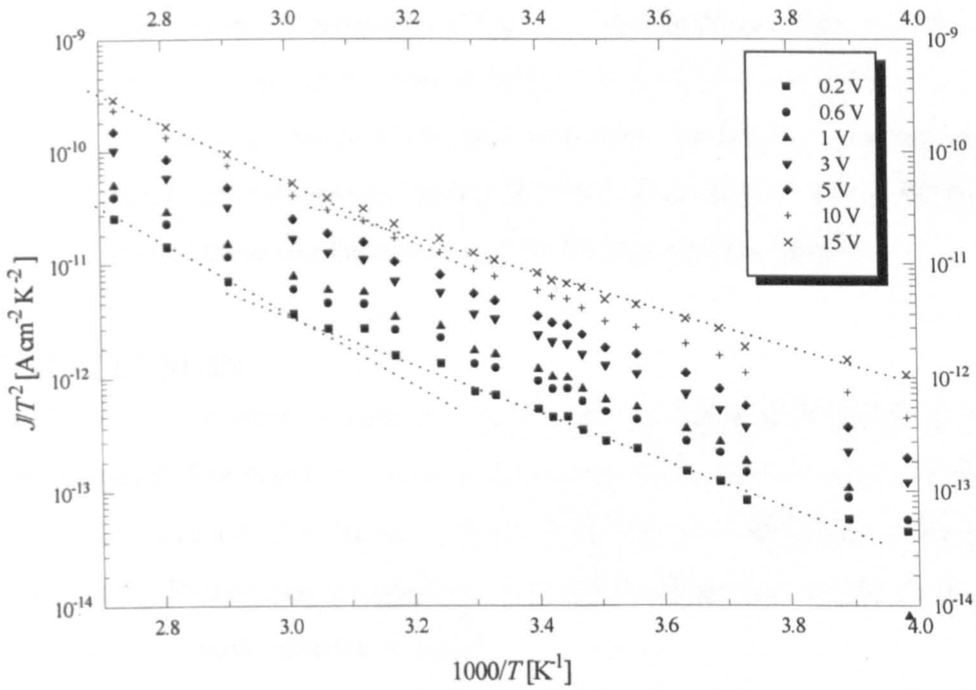


Figure 5.8 The variation of J/T^2 versus 1000/T for characteristics of Fig. 5.7.

Fig. 5.9. The barrier lowering has the best fit with $V^{1/6.7}$. From (5.4) it can be concluded that the maximum electric field is proportional to $V^{1/3.3}$.

The values of barrier height derived from temperature dependence are very

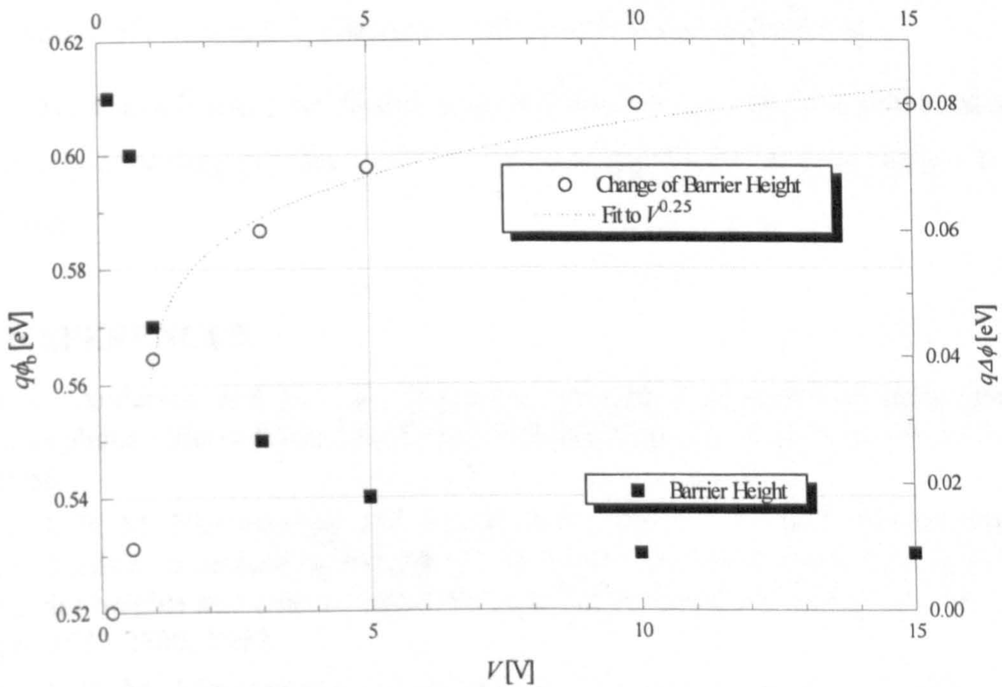


Figure 5.9 The variation of barrier height and change in barrier height with reverse voltage.

different from the values calculated from Fig.5.2. The temperature dependence seems to be more accurate, however, the barrier height calculated by interpolation is closer to published values. The data were checked with other conduction mechanisms, but they did not match any mechanism, except thermionic conduction and drift/diffusion conduction. Both of these mechanisms result in the same barrier height.

5.5 CONCLUSION

The reverse current-voltage characteristics of metal-a-Si:H Schottky contact were investigated. The dominant conduction process in the reverse direction seems to be thermionic emission. The barrier heights of a-Si:H with different contacts were calculated using Richardson's equation. The barrier height was found to be nearly independent of the work function of metal.

The effect of annealing on the chromium/a-Si:H contact was investigated. The barrier height linearly decreases with annealing time. In an extensively annealed sample, it seems that the current is affected by both the bulk and the contact.

The temperature dependence of reverse current in a gold/a-Si:H contact was analyzed. The barrier height at the contact from the temperature dependence of Richardson's equation is about 0.3 eV less than the barrier height calculated from the interpolation of J versus $V^{1/4}$. The reason for this is not well understood.

Most metals make rectifying contacts with intrinsic a-Si:H. Chromium, after extensively annealing provides higher reverse current, however, the contact is still rectifying.

5.6 REFERENCES

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CHAPTER SIX

THE FIELD EFFECT MOBILITY MEASUREMENT

6.1 INTRODUCTION

Carrier mobility in the surface of a semiconductor is different from the bulk because of additional surface scattering. In the bulk, carrier mobility is determined by scattering processes arising from the thermal vibrations of lattice atoms and from any impurities and lattice imperfection. Near the surface, in addition to the normal bulk scattering, free carriers are subject to scattering by the boundary surfaces. This additional scattering generally reduces the carrier mobility below that in the bulk [1]. In addition, the interface may contain a number of surface states or traps, which act as scattering centers and scatter more strongly than the lattice [2]. By reducing the channel thickness, scattering of carriers by the surface becomes more frequent, resulting in lower mobility.

The term "field effect" describes the change in sample electronic conduction taking place as a result of a capacitively field applied normal to the surface. In the presence of traps, some of the carriers induced by the applied field are captured by

the surface and bulk states. The density of mobile charge is less than the density of total induced charge, resulting in lower current. "Field effect mobility," is the effective carrier mobility calculated assuming that all the induced charge is mobile.

The structure usually used for field effect measurement is a field effect transistor similar to inverted-staggered TFTs [3]. However, many researchers have used real TFTs for this measurement. In the present work, a structure similar to inverted-staggered TFT is used for measuring the field effect mobility.

After the theory, the device fabrication and measurement procedure is explained. The resulting data is presented and analyzed in the next section. Finally, the ac field effect mobility measurement is described.

6.2 THEORY

Displacement of mobile charge carriers near the surface of a semiconductor builds up a space-charge region. The space-charge region may be produced by an external electric field, or an electric field caused by proximity of another material with different work function. It may also result from the presence of a localized charged layer at the surface due to surface states [1].

6.2.1 The Semiconductor Surface

Depending on the surface states, doping, and electrical field at the surface, there may be three conditions in the space-charge region; accumulation, when the majority carrier density in the space-charge region is greater than that in the bulk, depletion, when the majority carrier density in the space-charge region is smaller than that in the bulk, and inversion, when the minority carrier density in the surface exceeds the majority carrier density in the bulk. In a-Si:H TFTs, the material is usually intrinsic and there are no majority or minority carriers. Therefore, the above definitions should be revised. However, since the free electrons are the main carriers in the a-Si:H TFTs, the terms depletion and accumulation can be used when the surface is depleted from or accumulated by the free electrons. Inversion has no meaning in the intrinsic materials.

Surface states may be associated with the unfilled orbitals or dangling bonds of the surface atoms. In covalent crystals, for example, a bulk atom forms four valence bonds with its nearest neighbours, but a surface atom can form only three. The remaining unfilled orbital may thus be free to trap an electron [1]. In a-Si:H, the density of states in the surface is much higher than the bulk defect density, so the excess density of states can be attributed to surface states [4].

The conductivity of the surface layer, or space-charge region depends not only on the carrier concentration, which is determined by the barrier height, but also on the carrier mobility at the surface. The carrier mobility at the surface is usually lower than that in the bulk, because of additional scattering at the surface.

A film of a-Si:H is considered between two Ohmic electrodes and an electrical field is applied normal to the surface through an insulator (Fig. 6.1). The film consists of bulk and surface layers that are approximately in parallel. The total resistance of the film, with no applied field, is approximately equal to the bulk resistance. By application of external field, the electrons are accumulated in or depleted from the surface layer. When the field is strong enough, the electrons accumulate at the surface and reduce the surface resistance. The surface conductance can be varied by applying an external field normal to the surface. The change in total resistance is approximately equal to the change in surface resistance, because the bulk resistance remains nearly unchanged by the variation of applied field. The field effect mobility can be found from the change in the surface resistance by the applied field normal to the surface.

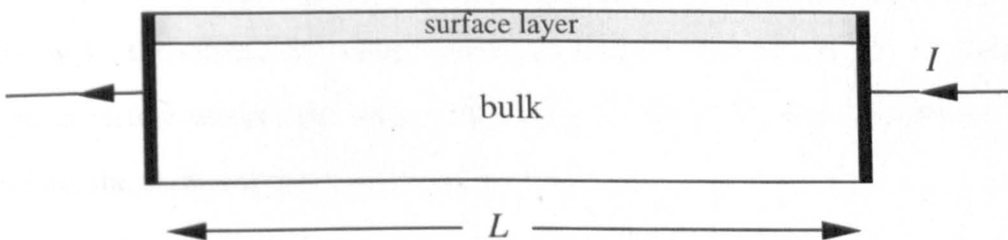


Figure 6.1 The a-Si:H specimen with surface layer.

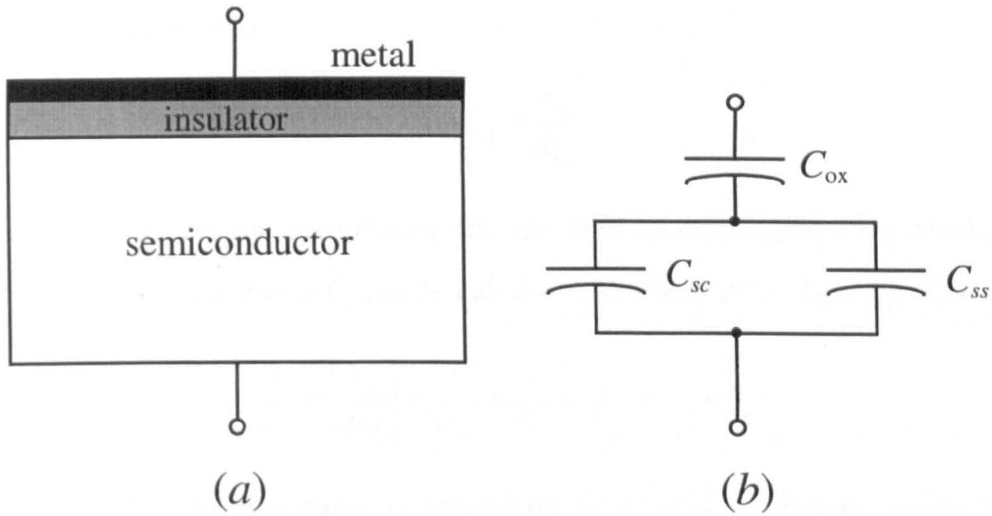


Figure 6.2 (a) A MOS structure, and (b) the capacitors associated to the structure.

A usual MOS structure is shown in Figure 6.2a. Three capacitors may be associated with this structure [1]. The space-charge capacitance (per unit surface area) C_{sc} is defined as the ratio of the space-charge density per unit surface area Q_{sc} to the barrier height V_s

$$C_{sc} \equiv |Q_{sc}/V_s|. \tag{6.1}$$

The surface-states capacitance C_{ss} is defined as

$$C_{ss} \equiv |\Delta Q_{ss}/V_s| \tag{6.2}$$

where ΔQ_{ss} represents the change in surface-state charge density by changing the barrier height from 0 to V_s. The surface capacitance is defined as the ratio of the total change in surface charge density ΔQ_s to the barrier height V_s

$$C_s \equiv |\Delta Q_s/V_s| = |(Q_{sc} + \Delta Q_{ss})/V_s| = C_{sc} + C_{ss}. \tag{6.3}$$

The other capacitance in this structure is associated with the oxide layer. If a change V_0 in the applied voltage between the gate and substrate contacts changes the barrier height by V_s, the change in voltage across the oxide layer will be $V_0 - V_s$, and the change in charge density per unit surface area in the oxide will be equal to ΔQ_s. Therefore, the oxide capacitor can be defined as

$$C_{ox} = |\Delta Q_s/(V_0 - V_s)| \tag{6.4}$$

and may be expressed as

$$C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}} \tag{6.5}$$

where ε_{ox} and d_{ox} are the permittivity and the thickness of oxide, respectively. The effective surface capacitance C_0 can be calculated by combining (6.3) and (6.4)

$$\frac{1}{C_0} \equiv \left|\frac{V_0}{\Delta Q_s}\right| = \frac{1}{C_{ox}} + \frac{1}{C_s} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{ss}} \tag{6.6}$$

and consists of oxide capacitance in series with the parallel combination of the space-charge and surface-state capacitors (Figure 6.2b).

If the thickness of oxide layer is much more than the thickness of space-charge region, the effective surface capacitance approaches the capacitance of the oxide layer

$$C_0 \approx C_{ox}. \tag{6.7}$$

6.2.2 Calculation of Field Effect Mobility

When the voltage applied between the conducting contacts is low enough, the surface conduction can be assumed Ohmic. The conductivity of the surface can be approximated by

$$\sigma_s = n_f q \mu_{FE} \tag{6.8}$$

where n_f is the mean free electron concentration at in the surface layer, q is the electronic charge and μ_{FE} is the field effect mobility. The charge in unit area in the surface equals to the charge in unit area induced in the oxide. A change in voltage of field plate, ΔV_G, results in a change in the charge in the surface layer

$$\Delta n_f q d_s \approx C_0 \Delta V_G \tag{6.9}$$

where d_s is the effective thickness of surface layer. Using (6.8) and (6.9) the change in conductance of the surface layer, or equally the change in total conductance of the film can be found

$$\Delta G \approx \Delta G_s = \frac{W d_s \Delta \sigma_s}{L} = \frac{C_0 W}{L} \mu_{FE} \Delta V_G \tag{6.10}$$

where W and L are width and length of the film, respectively. From (6.10) the field effect mobility can be calculated

$$\mu_{FE} = \frac{1}{C_0 (W/L)} \frac{\Delta G}{\Delta V_G}. \tag{6.11}$$

The field effect mobility can also be found using the standard TFT equations [5-8]. The basic characteristics of the TFT and the methods of calculations of field effect mobility are presented in the following section.

6.2.3 Characteristics of Thin-Film Transistors

An inverted-staggered TFT structure with channel length L and channel width W is shown if Fig. 6.3. The typical output characteristics, I_D versus V_{DS}, the transfer characteristics, I_D versus V_{GS} in the saturation region, and logarithmic plot of I_D versus V_{GS} are shown if Figs. 6.4a, b, and c, respectively. At low drain voltages and for

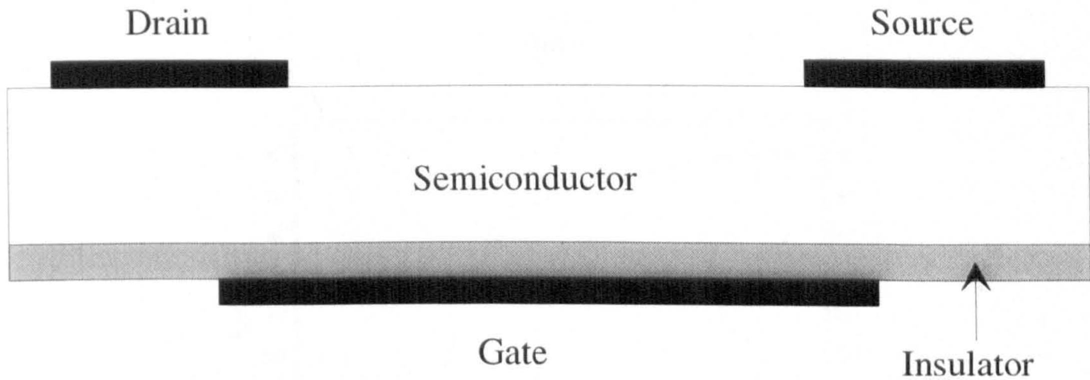
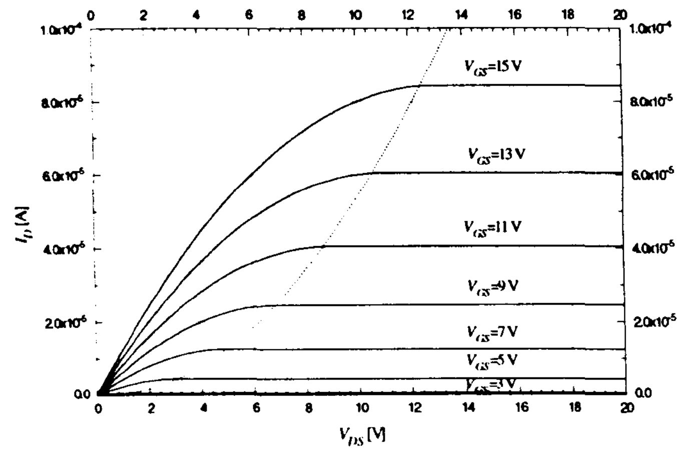


Figure 6.3 A typical inverted-staggered TFT.

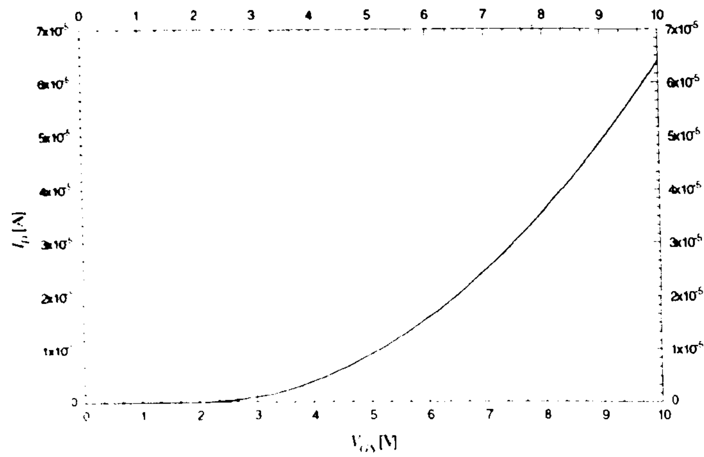
$V_{GS} > V_T$ the drain current can be expressed by [2]

$$I_D = \frac{C_0 W}{L} \mu_{FE} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] = \beta \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{6.12}$$

where



(*a*)



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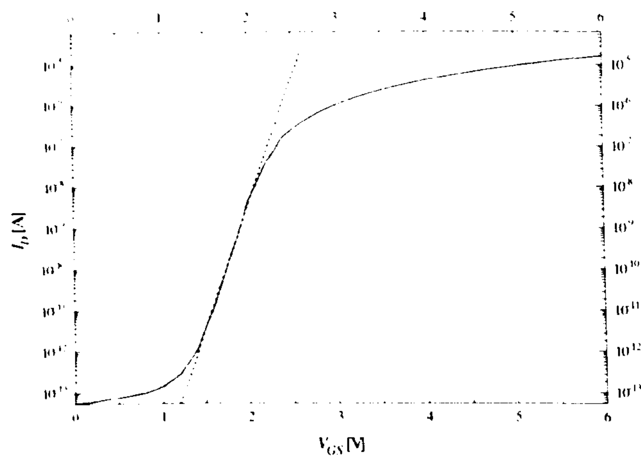


(*c*)

Figure 6.4 (a) Output characteristics, (b) transfer characteristics, and (c) subthreshold plot of a typical TFT.

$$\beta = \frac{C_0 W}{L}\mu_{FE}. \tag{6.13}$$

β is named the device constant and V_T is threshold voltage. For every value of V_{GS}, the drain current reaches a maximum at $V_{DS} = V_{GS} - V_T$. At this point, the channel reaches pinch-off and after that the current remains nearly constant (saturation region).

In the saturation region, the drain current can be expressed as

$$I_{DS} \approx \frac{\beta}{2}(V_{GS} - V_T)^2. \tag{6.14}$$

The transfer characteristics, the variation of I_{DS} versus V_{GS} in this region, is shown in Fig. 6.4b. The slope of transfer characteristics is defined as transconductance g_m.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta(V_{GS} - V_T) = (2\beta I_{DS})^{1/2}. \tag{6.15}$$

At very low drain voltages, the term $V_{DS}^2/2$ in (6.12) is much smaller than $(V_{GS} - V_T)\,V_{DS}$ and can be neglected. The relationship between I_D and V_{DS} in this region is Ohmic.

$$I_D \approx \beta(V_{GS} - V_T)V_{DS}. \tag{6.16}$$

The slope of output characteristics in the Ohmic region or channel conductance is defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \beta(V_{GS} - V_T). \tag{6-17}$$

The transconductance in the Ohmic region equals the derivative of I_D with respect to V_{GS} in (6.16)

$$g_m = \beta V_{DS}. \tag{6.18}$$

The region where the gate voltage is below V_T is called the subthreshold region. The subthreshold swing is an important parameter in TFTs since it describes the change of gate voltage needed to turn the transistor on and off. Low values of S

are obviously desirable. The drain current in this region varies exponentially with V_{GS} [9]. The logarithmic plot of I_D versus V_{GS}, usually called a subthreshold plot, is a straight line (Fig. 6.4c). The subthreshold swing S, by definition, is the inverse slope of the subthreshold plot, or the gate voltage swing needed to change the drain current by one decade.

$$S \equiv \frac{dV_{GS}}{d(\log I_D)} = \frac{dV_{GS}\ln 10}{d(\ln I_D)} = \frac{kT}{q}(1 + C_s/C_{ox})\ln 10 \tag{6.19}$$

where k is Boltzmann constant and T is temperature in Kelvin. The surface capacitance C_s defined in (6.3) is the parallel combination of space charge capacitance and surface states capacitance. The space charge capacitance is defined in (6.1) and equals to [9, 10]

$$C_{sc} = \left(\frac{q\varepsilon_s n_{sc}}{2V_s}\right)^{1/2} = q(\varepsilon_s N_{sc})^{1/2} \tag{6.20}$$

where n_{sc} is the space charge per unit volume and N_{sc} is the space charge density per unit volume per electron volt. The surface states capacitance is defined in (6.2) and can be described as

$$C_{ss} = q^2 N_{ss} \tag{6.21}$$

where N_{ss} is surface states density per unit area per electron volt. Substituting C_{sc}, C_{ss}, and C_{ox} in (6.19) yields to [11]

$$S = \frac{kT}{q}\ln 10 \cdot \left[1 + \frac{qd_{ox}}{\varepsilon_{ox}}\left(\sqrt{\varepsilon_s N_{sc}} + qN_{ss}\right)\right]. \tag{6.22}$$

The subthreshold swing depends on both oxide thickness and the density of surface states. Because of high density of surface states at the interface of a-Si:H and insulator, the subthreshold swing in a-Si:H TFTs is much smaller than that in crystalline silicon MOSFETs. The values of S for a-Si:H TFTs reported in the literature ranges from 0.3 to 2.5 V/decade [11].

Another important parameter in TFTs is the on-off ratio, which is the ratio of the currents associated with the maximum and minimum gate voltage applied to the

transistor. The on-off ratio is usually expressed in orders of magnitude or decades. It should be noticed that when the transistor is turned off by applying a negative voltage, the off-current is usually higher than the minimum current in the TFT.

6.2.4 Derivation of Field Effect Mobility from TFT Characteristics

Many researchers have used the TFT characteristics to calculate the field effect mobility [5-8]. In the saturation region, the drain current is fairly independent of drain-source voltage and can be expressed by Eqn. (6.14). A plot of $(I_D)^{1/2}$ versus V_{GS} would be a straight line whose slope is proportional to $(\mu_{FE})^{1/2}$ and its intercept with the voltage axis equals V_T. The field effect mobility can be found from the slope of this line

$$\mu_{FE} = \frac{2}{C_{ox}(W/L)}\left[\frac{\partial (I_D)^{1/2}}{\partial V_{GS}}\right]^2 . \tag{6.23}$$

In the Ohmic region, the channel conductance can be found from the slope of output characteristics and is given by (6.17). The channel conductance is proportional to V_{GS} and a plot of g_d versus V_{GS} is a straight line. The intercept of this line with the V_{GS} axis equals V_T and the field effect mobility can be found from its slope

$$\mu_{FE} = \frac{1}{C_{ox}(W/L)}\frac{\partial g_d}{\partial V_{GS}} . \tag{6.24}$$

This equation is similar to equation (6.11) in section 6.2.2.

The field effect mobility can also be found from equation (6.18), the transconductance in the Ohmic region [12]

$$\mu_{FE} = \frac{1}{C_{ox}(W/L)}\frac{\partial g_m}{\partial V_{DS}} \approx \frac{1}{C_{ox}(W/L)}\frac{g_m}{V_{DS}} . \tag{6.25}$$

Although most researchers have used the saturation region to calculate the field effect mobility [5-8], the field effect found from the Ohmic region seems to be more reliable, since the transverse field is minimum in this case.

Another method of determining the field effect mobility is by applying an ac signal between the drain and source biased in the Ohmic region. The mobility can be related to the electric field by the drift velocity of electrons

$$v_d = \mu_{fe} E \,. \tag{6.26}$$

For a specimen with length L the drift velocity equals to

$$v_d = L/t_1 \tag{6.27}$$

where t_1 is the time needed for an electron to travel from one side of specimen to the other side. With an ac signal applied between drain and source, and the period of signal less than a critical time T_c corresponding to the frequency f_c, the electrons can not reach the other end and the ac current will drop. By measuring this frequency and using (6.26) and (6.27) the field effect mobility can be estimated

$$\mu_{fe} = f_c \frac{L^2}{2V_m} \tag{6.28}$$

where V_m is the amplitude of ac signal.

6.3 EXPERIMENTAL

The structure used for field effect mobility measurement is shown in Fig. 6.5. A layer of 0.5 μm silicon dioxide was thermally grown on an n-type crystalline silicon substrate. A film of 0.3 μm GD intrinsic a-Si:H was deposited on the oxide layer. Aluminium with thickness of 300 nm was evaporated on the back of crystalline wafer as gate contact. A film of 200 nm aluminium was evaporated on the a-Si:H layer, and drain and source contacts were defined by photo-lithography and lift-off of aluminium. The samples then were annealed for 2 hr at 200 °C [13] in the presence of forming gas. The mask used for defining drain and source contacts contains devices with different drain and source areas and different aspect ratios. The dimensions of drain and source contact areas for the device discussed in this chapter are 1500 μm by 270 μm with separation of 10 μm.

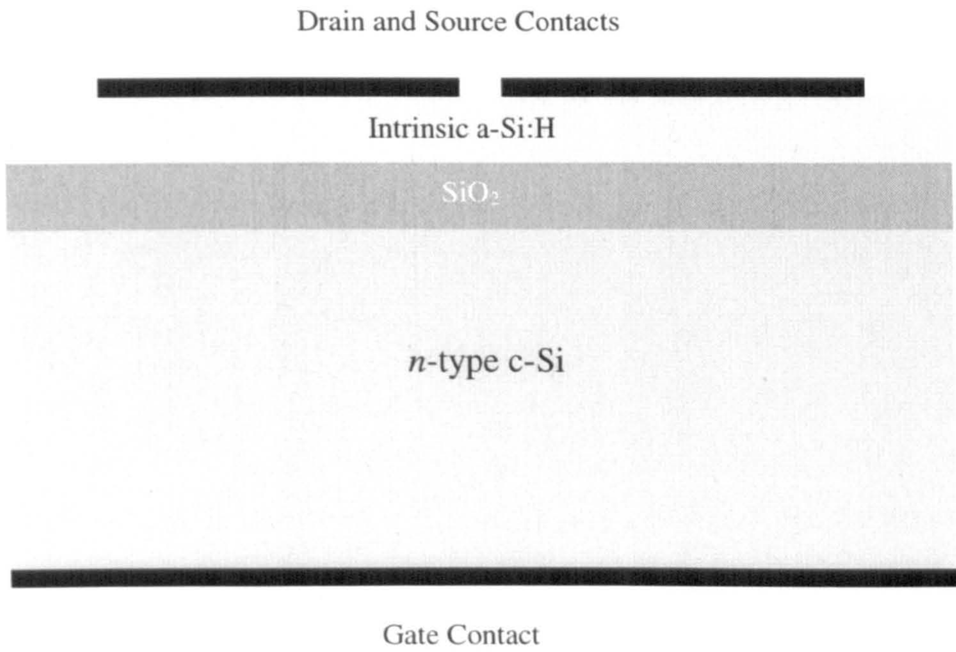


Figure 6.5 The structure used for field effect mobility measurement.

The output and transfer characteristics were measured at room temperature (295 K) using a Keithly 230 programmable voltage sources and a Keithly 617 programmable electrometer controlled by a personal computer.

The set-up for ac measurements is shown in Fig. 6.6. The gate voltage was applied by a Fluke 410B high voltage de power supply, and an ordinary signal generator provided the dc and ac drain voltage. The drain current was calculated by measuring the voltage across resistance R using a Tektronix 2430A digital storage oscilloscope.

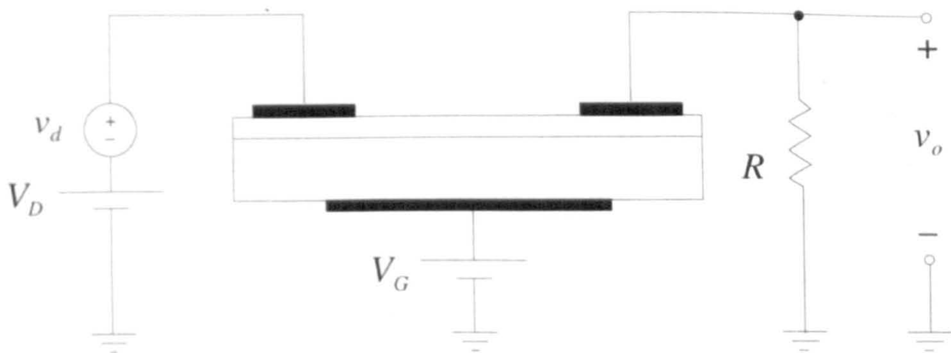


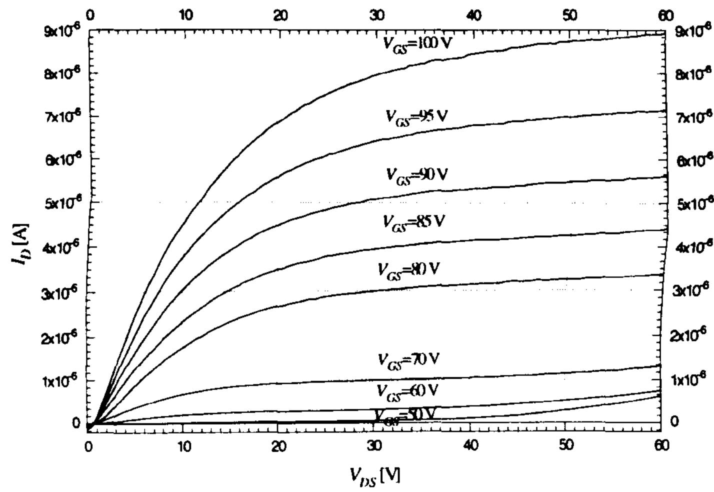
Figure 6.6 The set-up for ac measurement.

6.4 Results and Discussion

The output characteristics of the device for gate voltages of 50 to 100 V are shown in Fig. 6.7a. At V_{DS} less than about 1 V, the current is slightly negative due to oxide leakage. The maximum value of leakage is 1.28×10^{-7} A, which is about two orders of magnitude less than the channel current with the same gate voltage. There is also an offset of about 1 V in V_{DS} that relates to the oxide leakage. The transfer characteristics and the subthreshold plot of the device are shown if Figs. 6.7b and 6.7c, respectively. From Fig. 6.7c, the subthreshold swing was found equal to 18.5 V/decade, and on-off ratio is just more than two decades. The low on-off ratio could be due to oxide leakage. However, the on current is also low, possibly because of the Schottky barriers at drain and source contacts. The subthreshold swing is much higher than the published values of 0.3 to 1.5 V/decade [11]. Deane and Powell have claimed that the transfer characteristics of an a-Si:H TFT depend mainly on the fixed charge at the interface with the gate insulator [14]. Ignoring the space charge, the value of 1.36×10^{13} cm^{-2} eV^{-1} can be found for the surface states density from (6.22). This value is more than the maximum value of surface density of states reported [11] by at least a factor of two. If the space charge is taken into account, the density of surface states would be smaller than the value calculated. The high value of sub-threshold swing can also be related to the low on current.

6.4.1 Calculation of Field Effect Mobility

The plot of channel conductance g_d versus V_{GS} is shown in Fig. 6.8. The data points above the threshold voltage point lie on a straight line. The threshold voltage and the maximum value of field effect mobility can be found using (6.24) from the intercept of this line with V_{GS} axis and its slope, respectively. The threshold voltage is equal to 68 V and the maximum value of field effect mobility equals to 1.77×10^{-2} $cm^2V^{-1}s^{-1}$. The field effect mobility is a function of the gate voltage and can be calculated for each gate voltage using (6.11) or (6.24). The variation of field effect mobility versus V_{GS} is shown in Fig. 6.9. The field effect mobility increases with V_{GS} and then saturates to a maximum value.



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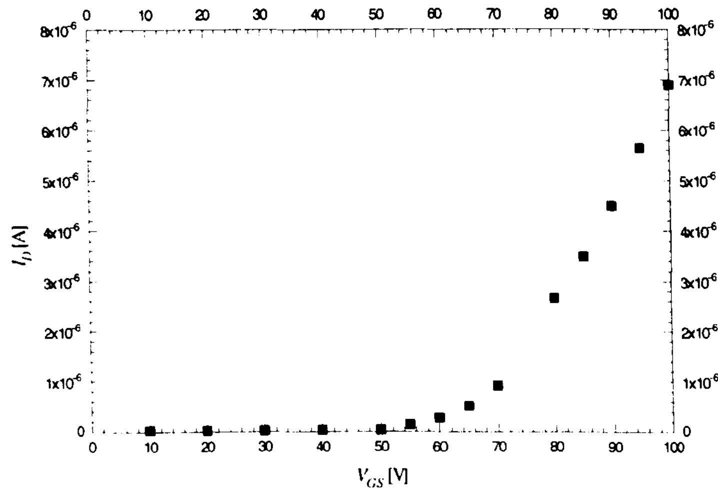

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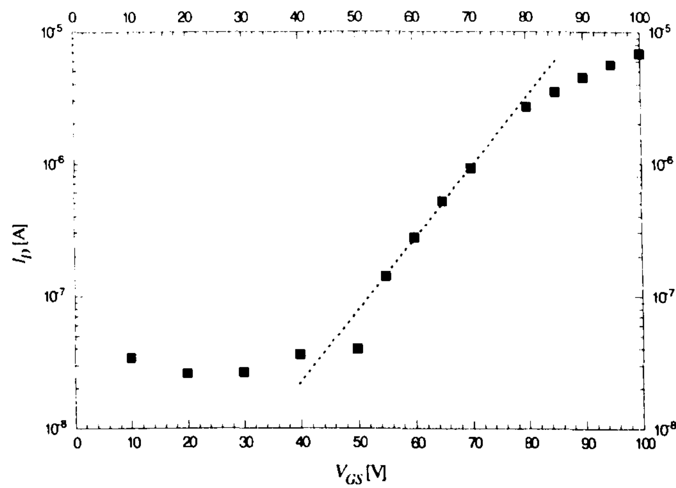

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***Figure 6.7** (a) Output characteristics, (b) transfer characteristics, and (c) subthreshold plot of the device.*

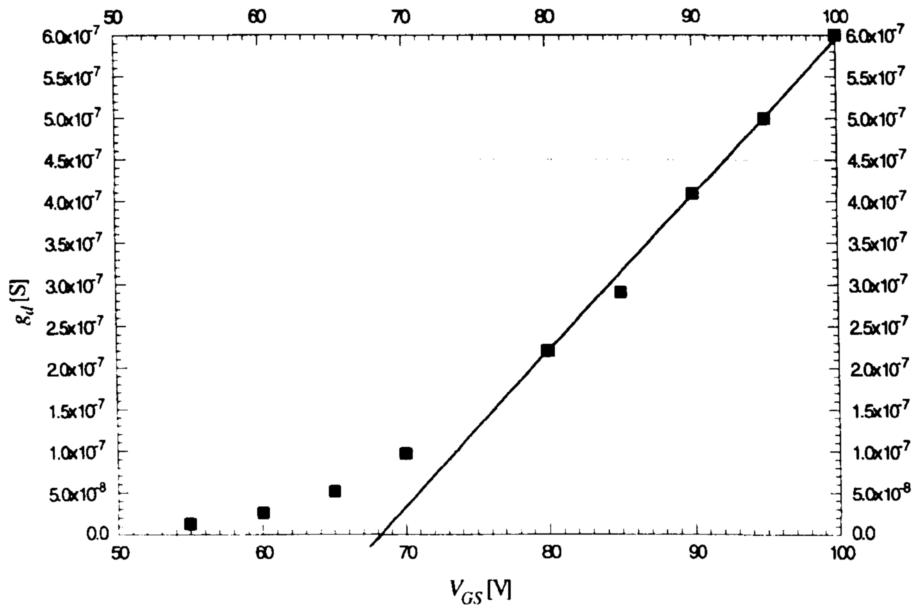

Figure 6.8 The channel conductance versus V_{GS}.

Some authors have derived relationships between field effect mobility and the bulk extended states mobility. The field effect mobility can be defined as the extended states mobility, μ_0, times the ratio of free charge to the total induced charge in the channel [2, 11, 15]

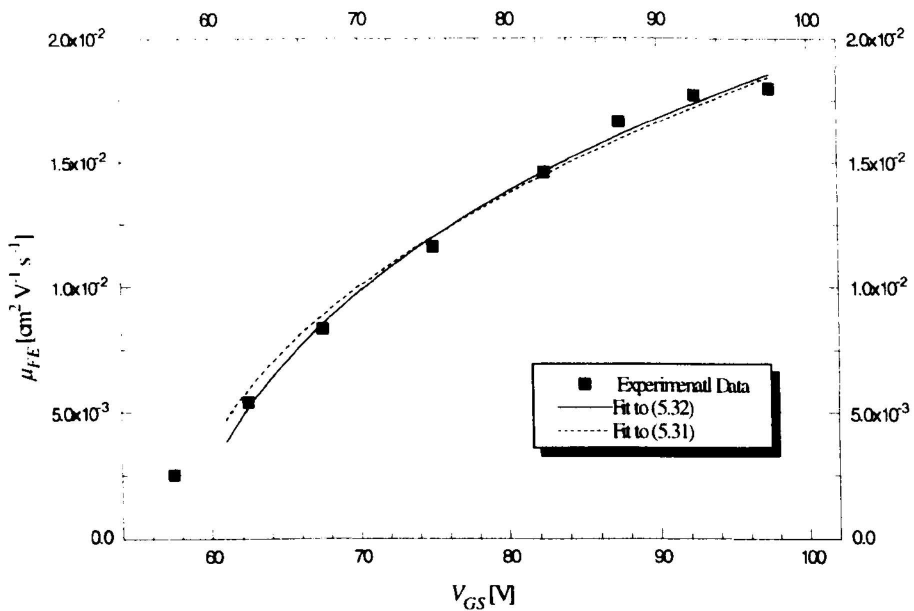

Figure 6.9 The variation of field effect mobility versus V_{GS} (square dots). The fit curve to Eqns. (6.31) and (6.32) are shown by dashed and solid lines, respectively.

$$\mu_{FE} = \mu_0 \frac{qn_s}{Q_{\text{ind}}}. \tag{6.29}$$

qn_s is the free charge per unit area and the total induce charge can be expressed as

$$Q_{\text{ind}} = C_{\text{ox}}(V_{GS} - V_{FB}) \tag{6.30}$$

where V_{FB} is the flat band voltage. In crystalline silicon, the field effect mobility decreases by increasing V_{GS} [9]. In a-Si:H, μ_{FE} increases by increasing V_{GS} as the induced charge fills the trap states and a larger fraction of this charge resides in the conduction band and is mobile. The field effect mobility can be expressed by the Shur-Hack approximation as [16, 17]

$$\mu_{FE} = \mu_0 K (V_{GS} - V_T)^{1/2} \tag{6.31}$$

where K is a fitting parameter. Lee *et al.* [18] and Shur *et al.* [19] have presented another relationship for field effect mobility as

$$\frac{1}{\mu_{FE}} = \frac{1}{\mu_0} + \frac{1}{K_\mu |V_{GTE}|^m} \tag{6.32}$$

where $V_{GTE} \approx V_{GS} - V_T$ for $V_{GS} > V_T$ and $V_{GTE} \approx 2kT/q$ for $V_{GS} > V_T$, and K_μ and m are constant fitting parameters. For low values of gate voltage, the field effect mobility is approximately proportional to $|V_{GTE}|^m$, while for large gate voltage μ_0 dominates and μ_{FE} saturates to the extended states mobility. One should notice that at low gate voltage, with $m = ½$, Eqn. (6.32) is the same as Eqn. (6.31).

The curves fitted to Eqns. (6.31) (dashed line) and (6.32) (solid line) are shown in Fig. 6.9. It can be seen that both curves fit well with experimental data (square dots). The fitting parameters from (6.31) are $V_T = 58.5$ V and $\mu_0 K = 2.95 \times 10^{-3}$ $\text{cm}^2 \text{V}^{-1/2} \text{s}^{-1}$. From (6.32) $V_T = 58.7$ V, $\mu_0 = 6.3\times10^{-2}$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, $K_\mu = 2.3\times10^{-3}$, and $m = 0.66$ was found. The threshold voltages found from both equations are very close and are about 10 V less than that obtained from g_d plot. The value of μ_0 is much lower than the typical values given in the literature and it seems that there exists a current limiting process.

A plot of $I_D^{1/2}$ versus V_{GS} in the saturation region is shown in Fig. 6.10. The data points above the threshold voltage lie on a straight line that meets the horizontal axis at V_T = 48 V. This value is about 20 V less than that found from g_d plot. The field effect mobility found from the slope of this line, using (6.23), equals to 4.71×10^{-3} cm^{2}V^{-1}s^{-1} which is, with a factor of about 4, smaller than the value obtained from g_d plot.

The drain current in the Ohmic region is proportional to V_{DS} and $V_{GS} - V_T$. The channel conductance, g_m, therefore, should be proportional to V_{DS} as shown if Eqn. (6.18). The field effect mobility can be calculated from the plot of g_m in the Ohmic region versus V_{DS} using (6.25). The transconductance is calculated by measuring the slope of transfer characteristics above threshold for different values of V_{DS}. A plot of g_m versus V_{DS} is shown in Fig. 6.11. The data points lie on a straight line passing from the origin for low values of V_{DS}, and then the slope decreases for higher values of V_{DS}. The data points deviate from straight line at very low drain voltages due to the effect of oxide leakage. At very low values of V_{DS}, the oxide leakage current is comparable to the channel current and therefore can affect the total current. The field effect mobility calculated from the slope of the curve using Eqn. (6.25) equals to

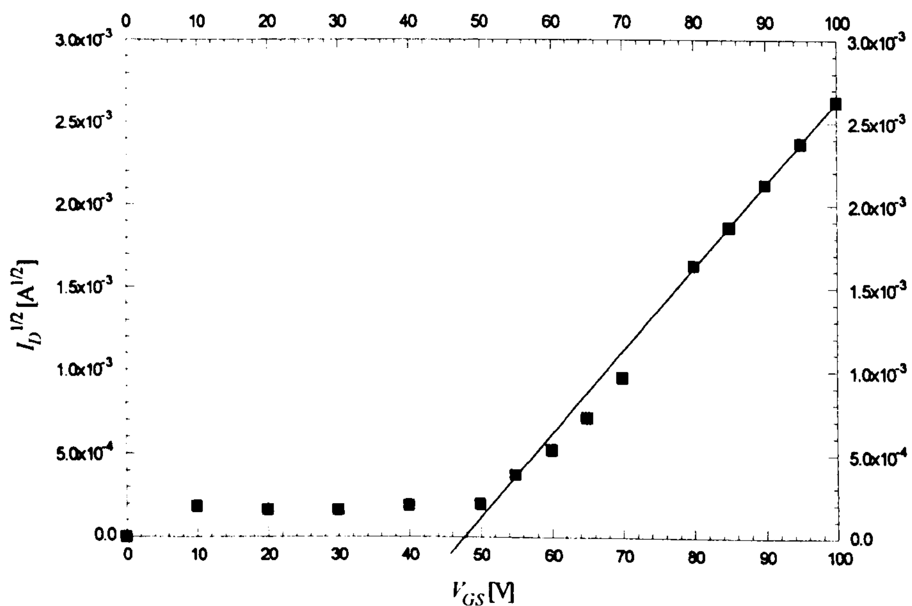

Figure 6.10 The variation of $I_D^{1/2}$ versus V_{GS}.

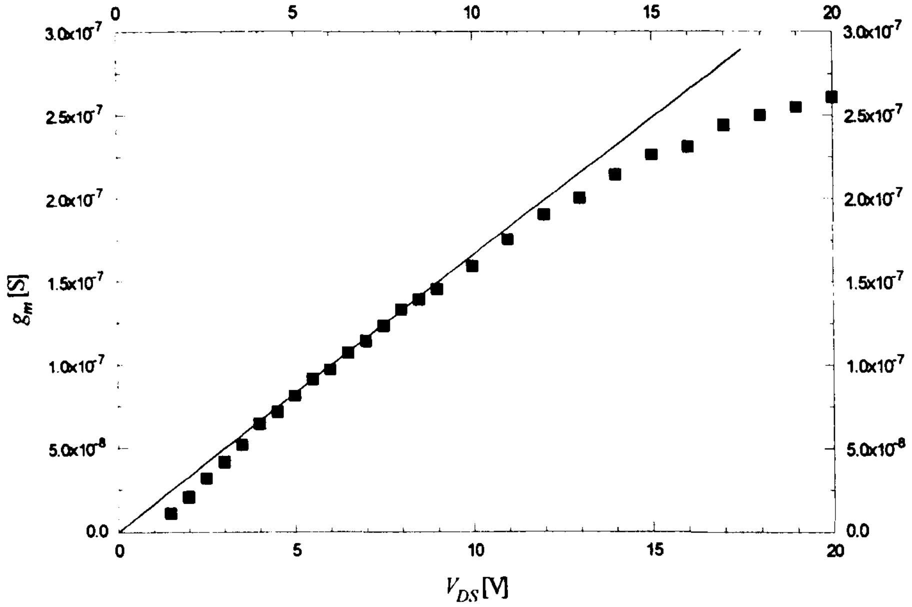

Figure 6.11 The variation of g_m versus V_{DS} in the Ohmic region.

1.57×10^{-2} cm^{2}V^{-1}s^{-1}, which is close to the value calculated from the g_d plot.

6.4.2 AC Measurement Results

The ac drain current versus frequency is shown in Fig. 6.12. The gate voltage is 100 V, and an ac voltage with amplitude of 0.5 V with a dc offset of 3V is applied between drain and ground (Fig. 6.6). The series resistor R is 100 kΩ. The frequency

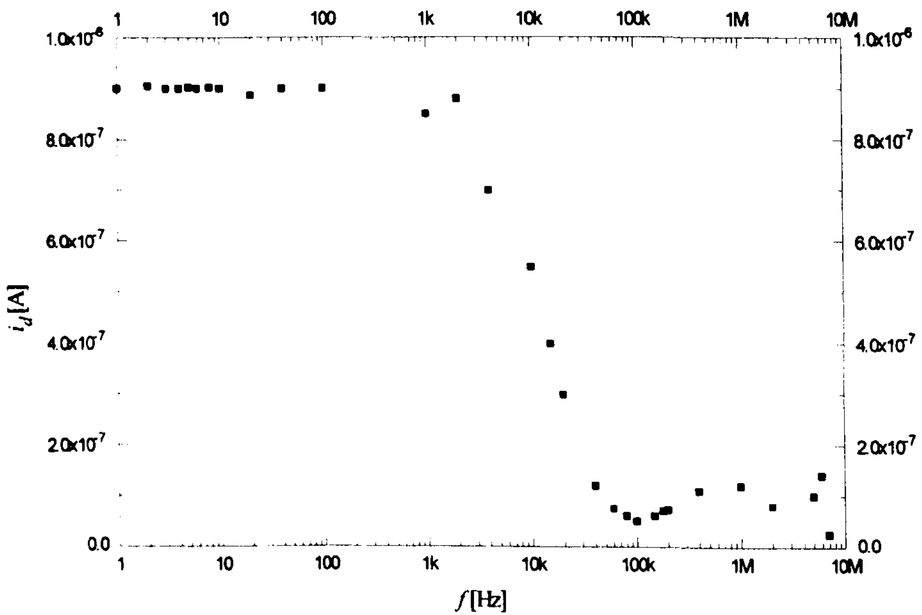

Figure 6.12 The variation of ac drain current with frequency.

response has a cut-off frequency of 6 kHz and the current reaches the minimum level at a frequency of about 100 kHz. Applying the cut-off frequency to Eqn. (6.28), the mobility of $\mu_{fe} = 6\times10^{-3}\ cm^2V^{-1}s^{-1}$ is calculated.

6.5 CONCLUSION

The field effect mobility was measured using a simple device similar to the inverted-staggered TFT. The methods of calculating field effect mobility in the Ohmic and saturation regions were explained, and the field effect mobility of electrons was measured using different methods. The sample has a very low on-off ratio and high subthreshold swing that could be due to the low on-current. It is concluded that the Schottky contacts at drain and source are responsible for the low current.

The calculated values of field effect mobility range from 4.71×10^{-3} to $1.77\times10^{-2}\ cm^2V^{-1}s^{-1}$. The field effect mobility increases with the gate voltage towards the extended states bulk mobility.

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CHAPTER SEVEN

MODELLING OF A HYDROGENATED AMORPHOUS SILICON VERTICAL THIN-FILM TRANSISTOR

7.1 INTRODUCTION

There has been a great interest in fabrication of vertical a-Si:H thin-film transistors (VTFT) [1-4]. The operating speed of a TFT is proportional to mobility and channel length. As a-Si:H suffers from low mobility, an alternative to increase the speed of operation is reduction of channel length. In the conventional planar structures, reducing the channel length is limited by the alignment error in the lithography process. The vertical TFT allows submicron performance without the need for critical lithography.

Computer modelling provides an understanding about the performance of the device to optimize the TFT prior to fabrication. In the present work, the two-dimensional device simulation package, Medici, has been used to model a vertical TFT structure.

The structure and simulation set up is described in the next section. The device was simulated without traps and by application of different sets of traps, based on the experimental results of SCLC measurements. The influence of density and energy level of different traps are studied. The effect of various physical dimensions of device, such as channel length, thickness of oxide, etc., and the type of metal used for drain and source on the performance of the TFT is investigated.

7.2 THE STRUCTURE

The vertical TFT structure used for simulation is shown in Fig. 7.1. The actual TFT can be made on glass substrate using the following process steps. A thick layer of aluminium is evaporated onto the glass substrate and the gate area can be defined by patterning the aluminium layer and by lift-off or etching the unwanted area. The oxide layer then is grown using aluminium anodization or plasma oxidation of aluminium. The drain and source contact areas are made by shadow evaporation that ensures the presence of a gap between drain and gate oxide. Chromium is a good choice for drain and source contact, since it provides the best contact with intrinsic a-Si:H [5]. Finally, the a-Si:H is deposited over the whole surface. Access to drain and source contacts can be made by lift-off or etching the a-Si:H using a second mask.

The dimensions of the device are given in Table 7.1. As Medici is a two-

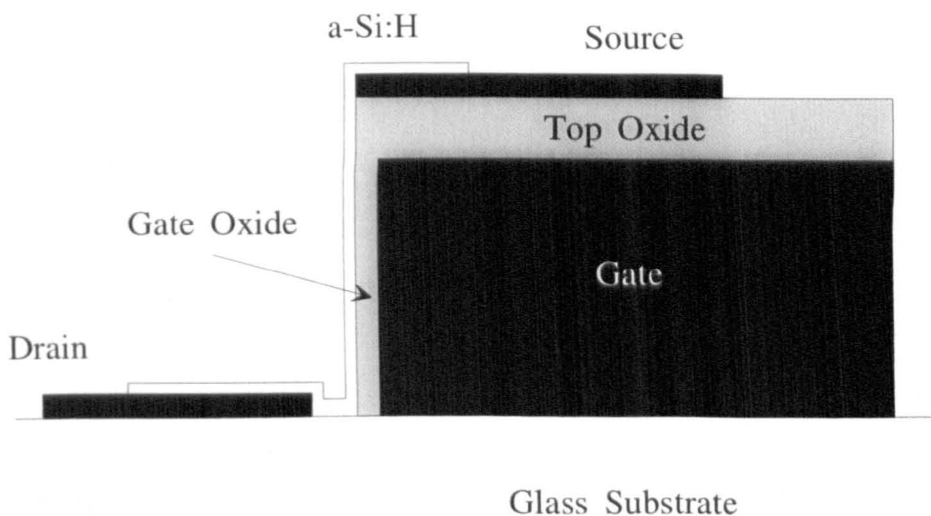


Figure 7.1 The vertical TFT structure used for simulation.

dimensional simulation package, all calculations are made per unit depth. The parameters of a-Si:H are the same as those given in Table 3.1, except for mobility the values of 0.1 and 0.01 $cm^2V^{-1}s^{-1}$ are used for electron and hole mobility, respectively. All the simulations are performed at 300 K, and the effect of different parameters such as channel length, thickness of oxide, metal work function, and the density and energy level of traps on the characteristics of device is considered.

t_{Gate}	Thickness of gate metal	5 μm
w_{Gate}	Width of gate metal	5 μm
L	Channel length = t_{Gate}	5 μm
t_{gox}	Thickness of gate oxide	0.1 μm
t_{tox}	Thickness of top oxide	0.5 μm
$t_{a\text{-}Si:H}$	Thickness of a-Si:H layer	0.15 μm
$t_{D/S}$	Thickness of drain or source contacts	0.05 μm
$w_{D/S}$	Width of drain or source contacts	5 μm
s	Gap space between drain and gate oxide	0.1 μm

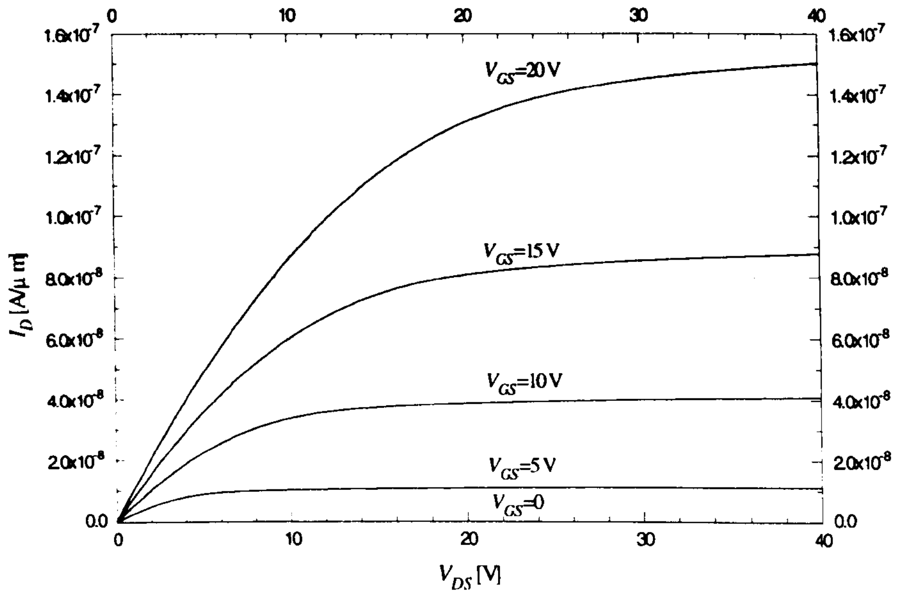
Table 7.1 The dimensions of device used for simulation.

7.3 SIMULATION RESULTS

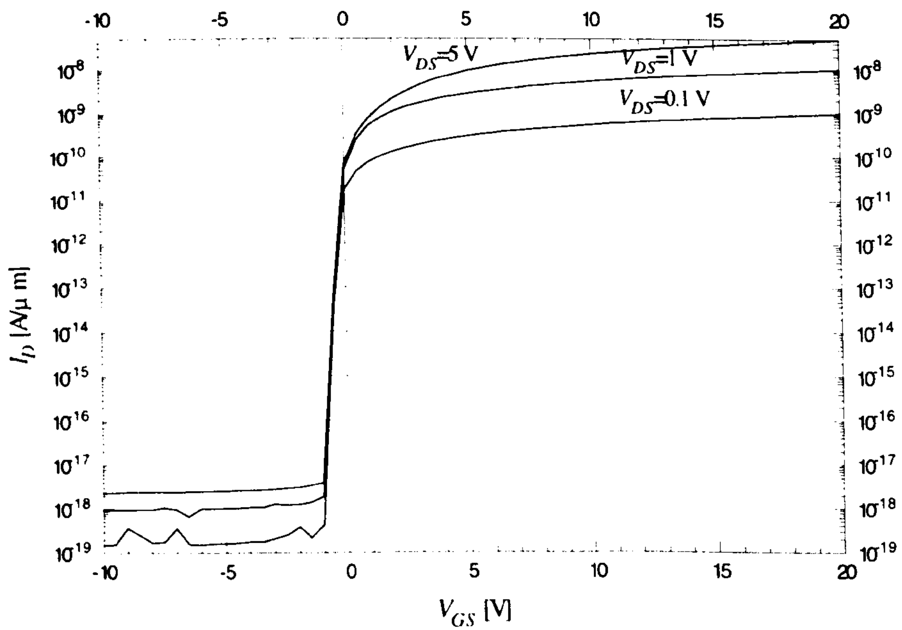
In the first step, the device without traps in the a-Si:H was simulated. Aluminium was used for drain and source contacts. As the work function of aluminium is close to the electron affinity of a-Si:H, without the presence of surface states, the contact between aluminium and intrinsic a-Si:H is non-rectifying. This makes it possible to model the device with Ohmic contacts without any need for n^+ layers.

7.3.1 The Device with Trap-Free a-Si:H

The output characteristics and the subthreshold plots of the device are shown in Figs. 7.2a and b respectively. Prior to application of any voltages, electrons are injected from the drain and source contacts, and due to the very large Debye length in intrinsic a-Si:H without traps, are accumulated in the whole of the semiconductor.



(a)



(b)

Figure 7.2 (a) The output characteristics and (b) the subthreshold plots for the device without traps.

Therefore, as it can be seen in the subthreshold plots, at zero gate voltage the semiconductor is very conductive and the transistor is on. By applying a positive gate voltage, more electrons are induced in the semiconductor, in the region close to the gate, resulting in an increase in drain current. However, since the concentration of

free electrons in the semiconductor is comparable to the induced electron concentration, the change in drain current is not huge. When a negative voltage is applied to the gate, the semiconductor is depleted of electrons and its conductivity decreases significantly. The device has a negative threshold voltage equal to – 0.3 V, calculated from the $I_D^{1/2}$ versus V_{GS} curve in the saturation region [6-9].

The device has an on-off ratio about ten orders of magnitude and a subthreshold swing of 0.1 V/decade. As there are no surface states defined in the model, the surface charge consists of only space charge. From Eqn. (6.19), the ratio of space charge capacitance to oxide capacitance equals to 0.67, and using (6.20) the average concentration of electrons making up the space charge is about 6×10^{15} cm^{-3}. This is consistent with the free electron concentration calculated from the drain current for zero gate voltage. The reason for the low off-current is that the a-Si:H layer is very thin, and therefore, a fairly small negative gate voltage can repel the free electrons from the entire semiconductor. The subthreshold plots for a very thick semiconductor layer (few microns) are shown in Fig. 7.3. In this case, the off-current is about 9 orders of magnitude higher than the case with thin film of a-Si:H, because the gate voltage is not sufficient to repel the free electrons from whole the semiconductor.

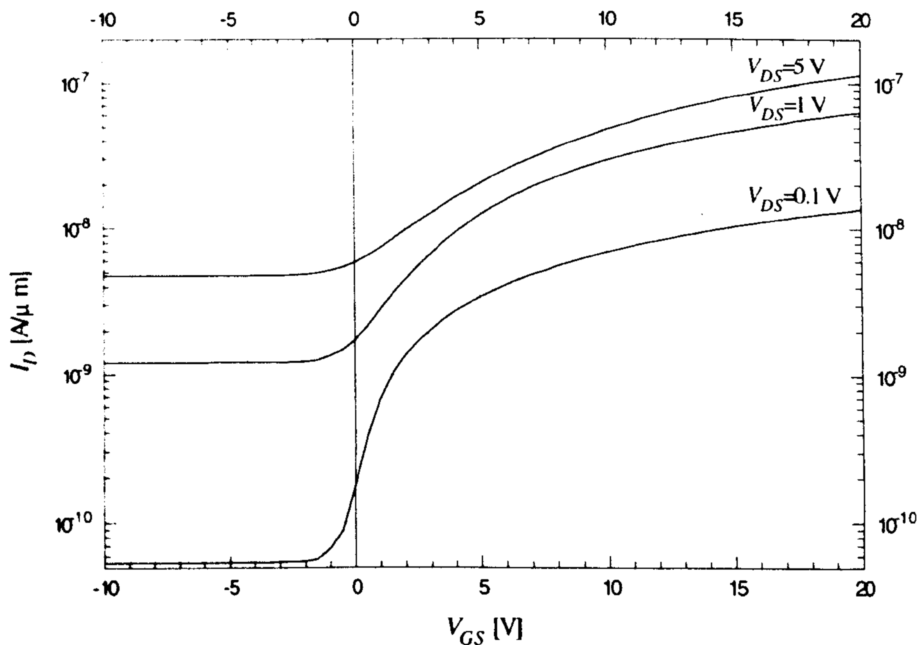


Figure 7.3 The subthreshold plots for the device without traps and very thick a-Si:H layer.

Consequently, the threshold voltage is much lower (–5 V) and the subthreshold swing has increased significantly.

7.3.2 The Effect of Traps

To examine the effect of traps on the behaviour of device, different trap sets were applied to a-Si:H. To preserve the symmetry of states in the mobility gap, for each electron trap set above midgap, a trap with the same density and relative energy level was set in the lower half of the mobility gap. In the first stage, a trap with density of 1×10^{13} cm^{-3} was set in the middle of the bandgap. Next, another trap with density of 1×10^{15} cm^{-3} was set at 0.6 eV below the conduction band. This is the first trap derived from the SCLC measurements discussed in chapter 4. Then, three other traps with density of 4×10^{13}, 1.5×10^{14}, and 6×10^{14} cm^{-3} were added at energy levels of 0.05, 0.1, and 0.15 eV above midgap, respectively. These traps provide a density of state with exponential growth in the middle of bandgap. The distribution of these traps, called trap set 1, is shown in Fig. 7.4.

None of the simulation results of all these stages were significantly different to the trap-free case. The only effect of these traps is the increase of off-current by

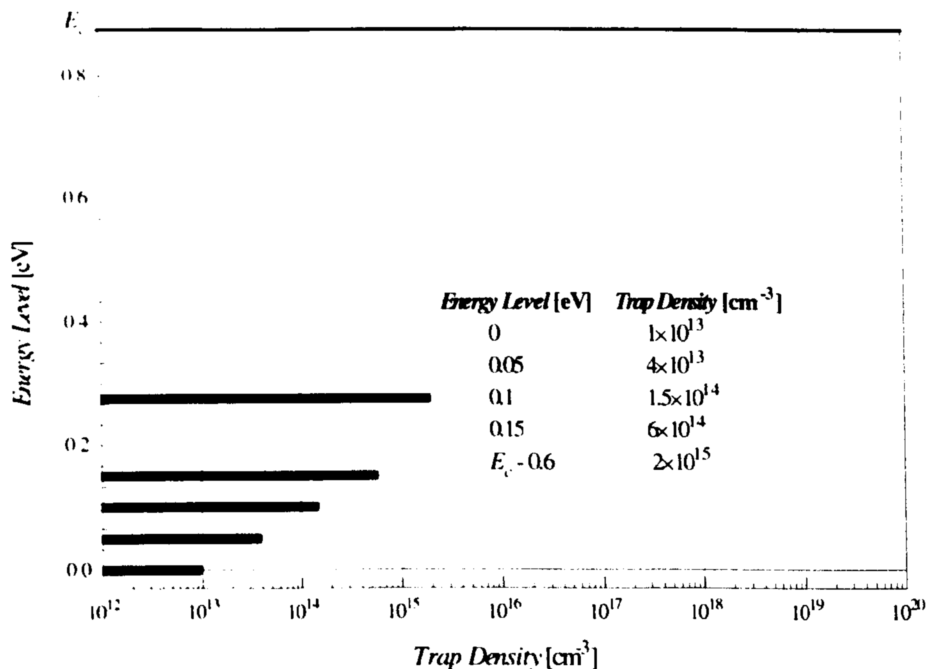


Figure 7.4 The distribution of traps in trap set 1.

less than one order of magnitude. This increase can be explained by the effect of trapped electrons. Some of the injected electrons from drain and source fill the traps. However, due to the low density of traps, the concentration of free electrons is much more than the total concentration of trapped electrons, assuming that all traps are filled. When a positive voltage is applied to the gate, the concentration of free electrons increases due to induced free electrons, and the situation is similar to the trap-free case. With negative voltage applied to the gate, both free and trapped electrons are repelled from semiconductor. The presence of traps causes the Fermi level to be in higher energy level compared to the trap-free case, resulting in the higher free electron concentration and higher conductivity.

In trap set 2, another trap with density of 2.18×10^{16} cm^{-3} is added to the trap set 1 (Fig. 7.5). This is the second trap derived from the SCLC measurements in chapter 4. The subthreshold plot of the device with trap set 2 in a-Si:H for V_{DS} = 5 V is shown by solid line in Fig. 7.6. The trap-free case is also given by the dotted line in the figure for comparison. With this set of traps the on-current has decreased slightly, and the subthreshold swing has increased to 0.28 V/decade. The threshold voltage has also increased to about 0.7 V. Since most of the injected electrons are captured

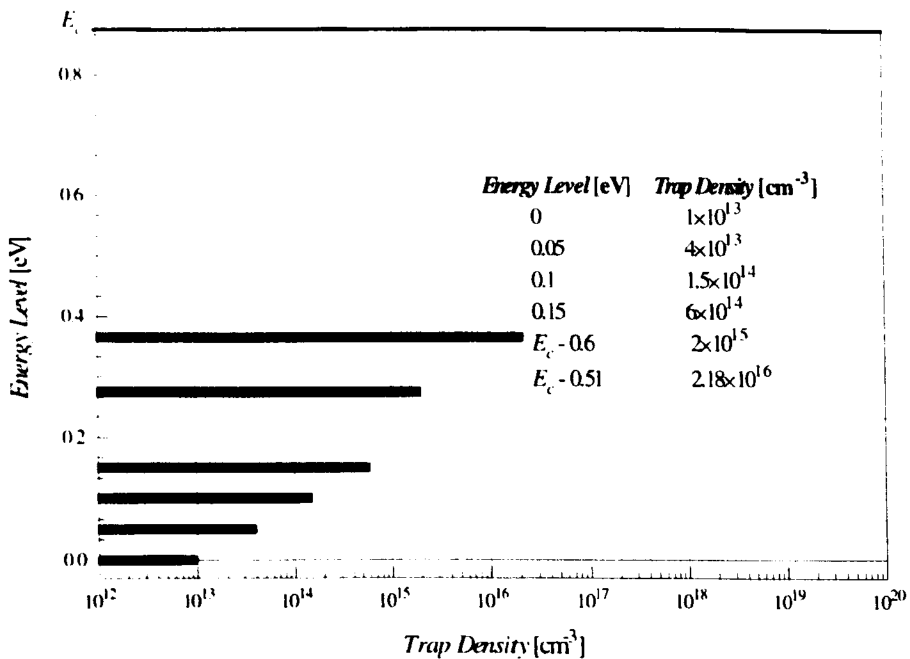


Figure 7.5 The distribution of traps in trap set 2.

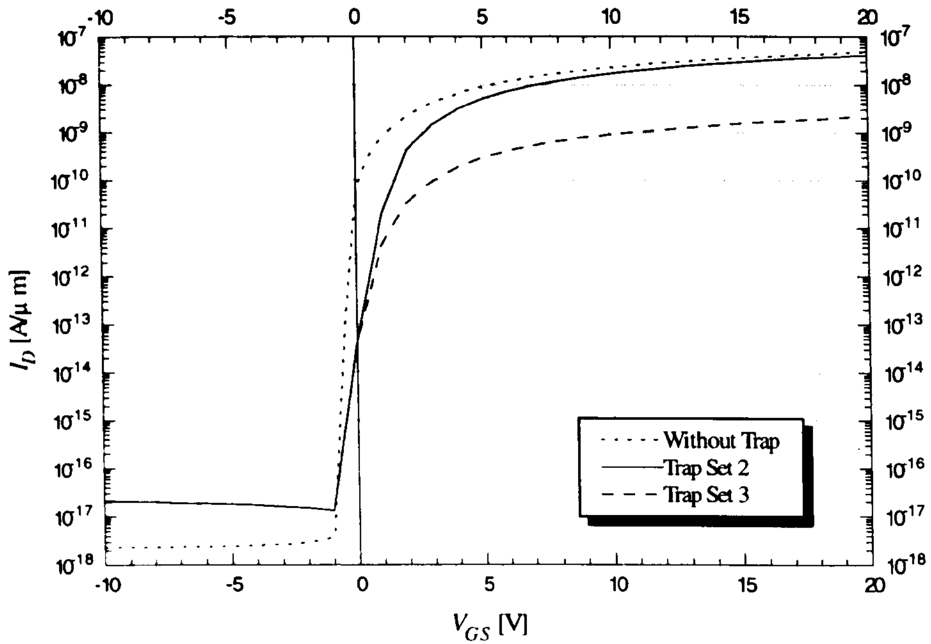


Figure 7.6 The subthreshold plots for trap set 2 (solid line), trap set 3 (dashed line), and trap-free case (dotted line).

by traps, the drain current at zero gate voltage has dropped by about three orders of magnitude comparing to the trap-free case. It means that the concentration of free electrons has reduced by the same order. A fraction of electrons induced by application of positive gate voltage fills the traps and the remaining produce the channel. Therefore, the subthreshold swing and threshold voltage have increased and the on-current has reduced slightly.

To investigate the effect of traps at higher energy levels, in trap set 3, another trap with density of 2×10^{20} cm^{-3} and at the energy level of 0.15 eV is added to trap set 2 (Fig. 7.7). The subthreshold plot associated with this trap set for V_{DS} = 5 V is shown by dashed line in Fig. 7.6. At low gate voltages, since the concentration of electrons captured by the high energy trap is very low, this trap is virtually empty and does not affect the current. Therefore, the characteristics at low gate voltages have not changed significantly compared to the plot associated with trap set 2. At high gate voltages, however, the lower traps are full and the high energy trap is effective. Due to the high density of this trap, many of the induced electrons have been captured by trap states, resulting in the reduction of free electron concentration and consequently decrease in drain current.

In the next stage, in trap set 4, three other traps with density of 1×10^{20} cm^{-3}, 1×10^{21} cm^{-3}, 1×10^{22} cm^{-3}, are added at energy levels of 0.1, 0.05, and 0.01 eV below the conduction band, respectively (Fig. 7.8). These traps make an exponential

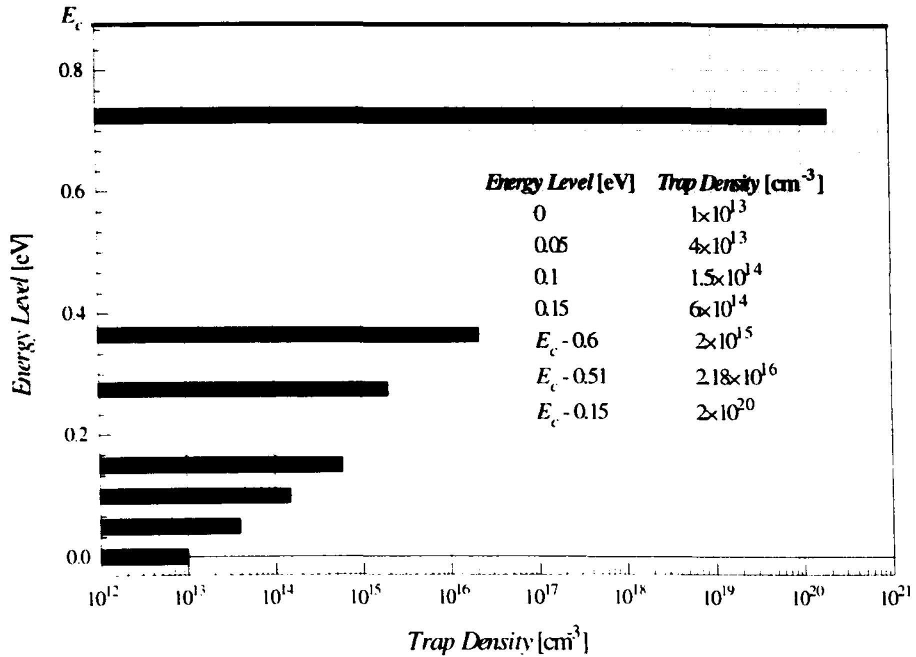


Figure 7.7 The distribution of traps in trap set 3.

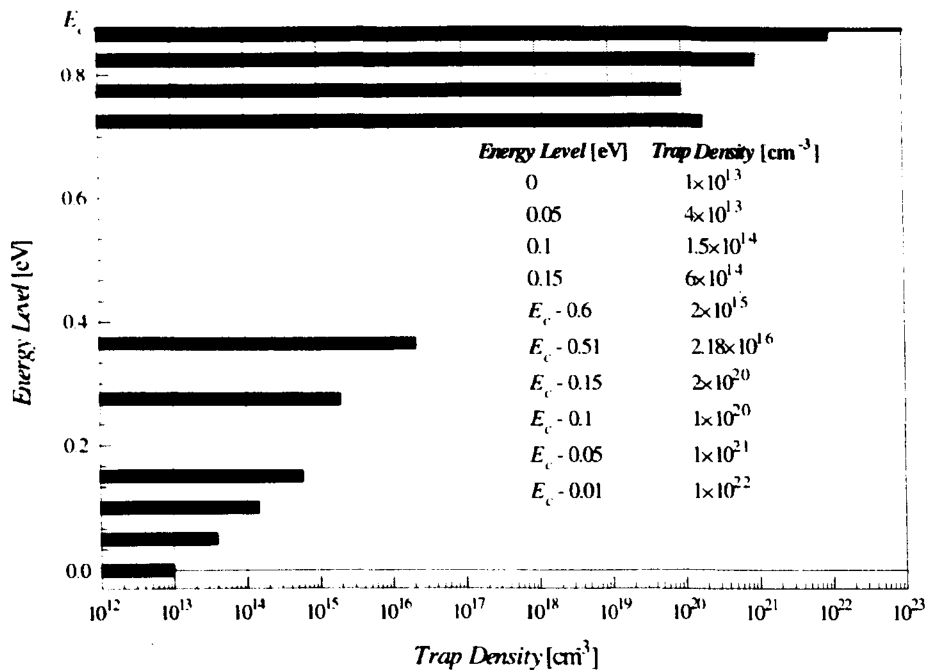


Figure 7.8 The distribution of traps in trap set 4.

distribution that can be a model for the band tail in a-Si:H. The simulation result does not have a significant change compared to the results of trap set 3. This is because of the presence of a trap with very high density just below these traps. A simple calculation shows that the concentration of electrons in the three higher traps is less than 40 percent of the electron concentration in the trap below them. Therefore, the presence of higher traps does not have a significant effect on the device characteristics. The trapped electrons are distributed among the trap states at different energy levels, and the four higher traps behave virtually like a single trap level. With usual gate voltages, it would be very difficult, if not impossible, to move the Fermi level above the band tail, in the extended states. This suggests that the band tail can be modelled by a single discrete trap in the middle of tail.

Trap set 5, shown in Fig. 7.9, was another trap set used in the simulation. This trap set is similar to trap set 4, but the density of lower energy traps has increased to provide a distribution with an exponential decay. The subthreshold plot associated with this trap set is shown if Fig. 7.10 by the solid line. The plots related to the trap-free case and trap set 4 are shown for comparison by the dotted line and dashed line, respectively. The main difference that can be seen is the increase of threshold voltage

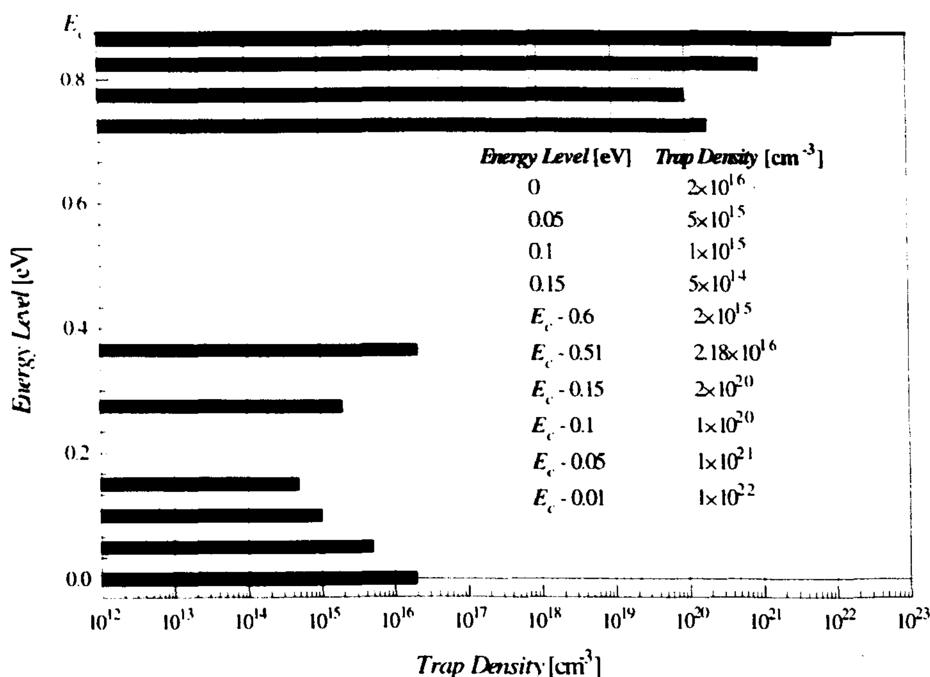


Figure 7.9 The distribution of traps in trap set 5.

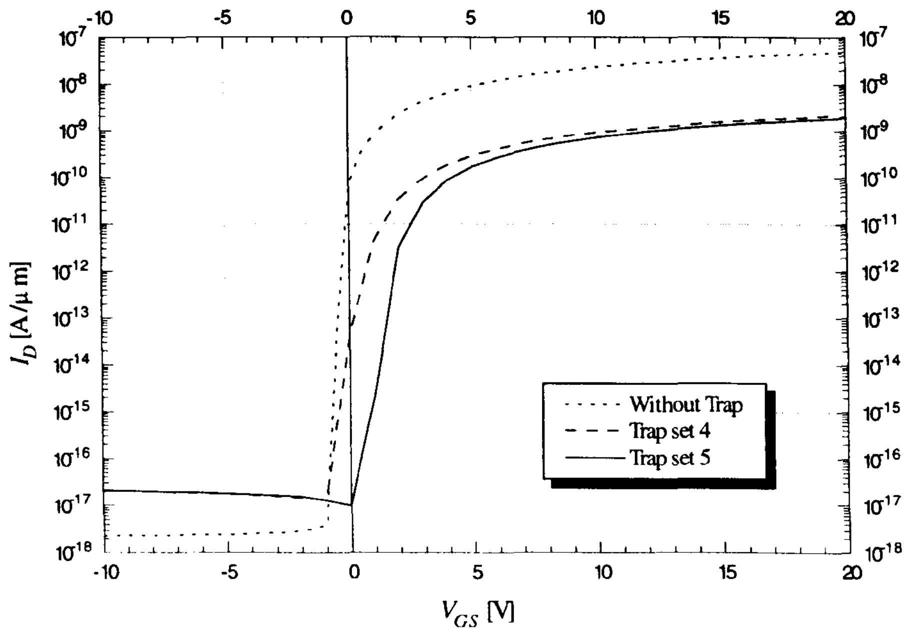


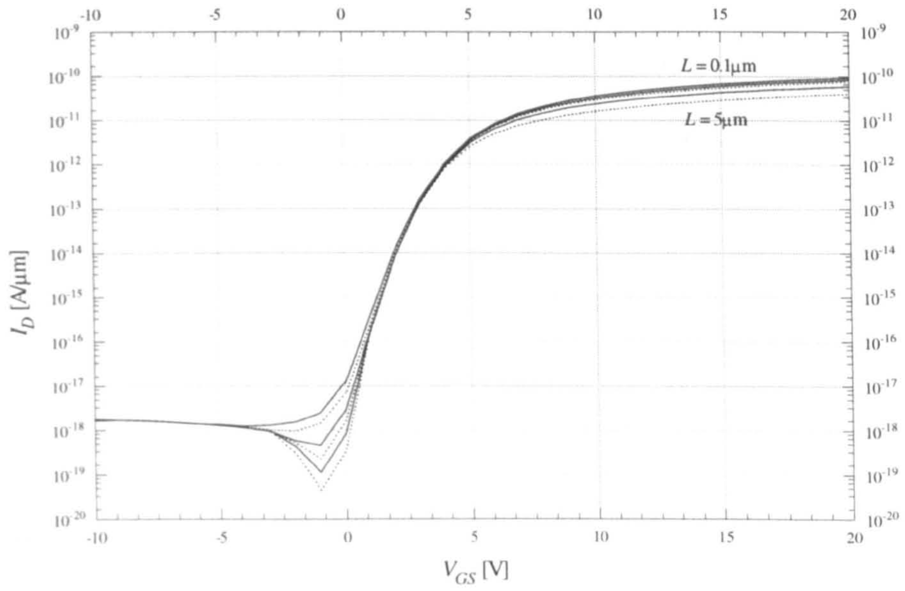
Figure 7.10 The subthreshold plots for trap set 5 (solid line), trap set 4 (dashed line), and trap-free case (dotted line).

to 1.5 V. The subthreshold swing has also increased to 0.36 V/decade. Because of the high density of traps in the middle of the bandgap, the trap states are not completely filled by electrons and the Fermi level is close to the midgap. At low positive gate voltage, the induced electrons are captured by empty states in traps. Therefore, the concentration of free electrons does not change significantly and the drain current is very low. By increasing the gate voltage, the Fermi level moves more slowly towards the conduction band, compared to the case of trap set 4, resulting in a higher sub-threshold swing. The increase of trap density in the middle of bandgap does not have a significant effect on drain current at high gate voltages. The midband trap states are full and only the higher energy traps are effective in this situation.

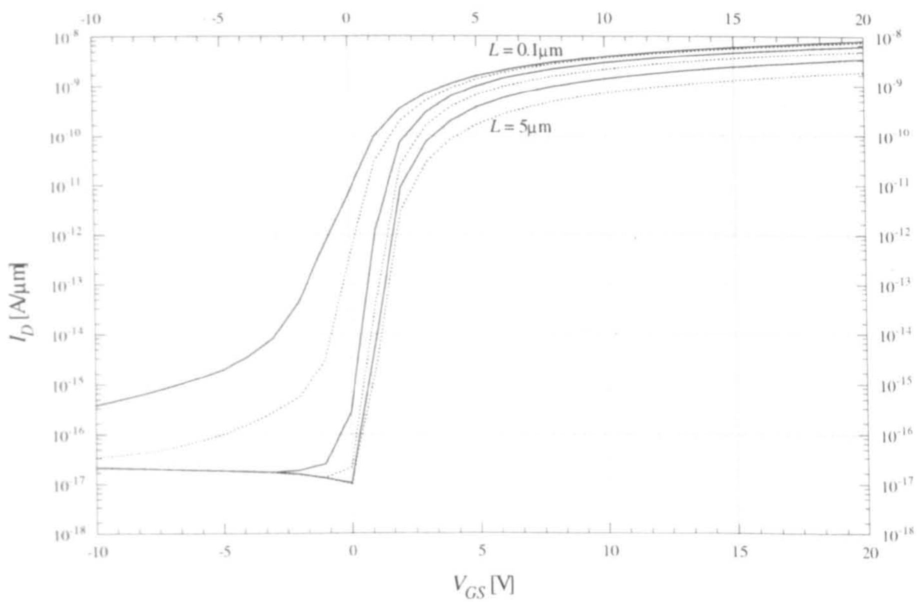
For the other simulations in this chapter, trap set 5 is assumed in the a-Si:H.

7.3.3 Variation with Channel Length

The channel length was varied between 5 and 0.1 μm with values of 0.1, 0.2, 0.5, 1, 2, and 5μm. the subthreshold plots of the device are shown if Figs. 7.11a and b, for V_{DS} = 0.1 and 5 V, respectively. For V_{DS} = 5 V, the short channel effect [10] can be observed, especially for channel lengths less than 0.5 μm. The short channel effect occurs with short channels and high drain voltage, when the longitudinal field is



(a)



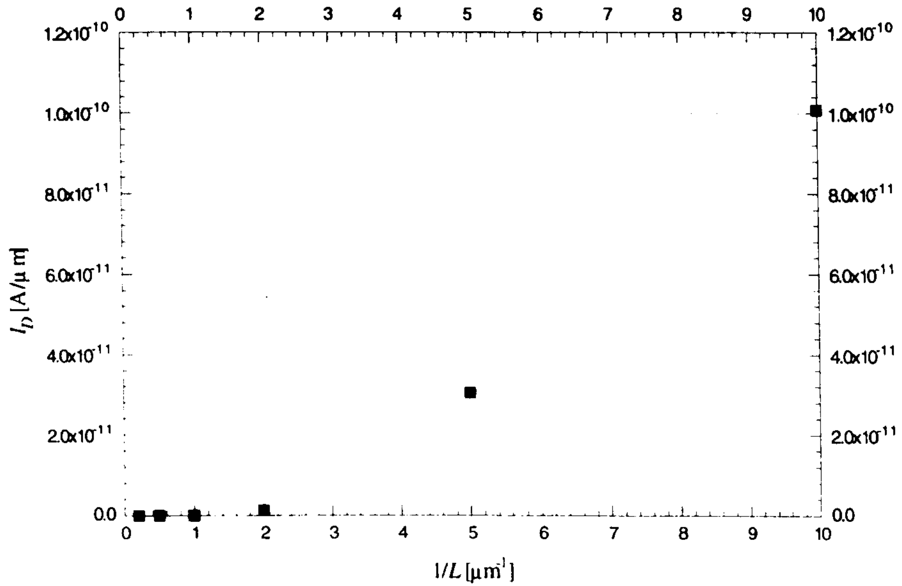
(b)

Figure 7.11 Variation of subthreshold characteristics with channel length (L = 0.1, 0.2, 0.5, 1, 2, and 5 μm) for (a) V_{DS} = 0.1 V, and (b) V_{DS} = 5 V.

comparable to the transverse field. This results in the shift of threshold voltage and increase of off-current [10].

The drain current is inversely proportional to the channel length L, as described by Eqn. (6.12-6.14) in chapter 6. A plot of drain current versus $1/L$, therefore,

should be a straight line. The plot of I_D versus $1/L$ for V_{GS} = 1 V and V_{DS} = 5 V is shown in Fig. 7.12a. As the longitudinal field in this case is much more than transverse field, the drain current increases rapidly with reducing channel length.



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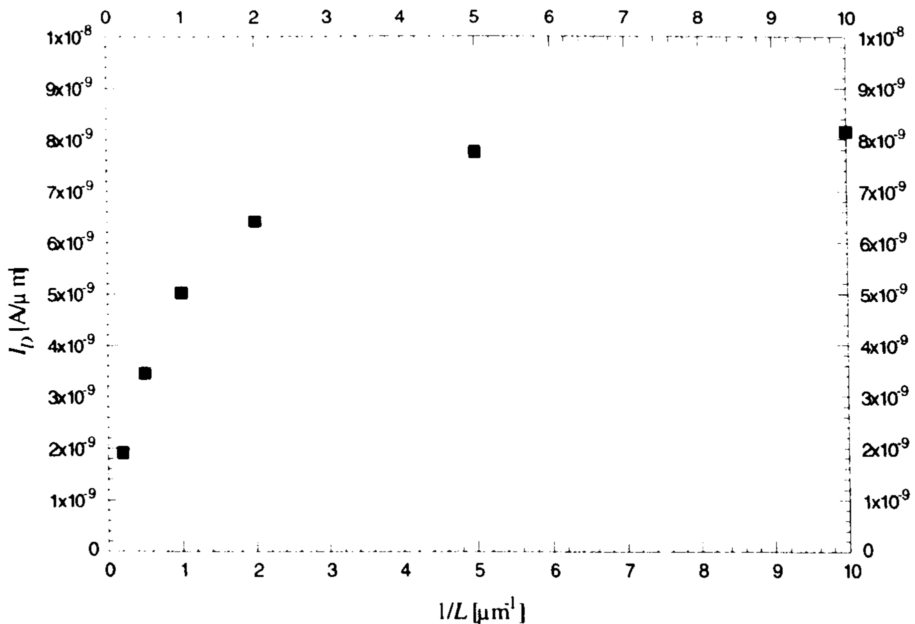

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Figure 7.12 Variation of drain current versus 1/L for (a) V_{DS} = 0.1 V, *and (b)* V_{DS} = 5 V.

The same plot for V_{GS} = 20 V and V_{DS} = 5 V is shown in Fig. 7.12b. In this case, even for the shortest channel length, the transversal field is greater than the longitudinal field, and no short channel effect is observed. However, the drain current changes by a lower rate with $1/L$ for small values of channel length. This effect is because of series resistance between drain/source and the channel. The drain and source do not have direct contact to the channel because of the top oxide and the gap between drain and gate oxide (Fig. 7.1), so that a series resistance can be associated with each one. For long channels, their effect can be neglected. However, when the channel length is comparable to the length of these areas, a part of the drain-source voltage drops across these regions that causes the drain current to reduce.

7.3.4 Variation with Thickness of Gate Oxide

The subthreshold plots of a trap-free device for V_{DS} = 5 V with different thickness of gate oxide, t_{gox} = 0.05, 0.1, 0.2, 0.3, 0.5, and 1 μm, are shown in Fig. 7.13. Except for the thickness of 1 μm, the other curves have the same threshold voltage and subthreshold swing. Since the change in induced charge depends on the oxide capacitance and the change in gate voltage, and because the oxide capacitance is proportional to $1/t_{gox}$, for a thick oxide more negative voltage is needed to repel the

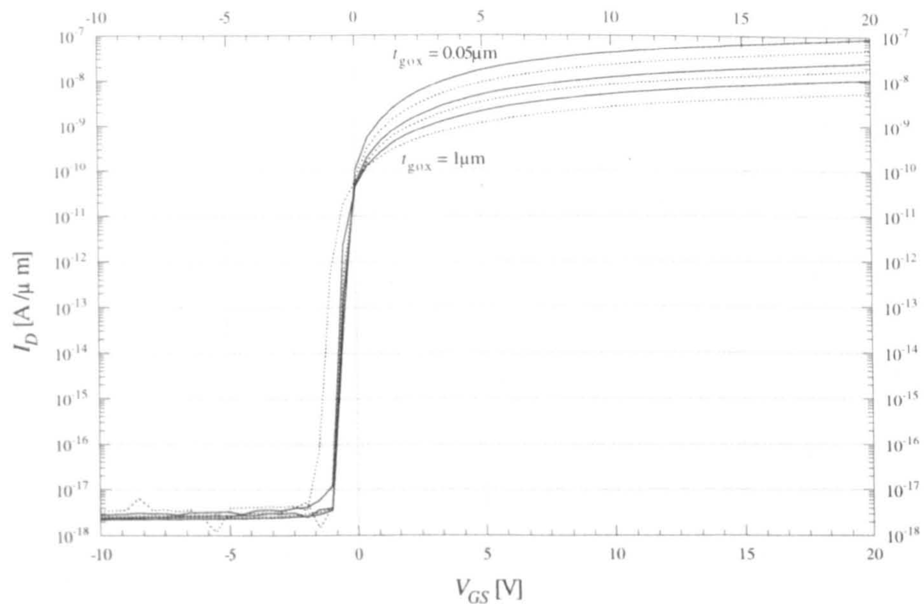


Figure 7.13 Variation of subthreshold plot with thickness of gate oxide (t_{gox} = 0.05, 0.1, 0.2, 0.3, 0.5 and 1 μm).

free electrons and turn the transistor off. Therefore, it has a lower threshold voltage.

The drain current is proportional to C_0, the series combination of oxide capacitance and surface capacitance. When the gate oxide is thick enough, the oxide capacitance is much smaller than the surface capacitance, the total capacitance can be approximated by the oxide capacitance C_{ox}, and drain current is proportional to $1/t_{gox}$. A plot of I_D versus $1/t_{gox}$ is shown in Fig. 7.14. It can be seen that for oxide thickness greater than 0.1 μm the data points lie well on a straight line. For thinner oxides, the surface capacitance is comparable to the oxide capacitance, resulting in reduction of C_0 and consequently drain current.

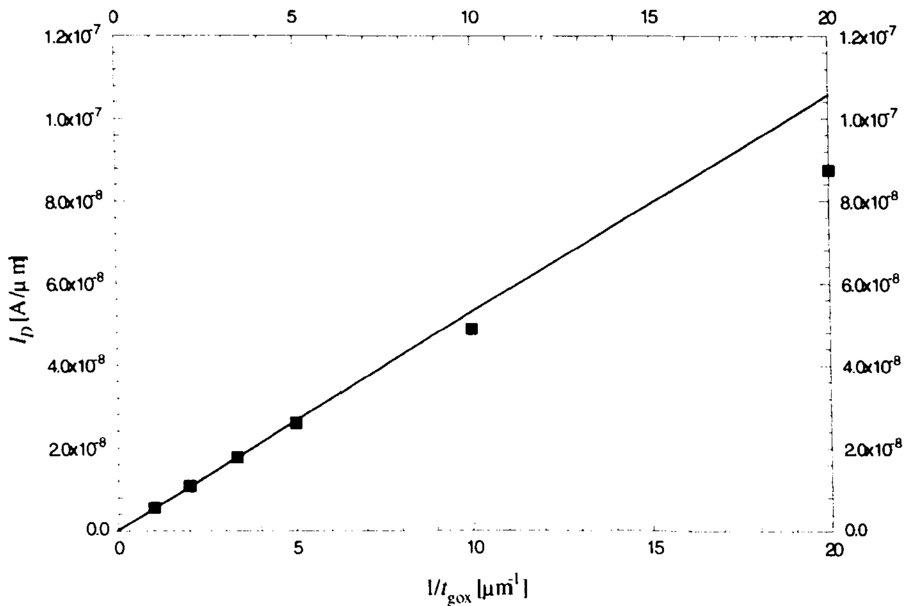


Figure 7.14 Variation of drain current versus $1/t_{gox}$.

7.3.4 Effect of a-Si:H Film Thickness

The subthreshold plots of a device with thickness of a-Si:H equal to 0.15, 0.5, and 5 μm for V_{DS} = 5 V are shown in Fig. 7.15. The thickness of the semiconductor mainly effects the off-current, which takes place through the bulk. When the transistor is on, the channel is more conductive than the bulk, and therefore, the on-current is independent of the semiconductor thickness. However, for unusually large

thickness of 5 μm the conductivity of bulk is so high that it has a dominant effect on the on-current.

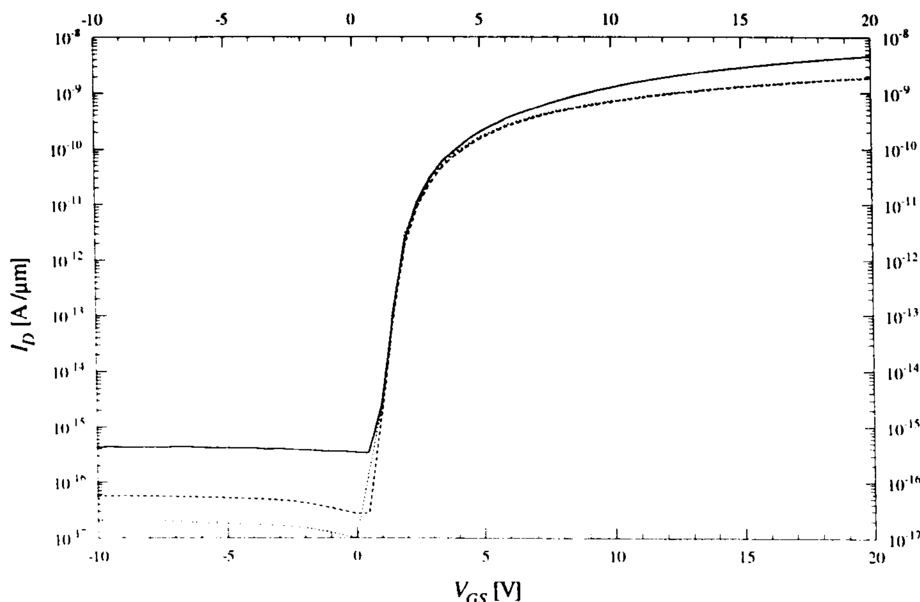


Figure 7.15 Variation of subthreshold plot with thickness of semiconductor.

7.3.5 Effect of Top Oxide

The top oxide that has been used for insulating drain and source provides a parasitic series resistance between source and the channel. This resistance is influence by both the gate field and the space charge close to the source contact, which is a function of voltage between drain and source. From the point of view of dc device operation, it is beneficial to reduce the thickness of oxide as much as possible. However, a thicker oxide provides smaller gate-source capacitance and improves the ac characteristics of device.

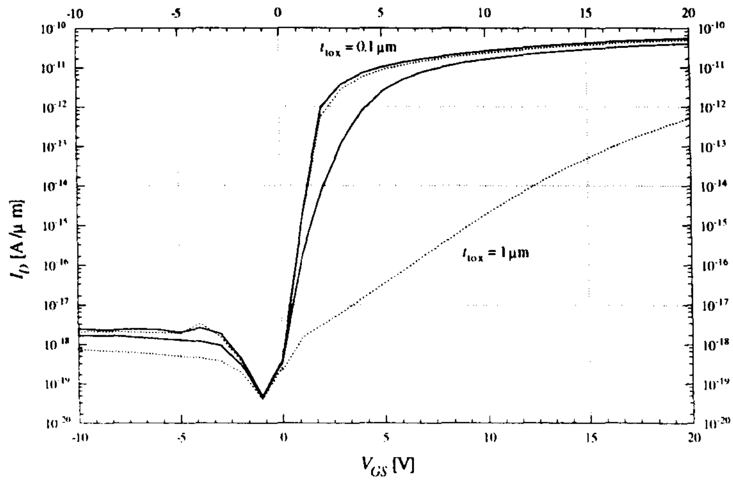
The subthreshold plots of devices with different thickness of top oxide, t_{tox} = 0.1, 0.3, 0.5, and 1 μm, for V_{DS} = 0.1, 1, and 5 V are shown in Fig. 7.16. For thickness of less than 0.3 μm, even with very low V_{DS}, the characteristics are nearly the same and do not change significantly. For thickness of 0.5 μm, with V_{DS} = 0.1 V, the threshold voltage and subthreshold swing are increased and the on-current is slightly reduced. However, there is no significant change for $V_{DS} \geq 1$ V. For thickness

of 1 μm, the top oxide has a considerable effect on the characteristics of the device at low V_{DS}, and the threshold voltage, subthreshold voltage and on-current have changed significantly. This effect is less remarkable for higher V_{DS}. It is concluded that for proper operation of the TFT the thickness of top oxide should be less than 0.5 μm.

7.3.6 Effect of Gap between Drain and Channel

The gap between drain and gate oxide is produced by shadow evaporation. If the shadow evaporation does not ensure that there is no short circuit between drain and source, it may be necessary to perform the evaporation of drain and source in two separate steps by using a proper mask. The minimum gap size in this case depends on the alignment error in the photolithography process.

The effect of this gap is rather similar to the effect of top oxide, discussed in the previous section. However, this region is less influenced by the gate field and its size is more critical. The subthreshold plots of the device with gap size of 0.1, 0.2, 0.5 and 1 μm, for V_{DS} = 0.1, 1, and 5 V are shown in Fig. 7.17. For V_{DS} = 0.1 V and V_{DS} = 1 V, with gap size of 0.5 and 1 μm, the transistor is virtually off with positive voltage applied to gate. This is the same case for V_{DS} = 5 V with gap size of 1 μm. Even with gap size of 0.2 μm, the current has reduced at low drain voltages. With larger gap size, the threshold voltage and subthreshold swing increases significantly. It is suggested that the gap size be kept at the minimum value possible. In fact, the drain metal edge is not abrupt and some conducting metal is found near to the channel. The above estimates are, therefore, an overestimate of the effect of this phenomenon on the drain current. However, the gap size should be kept less than 0.2 μm for proper operation of the TFT.



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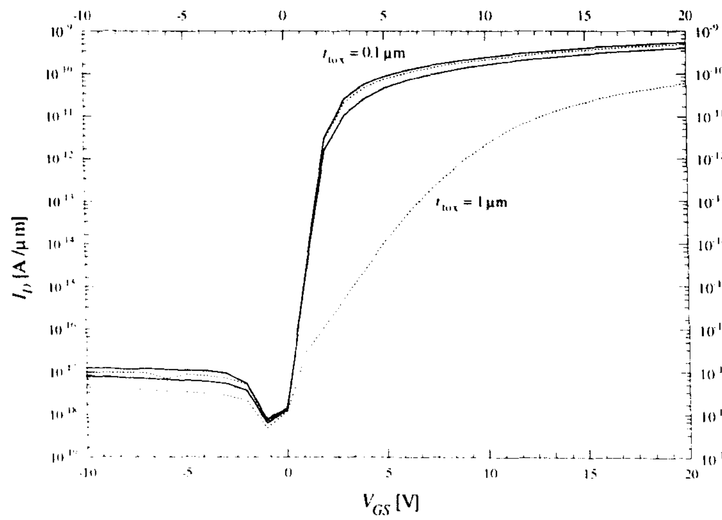

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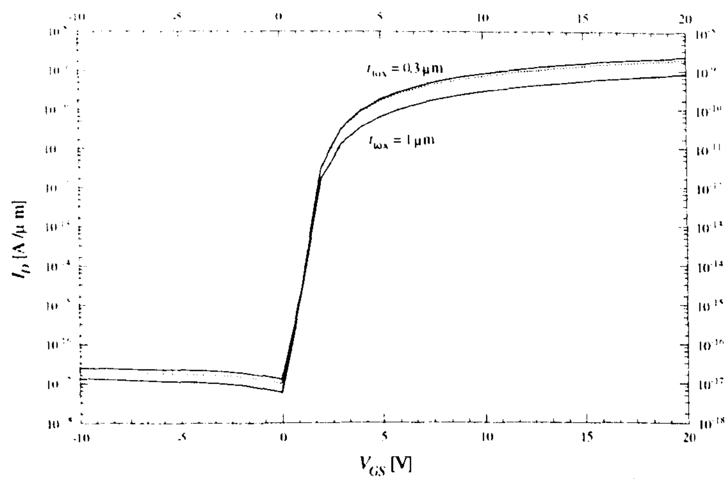

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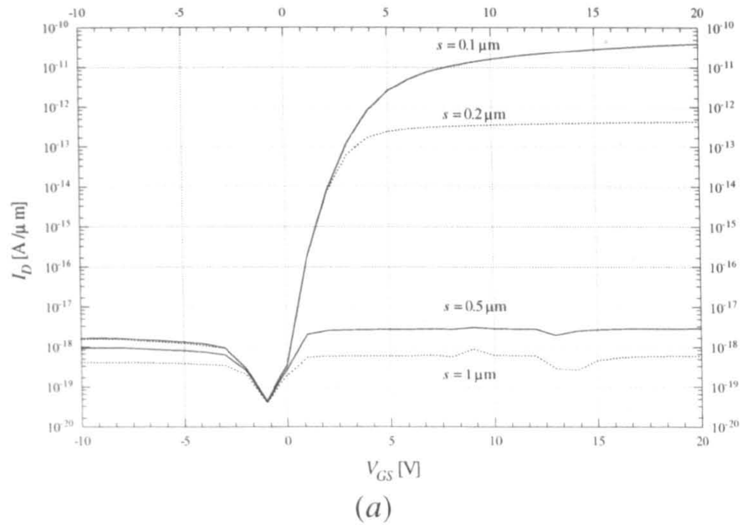
Figure 7.16 Variation of subthreshold plot with thickness of top oxide, t_{tox} = 0.1, 0.3, 0.5, *and* 1 μm, *for (a)* V_{DS} = 0.1 V, *(b)* V_{DS} = 1 V, *and (c)* V_{DS} = 5 V.

7.3.7 Effect of Metal Work Function

Without the presence of surface states, aluminium makes non-rectifying contact with a-Si:H. At zero bias condition, the electrons injected form drain and source fill the trap states and accumulate in the space charge region close to contacts. When a metal with larger work function is used, the drain and source contacts would be rectifying. Especially, when the work function of the metal is more than that of a-Si:H, such as gold, the electrons are depleted from the a-Si:H close to the contacts. When both contacts are rectifying, by applying a voltage between drain and source, the drain is always forward biased and the source is reverse biased for electrons.

Here a situation is investigated where the source contact is aluminium and drain contact is gold with work function of 5 eV. Therefore, the source contact is non-rectifying, and the Schottky contact between drain and a-Si:H is forward biased. In the simulation, in addition to the usual set up, the drain and source contacts were interchanged, and the top contact was used as drain. The subthreshold plots for three different situations are shown in Fig. 7.18 for V_{DS} = 0.1 V and V_{DS} = 5 V. The upper curve is for the case where both contacts are aluminium. In the lower curve, gold has been used for drain contact, and the middle curve is for the case that source and drain are interchanged and the gold contact at top has been used as drain.

Although the gold Schottky contact is in forward bias, the transistor cannot turn on at low drain voltage. With an aluminium contact, the series resistance of the gap and the top oxide regions is low, because electrons are accumulated in the space charge region close to the drain or source and extend towards channel. With a gold drain contact, the concentration of free electrons in the space charge region is very low, resulting in a higher series resistance that reduces the drain current. The transistor has worse characteristics when the drain is on the bottom and the depletion layer associated with the drain contact has extended into the gap.



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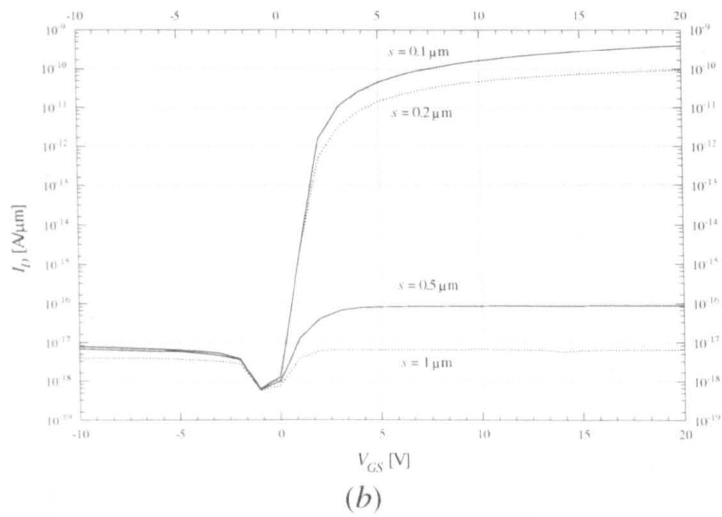

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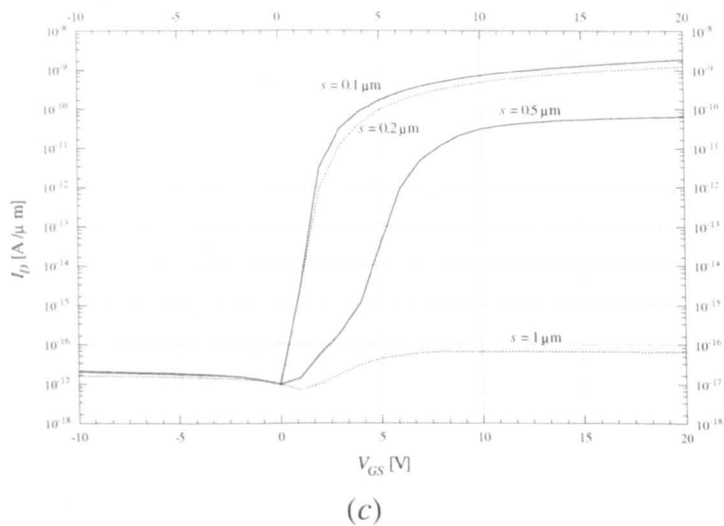

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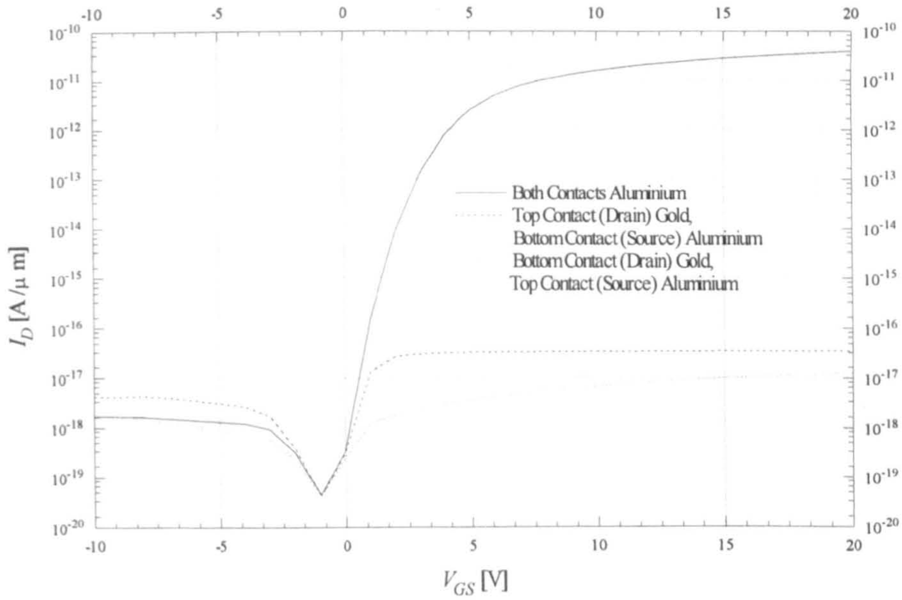
Figure 7.17 Variation of subthreshold plot with the gap size between drain and gate oxide for (a) V_{DS} = 0.1 V, *(b)* V_{DS} = 1 V, *and (c)* V_{DS} = 5 V.



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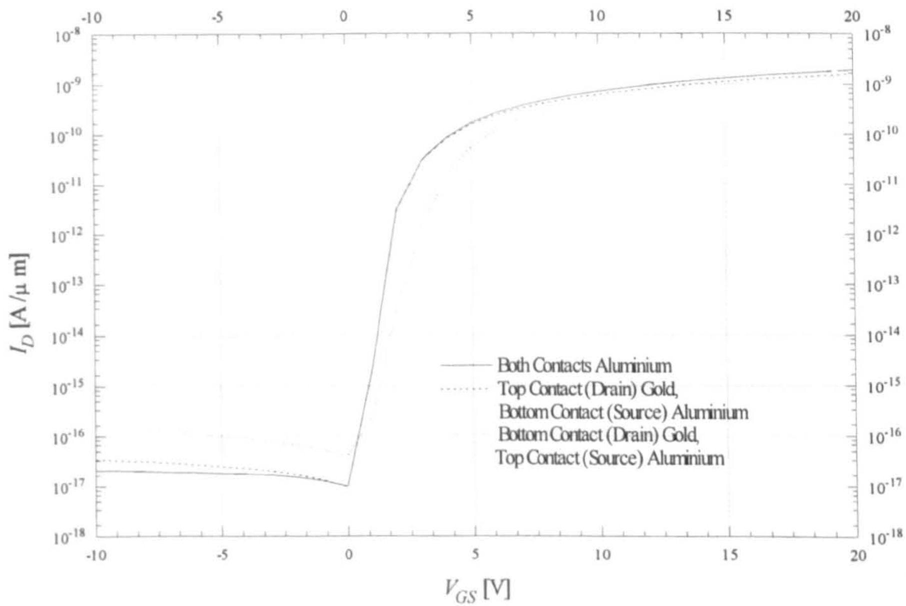

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Figure 7.18 Variation of subthreshold plot with work function of drain and source contacts for (a) V_{DS} = 0.1 V, (b) V_{DS} = 1 V, and (c) V_{DS} = 5 V.

7.4 CONCLUSION

A vertical a-Si:H TFT was modelled using the Medici device modelling package. The effect of different trap states with various trap density and trap energy

levels is investigated. The variation of device characteristics with channel length, thickness of gate oxide, thickness of semiconductor, thickness of top oxide, and the gap size was also studied.

Different trap sets were applied to the model and the effect of each trap set was studied. The trap sets were built up by the traps derived from SCLC measurements, an exponential distribution in the midgap, and an exponential distribution close to the conduction (valence) band representing the band tail. The low energy traps influence the threshold voltage and subthreshold swing, while the higher energy traps reduce the on-current. The off-current is also increased by the presence of traps.

The drain current is proportional to $1/L$ for large channel lengths. The short channel effect was observed for the channel lengths less than 1 μm.

The drain current is inversely proportional to the thickness of gate oxide. However, for very thin oxides the linear relationship is not satisfied due to surface capacitance effects.

The thickness of the semiconductor affects only the off-current. However, the on-current increases if the thickness of semiconductor is much increased.

The top oxide and the gap between drain and gate oxide produce parasitic series resistances that may influence the characteristics of the transistor. Thick top oxide layers or large gap size increase the subthreshold swing and threshold voltage and reduce the on-current. The gap size is more critical and if it exceeds a certain value the transistor can not be turned on.

The device was modelled using aluminium for drain and source contacts that provides non-rectifying contact. The effect of gold that makes Schottky contact with a-Si:H is also studied.

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CHAPTER EIGHT

CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER STUDY

In this thesis, some electrical properties of hydrogenated amorphous silicon (a-Si:H) and their application in thin-film transistors (TFTs) were studied. A part of the work consists of investigation of some key parameters of a-Si:H such as density of states (DOS) in the mobility gap, field effect mobility, and metal a-Si:H contacts. Another part is the theoretical establishment of space-charge limited current (SCLC) and its computer modelling. The experimental results were used in computer simulation of a vertical a-Si:H thin-film transistor.

8.1 MAIN CONCLUSIONS

After a review of various aspects of a-Si:H and thin-film transistors, a novel vertical a-Si:H TFT is demonstrated in chapter 2. The main features and processing steps of this device has been described.

The theory of space-charge limited current for a single discrete trap, proposed by Lampert and Mark, is presented in chapter 3 and has been extended to the multiple discrete trap case. Steady-state space-charge limited current was simulated using the Medici device simulation package with single and multiple set of traps. The structure used in this simulation is similar to the one used for experimental SCLC

measurements, described in chapter 4. In this chapter, the effect of density and energy level of traps, film thickness, temperature, and injection level of electrons has been analyzed.

The *J-V* characteristics of very thin intrinsic a-Si:H was measured using a new structure consisting of intrinsic a-Si:H film on *n*-type crystalline silicon substrate at different temperatures. It is shown that the dominant conduction mechanism in the bulk of a-Si:H is space-charge limited current. In chapter 4, the resulting data were used to investigate the density of states in a-Si:H, using different methods of investigation. The methods based on both assumptions of discrete trap levels and continuous density of states were used for the investigation. By comparison of experimental results with simulation results, it was found that the existence of peak points in the density of states of a-Si:H has nearly the same effect of discrete trap levels set at the peak energy levels. It is concluded that the DOS obtained using the step-by-step analysis or den Böer's method is more reliable than the results obtained from some more sophisticated methods.

The metal a-Si:H contact is studied in chapter 5. It has been shown that a-Si:H makes Schottky contact with all metals used in this study. The conduction mechanism of the contact in forward bias is space-charge limited, and in the reverse bias, thermionic emission is the dominant conduction mechanism. The barrier height of the contact was measured using the reverse characteristics and temperature dependence. It has been shown that the barrier height is rather independent of type of metal contact and mainly depends on the surface states. The effect of annealing has also been studied for chromium contacts. The reverse current showed an increase by annealing, indicating the reduction of barrier height.

Chapter 6 reports the field effect mobility measurement, using a structure similar to an inverted-staggered TFT. The field effect mobility was calculated from the output and transfer characteristics of the sample, and its variation with gate voltage was discussed. The field effect mobility was also calculated from the frequency dependence of drain current.

A vertical a-Si:H thin-film transistor was computer simulated and the results have been presented in chapter 7. Different trap sets derived from the SCLC measurements in chapter 4 were used. The lower energy traps influence the subthreshold swing and threshold voltage, while the higher energy traps affect the on-current. The effect of channel length, thickness of gate oxide and top insulating oxide, thickness of a-Si:H film, the gap size between drain and channel, and the type of drain and source metal contacts were studied. For very small channel lengths, the short channel effect was observed. The thickness of the top insulating oxide and the gap size between drain and channel have critical values. Above these values, the threshold voltage and subthreshold swing increase and the on-current reduces significantly.

8.2 Further Work

In the simulation of space-charge limited current and the vertical TFT, the surface states were ignored. Although SCLC is not sensitive to surface states, however, they affect the barrier height and can therefore influence the thermal equilibrium quasi-Fermi level for very thin a-Si:H films. In the TFT, the charge at the interface of a-Si:H and gate oxide has an essential role on the device characteristics. It is recommended that the surface states and interface charge be added to the models. Another useful effort is to put the other published densities of states in the model to have a more realistic simulation. However, the maximum number of trap energy levels in Medici is limited to 21 and maybe this number would not be adequate to finely define any density of states distribution.

The TFT with Schottky drain and source contacts is an interesting device, in which the leakage current of TFT is limited to the reverse current of Schottky contact. The simulation of this kind of device can provide valuable information about the operation of device. The image force barrier lowering and tunnelling parameters should be well defined in such a simulation. This aspect needs further work.

In the SCLC measurement, thin films of a-Si:H with two different thicknesses were used. These are not enough to study the effect of film thickness on SCLC results, and to analize the scaling law. It would be beneficial to use a-Si:H films with

different thicknesses, with as similar processing history as possible, to be able to compare the results of very thin films with those of thicker films.

In the field effect mobility measurements, silicon dioxide was used as the gate insulator. Silicon nitride is known to produce less surface states in the inverted-staggered structure. A device with silicon nitride as the gate insulator would provide a good comparison between two types of insulator. The device has a fairly large threshold voltage and subthreshold swing. This may be because of charge at the interface of the silicon dioxide and a-Si:H. Another possible reason could be presence of a Schottky barrier at drain and source contacts. Providing n^{+} a-Si:H contact layers on the device and comparing the characteristics of the new device with the current device would help to find out the effect of Schottky contacts on the device characteristics.

Vertical TFTs could overcome the limitated speeds of a-Si:H thin-film transistors, without needing high technology lithography equipment. Laboratory fabrication of structures presented in chapters 2 and 7 could be subject of a new work.

Based on this work an optimum vertical TFT process should be developed and characterized.