THE UNIVERSITY *of* EDINBURGH

Multi-Busbar Sub-Module Modular Multilevel Converter

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Declaration

I declare that this thesis was composed by myself and that the work contained therein is my own, except where explicitly stated otherwise in the text.

(*Chuantong Hao*)

Abstract

Modular multilevel converter (MMC) plays increasingly significant roles in large scale power electronics system including high voltage direct current (HVDC) system, static synchronous compensator (STATCOM), large scale energy storage, motor control, and so on, thanks to its advantages including modular configurations, reduced dv/dt, low total harmonic distortions, and low power losses. The classic sub-module (SM) topologies (e.g. half or full bridge types) all have in common their single connection arrangement between each SM in their series connection within a stack; i.e. a single busbar. This single busbar arrangement does come however with some drawbacks in terms of performance, reliability and flexibility. The lack of redundant switching states limits the potential optimization for the whole MMC.

To solve the above mentioned issue, this thesis presents the control and performance of a new topology of SMs for MMCs, which uses multiple parallel connections between SMs and is referred to as multi-busbar sub-module (MBSM). Stacks made entirely of MBSMs can see improved functionalities such as pre-charging capability, capacitor paralleling, lower power losses, improved reliability, and a rational bypass mechanism in the event of SM failure. The soft-parallel mechanism is proposed to maintain voltage balancing without the requirement of additional spike current inductors. Despite the fact that the number of semiconductors in MBSM MMC has been doubled, semiconductor losses have been reduced to 80% of those in its counterpart. Simulation results have verified the characteristics of a FB MBSM MMC in an HVDC scenario.

Several advanced control schemes for the control of the MBSM MMC are also investigated, including an algorithm to automatically generate independent

variables state space models from linear electrical circuits, a model predictive control-based start-up controller to simplify the SM pre-charge procedure and at the same time improve the transient performance, and a reinforcement learning-based low-level controller to achieve low switching frequency operation of the MBSM MMC. The control schemes are validated by detailed theoretical analysis and simulation results.

Besides, some MBSM applications in the operation scenarios of STATCOM are studied. Two topologies of delta-configured, partially rated energy storage (PRES) MBSM STATCOM and their corresponding low-level controllers are presented to improve the active power output capability. The soft parallel of MBSM is more effective in reactive power mode than active power mode due to the location of ES, which sees their current circulation limited to their own SM capacitor. The proposed controller for the MBSM STATCOM dynamically switches between two operation modes to reduce the converter losses over the extended range of active power. Simulation results confirm the earlier point, in that PRES-MBSM-STATCOM performs better at pure reactive power set-points and marginally better at high active power. This is explained by the fact that MBSM operates more frequently in soft-paralleling mode when the ES releases less power, i.e. reactive power set-points. Then the MBSM concept is further extended to a structure with more busbars, named multi-H-bridge SM, aiming at solving the current sharing issue of paralleled discrete SiC MOSFETs in large current applications. When compared to conventional FBSM constructed directly paralleled SiC MOSFETs, simulation results show that the current sharing performance against on-state resistance mismatch is improved and the switching loss is reduced. The same converter rating can be achieved with fewer MHSMs compared with Si IGBT SMs.

Finally, the designing process of a benchtop-scale, low-voltage, open-source, and affordable hardware prototype of a MMC, the μMMC, is presented with a case study of a three-phase inverter-mode MMC. The proposed μMMC is configured as full bridge SMs type in the experiment, yet the flexible structure makes it capable to be configured as other SM types, including MBSMs. The cost for a

single μMMC could be around 50 pounds. The control framework and concrete implementation are presented in detail. With the application of the μMMC, the STM32Cube Hardware Abstraction Layer, and the MATLAB/Simulink hardware support packages, it is possible to shorten the transition process from simulation to hardware realization to several hours. The experiment setup and results of a three-phase inverter mode MMC validate the proposed μMMC's effectiveness, scalability, and convenience.

Acknowledgement

I would like to express my sincere gratitude to my principal supervisor, Dr. Michael Merlin, for his consistent support and guidance throughout my PhD. Discussions with Michael were always motivating for both my research and my future personal development.

I would also like to thank my assistant supervisor, Prof. Stephen Finney. Steve saved me from the struggle at the start of my PhD and helped me pave the way to the domain of power electronics.

I also want to thank Dr. Paul Judge for the inspiration and valuable discussions on various research topics.

I'd like to thank my IES friends and teammates, including Zoe, Sebastian, Hongye, Nan, Peizhou, Chenqi, Ning, Joy, Mason, Agatha, Hongyi, Duo, Yu, and others, for their support. Also, I want to thank the experienced technicians, Jimmy, Ali, Ian, and Rom.

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Contents

Chapter 1

Introduction

1.1 Modern Electricity Grid

The extensive use of fossil energy and electric power promoted the second industrial revolution and made human society move towards industrial civilization. However, the impact of human development on the earth's climate is very crucial. Carbon dioxide is increasing in the atmosphere and is of considerable concern in global climate change because of its greenhouse gas warming potential [1, 2]. The widespread use of fossil energy may lead to unprecedented changes in the climate system. This has prompted people to discuss how to reduce the use of fossil energy to limit the production of greenhouse gases [3].

Climate change is no doubt a serious global challenge. In response to climate change, 197 countries reached a consensus on the Paris Agreement [4] in 2015 in order to limit the global temperature rise to 2 °C higher than the pre industrialization level, and seek measures to further limit the temperature rise to 1.5 °C. On the one hand, energy efficiency should be greatly improved to reduce the total consumption of fossil energy; on the other hand, renewable energy needs to be vigorously developed. Many countries and regions have proposed targeted energy reform and development objectives and greenhouse gas control goals. China proposes that by 2030, China's new energy demand will be mainly met by clean energy, and carbon dioxide emissions will peak around 2030 [5]. The EU's 2030 Climate and Energy Framework proposes the goal of reducing its net

greenhouse gas emissions by at least 55% compared with the 1990 level by 2030, and increasing its renewable energy consumption target to 38%–40% [6]. The US government proposes that by 2030, greenhouse gas emissions will be reduced by 50%—52% compared with the level in 2005 [7].

Because of its extremely low cost, fossil energy continues to dominate global electrical power production. In recent decades, renewable energy, mainly wind power and solar energy, has become a strategic emerging industry in the world. Scientific research and industrial development on renewable energy have been conducted for many years [8, 9]. For a long time, the development and utilisation of energy have been mainly based on resource endowment. As distributed renewable energy technologies, wind power and solar energy have broken through the resource endowment limit of carriers and can be produced in any place that meets the conditions.

To coordinate the development, allocation, and utilisation of global energy resources, the concept of global interconnected power grids is proposed [10, 11, 12]. Global interconnected power grids can facilitate decarbonization of the electricity system by enabling the harnessing and sharing of vast amounts of renewable energy [13]. Technologies in the area of high voltage direct current (HVDC) transmission [14], distributed energy resource (DER) [15] and smart grid [16] can be used to construct the global interconnected power grids.

1.2 Power Electronics and HVDC transmission

Power electronics play significant roles in the electrical grid due to their high controllability, fast response, and high conversion efficiency. In power generation, DER equipment such as wind turbines and photovoltaic (PV) panels cannot be directly connected to the power grid. Power electronic converters enable high-efficiency power conversion as well as high-power-quality DER-grid connections [18]; In the power distribution scenario and demand side, the connection of DERs, microgrids, energy storage (ES) and flexible loads increases reactive power and harmonics. Active power electronics equipment can ensure power quality and

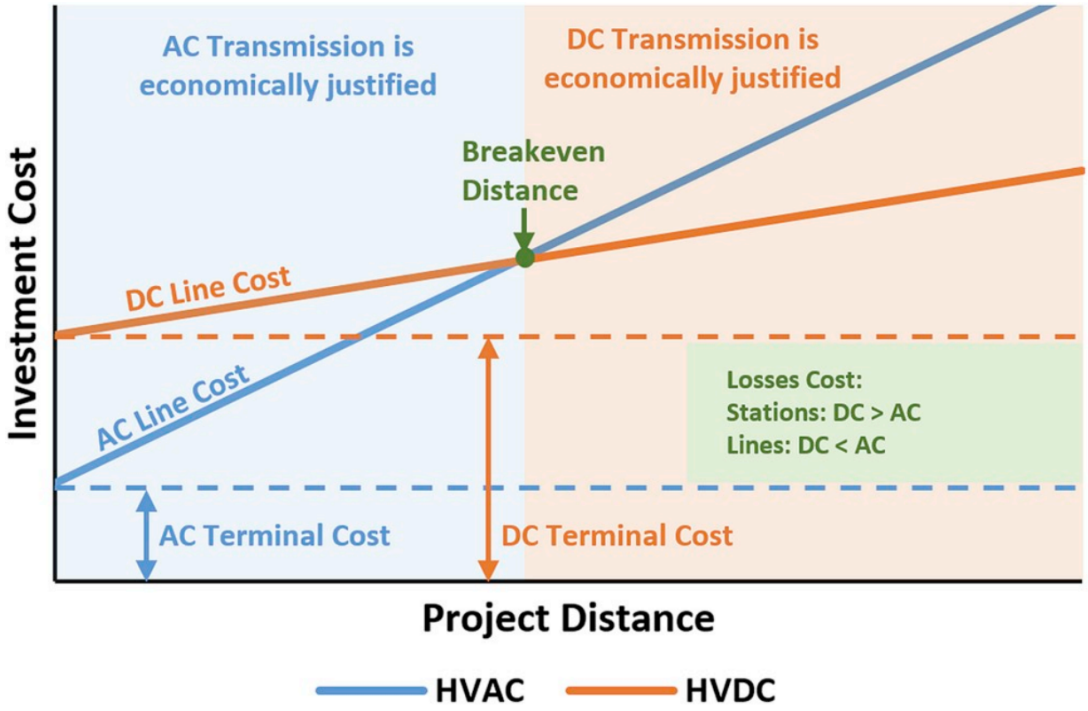


Figure 1.1: Comparative HVDC & AC transmission costs [17]

meet various power conversion requirements in complex application scenarios[19]; In power transmission, high-power power electronic equipment can significantly improve the transmission capacity, improve the power flow distribution, enhance the reliability of the power supply, improve the reliability of large-scale power grid interconnection, and improve the transmission efficiency [20].

HVDC transmission has been increasingly significant nowadays, especially in long distance electric power transmission scenarios, thanks to their superiority in transmission efficiency, controllability, and cost management over High Voltage Alternative Current (HVAC) transmission. Compared with HVAC transmission, the main advantages of HVDC transmission are [22]: (1) not generating reactive power; (2) higher power density, and (3) supporting the interconnection of asynchronous AC systems. Fig. 1.1 depicts the costs of HVDC and HVAC stations versus transmission distance. The requirements of converters and filters make the basic cost of a HVDC station higher, yet lower operation losses make HVDC more attractive for longer transmission distances [23]. The break even distance is 800 km for overhead lines and 50 km for submarine lines. According to the distribution of global HVDC projects shown in Fig. 1.2, Eurasia has obvious ad-

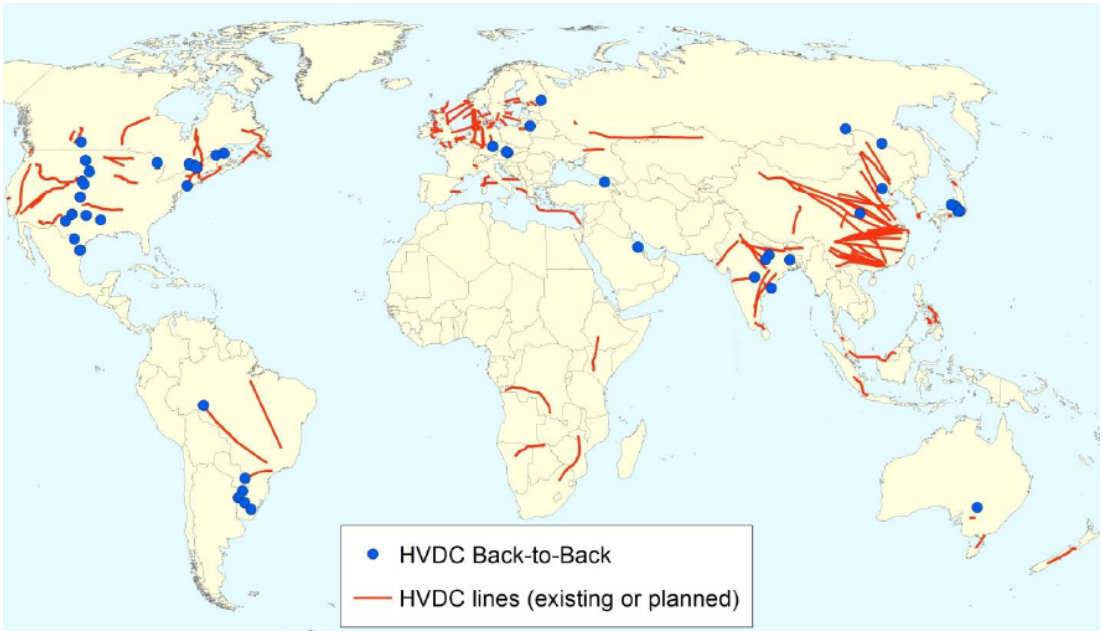


Figure 1.2: Map of HVDC projects distribution [21]

vantages in terms of project number and line length. It was followed by North America, Africa and South America. Australia and New Zealand also have several HVDC transmission projects. HVDC with very high voltage ratings – up to 1,100 kV – enables intercontinental transmission corridors that would otherwise be technologically and economically unfeasible.

The first commercial HVDC transmission scheme was launched by ABB in 1954, connecting the mainland of Sweden to the Island of Gotland, and transmitting 20 MW of power at 100 kV through a 96 km submarine cable. At present, the global HVDC market is dominated by three suppliers: ABB, Siemens, and General Electric (GE). Report [17] summarises 170 HVDC projects based on the BNEF dataset [24], as presented in Fig. 1.3, showing the geographical distribution of the main participants in the HVDC market and their projects. In addition, Fig. 1.4 presents the statistical analysis results of 134 projects according to different power transmission methods. The preferential transmission type is determined by the transmission terrain and the required transmission distance [17]. For example, it is found that most of the HVDC projects in Asia (mainly China and India) are mainly in type of overhead. Fig. 1.5 also summarises the average transmission length, voltage, and rated power of HVDC projects in each

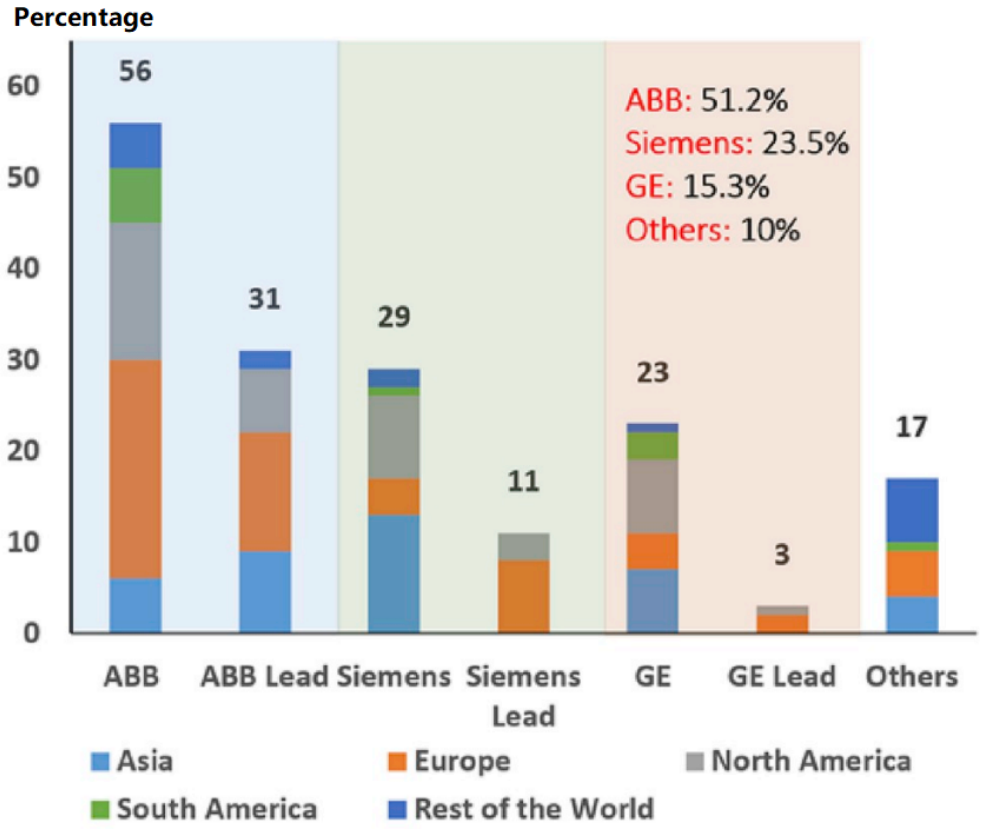


Figure 1.3: Global HVDC technology suppliers landscape based on geographic distribution [17]

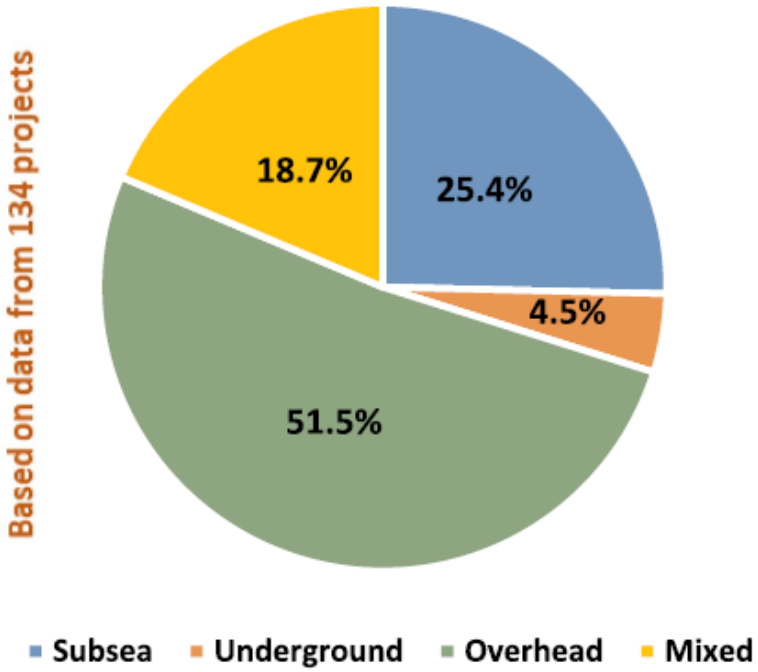


Figure 1.4: HVDC market share of different transmission types: technology adoption distribution [17]

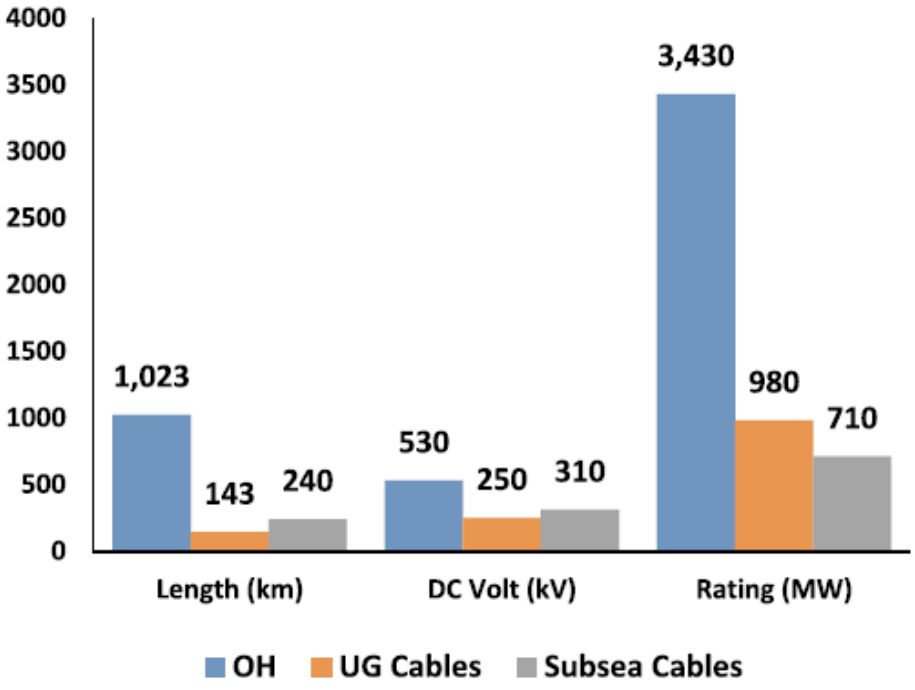


Figure 1.5: HVDC market share of different transmission types: average ratings/length per type [17]

transmission type.

Fig. 1.6 presents the overview of a typical HVDC converter station from the HVDC PLUS project [25]. Major components of an HVDC scheme include [26]: (1) AC switchyard: The AC system connects to a HVDC converter station via a converter bus which is simply the AC busbar to which the converter is connected; (2) AC harmonic filters: In order to limit the influence of AC harmonic current and absorbed reactive power, converter stations usually include parallel switchable AC harmonic filters; (3) Converter transformer: The converter transformers step up the voltage of the AC supply network and inevitability produce acoustic noise which should be considered in the siting of the converter station; (4) Converter: The converter is the most important component which provides the power conversion from AC to DC or DC to AC as required; and (5) DC switchgear: Switchgear on the DC side of the converter is typically limited to disconnectors and earth switches for scheme reconfiguration and safe maintenance operation.

Based on statistical results on recent HVDC projects, ratings at 1000 MW power, 400 kV AC voltage, and ±320 kV DC voltage are commonly applied.

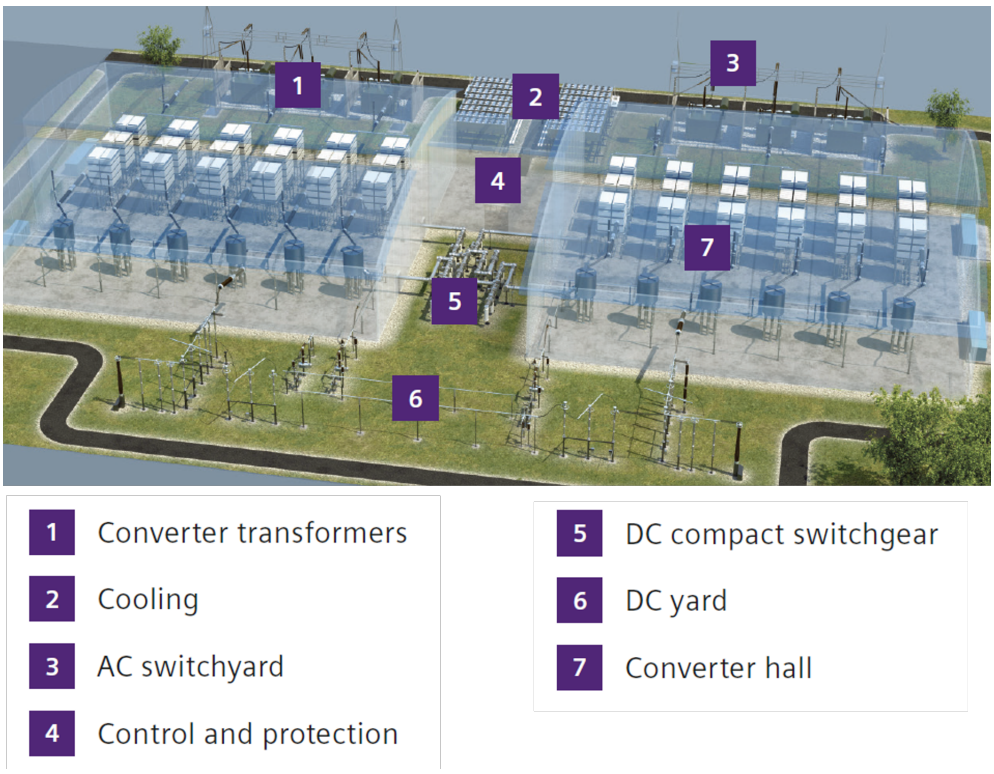


Figure 1.6: A converter station example from the HVDC PLUS project, Siemens [25]

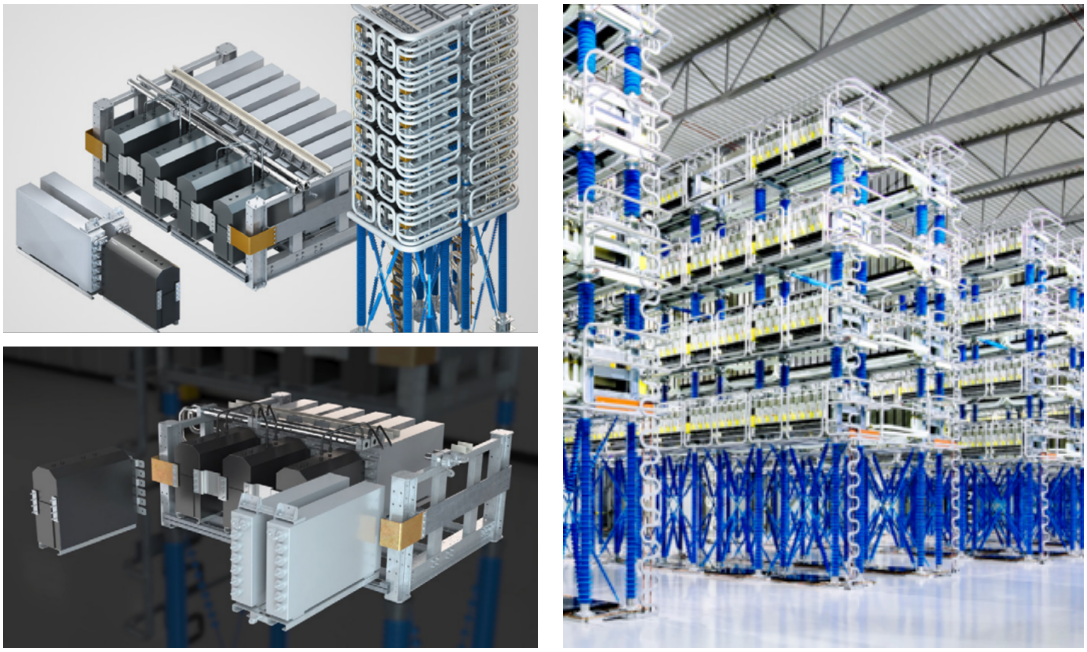
The largest HVDC project in use so far is the ±1100 kV ultra HVDC (UHVDC) project connecting Zhundong and Wannan in China. The power rating is 24,000 MW, and the total transmission length is 3324 km. By 2020, China has also constructed 11 ±800 kV UHVDC projects [27]. In addition to developing towards higher voltage and capacity, multi-terminal HVDC (MT-HVDC) [28] is another topic in the field of HVDC that attracts the interest and efforts of academia and industry. The development of MT-HVDC enables large-scale interconnection between different countries, and DER power generation can be shared and used more efficiently [29].

Modular multilevel converters (MMC), originally proposed by Prof. Rainer Marquardt in 2001 [30], are extensively applied in middle and high voltage applications, especially in HVDC scheme. The stack of an MMC is constructed by a couple of series-connected sub-modules (SMs) to provide the flexibility of stack voltage and, at the same time, extend the voltage capability [31]. By synthesising staircase stack voltage with SM capacitor voltages, MMC allows low total harmonic distortions (THDs) to be achieved with a low switching frequency. Hence,

high voltage output is achieved with a large number of identical SMs constructed by low-voltage-rating power semiconductors.

1.3 Modular Multilevel Converters

MMC serves as a inverter or rectifier in HVDC systems. The MMC reported in the HVDC PLUS project [32] applied more than 200 SMs per converter arm to deliver up to 400 MW at a voltage of 200 kV. The number of SMs required should be increased to match the increase in output voltage. After years of development, MMC has also derived other structures to adapt to different application scenarios. The MMC featuring three-phase to single-phase direct AC/AC conversion is a potential solution for AC power supply [33, 34, 35]. For DC/DC conversion, the application of the MMC concept can take advantage of the dual active bridge (DAB) principle where two cascaded DC-AC MMCs are coupled via transformers [36, 37] Some other novel MMC based topologies include Modular Multilevel Matrix Converter [38, 39], Alternate Arm Converter [40, 41], and so on.



(a) Valves (SMs) (b) Converter

Figure 1.7: Pictures of a MMC station from [42]

Fig. 1.7 shows the picture of SMs and the converter from GE's MaxSine scheme [42]. The SM technology has been deployed on three VSC projects including an offshore wind grid interconnection project. GE claims that quasi-sinusoidal voltage waveforms can be created with the MaxSine scheme and no filter is required for connection to the grid. The principle of the MMC operation is similar to those in Siemen's HVDC PLUS scheme [43] and ABB's HVDC Light scheme [44].

This thesis aims at presenting the research conducting on a new SM topology of MMC, named the multi-busbar SM (MBSM), to improve the performances of the MMC. The modeling, control method, applications are investigated in details and validated by simulation results. The design process of a benchtop-scale FBSM MMC is also presented.

1.4 Contributions from the Author

The contributions from the author are summarised as follows:

MBSM Topology and Control: The author proposed the MBSM topology and the distributed control framework on the basis of the series-parallel SM [45, 46]. The soft-parallel mechanism can effectively prevent the inrush current resulted from capacitor paralleling as well as maintain voltage balancing without the requirement of additional inductors which are commonly used in other parallel SM structures. The performances are verified by simulation results: (1) In-rush currents between MBSMs are eliminated thanks to the soft-parallel mechanism without the requirement of using additional inductors, compared to other reported SM capacitor-parallel techniques; (2) A reduction of about 17% in semiconductor losses compared with the conventional IGBT based FB-MMC. This work has been reported in [Paper1].

MBSM Failure Management and Reliability Study: The management of single semiconductor failures and capacitor failures are investigated by the author. Simulation results show (1) a MBSM stack with a similar over reliability figure over a 20-year operational window as FBSM but while requiring only vastly

fewer redundant SMs, and (2) MBSM is able to operate in degraded mode in case of single semiconductor failure instead of being completely taken out of action, leading to a similar overall MMC availability while using 6 times fewer redundant MBSMs compared to FBSMs. This work has been reported in [Paper1].

Automatic Derivation of State-Space Model from Linear Electrical Circuits: The increasing complexity of power electronic circuits calls for the use of advanced control algorithms, which in turns rely on extensive and accurate models. The author developed the rigorous mathematical framework for an elegant and automatable state space modelling of a linear electrical circuit based on Dr. Michael Merlin's initial proposal. The steps consist in extracting key information of a netlist and deriving the state space model after identifying independent states. The netlist can either be written by the designer or a SPICE software. The resulting MIMO state space model can then be fed into classic control design methods, e.g. LQR or MPC, possibly coupled with robust observing methods, e.g. Kalman filter, to create performant regulators. The proposed automatised derivation strategy is verified by a simple case of electrical circuit and a case of MMC. This work has been reported in [Paper2].

Advanced Control Method for the MBSM MMC: The author applied model predictive control technique to design the start-up controller of the MBSM MMC. The structure of MBSM and internal pre-charging method ensures MBSM capacitors are charged to nominal value smoothly without the requirement of using bulk current-limiting resistors. This work has been reported in [Paper1]. Besides, the author proposed a reinforcement learning based low level controller to further improve the power efficiency of the MBSM stacks.

Delta-Configured PRES MBSM STATCOM: The author proposed two PRES MBSM STATCOM topology and the corresponding control scheme to allow active power to be extracted from ES. ES-MBSMs are distributively configured in a stack in the first topology, and the mixed low level control algorithm contains an FBSM based mode (apart from the soft-parallel mode), which inspired by Dr. Paul Judge's idea, in order to extend the acitve power capability at the cost of higher losses; ES-MBSMs are configured in a sub-stack in the second topology,

the author proposed a sub-stack voltage references calculation algorithm and a mixed PDSC modulation framework to extend the active power capability. This work has been reported in [Paper3] and [Paper4].

Optimal Phase Angle of Additional Circulating Current for a Delta Configured STATCOM: The author derived the analytical solution of the optimal phase angle of the additional third harmonic circulating current that applied to maintain voltage balancing of a delta configured Modultar Multilevel STATCOM. This work has been reported in [Paper3].

Active Current Sharing of SiC Devices through Multi-H-bridges: A new SM topology constructed by multiple parallel-connected SiC MOSFET H-bridges is proposed by the author. Apart from the advantage of achieving high voltage applications with low voltage-rated devices as in conventional SMs in MMCs, the proposed multiple H-Bridge SM also provides the freedom of degree in current rating. A modular multilevel STATCOM model constructed by multiple H-Bridge SMs is built in MATLAB/Simulink. Simulation results show: (1) multiple H-bridge SMs not only allow active current sharing of SiC MOSFET devices without the requirement of auxiliary chokes or capacitors, but also allow voltage balancing of sub-module capacitors; (2) the proposed topology allows the same converter rating to be achieved with half the amount of SMs operating at approximately three times of PWM frequency, compared with Si IGBT SMs converter, while providing 40% power loss reduction; (3) the decoupled conduction paths of paralleled H-bridges see approximately 14.8% switching loss reduction compare with conventional paralleled SiC MOSFET full bridge sub-module. This work has been reported in [Paper5].

Designing of the Micro-MMC: The μMMC developed by the author integrates eight FBSMs in a 10×10-cm PCB with an embedded micro-controller (μC) and an external master controller. The electronics is rated for a 30 V DC bus voltage as typically found in traditional lab power supplies, providing both convenience and safety. The control architecture in the μMMC follows the distributed type: the embedded μC translates voltage commands from the master into MOSFET gate signals, and the master controller uses the stack energy and current

measurements sent by the embedded μC to monitor the energy balancing and power control of the overall structure. The electrical arrangement of the SMs is fully configurable, allowing many different modular converter topologies to be tested. This chapter details the setup process of the μMMC into a 3-phase inverter, later upgraded with energy storage to demonstrate its versatility and potential as a teaching and research tool. This work has been reported in [Paper6] and [Paper7].

This PhD project led to several research outputs arranged in chronological order:

[Paper1] C. Hao, S. Finney and M. Merlin, "Multi Busbar Sub-Module: Enhancing the Series-Parallel Sub-Module to Improve Start-Up Procedure, Power Efficiency, and Failure Tolerance of Modular Multilevel Converters," IET Power Electronics, to be submitted.

[Paper2] C. Hao and M. Merlin, "Automatic Derivation of State-Space Model from Linear Electrical Circuits with Dependent Variables using Modified Nodal Analysis," 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), 2020, pp. 1-6.

[Paper3] C. Hao, P. Judge, W. Ma, S. Finney and M. Merlin, "Delta Configured Multi Busbar Sub-Module Modular Multilevel STATCOM With Partially Rated Energy Storage for Frequency Support," in IEEE Transactions on Power Delivery, vol. 38, no. 4, pp. 2912-2923, Aug. 2023.

[Paper4] C. Hao, W. Ma, M. Merlin, P. Judge and S. Finney, "Multi Busbar Sub-Module Modular Multilevel STATCOM with Partially Rated Energy Storage Configured in Sub-stacks," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), 2022, pp. 1-8.

[Paper5] C. Hao, P. Judge, S. Finney and M. Merlin, "Enabling the use of lower current-rated SiC MOSFET devices in large-current power converters by paralleling multiple H-bridges in the sub-modules," 19th International Conference on AC and DC Power Transmission (ACDC 2023), Glasgow, UK, 2023, pp. 142-147.

[Paper6] C. Hao, J. Cao, P. Xia, S. Finney, and M. Merlin, "Meet the Micro-

MMC," IEEE Power Electronics Magazine, Revised version under review.

[Paper7] C. Hao, Z. Blatsi, P. Xia, S. Finney, and M. Merlin, "Designing a Low-Voltage Modular Multilevel Converter," 2023 IEEE 11th International Conference on Power Electronics (ECCE-Asia), Accepted.

1.5 Thesis Outline

The structure of this thesis are organised as follows:

Chapter 1 starts with an overview of the modern electricity grid, where power electronics play a significant role. The HVDC system is then introduced in detail as its superiority in transmission efficiency, controllability, and cost management over the HVAC system. The key equipment in HVDC system, the MMC, is briefly presented to start the discussion.

Chapter 2 introduces the structure of MMC, commonly used SM topologies, and distributed control systems. The control system is divided into three layers so that MMC with new SM topologies can share the same higher-level controllers as conventional MMC. Simulation results, including normal operation and loss analysis of a FBSM MMC, are also presented in this chapter.

Chapter 3 presents the control and performance of the MBSM, which uses multiple parallel connections between SMs. This chapter starts with a discussion on the operation principle of the MBSM designs and how the MBSM approach can eliminate in-rush current during the paralleling of MBSMs. Then, single device failure management and the reliable study are presented. At last, the multi-busbar equivalent of the classic full-bridge SM topology is simulated and compared with its single-busbar counterpart.

Chapter 4 is composed of three topics that relate to the advanced control method for the MBSM MMC. Section 4.1 lays out the rigorous mathematical framework for an elegant and automatable independent-variables state space modelling of a linear electrical circuit. The proposed automatised derivation strategy is verified by a simple case of electrical circuit and a case of MMC. Section 4.2 presents the MPC-based MBSM MMC start-up control scheme, where

the precharge of capacitors is converted into a DCDC converter control problem and solved by MPC. In Section 4.3, reinforcement learning approach is applied for MBSM low level control. A DQN agent is designed and trained to improve the voltage reference tracking, SM voltage balancing and switching frequency reduction performances.

Chapter 5 investigates more applications of the MBSM in the scenario of STATCOM. The modeling and higher control of the delta configured STATCOM, and how ES is configured in MBSMs are provided in Section 5.1. Section 5.2 investigates a STATCOM with distributedly integrated partially-rated ES in MBSMs. The study uses the analytical formulation of the MBSM to derive the mixed mode low level control system and the optimal phase angle of the circulating current required for SM balancing. The objective of the controller is to output 1 p.u. active power with 60 % ES-MBSMs. Section 5.2 studies the structure and low level controller to allow ES-MBSMs to be configured in a sub-stack in order to reduce the switching frequency. Section 5.4 further extend the concept of MBSM to structure with more busbars, named multi-H-bridge SM. The structure and the operation principle are introduced first, and followed by a detailed low-level control algorithm aimed at solving the unequal steady-state current issue resulting from on-state resistance mismatches of paralleled discrete SiC MOSFETs.

Chapter 6 presents the design process of a low voltage, cost efficient MMC, the μMMC, which consists of a benchtop-scale, low-voltage, open-source, and affordable hardware prototype of an MMC, intended for research and teaching. The PCB layout, components sizing, cost of element, concrete implementation of the distributed control system, and the case study of a three phase inverter mode MMC are all presented.

Chapter 2

Background on Modular Multilevel Converter

2.1 MMC Topology and Design

The MMCs in HVDC stations are essentially AC/DC or DC/AC converters [47, 48, 49]. Different from conventional two level converters, strings of series-connected SMs are controlled to construct staircase stacks voltages with capacitor voltages so that MMC has low harmonic distortion and low switching loss [40, 50]. Moreover, the modular design of MMC makes it more convenient for large-scale manufacturing and maintaining [51]. Recently, the MMC has also been gaining interests in MVDC applications [52, 53], such as motor drives [54], Static compensator (STATCOM) [55] and battery energy storage system [56].

The structure of a classic three-phase MMC is shown in Fig. 2.1 [57, 58, 59]. V_{dc} represents the voltage of the DC transmission link. In each phase, there are two arms consisting of a stack of series connected, nominally identical SMs and a small arm inductor (or stack inductor) L_S for suppressing high order harmonics in the arm current. The mid-points of the two arms in each phase are connected to three phase inductors L_P, and form the AC terminals, whose voltages are represented by u_a, u_b, and u_c in Fig. 2.1. The reference directions of currents indicate that the MMC operates in inverter mode. The upper and lower arms of three phase legs are represented by subscripts "u" and "l", respectively, in this

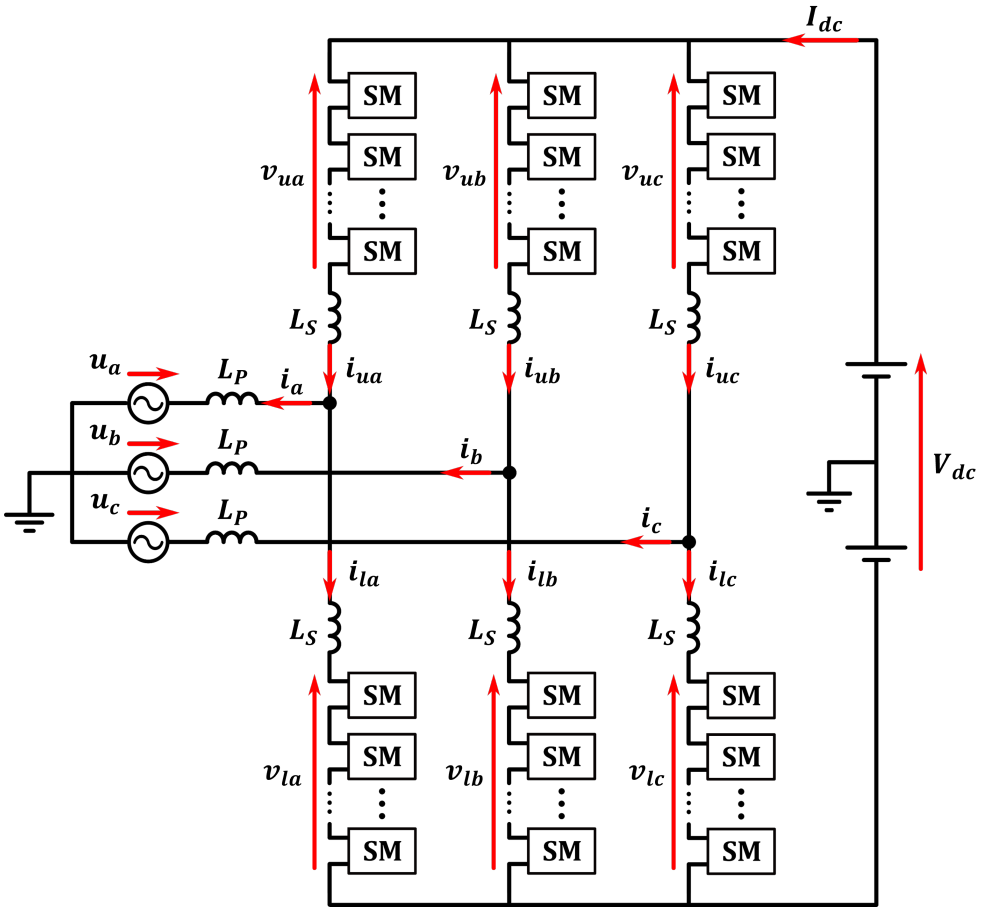


Figure 2.1: Three-phase modular multilevel converter (MMC)

thesis. Take v_{ua} and v_{la} as examples, the former represents the voltage of the upper stack in phase A, and the latter represents the current of the lower stack in phase C.

Among all of the advantages that MMC offers, the following are the most attractive to researchers [60, 61, 62, 63]:

(1) The modular configuration of the MMC provides an ability to scale in voltage and power ratings.

(2) Output voltage and current waveforms of the MMC have reduced $\frac{dv}{dt}$ and ripple; resulting in low total harmonic distortion (THD) thanks to the staircase stack voltage waveforms.

(3) MMC is able to operate at a very low switching frequency for each individual switches, yet the large number of series-connected SMs, results in a high compounded switching frequency for the whole converter.

(4) Fault-tolerant operation can be achieved when employing redundant SMs in each stack.

2.2 SM Topologies

The MMC can generate large voltage waveforms thanks to its stacks of hundreds of SMs connected in series. Extensive reviews on SM structures are provided in [31] and [64]. Even though many novel SM structures have been proposed for specific applications in the past decade [65], Half Bridge (HB) SM and Full Bridge (FB) SM are still the most commonly used topologies so far.

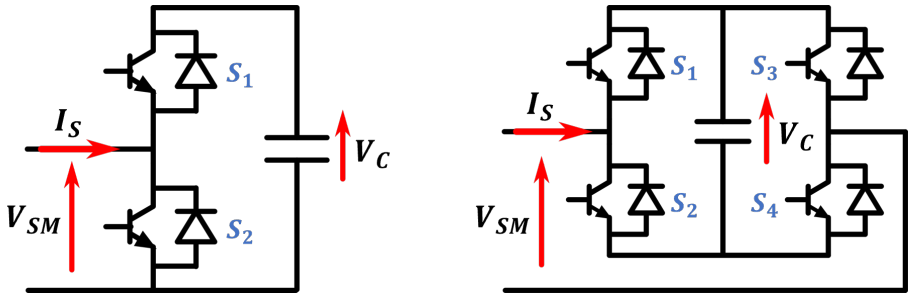


Figure 2.2: The most commonly used SM topologies: (a) HBSM, (b) FBSM.

Fig. 2.2 (a) shows the structure of an HBSM consisting of two semiconductors, S_1 and S_2, and a capacitor. S_1 and S_2 will not be turned on simultaneously otherwise the SM capacitor would be short-circuited. The output voltage that an HBSM can provide is 0 and $+V_C$ depending on the states of semiconductors, as summarized in Table 2.1. If S_1 is on while S_2 is off, the SM capacitor will be connected into the main circuit and contribute to stack voltage; If S_1 is off while S_2 is on, the SM capacitor will be bypassed. An HBSM based MMC exhibits low power losses as only one semiconductor in each HBSM conducts current in either case. However, since HBSM is not able to output negative voltage, an HBSM MMC doesn't have the capability of DC fault blocking.

The FBSM is constructed by one capacitor and four semiconductors, marked as S_1, S_2, S_3, and , S_4, as presented in Fig. 2.2 (b). Apart from states of Positive Voltage and Zero Voltage, the FBSM can also output Negative Voltage when S_2

Table 2.1: Semiconductor states and output voltage of the HBSM

State	S_1	S_2	V_{SM}
Positive Voltage	1	0	$+V_C$
Zero Voltage	0	1	0
Block	0	0	N/A

and S_3 are both on thanks to extra semiconductors. Similar to the situation in HBSM, the semiconductor pairs S_1-S_2 and S_3-S_4 can not be switched on simultaneously in order to support the capacitor voltage. The remaining feasible states of the FBSM and the output voltage are summarized in Table 2.2. The FBSM can provide DC fault blocking capability, however, at the expense of significantly higher semiconductor cost and losses compared with the HBSM, as twice the number of semiconductors are required and conduct stack current in all states.

Table 2.2: Semiconductor states and output voltage of the FBSM

State	S_1	S_2	S_3	S_4	V_{SM}
Positive Voltage	1	0	0	1	$+V_C$
Negative Voltage	0	1	1	0	$-V_C$
Zero Voltage 1	1	0	1	0	0
Zero Voltage 2	0	1	0	1	0
Block	0	0	0	0	N/A

Fig. 2.3 presents some other SM topologies of interest from [31]. The clamped double SM shown in Fig. 2.3 (a) consists of two HB SMs, two additional diodes, and one extra semiconductors. The semiconductor losses of an MMC configured with clamped double SMs is lower than a FBSM MMC, and higher than a HBSM MMC that has the same voltage level, yet can still handle DC fault. The five-level cross-connected SM presented in Fig. 2.3 (b) is a similar topology contains two HBSMs connected back to back by two extra semiconductors. The loss performance is also similar to that of the clamped double SM. Fig. 2.3 (c) and Fig. 2.3 (d) present two three level SMs: the three level flying capacitor (FC) SM [66, 67, 68] and the three level neutral-point-clamped (NPC) SM [69, 70, 71]. Compared to HBSM and FBSM, both FC and NPC see limited improvement in

efficiency performances but require more complex control scheme [31], make them less attractive to industry.

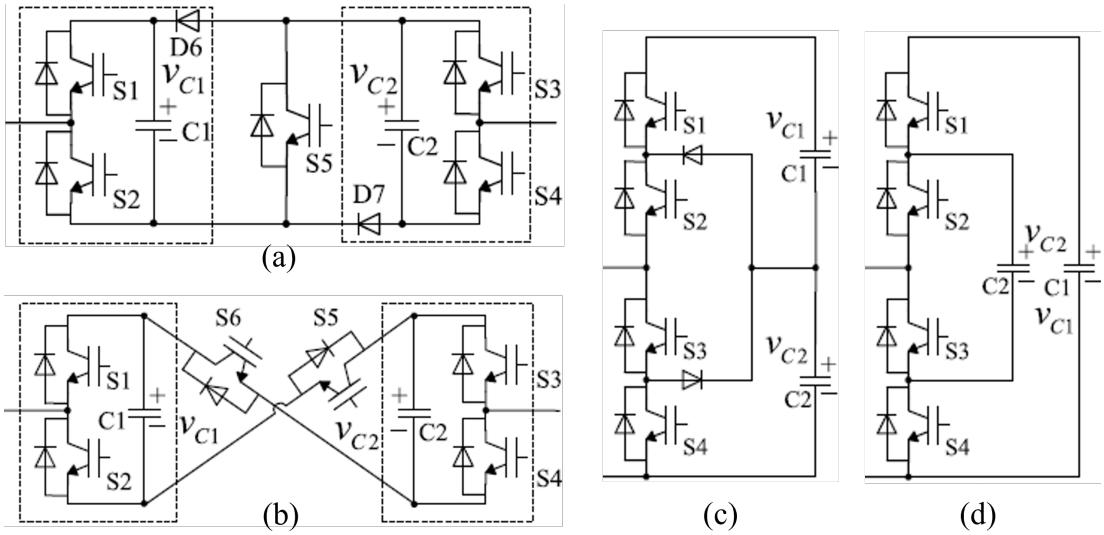


Figure 2.3: Other SM topologies: (a) the clamped double SM, (b) the five level cross-connected SM, (c) the three level FC SM, and (d) the three level NPC SM. Cited from [31]

The classic SM topologies (e.g. HBSM or FBSM types as shown in 2.2) all have in common their single connection arrangement between each SM in their series connection within a stack; i.e. a single busbar. This single busbar arrangement does come however with some drawbacks in terms of performance and flexibility. First, the pre-charging of the SM capacitors is traditionally conducted through high-impedance pre-insertion resistors to the AC or DC grids; in essence bulky devices which are bypassed and left unused outside the start-up periods [72]. Second, the bypass switch – employed to electrically shut across the SM terminals in case of SM failure – contradicts the pre-charging procedure and must thus remain open before energyzing the MMC station; failure to close the bypass switch during operation will lead to a total system failure of the MMC. Third, the SM capacitors will regularly experience voltage deviation outside the average SM voltage within the stack, in spite of the best efforts from the balancing algorithm; this means that extra voltage margin must be implemented when designing the SM hardware. Fourth, the single busbar arrangement restricts the number of switching states for the semiconductor devices within a SM to often only one

combination for a given voltage output; the failure of a single device will thus lead to the failure of the entire SM. Fifth, this lack of redundant switching states also limits the potential optimization for the whole MMC; some research [73] have attempted to demonstrate the benefit of parallel connections.

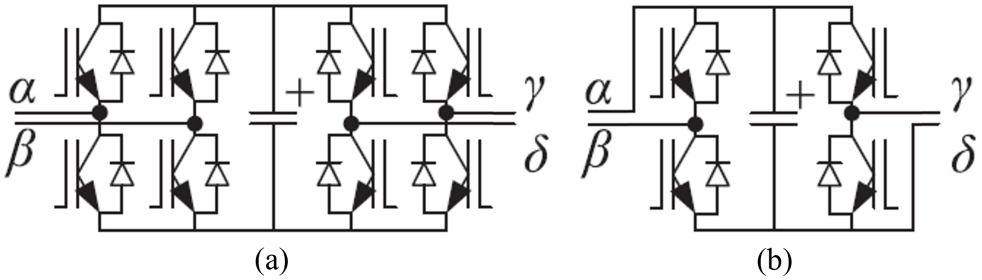


Figure 2.4: Series and Parallel SMs proposed in [45, 46]: (a) double full-bridge, (b) double half-bridge.

To tackle with the issue caused by single conduction path, many novel SM structures allow both series and parallel module connectivity are purposed [45, 46, 74, 75, 76], as shown in Fig. 2.4. The inactive modules are still used, instead of being bypassed, for energy storage through being parallelized. Even when the SMs cannot contribute to the stack voltage, the current load from active modules could be shared to reduce the total parasitic inductance and resistance [46]. The new SM structure allows energy storage elements to be dynamically rewired in various series–parallel configurations, thus generating a wide range of output voltage levels [74]. The series and parallel connection allows wide frequency range operation [75] and sensorless balancing [76], provides more possibilities for further improvements.

The comparison of different SM topology in terms of cost, complexity, losses, and negative voltage capability are summarized in Table 2.3

2.3 Modeling and Control

2.3.1 Distributed Control System

Widely applied in two-level or three-level converters, centralized controllers, normally Digital Signal Processor (DSP) [77, 78, 79, 80, 81], are required to realize

Table 2.3: Comparison of different SM topology

SM topology	Cost	Complexity	Losses	Negative Voltage Capability
Half Bridge	Low	Low	Low	No
Full Bridge	Medium	Medium	High	Yes
Clamped double	High	High	High	Yes
Five level cross	High	High	High	Yes
Three level NPC	High	High	High	Yes
Double Full Bridge	High	Medium	Medium	Yes

all measurement and control tasks. Then, high frequency (up to hundreds of kHz) gate signals for the power semiconductors are generated by Field Programmable Gate Arrays (FPGA) [82, 83, 84]. In the control of MMC with a large number of SMs, concentrating all tasks in one digital controller will lead to the necessity of larger amount of input and output (I/O) pins, heavy computational burden, and a long execution time that may exceed the control cycle. Moreover, centralized control limits the modularity and scalability of the whole MMC system in both hardware and software development [85, 86]. Therefore, distributed control system [87, 88, 89] attracts increasingly attention as control tasks and computational burden are distributed to different controllers, and the modularity of the system is consequently improved [90].

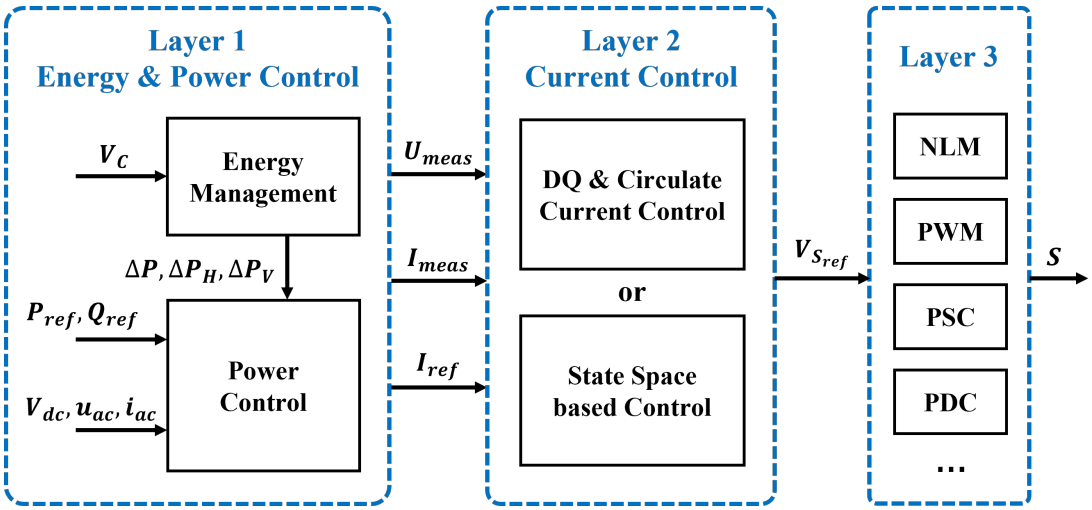


Figure 2.5: Distributed Control System

The distributed control system of MMC applied in this thesis is shown in

Fig. 2.5. Layer 1 is in charge of energy management and power control. SM voltages are used to calculate the energy stored in each stack and generate power references that should be transmitted among stacks. Then the reference of active power and reactive power, AC voltage and current, DC voltage, as well as balance power references are all fed into power controller to generate current references. In the second layer, currents are regulated by conventional Direct Quadrature (DQ) controller [91, 92, 93] (together with circulating current controller), or state space model based controller. Stack voltage references are obtained from Layer 2. Finally, the low level controller in Layer 3 translates stack voltage references into SM switch commands. Many modulation framework can be applied, including nearest level modulation (NLM) [94, 95], pulse width modulation (PWM) [96, 97], phase shift carrier (PSC) [98, 99], phase disposition carrier (PDC) [100, 101], and so on. NLM ensures MMC with large amount of SMs to operate in low switching frequency. PWM, PSC, PDC are usually applied to reduce the THD of the AC output. The demonstration of PSC is presented in Fig. 3.8. The demostration of PDC and PSC are presented in Fig. 5.15

2.3.2 Energy Management & Power Control

Total energy management ensures energy balance between the DC side and the AC side of the MMC. The total stack energy deviation is denoted as ΔE, and is calculated by the difference of energy stored in all SMs and the rated total energy. In ideal operation, the energy storage in all stacks should be balance, which means that $\Delta E_{ref} = 0$. The block diagram of total energy management is shown in Fig. 2.6, where $k_{\Delta P}$ is a real number between 0 and 1. The power difference commands are allocated to both the AC side and the DC side. Finally, DC current reference I_{dc} and AC current reference in DQ framework I_d are both generated.

In addition, the energy balance of the three phases, also known as horizontal balance, should be maintained as well. Suppose that ΔE_j represents the energy deviation of phase j where $j = a, b, c$. Then the reference of ΔE_j can be derived as $\Delta E_{j_{ref}} = \Delta E/3$. The control block diagram of horizontal energy management

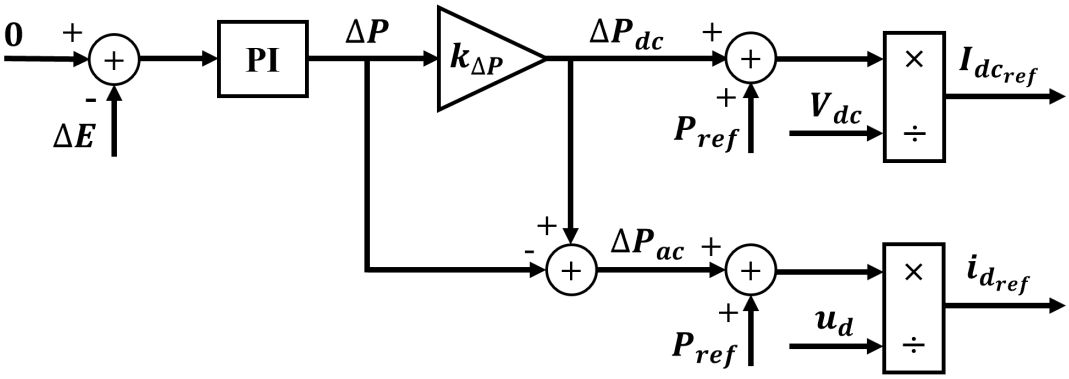


Figure 2.6: Total energy management

is shown in Fig. 2.7.

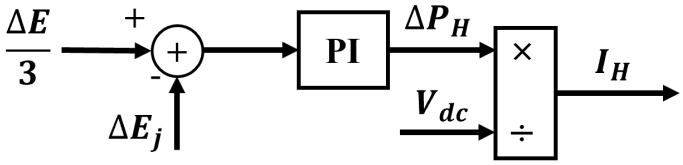


Figure 2.7: Horizontal energy management

Vertical energy management can tackle the issue of energy imbalance between the top and bottom stack in each phase. The control objective is to ensure that the energy deviation of the upper stack ΔE_{uj} is equal to the energy deviation of the lower stack ΔE_{lj}. As shown in Fig. 2.8, the difference of the upper and lower energy deviation is fed to a PI controller and finally vertical balance current signal I_V is generated.

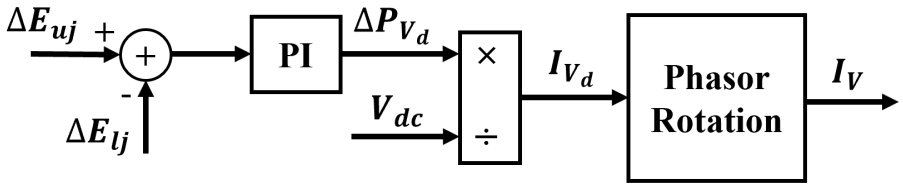


Figure 2.8: Vertical energy management

2.3.3 Current Control

DQ and Circulating Current Control

The principle of the conventional current control includes DQ and circulating current control. AC side current and DC side current control are analyzed separately based on superposition theorem. To further simplified the analysis of current control and the superposition of stack voltage commands, a simplified model of MMC which consists of single phase elements is used here, as shown in Fig. 2.9. The stack voltages v_{uj}, v_{lj} and stack currents i_{uj}, i_{lj} are the sum of DQ control outputs and circulate current control outputs.

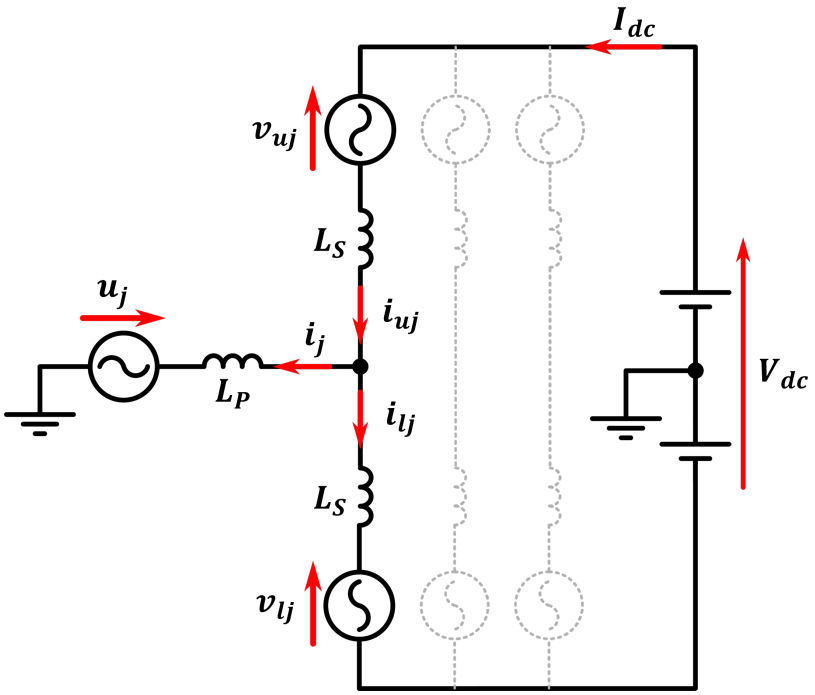


Figure 2.9: Simplified model of MMC for current control analysis.

At first, the model when only AC source functions is investigated. The stack voltages are represented as $v_{uj}{}'$ and $v_{lj}{}'$ while stack currents are represented as $i_{uj}{}'$ and $i_{lj}{}'$, as shown in Fig. 2.10 (a). The model in Fig. 2.10 (b) remains unchanged and only the layout of the studied circuit is rearranged to simplify the analysis. Suppose that the voltage and current responses in the two branches are the same, and merge the inductors and controlled voltage sources in the two brunches, a new equivalent classic model Fig. 2.10 (c) is obtained. The relationship between

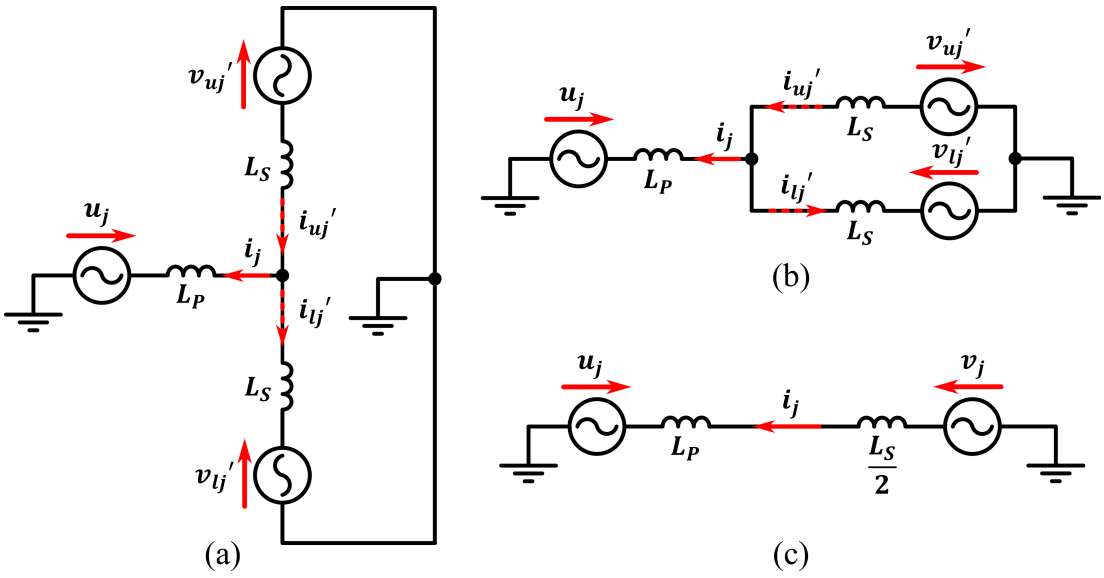


Figure 2.10: Simplified AC side equivalent model of MMC

the stack voltages and brunch currents are summarized as Eq. (2.1).

$$\begin{cases} {v_{uj}}' = -v_j \\ {v_{lj}}' = v_j \\ {i_{uj}}' = \dfrac{i_j}{2} \\ {i_{uj}}' = -\dfrac{i_j}{2} \end{cases} \tag{2.1}$$

According to Fig 2.10 (c) and Kirchhoff's law, Eq. (2.2) holds.

$$v_j = u_j + (L_P + \frac{L_S}{2})\frac{di_j}{dt} \tag{2.2}$$

Rewrite Eq. (2.2) in three phase version and introduce a new variable $L_0 = L_P + \dfrac{L_S}{2}$, the equation becomes Eq. (2.3), which is a typical model to describe the dynamic of a three phase inverter.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} + L_0 \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.3}$$

Eq. (2.4) describes the system in rotating frame after DQ transformation from Eq. (2.3). The block diagram of classic DQ control are shown in Fig. 2.11.

Numerous researches have been done on DQ control [102] so the derivation process is omitted in this thesis.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} + \begin{bmatrix} 0 & -\omega L_0 \\ \omega L_0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + L_0 \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.4}$$

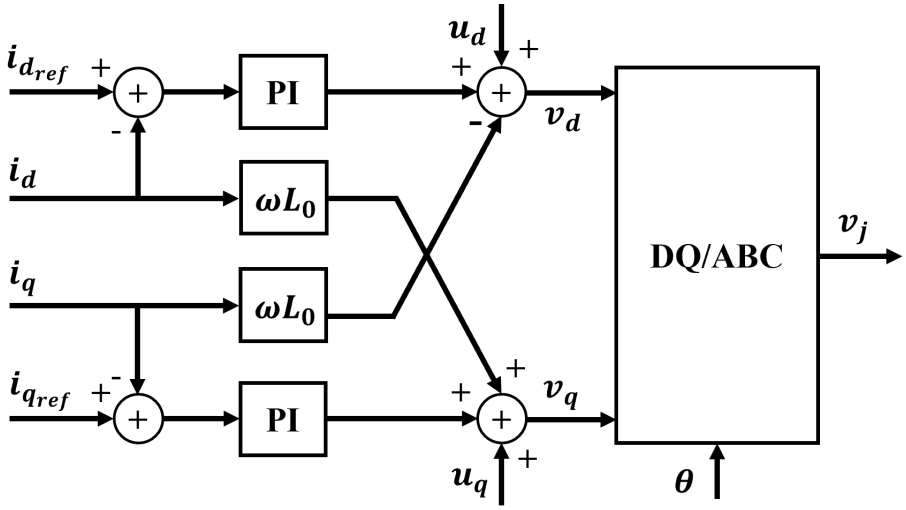


Figure 2.11: Block diagram of DQ control

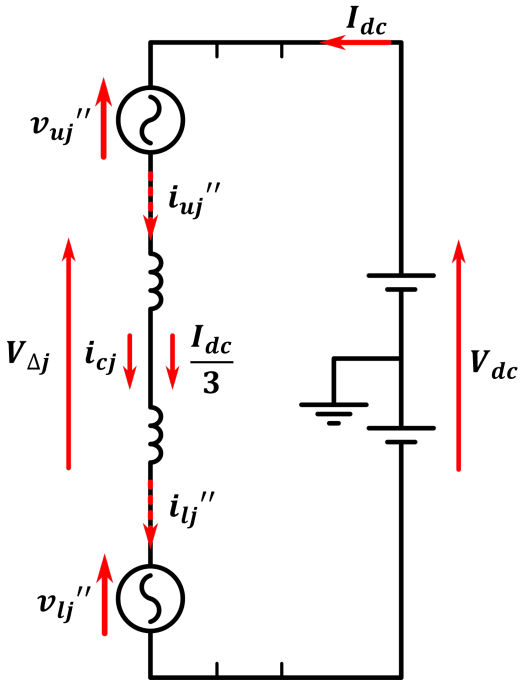


Figure 2.12: DC side equivalent model of MMC

DC source equivalent model is presented in Fig. 2.12. The stack current

contains part of the DC current and circulate current i_{cj}. The stack voltages are represented by ${v_{uj}}''$ and ${v_{lj}}''$ while stack currents are represented as ${i_{uj}}''$ and ${i_{lj}}''$. The voltage on the two series connected inductors is denoted as $v_{\Delta j}$. According to Fig. 2.12, the relationship between stack currents, DC current and circulate current is described by Eq. (2.5). Thus, $v_{\Delta j}$ can be calculated by Eq. (2.6). The block diagram of circulating current control to generate command $v_{\Delta j}$ is based on Eq. (2.6), as shown in Fig. 2.13 (a).

$$ {i_{uj}}'' = {i_{lj}}'' = \frac{1}{3} I_{dc} + i_{cj} \tag{2.5} $$

$$ v_{\Delta j} = 2 L_S \frac{d(\frac{1}{3} I_{dc} + i_{cj})}{dt} = 2 L_S \frac{d\, i_{cj}}{dt} \tag{2.6} $$

In superposition theorem, the response of elements to all the sources in electrical circuit is equivalent to the sum of response in several sub circuit where sources singly functions. Here we can derive the actual stack currents from the AC side and DC side equivalent models in Fig. 2.10 and Fig. 2.12. Based on Eq. (2.1) and Eq. (2.5), Eq. (2.7) holds.

$$ \begin{cases} i_{uj} = {i_{uj}}' + {i_{uj}}'' = \dfrac{1}{3} I_{dc} + i_{cj} + \dfrac{1}{2} i_j \\ i_{lj} = {i_{lj}}' + {i_{lj}}'' = \dfrac{1}{3} I_{dc} + i_{cj} - \dfrac{1}{2} i_j \end{cases} \tag{2.7} $$

Thus, Eq. (2.8) can be derived and the circulating current controller is updated according to Eq. (2.8), as is shown Fig. 2.13 (b).

$$ i_{cj} = \frac{1}{2} (i_{uj} + i_{lj}) - \frac{1}{3} I_{dc} \tag{2.8} $$

From Fig. 2.12 the voltages can also be derived as Eq. (2.9). Suppose that the upper stack voltage and lower stack voltage are equal, Eq. (2.10) holds.

$$ {v_{uj}}'' + {v_{lj}}'' + v_{\Delta j} = V_{dc} \tag{2.9} $$

$$ {v_{uj}}'' = {v_{lj}}'' = \frac{1}{2} V_{dc} - \frac{1}{2} v_{\Delta j} \tag{2.10} $$

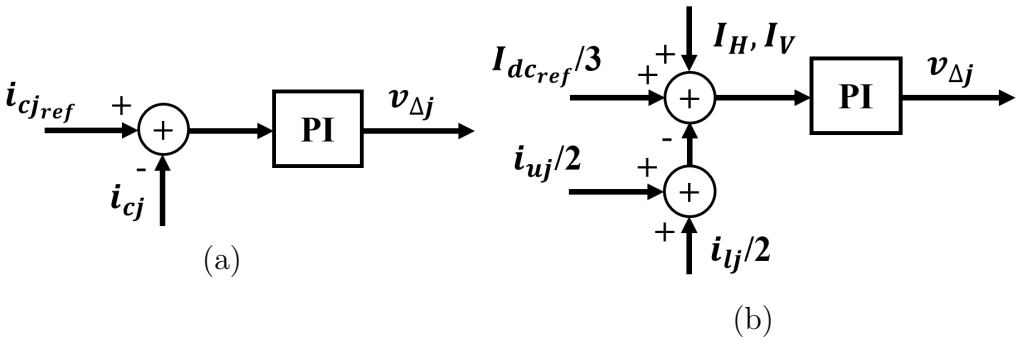


Figure 2.13: Block diagram of circulating current controller

According to Eq. (2.1) and Eq. (2.10), voltages are synthesized to form the stack voltage reference, as shown in Eq. (2.11), and to be fed into the low level controller.

$$\begin{cases} v_{uj} = v_{uj}' + v_{uj}'' = \dfrac{1}{2} V_{dc} - \dfrac{1}{2} v_{\Delta j} - v_j \\ v_{lj} = v_{lj}' + v_{lj}'' = \dfrac{1}{2} V_{dc} - \dfrac{1}{2} v_{\Delta j} + v_j \end{cases} \tag{2.11}$$

LQR based State Feedback Control

State Space Model can not only reflect the internal states of the system, but also reveal the relationship between the internal states and the external input and output variables [103, 104, 105]. Multiple variable time series are converted into vector time series, which is more suitable for solving the modeling problem in the case of Multi-Input Multi-Output (MIMO) variables. Consequently, State Space Model is widely used to describe the dynamics of power electronics circuits. A quadratic state-space modeling technique, which hybridizes the advantages of simulating circuit topology at circuit level and topology determination at device level is presented in [106] for analysis of power electronic converters. Besides, in [107] a new switching-cycle state-space model of the MMC is proposed. For the modeling of grid connected voltage source converter, [108] presents a modular state-space modeling framework that can model different control loops separately as building blocks. Moreover, many works implement linear quadratic regulator (LQR) into the state space model to achieve certain control objectives. Reference [109] reviews the LQR control for switching converters and presents a linear

matrix inequalities (LMI) based LQR controller for PWM converters. Then, applying converter loss equation as cost function, the LMI based controller proposed in [110] has effectively saved energy in boost converter.

LQR based state feedback control can take over the role of DQ and circulating current controll as current contoller. Regarding the model shown in Fig. 2.1, the dynamics of MMC are described by a set of loop voltage ordinary differential equations with $j = a, b, c$:

$$\begin{cases} u_j + L_P \dfrac{di_j}{dt} + L_S \dfrac{di_{uj}}{dt} + v_{uj} - \dfrac{1}{2} V_{dc} = 0 \\ u_j + L_P \dfrac{di_j}{dt} - L_S \dfrac{di_{lj}}{dt} - v_{lj} + \dfrac{1}{2} V_{dc} = 0 \end{cases} \tag{2.12}$$

As has been derived in the former section, AC current $i_j = i_{uj} - i_{lj}$, and circulating current $i_{cj} = \dfrac{1}{2} i_{uj} + \dfrac{1}{2} i_{lj}$. Stack currents ($i_{uj}$, i_{lj}), stack voltages (v_{uj}, v_{lj}), AC and DC voltage sources (u_j, V_{dc}), and the current references (i_j^*, i_{cj}^*) from high level control are identified as state x, control inputs u, disturbance u_d and output y, respectively. The dynamics can be rewritten into standard state space model (2.13).

$$\begin{cases} \dot{x} = Ax + Bu + B_d U_d \\ y = Cx + Du + D_d U_d \end{cases} \tag{2.13}$$

where x, u, u_d and y are represented by $x = [i_{ua}\ i_{la}\ i_{ub}\ i_{lb}\ i_{uc}\ i_{lc}]'$, $u = [v_{ua}\ v_{la}\ v_{ub}\ v_{lb}\ v_{uc}\ v_{lc}]'$, $u_d = [u_a\ u_b\ u_c\ V_{dc}]'$ and $y = [i_a\ i_{ca}\ i_b\ i_{cb}\ i_c\ i_{cc}]'$, respectively. From Eq. (2.12) the coefficient matrixes A, B, B_d, C, D and D_d can be derived.

In steady state, state $x = x_{ss}$ and controller input $u = u_{ss}$, the control formula can be obtained as $u = u_{ss} - K(x - x_{ss})$. The output of the current controller is supposed to be equal to current references obtained from higher level control. To achieve this, $x_{ss} = N_x\, r_{ss} + N_{dx}\, u_{dss}$ and $u_{ss} = N_u\, r_{ss} + N_{du}\, u_{dss}$ hold. Consider that x_{ss} =0, $y_{ss} = r_{ss}$ and combine the former mentioned equations with Eq. (2.13), Eq. (2.14) holds:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} N_x & N_{dx} \\ N_u & N_{du} \end{bmatrix} = \begin{bmatrix} 0 & -B_d \\ I & -D_d \end{bmatrix} \tag{2.14}$$

When LQR is applied, the block diagram of LQR based state feedback control is presented in Fig. 2.14.

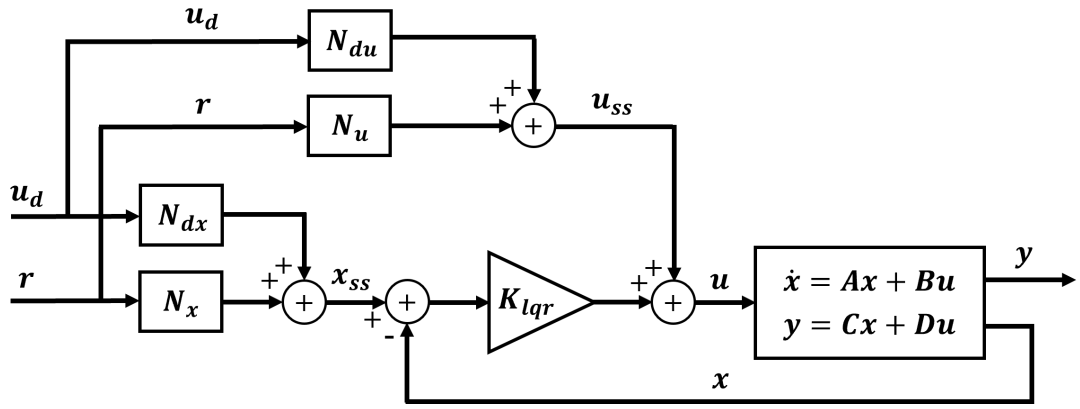


Figure 2.14: LQR based state feedback control

LQR is an optimal controller of linear system state feedback, which is easy to implement in the digital controller. The performance objective function J that should be minimized is calculated by the integral of the quadratic function of the state variable and the control variable, as demonstrated by Eq. (2.15).

$$J = \int_0^\infty (x'Qx + u'Ru + 2\,x'Nu)dt \tag{2.15}$$

where Q and R are the weight matrices for states and inputs, respectively. The cross term matrix N is set to zero in the model applied in this thesis.

2.3.4 Low-Level Control

The objective of low level control is to keep the stack voltage output tracking the voltage reference, and in the meantime, minimise the SM capacitor voltage differences. In conventional MMC, the objective is realised by periodically choosing certain SMs to be inserted into the conducting circuit. As illustrated in Fig. 2.15, stack voltage references are divided by the average SM capacitors voltages in a stack to calculate the modulation index, denoted as N_k. SMs are sorted by capacitor voltages, and the sorting index is ordered from low to high. Then the direction of stack current engages and updates the sorting index into inserting order V_{Sort}. The switching state of each SM and the gate signals of semiconduc-

tors can be simply acquired by comparing V_{Sort} with N_k and applying NLM plus PWM [111]. This algorithm requires accurate and real-time SM voltage monitoring, causing the complexity of the voltage measurement and control system to increase exponentially with the amount of SM quantity. This issue becomes more serious when a large number of SMs are needed in MMC for HVDC applications.

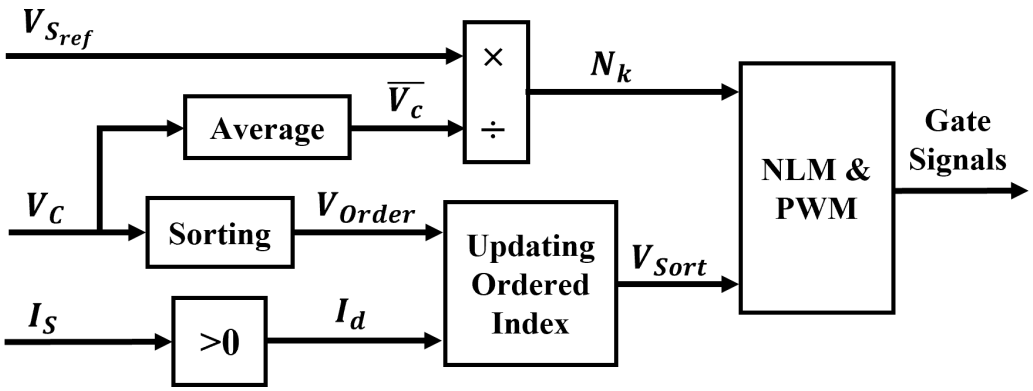


Figure 2.15: Low level control of a conventional MMC

2.4 Case Study

This section presents the simulation results of a FBSM MMC operating under the above introduced control framework. The simulation model based on the topology presented in Fig. 2.1 is built in MATLAB/Simulink. Each stack is designed to contain 15 FBSMs in order to evaluate the performances of the MMC with the same number of MBSMs. Some important parameters are summarized in Table 2.4.

Table 2.4: Parameters of the Simulation Model

Parameters	Value	Parameters	Value
Nominal Power	50 MVA	DC Voltage	30 kV
AC Voltage (RMS)	15 kV	Nominal V_C	2000V
AC Frequency	50 Hz	MBSM Capacitance	13.9 mF
Phase Inductance	0.15 pu	N_{SM} per Stack	15
Stack Inductance	0.1 pu	PWM Frequency	1 kHz

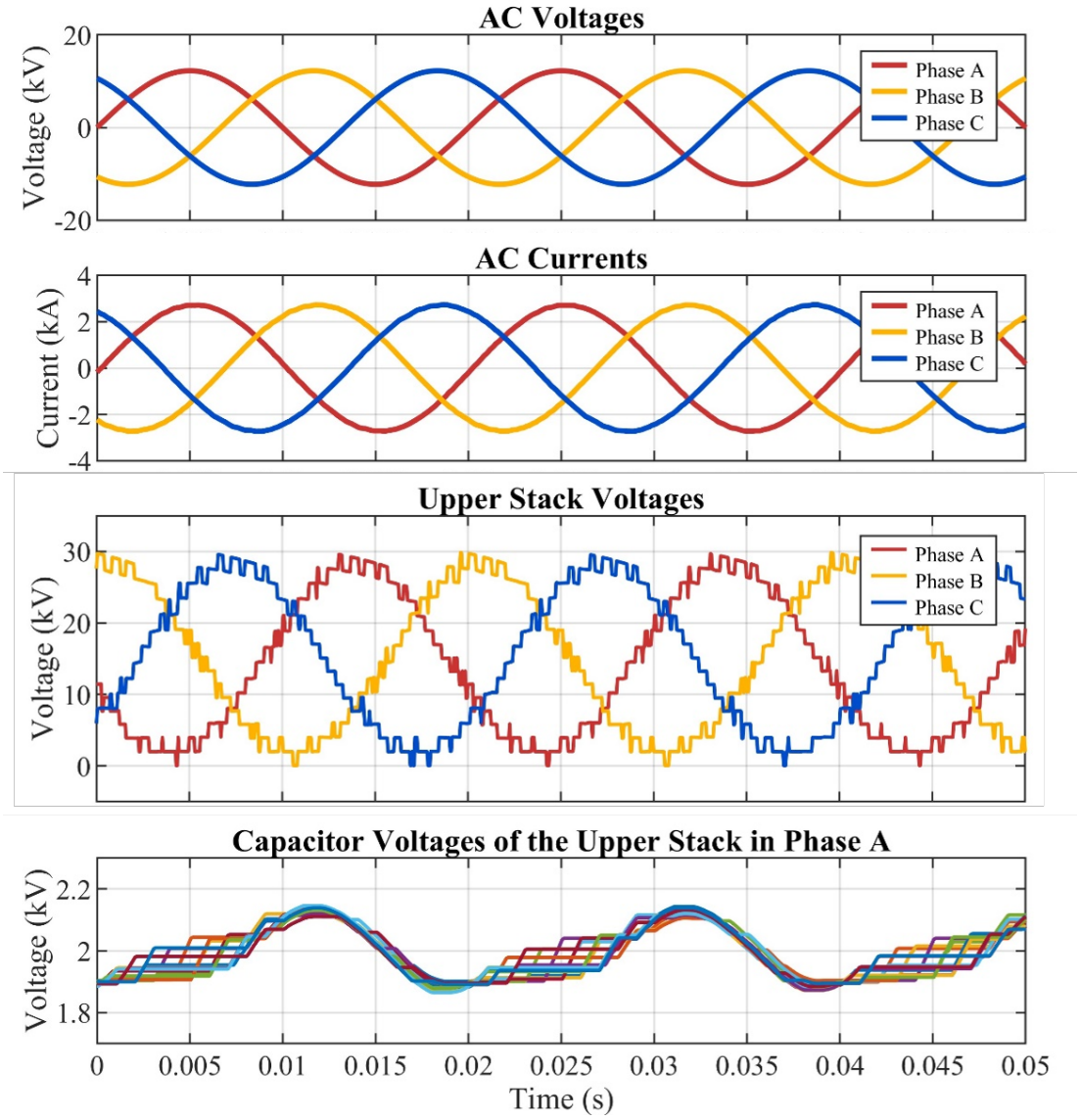


Figure 2.16: Performances of the FBSM MMC under normal operation

2.4.1 Normal Operation of a FBSM MMC

The characteristics reflect a typical scenario of MMC in HVDC converter station. The overall control target is to convert 1 p.u. active power, 50 MW, from the DC side to AC side. The waveforms generated by the FBSM MMC are shown in Fig. 2.16. The AC current presents standard sinusoidal waveform and has the same phase with the AC voltage. Both the power quality and the power factor are ensured. The stack generates staircase voltage. SM capacitor voltages are well balanced under the regulation of the low level control illustrated in Fig. 2.15.The maximum voltage deviation is about 20% of the nomimal capacitor voltage. The

voltage waveform is not marked with its corresponding SM here as what matters is the convergence of all SM voltages in a stack.

2.4.2 Losses Analysis

Generally, power semiconductor devices will see: 1) Switching Losses (P_{sw}) when switching between ON and OFF conditions, and 2) Conduction Losses (P_{cond}) in the ON state. These losses give rise to a temperature rise within the device which must not exceed the permitted junction temperature.

Switching Loss

Switching Loss happens when a semiconductor is switched either on (closed circuit) or off (open circuit). Diodes see reverse recover losses when they stop conducting abruptly because of reverse voltage across their junction. The switching energy and consequently switching power loss depends on the amount of current running through the device at the switching time and switching frequency (i.e. the amount of switching on and switching off times per unit time). Data sheets of semiconductors often provide values for switching energy E_{on} and E_{off}, which will require to be scaled when operating at voltages other than the test condition. Real switching waveform is more complicated but as a standard approximation switching loss is proportional to the current, voltage and switching time. The approximated switching loss of one IGBT/diode is:

$$P_{sw} = f_{sw} \cdot (E_{on} + E_{off}) \tag{2.16}$$

where f_{sw} represents switching frequency. The switching loss is proportional to the switching frequency of semiconductors.

Conduction Loss

If the circuit operates at a known load current then the on-state voltage and conduction loss can be estimated from data sheets as well. The average conduction loss seen by the device will be determined by the instantaneous power loss and

the device duty ratio. The voltage-current dynamics of IGBT and anti-parallel diode are quiet similar and their equivalent power circuits are both composed of series connected DC voltage source and resistor. For simplicity, the IGBT on-state zero-current collector-emitter voltage and the diode on-state zero-current forward voltage are both represented by u_0. Meanwhile, the collector emitter on-state resistance of IGBT and the on-state forward resistance of diode are both represented as r_0. Suppose the instantaneous current is $i(t)$, the instantaneous device voltage $u(t)$ becomes: $u(t) = u_0 + r_0 \cdot i(t)$, and the instantaneous conduction loss $p(t)$ will be:

$$p(t) = u(t) \cdot i(t) = u_0 \cdot i(t) + r_0 \cdot i^2(t)$$

Consequently, the average conduction loss is calculated by:

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p(t)dt = u_0 \cdot I_{aver} + r_0 \cdot I_{rms}^2 \tag{2.17}$$

where I_{aver} is average current, I_{rms} is the rms value of current and T_{sw} represents switching period ($T_{sw} = 1/f_{sw}$). Conduction losses can be reduced by reducing the average current or RMS current of semiconductors.

Losses of the FBSM MMC

Table 2.5: Power losses of the FBSM MMC

Characteristics	Values
IGBT Part Number	FZ1200R33HE3
Averaged Switching Frequency	385.6 Hz
Averaged RMS Current of Semiconductors	478 A
Conduction Loss	534 kW
Switching Loss	284 kW
Total Loss	818 kW
Power Efficiency	98.35 %

The simulation for losses analysis is conducted based on the IGBT module Infineon FZ1200R33HE3. The maximum rated collector-emitter voltage is up to

3300V and the repetitive peak collector current is 1200A. The voltage and current rating makes it capable for the studied scenario. The package type of the IGBT is not considered in this thesis. The power losses and some other characteristics are summarized in Table 2.5. The averaged switching frequency is obtained by monitoring the total switching actions of all IGBTs in one second and divide it by the amount of IGBTs. The results serve as a baseline for evaluating the performance of the MBSM MMC, which will be discussed in the following chapter.

2.5 Summary

The background on MMC is extensively introduced in this chapter. The topology and design of MMC is presented at first. Then different SM topologies are reviewed and compared in terms of cost, complexity, losses and negative voltage capability. The step-by-step modeling and distributed control framework are also summarized. Finally, simulation results of a reduced scaled FBSM MMC are presented to validate the aforementioned control method.

Chapter 3

Multi Busbar Sub-Module MMC

As has been introduced in Section 2.2, SM structures allow both series and parallel module connectivity have many advantages over single busbar structures, such as improving current capability, generating a wide range of output voltage levels, allows wide frequency range operation and sensorless balancing. Despite the benefit of parallel SM design, additional inductors should be connected between two SMs to suppress the inrush current caused by capacitor paralleling [46, 73, 74]. The number of these additional inductors required is twice the number of SMs, resulting in extra converter costs and power losses. This chapter presents the multi-busbar sub-module (MBSM) and the corresponding control algorithm. The detailed soft-parallel mechanism allows capacitors to be paralleled without the requirement of additional inductors. Besides, the failure management and reliability studies are also presented.

3.1 The Multi-Busbar Sub-Module

3.1.1 Topology and Basic States of the MBSM

The structure of HB MBSM and FB MBSM are presented in Fig. 3.1 and Fig. 3.2, respectively. Compared with their single busbar counterparts, MBSMs consist of twice the number of semiconductors. Stack current is divided into two parts (I_{S_1}, I_{S_2}) and flows through two parallel paths. The capacitors of any adjacent SMs can be connected in series as well as in parallel due to the multi busbar structure.

The normally closed bypass switches S_1 and S_2 allow better management during the start-up procedure and in case of SM failures. An MBSM can be bypassed even if the power semiconductors are not able to be activated.

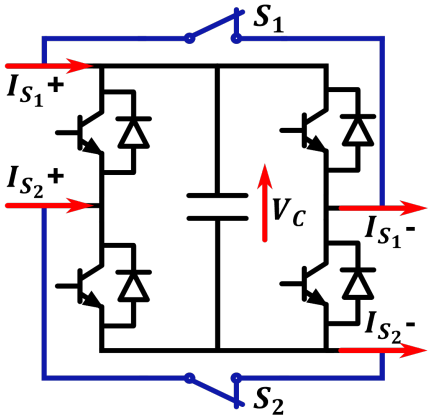


Figure 3.1: Half bridge MBSM topology

In HB MBSM, one of the flow-in busbars is connected directly to the positive side of the capacitor, while one of the flow-out busbars is connected to the negative side of the capacitor. This structure characteristic prevents the former capacitor from connecting its positive side to the latter capacitor's negative side. A stack consisting of HB MBSMs is not able to construct negative stack voltage and, consequently, the HB MBSM MMC is not capable of managing DC side fault. Apart from lacking DC fault management capability, the states, modulation method, and start-up analysis of HB MBSM are quite close to FB MBSM.

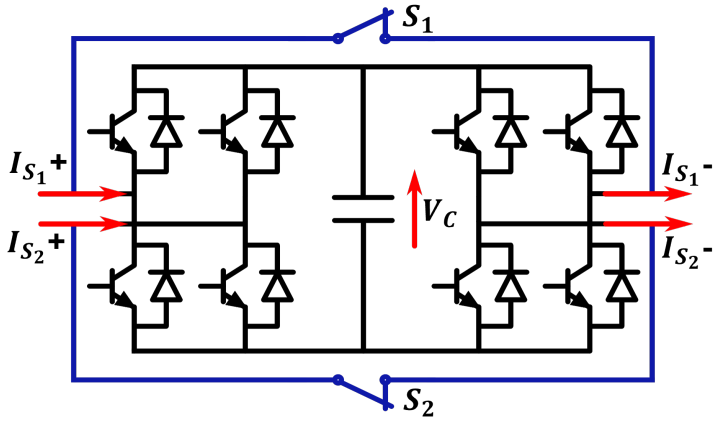


Figure 3.2: Full bridge MBSM topology

The FB MBSM is extensively investigated in this thesis. A stack composed

of two FB MBSMs (marked in the blue block) and most states are presented in Fig. 3.3, in which the external bypass switches S_1 and S_2 are omitted since they stay open during normal operation. The adjacent MBSMs are connected together through two busbars. The stack terminal (in the green block) and interconnections (in the yellow block) are also marked in the figure. When a MBSM is regarded as a controlled object of the low level controller, it can operate as a conventional FBSM with positive voltage state, negative voltage state and zero voltage state [112], as presented in Fig. 3.3 (a1)-(a4). All FBSM oriented control methods can thus be applied to MBSMs.

Apart from being inserted (positively or negatively) or bypassed as similar to FBSMs, two adjacent MBSMs can be parallelized through proper actions of the semiconductors between them. The control targets become the stack terminal and interconnections of two adjacent MBSMs, as paralleling requires joint actions of two adjacent MBSMs. States of MBSMs are consequently defined in two categories: (1) the stack terminal states include series positive, bypass, and series negative, as presented in Fig. 3.3 (b1)-(b4); (2) The interconnections states include series positive, parallel and series negative. Fig. 3.3(c) lists typical interconnection states proposed in previous publications [45, 46, 74]. When the interconnection of two MBSMs is in parallel mode, the capacitors voltage will be equal thanks to the paralleling of capacitors. Voltage balancing can thus be achieved. Notice that additional inductors should be connected in the conduction paths to avoid the inrush current and extra capacitor paralleling loss resulting from the paralleling of two capacitors with a voltage difference, as presented in Fig. 3.3(c3) and Fig. 3.3(c4). The series positive and series negative states correspond to the situation where the desired MBSM voltage output is positive capacitor voltage and negative capacitor voltage, respectively. When the MBSM is desired to output zero voltage, stack terminals are switched to bypass states and interconnections are in parallel states.

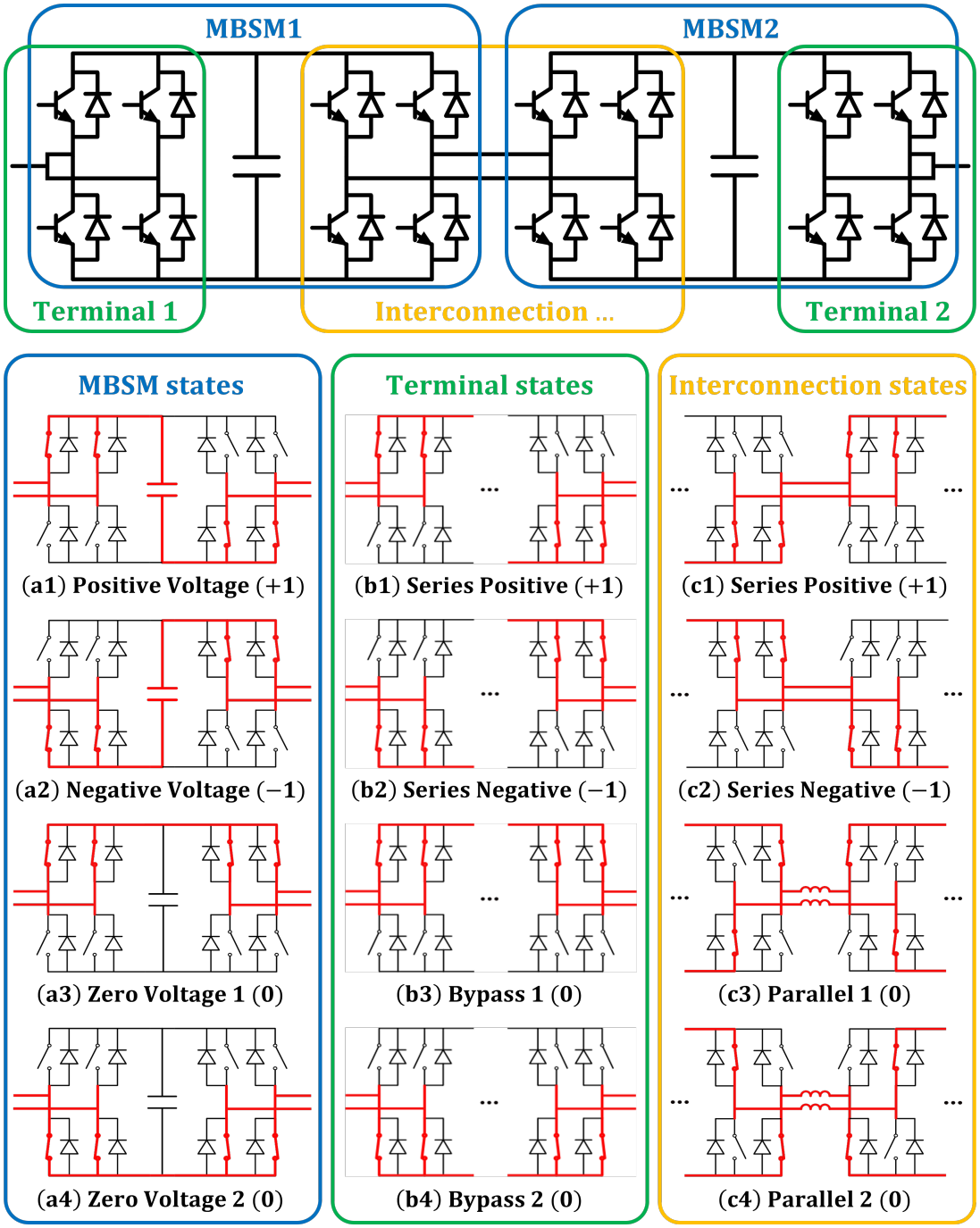
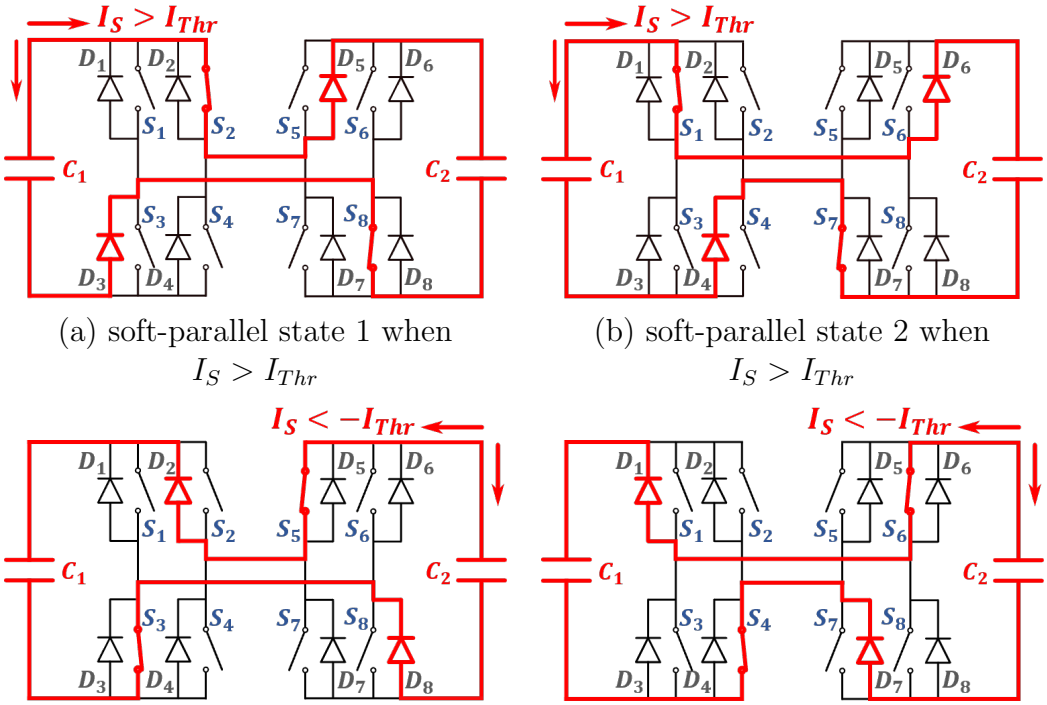


Figure 3.3: Structure of a stack constructed by two FB MBSMs and states of MBSMs



(a) soft-parallel state 1 when $I_S > I_{Thr}$

(b) soft-parallel state 2 when $I_S > I_{Thr}$

(c) soft-parallel state 1 when $I_S < -I_{Thr}$

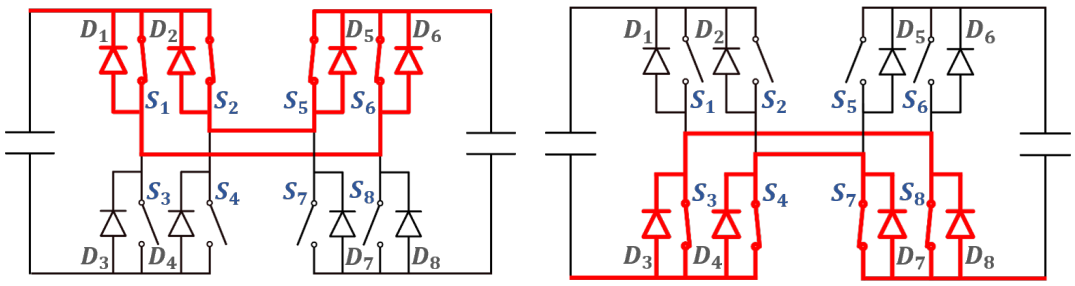
(d) soft-parallel state 2 when $I_S < -I_{Thr}$

Figure 3.4: Soft parallel States of the interconnection, semiconductors, and corresponding current paths in full-bridge MBSM

3.1.2 Soft-Paralleling of MBSM Capacitors

Fig. 3.3 (c3) and (c4) show the parallel states of two adjacent FB MBSMs. When there are more than two MBSMs in a stack, MBSM capacitors are periodically parallelized during normal operation to maintain voltage balancing. However, if two capacitors with large voltage difference are paralleled directly, the inrush charging balance current would be large. Implementing additional port inductors [73, 46] in the conduction circuit can help suppress inrush current, but at the cost of increasing system complexity, additional cost and losses, and converter footprint.

The proposed soft-parallel mechanism makes full use of the directional conduction characteristics of anti parallel power diode. The current paths and semiconductor states in the soft-parallel state of FB MBSMs are illustrated in Fig. 3.4. Two current paths are constructed respectively to connect the positive polar and negative polar of capacitors C_1 and C_2 in two adjacent MBSMs. Stack current



(a) bypass state 1 when $|I_S| \leq I_{Thr}$ (b) bypass state 2 when $|I_S| \leq I_{Thr}$

Figure 3.5: Bypass states of the interconnection, semiconductors, and corresponding current paths in full-bridge MBSM

will dynamically select one path to charge the capacitor with lower voltage, or discharge the capacitor with higher voltage, until achieving voltage balance. Hence not only is inrush current limited in the envelope formed by the stack current I_S, but also the direct parallel connection of capacitors is avoided. The activation of specific soft-parallel states is determined by the instantaneous stack current. Thanks to the characteristics of diodes, current will automatically choose one path to charge the capacitor with a lower voltage until achieving voltage balance if $V_{C_1} \neq V_{C_2}$. In addition, a positive value I_{Thr} is set as the current threshold to provide the margin for states transition in order to compensate the current measurement error and potential delay resulted by communications. Bypass states, as shown in Fig. 3.5 (a) and (b), will replace soft-parallel states if the absolute value of stack current is smaller than the current threshold ($|I_S| \leq I_{Thr}$). The set of bypass states also help on avoid the diodes to prevent the arm current changing direction — besides low current magnitude means that capacitor voltage deviation would be small anyway.

In Fig. 3.4, $I_S > I_{Thr}$ and $I_S < -I_{Thr}$ represent stack current flows from left to right and the opposite direction, respectively. Capacitor voltages of C_1 and C_2 are denoted as V_{C_1} and V_{C_2}. Take the soft-paralleling state 1 when $I_S > I_{Thr}$, as is shown in Fig. 3.4 (a), as an example, semiconductors S_2 and S_8 are switched on. If $V_{C_1} > V_{C_2}$, stack current will flow via S_2, D_5 and charge into C_2 as the anode of D_5 is positive relative to its cathode. While $V_{C_1} < V_{C_2}$, D_3 will be activated and the actual current path becomes $C_1 \rightarrow D_3 \rightarrow S_8$. C_1 are charged to reduce the voltage difference. Notice that semiconductor states in Fig. 3.4 (a)

Table 3.1: Semiconductor states in the soft-parallel based mode

Desired States	Measured Conditions	Interconnection States	Naturally Conditions	Semiconductor state							
				1	2	3	4	5	6	7	8
Soft-parallel (0)	$I_S > I_{Thr}$	Fig. 3.4 (a)	$V_{C1} > V_{C2}$	0	S_2*	D_3	0	D_5*	0	0	S_8
			$V_{C1} < V_{C2}$	0	S_2	D_3*	0	D_5	0	0	S_8*
		Fig. 3.4 (b)	$V_{C1} > V_{C2}$	S_1*	0	0	D_4	0	D_6*	S_7	0
			$V_{C1} < V_{C2}$	S_1	0	0	D_4*	0	D_6	S_7*	0
	$I_S < -I_{Thr}$	Fig. 3.4 (c)	$V_{C1} > V_{C2}$	0	D_2	S_3*	0	S_5	0	0	D_8*
			$V_{C1} < V_{C2}$	0	D_2*	S_3	0	S_5*	0	0	D_8
		Fig. 3.4 (d)	$V_{C1} > V_{C2}$	D_1	0	0	S_4*	0	S_6	D_7*	0
			$V_{C1} < V_{C2}$	D_1*	0	0	S_4	0	S_6*	D_7	0
Bypass (0)	$\|I_S\| \leq I_{Thr}$	Fig. 3.5 (a)	$I_S > 0$	S_1	S_2	0	0	D_5	D_6	0	0
			$I_S < 0$	D_1	D_2	0	0	S_5	S_6	0	0
		Fig. 3.5 (b)	$I_S > 0$	0	0	D_3	D_4	0	0	S_7	S_8
			$I_S < 0$	0	0	S_3	S_4	0	0	D_7	D_8
Series Positive (+1)		Fig. 3.3 (c1)	$I_S > 0$	0	0	D_3	D_4	D_5	D_6	0	0
			$I_S < 0$	0	0	S_3	S_4	S_5	S_6	0	0
Series Negative (+1)		Fig. 3.3 (c2)	$I_S > 0$	S_1	S_2	0	0	0	0	S_7	S_8
			$I_S < 0$	D_1	D_2	0	0	0	0	D_7	D_8

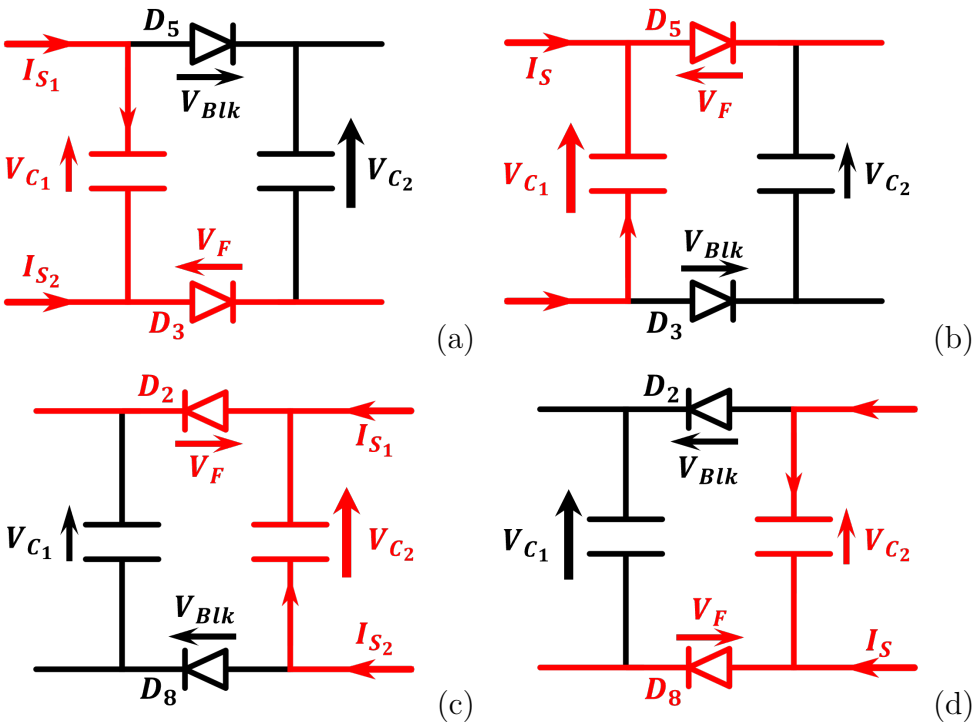


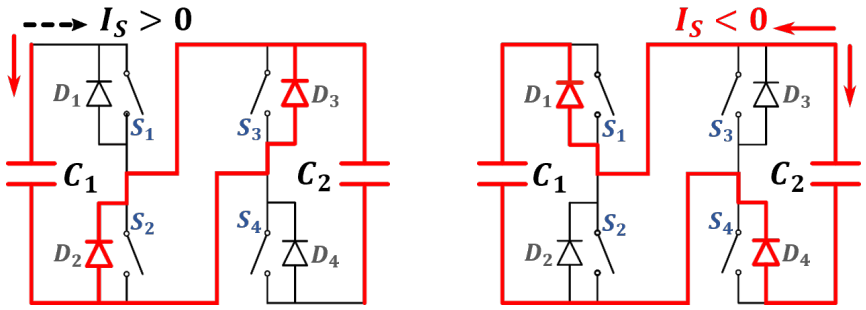
Figure 3.6: Equivalent circuits of the soft parallel states: (a) when $V_{C_1} < V_{C_2}$ as in Fig. 3.4 (a); (b) when $V_{C_1} > V_{C_2}$ as in Fig. 3.4 (a); (c) when $V_{C_1} < V_{C_2}$ as in Fig. 3.4 (c); (d) when $V_{C_1} > V_{C_2}$ as in Fig. 3.4 (c).

and in Fig. 3.4 (b) are different yet the same effect can be achieved. Similar performance can be found in Fig. 3.4 (c) and in Fig. 3.4 (d). By alternating between the equivalent states, average current, losses, and junction temperature rise are distributed to different semiconductors within a MBSM evenly.

All semiconductor states and the conditions to determine them in the soft parallel based mode are listed in Table 3.1. In all soft-parallel states, characters with $*$ represent current flowing through the corresponding semiconductor, either diode or IGBT; characters without $*$ represent the semiconductor is activated to form parallel path but no current is passing through. To further explain the principle of the soft-parallel mechanism and how it suppress inrush current, the equivalent simplified circuit of Fig. 3.4 (a) and Fig. 3.4 (c) in both voltage conditions are all presented in Fig. 3.6. In Fig. 3.6 (a), stack current flows through D_3 while D_5 is reverse blocked so no current is passing. The reverse voltage of D_5 can be describe by: $V_{Blk} = V_{C_1} - V_{C_2} - V_F$, in which V_F is the diode forward voltage. The capacitor charging current is equal to the stack current and no inrush

current or capacitor parallel loss is generated as the capacitor voltage difference is clamped by D_5. Similar analysis can be conducted to the circuit shown in Fig. 3.6 (b), Fig. 3.6 (c), and Fig. 3.6 (d). Fig. 3.6 (d) shows the condition when the stack current direction is negative and $V_{C_1} > V_{C_2}$, D_2 is reverse blocked and stack current flows through D_8 to the cathode of C_1, reducing the voltage difference by discharging the capacitor with higher voltage.

The direction of the stack current changes in an operation cycle. Whenever the current direction or the relative magnitude of capacitor voltages is changed, the conducting semiconductor device changes, as indicated by Table 3.1. As a result, semiconductors in different busbars take turns conducting current whether the relative magnitude of V_{C_1} and V_{C_2} changes or not in a cycle. So, the RMS current passing through a semiconductor is half of that in a single busbar SM when observing a whole cycle though the semiconductor should tolerate the whole instantaneous current. The reduction of RMS current leads to a reduction in power losses and temperature rises.



(a) current in positive direction (b) current in negative direction

Figure 3.7: Soft parallel states of half-bridge MBSM

As for HB MBSM, the circumstance is different because there is always a busbar connected directly to the capacitor without passing any semiconductors or diodes. When $I_S > 0$, it is impossible to construct current paths for soft-paralleling, as shown in Fig. 3.7 (a). Only when $I_S < 0$, with all the semiconductors blocked, path via $D_1 \rightarrow C_1$ and path via $C_2 \rightarrow D_4$ are applied to flattening the voltage difference between C_1 and C_2, as presented in Fig. 3.7 (b). Analysis for the HB MBSM will not be extended as the thesis focus on the FB MBSM.

3.1.3 Low Level Control for MBSM Stacks

On-time voltage measurement is not necessary in the low level control of the MBSM MMC as voltage balancing is maintained by periodically soft-paralleling. Similar to the state definition, the modulation framework aims at stack terminals and interconnections as well. Suppose each MMC stack has N_{SM} MBSMs, then N_{SM} triangular Phase Shift Carrier (PSC) [113] waves ($C(i)$) are assigned to the stack terminal and $N_{SM}-1$ interconnections. The expected states are determined by N_{ref} ($= V_{S_{ref}}/\sum V_C$) and the carriers $C(i)$ where $V_{S_{ref}}$ is the stack voltage reference, and V_C is nominal capacitor voltage.

$$State(i) = \begin{cases} 1,\ if\ \ \dfrac{V_{S_{ref}}}{N_{SM}\cdot V_C} > C(i) \\ -1,\ if\ \ \dfrac{V_{S_{ref}}}{N_{SM}\cdot V_C} \leq -C(i) \\ 0,\ if\ \ C(i) \geq \dfrac{V_{S_{ref}}}{N_{SM}\cdot V_C} > -C(i) \end{cases} \tag{3.1}$$

Semiconductor states of stack terminals are determined by Fig. 3.3 (b1), Fig. 3.3 (b2), and Fig. 3.3 (b3) (or Fig. 3.3 (b4)). State = 1, -1, 0 represent series positive, series negative, and bypass, respectively. For interconnections, semiconductor states are determined by Table 3.1. State = 1, -1, 0 represent series positive, series negative, and soft-parallel, respectively. The specific soft-parallel state is also determined by the stack current. The PSC framework allows adjacent capacitors to be soft-paralleled successively, and consequently SM voltage balancing is achieved.

Fig. 3.8 demonstrates applying PSC modulation framework to determine one terminal state and three interconnection states of a stack contains four MBSMs. $C(1)$, $C(2)$, $C(3)$, and $C(4)$ correspond to interconnection 1, interconnection 2, interconnection 3, and the terminal, respectively. The equivalent capacitor states and stack voltage outputs at $t = t_1$, t_2, t_3, t_4, and T are summarized in Table 3.2:

(1) At $t = t_1$, N_{ref} is larger than all carriers. All interconnections and the terminal are in series positive state, as presented in Fig. 3.3 (b1) and Fig. 3.3 (c1). The stack voltage is equal to $+4V_C$.

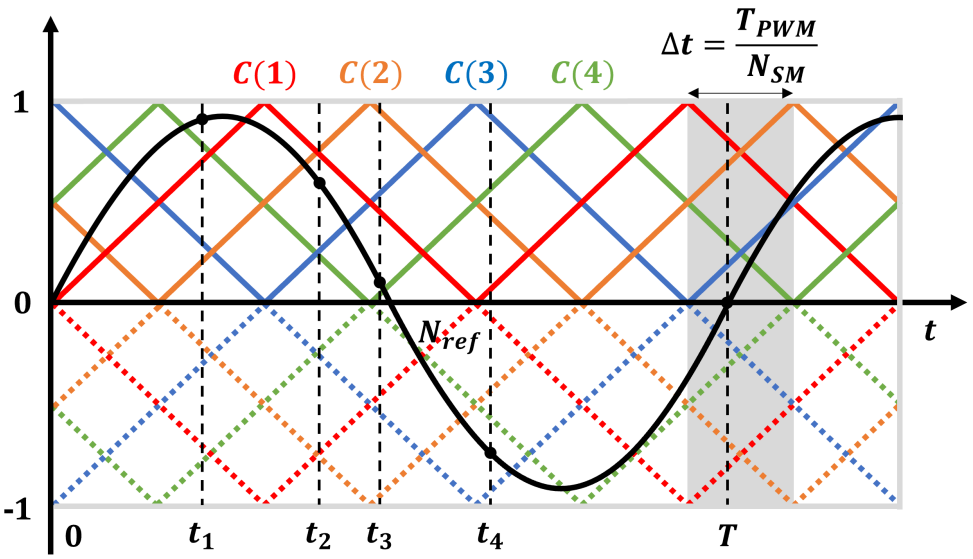


Figure 3.8: Phase shift carrier modulation for a stack contains four MBSMs.

(2) At $t = t_2$, $-C(1) \leq N_{ref} < C(1)$, $-C(2) \leq N_{ref} < C(2)$, $N_{ref} > C(3)$, and $N_{ref} > C(4)$. Interconnection 1 and interconnection 2 are in soft-parallel state, as presented in Fig. 3.4, Interconnection 3 and the terminal are in series positive state, as presented in Fig. 3.3 (b1) and Fig. 3.3 (c1). The stack voltage is equal to $+2\,V_C$.

(3) At $t = t_3$, $-C(1) \leq N_{ref} < C(1)$, $-C(2) \leq N_{ref} < C(2)$, $-C(3) \leq N_{ref} < C(3)$, and $N_{ref} > C(4)$. All interconnections are in soft-parallel state, as presented in Fig. 3.4. The terminal is in series positive state, as presented in Fig. 3.3 (b1). The stack voltage is equal to $+V_C$.

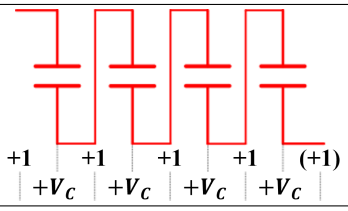
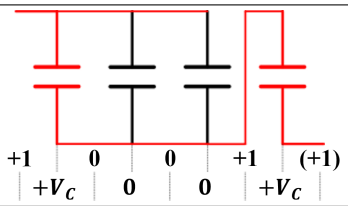
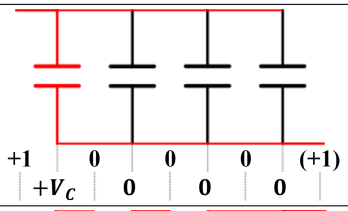
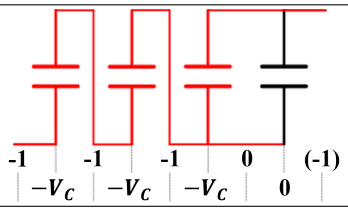
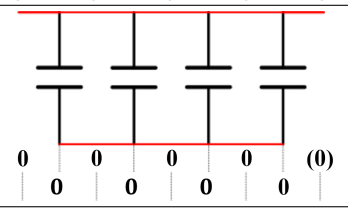
(4) At $t = t_4$, $N_{ref} \leq -C(1)$, $N_{ref} \leq -C(2)$, $-C(3) \leq N_{ref} < C(3)$, and $N_{ref} \leq -C(4)$. Interconnection 1, interconnection 2 and the terminal are all in series negative state, as presented in Fig. 3.3 (b2) and Fig. 3.3 (c2). Interconnection 3 is in soft-parallel state, as presented in Fig. 3.4. The stack voltage is equal to $-3V_C$.

(5) At $t = T$, $-C(1) \leq N_{ref} < C(1)$, $-C(2) \leq N_{ref} < C(2)$, $-C(3) \leq N_{ref} < C(3)$, and $-C(4) \leq N_{ref} < C(4)$. All interconnections are in soft-parallel state, as presented in Fig. 3.4. The terminal is in Bypass state, as presented in Fig. 3.3 (b3) or Fig. 3.3 (b4). The stack voltage is equal to 0.

This case proves that a stack with N_{SM} MBSMs can output voltage from

$-N_{SM}\,V_C$ to $+N_{SM}\,V_C$. Even though each stack contains 15 MBSMs and PWM frequencies are much higher than the frequency of N_{ref} (stack voltage reference frequency) in the simulation model of this chapter, Fig. 3.8 and Table 3.2 still help on explaining the principle.

Table 3.2: Equivalent Capacitor States and stack voltage

Time	N_{ref} [] $C(i)$	Equivalent Capacitor States	Stack voltage
$t = t_1$	$N_{ref} > C(1)$ $N_{ref} > C(2)$ $N_{ref} > C(3)$ $N_{ref} > C(4)$		$+4\,V_C$
$t = t_2$	$-C(1) \leq N_{ref} < C(1)$ $-C(2) \leq N_{ref} < C(2)$ $N_{ref} > C(3)$ $N_{ref} > C(4)$		$+2\,V_C$
$t = t_3$	$-C(1) \leq N_{ref} < C(1)$ $-C(2) \leq N_{ref} < C(2)$ $-C(3) \leq N_{ref} < C(3)$ $N_{ref} > C(4)$		$+1\,V_C$
$t = t_4$	$N_{ref} \leq -C(1)$ $N_{ref} \leq -C(2)$ $-C(3) \leq N_{ref} < C(3)$ $N_{ref} \leq -C(4)$		$-3\,V_C$
$t = T$	$-C(1) \leq N_{ref} < C(1)$ $-C(2) \leq N_{ref} < C(2)$ $-C(3) \leq N_{ref} < C(3)$ $-C(4) \leq N_{ref} < C(4)$		0

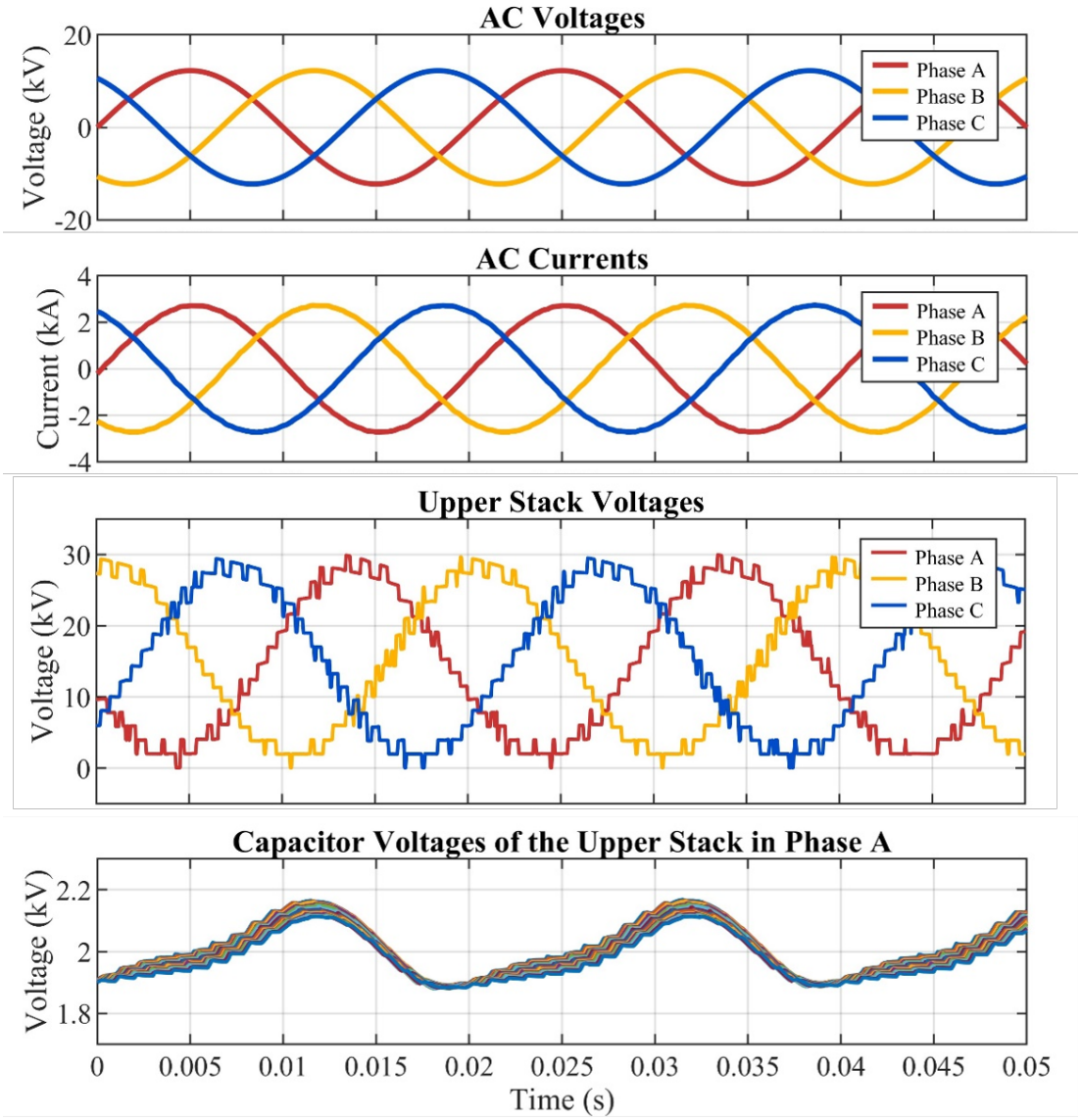


Figure 3.9: Performances of the MBSM MMC under normal operation

3.2 Demonstration of MBSM through Simulation

3.2.1 Normal Operation

The simulation model of the MBSM MMC with the same system parameters as summarized in Table 2.4 is also built in MATLAB/Simulink. The topology is the same as that shown in Fig. 2.1. The performances are compared with those of the conventional FBSM MMC, as shown in Fig. 2.16 on Page 46. The waveforms generated by the MBSM MMC are shown in Fig. 3.9. Both the AC

voltage and AC current present standard sinusoidal waveform with the THD of only 0.22%. The stack generates staircase voltage and the stack current shows sinusoidal waveform with positive offset, which are both typical for MMC stacks. The bottom part of this figure shows capacitor voltages of all MBSMs in one stack. Thanks to the periodically soft paralleling mechanism, capacitor voltages are well balanced among different MBSMs. The power factor of the converter is over 99.96%.

In comparison with the SM capacitor voltages of the FBSM MMC shown in the last figure of Fig. 2.16, MBSMs have lower capacitor voltage deviation than that of FBSMs when the same operation parameters applied. The difference between the MBSM and the conventional FBSM in terms of the THD and the voltage balancing are resulted by their different low level control method. Periodically paralleling of capacitors increased the equivalent capacitance. Consequently, the SM voltage deviation is reduced when the same stack current flows into the capacitor. Less SM voltage deviation further contribute to lower THD of AC voltage.

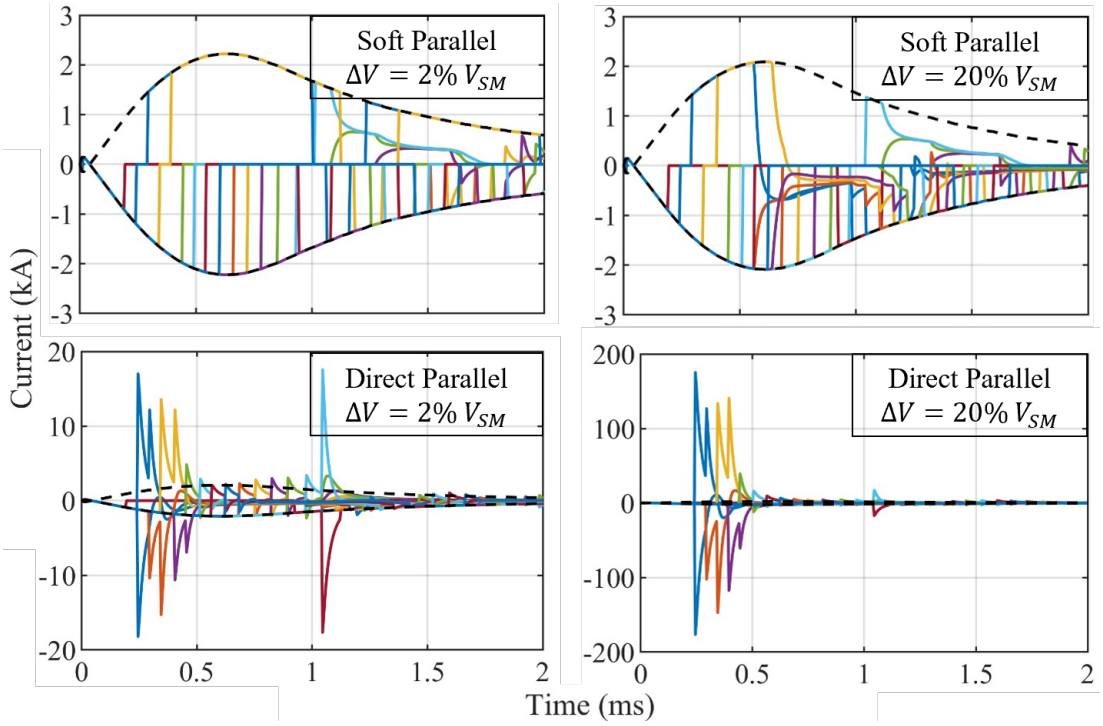


Figure 3.10: Inrush current with and without soft-paralleling (black dashed lines represents the envelope of the stack current;coloured lines represent capacitor currents).

The soft-paralleling mechanism prevents inrush current even when the capacitor voltage difference ΔV is not negligible. Denote $V_{C_{nom}}$ as the nominal capacitor voltage. The inrush currents of all capacitors in one stack when $\Delta V = 2\% V_{C_{nom}}$ and $\Delta V = 20\% V_{C_{nom}}$ are illustrated in Fig. 3.10. Inrush current can still be limited in the envelope formed by the stack current under the regulation of soft-paralleling even when the voltage difference is 400V. If these capacitors are paralleled directly, the inrush current will see about 10 times the increase when $\Delta V = 2\% V_{C_{nom}}$ and more than 200 times when $\Delta V = 20\% V_{C_{nom}}$. Such a large current will cause catastrophic damage to the converter. It should be noted that the IGBT module FZ1200R33HE3, which has been used before in the losses simulation, is NOT used in the demonstration of soft parallel mechanism.

3.2.2 Power Losses Analysis

In addition to switching loss and conduction loss, capacitor Paralleling Losses (P_{para}) also have a great impact on the overall power efficiency of converters where capacitors are periodically paralleled. Therefore, power losses analysis for a IGBT based MBSM MMC are developed from the above mentioned three aspects.

During normal operation, the states transitions of the stack terminal are: Bypass 1 $\Leftrightarrow$ Series Positive $\Leftrightarrow$ Bypass 2, while interconnections states change follows: Parallel 1 $\Leftrightarrow$ Series Positive $\Leftrightarrow$ Parallel 2. Each state transition results in the switching on (or off) of four semiconductors per MBSM. In comparison with its counterpart in conventional MMC, each state transition triggers twice the state change of semiconductors. However, since the current passing each semiconductor is halved, MBSM still shows better switching loss management performance.

In the MBSM MMC, the current passing a power device is half of that in conventional MMC. According to Eq. (2.17), the conduction loss of MBSM is less thanks to the squared term I_{rms}^2.

Capacitor Paralleling Loss

The soft-paralleling mechanism proposed in this paper helps to avoid capacitors being paralleled directly by automatically directing the stack current using the diode natural conduction property. Consequently, no energy is lost when paralleling capacitors, as opposed to other SM topologies proposed in the literature. For context, this capacitor paralleling loss can be substantial if not controlled as the short explanation below demonstrates.

Suppose there are two capacitors with the same capacitance C but different initial voltage (V_1 and V_2). After being parallelized, their equivalent capacitance C_{eq} will be equal to $2C$, and the voltage becomes:

$$V_{eq} = \frac{C \cdot V_1 + C \cdot V_2}{2C} = \frac{V_1 + V_2}{2} \tag{3.2}$$

The energy loss in this process is:

$$E_{para} = (\frac{1}{2}C \cdot V_1^2 + \frac{1}{2}C \cdot V_2^2) - \frac{1}{2}C_{eq} \cdot V_{eq}^2 = \frac{1}{4}C \cdot \Delta V^2 \tag{3.3}$$

where ΔV is the voltage difference of the two capacitors. Then capacitor paralleling loss will be:

$$P_{para} = f_{para} \cdot E_{para} = \frac{1}{4}f_{para} \cdot C \cdot \Delta V^2 \tag{3.4}$$

where f_{para} is the paralleling frequency of MBSMs. Although it is not the same as switching frequency, f_{para} is in positive proportion with f_{sw}. The capacitor paralleling loss is greatly influenced by paralleling frequency and voltage difference. The soft-paralleling method proposed in the previous section help on avoid capacitors being paralleled directly. Thus, the capacitor paralleling loss is eliminated.

Simulation Results for Semiconductor Losses

The losses analysis for the MBSM MMC is also conducted based on the IGBT module FZ 1200R33HE3. The power losses performances of the MBSM MMC

Table 3.3: Power losses of the MBSM MMC

Characteristics	Values	Improvement over the FBSM MMC
Averaged switching frequency	350.8 Hz	-9%
Averaged RMS current	247 A	-48%
Conduction Loss	463 kW	-13%
Switching Loss	219 kW	-23%
Total Loss	682 kW	-17%
Power Efficiency	98.63%	

are compared with the conventional FBSM MMC, whose losses performances are listed in Table 2.5 on Page 48. The higher level control parameters of the two MMC are all set the same as well. Since there are more than one current paths in the MBSM MMC, conduction losses and switching losses are both greatly reduced though the amounts of semiconductors are doubled. The total semiconductor loss has been reduced by approximately 17% while the average semiconductor switching frequency (f_{sw}) has been reduced by 9%, as is shown in Table 3.3. Notice that the averaged RMS current of semiconductors (I_{rms}) are reduced by 48% in the MBSM MMC, indicating simpler cooling design can be applied in an MBSM based MMC.

3.3 Failure Management of MBSM

Multiple busbars provide redundant conduction paths and consequently improve the fault tolerance capability of MBSM-MMC. Under certain failure conditions, the whole MBSM-MMC is still able to operate normally with the faulted MBSMs operating in a degraded mode – requiring only minor adjustments in the low-level control – depending on the type and location of the failures, as described in this section. Therefore, the faulted MBSMs may not need to be deactivated and bypassed while operating in degraded mode. In the event of a full failure of a MBSM (e.g. multiple IGBT failures or capacitor failure), then this MBSM can still be bypassed using the normally-closed bypass switches, as illustrated in

Fig. 3.2, and the converter will rely on the remaining redundant MBSMs to carry on operation. Single semiconductor failure responses and single capacitor failure responses are investigated respectively in Sections 3.3.1 and 3.3.2.

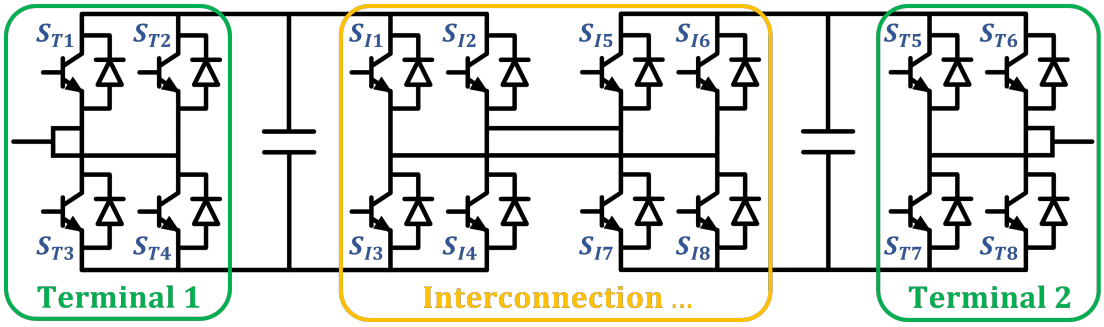


Figure 3.11: Semiconductors in the terminal and interconnections

3.3.1 Semiconductor Failure Responses

Short-Circuit Case

When a semiconductor device fails and becomes a short-circuit, current starts rushing through it. The failure of switches at the terminal and within SM interconnections are analysed separately using the notations of semiconductors marked in Fig. 3.11. Terminal switches (marked as S_{Ti}, $i = 1, 2, ..., 8$) operate in pairs, e.g. S_{Tj} and $S_{T(j+1)}$ ($j = 1, 3, 5, 7$) are always in the same state. For simplicity, the Bypass 1 state (Fig. 3.3 (b3)) and Bypass 2 state (Fig. 3.3 (b4)) of the terminal are represented by $(B1)$ and $(B2)$ respectively in the failure analysis. $(B1)$ and $(B2)$ are redundant and can thus be substituted with each other without affecting the stack's voltage output.

When one of the switches in the pair [S_{T1}, S_{T2}] is short-circuited, the terminal will no longer be able to operate in $(B2)$ state and only switch between Series Positive $(S+)$ and Bypass $(B1)$ states, yet the stack can still generate all $N_{SM}+1$ voltage levels. However, if any of the switches in the pair [S_{T3}, S_{T4}] fails as a short-circuit, the terminal will lose the ability to operate in $(S+)$, which means the stack output voltage cannot reach $N_{SM} \cdot V_C$. Consequently, the terminal in which the faulty switch S_{T3} or S_{T4} are located has to switch into Bypass $(B2)$ state to minimize the negative impacts. Interconnections switches (marked as

Table 3.4: MBSM states responses to semiconductors short circuit failures

Failure Switches	States Responses	Maximum Stack Voltage
S_{T1}, S_{T2}	$(S+) \Leftrightarrow (B1)$	$N_{SM} \cdot V_C$
S_{T3}, S_{T4}	$(B1)$	$(N_{SM}\text{-}1) \cdot V_C$
S_{T5}, S_{T6}	$(B2)$	$(N_{SM}\text{-}1) \cdot V_C$
S_{T7}, S_{T8}	$(S+) \Leftrightarrow (B2)$	$N_{SM} \cdot V_C$
S_{I1}, S_{I7}	$(P2)$	$(N_{SM}\text{-}1) \cdot V_C$
S_{I2}, S_{I8}	$(P1)$	$(N_{SM}\text{-}1) \cdot V_C$
S_{I3}, S_{I5}	$(S+) \Leftrightarrow (P1)$	$N_{SM} \cdot V_C$
S_{I4}, S_{I6}	$(S+) \Leftrightarrow (P2)$	$N_{SM} \cdot V_C$

S_{Ii}, $i = 1, 2, ..., 8$) do not work in pair – as opposed to terminals switches – yet interconnection states Parallel $(P1)$ and $(P2)$ can be substituted by one other as well, as presented in Fig. 3.3 (c3) and Fig. 3.3 (c4). Take a short-circuited S_{I3} as an example, the stack can still work normally since the interconnection still has access to the Series Positive $(S+)$ and Parallel $(P1)$ state. The MBSM states responses to all single semiconductors short circuit failures and their corresponding stack voltage output are listed in Table 3.4.

Open-Circuit Case

When open circuit failure occurs in a semiconductor device, it cannot conduct current any more. If only one switch in terminals is open-circuited, the whole stack can still operate normally without the requirement of adjusting the low-level control as the duty of the failure switch is taken over by the other switch in the same pair.

Table 3.5: MBSM states responses to semiconductors open circuit failure

Failure Switches	States Responses	Maximum Stack Voltage
S_{Ti} $(i = 1, ..., 8)$	$Normal$	$N_{SM} \cdot V_C$
S_{I1}, S_{I4}, S_{I6}, S_{I7}	$(S+) \Leftrightarrow (P1)$	$N_{SM} \cdot V_C$
S_{I2}, S_{I3}, S_{I5}, S_{I8}	$(S+) \Leftrightarrow (P2)$	$N_{SM} \cdot V_C$

For example, if S_{T1} is open-circuited, when the terminal state is $(S+)$ or $(B2)$, current that used to flow through S_{T1} and S_{T2} will all pass through S_{T2}. Neither stack voltage nor stack current is affected if no action is taken on low-level control. But if a semiconductor in interconnection is open-circuited, the interconnection can only switch into one parallel state, either $(P1)$ or $(P2)$. Adjustment should be made in the low-level control to ensure the interconnection remains in the right parallel state rather than switch between $(P1)$ and $(P2)$. Table 3.5 summarizes states responses to all single semiconductor open circuit failures.

3.3.2 Capacitor Failure Responses

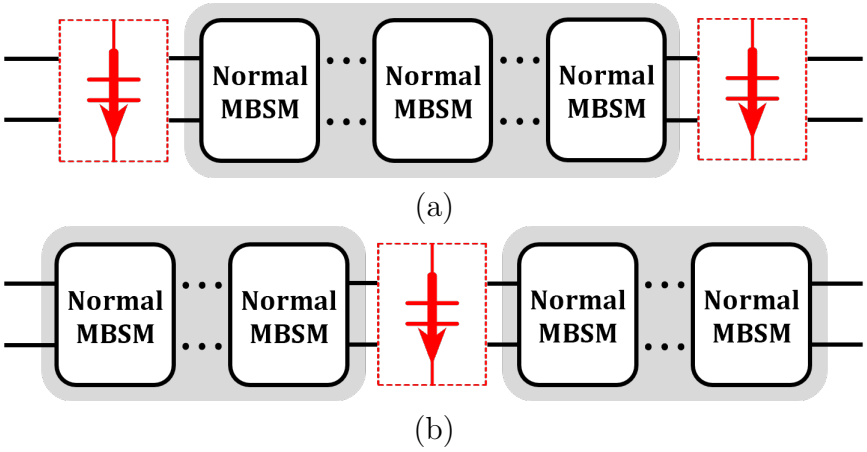


Figure 3.12: Stack responses when capacitor short circuit failure occurs on a: (a) failed head or rear MBSM, (b) failed middle MBSM.

Normally if a capacitor fails, whether open circuit or short circuit, the SM cannot contribute to the stack voltage any more. The converter however still needs to operate with this failed capacitor, at least until the next maintenance round. The following section proposes controllable responses with improved low-level control, providing extra reassurance against the risks caused by capacitor failures.

When a capacitor short-circuit failure occurs, the two poles of the capacitor share the same electric potential. Not only does the short-circuited capacitor lose the ability to construct staircase stack voltage output, but it also provides a current path that connect the positive and negatives poles of parallelized normal

capacitors directly. Under this circumstance, the failure MBSM is seen as a single node with all switches turned off. If the failed MBSM is located in the head or rear of the stack with N_{SM} MBSMs, as shown in Fig. 3.13 (a), the normal MBSMs will constitute a new stack with $N_{SM} - 1$ MBSMs. If the capacitor failure happens in a MBSM some other places in the stack, the stack will then split into two series-connected sub-stacks as illustrated in Fig. 3.13 (b). In both cases, the updated low-level controller uses $N_{SM} - 1$ carriers and determines the states of new stack or sub-stacks.

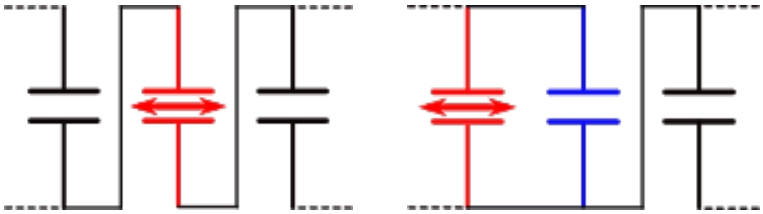


Figure 3.13: Capacitor open circuit failure happens when the MBSM is on: (a) a sole current path, (b) one of multi current paths.

In case of open-circuit failure, the capacitor will no longer be able to conduct electricity. This failure state is more likely as SM capacitors are often of the film types. In this failure mode, the updated low-level control ensures that the open-circuited capacitor is never again in the current path. In other words, the states of the two interconnections – or one terminal and one interconnection if the SM is at the head or rear of the stack – next to the failed MBSM shall not be $(S+)$ simultaneously. In this case, the stack is still able to generate most voltage levels except $N_{SM} \cdot V_C$. The most disruptive situations happen when the capacitor fails open-circuit while the MBSM is contributing to the stack voltage; thus the stack current is flowing through the capacitor at the time of failure as shown in Fig. 3.13. In the case illustrated in Fig. 3.13 (a), the neighboring MBSMs must switch to bypass state (for terminals) or soft-parallel state (for interconnections). In the case illustrated in Fig. 3.13 (b), the state of the stack remains the same with only a reduced equivalent capacitance for the paralleled MBSMs.

3.3.3 Management of Multiple Failures

HVDC converters most certainly have to survive multiple failures during their operating lifetimes. In the case of MBSM, it can be argued that all the MBSM failure management – explained in Sections 3.3.1 and 3.3.2 in the case of single device failure – can be extended to multiple failures. For example, the stack can be split into several sub-stacks in case of multiple IGBT failures in sparsely distributed MBSMs in the stacks.

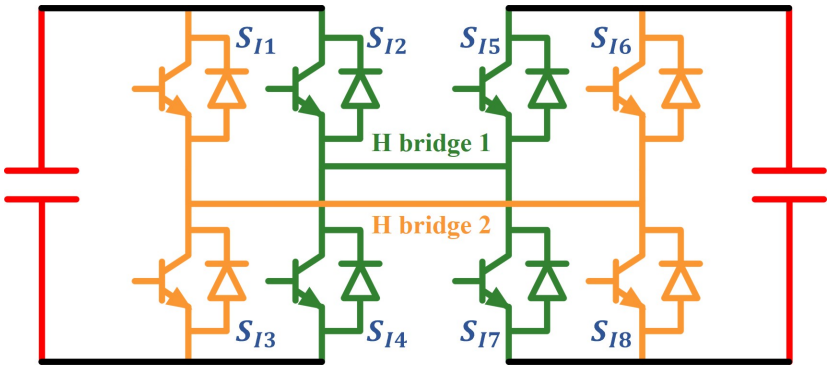
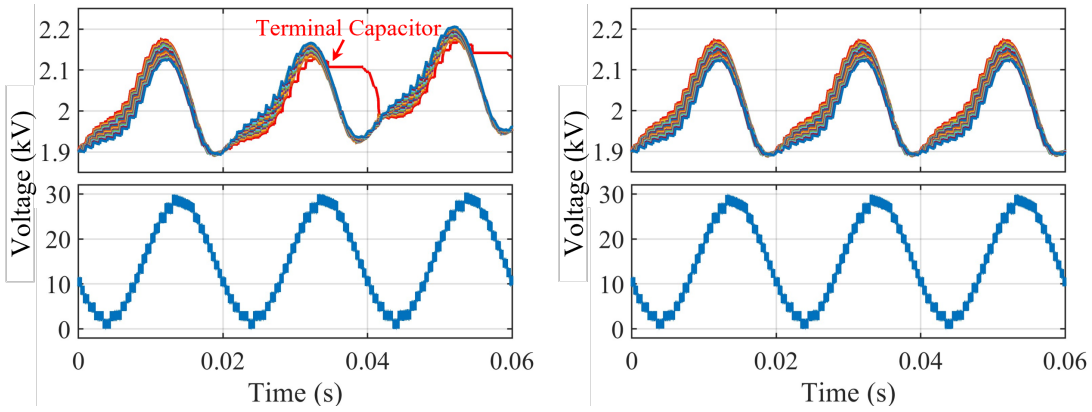


Figure 3.14: The interconnection of a MBSM stack.

The only exception consists in IGBT failures closely connected to each other, e.g. in two neighboring MBSMs. The interconnection of a MBSM stack is actually constructed by two parallel connected H-bridges, as shown in Fig. 3.14. At least one of the H-bridges should be operating to ensure the basic voltage building of the interconnection. In other words, the MBSM tolerates semiconductor failures as long as these failures do not occur on both H-bridges. In case of a single IGBT failure, the MBSM interconnection degrades to a single busbar FBSM interconnection, but essentially remains operative with minor adjustments in the low level control. In case of failures in both H-bridge interconnections, one of the two MBSMs needs to be considered entirely failed and thus bypassed.

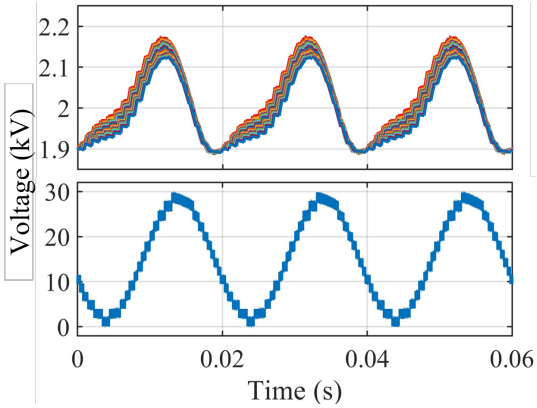
3.3.4 Failure Simulation

The same simulation model as in Table 2.4 is used to simulate all the single failure cases explained in Sections 3.3.1 and 3.3.2. Fig. 3.15 and Fig. 3.16 illustrate the capacitor voltages and stack voltage responses of eight representative failure

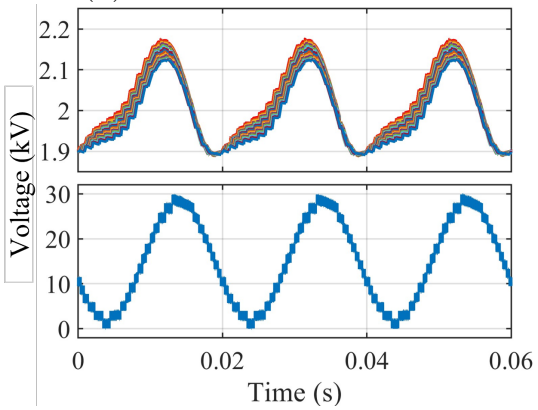


(a) IGBT S_{T3} short circuit

(b) IGBT S_{I5} short circuit



(c) IGBT S_{T1} open circuit

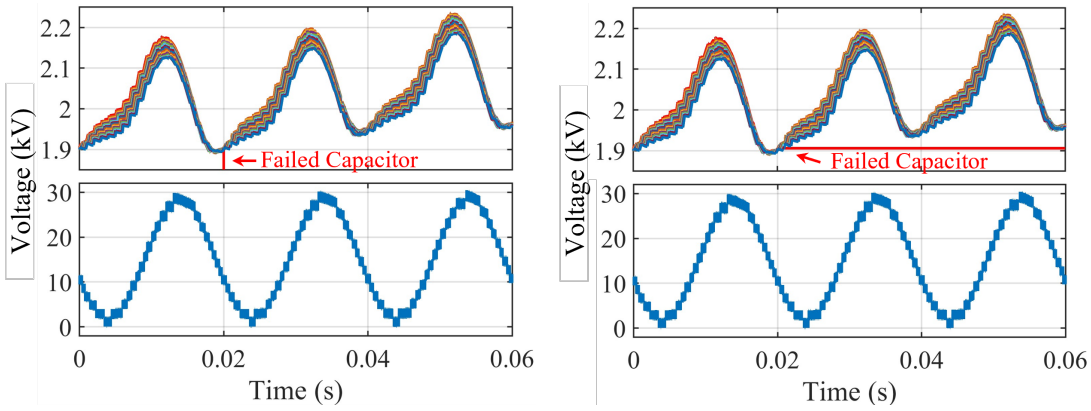


(d) IGBT S_{I7} open circuit

Figure 3.15: Responses of single semiconductor failure in MBSM-MMC.

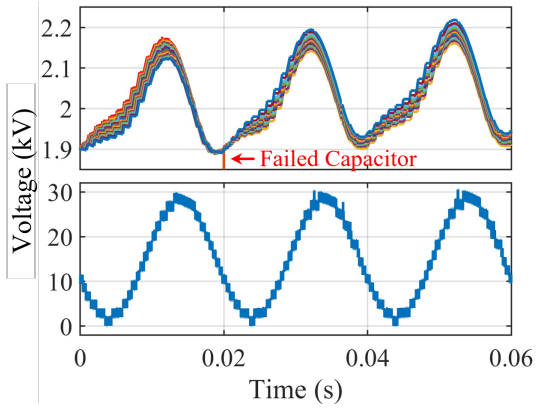
cases, in which failures occur at t = 0.02 s. The converted power qualities are all guaranteed in the eight failure cases with their corresponding fault tolerant low level control. In the case of IGBT S_{T3} short circuit failure (Fig. 3.15 (a)), the terminal capacitor can no longer contribute to stack voltage output yet it is still periodically paralleled to the subsequent capacitor. SM capacitor voltages are still balanced and have increased to another steady state after about 1.5 cycles. The asymmetrical operation of MMC is maintained thanks to stack energy feedback as introduced before. IGBT S_{I5} short circuit failure and IGBT S_{T1} or S_{T3} open circuit failure make no difference to all converter outputs performance, as presented in Fig. 3.15 (b), (c) and (d).

The voltages of the failed capacitors are highlighted in red in Fig. 3.16 (a)–(d). Short circuit capacitor voltages drop to zero while open circuit capacitor voltages remain unchanged after failures occur. The SM voltages and stack voltage performances are similar to those in the case of IGBT S_{T3} short circuit failure. SM

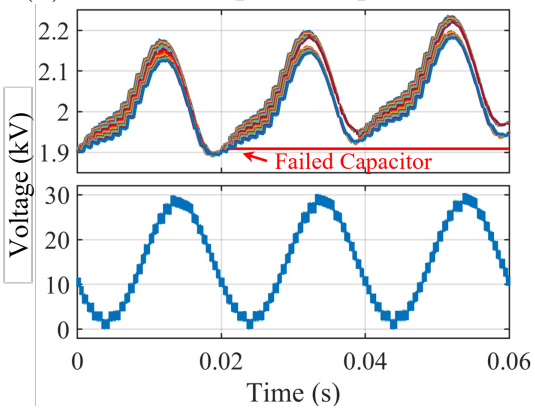


(a) Terminal capacitor short circuit

(b) Terminal capacitor open circuit



(c) Interconnection capacitor short circuit



(d) Interconnection capacitor open circuit

Figure 3.16: Responses of single capacitor failure in MBSM-MMC.

voltages increase to another steady state, and stack voltage references are well tracked with N_{SM} voltage levels (1 voltage level less than the stack voltages in normal operation).

3.3.5 Reliability Study

The availability of a MMC is an important metric for determining its reliability [114, 115]. The availability of a single MBSM and a stack consisting of MBSMs is numerically analysed and compared with that of FBSMs with a rigorous mathematical model derived. If all semiconductors in FBSMs or MBSMs have the same constant failure rate, λ_s. Then, for a single semiconductor, the reliability function is $R_s(t) = e^{-\lambda_s t}$. Normally, the availability of a SM is the product of the reliability of semiconductors, capacitor banks, and SM drive modules [114]. In this paper, the MBSM is compared with the FBSM, which has the same con-

figurations of capacitors and drive modules. Consequently, only the effect of semiconductors needs to be studied here.

Assuming that the condition of a single semiconductor (whether reliable or not) is an elementary event and the condition of different semiconductors are independent and identically distributed. The availability of the MBSM is given by Eq. (3.5). The first term ${R_s}^8$ represents the probability of all eight semiconductors are reliable. The accumulation term in Eq. (3.5) represents the probability of failure occurring in k semiconductors of the same H bridge, so the MBSM is still available. Base on the k-out-of-n model [116], $\binom{1}{2}$ indicates selecting one out of the two H bridges, and $\binom{k}{4}$ indicates selecting k failed semiconductors out of four semiconductors in one H bridge. By no means is a MBSM available if more than four semiconductors fail. In comparison, the FBSM is available only when all four semiconductors work normally, as shown in Eq. (3.6).

$$A_{MBSM}(t) = {R_s}^8 + \sum_{k=1}^{4} \binom{1}{2} \cdot \binom{k}{4} \cdot {R_s}^{8-k} \cdot (1 - R_s)^k \tag{3.5}$$

$$A_{FBSM}(t) = R_s(t)^4 \tag{3.6}$$

Table 3.6: Availability of a single FBSM vs MBSM Sub-Modules

Maintenance Time Interval	FBSM	MBSM
1 year	99.65021%	99.99878%
5 years	98.26326%	99.96984%
10 years	96.55668%	99.88144%
20 years	93.23192%	99.54193%

Periodic preventive maintenance and redundant SMs arrangements are two effective and commonly used approaches to improve the availability of MMC. The operation costs can be reduced with longer maintenance intervals and fewer redundant SMs. A target availability of 99.99% is assumed for a stack within an

Table 3.7: Parameters of the reliability study

Parameters	Value	Parameters	Value
Nominal Power	1,000 MVA	DC Voltage	± 320 kV
AC Voltage (RMS)	400 kV	N_{SM} per Stack	400

MMC, as the same with [115]. According to Eq. 3.5 and Eq. 3.6, the availability of a single FBSM and a single MBSM in different maintenance time intervals are summarized in Table 3.6 with $\lambda_{Sw} = 8.76 \times 10^{-4}$ (int/ year). The availability of the FBSM decreases rapidly with time, while the MBSM remains operational (or at least partly) for longer thanks to the redundant semiconductors.

Table 3.8: Different configurations of redundant SMs for case study

Configuration	SM Type	Level of Redundancy	Target 99.99% Availability
Conf. 1	MBSM	8 extra SMs (2.0%)	19.55 years
Conf. 2	FBSM	8 extra SMs (2.0%)	1.16 years
Conf. 3	FBSM	50 extra SMs (12.5%)	19.22 years
Conf. 4	FBSM	51 extra SMs (12.75%)	19.67 years

Taking the same system parameters (listed in Table 3.7) as in the ElecLink HVDC project [117], the higher availability of a single MBSM translates into a lower requirement for additional redundant MBSMs in the stacks to ensure a satisfactory overall availability of the MMC, as shown in Table 3.8 and Fig. 3.17. The redundancy of 2.0% in a MBSM stack (e.g. just 8 extra MBSMs per stack) is equivalent to that of 12.5% in a FBSM stack (e.g. about 50 extra FBSMs per stack). With such a low level of required redundancy (i.e. saved capital and running costs) and longer maintenance intervals (i.e. reduced downtime) required for an MBSM-based MMC, the increased costs caused by doubled semiconductors can be easily offset.

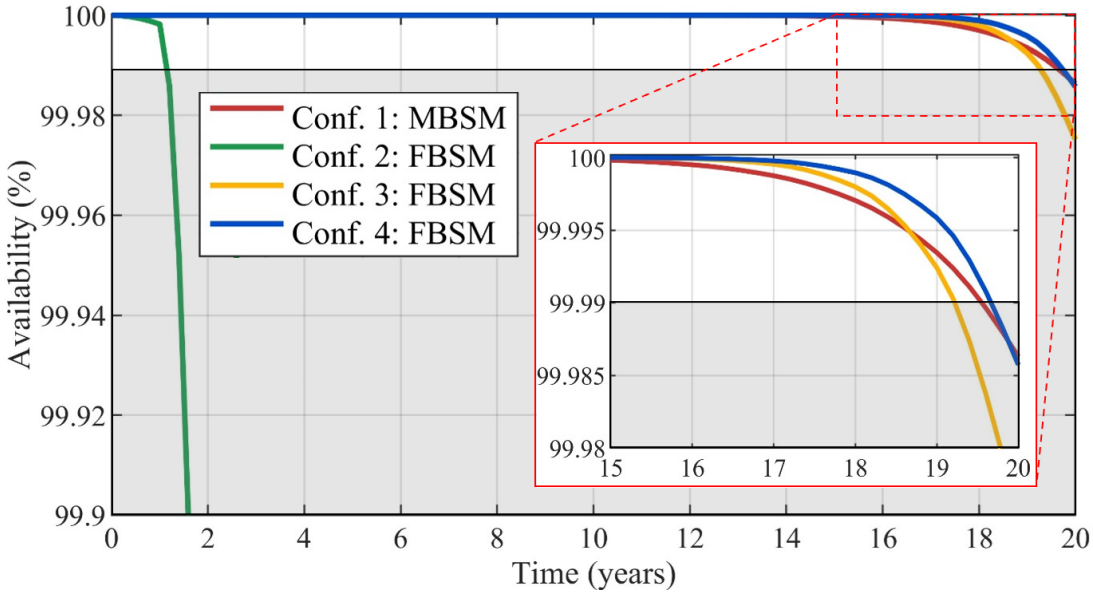


Figure 3.17: Availability for the configurations listed in Table 3.8

3.4 Discussion

The results from Section 3.2.2 on losses and Section 3.3.5 on converter reliability could be combined to extrapolate on the overall power efficiency of a fully-equipped MMC based on either FBSM or MBSM technology.

Taking the figures from Table 3.3 and Table 3.8, on one hand, an MMC made of (i) FBSM has a semiconductor power loss of 1.65% using the bare minimum of submodules but actually would require 112.75% this number to ensure a 99.99% reliability at about 19 years of operation. We could then extrapolate that the power losses would scale up to 1.86%. On the other hand, an MMC made of (ii) MBSM has a semiconductor power loss of 1.37% using the bare minimum of submodules, but would only require 102% for a similar level of reliability, thus scaling its power losses up to 1.40%. In summary, a fully-equipped MMC with MBSMs has the potential to save a total of 0.46% (i.e. 1.86%–1.40%) overall power losses compared to an MMC made solely of FBSMs.

The advantages of MBSM over FBSM are driven by the doubled number of semiconductors, which, just like the two faces of a sword, is the principal drawback of MBSM. For applications that can tolerate large SM capacitors and are sensitive to the cost of semiconductors, traditional SM topologies (FBSM and

HBSMs) are still the first choice to consider. It's still a long way to go for MBSM to be applied in industry.

3.5 Summary

This chapter presents the MBSM from aspects of topology, low level control, soft paralleling mechanism, failure management, and reliability study. MBSM shares higher level control framework with conventional MMC and has unique low level control requirements. This new topology simplifies the capacitor balancing strategy and at the same time increases the system failure tolerances. Although the amount of semiconductors is doubled in MBSM MMC, the semiconductor losses has been reduced to 80% of that in its counterpart. Simulation results have verified the characteristics of a MBSM MMC in HVDC scenario.

Chapter 4

Advanced Control Schemes for MBSM MMC

Several advanced control schemes for the control of the MBSM MMC are presented in this chapter. Firstly, an algorithm to automatically generate independent variables state space models from linear electrical circuits is introduced. Then, a model predictive control-based start-up controller to simplify the SM pre-charge procedure and at the same time improve the transient performance is studied. Finally, a reinforcement learning-based low-level controller to achieve low switching frequency operation of the MBSM MMC is investigated.

4.1 Automatic Derivation of State-Space Model

4.1.1 State Space Model of Electrical Circuit

Modeling of electrical circuit constitutes an essential skill for power electronics engineers. Accurate and concise models provide both insights into the operation of the circuit and constitutes an essential basis for the derivation of effective control system. In these circumstances, having access to high levels of both of control and power electronic skills unlocks the ability to design even more performant power converters. Furthermore, with the advent of stacks of sub-modules and modular converters [118], power electronics circuits are becoming even more

complex and modelling them becomes both a time-consuming and challenging task, which requires extensive experience in analysing extensive circuit diagrams.

The toolbox of an electrical circuit engineer contains the following linear elements: resistances, inductors, capacitors, current and voltage sources, as summarised in Fig. 4.1. These elements can be used to create any electrical circuits.

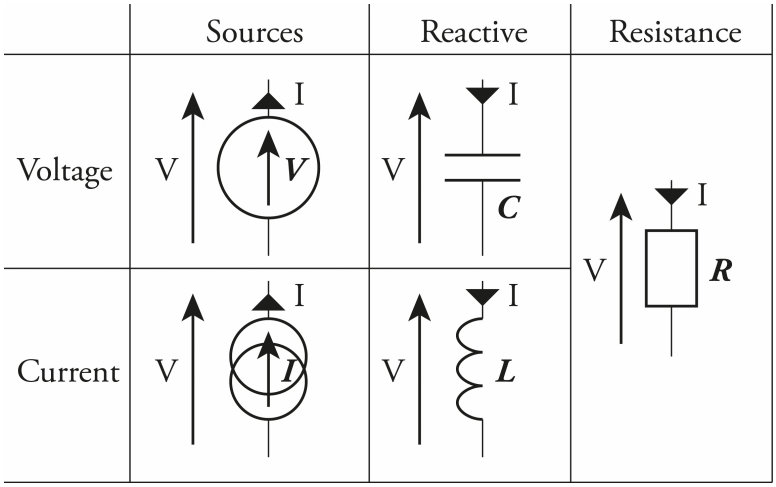


Figure 4.1: Fundamental elements for circuit analysis

The basic relationship between voltage and current in a circuit are described by Kirchhoff laws, including Kirchhoff Current Law (KCL) and Kirchhoff Voltage Law (KVL), which are the basis for analyzing and calculating complex circuits [119]. KCL determines the relationship between the branch currents at any node in the circuit, which is also known as the Node Current Law. KCL shows that: the sum of all the current entering a node is equal to the sum of all the current leaving the node. KVL determines the relationship between the voltages in any circuit, so it is also called the loop voltage law. KVL shows that the algebraic sum of the potential differences (voltages) at both ends of all elements along the closed loop is equal to zero.

Based on Kirchhoff's law, many systematic circuit analysis methods have been developed. Modified Nodal Analysis (MNA) is the most widely used among them. Extensively explanation of MNA are provided in [120], or more recently [121], and a didactically illustrated course is available in [122]. The use of MNA to derive state equations was suggested in [123], later improved in [124], then reused in [125]. Some MATLAB implementations already exist as in [122] but are limited

to Single-Input, Single-Output transfer functions and do not provide a clear indication regarding the current or voltage directions; particularly important later, when designing the sensing of the later-controlled circuit.

This section proposes an algorithm to automatically generate dependent variables state space model from linear electrical circuits. The automatic derivation of the state space model will require the following steps: (i) reading of the netlist, (ii) identifying the states, (iii) deriving the full set of equations describing the circuit, (iv) reducing the number of equations, (v) identifying a base of independent states, (vi) deducting the state space model for this base, and (vii) providing the full state space model. The obtained state space models of two cases are presented. Simulation results have verified the effectiveness and accuracy of the proposed method.

4.1.2 Derivation of Full Set of Equations from Linear Electrical Circuits

Electrical Circuit and Netlist

To assist in the explanation of the proposed algorithm, the circuit in Fig. 4.2 is used as an example to derive the state space model. Two capacitors C_1 and C_2 with different capacitance are parallelized together and then connected to a resistor in series. The circuit is powered by a voltage source. The input voltage V can be seen as the output voltage of an half-bridge power electronic stage. Three nodes and three branches construct this basic electrical circuit.

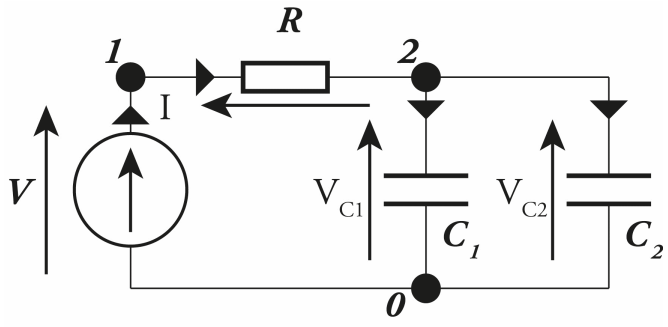


Figure 4.2: Electrical Circuit

Netlist is applied to describe the connections between circuit components.

Generally speaking, it is a text file that follows some simple markup syntax which can be either written by the designer or automatically generated by a SPICE software. The text file contains a table as is shown in Table 4.1. Suppose that there are n linear elements in the electrical circuit, include resistances, inductors, capacitors, current and voltage sources. The corresponding netlist will have n rows, each row represents the information of one element. There are four columns in total. The first column records the name of the component, while the second and third column show the labels of the first node and second node of the components, respectively. The last column gives the component's value.

Table 4.1: Netlist Format

Name of Component 1	First Node 1	Second Node 1	Value 1
Name of Component 2	First Node 2	Second Node 2	Value 2
...	...	...	...
Name of Component n	First Node n	Second Node n	Value n

A netlist for the circuit in Fig. 4.2 is presented in Fig. 4.3. The first row shows that the voltage source V is connected to Node 1 and Node 0, and the voltage is 50 V. The $1k\ \Omega$ resistor R connects Node 1 and Node 2. The two capacitors C_1 and C_2 are both connected to Node 2 and Node 0. There capacitance is 1 mF and 500 uF respectively.

```
V   1   0   50
R   1   2   1k
C1  2   0   1m
C2  2   0   500u
```

Figure 4.3: Netlist of Circuit in Fig. 4.2

States

State refers to the ordered set of the minimum number of variables that can determine the state of the system. An electrical circuit consists of sources, reactive components, and resistors, as illustrated in Fig. 4.1. When no reactive element

is present, the output component (either current or voltage) of the sources (of either voltage or current types, respectively) is determined by a linear relationship between the aggregated resistors and the magnitudes (voltage or current) of the sources' outputs. In this basic situation, there is no state as the voltages and currents are fixed. In circuits of greater interest in the context of this paper, a certain number of reactive elements are present. The algorithm will thus list their individual state (i.e. voltage for capacitors and current for inductors) in the order in which they appear in the netlist.

In the example in Fig. 4.2, the state is the voltages of the two capacitors $\begin{bmatrix} V_{C_1} & V_{C_2} \end{bmatrix}^T$. As the output voltage V changes, the capacitors will be charged or discharged. Their voltages have great impact on other variables in the circuit. The capacitor voltages reflect the state of the whole system. The voltage and current convention (i.e. direction) is illustrated in Fig. 4.1.

Full Set of Equations

MNA requires many more equations than traditional voltage loops analysis methods but is much more convenient to be implemented into an algorithm. Suppose there are n nodes and b branches in the circuit, including b_v ideal voltage source branches or current source control branches. MNA takes $n-1$ non reference node voltage and b_v voltage defined branch current as unknown circuit variables. The order of the modified nodal voltage equations is low, and it overcomes the shortcomings of the basic nodal analysis which can not directly deal with ideal voltage source branches, zero impedance branches and flow control devices.

Using MNA to formulate full set of equations can be divided into two steps. First, the currents flowing into or from each nodes except the reference Node 0 are expressed in terms of the other nodes' voltages or states. For this example, this results in Eq. (4.1). The currents flow into Node 1 include voltage source current i_V and current from the resister R. Meanwhile, three branch currents flow into Node 2, include the resister current, the current from capacitor C_1 and the current from capacitor C_2.

$$\begin{cases} -\dfrac{v_1 - v_2}{R} + i_v = 0 \\ \dfrac{v_1 - v_2}{R} - C_1\dot{V}_{C_1} - C_2\dot{V}_{C_2} = 0 \end{cases} \tag{4.1}$$

On the other hand, the voltage sources and reactive elements are linked to the nodes' voltages. The voltage of Node 1 is the same as source voltage V. What's more, the voltage of Node 2 is equal to capacitor voltage V_{C_1} and V_{C_2}. This gives Eq. (4.2).

$$\begin{cases} v_1 - V = 0 \\ v_2 - V_{C_1} = 0 \\ v_2 - V_{C_2} = 0 \end{cases} \tag{4.2}$$

As has been introduced in the previous subsection, capacitor voltages V_{C_1} and V_{C_2} are denoted as system state x. Besides, source voltage V is denoted as system input u. Node voltages v_1 and v_2 and voltage source current i_V are denoted as extra state z. Then, Eq. (4.1) and Eq. (4.2) can then be combined into a matrix format Eq. (4.3).

$$\underbrace{\begin{bmatrix} -\frac{1}{R} & \frac{1}{R} & 1 \\ \frac{1}{R} & -\frac{1}{R} & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}}_{G} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ i_v \end{bmatrix}}_{z} + \underbrace{\begin{bmatrix} 0 & 0 \\ -1 & -1 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{A_{\dot{x}}} \underbrace{\begin{bmatrix} C_1\dot{V}_{C1} \\ C_2\dot{V}_{C2} \end{bmatrix}}_{E_{\dot{x}}\dot{x}} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{bmatrix}}_{A_x} \underbrace{\begin{bmatrix} V_{C1} \\ V_{C2} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ -1 \\ 0 \\ 0 \end{bmatrix}}_{B_u} \underbrace{[V]}_{u} = 0 \tag{4.3}$$

4.1.3 State Space Model with Independent Variables

Reduction to State Space

In Eq. (4.3), the large vector z corresponds to all the nodes' states; several of them are redundant variables with the state x. Therefore, Eq. (4.3) can be downsized to make it easier to be solved and greatly reduce the time, space and computational complexity. For this, the most effective way consists in using

Gauss-Jordan elimination with partial pivoting to compute the Reduced Row Echelon Form (RREF) of the combined matrices G, $A_{\dot{x}}$, A_x, and B_u in Eq. (4.3), leading to the matrix M in Eq. (4.4).

$$M = rref\,[G\,A_{\dot{x}}\,A_x\,B_u] = \begin{bmatrix} \mathbf{1} & M_{12} & M_{13} & M_{14} \\ \mathbf{0} & M_{22} & M_{23} & M_{24} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & \frac{1}{R} & -\frac{1}{R} \\ 0 & 0 & 0 & 1 & 1 & 0 & \frac{1}{R} & -\frac{1}{R} \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \end{bmatrix} \tag{4.4}$$

After the transformation, the upper left part of M becomes a 3×3 Identity Matrix, which means that the node voltages v_1 and v_2 and voltage source current i_V are no longer coupled with each other and can be expressed by other variables. The full node voltage state can still be computed back from the state x and input u using the top part of M in Eq. (4.4) leading to Eq. (4.5).

$$z = -\begin{bmatrix} M_{12} & M_{13} & M_{14} \end{bmatrix} \begin{bmatrix} E_{\dot{x}}\dot{x} & x & u \end{bmatrix}^T \tag{4.5}$$

The upper left part of M becomes a 3×3 Zero Matrix. Consequently, the relationship of state x and input u is derived without the influence of extra state z. The rest of the bottom part of M in Eq. (4.4) now corresponds to the descriptor state space, as in Eq. (4.6).

$$\underbrace{\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}}_{M_{22}E_{\dot{x}}=E} \underbrace{\begin{bmatrix} \dot{V}_{C_1} \\ \dot{V}_{C_2} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{R} \\ -1 & 1 \end{bmatrix}}_{-M_{23}=A} \underbrace{\begin{bmatrix} V_{C_1} \\ V_{C_2} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{R} \\ 0 \end{bmatrix}}_{-M_{24}=B} \underbrace{[V]}_{u} \tag{4.6}$$

Base State Space Model

So far, the state space model of electrical circuit has eliminated the factors that are not relevant, and has become a classic form with only state and input. As it is the case in the circuit example in Fig. 4.2, reactive components may share their dynamic, e.g. parallel capacitors sharing voltage or series-connected inductors

sharing current. This situation can be quickly tested by calculating the rank of the descriptor matrix E:

$$rank(E) = \underbrace{1}_{n_b} < \underbrace{2}_{n_x}$$

If its rank n_b is inferior to the number of states n_x, then some of the states in x are dependent. The final number of independent states is thus equal to n_b and will translate into lines of zeros in matrix E as shown in (4.7).

$$Eq.\ (4.6) \Longrightarrow \begin{bmatrix} E_1 \\ \mathbf{0} \end{bmatrix} \dot{x} = \begin{bmatrix} A_1 \\ A_2 \end{bmatrix} x + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u \tag{4.7}$$

The controlability of a state space model indicates its ability to bring the state to any directions (i.e. element values) in a finite amount of time [126]. Having dependent states in the state space will however prevent most control techniques from being used since the controlability test will automatically fail. Given that the states and possibly the inputs linearly combine to zero, there must be a base of independent vectors such that $[A_2\ B_2]\, M_b = 0$, i.e. M_b constructs the zero space of matrix $[A_2\ B_2]$:

$$M_b = null\left([A_2\ B_2]\right)$$

This base can be either suggested by the user or identified automatically by a software, as in Eq. (4.8).

$$\begin{bmatrix} x \\ u \end{bmatrix} = M_b \begin{bmatrix} x_b \\ u_b \end{bmatrix} = \begin{bmatrix} M_{b_{11}} & M_{b_{12}} \\ M_{b_{21}} & M_{b_{22}} \end{bmatrix} \begin{bmatrix} x_b \\ u_b \end{bmatrix} \tag{4.8}$$

With $E_b = E_1\, M_{b_{11}}$, $A_b = A_1\, M_{b_{11}} + B_1\, M_{b_{21}}$, $B_b = A_1\, M_{b_{12}} + B_1\, M_{b_{22}}$ and $\dot{B}_b = E_1\, M_{b_{12}}$, from this base can be computed the base state space Eq. (4.9) from which any control design techniques could use to derive a performant regulator, e.g. LQR or MPC.

$$E_b\, \dot{x}_b = A_b\, x_b + B_b\, u_b + \dot{B}_b\, \dot{u}_b \tag{4.9}$$

In the case shown in Fig. 4.2, the matrix of independent state and input $(x_b \;\; u_b)^T$ is identified as $(V_{c_1} \;\; V)^T$. Finally, the base state space model with independent state is:

$$(C_1 + C_2)\,\dot{x}_b = -\frac{1}{R}\,x_b + \frac{1}{R}\,u_b \tag{4.10}$$

4.1.4 Case Studies

Simulation Results of Simple Circuit

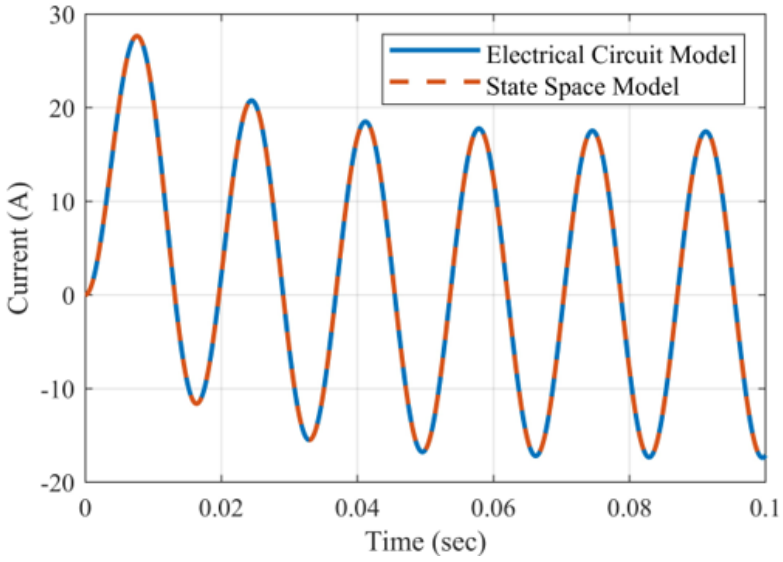


Figure 4.4: Simulation results for the simulated electrical circuit from Fig. 4.2 and state space model Eq. (4.9)

The electrical circuit illustrated in Fig. 4.2 has been simulated together with its derived state space model Eq. (4.10), which is realized by the state space equation blocks in Simulink/MATLAB. The system input is V, which is AC voltage with frequency at 60Hz and peak amplitude at 100V. V_{c_1} is monitored as system output to evaluate the accuracy of the state space model. The results are extremely similar since the error is down to a few mV or about 0.01%, as shown in Fig. 4.4. This difference is mainly down to the way the Simulink solver treats the two different models.

In this case, the proposed automatic deviation method doesn't show the superiority in convenience and computational complexity compared with conventional

manually deviation because the circuit has only one independent source, two nodes, two states and one independent state. The system complexity increases greatly as the extension of the state space.

Case of MMC

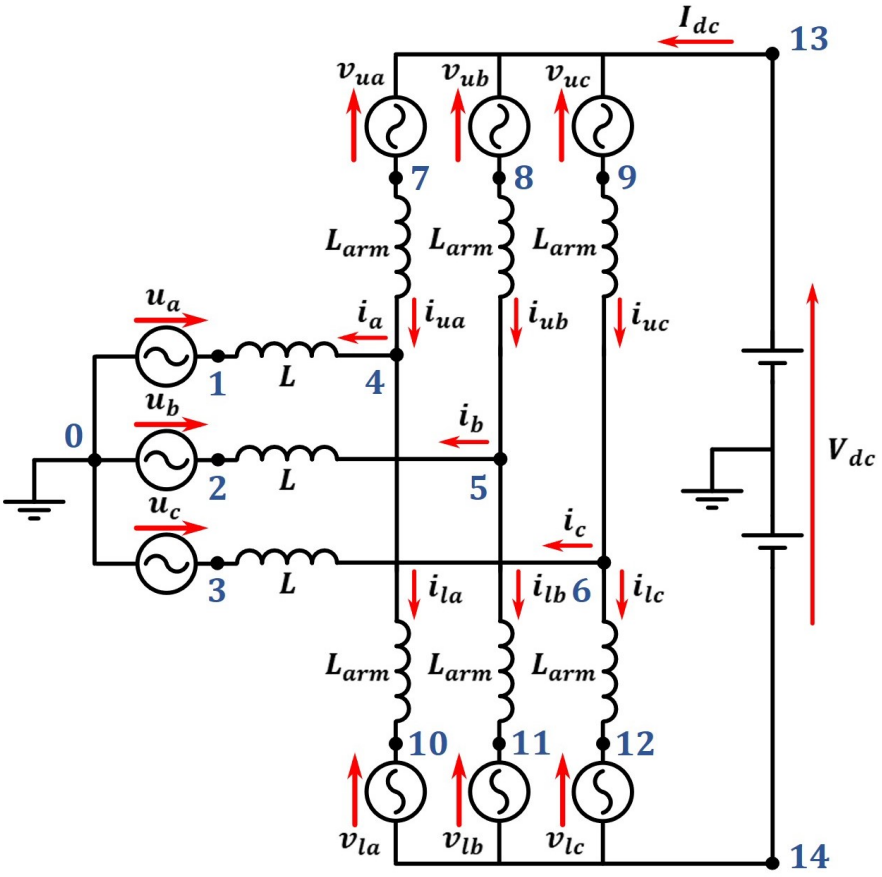


Figure 4.5: Electrical Circuit of MMC

As an example of how versatile the algorithm explained in this paper can be, the circuit of the MMC shown in Fig. 4.5 has also been modeled using the same method. In this case, DC voltage V_{dc} is converted to three phase AC voltage u_a, u_b and u_c. Each phase and arm of the converter has an inductor to regulate the current through it. The stack voltages are obtained from the output of high level and medium level control. Since the operation of the low level control and the SM topologies are not of interests in this topic, the stacks of SMs are replaced with voltage controlled voltage source and generate voltages at v_{uj} and v_{lj}, where $j = 1, 2, 3$.

There are in total fourteen nodes except the reference node ($n = 14$), ten voltage sources ($n_u = 10$) and nine reactive elements ($n_x = 9$) in the MMC case. Consequently, the state $\mathbf{x}$ and input $\mathbf{u}$ of the state space model are:

$$\begin{cases} \mathbf{x} = [i_a \ i_b \ i_c \ i_{ua} \ i_{ub} \ i_{uc} \ i_{la} \ i_{lb} \ i_{lc}]^T \\ \mathbf{u} = [u_a \ u_b \ u_c \ u_{ua} \ u_{ub} \ u_{uc} \ u_{la} \ u_{lb} \ u_{lc} \ V_{dc}]^T \end{cases} \tag{4.11}$$

Besides, denote all the node voltages into an array $\mathbf{V_n}$, then we have:

$$\mathbf{V_n} = [V_1 \ V_2 \ V_3 \ V_4 \ V_5 \ V_6 \ V_7 \ V_8 \ V_9 \ V_{10} \ V_{11} \ V_{12} \ V_{13} \ V_{14}]^T$$

The matrix format of extra states is: $\mathbf{z} = \begin{bmatrix} \mathbf{x} \\ \mathbf{V_n} \end{bmatrix}$.

Due to its large dimension, deriving the initial state space model manually is complicated and time-consuming. The corresponding equation is shown in a Block Matrix format, as in Eq. (4.12), where coefficient matrices G, $A_{\dot{x}}$, A_x, B_u are represented by matrices of several submatrices. In Eq. (4.12), $\mathbf{0}_{(m\times n)}$ represents a Zero Matrix with m rows and n columns, while $\mathbf{1}_{(m)}$ represents an m-dimensional Identity Matrix. Based on MNA, submatrices G_{11}, G_{21}, G_{32}, A_3 and B_2 are derived as follows. The dynamics of all the reactive elements in the MMC case are described with Eq. (4.12).

$$\begin{bmatrix} G_{11} & \mathbf{0}_{(n_x\times n_x)} \\ G_{21} & \mathbf{0}_{(n_u\times n_x)} \\ \mathbf{0}_{(n\times n)} & G_{32} \end{bmatrix} z + \begin{bmatrix} \mathbf{1}_{(n_x)} \\ \mathbf{0}_{(n_u\times n_x)} \\ \mathbf{0}_{(n\times n_x)} \end{bmatrix} E_{\dot{x}}\dot{x} + \begin{bmatrix} \mathbf{0}_{(n_x\times n_x)} \\ \mathbf{0}_{(n_u\times n_x)} \\ A_3 \end{bmatrix} x + \begin{bmatrix} \mathbf{0}_{(n_x\times n_u)} \\ B_2 \\ \mathbf{0}_{(n\times n_u)} \end{bmatrix} u = 0 \tag{4.12}$$

$$G_{11} = \begin{bmatrix} 1&0&0&-1&0&0&0&0&0&0&0&0&0&0 \\ 0&1&0&0&-1&0&0&0&0&0&0&0&0&0 \\ 0&0&1&0&0&-1&0&0&0&0&0&0&0&0 \\ 0&0&0&1&0&0&-1&0&0&0&0&0&0&0 \\ 0&0&0&0&1&0&0&-1&0&0&0&0&0&0 \\ 0&0&0&0&0&1&0&0&-1&0&0&0&0&0 \\ 0&0&0&-1&0&0&0&0&0&1&0&0&0&0 \\ 0&0&0&0&-1&0&0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&-1&0&0&0&0&0&1&0&0 \end{bmatrix} \quad G_{21} = \begin{bmatrix} 1&0&0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&1&0&0&0&0&0&-1&0 \\ 0&0&0&0&0&0&0&1&0&0&0&0&-1&0 \\ 0&0&0&0&0&0&0&0&1&0&0&0&-1&0 \\ 0&0&0&0&0&0&0&0&0&1&0&0&0&-1 \\ 0&0&0&0&0&0&0&0&0&0&1&0&0&-1 \\ 0&0&0&0&0&0&0&0&0&0&0&1&0&-1 \\ 0&0&0&0&0&0&0&0&0&0&0&0&1&-1 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}$$

$$G_{32} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & -1 \end{bmatrix} \quad A_3 = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

With the proposed automatic derivation method, the state space model becomes much more simple. Independent states are identified as $x_b = [i_{ub}\ i_{uc}\ i_{la}\ i_{lb}\ i_{lc}]^T$ and the coefficient matrices in corresponding state space model Eq. (4.9) have been downsized from dimension up to (33×24) to dimension no more than (5×10). The coefficient matrices of independent state x_b and differential of input u_b become Zero Matrices:

$$A_b = \mathbf{0}_{(5\times5)} \qquad \dot{B}_b = \mathbf{0}_{(5\times10)}$$

The coefficient matrices of extra elements and inputs are listed as follows.

$$E_b = \begin{bmatrix} -L & -2L & -L_a & L & L+L_a \\ L & -L & 0 & -L-L_a & L+L_a \\ -L_a & -L_a & 2L_a & L_a & L_a \\ L_a & 0 & 0 & L_a & 0 \\ 0 & L_a & 0 & 0 & L_a \end{bmatrix} \quad B_b = \begin{bmatrix} -1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & -1 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & -1 & 1 \end{bmatrix}$$

Given that the system output is $y_b = C_b\, x_b + D_b\, u_b$, where

$$C_b = \begin{bmatrix} -1 & -1 & 0 & 1 & 1 \\ 1 & 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 & -1 \\ -1 & -1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix}$$

and $D_b = \mathbf{0}_{(5\times10)}$, y_b becomes an array of three phase currents and the upper stack currents in phase A and phase B: $y_b = [i_a\ i_b\ i_c\ i_{ua}\ i_{ub}]^T$, which are observed to compare the results with electrical circuit model. The waveforms showed in Fig. 4.6 are also similar to the 0.01% margin between its electrical circuit and state space model. The accuracy of the proposed method is guaranteed while the computational complexity has been greatly reduced, lying a solid foundation for the application of advanced control tool. Time comparison between the derived state space simulation and the inherent electrical model in Simulink is not presented here.

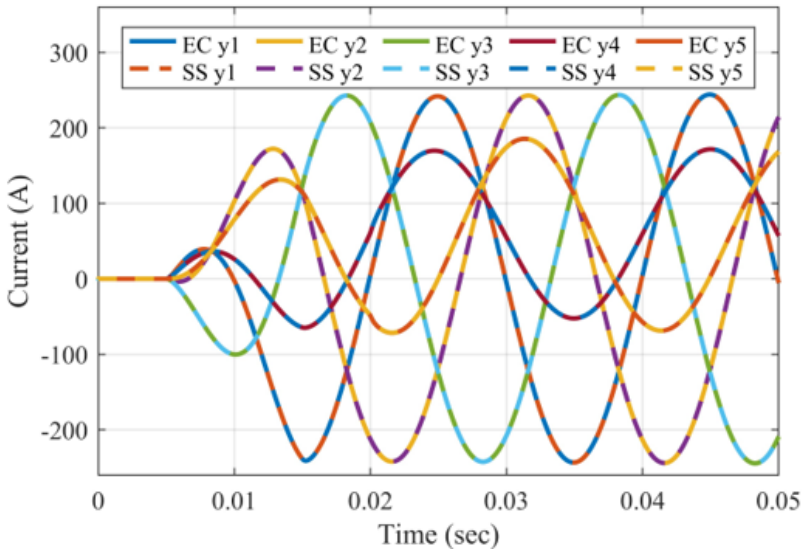


Figure 4.6: Simulation results for the simulated electrical circuit from Fig. 4.5 and its derived state space model

4.2 MPC based MBSM MMC Start Up Control

SM capacitor voltages fluctuate around the rated value during normal operation. Without charging SMs smoothly to nominal value in start up procedure, large inrush current would occur and threaten the condition of MMC and the whole HVDC system. The pre-charging of the SM capacitors in conventional MMC is traditionally conducted through high-impedance pre-insertion resistors to the AC or DC grids; in essence bulky devices which are bypassed and left unused outside

the start-up periods [127, 128]. Besides, start-up strategy for conventional MMC requires complicated current control strategy [129] to regulate charge current. MBSM allows much easier start-up and shut down thanks to possible pre-charging of SMs since the bypass switches connect the discharged capacitors in parallel.

4.2.1 Start Up of the MBSM MMC

During the start-up procedure of the MBSM MMC, auxiliary switches and breakers are used to connect or isolate different part to the main circuit. Apart from the AC side and DC side breakers which are commonly used in conventional MMC start up, stack breakers and internal charge breakers are integrated specially for MBSM MMC. The layout of auxiliary breakers in a stack is shown in Fig. 4.7. The proposed pre-charging strategy for MBSM MMC takes advantages of the unique features of the MBSM structure. To isolate the stack from external power circuit, stack breakers stay open and internal charge breakers keep closed. Meanwhile, all the normally closed bypass switches (S_1 and S_2 in Fig. 3.2) stay closed (uncontrolled). Capacitors in all MBSMs are parallelized together and form an equivalent capacitor with larger capacitance but same nominal voltage. Internal charging has greatly simplified the start up procedure and can be realized without using large voltage source.

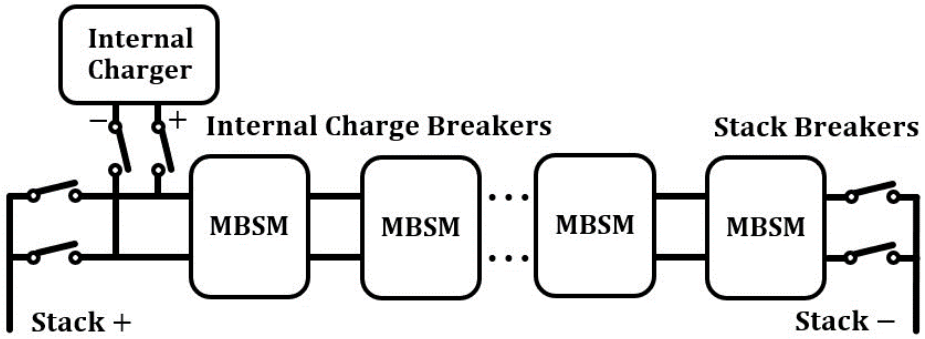


Figure 4.7: Layout of auxiliary breakers in a MBSM stack

Fig. 4.8 illustrates the equivalent internal charge circuit. The internal charger is constructed with a DC voltage source and a buck converter. Battery energy storage system serves as voltage source, generating DC voltage v_S at constant value. Buck converter provides controlled voltage to the subsequent LC loop.

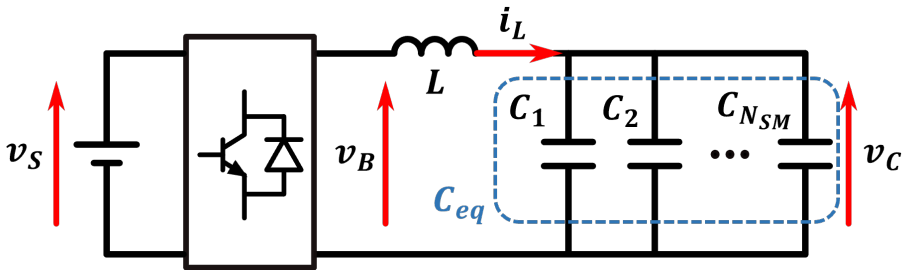


Figure 4.8: Equivalent internal charging circuit

During internal charging, all the semiconductors in MBSMs stay off. The charging current flows through reverse recovery diodes to capacitors. Since power diodes have negligible voltage drop when anode is positive, they are omitted in the equivalent charging circuit.

4.2.2 Model Predictive Control

MPC is an optimal controller that solves a finite-time domain constrained optimization problem at each time step to determine the control action that minimizes an objective function for the controlled dynamical system [130, 131, 132]. The block diagram of the MPC based controller used in this thesis is demonstrated in Fig. 4.9. The controller uses the prediction error, which is calculated by comparing the output y and the reference r, to correct the prediction model. The feedback correction improves the robustness of MPC against external disturbances and system uncertainty. Besides, MPC determines the future control role through the optimization of performance objective function [133, 134]. The optimization in MPC is different from the usual discrete optimal control algorithm [135]. It does not use a fixed global optimal goal, but rather a rolling finite time domain optimization strategy [136, 137].

MPC has several important features, including but not limited to [138, 139]:

(1) the ability to handle MIMO plants,

(2) the capability of dealing with time delays,

(3) the possibility of making use of information on future reference and disturbance signals.

If the control object is a linear system with no constraints and the objective

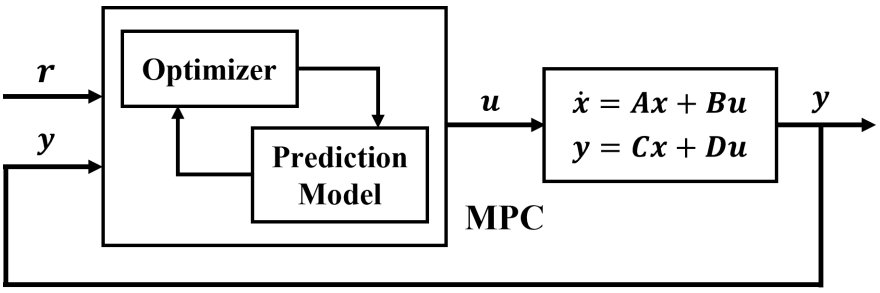


Figure 4.9: MPC

function is quadratic, the MPC will degrade to an LQR controller.

The MPC controller is applied in the start-up procedure of the MBSM MMC. MPC ensures the capacitor voltage and charging current constraints are satisfied at the same time. To the knowledge of the author, no previous work about the start-up of MBSM has been found.

Prediction Model

The output voltage of the buck converter v_B, the capacitor voltage v_C, and the charging (inductor) current i_L are investigated in the derivation of the prediction model. Suppose that a stack has N_{SM} MBSMs and the nominal capacitance is C_{SM}. Then the equivalent capacitance is: $C_{eq} = N_{SM} \cdot C_{SM}$. Consider the equivalent charging circuit in Fig. 4.8, state space model (4.13) holds. The pre-charging control problem of the MBSM MMC is simplified down to a buck converter control issue.

$$\begin{cases} \underbrace{\begin{pmatrix} \dot{v_C} \\ \dot{i_L} \end{pmatrix}}_{\dot{x}} = \underbrace{\begin{pmatrix} 0 & 1/C_{eq} \\ -1/L & 0 \end{pmatrix}}_{A} \underbrace{\begin{pmatrix} v_C \\ i_L \end{pmatrix}}_{x} + \underbrace{\begin{pmatrix} 0 \\ 1/L \end{pmatrix}}_{B} \underbrace{(v_B)}_{u} \\ \underbrace{\begin{pmatrix} v_C \\ i_L \end{pmatrix}}_{y} = \underbrace{\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}}_{C} \underbrace{\begin{pmatrix} v_C \\ i_L \end{pmatrix}}_{x} + \underbrace{\begin{pmatrix} 0 \\ 0 \end{pmatrix}}_{D} \underbrace{(v_B)}_{u} \end{cases} \tag{4.13}$$

Base on the Eq.(4.13), the discrete time state space model is derived by applying Forward Euler [140] method to approximate the differential element: $\dot{x} = \dfrac{x(k+1) - x(k)}{T_S}$, where T_S is the sampling period. The prediction model becomes:

$$\begin{cases} \underbrace{\begin{pmatrix} v_C(k+1) \\ i_L(k+1) \end{pmatrix}}_{x(k+1)} = \underbrace{\begin{pmatrix} 1 & \frac{T_S}{C_{eq}} \\ -\frac{T_S}{L} & 1 \end{pmatrix}}_{A_D} \underbrace{\begin{pmatrix} v_C(k) \\ i_L(k) \end{pmatrix}}_{x(k)} + \underbrace{\begin{pmatrix} 0 \\ \frac{T_S}{L} \end{pmatrix}}_{B_D} \underbrace{(v_B(k))}_{u(k)} \\ \underbrace{\begin{pmatrix} v_C(k) \\ i_L(k) \end{pmatrix}}_{y(k)} = \underbrace{\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}}_{C_D} \underbrace{\begin{pmatrix} v_C(k) \\ i_L(k) \end{pmatrix}}_{x(k)} + \underbrace{\begin{pmatrix} 0 \\ 0 \end{pmatrix}}_{D_D} \underbrace{(v_B(k))}_{u(k)} \end{cases} \tag{4.14}$$

The values of $v_C(k)$ and $i_L(k)$ are the measured value at the current sample time. The corresponding values of the next sample time, $v_C(k+1)$ and $i_L(k+1)$, are predicted by the selection of different values of $v_B(k)$. The selection of $v_B(k)$ should minimize an objective function that describes the performances of the start-up procedure.

Objective Function and Constraints

The control objective is charging the equivalent capacitor smoothly to its rated value and at the same time suppressing large charging current. Hence, the first term in the objective function describes the reference tracking performance, marked as J_y. Suppose that the nominal MBSM capacitor voltage is $v_{C_{rated}}$, J_y is calculated in Eq.(4.15).

$$J_y = \sum_{i=1}^{p} \left[\omega_i \frac{v_{C_{rated}} - v_C(k+i|k)}{v_{C_{rated}}} \right]^2 \tag{4.15}$$

where p represents the prediction horizon, k represents the current control interval, ω_i represents the tuning weight at the ith prediction horizon step, and $v_C(k+i|k)$ represents the predicted capacitor voltage at the ith prediction horizon step (in engineering unit).

The second term reflects the effect of constraint violation, marked as J_ϵ. Soft constraints are applied here since it allows a feasible solution under the condition where constraint violations might be unavoidable. The MPC controller employs a dimensionless, non-negative slack variable, ϵ_k, which quantifies the worst-case

constraint violation. J_ϵ is obtained implicitly from the Model Predictive Control Toolbox provided by MATLAB. The mathematical derivation process is not investigated in this thesis.

$$J_\epsilon = \rho_\epsilon {\epsilon_k}^2 \tag{4.16}$$

4.2.3 Simulation Results and Analysis

The simulation applies the same system parameters as listed in Table 2.4. When long prediction and control horizons are used in the MPC controller, both the dynamic performance of the system and the computational requirements of the controller improve. The prediction horizon and the control horizon are set as 10 and 2, respectively, in this thesis. The control objective is to charge the capacitors to 2000V while limit the charge current under 1500A as large current will cause damage to semiconducters and capacitors. Controller parameters are tuned by using Model Predictive Control Toolbox to improve the system performances. Fig. 4.10 illustrates the capacitor voltage and charging current. Start-up procedure starts at $t = 0.01$s. The capacitor voltage rises steadily and there is no overshoot after reaching the target value. Besides, the current has a slight fluctuation around the maximum value and then decreases to zero after the start-up is complete.

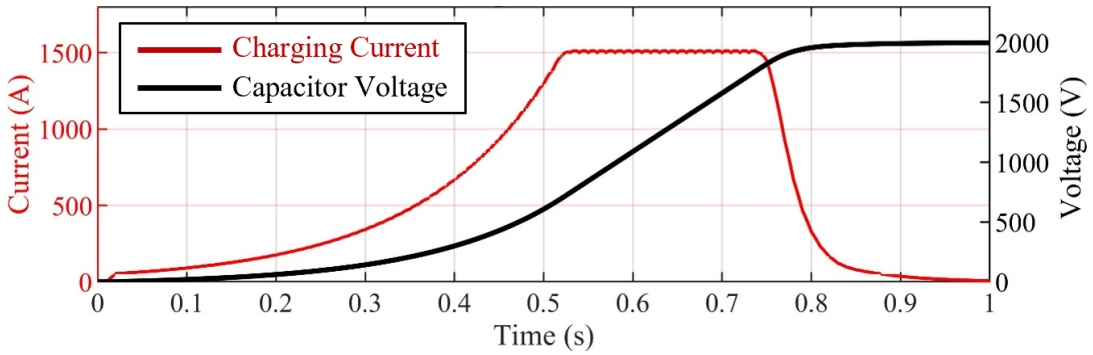


Figure 4.10: Voltage and current performance during start-up procedure.

Fig. 4.11 shows capacitor voltages during the transient process from start-up to normal operation at $t = 1$s. The smooth transition presents the effectiveness of the proposed start-up control strategy. The slight voltage difference at around $t = 0.4$s to $t = 0.8$s indicates the effect of the diodes.

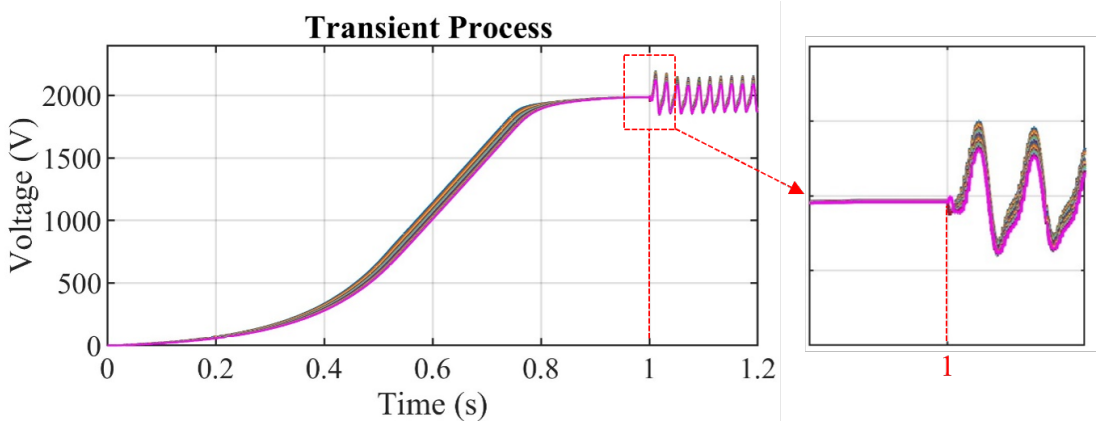


Figure 4.11: Transient process from start-up to normal operation at $t = 1s$

It should be noted that MPC relies on an accurate model of the controlled process, which may be unavailable. The modelling of the start-up process of MBSM is equivalent to the control of a DCDC converter. The implementation of MPC in an on-time controller may encounter more challenges and require further study in the future.

4.3 Reinforcement Learning based low level control

4.3.1 Challenges in MBSM Low Level Control

The fundamental objectives of the low-level controller, whether conventional single-busbar types or MBSM types, are tracking the stack voltage reference as well as maintaining the balance of SM capacitor voltages. Moreover, power efficiency is another important factor in evaluating the performance of a controller. The MMC industry expects low-power-loss operation, especially in high-voltage, large-power scenarios.

Many modulation strategies for conventional single-busbar MMC have been proposed, including low-frequency modulation (NLM, SHE, ...) and PWM-based modulation (PSC, PDC, ...). In a high-voltage MMC system with a large number of SMs, NLM is the most popular, mainly because it offers a better compromise between voltage quality and power loss. PWM-based strategies usually involve

unnecessary complexity for high-voltage systems, in which the high-speed switching will lead to lower efficiency and limited flexibility [141]. However, since the capacitor balancing of MBSM depends on the sequential parallel connection of adjacent capacitors, almost all modulation methods for parallel structures are based on PSC. In terms of efficiency, the PSC-based MBSM low-level control still has a lot of room for improvement.

Reinforcement learning (RL) is a research branch of machine learning that has been widely used in automatic driving [142], computer vision [143] [144], natural language processing [145], industrial control [146], smart grid [147], and other fields in recent years. Under the framework of RL, agents take actions based on the environment to maximize the expected rewards. Specifically, after the agent performs an action, the environment will switch to a new state, and the reward signal will be given for the new state environment. The agent then performs new actions in response to the rewards of the new state and feedback from the environment [148].

RL can be divided into model-based RL and model-free RL. The former requires explicit modeling of the environment [149]. Action planning is considered in advance, but the disadvantage is that if the model is not consistent with the real world, it will not perform well in actual application scenarios. The latter doesn't need to consider model learning, making it easier to implement and adjust the model to a good state. Therefore, the model-free RL is more popular, and has been developed more widely. Consider that the explicit modeling of the MBSM bottom-layer model is very complex, and the low-level controller involves the performance of many aspects, model-free RL is suitable for MBSM low-level control than model based RL.

4.3.2 Principle of Reinforcement Learning

In RL, the performance of an action (A) is evaluated by the reward (R), which is a value received by the agent from the environment as a direct response to the actions. In order to reflect the effect of the current action on future performance, another concept, discounted return (U), or cumulative discounted future reward,

is defined in Eq. (4.17).

$$U_t = R_t + \gamma \cdot R_{t+1} + \gamma^2 \cdot R_{t+2} + \gamma^3 \cdot R_{t+3} + \dots \tag{4.17}$$

where $\gamma \in (0, 1)$ is the discount rate, and R_t is the reward at time step t. Since $R_t, R_{t+1}, R_{t+2}, R_{t+3}, \dots$ are future rewards which are not observable, U_t is a random variable.

Another important concept is the policy function (π), which describes the decision making criteria of the agent. π is essentially a probability density function $\pi(a|s) = P(A = a|S = s)$ that maps the observed state $S = s$ to a probability distribution over all the possible actions. Given state s_t and policy π, the quality of the action a_t is evaluated by the Action Value Function $Q_\pi(s_t, a_t)$:

$$Q_\pi(s_t, a_t) = \mathbb{E}[U_t \,|\, S_t = s_t, A_t = a_t] \tag{4.18}$$

where $\mathbb{E}$ represents the expectation that related to future actions and future states. Now the Optimal Action-Value Function $Q*(s_t, a_t)$ can be described by Eq.(4.19).

$$Q^*(s, a) = \max_\pi Q_\pi(s, a) \tag{4.19}$$

The optimal action-value function (4.19) is implicit and contains random parts. So, it can not be implemented directly into digital controllers. Generally, neural network (NN) $Q(s, a; w)$ is applied to approximated Eq. (4.19) and control the agent, where w represents the NN parameters. Deep Q network (DQN) trained using temporal different (TD) [150] is applied in this thesis as a proof of concept. The parameters of the NN are updated every time step. According to Eq. (4.17), the relationship of U_t and U_{t+1} can be described by Eq. (4.20).

$$U_t = R_t + \gamma \cdot U_{t+1} \tag{4.20}$$

Combining Eq. (4.18) and Eq. (4.20), $Q_\pi(s_t, a_t)$ becomes:

$$Q_\pi(s_t, a_t) = \mathbb{E}\left[R_t + \gamma \cdot U_{t+1} | s_t, a_t\right] = \mathbb{E}\left[R_t + \gamma \cdot Q_\pi(S_{t+1}, A_{t+1}) | s_t, a_t\right] \tag{4.21}$$

When using $Q(s_t, a_t; w)$ to approximate the optimal action-value function (4.19), $Q(s_t, a_t; w) \approx \max_\pi \mathbb{E}\left[U_t | s_t, a_t\right]$, and then Eq. (4.22) can be derived:

$$Q(s_t, a_t; w) \approx r_t + \gamma \cdot Q(s_{t+1}, a_{t+1}; w) \tag{4.22}$$

The expected return is $q_t = Q(s_t, a_t; w)$ without the observation of R_t, while the TD target, represented by y_t, can be derived from Eq. (4.22) after observing $R_t = r_t$.

$$y_t = r_t + \gamma \cdot Q(s_{t+1}, a_{t+1}; w) \tag{4.23}$$

The TD error is defined base on the difference of the expected return q_t and the TD target y_t as $\delta_t = q_t - y_t$. A good RL policy expects a small TD error. Consequently, the loss is defined as L_t in Eq. (4.24) and the gradient is derived by Eq. (4.25) when assuming y_t is not a function of w. The DQN is updated by performing a gradient decent: $w_{k+1} \leftarrow w_k - \alpha \cdot g_t$ where α is the learning rate in the training process [151], [152].

$$L_t = \frac{1}{2}\delta_t^2 = \frac{1}{2}\left[Q(s_t, a_t; w) - y_t\right]^2 \tag{4.24}$$

$$g_t \triangleq \left.\frac{\partial L_t}{\partial w}\right|_{w=w_t} = \delta_t \cdot \left.\frac{\partial Q(s_t, a_t; w)}{\partial w}\right|_{w=w_t} \tag{4.25}$$

4.3.3 Environment and Agent

The workflow of the RL based low level control is demonstrated in Fig. 4.12 where the agent and the environment are presented in detail. The DQN agent serves as the modulator that translates the stack voltage reference into semiconductors' gate signals of a single phase MMC in which a stack contains eight MBSMs.

The case study investigated here aims at tracking the stack voltage reference, maintaining SM capacitor voltage balancing, and minimizing the semiconductor switching frequency. As a result, the observation contains 11 variables, including the stack voltage reference $V_{S_{ref}}$, the stack current I_S, eight SM capacitor voltages $V_{C_{(1\ldots8)}}$, and MBSM states from the previous time step $S(t-1)$. Stack voltages are

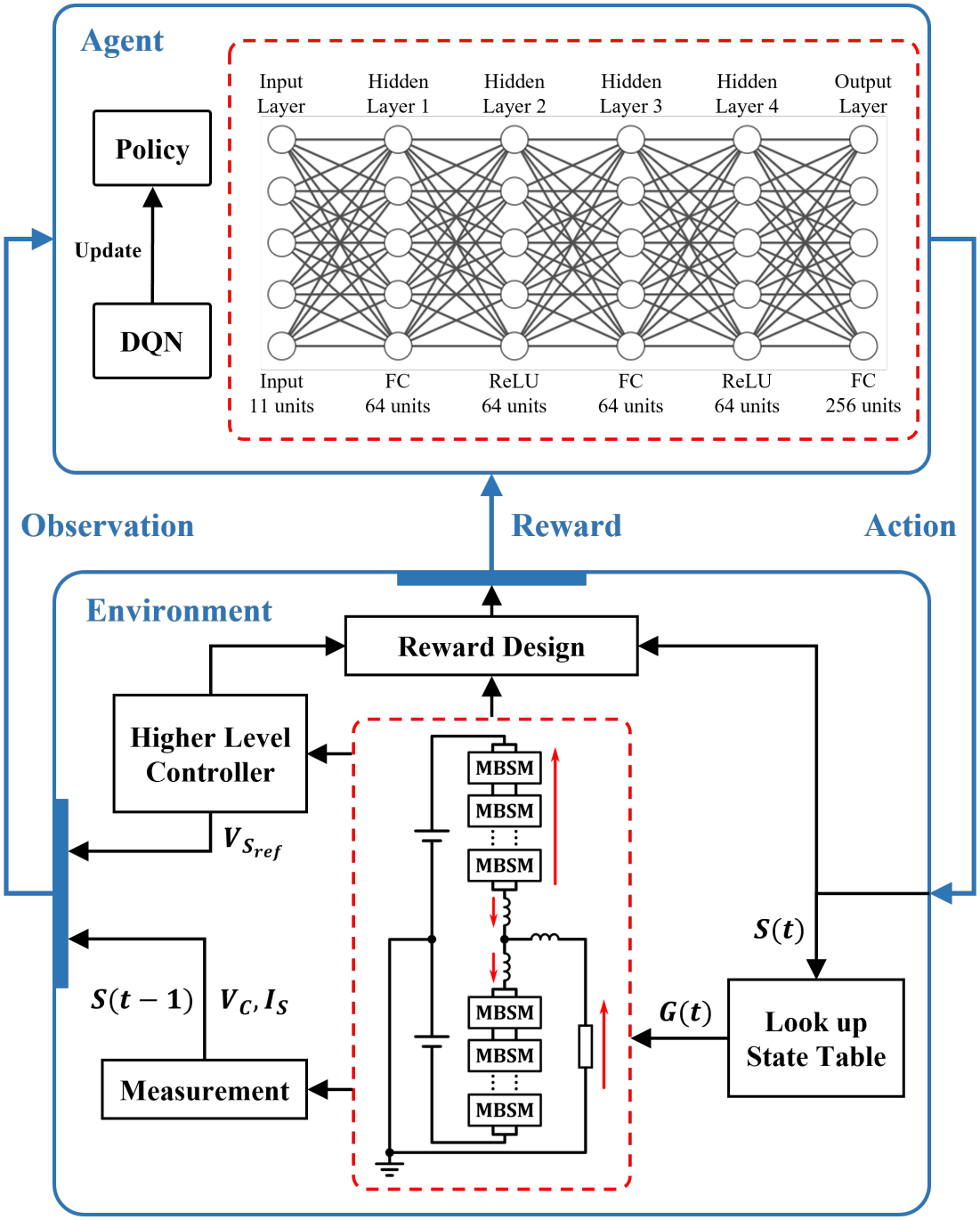


Figure 4.12: Work flow of the Reinforcement Learning based low level control

always non-negative in normal operation of the MMC, as presented in Fig. 2.16 and Fig. 3.9. The state of each MBSM is represented by 0 for soft parallel and bypass state, or 1 for positive insert state. Therefore, the states of eight MBSMs can be represented by one 8-bits binary number. For example, $S(t-1) = 3'd = 00000011'b$ is used to represent the condition in which MBSM 1-6 are soft-parallel and MBSM 7 and 8 are positively inserted. All possible states are consequently represented by one decimal variable in the range from 0 to 255. The purpose is for reducing the dimension of the observation, and moreover, reducing the computational resource required in the NN training process. Correspondingly, the action that the DQN agent generate is also a decimal variable representing MBSM states. $S(t)$ is translated into semiconductor gate signals $G(t)$ after being fed into a look-up table similar to Table 3.1.

The reward includes all of the performances that users are interested in. Similar to designing the objective function in MPC, the quantitative evaluation of different aspects should be considered in the design of the reward. The reward function $R(t)$ contains three parts, corresponding to the evaluation of the stack voltage tracking performance $R_V(t)$, the SM capacitor balancing performance $R_C(t)$, and the switching frequency reduction performance $R_S(t)$, as described by Eq. (4.26).

$$R(t) = w_1\, R_V(t) + w_2\, R_C(t) + w_3\, R_S(t) \tag{4.26}$$

with

$$R_V(t) = -\frac{|V_{S_{ref}}(t) - V_S(t)|}{V_{dc}} \tag{4.27}$$

$$R_C(t) = -exp\left[\frac{max\, V_C(t) - min\, V_C(t)}{V_{C_{rated}}} - 0.2\right] \tag{4.28}$$

$$R_S(t) = -\sum_{i=1}^{N_{SM}} \frac{|S'(t) - S'(t-1)|}{N_{SM}} \tag{4.29}$$

Here, t is the time index of the system, w_1, w_2, and w_3 represent the weight of each reward. The voltage tracking performance is evaluated by the difference of the voltage reference and the stack voltage in Eq. (4.27). The normalization

is achieved by dividing the difference by the rated DC voltage, which is equal to the maximum stack voltage output. The exponential in Eq. (4.28) criticizes over-larged SM voltage difference. The maximum voltage difference should be less than 20% of the rated SM voltage to ensure normal MMC operation[153]. In Eq. (4.29), $S'(t)$ is obtained from $S(t)$ after the integer-to-binary conversion. $\sum_{i=1}^{N_{SM}} |S'(t) - S'(t-1)|$ describes the number of MBSM states that change from time step $t-1$ to time step t.

4.3.4 Results and Analysis

The DQN updates the policy based on gradient decent every time step when the agent receives a reward in the training process. The input layer of the NN in the DQN agent contains 11 units, corresponding to the dimension of the observation. The output layer has 256 full-connected units which is determined by the size of the action set. The simulation model used to investigate the proposed RL based low level controller is a single phase MMC with a reduced number of MBSMs in each stack in order to reduce the time and computational resources required, especially in the training process. The MMC operates in inverter mode and provides stable sinusoidal AC voltage to a pure resistive load, as presented in Fig. 4.12. The model parameters are summarized in Table 4.2.

Table 4.2: Parameters of the RL based Low Level Control Simulation Model

Parameters	Value	Parameters	Value
DC Voltage	9600 V	Nominal V_C	1200 V
MBSM Capacitance	6.8 mF	N_{SM} per Stack	8
Load Resistance	50 Ω	AC Voltage Reference	4.5 kV
Stack Inductance	1.2 mH	AC Inductance	1.2 mH

The parameters of the DQN agent are summarized in Table 4.2. Due to the limited performance of the CPU used for RL training, the sample time is 0.1 ms, and the episode length is set at 2000. The simulation model runs for 0.2 seconds in each episode. The discount factor is set at 0.99 in order to improve future performance. Different numbers of hidden-layer units are investigated,

and the results show that 64 is the minimum number of units required for good performances.

Table 4.3: Parameters of the DQN Agent

Parameters	Value	Parameters	Value
Sample Time	0.1 ms	Learning Rate	0.005
Discount Factor	0.99	Batch Size	64
Epsilon Decay	0.003	Hidden Layer units	64
Maximum Episodes	1000	Episode Length	2000

The normalized rewards in the training process is presented in Fig. 4.13. Red line represents the episode reward, and blue line represents the 10-episodes moving average of the cumulative reward during training. The agent becomes stable after about 150 episodes.

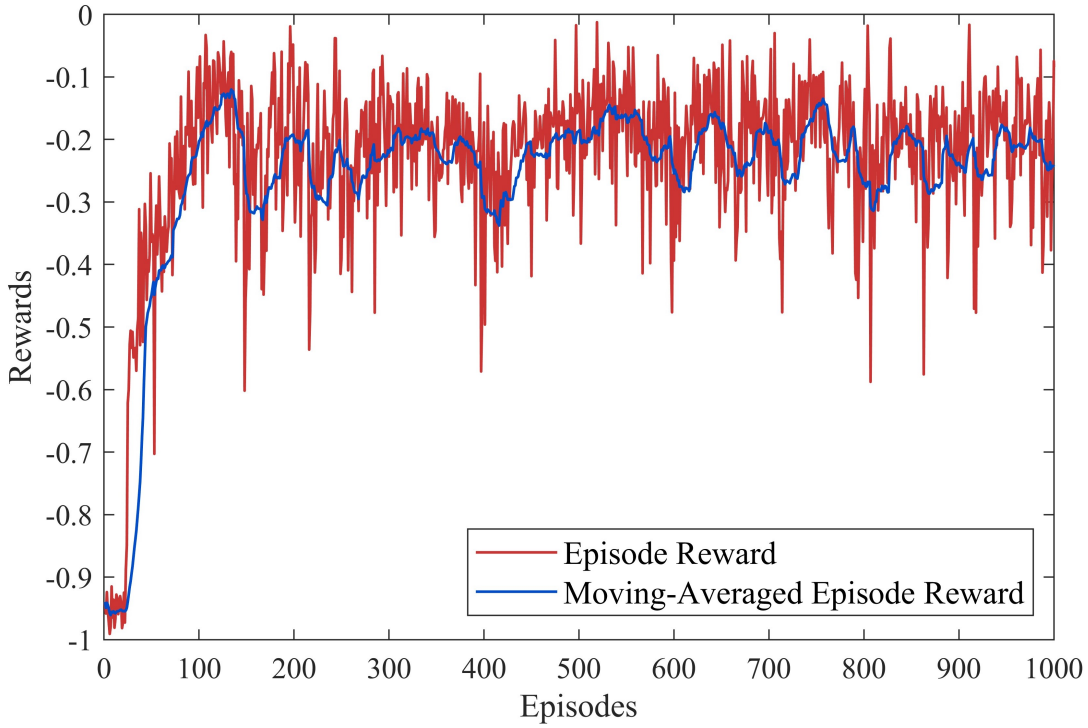


Figure 4.13: Normalized rewards in the training process.

Fig. 4.14 presents the stack voltage with the proposed RL controller. The waveform is an approximate staircase wave that is similar to the result from NLM modulation. Though some oscillation happens at around t=0.156s, the

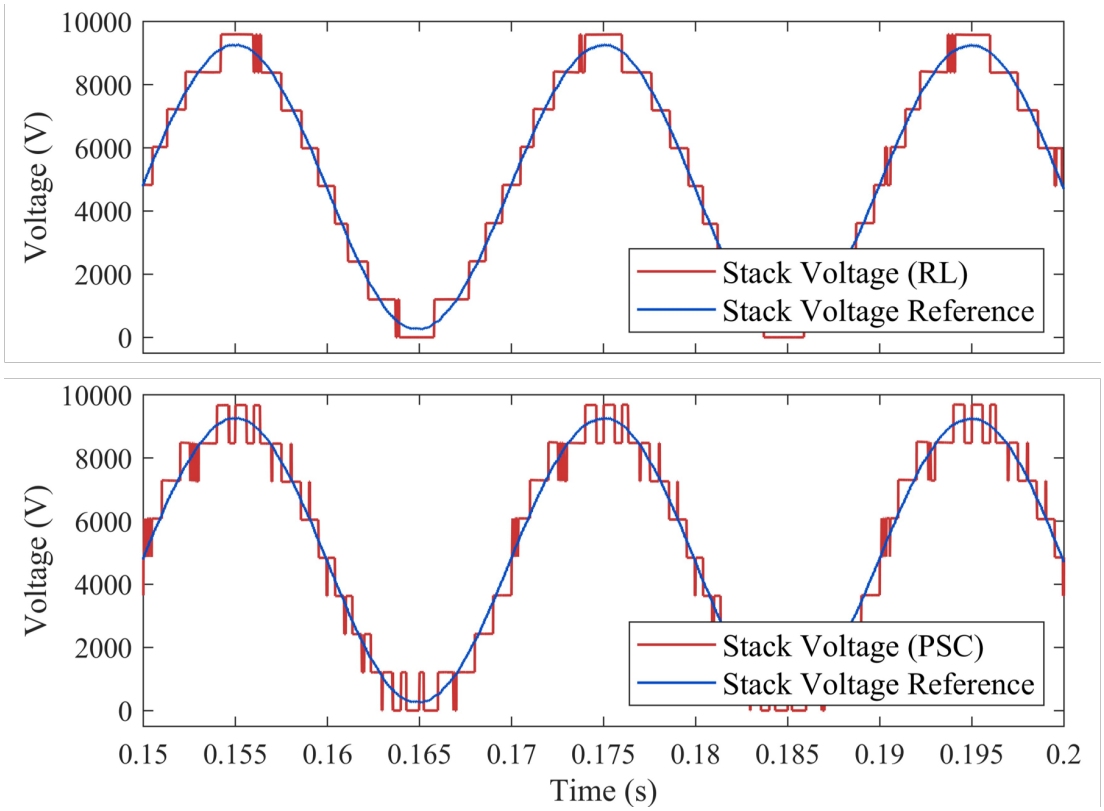


Figure 4.14: Stack voltages with different low level controllers

stack voltage still tracks the reference (blue lines) well. In comparison, the stack voltage with PSC based low level control, which has been introduced in Section 3.1.3, is also presented in Fig. 4.14. Several numerical simulations are carried out, and the results show that a PSC operating at 1250 Hz has roughly the same stack voltage THD (8.23%) as the RL controller (8.07%). The maximum frequency for THD calculation is 20 times of the fundamental frequency, 1000 Hz, as high order harmonics can be easily suppressed by inductors.

The maximum SM capacitor voltage deviations with the proposed RL based controller and with a 1250 Hz PSC low level controller are both presented in Fig. 4.15. Both of the deviations are far away from the margin, 20% of the rated SM voltage. The capacitor balancing performance of the RL controller is slightly better than that of the PSC controller.

Fig. 4.16 investigates the effect of different weights on the number of MBSM stats changes. Red line represents the result when the initial linear-penalty weights, $w_1 = 0.6$, $w_2 = 0.3$, and $w_3 = 0.1$, are applied. Yellow line repre-

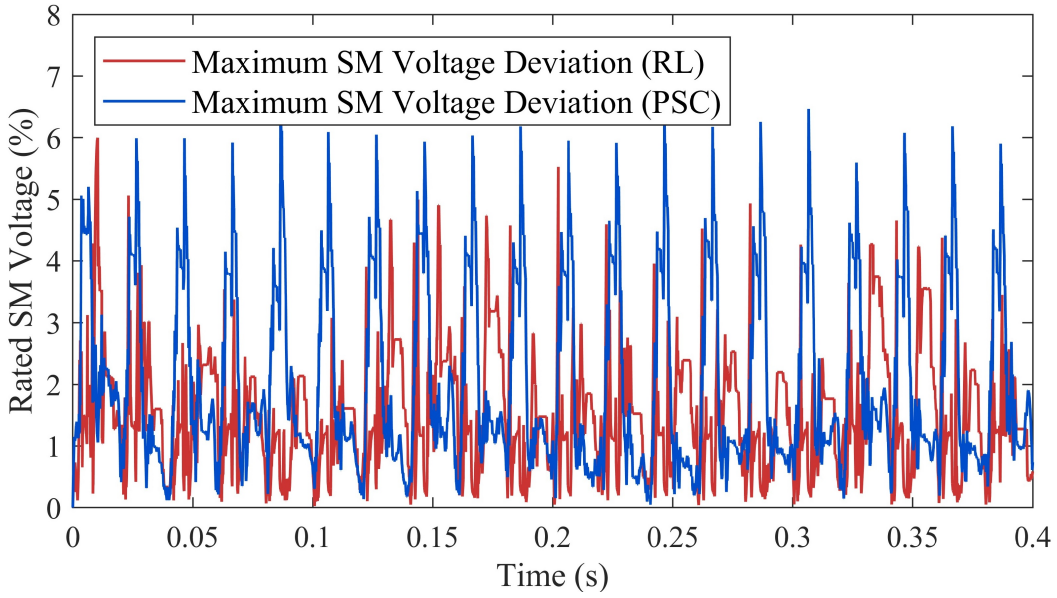


Figure 4.15: Maximum SM voltage deviation with different low level controllers

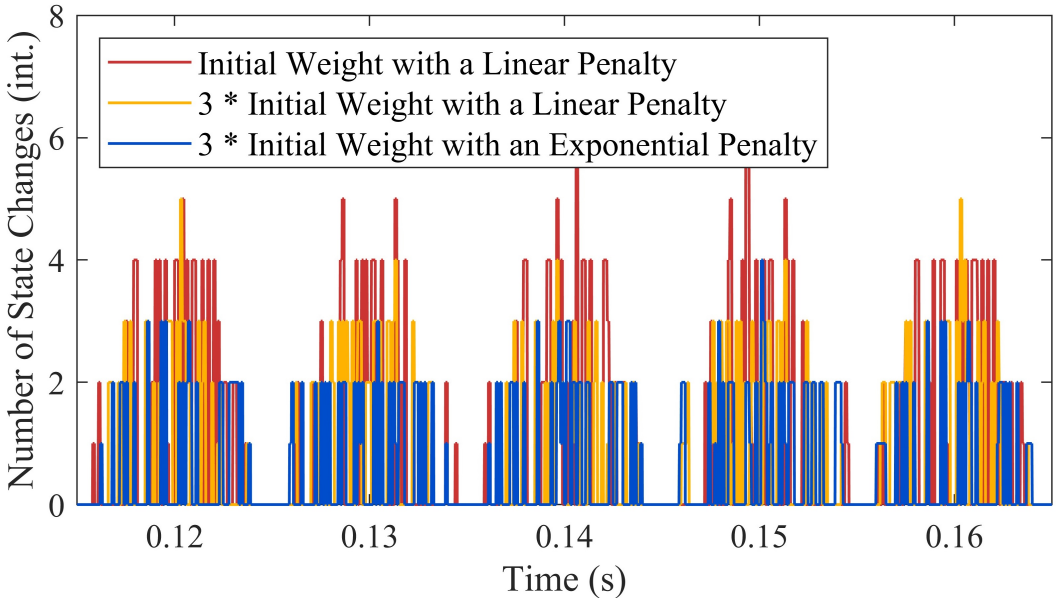


Figure 4.16: State Changes with different weights of Eq. (4.29)

Table 4.4: State Change Frequency with Different Weights of Eq. (4.29)

Low Level Control Scheme	MBSM State Change Frequency
PSC, 1250Hz	964 Hz
RL, $w_3 = 0.1$, Linear Penalty	937 Hz
RL, $w_3 = 0.3$, Linear Penalty	783 Hz
RL, $w_3 = 0.3$, Exponential Penalty	521 Hz

sents the result when $w_1 = 0.6$, $w_2 = 0.3$, and $w_3 = 0.3$. Blue line represents the result when $w_1 = 0.6$, $w_2 = 0.3$, and $w_3 = 0.3\, e^{N_{SC}}$. Here, $e^{N_{SC}}$ is an exponential part to penalize large number of state changes, where N_{SC} is the number of state changes in one sample step. Fig. 4.16 and Table 4.4 demonstrate that reasonably adjusting the reward design is a potential solution for further improving the performances of the RL-based low-level controller. Lower state change frequencies can be achieved without affecting the stack voltage tracking or SM voltage balancing.

4.4 Summary

To support the development of more powerful, yet more complex power electronics circuits, designers require the use of advanced control systems, themselves based on extensive models of the circuits. Section 4.1 presents an algorithm which automatically extracts the state space model of an electrical circuit using its netlist. The algorithm also identifies the base state representation in case of dependencies between reactive elements. The full state space model is then made available for more extensive analysis of all the dynamics of the circuit. The effectiveness has been verified in a simple electrical circuit case and furthermore the case of MMC.

Section 4.2 introduces the MPC based start-up control algorithm of the MBSM MMC. The proposed capacitor pre-charge algorithm and the structure of MBSMs not only allow the MMC to operate independently without grid, but also simplify the problem down to a DCDC converter control issue. Thanks to the characteristics of MPC, the charge current is well controlled. Voltage and current performances during start-up procedure and the transient process from start-up to normal operation have proved the effectiveness of the proposed controller.

The RL based MBSM low level control algorithm is presented in Section 4.3. The DQN agent is applied as the controller, and TD algorithm is used to train the NN. Stack voltage tracking performance, SM capacitor balancing performance ,and switching frequency reduction performance are all consider while designing

the reward. Results show that the RL based controller can effectively reduce the MBSM state change frequency while maintaining the stack voltage tracking and SM balancing. The simulation is based on a single-phase model with eight MBSMs in each stack due to computing resource constraints (CPU in personal computer). Training larger DQN networks with commercial GPU clusters could help to improve performance even further.

Chapter 5

MBSM Applications

5.1 Modular Multilevel STATCOM

The continuously increasing proportion of distributed renewable energy has been giving rise to more challenges for reliability and robustness of the power grid. An effective solution to increase the stability of AC grid is Flexible AC Transmission Systems [154], among which Static compensator (STATCOM) is widely implemented to provide power quality management and voltage support by releasing and absorbing reactive power. Enhanced frequency stabilization against disturbance or unbalance is also offered with partially rated energy storage (ES) system integrated as active power can be exchanged between STATCOM and the AC grid [155, 156].

For medium and high voltage applications, e.g. large scale wind farms [157], MMC style topologies is usually integrated into STATCOM to increase its voltage level and meanwhile reduce harmonic distortion and switching frequency. In each converter arm, several SMs are connected in series to generate staircase AC voltage waveform with capacitor voltages. Efforts and costs of periodical preventive maintenance are also reduced thanks to the modular design of SMs, especially in offshore converter stations [158]. Generally, FB is the first choice for SMs in MMC-STATCOM as HB is not able to output negative SM voltages, even though HBSMs are popular in classic MMC, in which only positive stack voltages are constructed during normal operation.

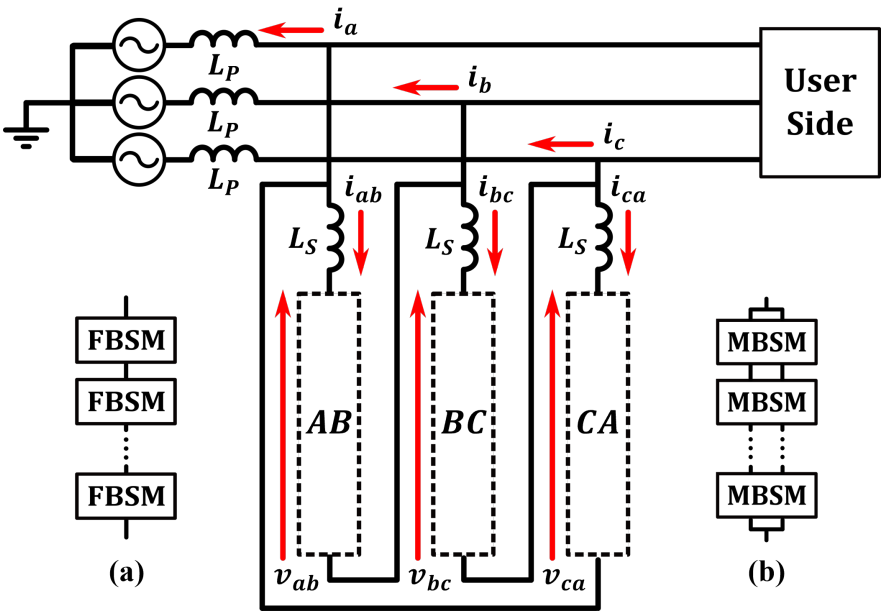


Figure 5.1: Topology of a delta configured modular multilevel STATCOM

5.1.1 STATCOM Modelling and Higher Level Control

Fig. 5.1 illustrates a typical MMC-STATCOM (also commonly referred to as a Cascaded H-Bridge) with delta configured arms so that additional circulating current can be applied to promote the SM voltage balancing. The connection manner of FBSMs within an arm is also presented in Fig. 5.1 (a).

The standard single-bus SMs, especially in partial rated ES topology, typically requires additional circulating current to maintain SM voltage balancing as well as suppress ripple current [159]. Additional circulating current, on the other hand, causes higher power losses and higher temperature rises in semiconductor junctions. Consequently, more challenges are faced in the cooling system design to ensure that the junction remains within its safe range. The MBSM proposed in this thesis provides ideas to solve the above problems by distributing the stack current to doubled conduction paths, as shown in Fig. 5.1(b). According to Fig. 5.1, the dynamics of a delta configured STATCOM can be described by loop voltage ordinary differential equations:

$$\begin{cases} u_a - u_b + L_P\dfrac{di_a}{dt} - L_S\dfrac{di_{ab}}{dt} - v_{ab} - L_P\dfrac{di_b}{dt} = 0 \\ u_b - u_c + L_P\dfrac{di_b}{dt} - L_S\dfrac{di_{bc}}{dt} - v_{bc} - L_P\dfrac{di_c}{dt} = 0 \\ u_c - u_a + L_P\dfrac{di_c}{dt} - L_S\dfrac{di_{ca}}{dt} - v_{ca} - L_P\dfrac{di_a}{dt} = 0 \end{cases} \tag{5.1}$$

where u_a, u_b, u_c represent three phase AC voltage, L_P and L_S represent phase inductance and stack inductance. Besides, the current relationships are decribed by Eq. (5.2).

$$\begin{cases} i_a + i_b + i_c = 0 \\ i_a + i_{ab} - i_{ca} = 0 \\ i_b + i_{bc} - i_{ab} = 0 \\ i_c + i_{ca} - i_{bc} = 0 \end{cases} \tag{5.2}$$

The dynamics can be rearranged and reduced to a base state space model with independent states [160] and regulated by LQR [161] based state feedback controller as introducted in Chapter 2. The MBSMs investigated in the following sections within this chapter all operate in STATCOM mode.

5.1.2 Energy Storage in MBSM

Instead of implementing the ES elements into a large scale and concentrated pack, as has been introduced in [162], the characteristics of MMC-STATCOM allow ES to be distributed into the SMs themselves. The management of ES conditions, e.g. state of charge and state of health, are additionally integrated into converter control algorithm. Many excellent works have been done on the joint regulation of converter control and ES management. Ref. [163] analyses different operating modes in an ES-MMC and develop control algorithms that offer the flexibility to directly manipulate the active power components for state of charge balancing of the batteries. The MMC with partially rated integrated ES and its control system proposed in [164] is suitable for frequency support and ancillary service provision such as decoupled power oscillation damping. In [165], the partially rated energy storage (PRES)-STATCOM capable of providing both reactive and

active power support and voltage balancing algorithm are introduced together.

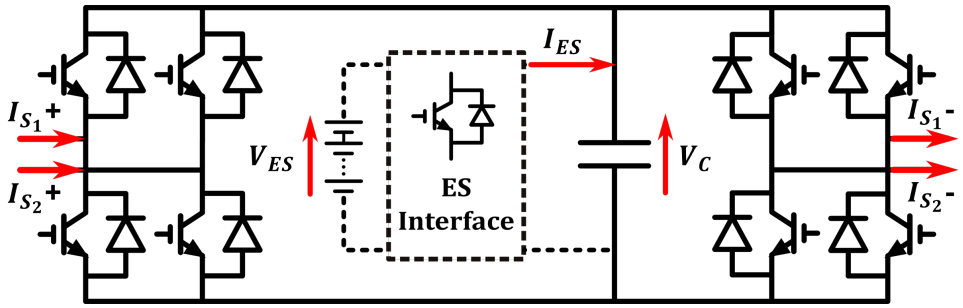


Figure 5.2: MBSM with energy storage (ES-MBSM)

Fig. 5.2 depicts how ES interface is connected to SM capacitor. The interface could be through a passive filtering network, or through an actively controlled DC/DC converter, such as buck-boost converter or dual active bridge for isolated applications. When the interface is disabled, the ES-SM becomes a normal SM. The ES interface will be modelled as a controlled current source in simulation and analysis of its specific structure is not the focus of this chapter.

5.2 The PRES MBSM STATCOM

This section presents a delta-configured, modular multilevel, STATCOM based on MBSM topology where PRES are distributedly integrated in MBSMs to provide ancillary service, e.g. frequency support, in addition to the classic reactive power provision. The study uses the analytical formulation of the MBSM to derive the control system and the optimal phase angle of the circulating current required for SM balancing. Apart from the soft-parallel based mode, the proposed STATCOM can also operate in the FBSM based mode to extend its capability of generating active power. A comparison of different operating modes (MBSM vs emulated full-bridge SM) is presented and confirmed by simulation results. Analysis indicates that the MBSM improves the power efficiency (30.5% total losses reduction at the 1 pu reactive power set-point and 3.56% reduction at 1 pu active power set-point) compared with the conventional FBSM, at the cost of doubling the number of semiconductor devices; but not the number of sub-modules. The capacitor balancing is achieved without the use of additional inductors compared

with double FBSM.

5.2.1 Low Level Control System

Thanks to the flexibility provided by the distributed control framework, as introduced in Chapter 2, the MBSM STATCOM can share the same soft-parallel based low level control scheme with the MBSM MMC. Besides, the low level control system proposed in this section includes another mode, named the FBSM based mode, to further extend the active power capability of the MBSM STATCOM.

Fig. 5.3 presents the flowchart of the proposed low level control system. The initialization involves importing the stack voltage reference $V_{S_{ref}}$, capacitor voltages V_C, stack current I_S and the counter value t. The first step is dynamically selecting the operation mode of the MBSM STATCOM to maintain voltage balancing and meanwhile lower down the power losses to the greatest extent. The mode selection follows a hysteresis manner: The conventional FBSM based mode is selected if $\overline{V_{ES}} - \overline{V_{cap}} > V_{Thr}$ until the difference decreases to zero, where $\overline{V_{ES}}$ represents the average voltage of ES-MBSMs, $\overline{V_{cap}}$ is the average voltage of normal MBSMs, and V_{Thr} is the voltage threshold, to bring MBSMs back to balance as soon as possible. Or, the MBSM STATCOM will stay in the soft-parallel based mode operating under the control algorithm introduced in Section 3.1.3. The counter t is used to switch states between Fig. 3.4 (a) and (b), or between Fig. 3.4 (c) and (d), after a fixed number of controller steps (T). Such arrangement can avoid excessive switching of semiconductors at specific positions, helping on reducing the risk of wear out failure.

In conventional FBSM based mode, the MBSM is regarded as a whole to define states Positive Voltage (1), Zero Voltage (0) and Negative Voltage (-1), as presented in Fig. 3.3 (a1), (a2), (a3), and (a4). At first the sorted index R is obtained by ranking all MBSMs by their absolute deviation from the average capacitor voltage $\overline{V_C}$. The initial value of iterations are set as $V_{ref}(1) = V_{S_{ref}}$ and $V_{avail}(1) = \sum V_C$. Eq. (5.3) summarizes the criteria of preferential states, where the MBSM whose voltage $> \overline{V_C}$ is discharged and those whose voltage$\leq \overline{V_C}$ is charged with I_S.

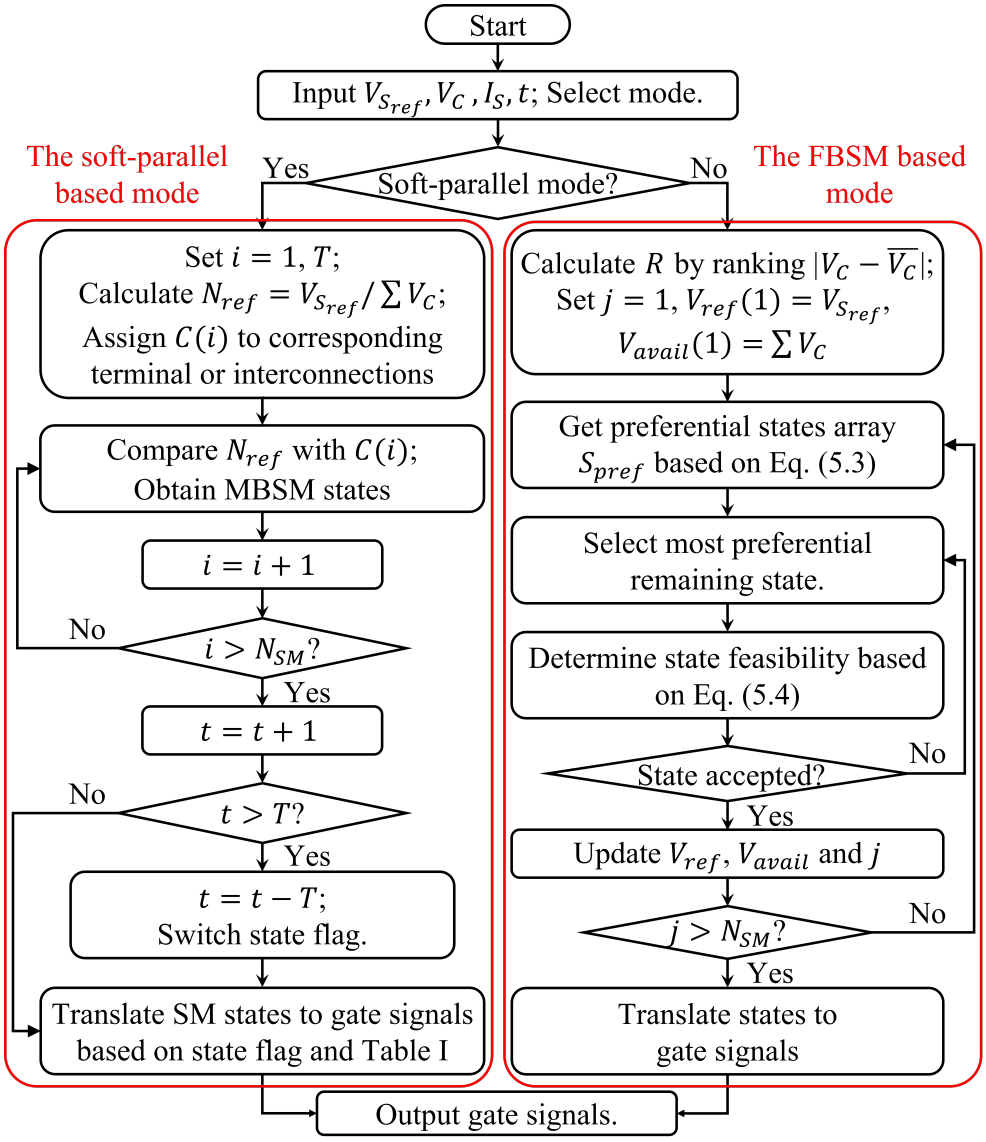


Figure 5.3: The proposed low level control system for the PRES STATCOM

$$S_{pref}(j) = \begin{cases} [1, 0, -1], \ if \ (V_C(R(j)) - \overline{V_C}) \cdot I_S \leq 0 \\ [-1, 0, 1], \ if \ (V_C(R(j)) - \overline{V_C}) \cdot I_S > 0 \end{cases} \tag{5.3}$$

The feasibility of the most preferential state, determined by Eq. (5.4), will be certificated if no potential voltage limit violation is found. Or the state will be discarded and the subsequent remaining state in the array is tested. The parameters V_{ref}, V_{avail} and j are then updated and processed to the next iteration until states of all MBSMs are assigned. The semiconductor states are consequently obtained based on the MBSM state and state shown in Fig. 3.3 (a1), (a2), (a3),

and (a4).

$$\begin{cases} 1, & if \ \ |V_{ref} - V_C(R(j))| \leq V_{avail} - V_C(R(j))/2 \\ 0, & if \ \ |V_{ref}| \leq V_{avail} - V_C(R(j))/2 \\ -1, & if \ \ |V_{ref} + V_C(R(j))| \leq V_{avail} - V_C(R(j))/2 \end{cases} \tag{5.4}$$

5.2.2 Theoretical Analysis

Optimal Phase Angle of the Additional Circulating Current

Generally, MBSMs can operate in either soft-parallel based mode or conventional FBSM based mode. When injecting active power from the ES-STATCOM to the external grid, the ES interfaces always charge the capacitor in ES-MBSMs. It should be ensured that the ES-SM outputs the same amount of active power as it received from the ES interface at the end of each cycle to maintain voltage balancing. Additional third harmonic circulating current (I_{3rd}) is injected in the delta-configured loop to improve the capability of MBSMs for active power exchanging. I_{3rd} will not change the AC current or cause any interference to the overall energy balance of the converter as it does not contain any fundamental component.

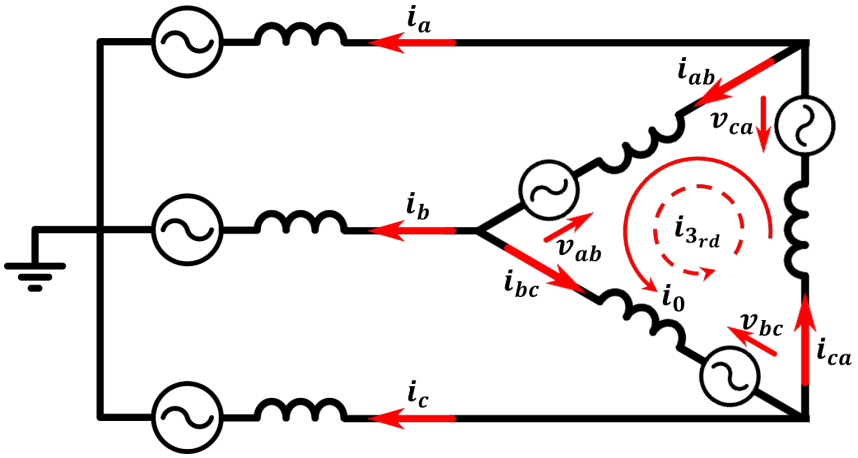


Figure 5.4: Equivalent circuit for current analysis

Fig. 5.4 illustrates the equivalent circuit for current analysis. The overall stack current reference involves: (1) Phase current I_{ph} (i_{ab}, i_{bc}, i_{ca}) that contribute to the AC output; (2) Zero sequence circulating current I_0 for balancing the energy

stored in each stack; and (3) Additional 3rd harmonic circulating current I_{3rd} for maintaining voltage balancing between ES-MBSMs and normal MBSMs. The stack current reference is:

$$I_{S_{ref}} = I_{ph} + I_0 + I_{3rd} \tag{5.5}$$

Assuming the STATCOM operates in steady state where energy is distributed evenly among three stacks and I_0 becomes negligible. Define the phase of I_{ph} and the phase of I_{3rd} as $\phi_{I_{ph}}$ and $\phi_{I_{3rd}}$, respectively. The overall stack current reference becomes:

$$I_{S_{ref}} = \hat{I_{ph}} \cdot sin\left(wt + \phi_{I_{ph}}\right) + \hat{I_{3rd}} \cdot sin\left(3wt + \phi_{I_{3rd}}\right) \tag{5.6}$$

Apply $\theta = wt + \phi_{I_{ph}}$, and $\Delta\varphi = \dfrac{\phi_{I_{3rd}}}{3} - \phi_{I_{ph}}$, Eq. (5.6) becomes:

$$I_{S_{ref}} = \hat{I_{ph}} \cdot sin\,\theta + \hat{I_{3rd}} \cdot sin\,3(\theta + \Delta\varphi) \tag{5.7}$$

Capacitors in ES-MBSMs are charged by ES current. The higher active power the STATCOM output, the larger the ES current will be. It should be ensured that the capacitor voltage at the start of each cycle is equal to the capacitor voltage at the end of the same cycle to maintain voltage balancing, which means the voltage deviation caused by ES current should be offset by voltage deviation caused by stack current. As a result, the optimal phase angle should maximize the capability of the phase current to offset the voltage deviation caused by ES current in a whole cycle. Besides, according to Eq. (5.7), stack current is composed of a sine wave in fundamental frequency and a sine wave in the 3rd harmonics. The positive half cycle of the stack current is symmetrical to the negative half cycle. Consequently, the optimal phase angle of I_{3rd} should maximize the voltage deviation caused by the total stack current in a half cycle. The variation of capacitor voltage caused by stack current in the positive half cycle is:

$$\begin{aligned}\Delta V_C &= \frac{1}{C}\int_0^{\pi} \hat{I_{ph}} \cdot sin\,\theta + \hat{I_{3rd}} \cdot sin\,3(\theta + \Delta\varphi)\,d\theta \\ &= \frac{2}{C} \cdot \hat{I_{ph}} + \frac{2}{3C} \cdot \hat{I_{3rd}} \cdot cos\,(3\Delta\varphi)\end{aligned} \tag{5.8}$$

ΔV_C is maximized when $cos\,(3\Delta\varphi) = 1$, as a result:

$$\Delta\varphi = \frac{\phi_{I_{3rd}}}{3} - \phi_{I_{ph}} = 0 \tag{5.9}$$

The STATCOM operating point describes how much active power and reactive power are released by the converter, represented by p.u. value P_{ref} and Q_{ref}, respectively. Denote the phase angle of stack voltage as $\phi_{U_{ph}}$, the operating point is described as:

$$\begin{cases} P_{ref} = cos\,(\phi_{U_{ph}} - \phi_{I_{ph}}) \\ Q_{ref} = sin\,(\phi_{U_{ph}} - \phi_{I_{ph}}) \end{cases} \tag{5.10}$$

So, $\phi_{I_{ph}}$ can be represented with converter operating point and $\phi_{U_{ph}}$:

$$\phi_{I_{ph}} = \phi_{U_{ph}} - \arctan\,(\frac{Q_{ref}}{P_{ref}}) \tag{5.11}$$

The derivation of $\phi_{U_{ph}}$ can be found in ref. [166]. Notice that the reference direction of stack voltage applied in this paper, as shown in Fig. 5.1 and Fig. 5.4, is opposite to that in the literature. So we have:

$$\phi_{U_{ph}} = \frac{2\pi(m-1)}{3} - \frac{\pi}{6} \tag{5.12}$$

where m = 1, 2, 3 representing the sequence of three phase. Combine Eq. (5.9), Eq. (5.11), and Eq. (5.12), the optimal phase angle of I_{3rd} is:

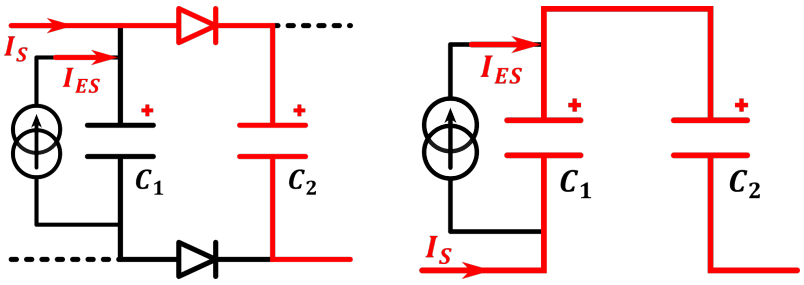
$$\phi_{I_{3rd}} = 3 \cdot \phi_{I_{ph}}\ mod\ 2\pi = \frac{3}{2}\pi - 3\arctan\,(\frac{Q_{ref}}{P_{ref}}) \tag{5.13}$$

Comparison of Different Operation Modes

Depending on the MBSM states, ES-MBSM capacitor charging current has three cases: (1) $I_{ES} + |I_S|$ when I_S flow into the anode of the capacitor, (2) $I_{ES} - |I_S|$ when I_S flow into the cathode of the capacitor and (3) I_{ES} when the capacitor is bypassed. In comparison, the charge current of capacitor in normal MBSMs is $|I_S|$, $-|I_S|$ or 0. Soft-parallel mode enables I_S to flow into the capacitors with lower voltage than their neighbours. The energy management controller keeps the total energy stored in the stack balanced during operation, so in most cases the voltage of ES-MBSM tends to be greater than the rated value, while voltage of capacitor in normal MBSM deviates to a lower value. I_{ES} and I_S flowing through a ES-MBSM and a normal MBSM next to it in soft-parallel mode are shown in Fig. 5.5 (a). I_{ES} is all injected to C_1 because of the diodes and consequently $V_{C_1} > V_{C_2}$, resulting in I_S flowing in C_2. Then the voltage difference decreasing speed is:

$$\frac{d\Delta u}{dt} = \frac{1}{C_{SM}} \left(I_{ES} - |I_S| \right) \tag{5.14}$$

The absolute value of the stack current needs to be larger than I_{ES} to reduce the voltage difference.



(a) (b)

Figure 5.5: ES current and stack current flowing through a ES-MBSM and a normal MBSM in (a) Soft-paralleling based mode, (b) FBSM based mode.

When the MBSMs operate in conventional FBSM based mode, I_S tends to charge the capacitor whose voltage is higher than average value, while discharge those whose voltage is lower, to accelerate the SM voltage balancing. The current state is shown in Fig. 5.5 (b). The voltage difference can be reduced as long

as $|I_S| > I_{ES}/2$ according to the voltage difference decreasing speed calculated in (5.14):

$$\frac{d\Delta u}{dt} = \frac{1}{C_{SM}} \left(I_{ES} - 2 \left| I_S \right| \right) \tag{5.15}$$

Less stack current is required for voltage balancing than the former mode. Consequently, the conventional FBSM based mode is more powerful than the soft-parallel based mode in terms of reducing the voltage deviation while the same amount of circulating current is injected.

While operating in the soft-parallel based mode, the interconnection states of the MBSMs are obtained by compare the modulation index with PWM carriers. Based on the semiconductor states summarized in Table 3.1, at most four semiconductors (out of eight semiconductors in an interconnection) change their states in each SM state transition, so the average semiconductors switching frequency is less than the PWM frequency. In contrast, in the FBSM based mode the gate signals are updated after every controller step. The switching loss when operating at the soft-parallel based mode is consequently lower than that in the FBSM based mode.

5.2.3 Simulation Results and Discussion

Simulation models of partially rated ES STATCOMs in 4 different configurations are built in MATLAB/Simulink to evaluate the converter performances and the proposed control system. The system parameters are summarized in Table 5.1. The quantity ratio of ES-MBSMs to total MBSMs in a stack is 9/15 (60%). ES-MBSMs are distributed evenly in the stack. V_{Thr} is set at 2.5% of the nominal capacitor voltage (50V) to determine the operation mode. I_{Thr} is determined by the current measurement resolution and communication bandwidth, and is set as 50A in simulation. In all simulations, the STATCOM output 1 p.u. apparent power while only the power factor (PF) changes.

Table 5.1: System Parameters

Parameters	Value	Parameters	Value
Nominal Power	30 MVA	N_{sm} per Stack	15
AC Voltage (RMS)	18 kV	Nominal V_{sm}	2000V
AC Frequency	50 Hz	MBSM Capacitance	2.5 mF
Phase Inductance	0.1 pu	Sampling Time	5 μs
Stack Inductance	0.1 pu	PWM Frequency	1 kHz

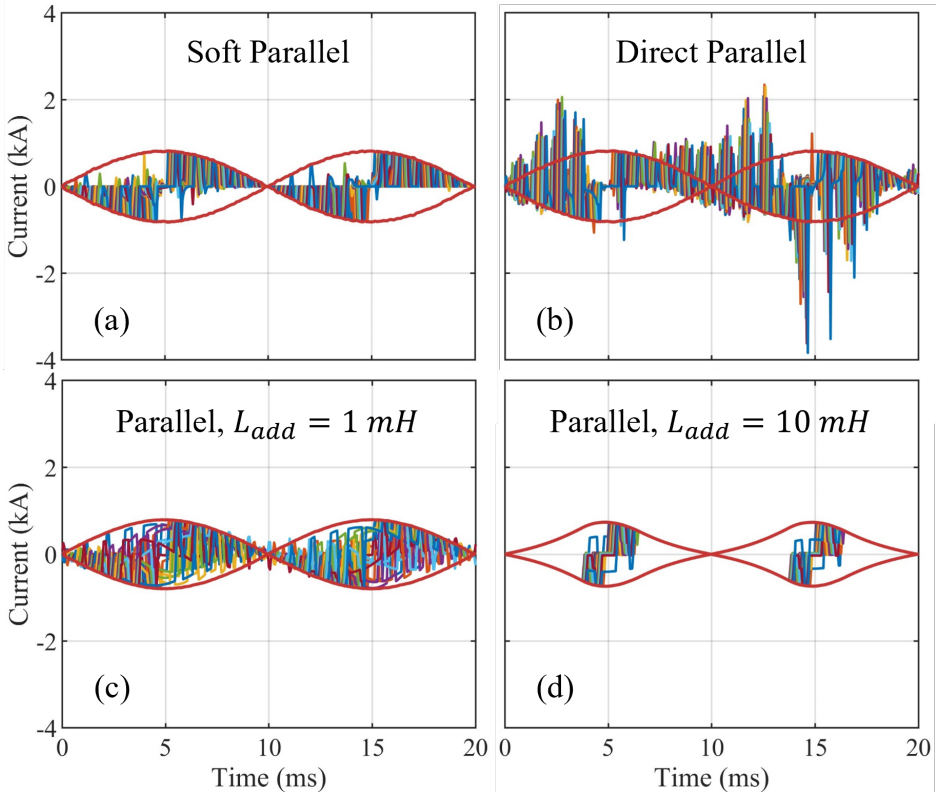


Figure 5.6: Instantaneous capacitor currents with different parallel mechanism: (a) Soft parallel; (b) Direct parallel; (c) Parallel through 1 mH inductors; (d) Parallel through 10 mH inductors. Capacitor currents are represented in coloured lines; Red lines represent the envelop of stack current.

Table 5.2: ΔV_{SM} and I_{cap} in MMSPC versus L_{add} when Power Factor = 0

L_{add} (H)	10^{-8}	10^{-7}	10^{-6}	10^{-5}	10^{-4}	10^{-3}
ΔV_{sm} (V)	137	142	222	338	480	671
I_{cap} (A)	3775	3296	2337	1936	1241	835

Table 5.3: ΔV_{SM} in MBSM and in MMSPC versus Power Factors

Power Factor		0	0.1	0.2	0.3
ΔV_{sm} (V)	MBSM, Soft parallel	159	172	276	402
	MMSPC[74], L_{add} = 1mH	671	692	745	890

Effectiveness of the Soft-parallel mechanism in STATCOM

The fundamental benefit of the soft-parallel over MMSPC [74, 46] is to suppress the inrush current resulted by capacitor parallel without the requirement of using additional inductors. Instantaneous capacitor currents (I_{cap}) with different parallel mechanism when the STATCOM operating at PF = 0 output are investigated. As has been explained in Section II, with soft-parallel I_{cap} is restricted by the envelop of stack current as the capacitor voltage difference is clamped by the reverse blocked diodes, as is shown in Fig. 5.6 (a). Direct parallel leads to large inrush current, the amplitude of which is about four times of the stack current, as in Fig. 5.6 (b). Fig. 5.6 (c) and (d) demonstrate the effect of different inductance to inrush current in MMSPC. Similar I_{cap} suppression performance as the soft-parallel mechanism can be achieved with L_{add} = 1 mH. However, large harmonics occurs in the stack current when L_{add} = 10 mH. SM voltage deviation (ΔV_{SM}) is also of great interest and is suggested to be keep lower than 20% of the rated SM voltage [153] as it determines the AC output quality as well as the volume and cost of SM capacitors. ΔV_{SM} and I_{cap} in MMSPC versus different L_{add} are listed in Table 5.2. It can be summarised that as the applied inductance increases, so does ΔV_{SM}, while I_{cap} decreases. $L_{add} < 1$ mH can't effectively suppress I_{cap}. In the simulation of MMSPC, L_{add} = 1 mH to fairly compare ΔV_{SM} versus different power factors with the soft-parallel method, as listed in Table 5.3. The result indicates MMSPC may not capable enough for a PRES STATCOM as the ΔV_{SM} is already larger than 20% of the rated SM voltage when PF = 0.3.

Normal Operation

The converter ability of reactive power compensating as well as providing active power for frequency support, are verified by simulation results. Three different

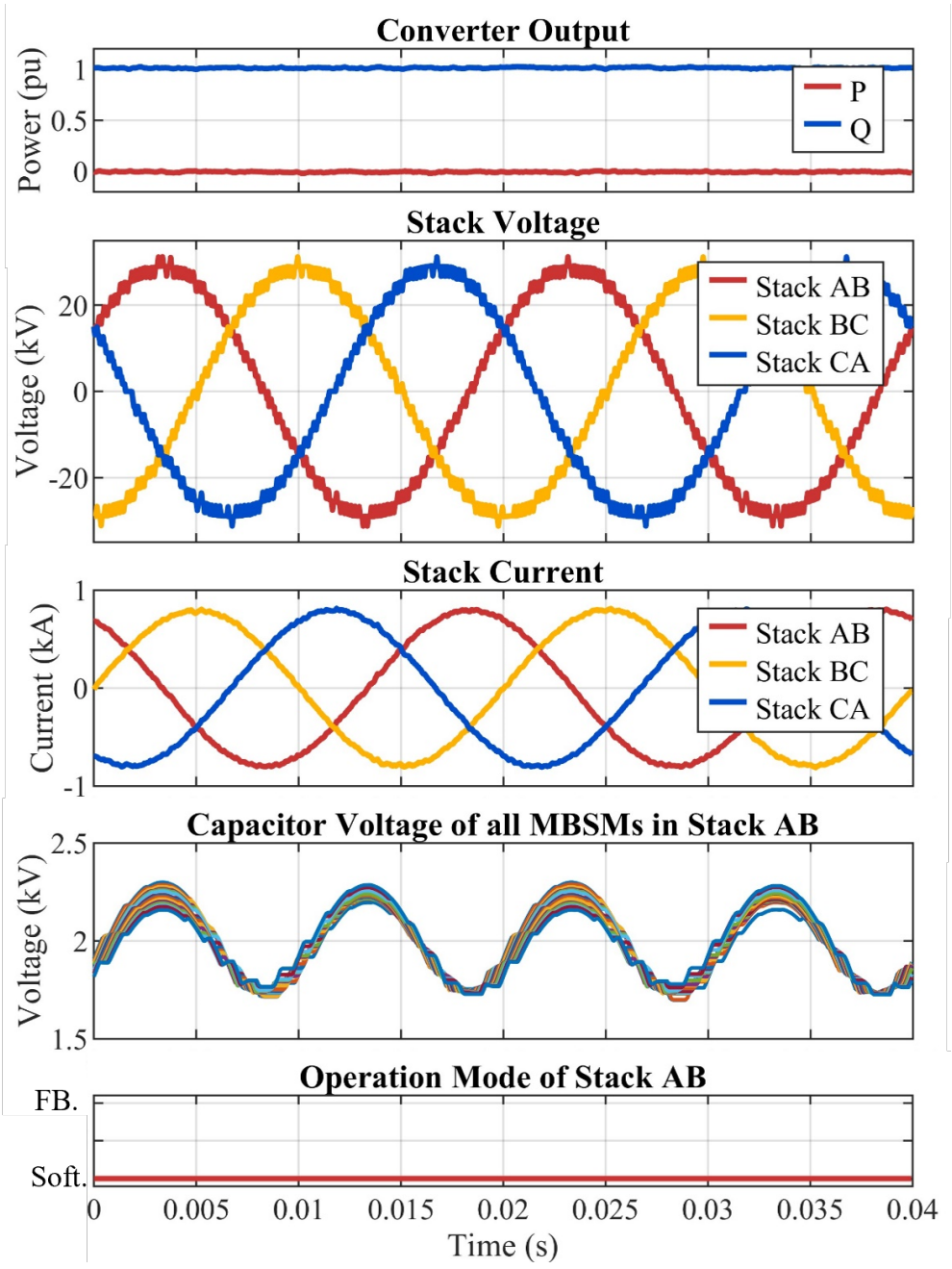


Figure 5.7: Converter performances when PF = 0

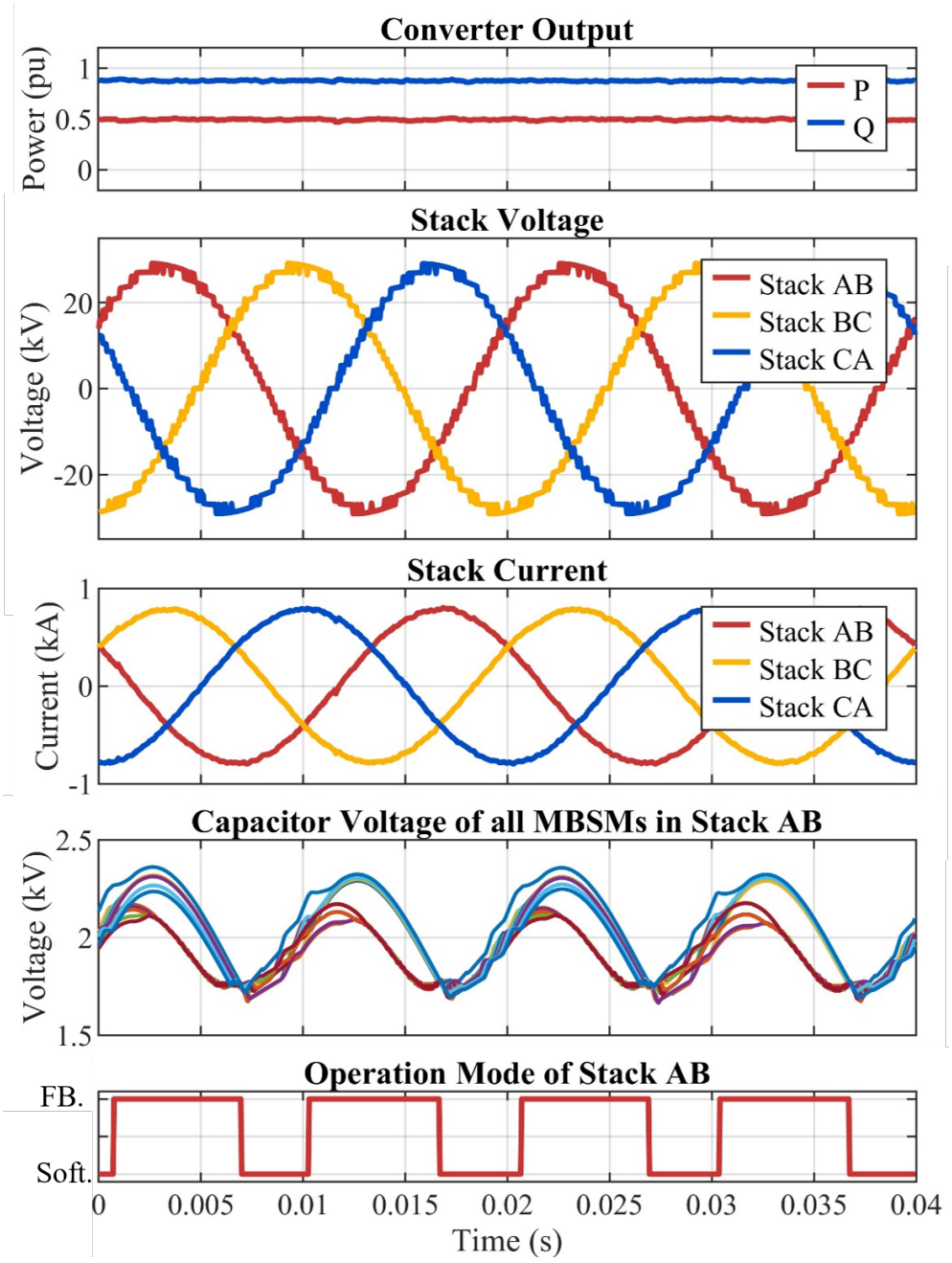


Figure 5.8: Converter performances when PF = 0.5

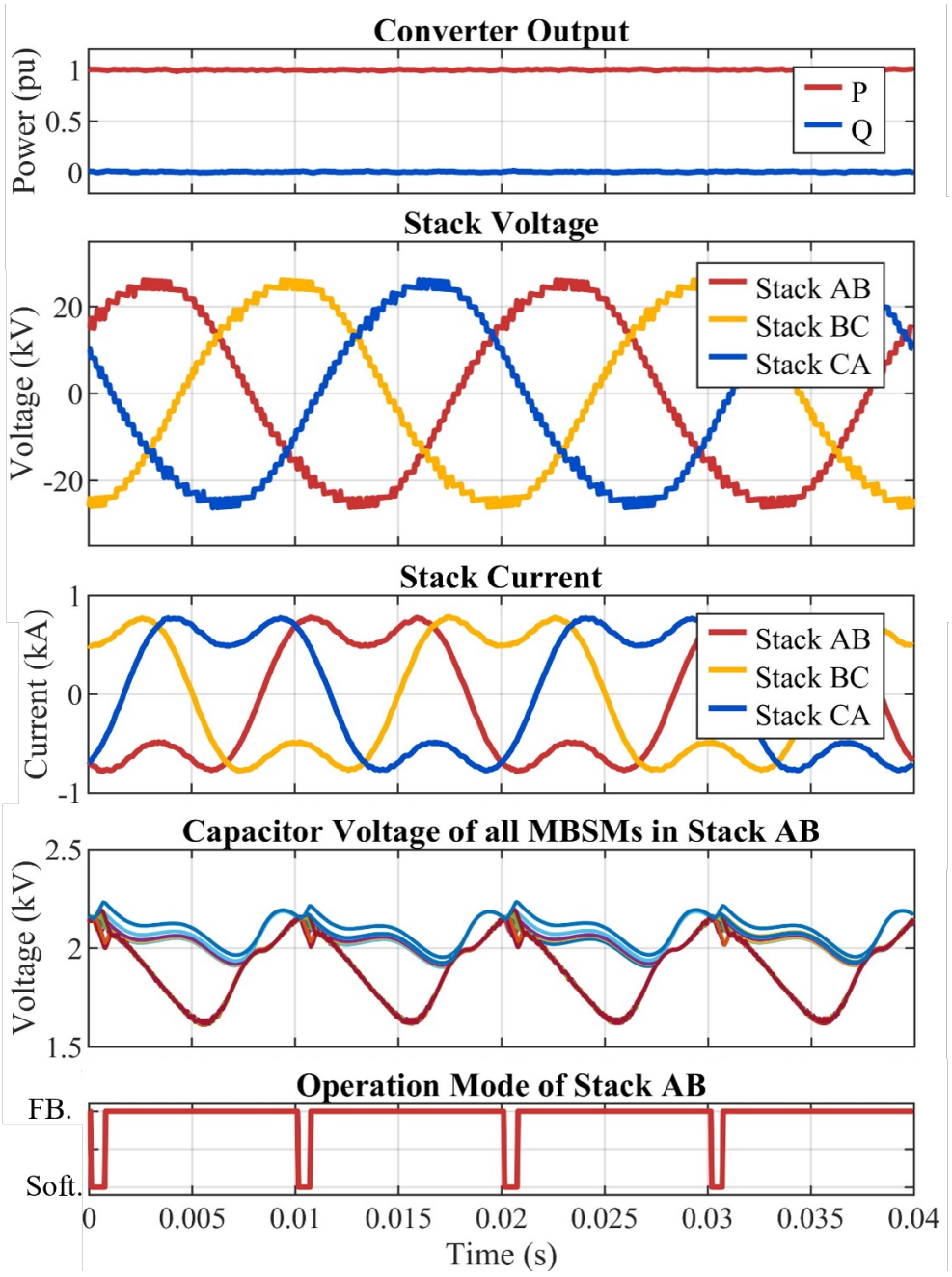


Figure 5.9: Converter performances when PF = 1

operating points are investigated: (1) PF = 0 as in Fig. 5.7; (2) PF = 0.5 as in Fig. 5.8; (3) PF = 1 as in Fig. 5.9. Results show the power outputs are well tracked, and the AC currents have low total harmonic distortion (THD) in different set-points. Capacitor voltages stay balanced and the upper bound of the deviation stays in the safe margin (20% of the rates SM voltage). Voltages of SMs with ES deviated from voltages of SMs without ES as the effect of ES current is different. I_{3rd} with the optimal phase angle derived by Eq. (5.13) and an amplitude of 300A is injected to maintain the voltage balancing when PF = 1, so third harmonics current exists in the stack current in Fig. 5.9. The ratio of soft-paralleling based mode decreases as the increase of power factors. The PRES MBSM STATCOM is verified to be capable to output 1 p.u. active power with the proposed low level controller applied.

Optimal Phase Angel of Additional Circulating Current

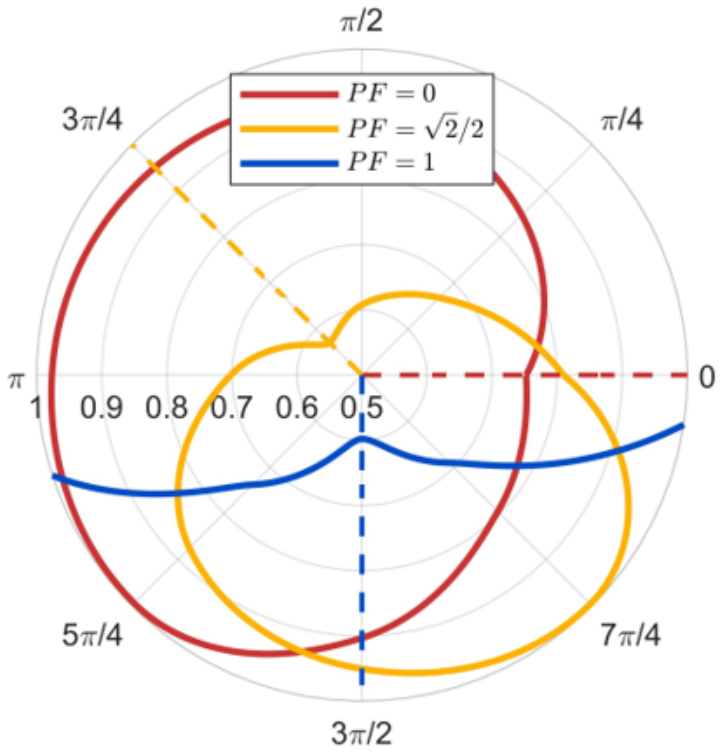


Figure 5.10: Normalized maximum SM voltage deviation versus phase angle of circulating current at three different set-points. Dashed lines are optimal value from Eq. (5.13).

Fig. 5.10 illustrates the effect of circulating current phase angles to the nor-

Table 5.4: Different STATCOM Configurations to compare active power capability and losses

Label	SM Type	Low level Control Scheme
Conf. 1	MBSM	The controller as is shown in Fig.5.3
Conf. 2	FBSM	Conventional SM sorting controller [163]
Conf. 3	FBSM	Voltage balancing Algorithm (VBA) proposed in [165]

malized maximum ΔV_{SM} within a stack at three different operation points with the same circulating current amplitude. The presented data is obtained through dividing the measured ΔV_{SM} by the maximum deviation versus phase angle in each operation point (195V for PF = 0, 815V for PF = $\sqrt{2}/2$, and 900V for PF = 1). When PF = 0 the minimum deviation is obtained when $\phi_{I_{3rd}} = 0$. The optimum $\phi_{I_{3rd}}$ becomes $3/4\pi$ when the active power output is equal to reactive power (PF = $\sqrt{2}/2$), while it is $3/2\pi$ at PF = 1. The performances verify the analytical result from Eq. (5.13). It could also be concluded from Fig. 5.10 that the more active power released from the converter, the larger deviation is seen by the SM voltages. The system becomes unstable when the converter generating full active power if $\phi_{I_{3rd}} \notin [5/4\pi, 7/4\pi]$ as ΔV_{SM} is too large.

Active power capability and losses

The power capability and efficiency of the MBSM STATCOM are further investigated and compared with its single bus FBSM counterparts, as listed in Table 5.4. The PWM frequencies of Conf. 1 and Conf. 2 are both 1000 Hz, while the sorting frequency in the iteration based controller of Conf. 3 is set as 10kHz as a trade-off between tracking accuracy and power efficiency. In Fig. 5.11, the solid lines show the results with no I_{3rd}, whereas the dashed lines represent results under I_{3rd} with the optimal phase angle and an amplitude of 300A. Higher PF represents larger I_{ES} charges capacitors in ES-MBSM. Hence, capacitor voltages are more likely to deviate from each other. Overall, the maximum ΔV_{SM} increases in all STATCOMs as the PF increasing. Conf. 1 has the best performances in all set-points whether the additional circulating current is injected or not. Conf. 2 has

lower ΔV_{SM} than Conf. 3 when PF ≤ 0.4, however will become unstable if PF $>$ 0.5. The active power capability of Conf. 1 and Conf. 3 are both up to 0.8 p.u. if there's no I_{3rd}. While comparing the solid and dashed lines, it can be concluded that not only will the maximum ΔV_{SM} be reduced but also the active power capability can be further pushed to 1 p.u. with I_{3rd} applied. Moreover, the average RMS currents of all semiconductors in a stack in the Conf. 1 is approximately halved in all set-points, as in Fig. 5.11 (b).

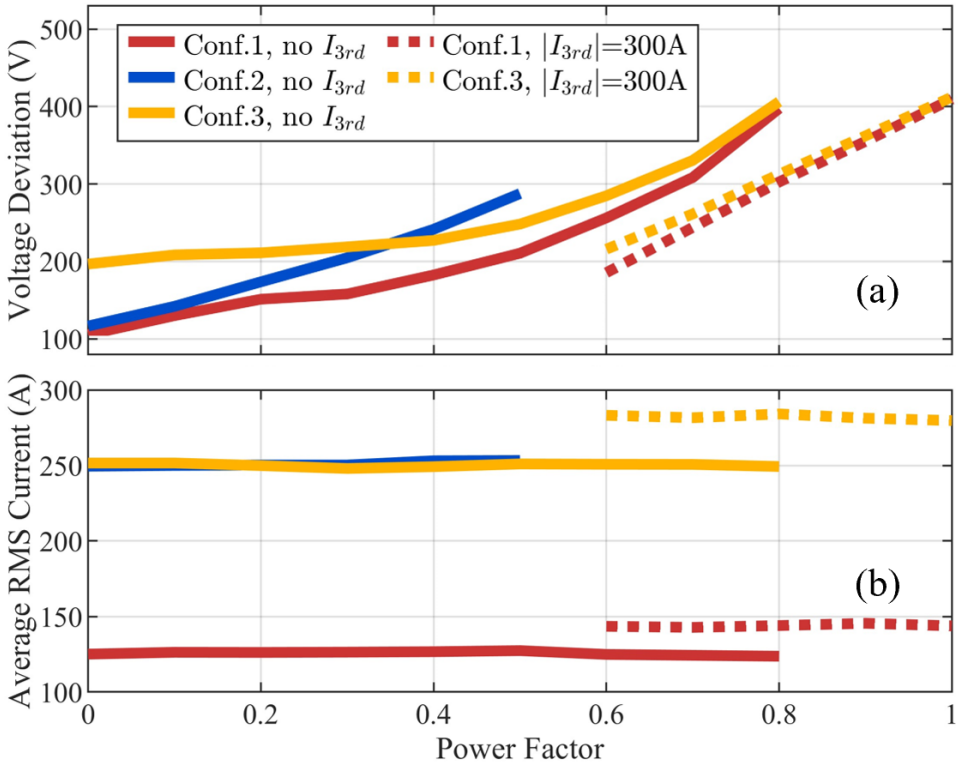


Figure 5.11: (a) Maximum ΔV_{SM}, and (b) Average RMS currents of all semiconductors in a stack versus power factor.

The losses analysis are conducted based on the IGBT module FZ1200R33HE3 produced by Infineon from which the losses curves have been extracted to compute the energy lost through conduction and switching at every simulation time step ($5\mu s$). The power losses of three different STATCOMs are summarized in Fig. 5.12 and Fig. 5.13. When the active power output is greater than a certain value, the SM voltages will be imbalanced and the whole converter cannot normally operate any more. Losses for an unstable STATCOM are not applicable and are presented as grey columns. Fig. 5.12 presents losses of all three configurations when no I_{3rd}

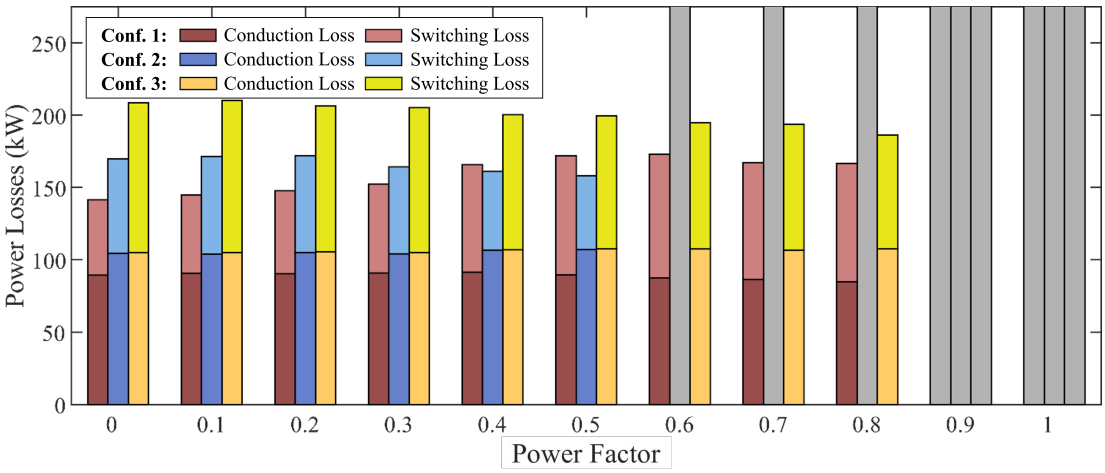


Figure 5.12: Semiconductor losses of different STATCOMs versus power factor without circulating current.

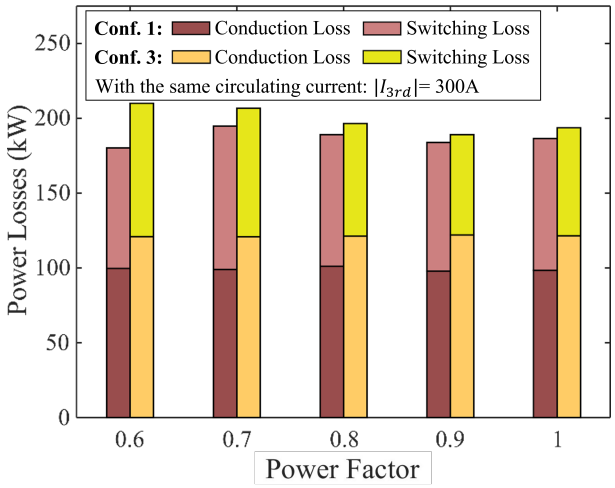


Figure 5.13: Semiconductor losses of different STATCOMs versus power factor with circulating current.

is applied. Conf. 1 has the lowest conduction losses in all set-points. With the increase of PF, the switching losses are also increasing as Conf. 1 operates less frequently in the soft-paralleling based mode. Notice that even though Conf. 2 has lower total losses when PF $\in [0.4, 0.5]$, it has much larger SM voltage deviation and distortions compared with Conf. 1. Additional I_{3rd} is inserted to output 1 p.u. active power as introduced before. The amplitude of I_{3rd} should also ensure that the peak stack current does not exceed 1 p.u., as suggested in [165, 167]. With the system parameters listed in Table II, the maximum amplitude of total stack current is 962A, and the maximum amplitude of I_{3rd} can be injected is 394A. Different circulating current amplitudes are investigated in the simulation

model, and the results show 300A is the minimum circulating current amplitude that ensure the studied STATCOM (Conf. 1, 60% ES-MBSMs) can output 1p.u. active power while the maximum SM voltage deviation is still within the normal range (20% of the nominal SM voltage). Fig. 5.13 presents the power losses of Conf. 1 and Conf. 3 when the same I_{3rd} with the optimal phase angle and an amplitude of 300A applied. Even when the maximum circulating current amplitude (394A) is applied in Conf. 2, the maximum power factor is 0.5, the same as when no circulating current is injected, as in Fig. 5.12. The active power output capability of Conf. 2 does not perform as well as Conf. 1 and Conf. 3. So, the results of Conf. 2 is excluded in Fig. 5.13. Conf. 1 almost fully operates in conventional FBSM based mode, as illustrated in the last figure of Fig. 5.9, and its losses are very close to that of the Conf. 3. The PRS MBSM STATCOM is a potential solution for fast frequency response in the first few seconds of a major grid disturbance. As part of the ancillary service, fully active power operation mode takes up a comparatively small portion of a STATCOM's lifetime compared to its major job, reactive power support. Consequently, the proposed MBSM STATCOM and the corresponding control system is able to effectively improve the power efficiency, especially in long term operation.

5.3 STATCOM with PRES Configured in Sub-stack

5.3.1 PRES Substack

This section investigates another PRES MBSM STATCOM structure where PRES MBSMs are configured in a sub-stack. Fig. 5.14 shows the detail of how different type of MBSMs are placed. ES-MBSMs and normal MBSMs are placed into two groups, forming an ES sub-stack and a normal sub-stack. The two sub-stacks can output voltage in opposite polarities so that SM voltage balancing is promoted. The MBSM STATCOM is different from the FBSM STATCOM in structure only inside the stacks. So the same higher level control method can be applied to both

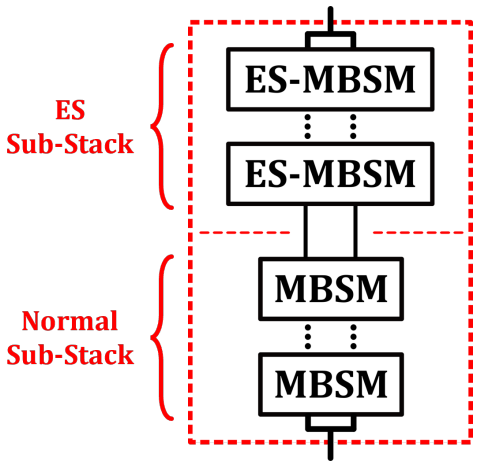


Figure 5.14: Energy storage configured in sub-stacks

topology while their low level controller should be designed separately.

5.3.2 Low level Control Algorithm

Sub-stack Voltage References

The first step of the soft-paralleling based controller is calculating the voltage references of the whole stack or the sub-stacks. Voltage references for two sub-stacks will be generated when the required voltage output of the whole stack is not exceed the voltage capability of sub-stacks, as presented in **Algorithm 1** (See Appendix). As ES currents are all charged to SM capacitors in the ES sub-stack, their voltages are more likely to be higher than the rated value. Therefore, the ES sub-stack will be discharged by stack current while the normal sub-stack will be charged to reduce the average voltage differences.

Mixed Modulation Framework

The second step of the soft-paralleling based controller is illustrated in **Algorithm 2** (See Appendix). Overall, the principle is to generate gate signals with the voltage references and the carriers. If $Flag = 1$, the stack will be controlled as a whole part to track the voltage reference. If $Flag = 0$, the reference voltages of two sub-stacks will be applied to allow the sub-stacks generate different voltage outputs, as long as the sum voltage is equal to the total voltage reference.

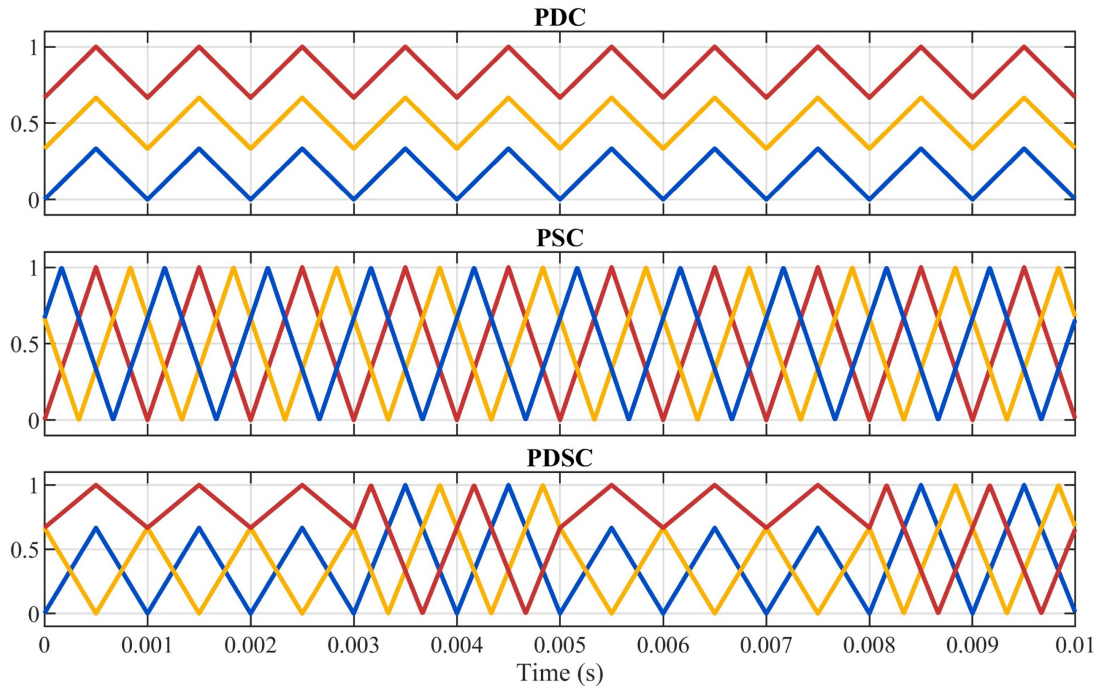


Figure 5.15: Modulation frameworks: (a) Phase Disposition Carrier (PDC), (b) Phase Shift Carrier (PSC), (c) the proposed Phase Disposition and Shift Carrier (PDSC).

Table 5.5: Simulation Model Parameters

Parameters	Value	Parameters	Value
STATCOM nominal power	30 MVA	AC side line voltage (RMS)	18 kV
Nominal frequency	50 Hz	Simulation sampling time	5 μs
Branch inductance	0.1 pu	Phase inductance	0.1 pu
Nominal cell voltage	2000 V	MBSM capacitance	2.5 mF
MBSMs per stack	15	ES-MBSMs per stack	9

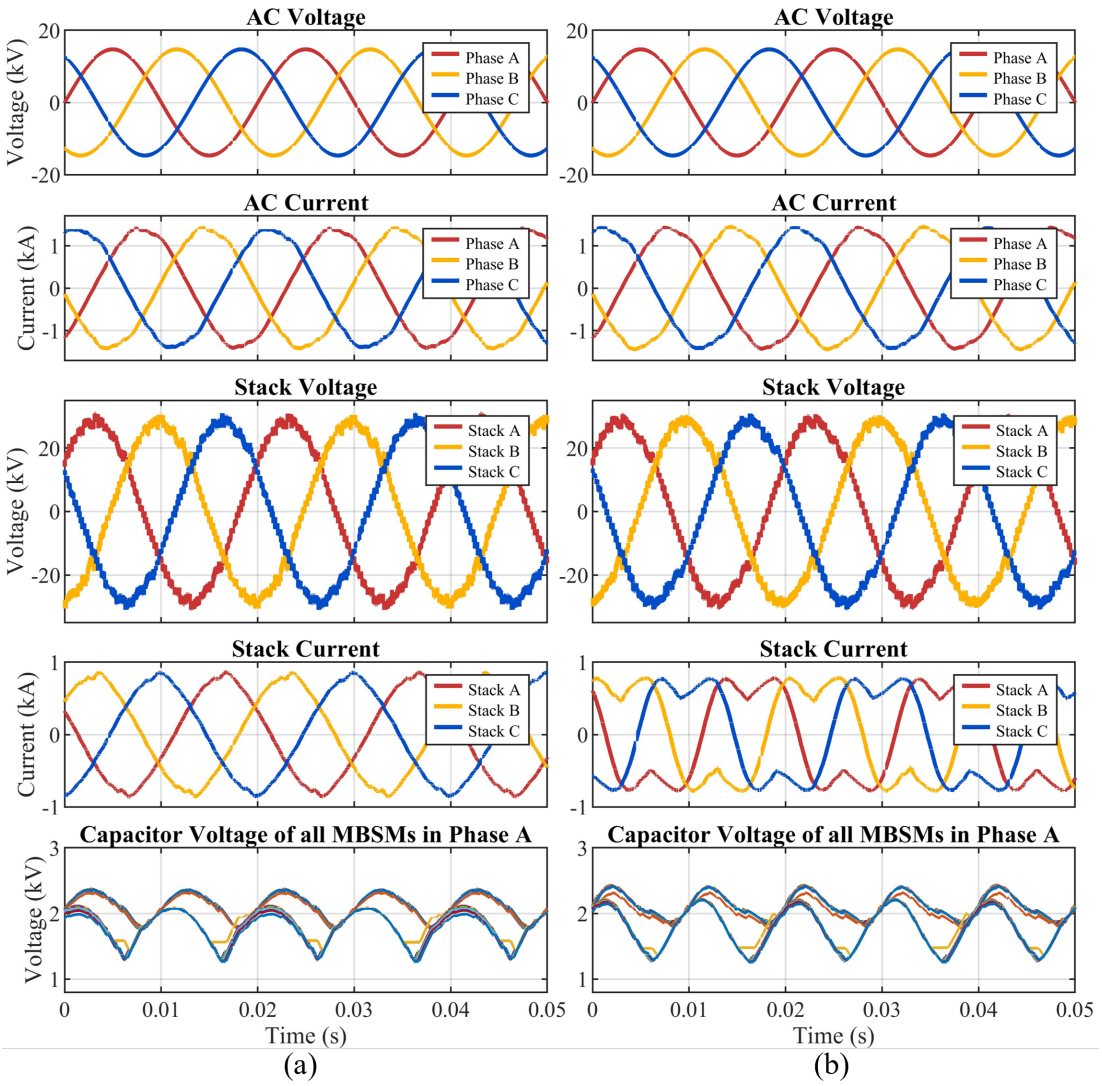


Figure 5.16: Converter outputs when operating at: (a) $P_{ref} = 0.6$, $Q_{ref} = 0.8$ without circulating current, (b) $P_{ref} = 0.6$, $Q_{ref} = 0.8$ with constant amplitude (300A) third harmonic circulating current.

The computational complexity of the soft-paralleling based controller is greatly reduced. Besides, the average semiconductor switching frequency is also limited by the carrier frequency. The phase disposition and shift carrier (PDSC) modulation framework is proposed here to enhance the voltage balancing of two sub-stacks while the carriers are assigned to the whole stack. PDSC is a mixed framework of phase disposition carrier modulation (PDC) [168] and phase shift carrier modulation (PSC) [169]. The carrier with the largest average value is assigned to the interconnection between two sub-stacks to make it operate longer time at soft-paralleling mode, as illustrated by the red line in Fig. 5.15 (c).

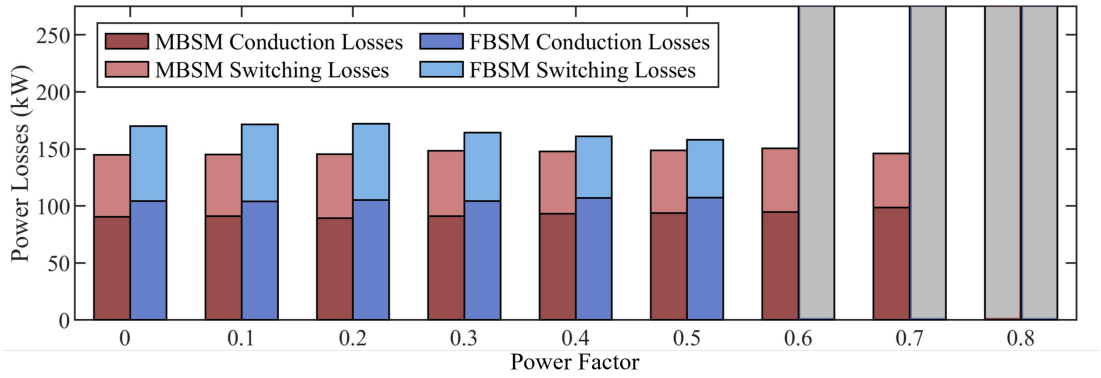


Figure 5.17: Conduction losses and switching losses versus varying power factors with 1 p.u. apparent power. Grey columns represent data when the converter is not stable.

5.3.3 Simulation Results and Analysis

The performances of the proposed converter are verified by a MBSM STATCOM model built in MATLAB/ Simulink and the parameters are listed in Table 5.5. The controller step is set as 5 μs and the PDSC frequency is 500 Hz. The losses curves of the IGBT module FZ1200R33HE3 produced by Infineon are applied for losses analysis.

Fig. 5.16 illustrates the converter outputs at different set-points. When realising 100% reactive power, as is shown in Fig. 4 (a), the AC current and stack current are both of high quality with low THD at 0.1%. In addition, the maximum capacitor voltages deviation is approximately 9.1%. At the set-point of $P_{ref} = 0.6$ and $Q_{ref} = 0.8$ (Fig. 4 (b)), where the apparent power is equal to the former set-point, active power generated by ES-MBSMs results in voltage unbalance of different sub-stacks. Due to the effect of ES current in ES-MBSMs, voltages of SMs in different types are not balanced. The maximum SM voltage deviation increases to approximately 22.8% and consequently the output current has larger distortion. Fig. 4(c) presents the results when $P_{ref} = 0.6$ and $Q_{ref} = 0.8$ with constant amplitude (300A) third harmonic circulating current applied. The maximum voltage deviation is reduced to 19.4 %, verifying that additional circulating current is able to promote the SM voltage balancing.

The performances of the proposed MBSM STATCOM together with its low

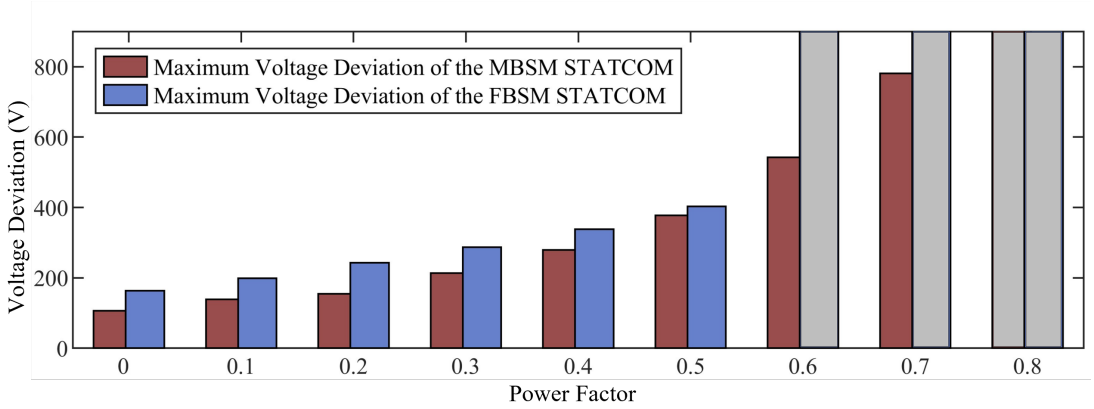


Figure 5.18: Maximum SM voltage deviation versus varying power factors with 1 p.u. apparent power. Grey columns represent data when the converter is not stable.

level controller are compared with a conventional FBSM STATCOM controlled by classic SM sorting low level controller [168]. The system parameters are the same as those listed in Table I. The power losses and maximum SM voltage deviation versus varying active powers with constant apparent power are illustrated in Fig. 5.17 and Fig. 5.18. The grey columns represent data when the converter is not stable. The MBSM STATCOM is able to release 0.7 pu active power while the conventional FBSM STATCOM becomes unstable when $Q_{ref} > 0.5$. The MBSM STATCOM performs better on conduction losses, switching losses and the maximum voltage deviation than its FBSM counterpart.

5.4 Active Current Sharing of SiC Devices through Multi-H-Bridges

5.4.1 Paralleling of SiC Devices

High voltage SiC MOSFETs have been attracting increasing attention due to their promising performances in low on-state resistance, high breakdown voltage, fast switching speed, and high power efficiencies over Si IGBTs [170], which are the basis of SMs in most of the current MMC projects. Specifically, in the design of the MMC, adopting SiC MOSFET as the substitution of Si IGBT could increase the rating voltage of a single SM. In addition, thanks to their higher switching

frequency and much lower switching loss, SiC MOSFETs make it possible to build an equivalent-scale MMC with fewer SMs, while maintaining high efficiency and low THDs. SiC MOSFETs are usually connected in parallel for high power applications due to the low current rating of discrete devices. Fig. 5.19 illustrates a FB SM constructed by four integrated power modules consisting of paralleled SiC MOSFETs.

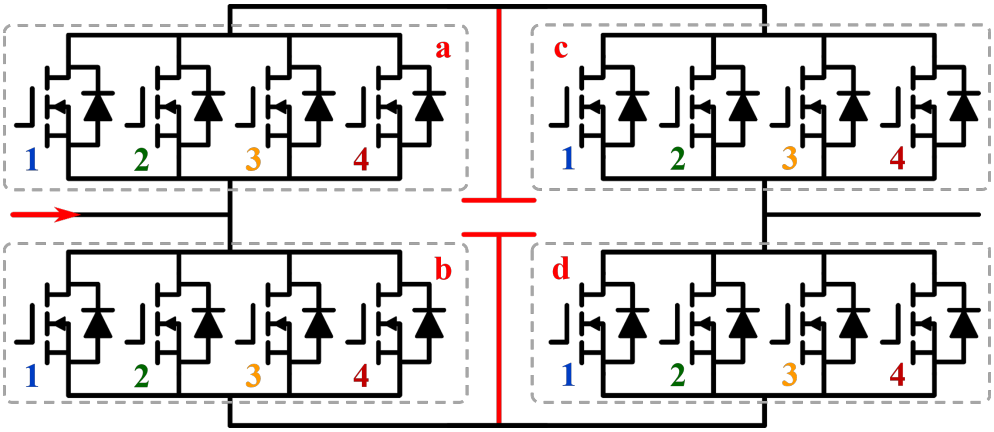


Figure 5.19: Structure of SiC MOSFET based FBSM with paralleled devices.

In spite of the above mentioned superior performances, paralleled SiC MOSFETs need to face current unbalance issues resulting from device parameter mismatches, which may cause unequal power losses and higher current overshoot. Much research has been conducted to analyse and suppress the effects of unbalanced current. An active current balancing scheme is proposed in [171] in which the unbalanced current is sensed and eliminated by actively controlling the gate drive signal to each device. In [172], the influence of circuit mismatch is investigated and experimentally evaluated, and a power module layout with an auxiliary source connection is developed to reduce the coupling effect among the paralleled dies. Ref. [173] presents a paralleled half-bridge unit characterised by a distributed arrangement of dc capacitors to improve the transient current sharing performance. Moreover, an approach with the incorporation of a differential mode choke is proposed in [174] to suppress the imbalance current among parallel SiC MOSFETs.

Considering the large number of SMs configured in a MMC, higher costs and more sophisticated control algorithms are expected if the current balancing meth-

ods require auxiliary capacitors, chokes, inductors, or on-time sensors for each discrete MOSFET. The multi-busbar SM (MBSM) [175] and the corresponding soft-paralleling mechanism are proposed initially for capacitor voltage balancing. Doubled current paths are constructed and consequently the SM current rating is increased thanks the intrinsic characteristic of the MBSM structure. The semiconductors in different busbars cooperate to connect the adjacent capacitors either in series or in parallel. The extra degree of freedom in multiple current paths inspires the idea of extending the MBSM to a new structure with more than two busbars, allowing actively parallel of not only SM capacitors but also SiC MOSFETs for better current sharing and power efficiency.

The Multi-H-bridges Submodule (MHSM) proposed in this section parallelizes multiple H-bridges. The goal of MHSM is to deal with the unequal steady-state current caused by on-state resistance (R_{on}) mismatches in discrete SiC MOSFETs. The contribution of this section can be summarised as follows:

(1) The MHSM structure, basic elements, and basic states are introduced in detail, to help in explaining the low-level control algorithm.

(2) Active current sharing is achieved by sorting and feedback-ing the average H-bridge current since H-bridges in a MHSM is decoupled from each other.

(3) When instantaneous current is low, fewer H-bridges are actively switched into conduction paths rather than all of them for improved power efficiency.

(4) Four modular multilevel STATCOM models with different SM configurations are built for simulation. Apart from verifying the normal operation of the proposed topology and control algorithm, results also show MHSM allows the same converter rating to be achieved with fewer submodules; MHSM STATCOM has the best power efficiency among all investigated configurations; and the current sharing performance versus R_{on} mismatch is assuring.

5.4.2 MHSM Configuration

The Paralleled H-bridges

The structure of a MHSM consists of 4 paralleled H-bridges and how MHSMs are connected in a stack is demonstrated in Fig. 5.20. Similar to the series and parallel SM and the MBSM, the states are defined for stack terminals. The stack terminals shown in the dashed blocks in Fig. 5.20 apply the same structure and operation principles as those introduced in [74] and [176]. This paper focuses on the interconnection and defin-es it as MHSM, as presented in the solid block in Fig. 5.20. All paralleled H-bridges are connected to two adjacent capacitors. The MHSM requires the cooperation of all H-bridges to output the desired SM state: Positive, Zero Voltage, or Negative.

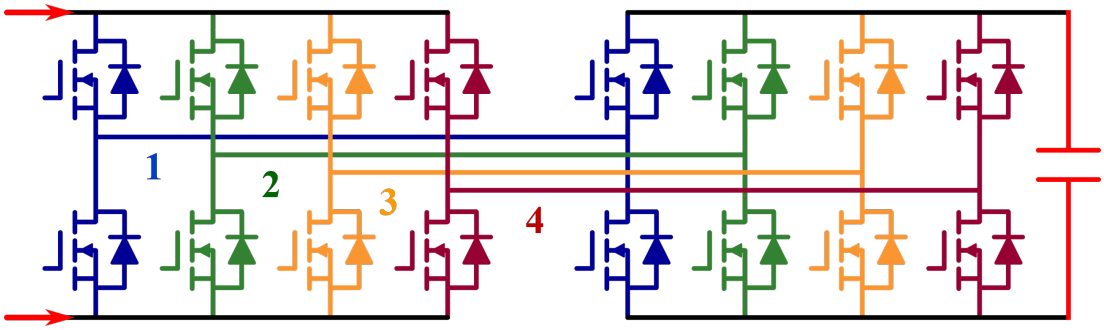
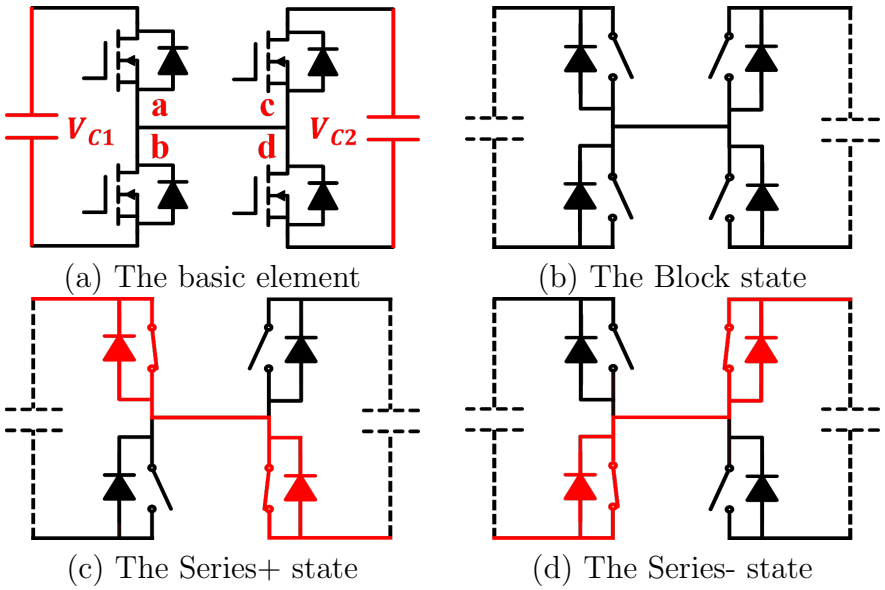


Figure 5.20: The structure of a MHSM constructed by 4 paralleled H-bridges.

Notice that different H-bridges in the MHSM in Fig. 5.20 are marked with different colours and labelled with Arabic numerals (1, 2, 3, 4). In the basic element of a MHSM, the H-bridge, shown in Fig. 5.21 (a), SiC MOSFETs in different positions are labelled by lowercase letters (a, b, c, d). Similar label rules are also applied in Fig. 5.19(a) to define the positions of semiconductors in the FBSM with paralleled SiC MOSFET devices.

Fig. 5.21 (b), Fig. 5.21 (c), and Fig. 5.21 (d) present the block state, the series+ state, and the series- state of the H-bridge. The SM state will be Positive when there is at least one H-bridge in the series+ state while the rest of the H-bridges are in the block state. Similarly, if there is at least one H-bridge in the series- state and the rest of the H-bridges are in the block state, the SM state becomes Negative.



(a) The basic element (b) The Block state

(c) The Series+ state (d) The Series- state

Figure 5.21: The proposed MHSM states.

Soft-parallel States

The soft-parallel states of the H-bridge are co-determined by the direction of stack current and the voltages of the two capacitors connected to the H-bridge (V_{C1} and V_{C2}). Power diodes play an important role in conducting current. All soft-parallel states are listed in Fig. 5.22. Stack current flowing from left to right is defined as a positive direction, while current flowing from right to left is defined as a negative direction.

The soft-parallel states when the stack current is positive are presented in Fig. 5.22 (a1) and Fig. 5.22 (a2). For simplicity, SP-5.22-a1 and SP-5.22-a2 are applied to represent the corresponding soft-parallel states in the following content. If the desired SM state is Zero Voltage, there should be at least one H-bridge in the SP-5.22-a1 state, and at least one H-bridge in the SP-5.22-a2 state, in order to parallel the adjacent capacitors for voltage balancing. The rest of the H-bridges in the MHSM are in the block state. Fig. 5.22 (a3) and Fig. 5.22 (a4) present the equivalent conduction paths of the whole MHSM when V_{C1}¿V_{C2}. Because of the voltage difference, only the H-bridge(s) in the SP-3-a1 state is conducting current while the H-bridge(s) in the SP-5.22-a2 state is not. In this instance, we define the SP-5.22-a1 state as active soft-parallel, and the SP-5.22-a2 state as inactive soft-parallel. In the equivalent conduction paths when V_{C1}¡V_{C2}, as

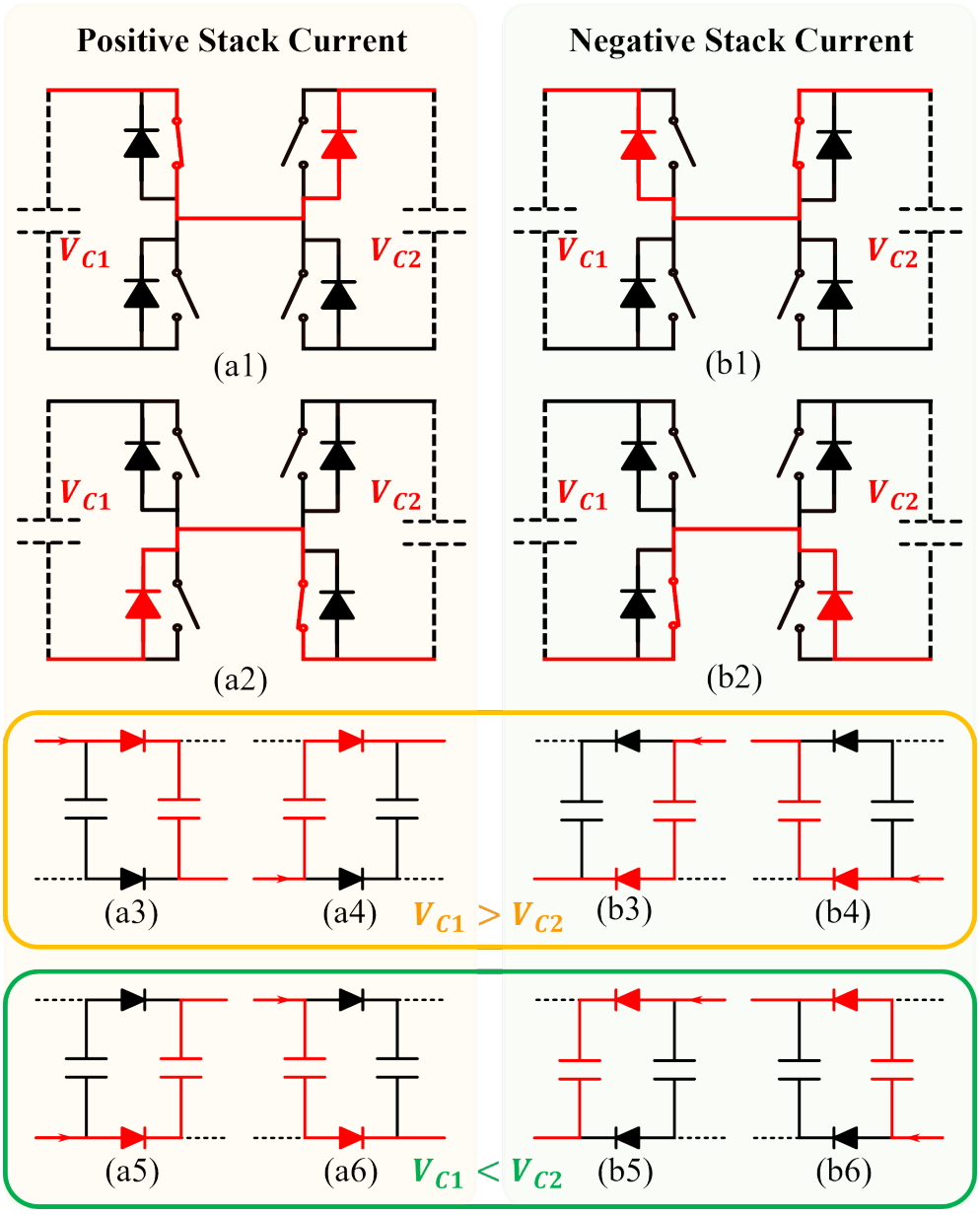


Figure 5.22: Soft-parallel states and equivalent conduction paths.

Table 5.6: SiC MOSFET States in a H-bridge of the MHSM.

MHSM H-bridge State	Semiconductor Position			
	a	b	c	d
Block	0	0	0	0
Series +	0	1	1	0
Series -	1	0	0	1
SP-5.22-a1	1	0	0	0
SP-5.22-a2	0	0	0	1
SP-5.22-b1	0	0	1	0
SP-5.22-b2	0	1	0	0

presented in Fig. 5.22 (a5) and Fig. 5.22 (a6), the SP-5.22-a1 state becomes inactive soft-parallel, and the SP-5.22-a2 state becomes active soft-parallel.

Soft-parallel states when the stack current is negative can be found in Fig. 5.22 (b1) and Fig. 5.22 (b2), and are marked as SP-5.22-b1 and SP-5.22-b2. Equivalent conduction paths in different capacitor voltage circumstances are listed in Fig. 5.22 (b3), Fig. 5.22 (b4), Fig. 5.22 (b5), and Fig. 5.22 (b6). The definitions of active and inactive soft-parallel are similar to those when the stack current is positive. The analysis will not be repeated here to save space.

5.4.3 Semiconductors Current Imbalance Issue

Based on the label system introduced in the previous section, the combination of lowercase letters (a, b, c, d) and Arabic numerals (1, 2, 3, 4) can be applied to specify a SiC MOSFET, either in the MHSM or in the FBSM. For example, c4 represents the SiC MOSFET on the top right of the 4th H-bridge in a MHSM. While in a FBSM, c4 represents the 4th paralleled SiC MOSFET in the top right power module.

Semiconductors current imbalance issue among different positions is caused by operation points. In the MHSM, semiconductor states are determined by the SM state, the stack current direction, and the relative magnitude of capacitor voltages, as listed in Table 5.6. The semiconductor states in FBSM are similar.

When the SM state is Positive, position a and position d conduct current; when the SM state is Negative, position b and position c become the new conduction path; When the SM state is Zero Voltage, either position a + c or position b + d is the conduction path. In the typical operation point of a STATCOM when generating reactive power, both the stack voltage and stack current are sine waves without offset, which means SMs have an equal time ratio in the Positive state and in the Negative state during a cycle, and meanwhile, the MHSM is able to operate evenly in four soft-parallel states to output zero voltage. With the control scheme proposed in [177] applied, the current imbalance among different semiconductor positions can be suppressed.

As for the current imbalance issue of MOSFETs among different paralleled H-bridges in the same position, the solution is based on decoupling the conduction of each H-bridge. The average semiconductor current in each H-bridge is fed into the controller. The H-bridge with the lowest average current will be allocated the highest priority to conduct current for paralleled SiC MOSFET current balancing.

5.4.4 Active Current Sharing Low Level Control Algorithm

The MHSM STATCOM studied in this paper applies distributed control framework, in which energy management, power control, current control, and low level control are decoupled and allocated to controllers in different layers. The higher level algorithm is the same as that applied in conventional STATCOM [165]. The active current sharing low level control algorithm takes the desired MHSM state, capacitor voltages, current rating of a discrete SiC MOSFET and the average current of all MOSFETs in each H-bridge as inputs and outputs gate signals for all SiC MOSFETs.

As detailed and presented in **Algorithm 3**, at first, the controller calculates the number of H-bridges to be actively switched in, denoted by N_A, based on the instantaneous stack current and the current rating of discrete SiC MOSFET:

Algorithm 3 Active Current Sharing Low Level Control.

Input:

$\boldsymbol{S}$: Desired state of the MHSM;
$\boldsymbol{V_{C1}}$: Voltage of the capacitor on the left;
$\boldsymbol{V_{C2}}$: Voltage of the capacitor on the right;
$\boldsymbol{I_{stack}}$: Stack current;
$\boldsymbol{I_{rated}}$: Rated current of the discrete SiC MOSFET applied;
$\boldsymbol{I_H}$: Average current array ($\boldsymbol{N_H}$ by 1) of all MOSFETs in each H-bridge.
($\boldsymbol{N_H}$ denotes the number of H-bridges in a MHSM)

Output:

$\boldsymbol{G}$: Gate signals array ($4\boldsymbol{N_H}$ by 1) of all SiC MOSFETs.

Start algorithm

Calculate the number of H-bridges to be actively switched in based on Eq. (1).
Sort $\boldsymbol{I_H}$ ascendingly, assign 0 to the minimum element in the sorted array $\boldsymbol{I_{Hsorted}}$.
Calculate H-bridge state array $\boldsymbol{S_H}$ based on Eq. (2).
if $(\boldsymbol{S == 1})$
  for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
    if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *Series+*;
    else: Assign corresponding state = *Block*;
else if $(\boldsymbol{S == 0})$
  if $(\boldsymbol{I_{stack} > 0})$
    if $((\boldsymbol{V_{C1} > V_{C2}}))$
      for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
        if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *SP-5.22-a1*;
        else if $(\boldsymbol{S_H(i) == 0})$: Assign corresponding state = *SP-5.22-a2*;
        else: Assign corresponding state = *Block*;
    else
      for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
        if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *SP-5.22-a2*;
        else if $(\boldsymbol{S_H(i) == 0})$: Assign corresponding state = *SP-5.22-a1*;
        else: Assign corresponding state = *Block*;
  else
    if $((\boldsymbol{V_{C1} > V_{C2}}))$
      for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
        if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *SP-5.22-b1*;
        else if $(\boldsymbol{S_H(i) == 0})$: Assign corresponding state = *SP-5.22-b2*;
        else: Assign corresponding state = *Block*;
    else
      for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
        if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *SP-5.22-b2*;
        else if $(\boldsymbol{S_H(i) == 0})$: Assign corresponding state = *SP-5.22-b1*;
        else: Assign corresponding state = *Block*;
else
  for $\boldsymbol{i = 1 \rightarrow N_H}$ **do**
    if $(\boldsymbol{S_H(i) > 0})$: Assign corresponding state = *Series-*;
    else: Assign corresponding state = *Block*;

End algorithm

Figure 5.23: Active Current Sharing Low Level Control Algorithm.

$$N_A = ceiling(\frac{|I_{stack}|}{I_{rated}}) \tag{5.16}$$

Not all MOSFETs are required to conduct current in a full cycle. Consequently, switching losses can be reduced by dynamically determining the minimum conduction paths, especially when the stack current is low. The average current of each H-bridge are sorted and H-bridge states are determined by N_A and the sorted array $I_{Hsorted}$ based on Eq. 5.17.

$$S_H = sgn(N_A - I_{Hsorted}) \tag{5.17}$$

For each element in the array S_H, "1" represents the corresponding H-bridge should be actively switched in; "0" represents the H-bridge should be inactively switched in; "-1" represents the H-bridge should be blocked. Then the specific state of each SiC MOSFET is obtained based on the capacitor voltages, desired MHSM state, and stack current direction, as illustrated by Step 1 to Step 34 in Fig. 5.23.

5.4.5 Simulation Results

Table 5.7: MHSM System Parameters

Parameters	Value	Parameters	Value
Nominal Power	30 MVA	Phase Inductance	0.1 pu
Line Voltage (RMS)	15 kV	Stack Inductance	0.1 pu
Nominal Frequency	50 Hz	Sampling Time	5 μs
Stack Energy	300kJ	Control Frequency	10 kHz

The proposed MHSM is investigated in typical modular multilevel STATCOM scenario, generating certain reactive power. The parameters of the system are summarised in Table 5.7. Four STATCOM models with stacks constructed by different SM configurations are built in MATLAB/Simulink to compare the performance of the proposed SiC MOSFET MHSM (Conf. 1) [178] with directly paralleled SiC MOSFET FBSM in the same voltage rating (Conf. 2), Si IGBT

Table 5.8: SM Configuration Parameters

Label	Type	Semiconductor	N_{SM}	V_{rated}	N_{rated}
Conf. 1	MHSM	SiC MOSFET (XHV-7 [178])	8	3300V	400A
Conf. 2	FBSM	SiC MOSFET (XHV-7)	8	3300V	400A
Conf. 3	FBSM	Si IGBT (FZ1600R33HE4)	8	3300V	1600A
Conf. 4	FBSM	Si IGBT (FZ1600R17HP4)	8	1700V	1600A

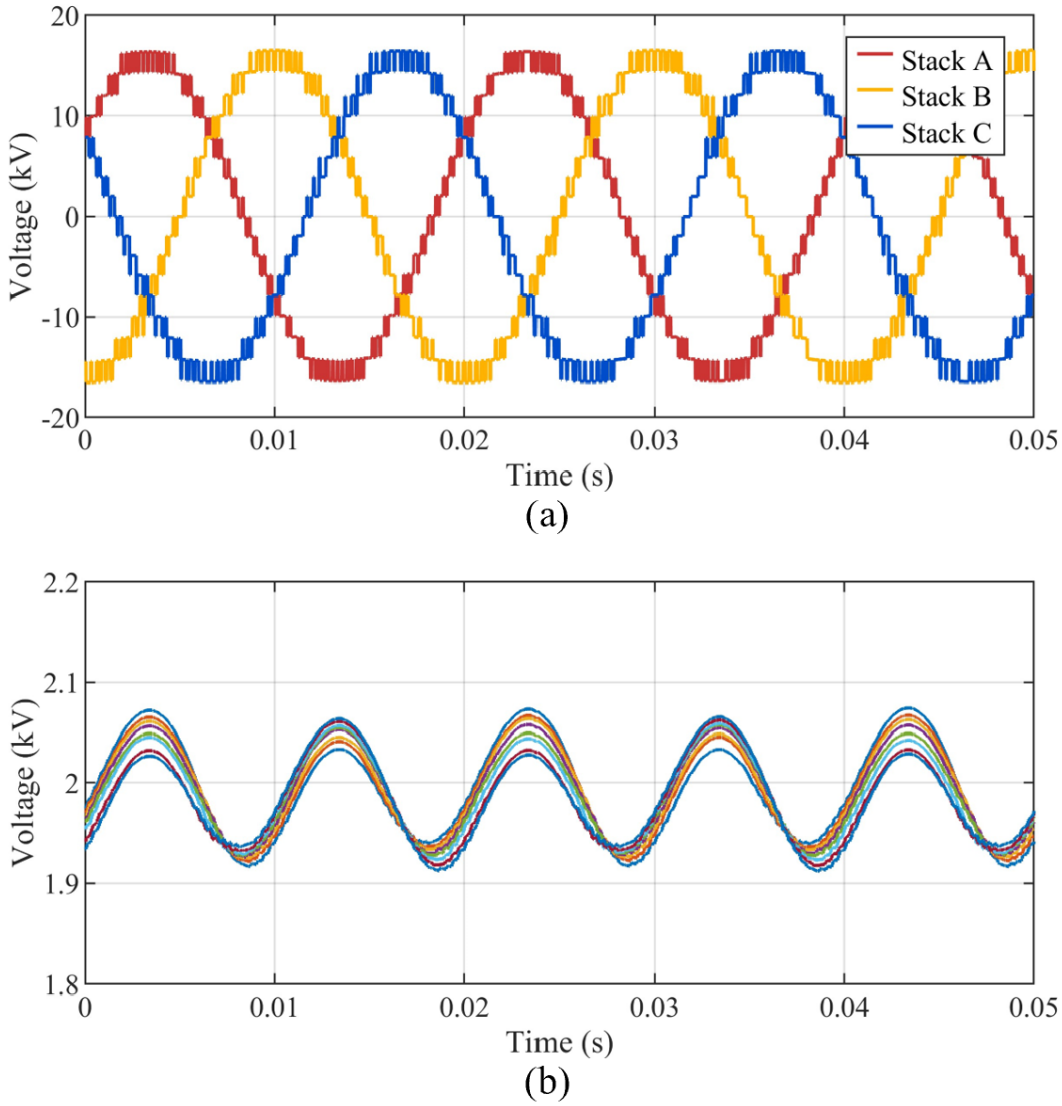


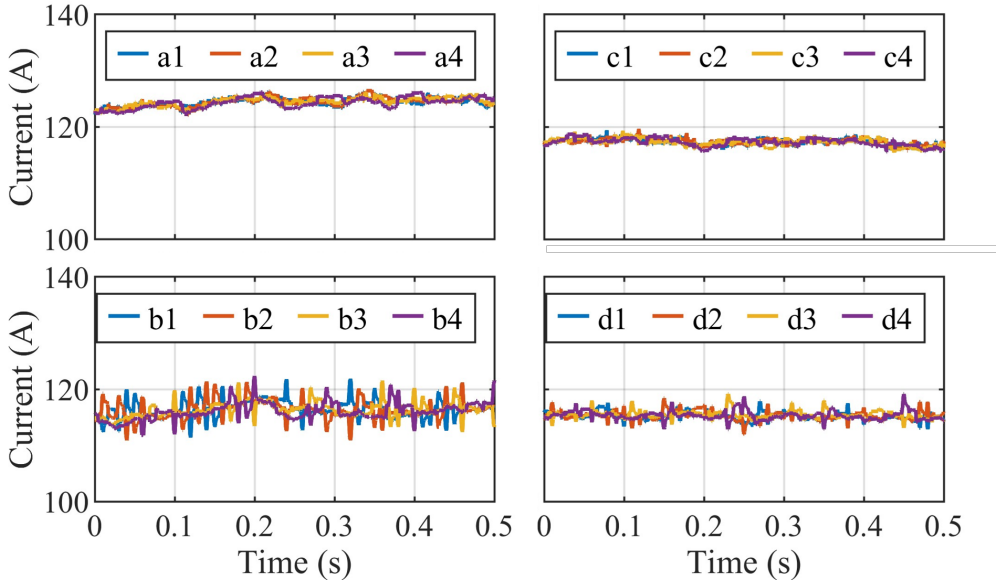
Figure 5.24: Performances of the MHSM STATCOM and the proposed controller: (a) Stack voltages in three stacks, (b) Capacitor voltages of all MHSMs in the Stack A;

FBSM in the same voltage rating (Conf. 3), and Si IGBT FBSM in half the voltage rating (Conf. 4). The parameters of four different SM configurations are summarised in Table 5.8. The current rating of the SiC MOSFET is 400A while the current rating of the Si IGBT is 1600A. Consequently, both the MHSM in Conf. 1 and the FBSM in Conf. 1 connect four SiC MOSFETs in parallel for fair comparison. The stacks in Conf. 1, Conf. 2 and Conf. 3 are constructed by eight SMs with a 3300V semiconductor rated voltage and a 2000V capacitor rated voltage. The stack in Conf. 4 has sixteen SMs. The semiconductor rated voltage and the capacitor rated voltage are 1700V and 1000V, respectively. The SM capacitance ensures different configurations have equal stack energy.

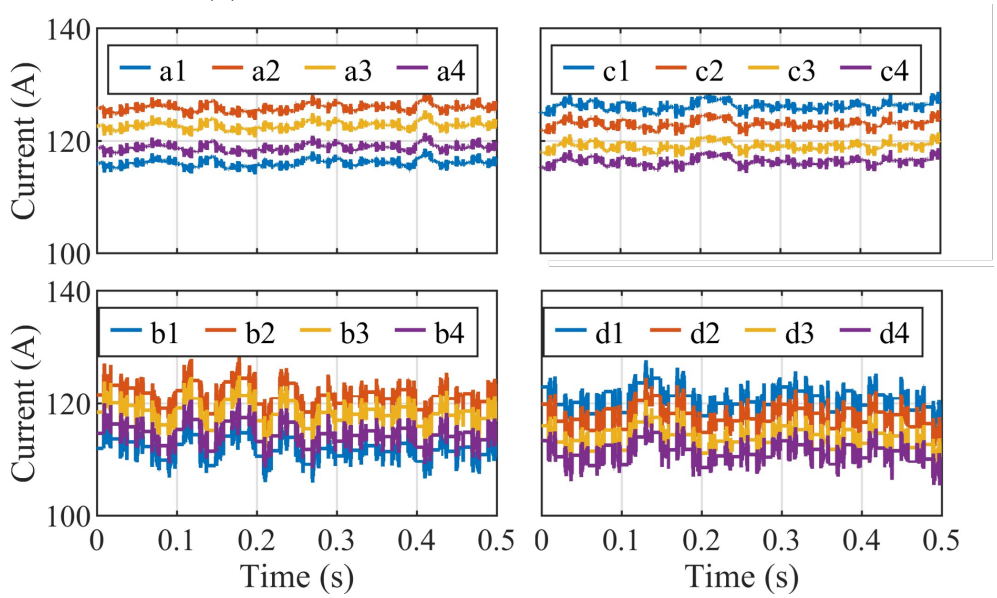
The stack voltage and SM voltage of the model in Conf. 1 are presented in Fig. 5.24 (a) and Fig. 5.24 (b). During normal operation, the STATCOM is set to push 1 p.u., 30 MVar, reactive power to the AC side. The stack generates staircase voltage tracking the reference obtained from the higher level current controller. Because of the periodically paralleling mechanism of adjacent capacitors, the maximum SM voltage difference is regulated to less than 6.3% of the nominal SM voltage.

The current sharing performances are then investigated under a 5% R_{on} mismatch, and the steady state currents of all SiC MOSFETs in a MHSM and a FBSM are shown in Fig. 5.25 (a) and Fig. 5.25 (b), respectively. In each controller step, the H-bridge with the lower average current is allocated higher priority to conduct current and compensate for the imbalances. Evenly distributed currents are found among different SiC MOSFETs in the MHSM, which also indicates better thermal performance than that of the FBSM.

The modulation framework applied by the MHSM in Conf. 1 is PSC modulation. The FBSMs in the other three configurations all apply NLM with PWM on the last voltage level (NL-PWM). The THDs of different SM configurations versus different PWM frequencies are presented in Fig. 5.26. THDs are dropping with the increase of PWM frequencies in all SM configurations. Conf. 1, Conf. 2, and Conf. 3 have similar THDs at the same PWM frequency, though different modulation frameworks are applied. Since Conf. 4 has twice the number of SMs



(a) Currents of SiC MOSFETs in a MHSM



(b) Currents of SiC MOSFETs in a FBSM

Figure 5.25: Current Sharing Performances of the MHSM STATCOM and the proposed controller.

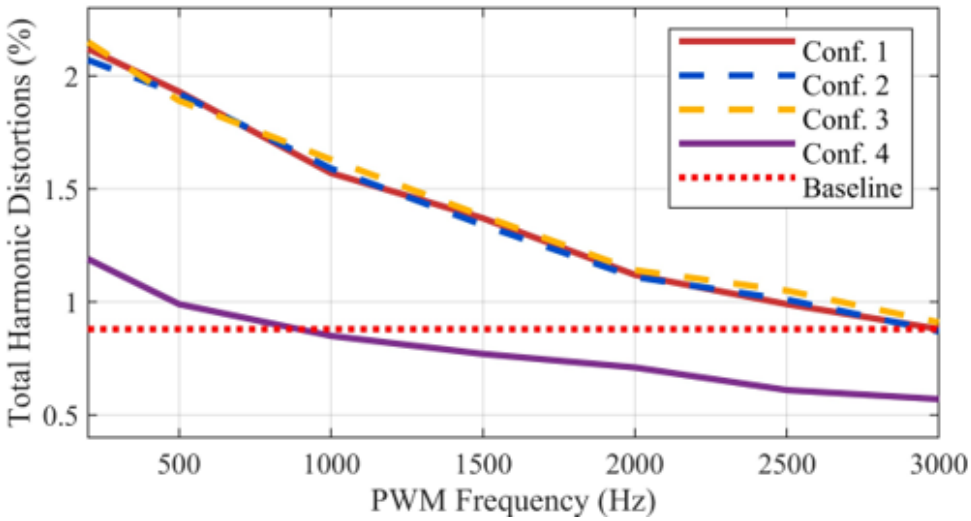


Figure 5.26: THDs of different STATCOM configurations versus PWM frequencies.

in each stack, the same THD can be achieved with a lower PWM frequency compared with the other configurations. The baseline (red dotted line) indicates that a stack with eight SMs modulated by a 3000 Hz PWM has a similar THD to a stack with sixteen SMs modulated by a 1000 Hz PWM. The conclusion is used to compare the power losses of different configurations.

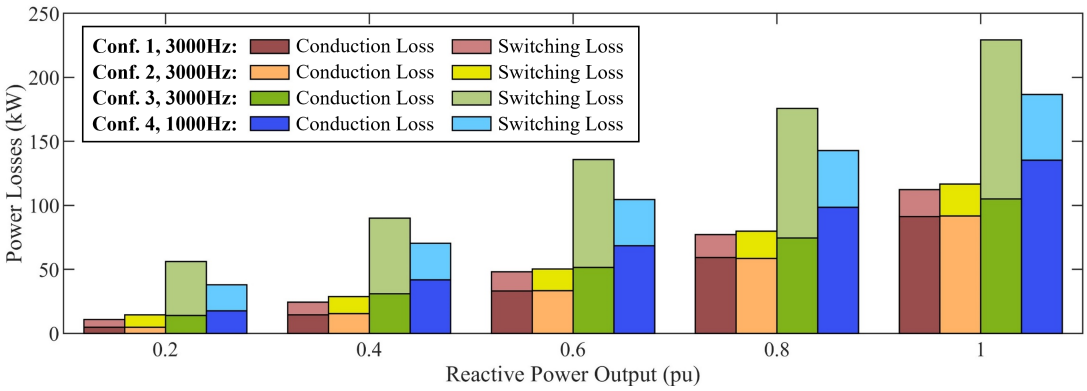


Figure 5.27: Conduction losses and switching losses of STATCOMs in four different SM configurations versus reactive power output.

Conduction losses and switching losses of STATCOMs in four different SM configurations versus reactive power output are illustrated in Fig. 5.27. The PWM of STATCOMs in Conf. 1, Conf. 2, and Conf. 3 are 3000 Hz, while the converter in Conf. 4 operates at 1000 Hz, as all STATCOMs have AC output in the same THD. Results show: 1) SMs constructed by SiC MOSFETs can reduce both

conduction loss and switching loss even modulated by a higher PWM frequency compared with Si IGBT based MOSFET. 2) Conf. 1 has approximately the same conduction loss compared with Conf. 2, but the MHSM (Conf. 1) is able to reduce the switching loss, especially at lower current operating points. The switching loss is reduced by about 14.8 % when generating full rate reactive power and by 38.4 % when generating 0.2 p.u. reactive power.

5.5 Summary

This chapter investigates MBSM applications in STATCOM where MBSMs operate in four quadrants. Section 5.1 provides the STATCOM modelling and the corresponding higher level control, and introduces how ES is configured in MBSMs.

Section 5.2 presents a delta-configured, modular multilevel, STATCOM based on MBSM topology where PRES are distributedly integrated in MBSMs to provide both active power and reactive power. The soft parallel of MBSM is more effective in reactive power mode than active power mode due to the location of ES, which see their current circulation limited to their own SM capacitor. The proposed controller for the MBSM STATCOM dynamically switches between two operation modes to reduce the converter losses over the extended range of active power, in line with the state-of-the-art papers. Simulation results confirm the earlier point, in that PRES-MBSM-STATCOM performs better at pure reactive power set-points and marginally better at high active power. This is explained by the fact that MBSM operates more frequently in soft-paralleling mode when the ES are released less power, i.e. reactive power set-points.

Section 5.3 proposes a new type of PRES STATCOM configured in ES-MBSM sub-stacks. The mixed control system and modulation framework are also presented. Compared with the conventional FB counterpart, the active power capability is increased from power factor = 0.5 to power factor = 0.7, while the power losses and the maximum SM voltage deviation are reduced by 14.9% and 35.2% respectively when operating at pure reactive power output. Moreover, the active

power capability can be further improved with larger circulating current applied.

Section 5.4 presents the MHSM constructed by multiple parallel-connected SiC MOSFET H-bridges to provide the freedom of degree in the current rating. Simulation results have verified that the current sharing performance against on-state resistance mismatch is improved, and the switching loss is reduced compared with conventional FBSM constructed directly paralleled SiC MOSFETs. The same converter rating can be achieved with less MHSMs compared with Si IGBT SMs.

Chapter 6

Design of Micro-MMC

The extensive applications make the MMC a key topology within the power electronics community, requiring further research and, crucially, education of the next generation of power electronics engineers. It remains impractical to build an MMC at industrial-scale (typically in the hundreds of megawatts) within a traditional experimental lab. The micro-MMC (μMMC, μ for its rating at one millionth of usual transmission-scale MMCs) aims to provide a solution to break the barrier from theory to practice. It should be noted that the demonstration of the μMMC in this chapter is based on the FBSM MMC rather than the MBSM MMC introduced in the previous chapters. Thanks to the distributed control framework, the μMMC shares the same higher level control algorithm as the MBSM MMC. Besides, the scalability characteristics of the μMMC allow an MBSM MMC to be constructed with specific inter-connections of the reserved ports.

6.1 Motivation

In industrial projects, the MMC usually has extremely large footprint. Building an industrial-scale MMC is high cost and time-consuming, make it unapplicable for research and education. Building reduced-scale MMCs based on specific research objectives becomes a widely accepted option, especially for university laboratories [179, 180, 181, 182]. Generally speaking, the specification for the reduced-scale MMC can be roughly divided into five types of studies according to

their intended purpose [183, 184], including: (A) Power system and multi-terminal network studies; (B) Power and control system studies; (C) Communications and control architecture studies; (D) Future converter topology and SM configuration studies and (E) Fault and protection studies [185]. In the case of the lab-scale MMC focusing on type (B) and type (D) studies in Imperial College London, three researchers spent two years' efforts in the designing and constructing stage of two full design iterations, not to mention the time and cost spent on carrying out the follow-up research and teaching tasks.

Even a reduced-scale MMC could contain dozens or even hundreds of SMs in total, which means the control system should handle the interaction of large amounts of sensors, communication units and control targets, i.e. power semiconductors [186]. Instead of centralized control, hierarchical control structure consisting of multi layers distributed controllers, is proved to be convincing in many projects developed by industry and academia. In a typical control structure, the upper level controller accepts output voltage and power reference orders to generate stack voltage references for the lower level controller. Lower level controller is in charge of SM balancing and output the gate signals of power semiconductors. Detailed summary of the distributed control system of MMC can be found in [187].

The popularity of integrated development boards and their corresponding open source community have profoundly simplified the barriers from analytical and simulation models to hardware realization. A large number of mature projects are open to researchers and engineers for reference to accelerate the development process. In addition, MATLAB/Simulink provides comprehensive hardware support packages for popular development boards, such as Arduino [188], Raspberry Pi [189], Texas Instruments LaunchPad [190], STMicroelectronics Nucleo Boards [191], NVIDIA Jetson Nanos [192], etc. It is practical to transform power electronics from simulations to experiments in hours with versatile integrated controllers and experiment tools.

This chapter presents a time-efficient, economical and integrated choice for MMC researchers, the μMMC. From the perspective of the power circuit, the

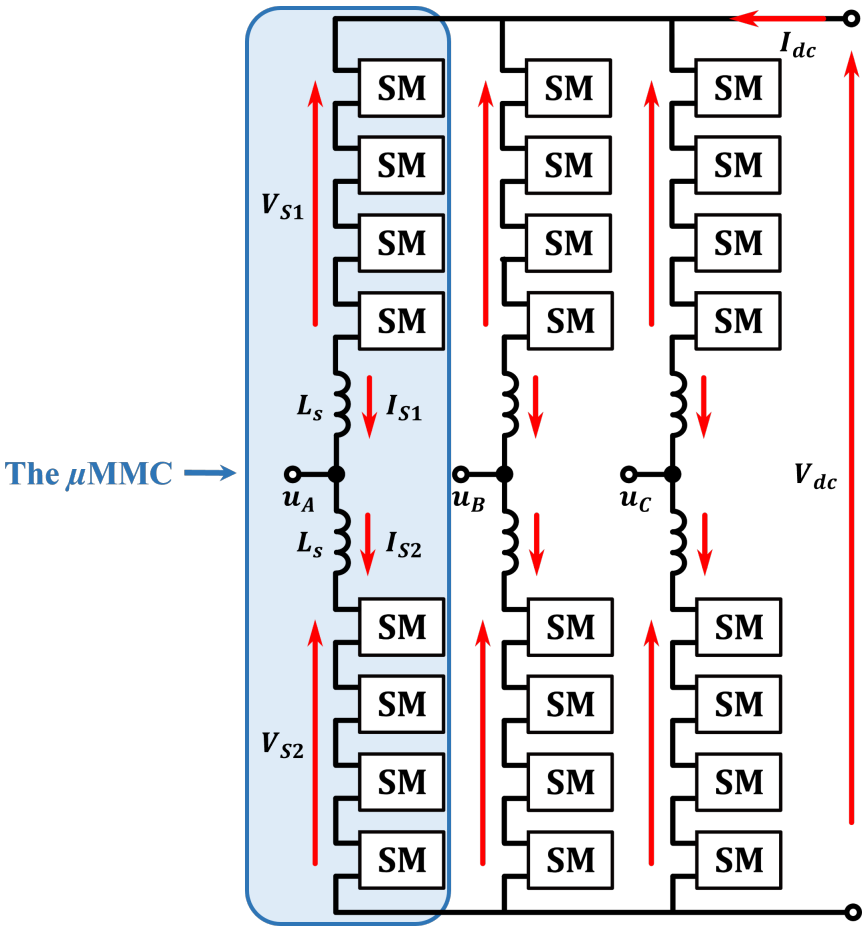


Figure 6.1: Three phase MMC with 4 SMs in each stack and the primary circuit of the micro-MMC

μMMC can be seen as a single phase of the classic three phase MMC, as shown in the shaded area in Fig. 6.1. Eight re-configurable FBSMs, an embedded μC, current sensors, and components for the primary circuit are integrated into a 10× 10 cm PCB. The DC bus operating voltage is designed to be lower than 30 volts, the same as the typical output of the traditional laboratory power supply. Users can access the open-sourced design files directly for PCB manufacturing and get it in weeks with cost around 50 pounds. The control architecture follows the distributed type. Both Serial Peripheral Interface (SPI) and Universal Serial Bus (USB) communication ports are reserved, making it is possible for μMMC to either operate independently, or act as lower layer system and controlled by most of the popular integrated development boards. Users can benefit from various of features of the μMMC, including but not limited to:

(1) Safe: The μMMC is capable to operate in low voltage/power scenario so

users are free to use it either in a lab or at home.

(2) Economical: The low-cost of the μMMC make it suitable for education and training.

(3) Open-source: All hardware design files and software project files are provided. Users can simply download, order, test and transform their ideas from simulation to practise in days.

(4) Scalability: Apart from operating as a single board power electronics system, the multi-layer control framework, together with the power ports and communication ports reserved in the μMMC allows more complicated system to be constructed and demonstrated.

The μMMC is essentially an ultra reduced-scale MMC. To reduce the total cost of the system, the accuracy of measurement elements are not as good as those used in industry. Besides, the bandwidth of communication is narrow, making it harder to design controller parameters.

6.2 Hardware Design

6.2.1 Overall Layout

The μMMC is essentially a 10 cm $\times$ 10 cm PCB, as presented in Fig. 6.2 and Fig. 6.3, which integrates a single phase MMC with the primary circuit, eight reconfigurable SMs, and related sensors and controllers. The overall layout of the μMMC is illustrated in Fig. 6.4, where the black solid lines represent the internal electrical connection within the PCB, while the red dashed lines demonstrate the user-defined connections. The primary circuit, located at the top of the PCB, includes two stack inductors for the sake of compensating high order harmonics. Stack currents are measured by two hall effect current sensors rather than current transformers because the former requires less space on the PCB. The output pins of the current sensors are connected to the stack controller. A Double Pole Double Throw (DPDT) relay is also included in the design, allowing two resisters to be switched into the primary circuit when demonstrating the start-up procedure. The resisters aim to limit the pre-charge current injected to SM capacitors.

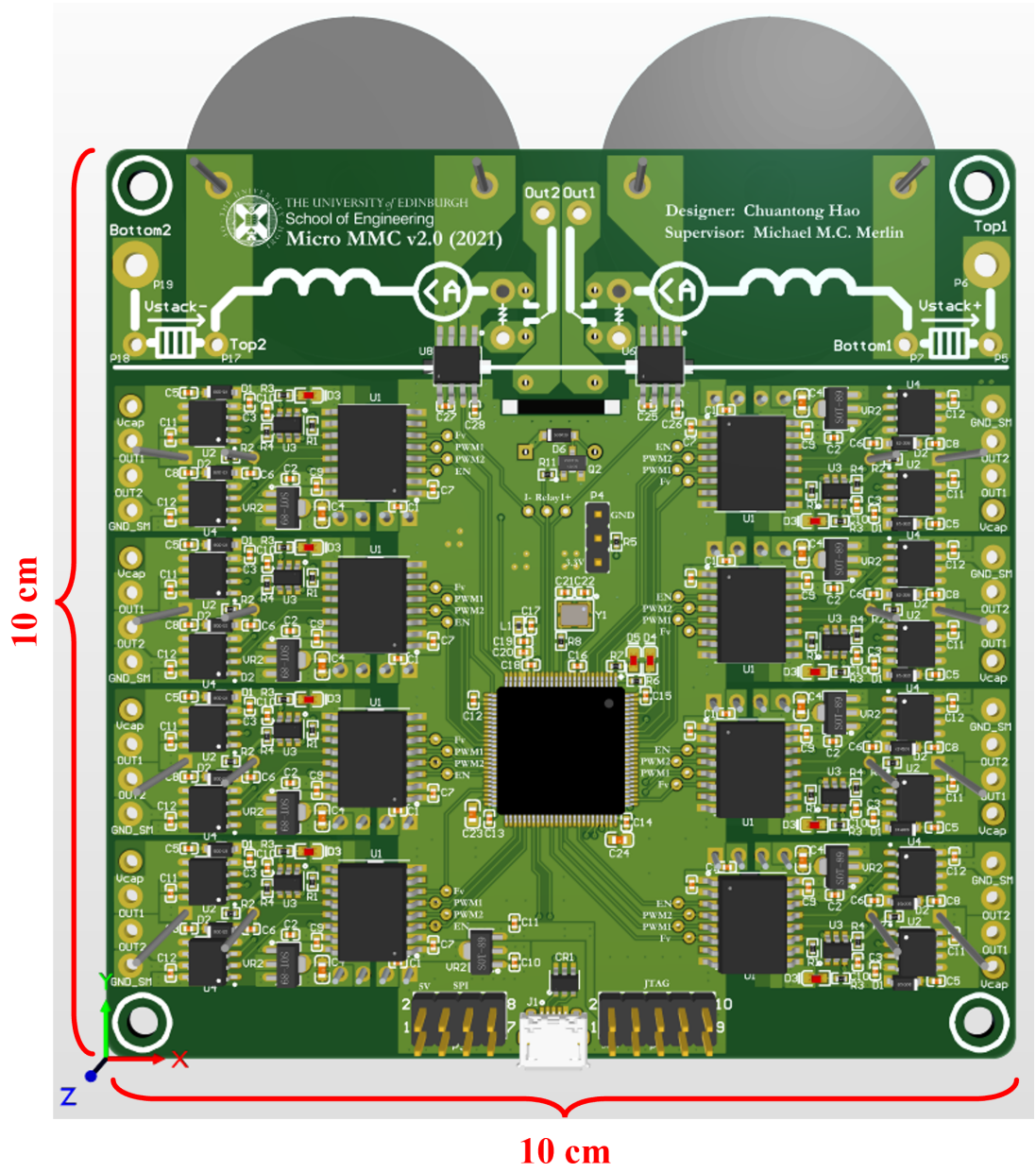


Figure 6.2: The top view of the μMMC

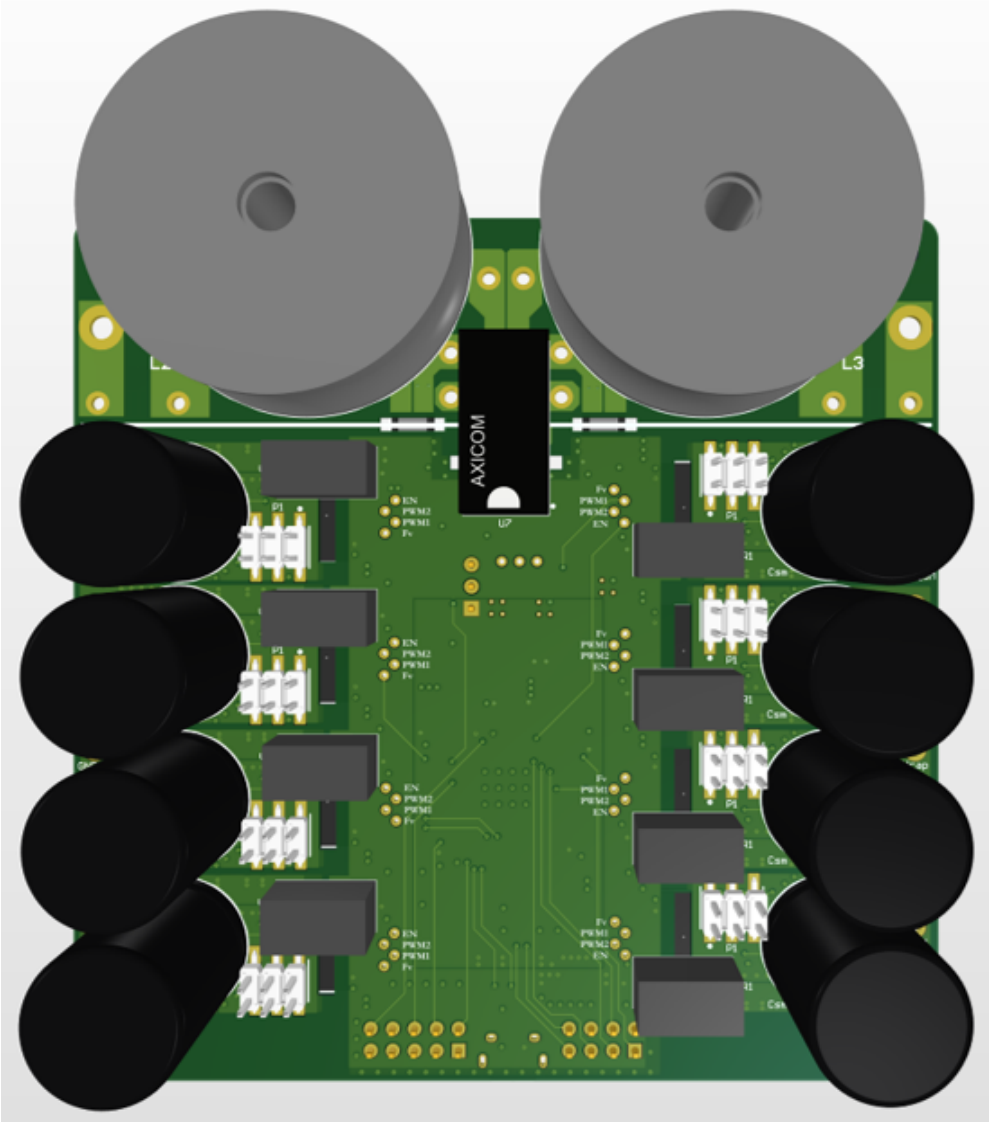


Figure 6.3: The bottom view of the μMMC

The layout of signal tracks, represented by the blue dashed lines in Fig. 6.4, is centered on the stack controller, an embedded STM32 micro-controller (μC). In the μC, two analogue to digital converter (ADC) pins are connected to the output pins of current sensors to read the voltages corresponding to stack currents; a general-purpose input/output (GPIO) pin is connected to the relay to control the switching status of the resistors. Besides, the μC also interacts with eight SMs through GPIO pins and timer modules (TIM) to measure SM voltages and control the switching of semiconductors. Universal serial bus (USB) Interface and Serial Peripheral Interface (SPI) are both reserved so that the μC is able to communicate with higher-level controller to realize sophisticated control schemes.

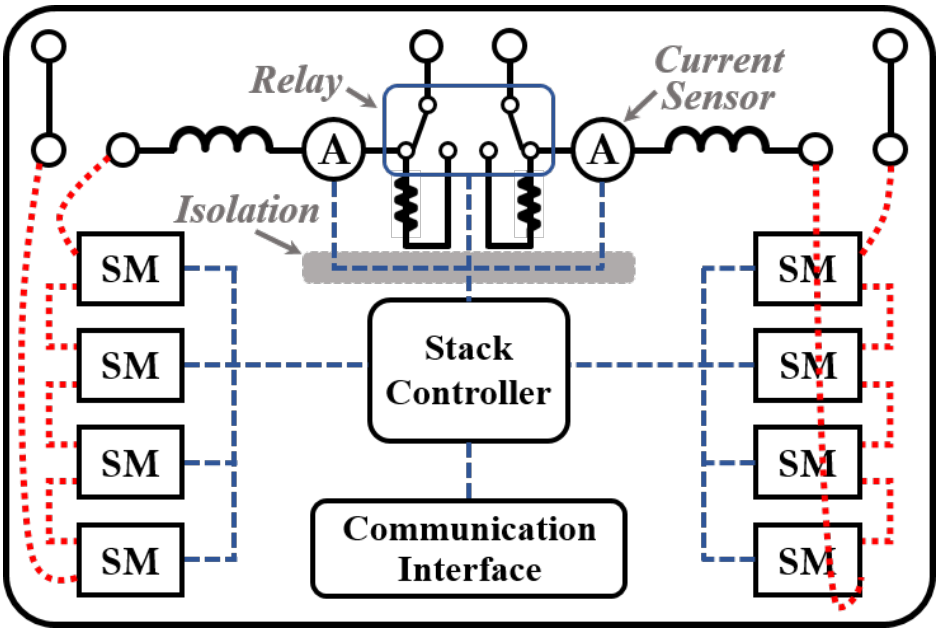


Figure 6.4: Overall layout of the μMMC.

6.2.2 Submodule

The design of the SM has taken supporting both HB and FB topologies into consideration. As shown in Fig. 6.5, two integrated HBs and a power capacitor are connected in parallel to construct the power circuit of the SM. Ports connected to the anode of the capacitor, the switch node of the first HB, the switch node of the second HB, and the cathode of the capacitor are all reserved, denoted as V_{SM}, OUT_1, OUT_2 and GND respectively in Fig. 6.5. The SM will operate as

an HB-SM when one of the OUT ports and GND are connected to the primary circuit, while if both OUT_1 and OUT_2 are connected to the primary circuit the SM becomes a FB type. The power capacitor can either be soldered in the PCB or be connected externally via V_{SM} and GND, making it is flexibility to change the capacitance as required for different applications.

Each HB is realized by a high-efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and integrated drivers. The switching states of the SM are controlled by an enable signal and two-channel PWM signals from the stack controller. A tiny μC is configured in the SM to measure the capacitor voltage and convert the voltage into a digital signal, denoted as f_V, of which the frequency is proportional to the SM voltage. Thus, voltages are transformed to digital signals and are transmitted through a digital isolator, and finally to the stack controller. Besides, the tiny μC is also used to light on a local LED (omitted in Fig. 6.5) when the measured voltage is in a safe range. Consequently, the state of the SM is demonstrated explicitly, as a reference for users to take corresponding actions.

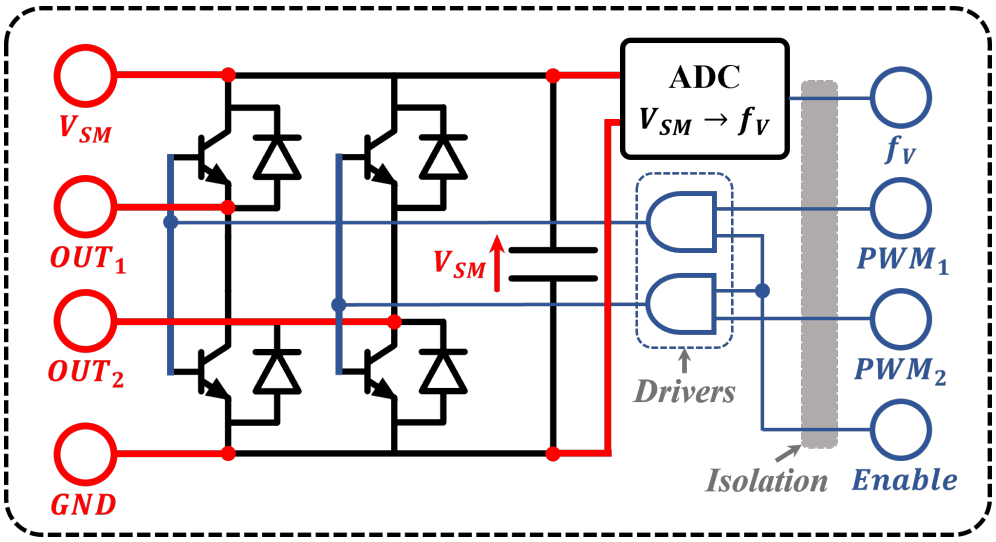


Figure 6.5: SM design in the μMMC.

6.2.3 Components Sizing

Capacitors sizing issue has been extensively investigated in [153], which proposes a mathematical model that estimates the energy deviation for the stacks of the

MMC during steady-state operation under any power factor and for AC voltage magnitude fluctuation of up to ±10%. The analysis is used to calculate the minimum size for the cell capacitors in order to keep their voltage fluctuation within set boundaries. The results show that the MMC requires $39\,kJ/MVA$ of capacitive energy storage under sinusoidal modulation. The corresponding function for the μMMC is:

$$\frac{3 \cdot 2 \cdot N_{SM} \cdot C_{SM} \cdot {V_C}^2\,(J)}{S_{\mu MMC}\,(VA)} = 39\,kJ/MVA = 39 \cdot \frac{10^3\,(J)}{10^6\,(VA)} \tag{6.1}$$

The rated power of the μMMC is set at $S_{\mu MMC} = 90$ VA. Then the minimum SM capacitance required is 5.2 mF. Take the operation margin and the commonly found size in the component market into consideration, the final value is 6800 uF.

The sizing for phase inductors is based on Eq.(6.2) to suppress second order harmonic current [193]. The selected value for inductors is 1.2 mH.

$$L_S \cdot C_{SM} > \frac{5\,N_{SM}}{48\,\omega^2} \tag{6.2}$$

6.2.4 Cost for Hardware

Aiming at developing an economical experiment bench-top that is suitable for education and research, much effort has been spent on the cost management of the μMMC. According to the market situation of electronic devices in July 2022, the total cost of a μMMC can be controlled at £62.79. With an order for more than 1000 pieces, the unit cost can be further reduced to around £50. Most of the MMC-related experimental research can be carried out on μMMC even with a small project budget. The cost of elements is summarized in Table 6.1 and extensively presented in Table 6.2. The detailed PCB design files and bill of materials (BOM) are provided on GitHub [194] for users' interest.

Table 6.1: Cost of Elements (July 2022)

Items	Price (1 piece)	Price (Mass Production)
Electronics Components	£58.56	£47.43
PCB Manufacturing	£1.22	£0.69
SMT Service	£3.01	£1.96
Total Price of a μMMC	£62.73	£50.08

6.3 Distributed Control System

The μMMC adopts a distributed control structure. The embedded stack controller and SM controllers within the PCB take into account both performance and cost. The μMMC can operate independently to realize the control algorithm that does not require strict computing resource, such as traditional Proportional Integral (PI) control, open-loop motor control, etc. With the communication interfaces reserved, the embedded controllers can also coordinate with external master controllers while they are decoupled physically. Advanced control algorithms that require high computational power can be realized with the master controller, while the controllers embedded in the μMMC undertake part of the control tasks, such as running MPC and Deep learning based higher level algorithm with Raspberry Pi or Jetson Nano, and leave the low-level control on the embedded controllers. In addition, the external controller can also coordinate multiple μMMCs to construct a more complex power electronic system. This section introduces the implementation of a three phase inverter mode MMCs based on one master controller and three μMMCs. The MMC control framework and related peripherals of the controllers are illustrated in Fig. 6.6. The overall control tasks are distributed to the master controller and the embedded stack controller.

6.3.1 Control Algorithm

The Master Controller undertakes energy management, power control and current control. As the output voltage of the MMC is constructed by SM voltages, SM

Table 6.2: Detailed Bills of Elements (July 2022)

Components	Manufacturer Part No	Packaging	Quantity	Unit Price	Total Price
SM Controller	ATTINY10-TSHR	6ST1_ATM	8	£0.33	£2.64
Phase Controller	STM32F407VET6	LQFP100	1	£12.92	£12.92
Current Sensor	ACS712ELCTR-05B-T	SOIC-8	2	£4.10	£8.20
Micro-USB Connector	10118194-0001LF	N/A	1	£0.39	£0.39
Telecom Relay	V23105A5001A201	DPDT	1	£3.64	£3.64
Arm Inductor	1140-122K-RC	Radial Leaded	2	£4.79	£9.58
SM Capacitor	KM688M016K25RR0VH2FP0	Radial Leaded	8	£0.30	£2.40
Isolated Power Supply	B0512S-1WR3	SIP-4 Module	8	£0.62	£4.96
Buck Power Stage Module	LP1130BSOF	SOP-8	16	£0.239	£3.82
Digital Isolator	SI8641BD-B-ISR	SOIC-16	8	£0.617	£4.94
ESD Suppressors	USBLC6-2SC6	SOT-23-6	1	£0.487	£0.487
Linear Voltage Regulator	HT7533-1	SOT-89-3	9	£0.108	£0.972
SMD capacitors, Resisters, Schottky diodes, LEDs, Connectors					£2.85
PCB manufacturing and SMT Service					£4.94
Total Price of a Micro-MMC					£62.73

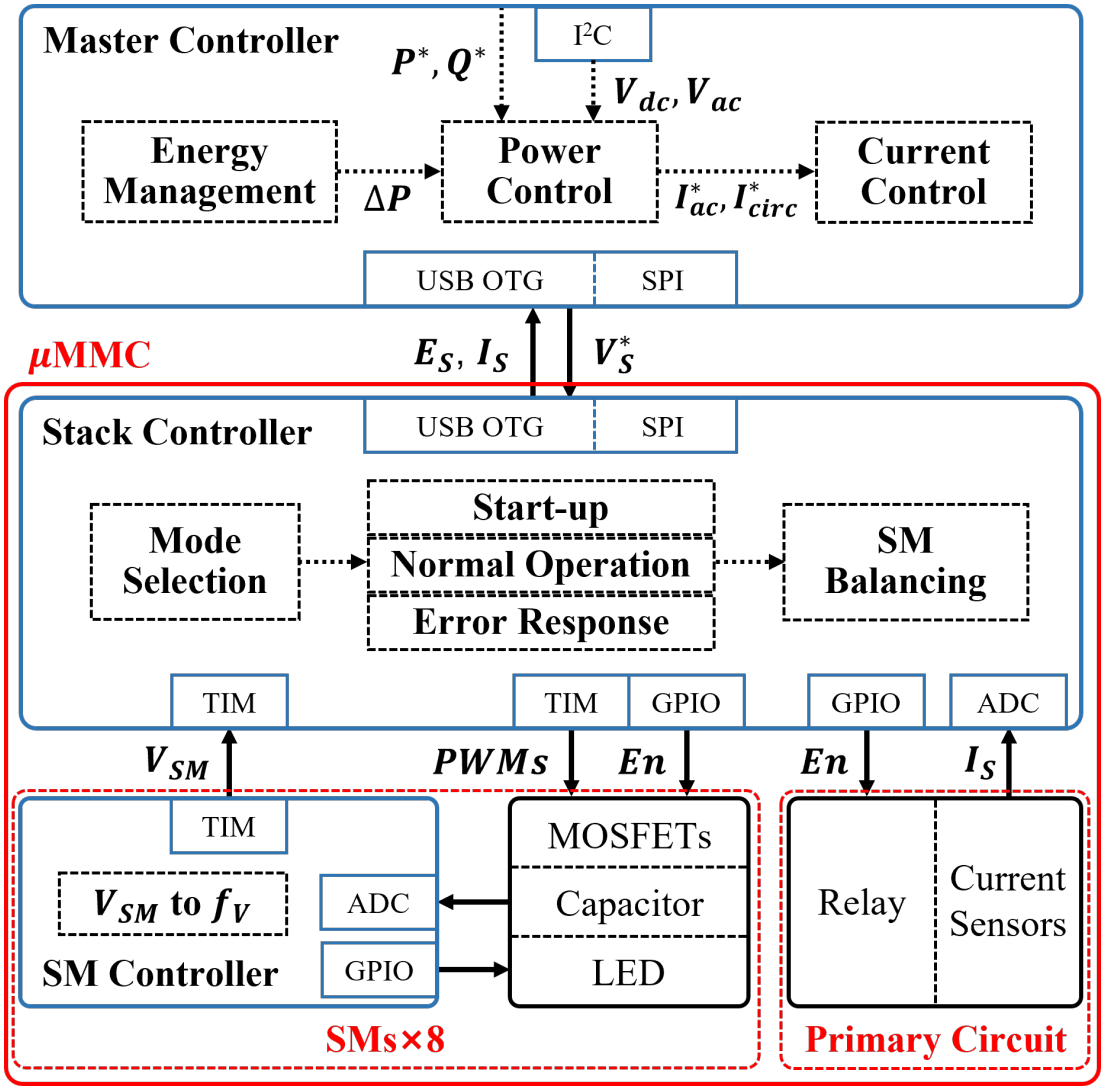


Figure 6.6: Control Framework and Peripherals.

capacitor voltage balancing, determined by the energy stored in the capacitors, is the prerequisite of normal operation. The objective of energy management in the master controller is to ensure that energy stored in each stack is converge to the rated value. The difference of the measured stack energy and the rated value is fed into PI controllers to generate the power correction command. Then power control takes the command, together with the set-points of active power and reactive power, and the measured DC and AC voltage, to calculate the AC current references and the circulating current references. Regarding the model and the variables presented in Fig. 6.1, the dynamics of phase A can be described by a set of loop voltage ordinary differential Eq. (6.3). Popular current controllers including DQ controller, LQR and MPC are all based on Eq. (6.3). The outputs of the current controller, stack voltage references (V_{S1} and V_{S2}), are finally calculated from the stack currents (I_{S1} and I_{S2}), the AC and DC side voltage (U_A and V_{DC}) and the current references.

$$\begin{cases} u_A + L\dfrac{d(I_{S1} - I_{S2})}{dt} + L_S\dfrac{dI_{S1}}{dt} + V_{S1} - \dfrac{1}{2}V_{DC} = 0 \\ u_A + L\dfrac{d(I_{S1} - I_{S2})}{dt} - L_S\dfrac{dI_{S2}}{dt} - V_{S2} + \dfrac{1}{2}V_{DC} = 0 \end{cases} \tag{6.3}$$

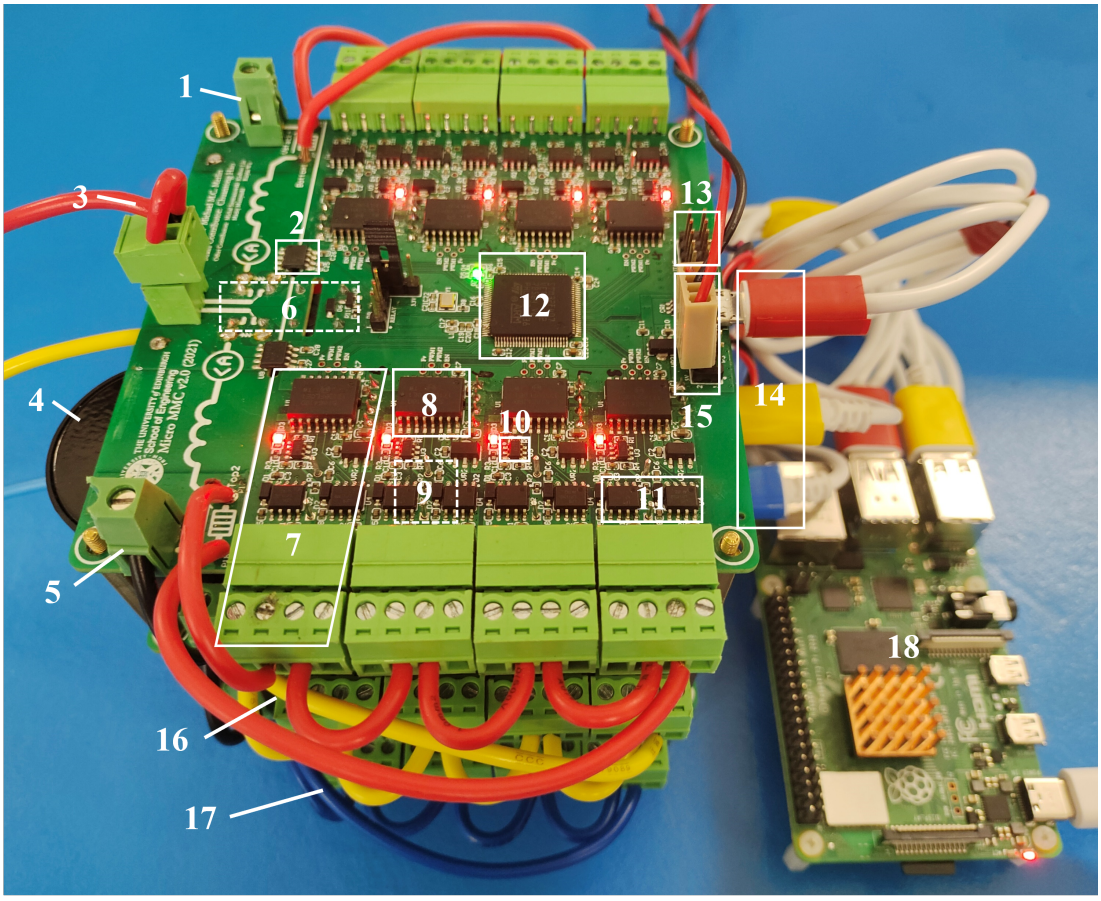
The Stack Controller is embedded in the μMMC. SM voltages and stack currents are measured and applied for selecting the operation mode. During normal operation, the fundamental task of the stack controller is to generate PWM signals to control the switching states of semiconductors so that the stack voltage formed by SM voltages tracks the stack voltage references transmitted by the master controller. Meanwhile, the voltage balancing of different SMs within one stack is realized by periodically choosing certain SMs to be inserted into the conducting circuit. The SM are sorted by their capacitor voltages. If the stack current is in the direction of charging the stacks, the SM with the lowest voltage will be allocated the highest priority to be inserted, and vice versa. When the average SM voltage is lower than a certain threshold, the stack controller will operate in start-up mode and charge the capacitors until their voltage reach the rated value. The third mode is error response when the SM voltage or stack up exceeds the safety value. The stack resister will be switched in the primary circuit

and all SMs will be blocked to protect the components from damaged.

6.3.2 Concrete Implementation

Generally in power electronics design, voltages are measured by ADC peripherals of controller or specially-designed voltage sensing Integrated Circuit (IC). However, the SM voltages in MMC are floating rather than grounded to the primary circuit, making it's impossible to measure multiple SM voltages directly with ADC peripherals on a single controller. Besides, analog signals are more likely to be interfered by noises than digital signals. Compared to voltage sensing IC, the solution in the μMMC converts voltages into digital signals in a much more economical way. As is illustrated in the left bottom of Fig. 6.6, the SM controller reads the voltage from a potentiometer on ADC, and then uses it to set the compare match register of TIM, to generate a square wave whose frequency is linear proportional to the input voltage.

The square waves generated by SMs are decoded by the stack controller with TIM modules operation in input capture mode. Whenever a specified signal edge occurs on the input capture channel pin, the current value of the TIM counter is captured and saved to the input capture register (CCR). The time period of the input signal is calculated by the difference between the CCR values of two adjacent rising or falling edges and the clock frequency of the TIM module. Together with the linear Frequency/Voltage function obtained from the SM controller, the SM voltages can be inversely derivated in the stack controller. The current version μMMC applied a STM32 μC as stack controller. The μC offers three 12-bit ADCs, sixteen general-purpose TIMs, sufficient GPIOs and standard and advanced communication interfaces. So, it is capable to handle low level control of two stacks, eight SMs. In addition, the STM32Cube Hardware Abstraction Layer (HAL) [195] used for programming the stack controller offers high-level and feature-oriented Application Programming Interface (API), and help accelerating the development process. With the high-portable HAL, the low level control framework illustrated in Fig. 4 can be easily implemented in the μMMC by students or engineers.



1: DC+ Connector	7: Sub-Module	13: Debugger Connector
2: Current Sensor	8: Digital Isolator	14: Micro-USB Ports
3: AC Output Connector	9: SM Capacitor(Bottom)	15: SPI/Power Connector
4: Arm Inductor	10: SM Controller	16: Phase B
5: DC- Connector	11: Half Bridge Modules	17: Phase C
6: DPDT Relay(Bottom)	12: Stack Controller	18: Master Controller

Figure 6.7: Experiment Setup of a three phase inverter mode MMC.

The communication between the μMMC and the external master controller are conducted by USB [196] or SPI [197, 198] interfaces. The USB provides the most successful serial interface having the characteristics of simplicity and flexibility (plug-and-play), bi-directionality, increasing speeds, and low cost. The intelligent mechanism allows USB system to detect the device attachment and detachment at any time. SPI is a synchronous communication scheme with a separate clock wire, apart from the signal wires and chip select wire, so it can work up to faster speed than what Universal asynchronous receiver-transmitter (UART) [199] and Inter-Integrated Circuit (I2C) [200] can provide. The μMMC operates in USB device mode or SPI slave mode, so technically multiple μMMCs can be controlled by a single master controller to demonstrate a more sophisticated power electronics system.

Table 6.3: Micro-MMC Operation Parameters

Parameters	Values	Parameters	Values
Active Power	90 W	Load Resistance	20 Ω
Number of SMs (per stack)	4	Nominal SM Voltage	4 V
AC Line Voltage (Amplitude)	7 V	DC Voltage	16 V
AC Frequency	50 Hz	PWM Frequency	10 kHz
Master Controller Execution Frequency			1 kHz

MATALB/Simulink provides comprehensive support packages [201] for hardware development boards (e.g. Raspberry Pi, TI LaunchPad, Arduino, STM32 Nucleo...), allowing the transition from simulation models to hardware programs in hours to be practical. After creating the Simulink model, users can simulate the model and download the completed algorithm for standalone execution on the development boards. MATALB/Simulink has also offered a particularly useful capability to tune parameters live from the Simulink model while the algorithm runs on the hardware. Both the communication interfaces on the master controller and the control algorithms can be configured through graphical interfaces, greatly shortening the process from theory to practice.

6.4 Case Study

To verify the performance of the proposed μMMC and the control framework, this section demonstrates a three phase inverter mode MMC constructed by three μMMCs and a Raspberry Pi serving as the master controller. The experiment setup is presented in Fig. 6.7 and all key components are listed. Each μMMC operates as one phase of the MMC, configured by red, yellow and blue wires and USB cables representing Phase A, Phase B and Phase C respectively for the sake of distinguishing. The MMC converts 16V DC voltage from the power supply, to 7V three phase AC voltage output on three 20 Ω star-configured resistive loads. The Raspberry Pi communicates with the μMMCs through USB interfaces. Energy management and voltage and current double closed-loop control models are built in Matlab/simulink and downloaded to the Raspberry Pi. The control objective is to track the sine waves output voltage references, whose frequency is 50Hz and amplitude is 7V, and meanwhile maintain the voltage balancing of all SMs. The system parameters are summarized in Table 6.3. The number of SMs per stack is restricted by the PWM pins of the μC and the size of the PCB. Eight PWM channels are occupied for singe phase MMC with two stacks. To ensure a low THD of the output voltage, the PWM frequency is set at 10 kHz.

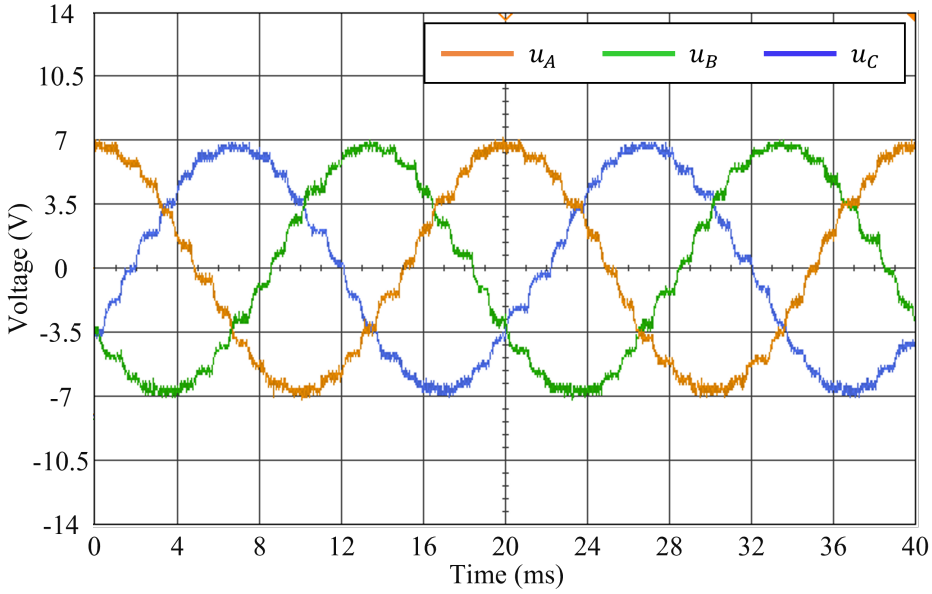


Figure 6.8: Three phase AC output voltage.

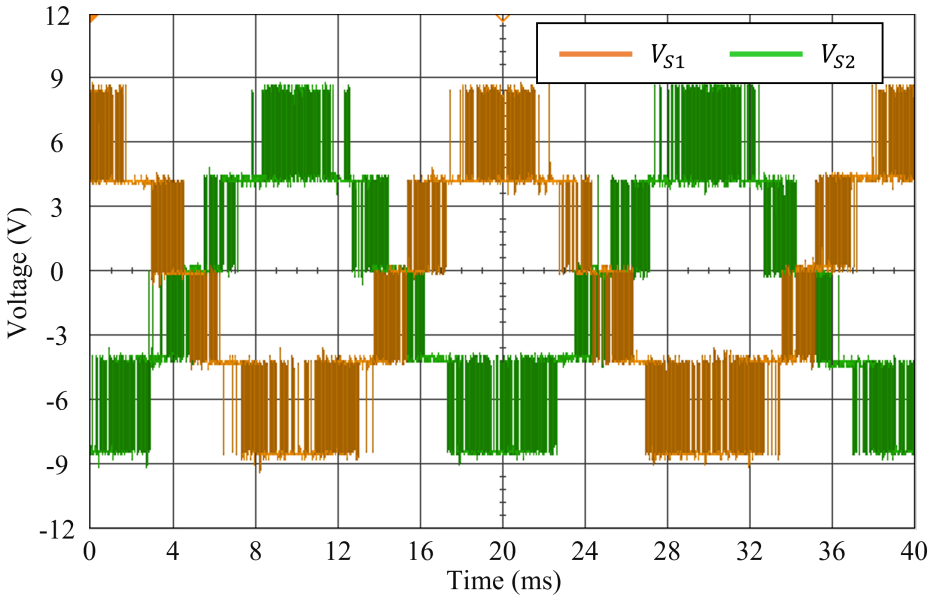


Figure 6.9: Stack voltages of Phase A.

Two cycles of the three phase output voltages are shown in Fig. 6.8. The output voltages are in standard sine wave and track the frequency and amplitude of the references accurately. The master controller frequency is set at 1 kHz, which means the voltage references are updated at every 1 ms. The outputs of the μMMCs are connected to the resistive loads directly without filters. Consequently, high order harmonics resulted by the controller intervals can be seen on the voltage outputs. Such harmonics can be simply removed with conventional inductive filters.

Fig. 6.9 presents the stack voltages of Phase A. Both the upper stack voltage and the lower stack voltage are in typical staircases and complementary in amplitude, showing that the stack controller and the semiconductors in the μMMCs operate normally. It should be noticed that the stack voltages are floated from each other and measured with differential probes. The voltage scale matters rather than the specific values of the labels in the vertical axis.

The capacitor voltages of four SMs in the upper stack of the phase A are shown in Fig. 6.10. The SM voltages balancing are ensured in a long time scale, indicating the effectiveness of the SM balancing algorithm implemented in the stack controller. In addition, Fig. 6.11 presents four SM voltages in four different

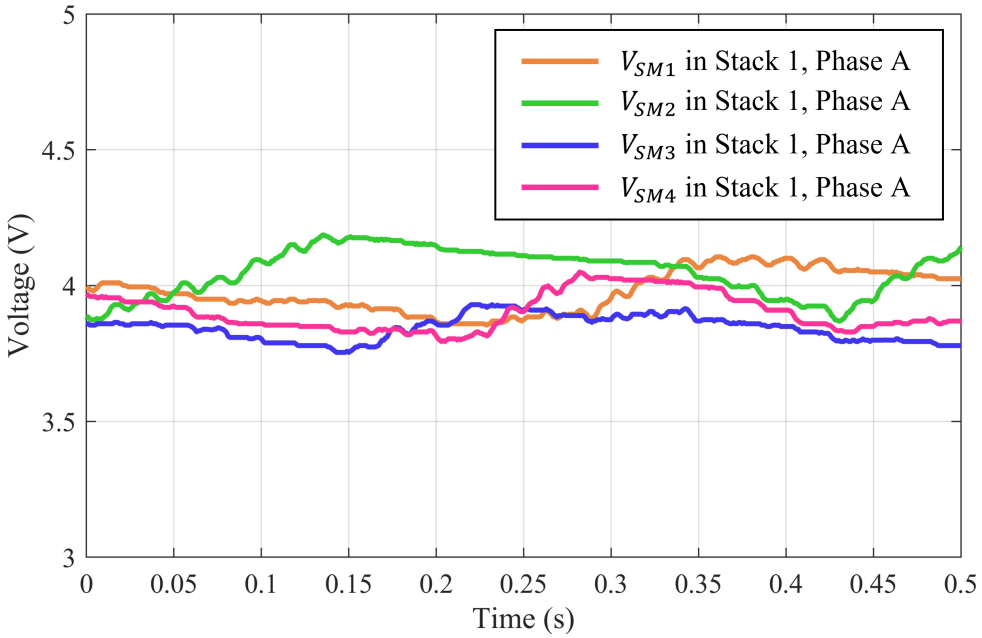


Figure 6.10: SM voltages in a single stack.

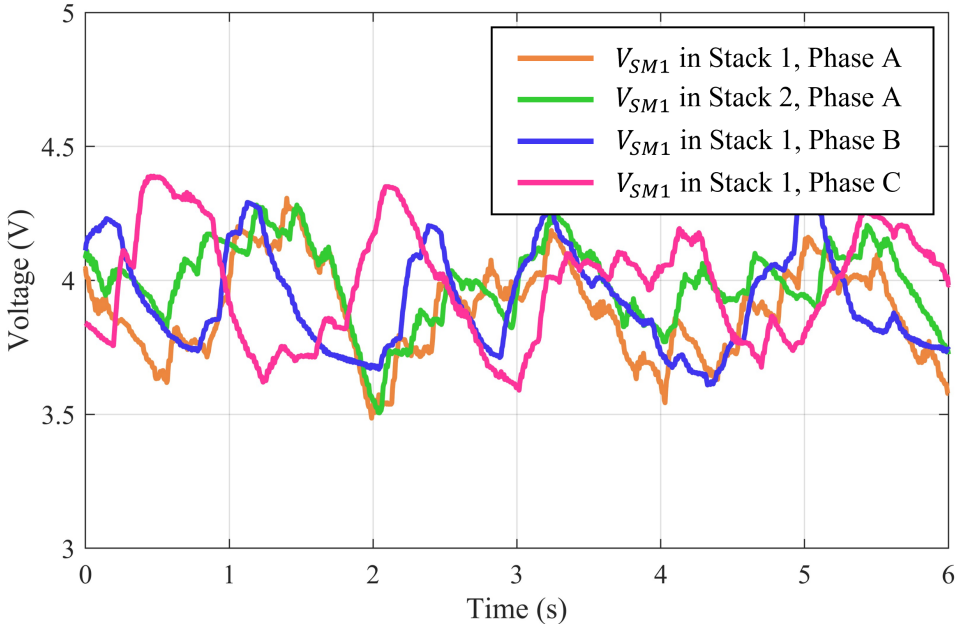


Figure 6.11: SM voltages in four different stacks.

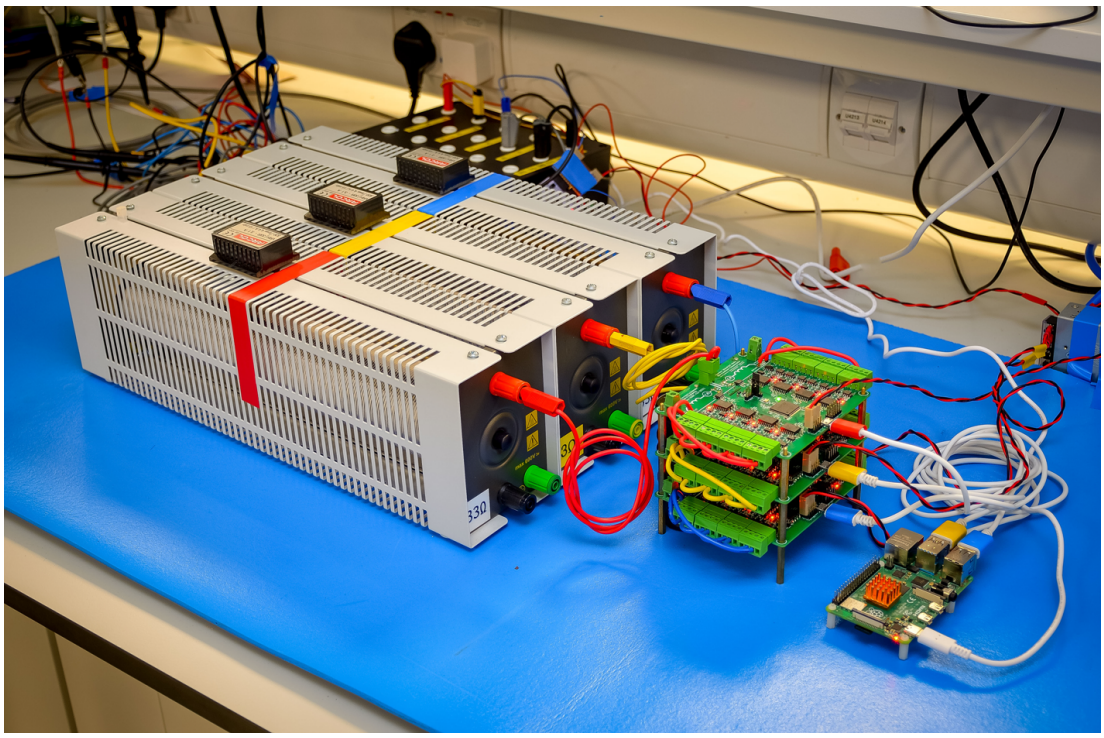


Figure 6.12: The Overall Experimental Setup for a Three-phase, Inverter-mode, Resistive-load MMC.

stacks. All voltages are balanced and converged to the nominal SM voltage, 4V. As has been introduced in Section III, SM voltages are measured by the SM controller and decoded by the stack controller, then transmitted to the Raspberry Pi through USB interface for energy management. The results presented in Fig. 6.10 and Fig. 6.11 have proved the coordination between controllers in different layers can achieve expected results.

Fig. 6.12 presents the overall experimantal setup where three rheostats serve as resistive loads, and three μMMCs operate together as a three phase inverter mode MMC. The master control algorithm is simulated and compiled in Simulink, as shown in Fig. 6.13, and then downloaded to the Raspberry Pi controller via the Simulink Hardware Support Package. The whole procedure doesn't require line-by-line programming and coding. Besides, the I2C signals representing voltage measurement results are illustrated in Fig. 6.14. Fig. 6.15 presents details of the communication ports, which are distinguished by different colored wires representing three different phases.

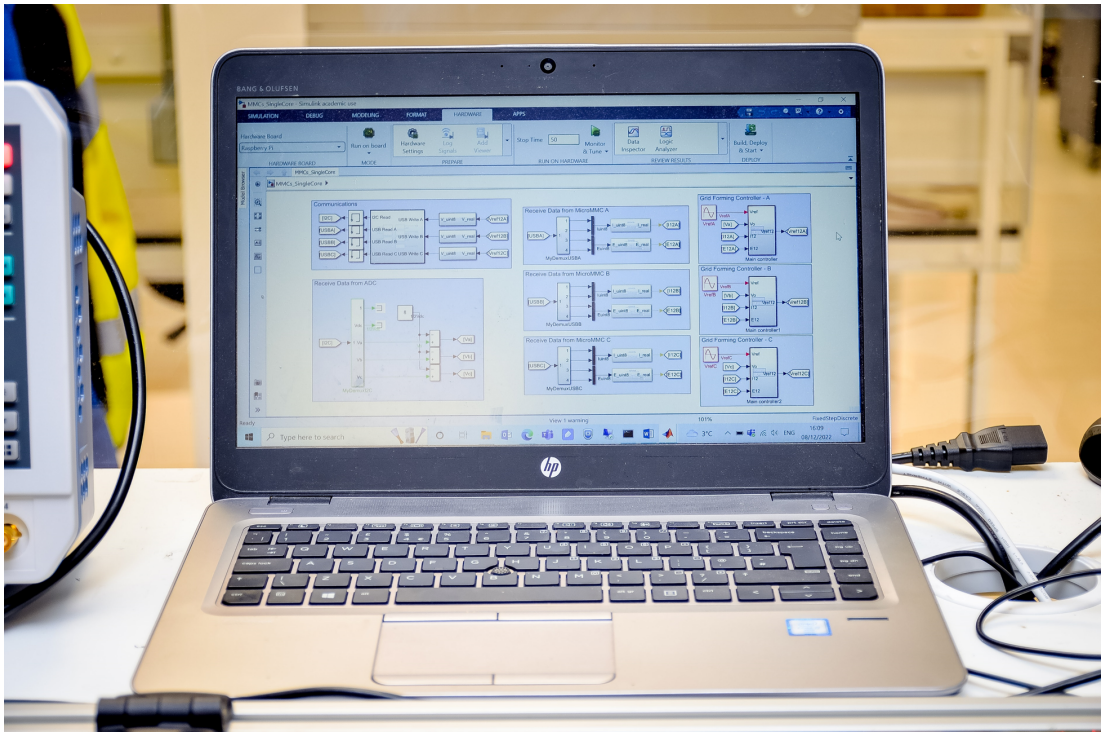


Figure 6.13: The Master Control Algorithm implemented via the Simulink Hardware Support Package.

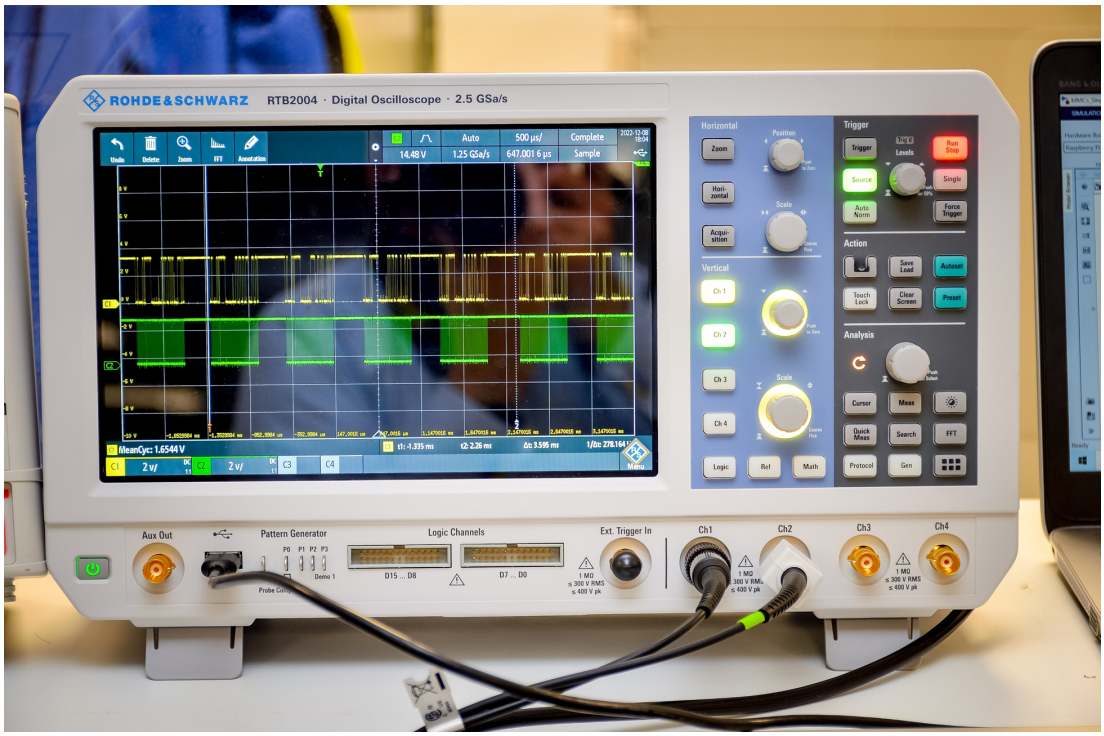


Figure 6.14: I2C Signals for Transmitting Voltage Measurement Information.

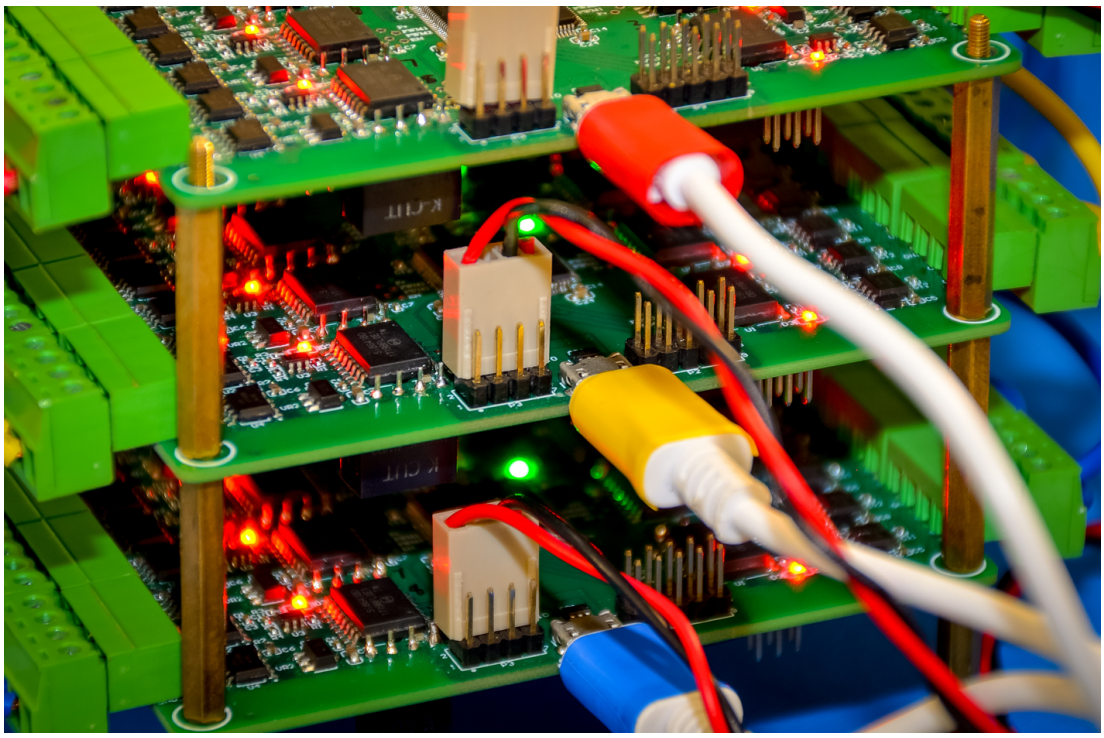


Figure 6.15: Details of the Communication Ports.

6.5 Summary

This chapter introduces the hardware design of the μMMC, which integrates eight FBSMs in a 10×10 cm PCB with an embedded μC and communication interfaces to interact with an external master controller. The cost for a single μMMC could be around 50 pounds for mass production. Then the control framework and concrete implementation are presented in detail. With the application of the μMMC, the STM32Cube Hardware Abstraction Layer, and the MATLAB/Simulink hardware support packages, it is possible to shorten the transition process from simulation to hardware realization to several hours. The experiment setup and results of a three phase inverter mode MMC verify the effectiveness, scalability and convenience of the proposed μMMC.

Chapter 7

Conclusion

7.1 Summary of the Thesis

This thesis presents the MBSM MMC and the distributed control system for HVDC applications. The topology, basic states, soft-parallel mechanism, single device failure management, and reliability study are introduced first. The operation principle of the MBSM designs and how the MBSM approach can eliminate in-rush current during the paralleling of MBSMs are introduced. Then, single device failure management and the reliable study are presented. In the end, the multi-busbar equivalent of the classic full-bridge SM topology is simulated and compared with its single-busbar counterpart. MBSM improves performance at the cost of doubling the number of semiconductors compared to conventional FBSM. For applications that are sensitive to cost, it's hard for the MBSM to be considered before the price of semiconductors goes further down.

The rigorous mathematical framework for an elegant and automatable independent variables state space modelling of a linear electrical circuit is presented. The proposed automatised derivation strategy is verified by a simple case of electrical circuit and a case of MMC. Besides, the MPC-based MBSM MMC start-up control scheme is proposed, where the precharge of capacitors is converted into a DCDC converter control problem and solved by MPC, which has greatly simplified the precharge of capacitors in MMC. Then, a reinforcement learning approach is applied for MBSM low level control. A DQN agent is designed and trained to

improve the voltage reference tracking, SM voltage balancing and switching frequency reduction performances.

More applications of the MBSM in the scenario of STATCOM are investigated in Chapter 5. The modeling and higher control of the delta configured STATCOM, and how ES is configured in MBSMs are provided first, and then a STATCOM with distributedly integrated partially-rated ES in MBSMs is investigated. The study uses the analytical formulation of the MBSM to derive the mixed mode low level control system and the optimal phase angle of the circulating current required for SM balancing. The objective of the controller is to output 1 p.u. active power with 60 % ES-MBSMs. What's more, the structure and low level controller to allow ES-MBSMs to be configured in a sub-stack in order to reduce the switching frequency are studied. The concept of MBSM is further extended to structure with more busbars, named multi-H-bridge SM. The new structure and the operation principle of multi-H-bridges are introduced first, and followed by a detailed low-level control algorithm aimed at solving the unequal steady-state current issue resulting from on-state resistance mismatches of paralleled discrete SiC MOSFETs.

The micro-MMC consisting of a benchtop-scale, low-voltage, open-source, and affordable hardware prototype of a MMC, intended for research and teaching applications, is finally introduced in this thesis. The micro-MMC aims to provide a solution to break the barrier from theory to practice, thanks to its all-integrated 8 full-bridge sub-modules in a 10×10cm PCB with a local microcontroller able to communicate with an external master controller. The electronics is rated for a 30V DC bus voltage as typically found in traditional lab power supplies, providing both convenience and safety. This structure allows a lot of flexibility in terms of testing converter topology and control architectures. The setup process of the µMMC into a 3-phase inverter is detailed to demonstrate its versatility and potential as a teaching and research tool.

The concept of MBSMs and the distributed control framework are proved by rigorous theoretical analysis, modeling and simulation, and experimental verification presented in this thesis.

7.2 Reflections on MBSMs

The price for discrete MOSFETS and IGBTs is expected to remain steady despite growing demand. Besides, wide band-gap semiconductors are playing increasingly significant roles in the power electronics industry. Power semiconductors are paralleled for larger current applications, while are connected in series in high voltage scenarios.

In the same voltage level applications, the MBSM is built with twice the number of semiconductors as its IGBT-based FBSM counterpart, as introduced in Chapter 3. However, it should be noted that the MBSM has the same number of discrete SiC MOSFETs as conventionally integrated SiC MOSFET power modules in the same current-level applications, as shown in Section 5.4. MBSM and its corresponding low-level control method provide a new solution for the integration of discrete semiconductors. MBSM's scalability in both series and parallel connections provide extra flexibility in both voltage rating and current rating of power converters. Even though a more complex low-level control algorithm is necessary for the MBSM, the better performance it exhibits makes this new SM topology attractive for further research.

The advantages of the MBSM are recalled and summarized as follows:

(1) The MBSM allows for easier start-up and shut-down since the bypass switches connect the capacitors in parallel.

(2) Paralleling of SM capacitors results in a lower individual SM capacitor voltage deviation; hence, smaller capacitors could be applied.

(3) Redundant SMs can stay in bypass mode while still charged, thus minimizing power losses and switch-in time. Better management of the bypass switches in case of SM failure.

(4) Some switching combinations offer multiple current paths, thus lowering the overall conduction losses of the stack of MBSMs.

(5) The MBSM can have any sets of positive and negative voltage levels to minimize the number of semiconductor devices in the conduction path while retaining the above features.

(6) The MBSM is still a modular design for easy design and manufacturing.

(7) More switching combinations of the MBSM provide potentially better temperature and wear-out distribution.

7.3 Future Works

Many aspects of the topic presented in this thesis remain subject to further investigation, including but not limited to:

Investigating MBSM with even more Busbars:

More busbars provide more freedom of degrees for semiconductor state combinations. In addition to improving power efficiency, the management of semiconductor states can also improve temperature and wear-out distribution. Future work could focus on developing the corresponding low-level controller for MBSMs with more busbars.

Building Experimental Platform to Validate the MBSM Concept:

The results related to the MBSM MMC provided in this thesis are from simulation models. Subsequent research could focus on the development of an MBSM MMC prototype to further validate the concept of MBSM. Since the MBSM makes full use of the characteristics of power diodes, IGBTs and anti-parallel diodes are preferable to power MOSFETs in the design of the prototype.

Training large Neutral Network for Improved Performances:

There is still much room for improvement in the performance of the RL based low level control. The results is based on a single-phase model with only eight MBSMs in each stack due to computing resource constraints (CPU in personal computer). Training larger DQN networks with commercial GPU clusters could help to improve performance even further. Besides, other performances can also be considered in the design of the reward. Potentially, the effect of different NN types or NN layers can also be investigated in future work.

Building the open-source community of the micro-MMC:

Related files developed by the author have been uploaded on GitHub [194], including PCB files, bill-of-material forms, controller algorithm files, user manuals, photos of demonstrations, and so on. Many other interesting ideas could also be tried on the micro-MMC prototype. All users are welcome to download the related files, order the PCBs, explore new ideas, provide comments and feedback, and contribute to the open-source community of the micro-MMC.

Appendix A

Algorithms

Algorithm 1 Soft-paralleling based sub-stack voltage reference creation algorithm

Input: V_{stack}: Stack voltage reference;
V_C: MBSM capacitor voltages;
I_{stack}: Stack current;
N_{ES}: Number of ES MBSMs;
N_{Cap}: Number of Normal MBSMs;

Output: V_{ES}: ES sub-stack voltage reference;
V_{Cap}: Normal sub-stack voltage reference;
$Flag$: Flag indicating whether control the whole stack (= 1) or two sub-stacks (= 0);

Calculate average MBSM voltage V_{aver}, average ES-MBSM voltage V_{ESaver} and average normal MBSM voltage V_{Caver}, calculate the sign of stack current $sgn(I_{stack})$;
if $(sgn(I_{stack}) \cdot V_{stack}/V_{aver} \geq N_{Cap}) \vee (sgn(I_{stack}) \cdot V_{stack}/V_{aver} \leq -N_{ES}) \vee (V_{ESaver} < V_{Caver})$ **then**
    $Flag = 1$;
else
    $Flag = 0$;
    if $(sgn(I_{stack}) \cdot V_{stack}/V_{aver} \geq N_{Cap} - N_{ES})$ **then**
        $V_{ES} = V_{stack}/V_{aver} - sgn(I_{stack}) \cdot N_{Cap}, \quad V_{Cap} = sgn(I_{stack}) \cdot N_{Cap}$;
    else
        $V_{ES} = -sgn(I_{stack}) \cdot N_{ES}, \quad V_{Cap} = V_{stack}/V_{aver} + sgn(I_{stack}) \cdot N_{ES}$;
    end if
end if

Algorithm 2 Soft-paralleling based gate signals generation algorithm

Input: V_{ref}: Voltage reference of the stack (or sub-stack);
V_{sm}: MBSM voltages of the stack (or sub-stack);
$Carrier$: Carriers for all MBSMs in the stack (or sub-stack);
N_{sm}: Number of MBSMs in the stack (or sub-stack);
I_{stack}: Stack current;

Output: Gate signals

1: **for** $i = 1 \rightarrow N_{sm}$ **do**
2: Assign $Carrier(i)$ to the corresponding terminal or interconnections;
3: Compare $V_{ref}/\sum V_{sm}$, Get states: (1) $State(i) = 1$, if $N_{ref} > Carrier(i)$, (2) $State(i) = 0$, if $Carrier(i) \geq N_{ref} > -C(i)$, (3) $State(i)$ = -1, if $N_{ref} \leq -Carrier(i)$;
4: **end for**
5: Translate states to gate signals.

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