Optimisation of High Reliability Integrated Motor Drives

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Optimisation of High Reliability Integrated Motor Drives

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This dissertation is submitted for the degree of

Doctor of Philosophy

October 2023

I would like to dedicate this thesis to my family, friends, my supervisors and everyone else who supported me along the way …

Publications

1. H. Calder, A. Horsfall, M. Shahbazi, **"Optimal Device Selection Tool For Discrete SiC MOSFETs Considering Switching Loss Challenges Of Paralleled Devices"**, 2022 Power Electronics and Motor Drives (PEMD), Conference Paper

2. L. Robinson, H. Calder, A. Gallant and A. Horsfall, **"Short circuit ruggedness of SiC MOSFETs for high reliability applications"**, 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1-7, doi: 10.1109/ECCE50734.2022.9947766.

Abstract

The development of integrated motor drives (IMDs) with high volumetric power density and reliability are crucial for the continued development and adoption of electric vehicles (EV). The development of the wide bandgap (WBG) devices, especially Silicon Carbide (SiC) MOSFETs, enables new possibilities for traction drive systems. However, to maximise the benefits of SiC, the IMD design process, including passive component selection, control and thermal management should be optimised. This thesis goes through the initial major design steps in SiC power system design, from SiC device analysis and modelling to circuit design and electrothermal simulation of an IMD system.

A novel approach to discrete SiC MOSFET selection, using a method of calculating performance based on experimental data, is described. Dynamic behaviour of a family of 1200 V MOSFETs is studied at temperatures up to 175 °C using a double pulse test to show the combined effect of the differences in internal design between MOSFETs with different current ratings. It is observed that the 30 mΩ MOSFET had a 24 % higher switching loss than a 140 mΩ at a 30 A load current. The study then goes on to compare the effect of switching frequency, paralleling of MOSFETs and the device type used to demonstrate the inverter design with the lowest power losses, which will equate to low temperatures and high lifetime.

The novel methodology can find the optimal choice of MOSFET from the family, and number required through paralleling, for a circuit when given the load current, temperature and switching. Understanding the device interdependencies in a single family is utilised to also predict the relative performance between SiC MOSFETs from different manufacturers.

An axial-flux permanent magnet synchronous motor (PMSM) driven by a three-phase SiC inverter is simulated in PLECS using experimentally validated MOSFET models chosen by the device selection methodology. Electrothermal analysis shows the influence of switching frequency, temperature, MOSFETs paralleling and DC-link capacitance on voltage ripple, total harmonic distortion, efficiency and MOSFET loss and temperature profiles. With a 60 % decrease in THD and 50 % increase in maximum MOSFET junction temperature when switching frequency is increased from 10 to 100 kHz.

The high-temperature stress on the semiconductors due to close proximity with the machine stator means reliability is an important consideration that is yet to be fully investigated in IMD optimisations. This study uses a lifetime model specific to the transistor package TO-247 in reliability optimisation for IMD for the first time. It requires detailed MOSFET simulation outputs to provide a highly accurate lifetime for discrete SiC MOSFETs.

Both single and multi-objective optimisations of the volume and lifetime of the three-phase inverter are presented. The single objective optimisation demonstrates the minimum volume and the corresponding switching frequency and lifetime when between three and six MOSFETs are paralleled at a temperature range between 50 and 150 °C. Design constraints were set limiting the feasible switching frequency range to between 13 kHz because of THD and 118 kHz because of efficiency limits, corresponding to required DC-link capacitors of 520 and 55 μF respectively. Increases in temperature were found to further limit the maximum switching frequency and therefore increase the minimum volume of the inverter. A Pareto front identifies a range of possible solutions for the volume and lifetime of an inverter with six paralleled MOSFETs through the multi-objective objective procedure. Further analysis of these possible solutions identified a single optimal solution for the system, using a DC-link capacitance of 190 μF at 45 kHz, giving a combined volume of the capacitor and MOSFETs of 440 cm^3 and a lifetime of 12,000 hours.

Finally, the electrothermal analysis of a dual inverter driving a symmetric six-phase PMSM is presented with the benefits of modular multi-phase systems in IMDs summarised. Effect on performance of lower per-phase current, interleaving strategies and fault tolerance

are analysed and compared to equivalent three-phase systems, for 60 kW and 120 kW operation.

A novel method for lifetime prediction of systems with paralleled MOSFETs or fault tolerance capabilities considering incremental damage is developed based on TO-247 lifetime calculations from PLECS simulation, and component-level reliability profiles using Monte Carlo analysis. The dual inverter is used to model the system and implements control schemes for both single-phase and single inverter failure while maintaining the 4000 rpm and 140 Nm speed and torque requirements. A twofold increase in B_{10} lifetime of is observed when the effect of paralleled SiC MOSFETs prevents immediate system failure in a three-phase inverter.

A computational fluid dynamics (CFD) and 3D finite element thermal model are designed to study the inverter behaviour based on the thermal analysis of its shared cooling plate with a 300 mm diameter axial flux PMSM. Concentric layout designs minimise the variation of junction temperatures to 5 °C and the effect of the flow rate and temperature of the coolant in the PMSM cold plate is presented between 5 and 30 l/min.

The multi-objective optimisation procedure used to compare the dual inverter demonstrated it outperformed the three-phase inverter with 15 % smaller required DC-link capacitance, higher efficiency and increased lifetime in part due to its fault-tolerant nature. The optimal dual inverter considering the design constraints consists of four 40 μF KEMET film capacitors operating with a switching frequency of 46 kHz giving an inverter volume of 300 cm^3 and a lifetime of 16.3 years, assuming 1000 hours of operation annually.

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Nomenclature

Acronyms

AHM	Axially housing mounted
ASC	Active short circuit
ASM	Axially stator mounted
BEV	Battery electric vehicle
CDF	Cumulative distribution function
CFD	Computational fluid dynamics
CTE	Coefficient of thermal expansion
DFVC	Direct flux vector control
DPT	Double-pulse test
DUT	Device under test
EMI	Electromagnetic interference
EMI	Electromagnetic interference
EV	Electric vehicle
FEA	Finite element analysis

FOM	Figure of merit
GaN	Gallium nitride
IMD	Integrated motor drive
IMMD	Integrated modular motor drive
LUT	Look-up table
MLI	Multi-level inverter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPI	Multi-phase inverter
MPPF	Metallised polypropylene film
NPC	Neutral point converter
PDF	Probability distribution function
PE	Power electronics
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
RHM	Radially housing mounted
RSM	Radially stator mounted
SiC	Silicon carbide
SVPWM	Space vector pulse width modulation
THD	Total harmonic distortion
TRN	Thermal resistance network

VSI	Voltage source inverter
WBG	Wide bandgap

Variables

α	Coffin-Manson exponent
ΔT	Temperature swing
ΔV_{pp}	Voltage ripple
η	Efficiency
λ	Thermal conductivity
λ_f	Failure rate
μ_n	Electron mobility
v_{sat}	Saturation electron drift velocity
ω_m	Mechanical speed
ϕ_d	D axis flux
ϕ'_m	Flux induced by magnets
ϕ_q	Q axis flux
ε_r	Relative dielectric constant
B_x	Time when a group of samples has x probability of failure
C_{DS}	Drain-source capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance

C_{iss}	Input capacitance
C_{min}	Minimum required capacitance
C_{oss}	Output capacitance
C_{ploss}	Power loss from capacitor
C_{rss}	Reverse transfer capacitance
C_{ths}	Capacitor hot spot temperature
D	Damage
E_A	Activation energy
E_G	Bandgap
F	Friction constant
F_{com}	Failure function of component
F_{sub}	Failure function of sub-system
f_{sw}	Switching frequency
F_{sys}	Failure function of system
FOM_{iss}	Input figure of merit
g_m	Transconductance
I_0	Full load current
I_b	Current per bond
I_D	Drain current
i_d	D axis flux current

I_g	Gate current
i_q	Q axis flux current
$I_{C(RMS)}$	Capacitor RMS current
J	Inertia
K	Basic lifetime
k	Boltzmann's constant
L	Load inductance
L_d	D axis stator inductance
L_q	Q axis stator inductance
L_σ	Parasitic inductance
L_σ	Stator leakage inductance
n	Voltage stress factor
N_f	Number of cycles to failure
Q_{GD}	Gate-drain charge
Q_{GS}	Gate-source charge
Q_g	Total gate charge
Q_{iss}	Input gate charge
R_G	Gate resistance
R_s	Stator resistance
$R_{DS(on)}$	On-state resistance

R_{ESR}	Capacitor equivalent series resistance
$R_{G_{int}}$	Internal gate resistance
$R_{th,c-a}$	Thermal resistance between capacitor and ambient
$R_{th,j-c}$	Thermal resistance between junction and case
T_a	Ambient temperature
T_e	Electromagnetic torque
t_f	Fall time
T_j	Junction temperature
T_m	Load torque
t_r	Rise time
$t_{d(off)}$	Turn-off delay time
$t_{d(on)}$	Turn-on delay time
$t_{d(on)}$	Turn-on delay time
T_{hs}	Heat sink temperature
T_{jm}	Mean junction temperature
T_{max}	Maximum operating temperature
t_{on}	Load pulse duration
V_{DD}	Applied drain voltage
V_{DS}	Drain-source voltage
V_{GG}	Applied gate voltage

V_{GS}	Gate-source voltage
V_{miller}	Miller plateau voltage
$V_{overshoot}$	Voltage overshoot
V_{pl}	Plateau voltage
V_{th}	Threshold voltage

Chapter 1

Introduction

The transportation sector is a significant contributor to greenhouse gas emissions, with vehicles being responsible for approximately 14% of global emissions [1]. Governments and industry worldwide are moving towards a greener, more sustainable future with the UK setting a target of net zero carbon emissions by 2050 and ending the sale of new petrol and diesel cars by 2030 [2]. Recent studies have also highlighted the damaging health damage effects of the transport industry, with pollution from petrol and diesel vehicles linked to an estimated 40,000 early deaths in the UK and a cost to the NHS and society in general of more than £6 billion annually [3]. The emergence of electric vehicles (EVs) and the move to low emission transport provides one solution to these complex problems.

The global electric passenger car stock between 2010 and 2020 is shown in Figure 1.1. After a decade of rapid growth, global electric car stock reached 10 million in 2020, with a 43% increase in sales from 2019, the majority made up of all-electric battery electric vehicles (BEVs). The increasing demand for EVs is driving significant advancements in technology, resulting in improved performance, driving range, and charging times. The average driving range of new BEVs has been steadily increasing. In 2020, the weighted average range for a new battery electric car was about 350 kilometres (km), up from 200 km in 2015 [4]. Consumer doubts still remain when it comes to range, reliability and performance, but with continued investment and innovation, EVs have the potential to revolutionise the transportation sector.

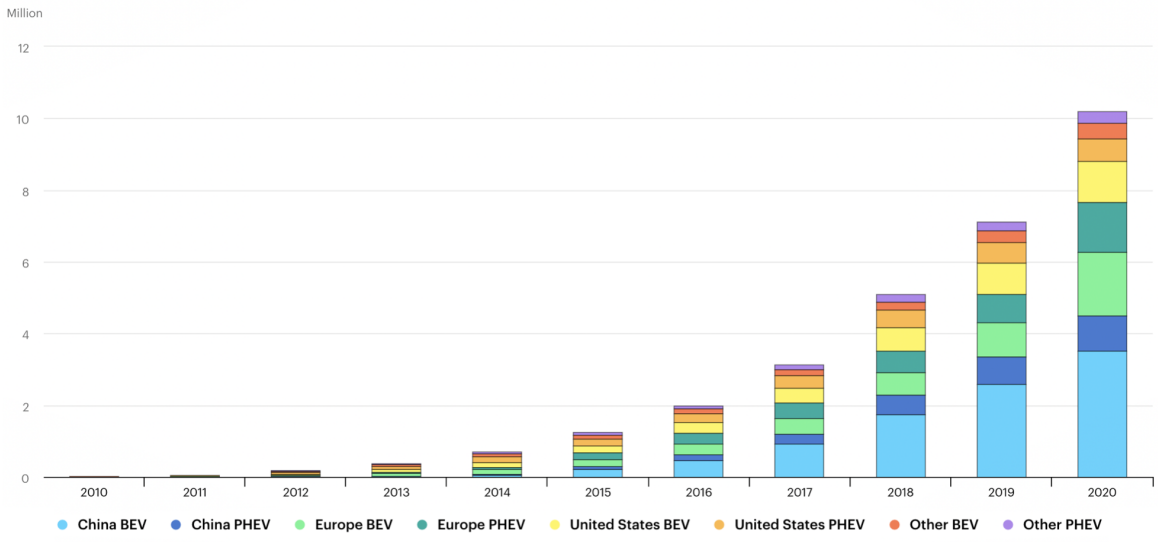


Fig. 1.1 Global electric passenger car stock, 2010-2020 [4]

1.1 Integrated Motor Drives

Power electronic (PE) converters in EVs determine a large part of the vehicle's efficiency and power output, with trends moving toward smaller, high-power-density components. Furthermore, the Department of Energy has set a power density target for automotive power electronics (PE) at 100 kW/L by 2025 due to the limited space in vehicles [5]. The integration of the power converter and electric machine results in a drive with high power density, low volume, and superior efficiency [6, 7]. This ultimately contributes to the development of lighter and more compact vehicles with extended range capabilities.

Current research has proposed a variety of techniques for the functional and structural integration of the PE converter with the machine, ranging from simple mounting of the converter on the machine housing to high levels of modular integration. Figure 1.2 shows some of the possible designs for IMDs used in automotive applications.

By combining the cooling and housing systems, both volume and weight are minimised. Additionally, in IMDs cabling connecting the power converter and machine can be eliminated, reducing electromagnetic interference (EMI) and making output filters redundant [8]. As a result, system reliability is enhanced, cost is reduced, and volume is further decreased.

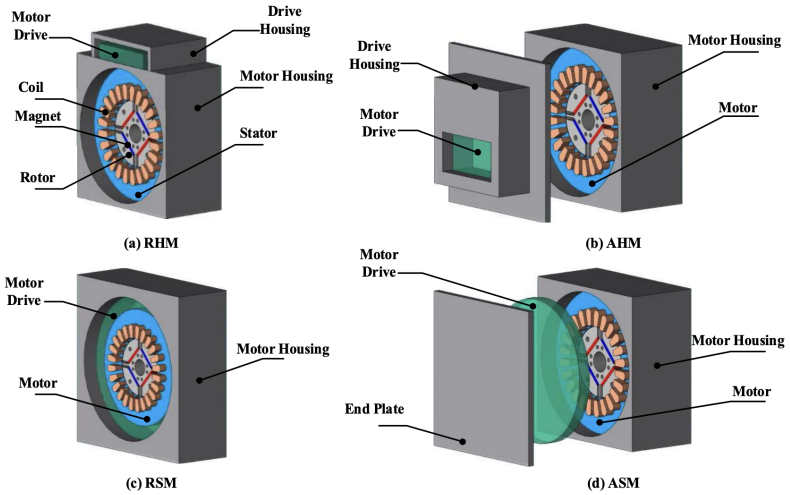


Fig. 1.2 Four categories of IMDs (a) Rotor Housing Mounted (RHM); (b) Axial Housing Mounted (AHM); (c) Radial Stator-iron Mounted (RSM); (d) Axial Stator-iron Mounted (ASM) [6]

Despite the attractive opportunities that IMDs present for EVs, there are still challenges to optimise their design and achieve widespread use, especially when considering the system PE. The thermal coupling of the motor and converter poses new challenges for the heat dissipation of the system. Without a careful approach to the system-level design of IMDs, a combination of thermal and mechanical problems can cause damage to the components of the converter, leading to low reliability and performance issues.

1.2 Application of Wide bandgap Semiconductors

Robust electronic components capable of withstanding the harsh environments required in IMDs have been a major focus of power electronic research and development in the last decade [9]. Wide bandgap (WBG) semiconductors such as GaN (gallium nitride) and SiC (silicon carbide) are regarded as the next-generation power semiconductor for automotive applications due to their superior properties such as high switching frequency, low switching loss, and better thermal capability [10, 11]. These properties translate into lower volume, high performance inverters capable of operating effectively in high temperature environment,

such as an IMD, and the efficiency benefits offered by SiC inverters can result in higher driving range or a lower requirement on the installed battery energy storage.

Discrete MOSFET packages and power modules are two common methods of packaging power SiC devices. Power modules can offer certain advantages in terms of convenience and until recently were far better suited to the high load currents in high power drives. However, discrete MOSFET packages are becoming more common due to recent developments, with discrete SiC MOSFETs available up to 225 A [12], alongside their greater design flexibility, thermal management, and more cost-effective nature.

1.3 Importance of Reliability

The power train is one of the most critical components in electric vehicles (EVs) because it controls the transmission of power from the battery to the wheels. The reliability of the system is defined in this work as the probability that it will perform its required function without failure, under stated conditions for a specified period of time. Any malfunction in the power train can cause reduced performance, safety hazards, and complete failure of the vehicle. Therefore, high reliability is essential to ensure that the vehicle functions consistently and without significant issues or failure. A reliable power train is important to ensure that the EV can provide a smooth, consistent and safe driving experience.

Moreover, the power train in EVs is a costly component, and repairs can be time-consuming and expensive [13]. Ensuring the reliability of the power train is critical to prevent unexpected downtime and repair costs, which can increase customer satisfaction and confidence in the technology. Reliability is of significant interest in IMDs for EVs because designs with high volumetric power density without consideration of the high temperature environment of the inverter can lead to highly unreliable systems with short lifetimes [14].

1.4 Research question and contribution

The key question this thesis aims to answer is:

- How can an integrated motor drive be designed so that it is optimal?

The definition of optimal is dependent on the chosen application for the IMD, however a key new factor in this work is the importance of the reliability of the system. Much of the work in this thesis is about the design process for IMDs, with examples applied to show the effectiveness of the developed methods and the potential for the improvements in this research area. Below are the key outcomes from the thesis.

1. Experimental investigation into SiC discrete family comparison enabling understanding of combined effects of MOSFET parameters and allowing validation of simulation models.

2. Development of novel SiC discrete device selection tool, including the capability for paralleling and temperature input. Applicable to a range of MOSFETs from different manufacturers.

3. Novel use of TO-247 package lifetime prediction data to carry out a multi-objective optimisation methodology for a three-phase IMD using combination of PLECS and Matlab-Simulink to demonstrate a system-level electrothermal simulation. This is then used to find optimal design solutions in terms of volumetric power density and reliability optimisation.

4. New lifetime calculation based on incremental damage theory suited for paralleled MOSFETs and fault tolerant inverter topologies.

5. Multi-objective of dual three-phase inverter and six-phase PMSM, using the novel reliability calculation and detailed computational fluid dynamics (CFD) analysis, allows comparison with the conventional three-phase IMD.

1.5 Thesis Structure

This thesis consists of six chapters. A brief description of each chapter is given below:

- **Chapter 1**: This chapter introduces the importance of EVs in the transition to a net-zero future, as the well as the potential improvement to health globally. Government policy and recent technological advances mean EV sales continue to grow, however further development and innovation is required to achieve the potential of EVs and increase their widespread use. Integrated motor drives that contain a wide bandgap transistor are identified as potential solutions to these challenges, but are a relatively immature technology that needs further investigation to provide an effective and reliable system for EVs.

- **Chapter 2**: This chapter includes a review of current integrated motor drives, their limitations and challenges. IMD inverter topologies, passive components and semiconductor transistor technologies are investigated with a focus on SiC discrete MOSFETs alongside relevant lifetime prediction methods and reliability analysis. Finally, methods for improving design through optimisation procedures, used throughout this thesis are discussed, particularly relating to IMDs for automotive traction applications.

- **Chapter 3**: This chapter focuses on the investigation of the electrical characteristics and device performance parameters of discrete SiC MOSFETs, with a particular reference to a 1200 V Infineon series. The knowledge gained and data presented is used to establish a device selection methodology for any application, but will be used in this thesis as part of the design of an integrated motor drive.

- **Chapter 4**: An electrothermal model of the entire power train is built in PLECS allowing component interactions and interdependencies to be investigated. Validated SiC MOSFET models were used in the simulation of a three-phase inverter, allowing system-level simulation under a range of operating conditions. An optimisation procedure to increase volumetric power density by reducing the size of the DC-link capacitor is presented and compared to analytical methods of individual component

sizing and design. A multi-objective optimisation allowed the lifetime, based on a recently developed lifetime model specific to transistors in a TO-247 package, to be considered as an objective function alongside the conflicting variable of inverter volume. A Pareto front identifies a range of possible solutions allowing a single optimal solution for the three-phase inverter to be selected, with its electrothermal performance and characteristics known.

- **Chapter 5**: A multi-phase integrated drive system is investigated and optimised using PLECS simulation, detailed thermal analysis and a novel lifetime prediction procedure in this chapter. These studies allow optimal parameter selection alongside other important design decisions such as control methods, including fault tolerant designs, as well as thermal management and physical layout considerations.

- **Chapter 6**: Finally, chapter 6 offers a summary of the work presented in this thesis and identifies areas for additional development if this work were to be taken forward in the future.

Chapter 2

Literature Review

2.1 Introduction

The ability to reduce volume, weight and increase efficiency of traction power trains is critical to the targets of increased range, performance and therefore popularity of electric vehicles (EV) and the move to a net zero future. The main scope of this project is to design an integrated motor drive (IMD) to meet these targets, while maintaining high reliability, which requires optimised component selection and application of new technologies. In the following chapter IMD are introduced and IMD specific power converters are examined. Wide bandgap semiconductors are discussed as a key enabling technology for development of IMDs with higher volumetric power density and increased reliability. Thermal management strategies for the inverters and machines in IMD systems are outlined before the reliability analysis of motor drives and the approaches to lifetime modelling for power semiconductor devices are presented.

Power converters in IMDs must be designed with consideration for the significant thermal, vibration, and electromagnetic challenges of close coupling with the machine. The use of different topologies and designs in IMDs is an area of further research, with current literature suggesting that the optimal topology choice is dependent on the IMDs application [15].

Aims to increase the power density, reliability, and efficiency of traction drives has prompted active research and development of smaller, more efficient, and reliable power

systems. In IMD systems optimised design is required to overcome the challenges associated with limited volume, high temperatures and high mechanical stresses for the power electronic devices and machine components. Advancements in passives and semiconductor device material and packaging have improved the performance of high-power IMDs, making them commercially feasible. Previously a limit of 7.5 kW was acknowledged for commercial IMDs [16] because in early research into IMDs design did not consider the system-level considerations and interconnected nature of the design problem. However, increases in power and power density are expected as WBG devices, improved component materials are fully incorporated, and research continues to grow in regard to optimal configurations, topologies, and thermal design [17].

This thesis comprises research containing all aspects of the power train for a motor drive. Analysis and modelling of the semiconductor power electronics, with a focus on discrete silicon carbide (SiC) devices can lay the foundations for accurate and detailed IMD study. Holistic power train simulation, design and optimisation with a focus on system reliability and power density is then investigated. A comprehensive review of the current research and literature regarding IMD analysis, design and improvement allows novel research opportunities to be identified.

2.2 Integrated Motor Drives

Integrated motor drives (IMDs) are a novel concept that has been proposed where all components of the motor drive system are integrated into the motor housing, including power electronics, control electronics, passive components, and heat sink [7]. By doing so, the volumetric power density of the system can be enhanced significantly which is central to improvements in aerospace and electric traction applications [18], [19]. However, the physical integration of the inverter with the machine presents technical challenges that require solutions. Research has proposed constructive solutions to some of these problems and ensure that IMDs are optimised for power density and adaptability using novel technologies

and processes [6]. Most of the literature and research exists as reviews of current IMD technologies [7] [20] and design improvements and analysis [21] [22].

2.2.1 IMD Topologies

Depending on the location of the power converter, IMDs are classified into four basic topologies: radially housing mounted (RHM), axially housing mounted (AHM), radially stator mounted (RSM) and axially stator mounted (ASM) [23]. These topologies will be presented and reviewed below.

Housing Mounted

In early IMDs the inverter was housed in a separate enclosure with a separate cooling structure, either on top of the machine housing in the RHM topology [24] or on the end plate in the axial direction in the AHM topology [25] [8].

Housing mounted topologies provide convenient integration without the need for complex design considerations [26]. However, this approach does not consider the entire system perspective, and, as a consequence, volume optimisation is limited. Figure 2.1 illustrates the mechanical construction of RHM and AHM integrated drives.

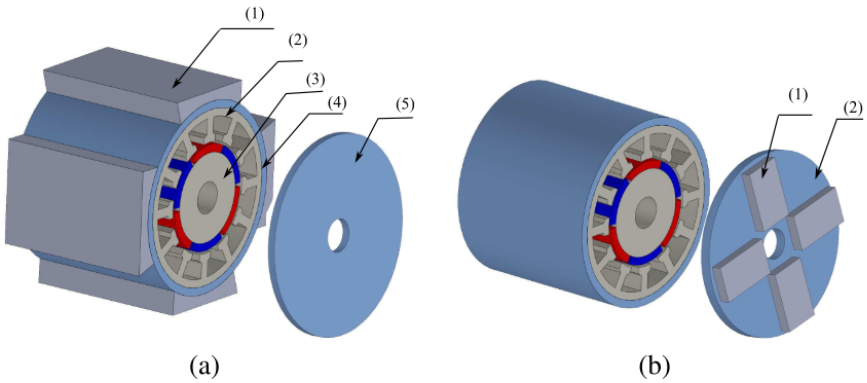


Fig. 2.1 Demonstration of housing mounted integration topologies (a) RHM: (1) power converter modules, (2) stator, (3) rotor, (4) housing, (5) end plate. (b) AHM: (1) power converter modules, (2) end plate [27]

Variations of housing mounted topology have been proposed with different levels of complexity, but all are generally attractive due to their simplicity, low cost, and ease of implementation [28]. In this topology, the housing provides thermal isolation between the converter and the machine, and by redesigning the housing to accommodate an active cooling system [24], it can also act as a heat sink for the inverter. The housing also improves mechanical stability and provides a mounting surface for the converter [18].

Many low-power housing mounted IMD configurations exist commercially, the majority being pumps, fans, and compressors [29, 16]. High power IMDs are becoming more popular, and with it the opportunity of traction applications, with the Siemens producing the SIVETEC series for EVs in the power range of 30-200 kW with power densities up to 2.6 W/kg [30]. Siemens operates at these power ratings through novel design of a water cooling system between the inverter and motor, leading to a 10-15% weight reduction due to removal of the inverter housing and connections[31].

Nidec has developed a 150 kW housing mounted IMD as the first fully integrated traction motor system . Through using SiC MOSFETs at high switching frequencies it could achieve a significantly reduced volume and weight of 68% and 31% compared to the conventional drive system [32]. UQM developed an AHM integrated electrical traction system for a permanent magnetic motor with a maximum power of 75 kW [33] where both the machine and the inverter are liquid-cooled. The examples provided illustrate the diversity of power ratings and capabilities, and potential of IMDs and show the limitations are mostly dependent on their current suitability to specific applications.

Stator mounted

The stator mounted topologies provide more compact integration compared to the housing mounted topologies, but this approach can make design more challenging. Coordination of the systems electrical and thermal design is required because of the heat generation and electromagnetic issues in close integration of IMDs [34]. Figure 2.2 illustrates the mechanical construction of RSM and ASM integrated drives.

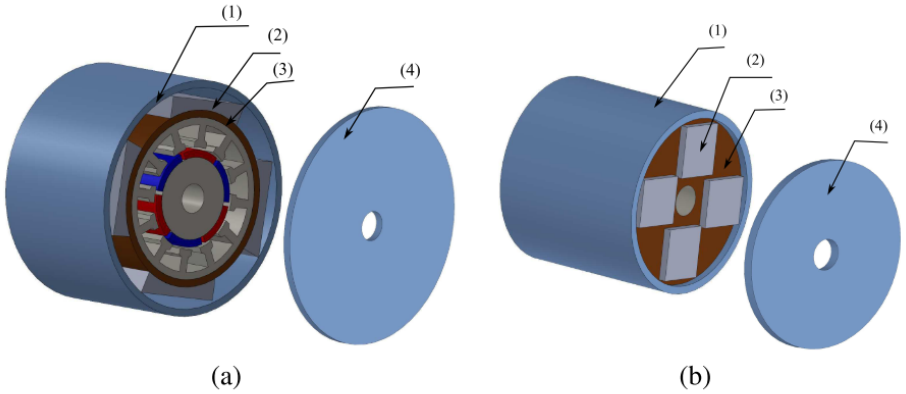


Fig. 2.2 Demonstration of stator mounted integration topologies (a) RSM: (1) housing, (2) power converter modules, (3) shared cooling structure, (4) end plate. (b) ASM: (1) housing, (2) power converter modules, (3) shared cooling structure, (4) end plate [27]

The objective of the RSM and ASM configurations is to produce an IMD with an improved volumetric power density, however this often comes at the cost of reduced reliability and efficiency. Modular power converters can be utilised and with individual modules connected in series supplying independent machine windings [8].

The 83 kW Protean electric wheel [35, 36] is among a small number of stator mounted IMDs available commercially. Designing a converter capable of withstanding the high temperatures and high vibrations within the machine enclosure is even more challenging compared to housing mounted IMDs. A liquid cooling system is developed in [36] to cool the converter and machine windings simultaneously with a axial and orthogonal paths to improve heat dissipation.

Integrated Modular Motor Drives

Modular integration involves segmenting the power electronics into smaller modules that control dedicated stator winding sections. These modules are physically independent of each other and are usually electrically connected together in series or parallel for the purpose of control. Advantages of modular systems include fault tolerance, better thermal capabilities, power rating scalability and a possible reduction in the overall size and cost of the PE.

Drive modularisation is independent of converter position as mounting can occur on the motor housing [37] on the stator iron [17, 38], or on the end plate [39]. Fault tolerance is one obvious advantage as multiple modules exist which form a unit as opposed to a centralised power electronics module and so the system can be designed to allow for individual module failure. Current and voltage loading stress is also reduced in the power electronics (PE) as lower rated components are used in the modules to form a much larger rated unit [40].

Improved thermal capability is another advantage. This is as a result of having individual lower rated components and more evenly distributed heat dissipation [7]. Due to these potential benefits, modular drives are very beneficial for IMD design. In [17], both machine and drive are modularised (one converter phase leg per machine pole) resulting in better thermal performance due to lower rated devices, increase in machine lifespan as a result of low voltage change in the slot insulation layer, lower maintenance cost and fault tolerance. The possible drawbacks are the necessity for a complex control system for the individual power modules and the difficulty of mechanically and structurally integrating the modules with the motor [20].

To further increase the level of integration between the EM and inverter, the concept of an integrated modular motor drive (IMMD) has been proposed [8]. The modularisation of the machine into concentrated winding pole pieces each with integrated drive electronics allows a further reduction in the total drive volume and enables simultaneous optimisation of the machine and inverter characteristics. Lenze offer modular low to mid-range IMDs with power ratings ranging from 0.4-7.5 kW [41]. Commercial high power modular IMDs with ratings up to 16.5 MW are currently manufactured by Siemens under the integrated drive systems range [42].

A prototype nine-phase drivetrain including a PM machine, gearbox and integrated inverter has been developed to demonstrate the concept [43]. The integrated inverter is reported to achieve a power density of 35 kW/litre with the entire system capable of a peak mechanical output power of 60 kW [44].

2.2.2 Thermal Management

The complex thermal coupling between the motor and inverter in IMDs can lead to high temperatures in the motor and inverter system, reducing the performance and lifetime of the switching devices and DC-link capacitors. Extensive thermal analysis is required to maximise the potential of IMDs, including evaluation of the converter and machine individually and combined.

Thermal Analysis

Accurate IMD thermal models has become important as the basis for research and thermal analysis of IMDs, the research system is shown in Figure 2.3. Thermal resistance networks (TRNs) and numerical analysis are the main methods of thermal analysis for power electronics and drives. TRNs rapidly analyse conduction, convection, and thermal radiation resistance for each part of the system. Numerical analysis, consisting of finite element analysis (FEA) and computational fluid dynamics (CFD), is more accurate but more complex, requiring more design information from the inverter system such as detailed dimensions and fluid flow paths in many cases [45].

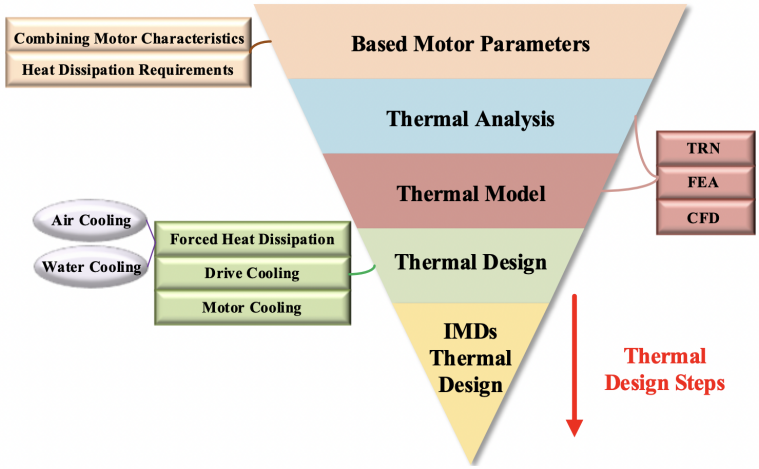


Fig. 2.3 IMDs integrated thermal design system [6]

Cooling Systems

Modern IMDs use a combination of active and passive cooling systems due to the extreme thermal demands on the system [46]. Passive cooling system utilises heat dissipation through natural convection, thermal mass, ventilation and thermal isolation. In active cooling system the base plate of the converter or motor can be cooled through forced convection. Generally, liquid cooling provides good heat transfer [47] however it can increase the volume of the system due to the complex heat sink and equipment used for coolant circulation. Forced air cooling increases design flexibility and has low maintenance costs but is less effective than liquid cooling [48]. Thermal coupling between semiconductors and heat sink and cooling mechanisms of passive components impacts the power density significantly. The European Center for Power Electronics (ECPE) has introduced a cooling system performance index to compare power density when using different heat sink designs and demonstrated two water cooled power electronics systems including a 75 kW/l IMD [49].

2.3 IMD Converter Topologies

Power converters in IMDs must be designed with consideration for the significant thermal, vibration, and electromagnetic challenges of close coupling with the machine. This section introduces the main converter configurations and topologies that have been analysed extensively in literature [15]. The use of different topologies and designs in IMDs requires more research and the optimal topology choice is dependent on the IMDs application. The main topologies analysed that are relevant to IMDs are:

- Two-level full bridge converter
- Three-level converters
- Multi-phase converters

Two-level full bridge converter

The most common converter used in traction system is the two-level full bridge due to its simplicity and flexible control. However, when compared to multi-level topologies it has relatively high current total harmonic distortion (THD), when operated in pulse width modulation (PWM) [50].

Three-level converters

Multi-level inverters can produce output voltage waveforms with lower harmonics [51], lower $\frac{dV}{dt}$ and electromagnetic interference (EMI) emissions. Three-level neutral-point and T-type neutral-point converter (NPC) are the most commonly used multi-level inverter topologies [52].

For lower power and low-voltage applications, the NPC suffers from higher conduction loss due to the series connection of two devices in the conduction paths. By contrast, T-type topology has less number of devices in the conduction path, which notably decreases the conduction loss. However, the switching losses in the T-type topology may be higher than that of the NPC due to higher voltage stress over a single-switch position and devices with higher voltage ratings are needed. These issues can be potentially addressed by emerging WBG devices.

Multi-phase converters

Multi-phase can deliver high-power, due to improved per-phase current handling [53], offer improved fault tolerance capability, lower torque pulsations, better noise characteristics, and modularity [54]. Multi-phase converters require more components and complex control, however lower per-phase current can result in easier structural integration into the machine, and more spatially distributed converter losses.

2.4 Semiconductor Power Devices

The growing demand for converters with improved volumetric power density, high efficiency and potential to operate in high temperature environments has led to research on wide bandgap (WBG) semiconductor devices [11]. The majority of research into WBG semiconductors focuses on Silicon Carbide (SiC) and Gallium Nitride (GaN), for which commercial devices are now widely available. IMD design could benefit from the ability of WBG semiconductor devices to operate at high blocking voltages, high temperatures, and high switching frequencies, resulting in a smaller system size while maintaining high efficiency and reliability.

2.4.1 Overview of WBG materials

The material properties of SiC and GaN are compared with those of Silicon in Table 2.1 [39]. To allow the comparison of semiconductor materials in power devices, Huang [55], devised figures of merit (FOM) for unipolar devices based on theoretical switching performance, power density and thermal capability. Only 4H-SiC is considered here for SiC, because of its dominance commercially.

Table 2.1 Properties and FOM for Si, SiC and GaN [39]

	Si	4H-SiC	GaN
Bandgap, E_G (eV)	1.1	3.2	3.4
Relative dielectric constant, ε_r	11.7	9.7	9.0
Electric breakdown field, E_C (kV/cm)	300	3500	3300
Electron mobility, μ_n (cm^2/Vs)	1400	650	990
Thermal conductivity, λ (W/cm K)	130	430	130
Sat. electron drift velocity, v_{sat} (x10^3 m/s)	100	300	250
Max. operating temperature, T_{max} (°C)	300	870	500
HMFOM (switching performance) = $E_C\sqrt{\mu}$	1	7.9	9.3
HCAFOM (power density) = $\varepsilon E_C^2\sqrt{\mu}$	1	77	78
HMFOM (thermal capability) = $\frac{\lambda}{\varepsilon E_C}$	1	0.3	0.1

The most significant improvements of WBG semiconductor devices over Si is because of the materials higher critical breakdown field (E_C). This enables smaller drift regions in

both SiC and GaN devices for a given blocking voltage, reducing the on-state resistance and therefore conduction losses, which occur when the device is on [11]. Therefore, higher blocking voltages are feasible and WBG devices can be smaller for a given current rating, reducing parasitic capacitances which reduces switching losses [10], allowing operation at higher switching frequencies. The high electron saturated velocity of the WBG devices also improves operation at high switching frequency, due to faster switching speeds. The capability to operate at high switching frequency results in small passive filters and DC-link capacitors [56] which further increases the power density of the IMD.

Larger bandgap increases the maximum operational temperature as the temperature limit is reached when the number of intrinsic carriers approaches the number of extrinsic carriers [56]. SiC also has the highest thermal conductivity which determines how a material conducts heat to its surroundings which is advantageous in IMDs [11]. SiC power devices exist with operating temperatures up to 200°C [57] however uncertainties exist over their reliability at these temperatures due to the expected performance of the device packaging.

2.4.2 SiC Power MOSFETs

SiC MOSFETs have been commercially available since 2011 and are currently available with ratings up to 4400 V and 1900 A for specific applications [12]. Lower gate charge and smaller parasitic capacitances enable faster switching compared to other device types. Low on-state resistance and high voltage rating due to the benefits of SiC allows an increase in power density of converters when using SiC MOSFETs. SiC MOSFETs are normally-off (enhancement-mode) devices, so will fail safely in a power converter. The two most common power MOSFET structures, the planar MOSFET (D-MOSFET) and the trench MOSFET (U-MOSFET) are shown in Figure 2.4.

The trench MOSFET is considered the ideal structure for taking advantage of SiC. The design has no JFET resistance, high mobility and easy miniaturisation [59]. However, until the design was edited to create the double trench structure in 2015, the oxide film was easily damaged at high voltages, limiting its commercial use.

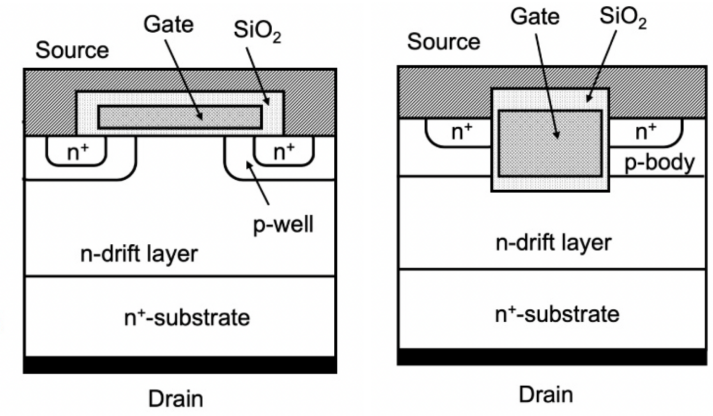


Fig. 2.4 Cross section of simplified n-channel power MOSFETs (a) Planar (b) Trench [58]

Figure 2.5 shows the parasitic capacitances between the devices three terminals, the gate-to-source, C_{GS}, gate-to-drain, C_{GD}, and drain-to-source, C_{DS}.

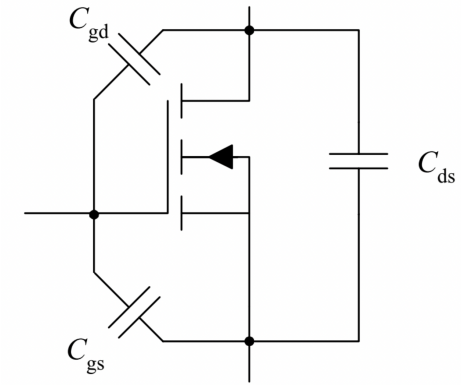


Fig. 2.5 Electrical equivalent circuit of MOSFET with parasitic capacitances [60]

The values of these capacitances are nonlinear and a function of device structure, geometry, and bias voltages. The parameters are important when considering MOSFET switching and during turn-on. Capacitances C_{GD} and C_{GS} must be charged through the gate, hence, the design of the gate control circuit must take into consideration the variation in these capacitances. The largest variation occurs in the gate-to-drain capacitance as the drain-to-gate voltage varies. The MOSFET parasitic capacitance is given in terms of the device data sheet

parameters C_{iss}, C_{oss}, and C_{rss} as follows:

$$C_{DS} = C_{oss} - C_{rss} \tag{2.1}$$

$$C_{GS} = C_{iss} - C_{rss} \tag{2.2}$$

$$C_{GD} = C_{rss} \tag{2.3}$$

where C_{rss} is the small-signal reverse transfer capacitance; C_{iss} is the input capacitance with the drain and source terminals shorted; and C_{oss} is the small-signal output capacitance with the gate and source terminals shorted.

Transconductance, g_m, is another important parameter found in the datasheet. It is a measure of the sensitivity of drain current to changes in gate-source bias and decreases with temperature due to a reduction in carrier mobility. It is usually measured at saturation region with fixed V_{DS} and is found using equation 2.4.

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{\mu_s . C_{ox} W}{L_{CH}} \tag{2.4}$$

where ΔI_{DS} is the change in drain-source current, ΔV_{GS} is the change in gate-source voltage, W is gate width, L_{CH} is channel length, μ is mobility, and C_{ox} is gate capacitance of the devices.

MOSFET Regions of Operation

The characteristic curves in Figure 2.6 show the three regions of operation for SiC MOSFETs:

- Triode region: when the channel is continuous with no pinch-off, so the drain current is proportional to the resistance of the channel
- Saturation region: the channel pinches off, resulting in constant drain current
- Cut-off region: off-state

For enhancement mode MOSFETs, when a gate-source voltage, V_{GS} greater than the threshold voltage, V_{th} is applied, a conducting channel is created between the drain and

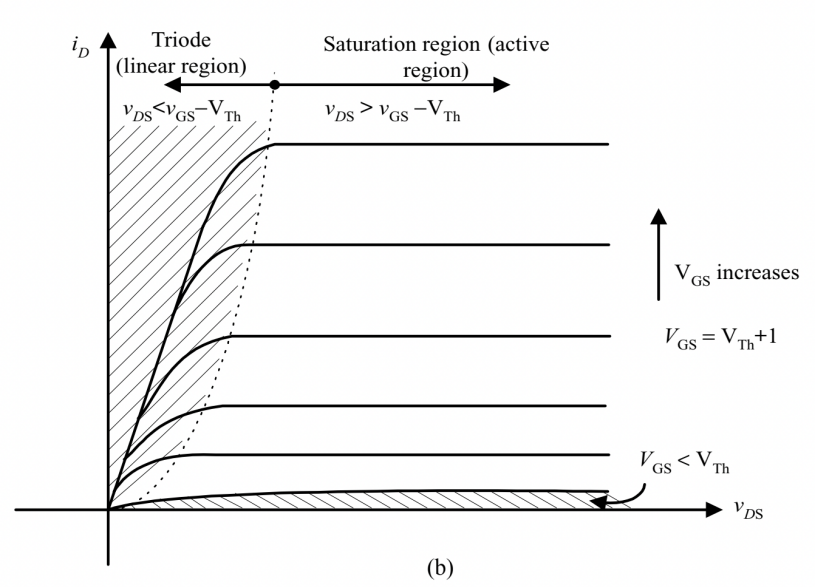


Fig. 2.6 Typical output characteristic of basic n-channel SiC MOSFET [60]

source that allows the load current to flow through the device. For an applied gate voltage, where $V_{GS} > V_{th}$, the device will operate in either the triode region or the saturation region, depending on the value of the drain-source voltage, V_{DS}, applied to the MOSFET. For given V_{GS}, if $V_{DS} < V_{GS} - V_{th}$, the device operates in the triode region, and for larger V_{DS}, the device operates in the the saturation region.

When $V_{GS} < V_{th}$, there is no channel induced and device operates in the cut-off region (off-state) where the drain current is equal to almost zero. SiC MOSFETs can support a high V_{DS} across the junction in the off-state, however exceeding the rated voltage can lead to avalanche breakdown and device damage.

MOSFET Switching Characteristics

Many papers focus on dynamic modelling, analysis and predicting switching behaviour of transistors with the majority of recent work focusing on SiC MOSFETs. Comparative studies exist between SiC and Si MOSFETs and IGBTs [61], but these often do not refer the difference between the datasheet parameters and focus on fundamental properties of the materials and technologies to explain differences in switching characteristics [62]. Papers that compare SiC MOSFETs from different manufacturers to each other include the impact of

capacitance, inductance and resistance to describe the difference in losses, but do not directly analyse the impacts of specific parameters from the datasheet, for example what effect the value of input capacitance has on switching energy losses [63]. The switching waveforms have been studied and many analytical models have been created using equations that explain the behaviour of MOSFETs based on circuit and device parameters [64]. Although these are often not supported experimentally they provide an understanding of turn-on and turn-off and detail of the processes involved.

Turn-on: The turn-on waveforms for the power MOSFET are shown in Figure 2.7, where at time t=0 voltage V_{GG} is applied to the gate where V_{GG} is greater than the device threshold voltage, V_{th}. During the first interval, turn-on delay time, $t_{d(on)}$, V_{GS} will rise from zero to V_{th}. This delay is due to the charging of C_{GS} and C_{GD} by the current flowing through the gate resistor R_G.

V_{GS} rises as V_{GG} charges the input capacitance of the MOSFET:

$$\upsilon_{GS} = V_{GG}(1 - e^{(t-t_0)/\tau}) \tag{2.5}$$

where the time constant is defined as

$$\tau = R_G(C_{GD} + C_{GD}) \tag{2.6}$$

In the next interval the device starts conducting as $\upsilon_{GS} > V_{th}$ and channel begins to form between the drain and source. Drain current, i_D starts flowing exponentially from zero, with the rate limited by the transconductance, g_m:

$$i_D(t) = g_m(\upsilon_{GS} - V_{th}) \tag{2.7}$$

where υ_{GS} still follows equation 2.5 so i_D is also dependent on the input capacitance.

The gate current continues to decrease exponentially and V_{DS} stays constant until I_D reaches its maximum value of I_0 at t_2. For $t > t_2$ the diode turns off and i_D is assumed to

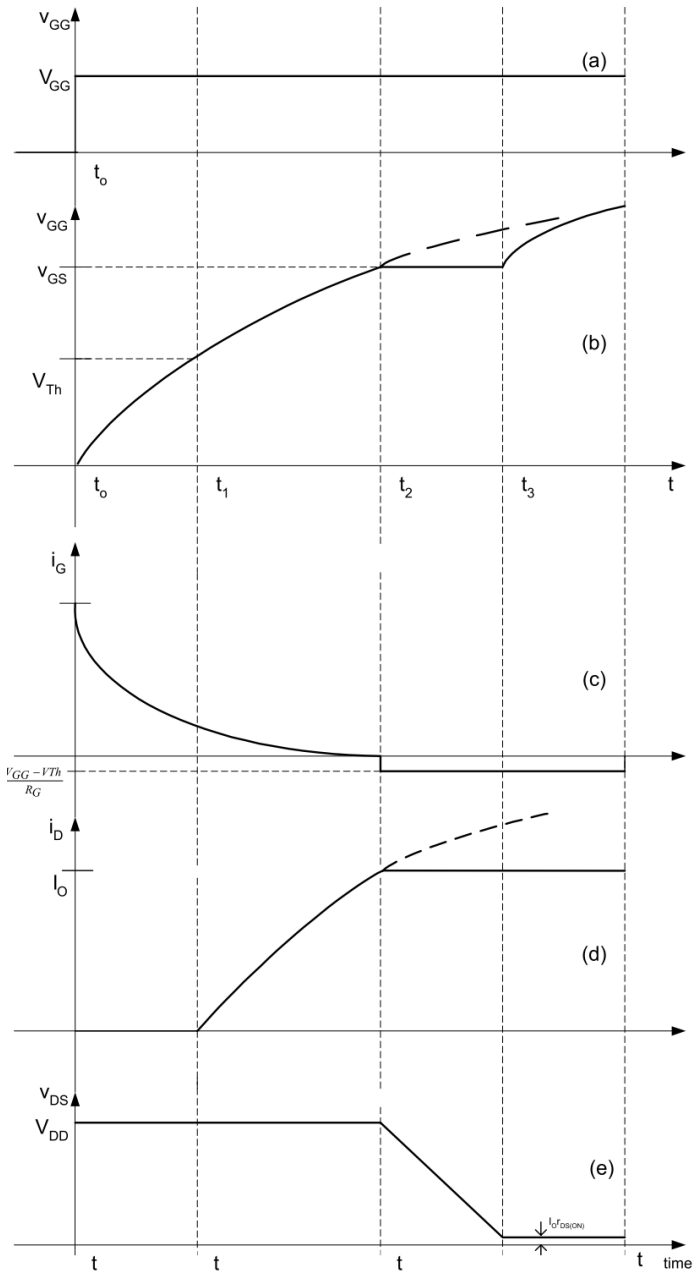


Fig. 2.7 Turn-on waveforms of a MOSFET with an inductive load [60]

equal I_0. According to the input characteristics of the MOSFET in this region, as the i_D is constant, so is υ_{GS}.

For the time between t_2 and t_3 the diode turns off the load current I_0 and the drain current starts discharging the drain-source capacitance, C_{DS}. As υ_{GS} is constant the gate current flows through C_{GD} and $\upsilon_{DS}(t)$ in this time period can be solved:

$$\upsilon_{DS}(t) = -\frac{V_{GG} - V_{th}}{R_G C_{GD}}(t - t_2) + V_{DD} \tag{2.8}$$

After t_3 the gate current continues to charge C_{GD} and as υ_{DS} is constant, υ_{GS} starts charging at the same rate as in the first interval. When it reaches V_{GG} the gate current is zero, C_{GS} and C_{GD} are fully charged and the device is fully on.

Turn-off: A typical turn-off waveform is shown in Figure 2.8 and involves the same steps as during turn-on, but in a reverse sequence. At time zero the device is turned off by applying 0 V to the gate. If the device permits, negative voltage can also be applied to turn-off the device, as this will give a higher gate current and will speed up the turn-off transient. Also, different values for R_G can be used for turn-on and turn-off in order to speed up or slow down the device, depending on the application requirements.

In both turn-off and turn-on, between t_1 and t_2 and between t_2 and t_3 the MOSFET sustains high voltage and current simultaneously leading to high switching losses in these periods. Therefore the losses are dependent on the times set by the equations above and to reduce the MOSFET switching times, smaller input capacitance is required. For more detailed switching analysis of MOSFET switching, see the reference by Baliga [65].

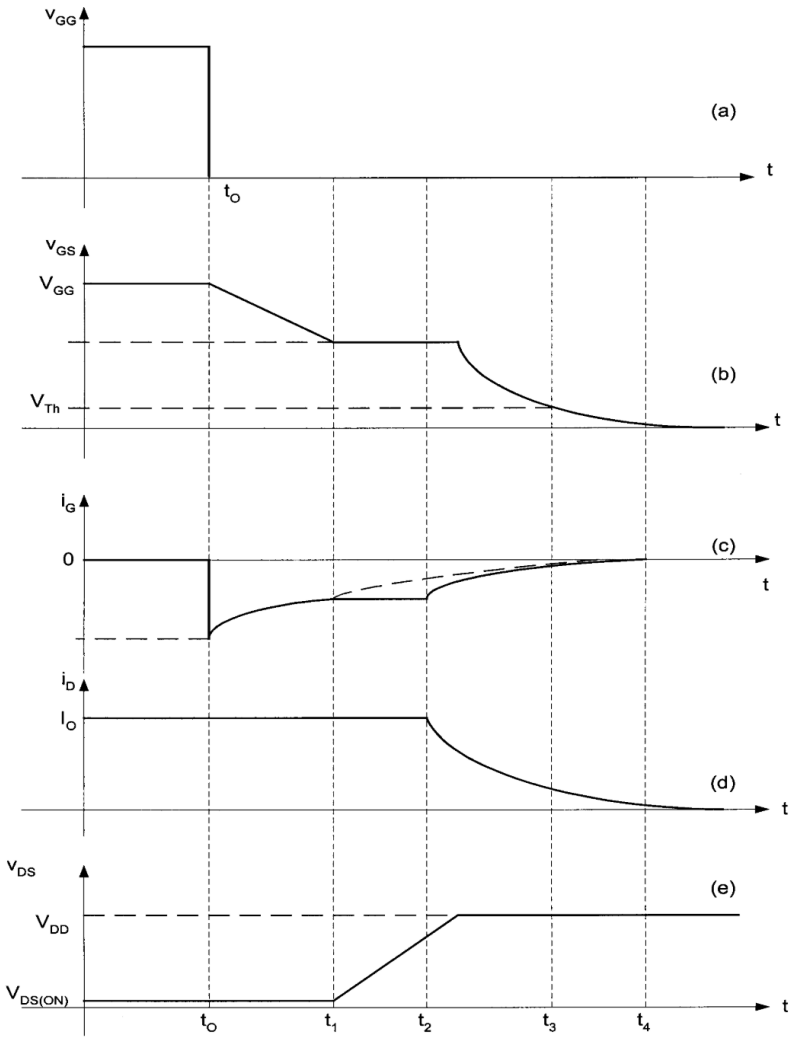


Fig. 2.8 Turn-off waveforms of a MOSFET with an inductive load [60]

Gate Charge Analysis

Behaviour during the switching transient is strongly influenced by the capacitances present in the structure of the device. The gate current during the switching has the typical behaviour of the current in an RC circuit. In order to better understand the phenomena that occur during switching, and view the switching from a different perspective to the previously described descriptions, it is possible to refer to the gate charge curve in Figure 2.9.

During operation, before the gate current is turned on, the DUT withstands all the supply voltage, V_{DD}, while the voltage V_{GS} and the drain current are zero. Once the gate current

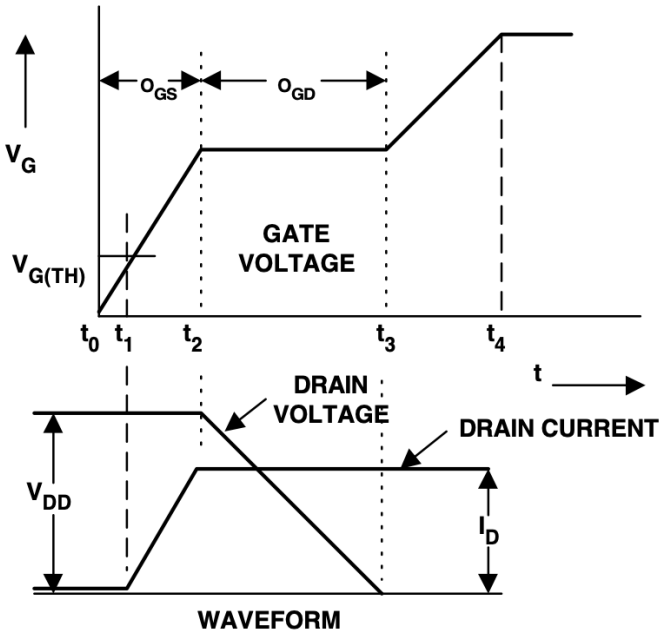


Fig. 2.9 Simple turn-on waveform of MOSFET with gate voltage curve and gate charge presented [12]

I_g flows at t_0, C_{GD} and C_{GD} start to charge and the V_{GS} increases. The rate of charging is given by I_G/C_{iss}. Once the voltage V_{GS} reaches the threshold voltage of the power MOSFET, drain current starts to flow at t_1. The gate voltage continues to rise to the plateau voltage, V_{pl}, which is equal to V_{th}+I_d/g_m, while the voltage across the DUT remains equal to V_{DD}. The charge needed to reach this state at t_2 is Q_{GS} as given by equation 2.9.

$$Q_{GS} = \int_{V_{DD}-V_{pl}}^{V_{DD}} C_{iss}(V_{DS}).dV \tag{2.9}$$

At time t_2, C_{GD} is completely charged and the drain current reaches the predetermined current I_d and stays constant while the drain voltage starts to fall. At t_2, C_{GD} is fully charged so V_{GS} remains constant at V_{pl}. The gate current is used to charge the C_{GD} capacitance until t_3, where I_g= $C_{GD}.\frac{dV_{DS}}{dt}$. Charge time for the Miller capacitance, C_{GD}, is larger than that for the gate to source capacitance C_{GS} due to the rapidly changing drain voltage between t_2 and t_3. The plateau phase ends when V_{DS} reaches its on-state value. The gate charge injected

during this plateau phase is Q_{GD} and is often used to estimate voltage transition times and switching loss.

$$Q_{GD} = \int_0^{V_{DD}-V_{pl}} C_{rss}(V_{DS}).dV + \int_{V_{pl}}^{0} C_{rss}(V_{GS}).dV \tag{2.10}$$

The gate charge (Q_{GS} + Q_{GD}) corresponding to time t_3 is the bare minimum charge required to switch the device on.

Once C_{GD} and C_{GD} are fully charged, the device gate continues charging until V_{GS} reaches its supply voltage at t_4, and the drain-to-source voltage becomes equal to $R_{DS(on)}.I_d$. The gate-source voltage is free to rise with a slope controlled by the gate charging current and the C_{iss}, which is higher at V_{GS}>V_{th} leading to a lower slope in the gate charge curve, until the gate-source voltage reaches its maximum value.

$$Q_c = \int_{V_{pl}}^{V_{DD}} C_{iss}(V_{GS}).dV \tag{2.11}$$

where Q_c is the remaining charge needed to fully charge C_{iss} after t_3. The total gate charge, Q_G, is the total of these three components of gate charge. Datasheets quote values for gate charge and supply a figure for gate charge against V_{GS}. This has been used in some cases to predict the behaviour of the device [66, 67].

2.4.3 Power Electronic Packaging

The packaging of SiC MOSFETs greatly influences the thermal performance, reliability and power density of power electronics systems. In IMDs the MOSFETs need to be well protected against external environmental factors such as high temperature, vibration, humidity and dust.

The TO-247 discrete package is the state-of-the-art packaging choice for single SiC MOSFET chips, the structure is shown in Figure 2.10. The SiC chips are covered with epoxy resin moulding compound that mechanically fixes the chip in place while protecting from moisture and electrically insulating the semiconductor. The chips are soldered on a copper layer which serves as load current terminal and base-plate. It comes in both three and four leg versions which have proven high ruggedness and reliability [68].

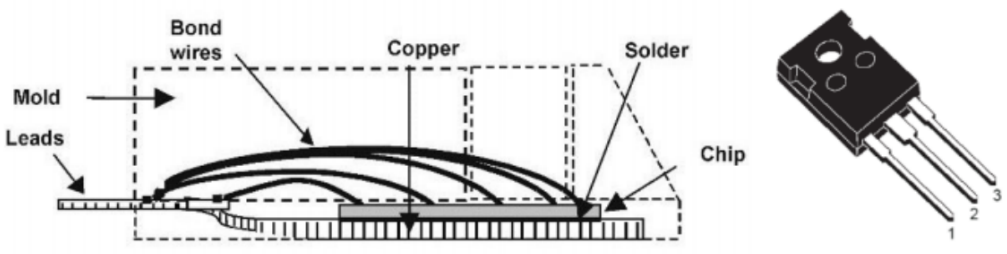


Fig. 2.10 Classic structure of TO-247 package [11]

With the increased application of discrete devices in fast switching applications, the effect of the parasitic elements in the packaging is becoming increasingly important [69, 70]as it can lead to failure due to current or voltage spikes. This thesis will focus on the design opportunities for medium and high power IMDs that improvements in SiC discrete devices in packages such as the TO-247 can offer over use of traditional power modules.

MOSFET failure mechanisms

The failure modes of semiconductor devices can be characterised into two groups, chip-related and package-related. An extensive summary of these failure modes has been outlined in [68]. Chip-related failures are those that destroy the device, whilst package-related failures affect the fatigue experienced by the device. As fatigue leads to eventual device failure, the two failure mode groups are not always mutually exclusive [68].

Research has identified the chip bond-wire connections and die-attaching solder layer as the weak points in the TO-247 package [71]. Thermal expansion during operation causes stresses between the chip, wires and baseplate due to the different coefficients of thermal expansion (CTE) of the materials. More detail on how this information can be used in IMD analysis and lifetime prediction is covered later in this chapter.

2.4.4 Modelling SiC Devices

There are three main approaches when analysing SiC devices: analytical models, simulation models, and experimental investigations. Determining the accuracy, speed and effectiveness of methods of analysis is important for studying device characteristics and allowing

comparisons. This thesis studies each to enable all three methods to be applied in different ways.

The objective of MOSFET modelling is to obtain a description of the on-state characteristics and switching behaviour as a function of the applied voltage, current, temperature and intrinsic physical characteristics. SiC MOSFET models are particularly helpful as a way of expanding the scope of experimental work by enabling the interpolation of data points, or by allowing estimation of parameters that are inaccessible with test equipment.

Simple analytical models give fast results but lack detail and therefore have limited accuracy. However, as they are based on fundamental theory and use real device and circuit characteristics as variables, they can be used to study changes in specific parameters to further understanding of MOSFET behaviour.

In contrast, complex physics-based model provides accurate estimation of the device behaviour but also have higher computational requirements. Detailed physics based models of MOSFET non-linear behaviours have been developed [72]. In [73] a simple and generic physics-based model is presented that improves on the speed of the previous literature while still showing excellent prediction of dynamic behaviour. LTSpice is an program for simulating transient response of electrical circuit components, and includes the capacity to produce and test complex SiC MOSFET models [74]. Behavioural models have often been considered a good compromise between accuracy and computational complexity [75], and a suitable behavioural model for WBG devices is explored in [76].

Experimental studies are the most expensive in terms of time and cost so are often not chosen for concept stage design of power systems but are required to determine accuracy of any modelling techniques. Once validated experimentally, it is possible to use models for both SiC MOSFET behaviour investigations and within circuit analysis.

2.5 Passive Components

In IMD converters, the primary function of DC-link capacitors is to attenuate current ripple and suppress transient over-voltages caused by excessive inverter switching and power-

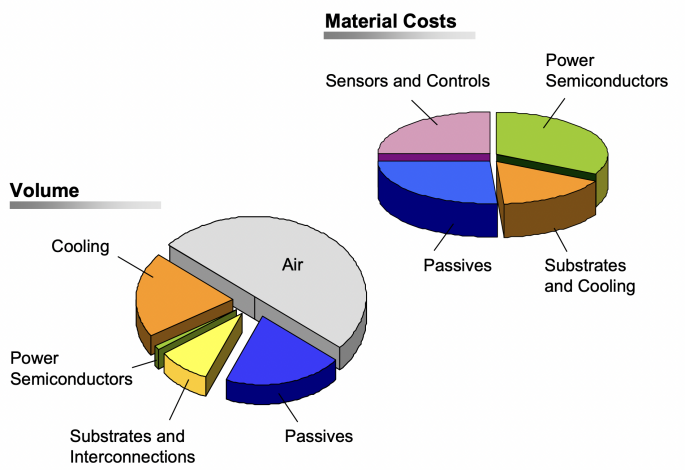


Fig. 2.11 Typical material cost and volume distribution in power electronics system [20]

loop inductor interactions [77]. Despite the positive implications of DC-link capacitance on converter performance, IMDs systems face the problem of DC-link capacitor size and height. Reducing the size of the driver is very important to increase the power density of the integrated motor.

Figure 2.11 illustrates the material costs and volume of passive components compared with other components in an inverter. The data in the figure shows that passives, in particular the DC-link capacitors typically account for 20% of the cost and 30% of the driver's volume [20]. This limits the power density of the system and as a result, minimising the DC-link volume has become a focus of current research.

Currently the three main capacitor technologies used in traction inverters are:

- Ceramic capacitors
- Electrolytic capacitors
- Film capacitors

Ceramic Capacitors

Ceramic capacitors are used mostly for high temperature and high voltage applications [78], with capacitors available that can withstand temperatures up to 250 °C [79]. However, in

IMD traction applications where shock and vibration is prominent, reliability issues arise over the mechanical stability of ceramic capacitors due to the brittle nature of ceramic capacitors [80]. In addition, they have a low energy density and therefore, several components have to be paralleled to achieve the necessary ratings required in high power systems, increasing the overall cost of the IMD system.

Electrolytic Capacitors

The high energy density and wide availability of electrolytic capacitors make them the most common choice for DC-link capacitors in conventional motor drives. However, their limited current handling capabilities and short lifetime due to thermal degradation [81] restricts their use in IMDs. They also have relatively high equivalent series resistance and equivalent series inductance, leading to problems in converters with high switching frequencies.

Film Capacitors

Polymer film capacitors offer the benefits of both low losses and mechanical durability, while also providing a high capacitance in a compact size. Commercially available film capacitors operate at temperatures up to 170 °C [82] and exhibit higher lifetime and higher ripple current capability compared with electrolytic capacitors [83]. Therefore, film capacitors offer a realistic capacitor choice in IMDs due to smaller size and longer lifetime compared with electrolytic capacitors and good mechanical robustness and high energy storage density compared with ceramic capacitors. The majority of recent IMD design studies use film capacitors for these reasons [84, 21]

2.6 Reliability Analysis of Power Converters

Studies analysing the failures of power converter components in industry are summarised in Figure 2.12. These surveys investigated the failures of 200 products from 80 companies to identify which converter components the industry consider to be the most prone to failure [85, 86]. Both surveys identify semiconductor devices and capacitors as the main cause of

failure in power converters. It can be assumed that IMDs will follow the same trends, with the extreme conditions in IMDs only increasing the need for accurate reliability analysis.

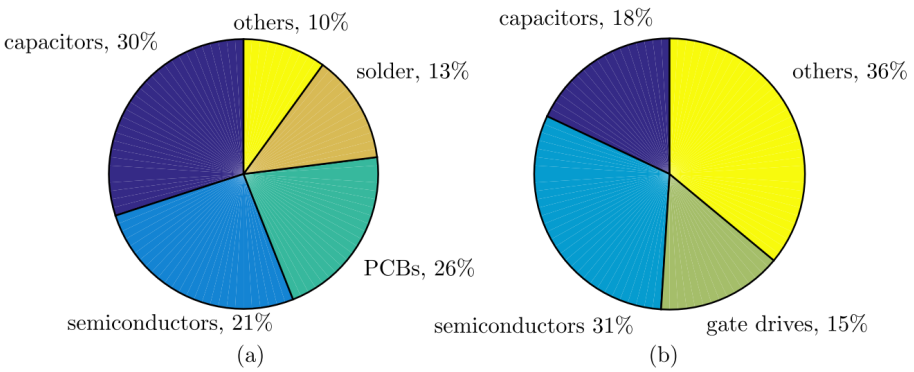


Fig. 2.12 Results of surveys on failures within power converter devices (a) [85], (b) [86]

2.6.1 Reliability Analysis

The engineering definition of reliability is the probability that an item will perform a required function without failure under stated conditions for a specified period of time [87]. A comprehensive reliability description includes five aspects: definition of failure criteria, stress condition, reliability numbers (%), confidence level (%), and the time of interest [88]. In this work, lifetime under specified stress conditions and failure conditions is considered a good measure of system reliability.

Accurate lifetime estimation of the MOSFETs and capacitors in an IMD allows the design of reliable and robust systems that can withstand the expected lifetime of the application. Understanding potential failure mechanisms is required for lifetime prediction and can be used to anticipate failure modes and design around them [14]. In this section procedures for modelling the reliability of power converters and the current research into lifetime prediction methods of power semiconductor devices is introduced.

The bathtub curve, shown in Figure 2.13, can be used to represent the failure of the components in a inverter over time [89]. Early failures caused by flaws in some components due to problems in the design or manufacturing lead to high failure rate at the start of operation. This failure rate can be low for mature designs and screening that removes any

defective components prone to early failure is common for applications that require high reliability.

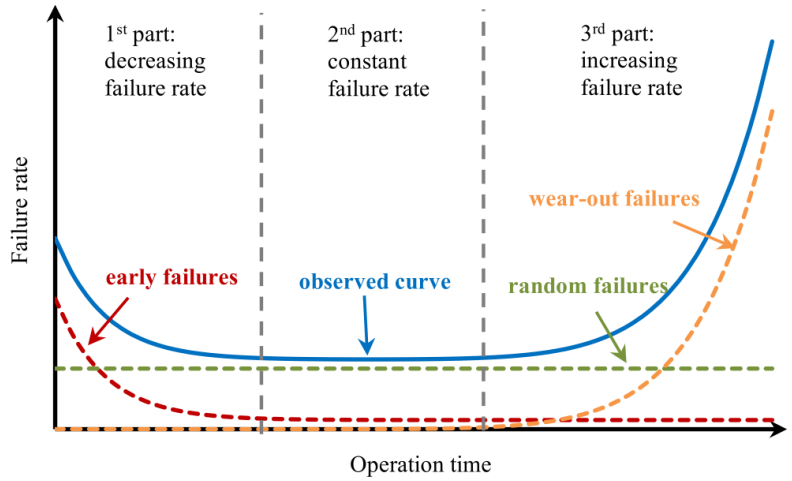


Fig. 2.13 Bathtub curve describing the failure rate during life cycle of a consumer product (not to scale) [89]

Random failures result in a low and constant failure rate throughout the operating time of the component and dominate during the second part of the curve. This stage is of particular interest in design because this represents the majority of the component's usable lifetime. As the product approaches its design lifetime limit the failure rate increases due to what are known as wear-out failures. These failures are a result of thermo-mechanical stresses during operation and can be predictable, and therefore are the focus of research for lifetime improvement.

Power semiconductor devices are expected to function without any failure for extended periods, and consequently, evaluating these devices for end-of-life is challenging without accelerated testing. Power cycling is used to generate of test data for the lifetime modelling and is an important quality and reliability assessment method. In literature, power cycling test data is used in three methods of reliability modelling:

1. Assignment of statistical reliability index based on large datasets
2. Modification of failure rates based on reliability handbooks
3. Lifetime Models and failure rate functions

Reliability based on handbook methods derive the failure rate, λ_f, for a system from the failure rates of its individual components. Correction factors are used to modify the failure rate for the devices operating conditions. In literature for power converters, the commonly used failure-rate catalogues are the Military Handbook (MIL-HDBK-217F) and FIDES [90, 91], which are based on large empirical investigations of electronics. However, more recent studies consider handbook data unreliable, with the lifetime predictions pessimistic and important factors such as thermal cycling not included.

Lifetime Models

The major steps in the lifetime estimation procedure for power semiconductor devices are shown in Figure 2.14. The operating conditions of a specified mission profile allow the temperature profile of the power semiconductors $T_j(t)$ to be calculated analytically or through simulation. The block in the diagram containing '?' represents analysis of whether the temperature has converged, as the power loss $p_v(t)$ depends on its temperature so is calculated iteratively. Cycle counting is used to convert the temperature profile into a set of repeated single stress conditions with corresponding cycles, N. Each cycle includes device electrothermal information required for lifetime prediction. The expected time to failure N_f of power semiconductor devices can be calculated using lifetime models based on power cycling tests [71].

The most well-known lifetime model is the Coffin-Manson relationship for the acceleration of fatigue under thermal cycling conditions [92, 93]. The number of cycles to failure, N_f, based on Coffin-Manson relationship can be expressed as:

$$N_f = K\Delta T^{\alpha} \tag{2.12}$$

where K is the basic lifetime, ΔT is the temperature swing, and α is the Coffin-Manson exponent which is found through cycling tests.

The Coffin-Manson approach is too simple for a complex systems and was extended, as shown in equation 2.13 to consider absolute temperature after the Arrhenius equation

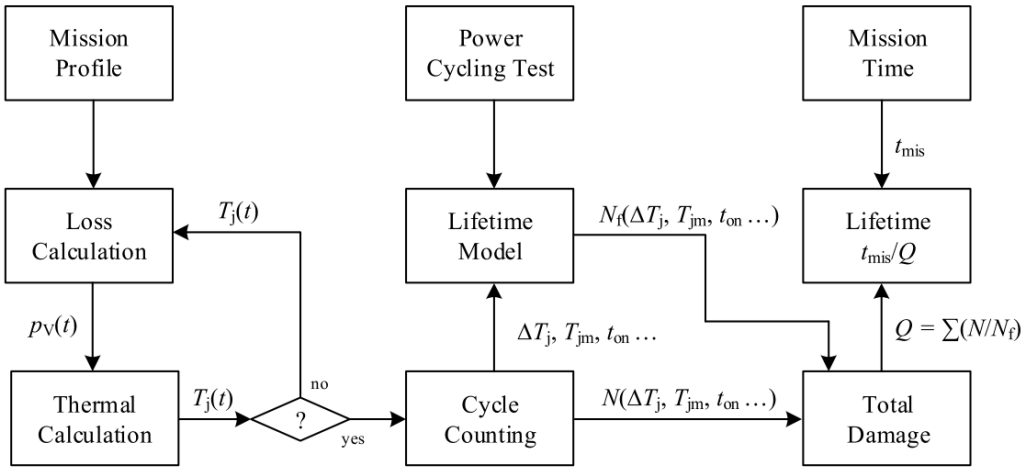


Fig. 2.14 Flow diagram for the lifetime estimation procedure [71]

described the relationship between the rate of chemical reaction and temperature, suggesting lifetime of components decreases with increasing absolute temperature.

$$N_f = K\Delta T^{\alpha} e^{\frac{E_A}{kT}} \tag{2.13}$$

where E_A is the activation energy, T is the temperature, and k is Boltzmann's constant.

Early research into semiconductor lifetime modelling was mainly focused on the power cycling capability of IGBTs in power module packaging, for example the LESIT and RAPS-DRA projects [94, 95]. In the LESIT project, 300 A 1200 V single switch IGBT modules were tested for junction temperature swings between 30 and 80°C and a mean junction temperatures between 60 and 100 °C. The CIPS 08 lifetime model, shown in equation 2.14 is an empirical multi-parameter lifetime model proposed by Bayerer for IGBT modules [96]:

$$N_f = K\Delta T_j^{\beta_1} e^{\frac{\beta_2}{T_{jmin}+273}} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} \tag{2.14}$$

where the impact of junction temperature swing ΔT_j, load pulse duration t_{on}, current per bond foot I, voltage class V, and bond diameter D are represented by power laws with exponents β_1, β_3, β_4, β_5 and β_6 respectively. The impact of minimal junction temperature T_{jmin} is expressed by an Arrhenius approach with the parameter β_2.

The CIPS 08 lifetime model includes the effect of a range of factors, which can impact the power cycling lifetime including the novel addition of the dependency of the power cycling lifetime on load pulse duration.The model describes the dependence of power cycling lifetime on the module design parameters including the chip thickness (voltage class V) or bond diameter D. Since the parameters β_4, β_5 and β_6 are negative, the lifetime is expected to decrease with increase of the corresponding parameter.

For transfer moulded discrete power devices in the TO-247 package, the first lifetime model with comparable parameter scope like power modules is proposed in [71]. Previously for discrete packaged MOSFETs and IGBTs handbook data or lifetime models for power modules was used which limits accuracy. The lifetime model shown in equation 2.15 was calculated by least square fit on the complete results where it was found the cause of failure was wear out of bond wires.

$$N_f = K \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{E_A}{k \cdot T_{jm}}} \cdot t_{on}^{\beta} \cdot I^{\gamma} \tag{2.15}$$

with the parameters of the basic constant K, the Coffin-Manson exponent α, junction temperature swing $\Delta T j$, the activation energy E_A, Boltzmann constant k, mean junction temperature T_{jm} in Kelvin, exponent β for load pulse duration t_{on}, and exponent γ for current per bond I_b. Using a lifetime model specific to the discrete package used in a system allows more accurate lifetime prediction and can be applied in the reliability analysis in this thesis.

2.7 Optimisation-based Design

Motor drive designs require analysis or modelling to gain an understanding of the real-world system, as well as optimisation to identify the most effective designs. Traditionally, to achieve optimal system parameters, a combination of analysis and optimisation are required. The complexity and multi-domain nature of IMD design means optimisation is challenging as the electric machine and power converter have to be optimised together. Power density and efficiency optimisations for converters is covered extensively in literature [97–99]. New topologies and optimisation procedures are implemented in using SiC in traction drives to

improve performance of circuit models based on analytical equations [100]. The novelty of many optimisation-based design papers is through new applications or new optimisation methods. In [101], conventional three-phase two-level inverters are optimised for power density using an approach that develops an algorithm to reduce number of potential design combinations by over 99% creating faster simulation times. The tool is composed of a set of interdependent component models but is not truly system level.

The objective in the majority of recent research into design optimisation of traction IMDs is to improve volumetric power density and efficiency through component design. [102] uses a multi-objective optimisation process to trade volumetric power density, DC bus voltage, SiC device type, switching frequency and passives for a 250 kW SiC three-level inverter.

Focus on DC-link optimisation to reduce volume is common, however use of analytical models for devices is common in this research [103, 104]. The minimum required DC-link capacitance is found through calculation in all the previously covered optimisation literature, demonstrating the possibility for optimisation that uses system-level simulations to determine optimal components.

Reliability Optimisation

Reliability optimisations often focus on aircraft [105], grid connected photovoltaic systems [106] or DC-DC converters where reliability has traditionally been more important than in traction drives. Additionally, reliability of power electronic systems in these optimisation studies use data from handbooks MIL-HDBK [90] or FIDES [107] to predict lifetime of semiconductor devices- the main source of failure in inverters. The LESIT model uses a variation of the Coffin-Arrhenius equation to use experimental power-cycling data to allow more detailed circuit conditions to more accurately predict lifetime. In [108] the LESIT model is used for SiC power module lifetime prediction as part of a multi-objective optimisation problem for a traction drive system that considers power density, cost, and reliability. Lifetime models specific to TO-247 packaging models have only recently been determined [71] so are yet to be implemented in work of this nature.

2.8 Summary

The requirement for power electronics capable of operating at higher temperatures and in smaller volumes within IMDs whilst maintaining performance and reliability is identified with the limitations of components and designs, also discussed. The suitability of SiC discrete devices to overcome these limitations and enable the development of reliable and highly compact IMDs is discussed alongside developments in passive components. Challenges within power converter design are also discussed, namely, the influence of topology and control on the electrical and physical properties of the system. As well as methods of improving suitability of the drive to operate under extreme conditions, methods of thermal management and IMD design changes are discussed, the development of which would allow for further improvements in performance. Finally, reliability analysis techniques that are used throughout this thesis are discussed with particular focus on how they are applied to lifetime estimation of SiC devices and power converters.

When considering the design of an integrated motor drive and the research question of this thesis, which is: "how can an integrated motor drive be designed so that it is optimal?". There are multiple aspects within the research areas covered in this literature review that are relevant to the design process of an IMD that would benefit from further investigation. Methods for improving analysis accuracy as well and design improvement will contribute to a more optimal IMD design.

Improvement of discrete devices recently has made them worthy of analysis to determine their feasibility in IMDs as well as the potential to improve designs through the benefits of design flexibility, paralleling, and improved reliability. This focus puts this work at the forefront of new research and challenges the convention of using power modules for automotive applications. Analysis of these SiC discretes has been covered in literature, with experimentally validated analytical models common and improving frequently. However, there is limited research into MOSFET internal parameters and how these characteristics relate to switching performance. Especially how these parameters can be used in a predictive tool in relation to the optimal choice of discrete device for an application.

Optimisation of power electronics is common however in current literature the focus is on improving power density, efficient and cost but reliability is rarely considered. Many optimisations of inverters use equations and do not consider the full system including motor modelling. Simulation of the inverter using validated MOSFET models and connection to a motor model will allow a more accurate and reliable model which is useful within the design process. The recently developed TO-247 lifetime model has not yet been used for modelling SiC discretes in an inverter so applying this to model the system will also improve the reliability modelling of the inverter.

Bringing together state-of-the-art research into the many aspects of SiC inverter design, and applying novel methodologies for improved accuracy, optimisation and reliability make this thesis an important new addition to the literature regarding power electronics and IMD design.

Chapter 3

Optimised Selection of Power Devices

3.1 Introduction

This chapter focuses on optimising the selection process of SiC discrete MOSFETs for a specific application, through the development of a device selection tool based on experimental analysis of MOSFET behaviour. When designing a power electronics system, it is important to use a dependable and consistent method for choosing the most suited device in order to maximise system performance. An optimised method can accelerate the speed of development cycles and help to optimise application-specific designs. Device selection is based on minimising conduction and switching losses whilst choosing a device with adequate thermal properties as well as considering the maximum drain-source voltage, peak current, reliability and cost.

Analysis of a range of SiC MOSFETs identifies a family of Infineon 1.2 kV devices as having the lowest figure of merit (FOM). An experimental investigation into the behaviour of this family of devices then enables an in-depth understanding of the impact of key parameters on device performance, which can be used to develop a system of device selection. Comparison of devices using datasheets has been found to be an inaccurate method as these parameters are often quoted at 50% of the rated current and voltage, making direct comparison between different devices difficult. Instead, understanding how the parameters shown in the

datasheet impact the switching characteristics of a SiC MOSFET offers a greater level of insight.

This chapter investigates how these parameters change between devices within the family, and presents the effect on the switching characteristics due to these parameters. Once fundamental understanding is in place, a supporting tool to predict performance and aid in device selection is developed, aiding in the project moving towards inverter design and component selection.

The load current, switching frequency, and ambient temperature can be defined to identify the most suitable device for a given application, with the tool automatically paralleling MOSFETs when necessary. The tool combines both power losses and the number of devices required to find the optimal device, giving the user useful information and flexibility. The tool is then further developed to allow prediction of power losses for a SiC MOSFET input by the user and allows comparison of its entire device family with the baseline MOSFETs, enabling device selection to include devices from other manufacturers.

3.2 Figure of Merit

The performance of a power device and semiconductor materials is usually evaluated using a value determined from figure of merit (FOM) equations [109]:

$$FOM_{iss} = R_{DS(on)} Q_{iss} \tag{3.1}$$

where $R_{DS(on)}$ is the on-state resistance, Q_{iss} is the gate charge required during switching for the input capacitance, C_{iss}, which is a combination of the gate-drain capacitance, C_{GD}, and the gate-source capacitance, C_{GS}.

The logic behind the equations is that lower on-state resistance, $R_{DS(on)}$, will generally result in lower conduction losses, while a lower gate charge results in lower switching losses. Therefore, total losses are minimised if the product of on-state resistance and gate charge is minimised. FOM can be used as a basic tool for device comparison and selection and is to be used here to identify the best performing family of devices to be investigated further

Table 3.1 Manufactured 1.2 kV SiC Devices

Manufacturer	Device Family Name	FOM Range
Infineon	IMW120	0.9 - 1.3
Cree-Wolfspeed	C2M0	2.4 - 4.4
Cree-Wolfspeed	C3M0	2.1 - 2.8
Rohm	SCT2	4.7 - 7.2
Rohm	SCT3	2.5 - 5.1
UnitedSiC Cascodes	UJ/UF	1.1 - 2.4
LittelFuse	LSICMO	5.4 - 5.8

in this thesis. A selection of recently released 1.2 kV SiC device families from leading manufacturers with the calculated FOM range are shown in Table 3.1.

The data in Figure 3.1 and Figure 3.2 show the $R_{DS(on)}$ and the input capacitance charge, Q_{iss}, which is the sum of the gate-drain charge, Q_{GD}, and gate-source charge, Q_{GS} from the device datasheets [12]. These figures can be used to represent the input switching FOM ($R_{DS(on)}.Q_{iss}$) and compare between devices.

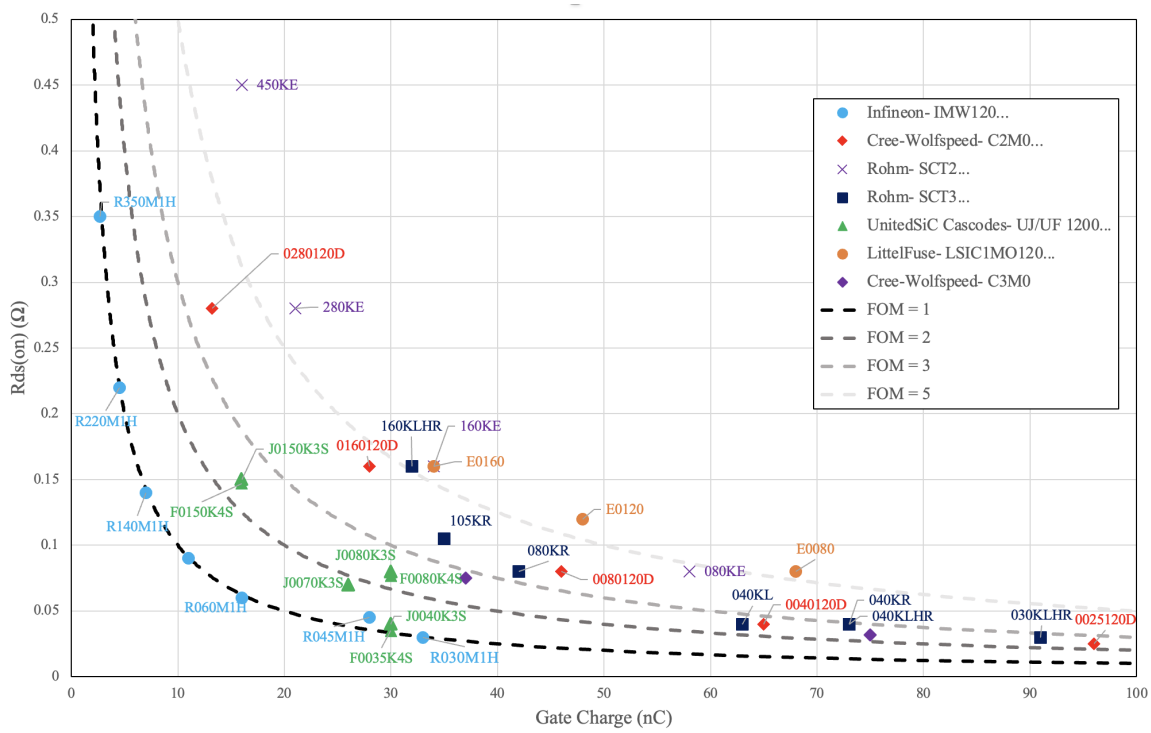


Fig. 3.1 On-state Resistance against Input Capacitance Charge for Range of 1.2 kV SiC MOSFETs Based on Datasheet Values

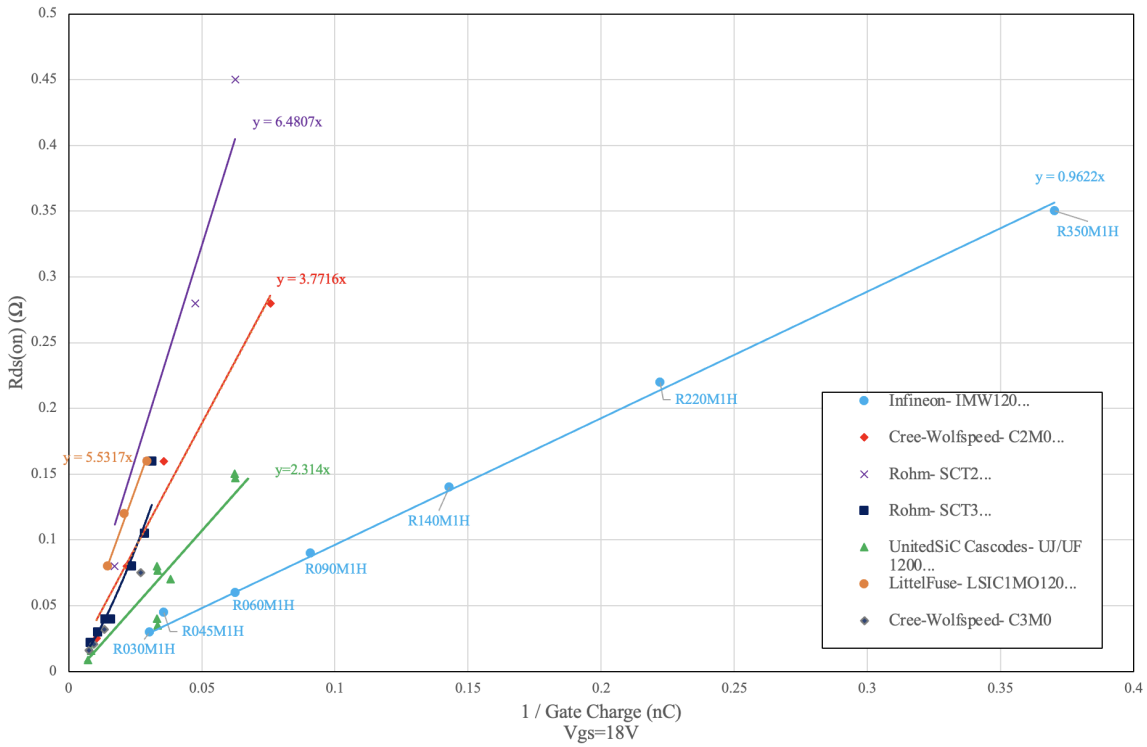


Fig. 3.2 On-state Resistance as a function of the reciprocal Input Capacitance Charge for Range of 1.2 kV SiC MOSFETs Based on Datasheet Values

Figure 3.1 shows the trendline of any devices with a FOM equal to 1, 2, 3 and 5 and in Figure 3.2 the gradients are shown, which represent the average FOM of the device family, allowing better comparison of devices. The Infineon IMW120 series MOSFETs have the lowest FOM, observed in Figure 3.1 as the curve closest to the origin and in Figure 3.2 the series with the lowest gradient. This family of devices was chosen as the best performing by FOM analysis and was taken forward for further study. Using these parameters it is possible to not only compare the overall figure of merit but also identify the suitability for high power and high frequency operation, for example a smaller contribution to the FOM due to the gate charge may suggest superior switching performance.

The total losses incurred by a MOSFET are dictated not only by its own intrinsic properties, but also the suitability to an application and operating conditions, including the operating load currents, switching frequency and temperatures. FOM does not enable the selection of ideal devices, but does give an overview of the device technology and indicates possible performance. FOM is a simplistic method of comparison and the next sections focus

on methods for modelling discrete SiC devices. After device losses are determined through analytical, experimental, and simulation methods, more detailed and accurate comparisons can be made.

3.3 Methods for Investigating SiC Device Performance

A key enabling technology for integrated motor drives (IMDs) is the effective switching behaviour of SiC MOSFETs. A discussion of the capability and validity of a range of modelling techniques and experimental methods is the starting point for accurate discussions and device comparisons. Through the analytical analysis of MOSFET switching, factors affecting switching behaviour and, therefore, the parameters of interest during experimental analysis and power converter design have been identified. By experimentally investigating the different switching behaviour of SiC devices, the effect of these parameters can be investigated and the different methods of device modelling can be validated and compared. This is important as accurately modelling power devices can be a key stage in IMD design.

3.3.1 Double Pulse Testing

A double-pulse test (DPT) fixture was constructed to obtain experimental switching waveforms for a device, which can be used for dynamic performance analysis and for validation of SiC MOSFET modelling methods. Examples of the V_{GS} input and the measured waveforms are shown in Figure 3.3.

During the first pulse, the current increases in the load inductor to a specified value. The time of the first pulse required to achieve the desired current can be calculated by equation 3.2.

$$t = I_{load} \cdot \frac{L}{V_{DS}} \tag{3.2}$$

where I_{load} is the load current, V_{DS} is the drain-source voltage and L is the load inductance. This is used to apply a range of drain currents to the DUT.

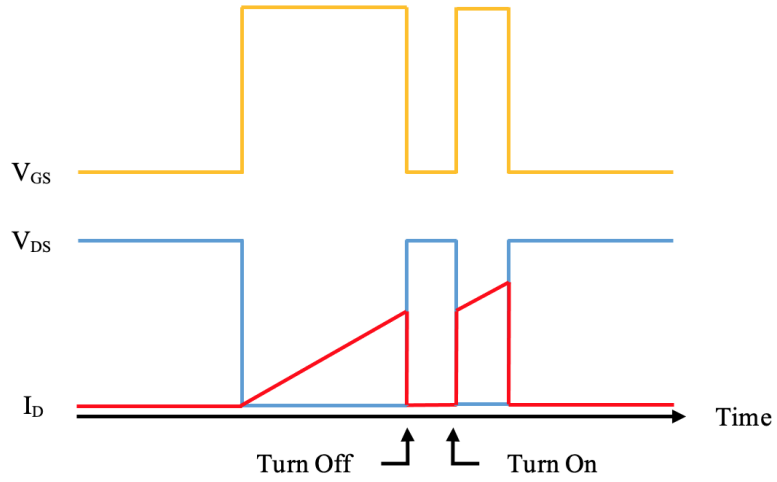


Fig. 3.3 Sample Waveforms for DPT

The turn-off characteristics of the DUT are investigated using the high-to-low transition of the first pulse, when the load current reaches the desired value and the drain current commutates from the DUT to the freewheeling diode. After a delay of 2 μs, the second pulse is used to measure the turn-on time of the device. The delay needs to be sufficiently short so the inductor current is the same level at turn-on as turn-off and the second pulse duration is kept short, to reduce the power dissipation of the device. Pulses are applied manually with long pauses so as not to heat up the DUT due to the switching losses. All tests are repeated three times with an average then calculated for each data point in this thesis.

Precise measurement methods are required in a DPT to acquire clear waveforms and accurate calculation of device switching losses. Consideration of the presence of parasitic inductance and capacitance circuit can cause undesired oscillations and couplings when used for analysing the fast switching of SiC MOSFETs. When employing the DPT technique, major obstacles include the need for wide-bandwidth current and voltage sensors, the insertion of a current measurement sensor into the switching circuit, and the misalignment between measurement of the voltage and current transient data.

The DPT in this chapter was designed to characterise the hard switching performance of the 1.2 kV SiC MOSFETs for inductive loads [110], replicating the conditions of driving a

permanent magnet synchronous motor that will be the focus of this project. A schematic of the DPT is shown in Figure 3.4, and pictures of the fixture in Figure 3.5.

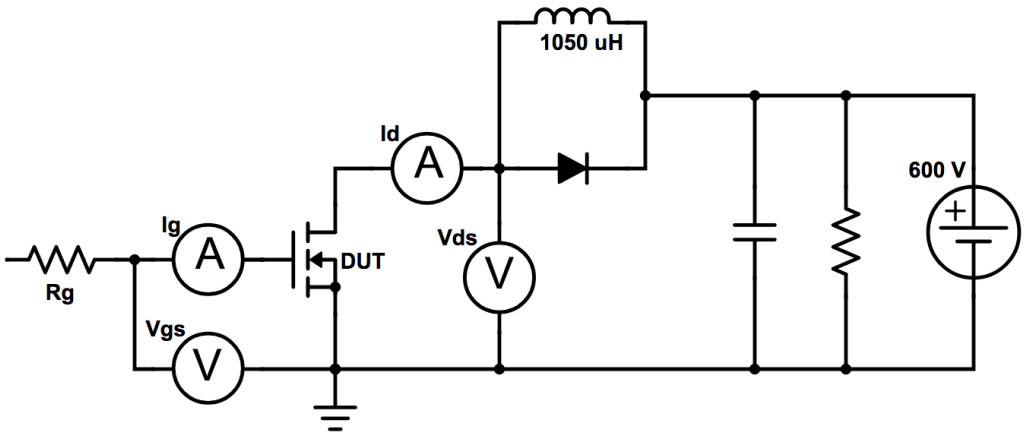
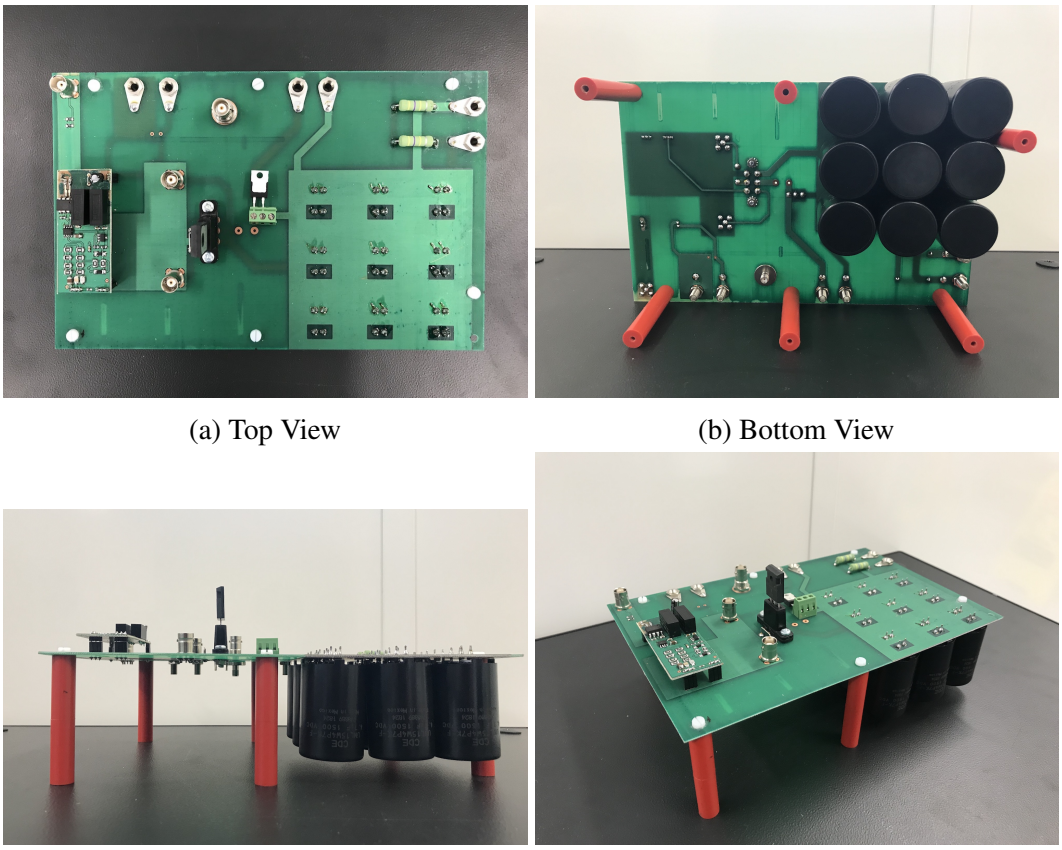


Fig. 3.4 DPT Fixture Schematic

The PCB used in this work allows dynamic measurements to be made with easy changes of the DUT. Connections for the voltage probes measuring gate-source voltage, V_{GS}, and drain-source voltage, V_{DS}, were built into the PCB to minimise ground loops and electromagnetic interference. A Tektronix TMDP0200 high-voltage probe was used to measure V_{DS} and a 10x scope probe was used for V_{GS}. The drain current, I_d, is measured using a two-stage current transformer, consisting of a small 1:10 ferrite first stage transformer and a Pearson Electronics model 2878 current monitor, which has a 70 MHz bandwidth, for the second stage. The digital oscilloscope used was a TBS2104 which has a 100MHz bandwidth and 1GS/s sample rate.

Multiple gate resistors can be populated or depopulated to change the value of the gate resistance, R_G, and provide optimum turn-on and turn-off performance. To minimise stray inductance, the capacitor bank, made up of nine film capacitors to provide a low inductance voltage source, is located very close to the source output pin and the gate driver.

The value chosen for R_G, is chosen as 10 Ω. Relatively long switching transients enables clear demonstration of the switching stages and the effect of the internal gate resistance, $R_{G_{int}}$, on the measurement of V_{GS} can be disregarded. Also, with limited measurement bandwidth,



(a) Top View (b) Bottom View

(c) Side View (d) Front View

Fig. 3.5 DPT Fixture

large R_G helps ensure credibility of the measurement results, for smaller R_G with faster switching speed will increase the requirement for increased measurement bandwidth.

In the fixture, the DUTs were mounted on a specifically designed hot plate to change the device temperature to allow switching performance measurements up to 175°C. The temperature was measured using a probe to monitor the device case temperature, which was assumed to be the same as the junction temperature after 10 minutes of heating to allow thermal equilibrium.

3.3.2 Method Comparison and Validation

Modelled behaviour of SiC MOSFETs is validated by experimental switching waveforms from double pulse testing. Analytical analysis and modelling allows the effect of device and

Table 3.2 DPT Circuit Parasitic Values

	Symbol	Value
Drain Inductance	L_d	107 nH
Source Inductance	L_s	10 nH
Gate Inductance	L_g	52 nH

circuit parameters on switching behaviour to be determined. The analytical model used in this project is developed from the switching stage descriptions and equations discussed in Chapter 2 and [111]. The model utilised in this work considers the non-linearity of internal capacitances and both circuit and device packaging parasitic inductances. The DPT circuit, the schematic of which is depicted in Figure 3.4, was also simulated in LTSpice. In this work, the manufacturer published level-3 MOSFET models are used where the electrical model is coupled with a thermal model.

Since the parasitic circuit elements in the MOSFET packaging and the circuit have an important effect on the switching performance in the analytical and LTSpice models, the identification of these parameters is required for an effective validation. The PCB geometry and device packaging result in parasitic inductances that impact the switching performance of the MOSFETs in the DPT, with large voltage swings across these parasitic elements when there is large di/dt. TO-247 package inductances were available from a study [112], however the circuit inductances dominate the switching. Without access to the complex experimental equipment required to measure the partial inductances of the DPT fixture, extraction from experimental switching data was attempted. Using experimental data for switching rates, oscillation amplitude and frequency, an initial estimate for circuit parasitic inductances at the gate, drain, and source of the DUT was found using equations developed in [112]. Choosing the IMW120R030M1H LTspice device model, and a load current of 15 A and drain-source voltage of 600 V for switching, these estimates were tuned to match the LTspice output to experimental data. These circuit inductance values, shown in Table 3.2, were then used in the simulation over a range of operating conditions for the devices.

Validation of simulation results with experimental waveforms was carried out using the IMW120R030M1H model at turn-on. The oscillation frequency and amplitude and the rise

time of the measured waveforms are accurately captured in the simulations. The switching energy loss is calculated over the full operating range of the device (up to 50 A) at the nominal drain-source voltage of 600 V by integrating the instantaneous power during the turn-on and turn-off. Comparisons are shown in Figure 3.6 for a load current of 30 A at 600 V based on analytical and LTspice models. The analysed data is summarised in Table 3.3, with the discrepancy between the turn-on switching energy loss, E_{sw-on}, below 10 % for both models.

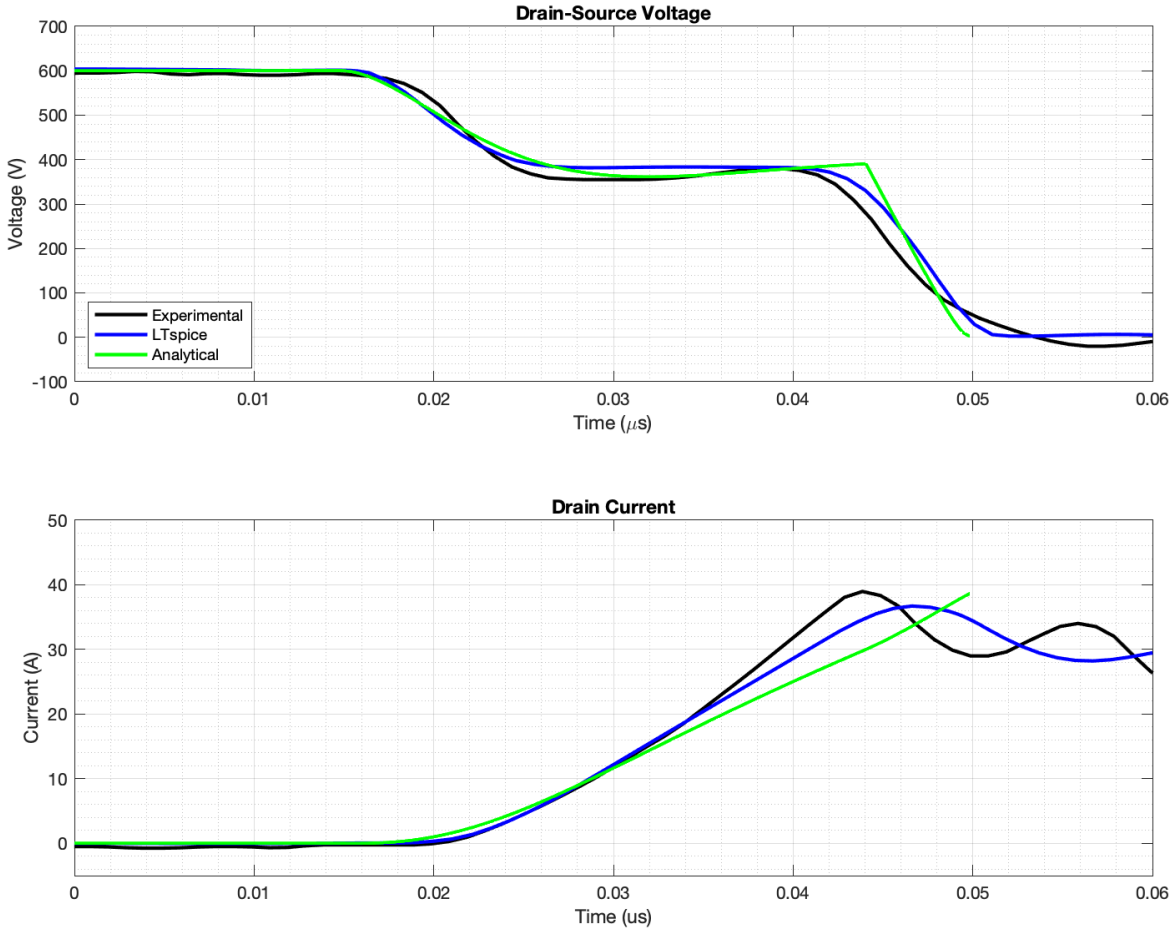


Fig. 3.6 Switching Waveform from Experimental Data, LTspice and Analytical Model

The LTSpice model is nearer to the experimental data than the analytical model, although it takes longer computationally and is limited as the models are provided by the device manufacturer. The analytical model can be modified for any device using only basic datasheet values. However when the temperature is not equal to 25 °C quoted on the majority of

Table 3.3 Comparison of Turn-On Switching for Experimental and Analytical

	Experimental	Analytical	Error	LTspice	Error
E_{sw-on} (μ J)	204.25	184.19	-9.8 %	221.78	8.5 %
T_{on} (ns)	53	49.85	-5.9 %	48.67	-8.1 %
$T_{delay-on}$ (ns)	23	19.78	-14.0 %	21.20	-7.8 %
T_{rise} (ns)	30	35.01	16.9 %	30.67	2.2 %

datasheets the analytical model requires further information. The static parameters of transconductance, V_{th}, $R_{DS(on)}$ and $R_{g_{int}}$ are temperature dependent and therefore to accurately model devices at temperatures other than those given in the datasheet these variations must be known, requiring further experimental work for each specific device, as described in [63].

The models described in this section may be used to represent the switching characteristics of the power MOSFET. All of the crucial parasitic elements are considered in the analytical model, enabling their effect on the switching performance of a MOSFET to be individually investigated. This difference in characteristics is reflected in the datasheet, which quotes a range of parameters, from maximum rating to static, dynamic, and switching electrical characteristics. These parameters are determined by the internal structure of the device and vary depending on the size, design, and layout.

In conclusion, analytical, SPICE, and experimental methods of analysis have different applications in engineering design. Experimental analysis is the basis of the investigation in this chapter, it provides accurate data for analysis and allows the validation of the other approaches. The analytical model is used to identify important parameters, investigate the effect of individual parameters, and can be used to relate differences in device performance back to fundamental semiconductor physics. Once SPICE simulation models are validated, they enable faster investigation of new operating conditions for devices under investigation and allow for experimentally unavailable data to be produced. The validated SPICE models can also be used within full circuit systems containing SiC MOSFETs to accurately simulate a variety of power systems; as will be done in future Chapter 4 and Chapter 5 of this thesis.

3.4 Switching Investigation for a Family of 1.2 kV SiC MOSFETs

The investigation into the dynamic performance of the family of SiC is an important contribution of this thesis as it forms the basis of device selection for an optimised integrated motor drive and is required to maximise the potential benefits of SiC. Explanation of the experimental data based on theory applied to the family of devices allows parameter trends in state-of-the-art commercial MOSFETs to be analysed and is required for validation of device models.

Comparative studies exist between SiC and Si MOSFETs and IGBTs, but these often do not refer to the difference between the datasheet parameters and instead focus on fundamental properties to explain differences in switching characteristics. A study in [113] compares static and dynamic behaviour of SiC MOSFETs from different manufacturers without developing detailed understanding of causes of the differences.

In recent years, many scholars have studied the influence of circuit parasitic parameters on the switching characteristics of SiC devices. Experimental studies of switching waveforms under the influence of parasitic elements demonstrate what are observed but do not provide detailed explanations on the mechanism behind those observations [114, 112, 115]. Switching characteristics of MOSFETs can be analytically modelled to assess the effect of parasitic elements [64] to explain the physical meaning behind these observations. Use of experimental data as well as analytical analysis is required for a complete and comprehensive understanding of SiC MOSFET behaviour analysis and will be the focus of this section.

The theory describing the switching stages and device behaviour is demonstrated by the analysis in Chapter 2 and the subsequent analytical model. From the analytical study the influence of the parasitic capacitances, C_{GS}, C_{GD} and C_{DS}, as well as $R_{DS(on)}$ and transconductance are identified as important and are determined. The parameters in Table 3.4 show the relevant MOSFET characteristics, as identified in Chapter 2, available in the manufacturer's datasheets.

Table 3.4 MOSFET Characteristics

Parameter	**Symbol**	**Units**
Drain-Source On-state Resistance	$R_{DS(on)}$	mΩ
Input Capacitance	C_{iss}	pF
Output Capacitance	C_{oss}	pF
Reverse Capacitance	C_{rss}	pF
Transconductance	g_m	S
Total Gate Charge	Q_G	nC
Diode Reverse Recovery Charge	Q_{rr}	nC

A number of studies have experimentally shown the effect that datasheet parameters have on switching performance. However, this study hopes to experimentally investigate the parameter trends of commercial devices and understand the relationship between device parameters and performance, allowing the development of the device selection tool. To achieve this, it was decided to focus on a single manufacturer and a single family of SiC MOSFETs, to discount differences in behaviour due to internal structure, design, and manufacturing practise. This allows conclusions to be drawn on the combination of parameters that are both physically possible and desirable in state of the art devices and what effect these parameters have on device performance overall. The device names and parameters of interest for the Infineon family are shown in Table 3.5, where I_D is the rated load current.

Table 3.5 Infineon Family of Devices

Device Name	$R_{DS(on)}$(mΩ)	I_D(A)	C_{iss}(pF)	C_{oss}(pF)	C_{rss}(pF)	g_m(S)
IMW120R030M1H	30	56	2120	116	13	14
IMW120R060M1H	60	36	1060	58	67	7
IMW120R090M1H	90	26	707	39	4	5
IMW120R140M1H	140	19	454	25	3	3
IMW120R220M1H	220	13	289	16	2	2
IMW120R350M1H	350	5	182	10	1	1

The data in Figure 3.7 show a comparison between the datasheet value for the Infineon devices. When investigating real devices from a manufacturer family, the combined effects of the changes in datasheet parameters can be observed with trends and analysis that enable

a novel understanding of these parameters. The data shows that, as the current rating of the device increases, the on state resistance and internal gate resistance decrease whilst the parasitic capacitances and transconductance increases, and gate charge and reverse recovery charge at test conditions increase.

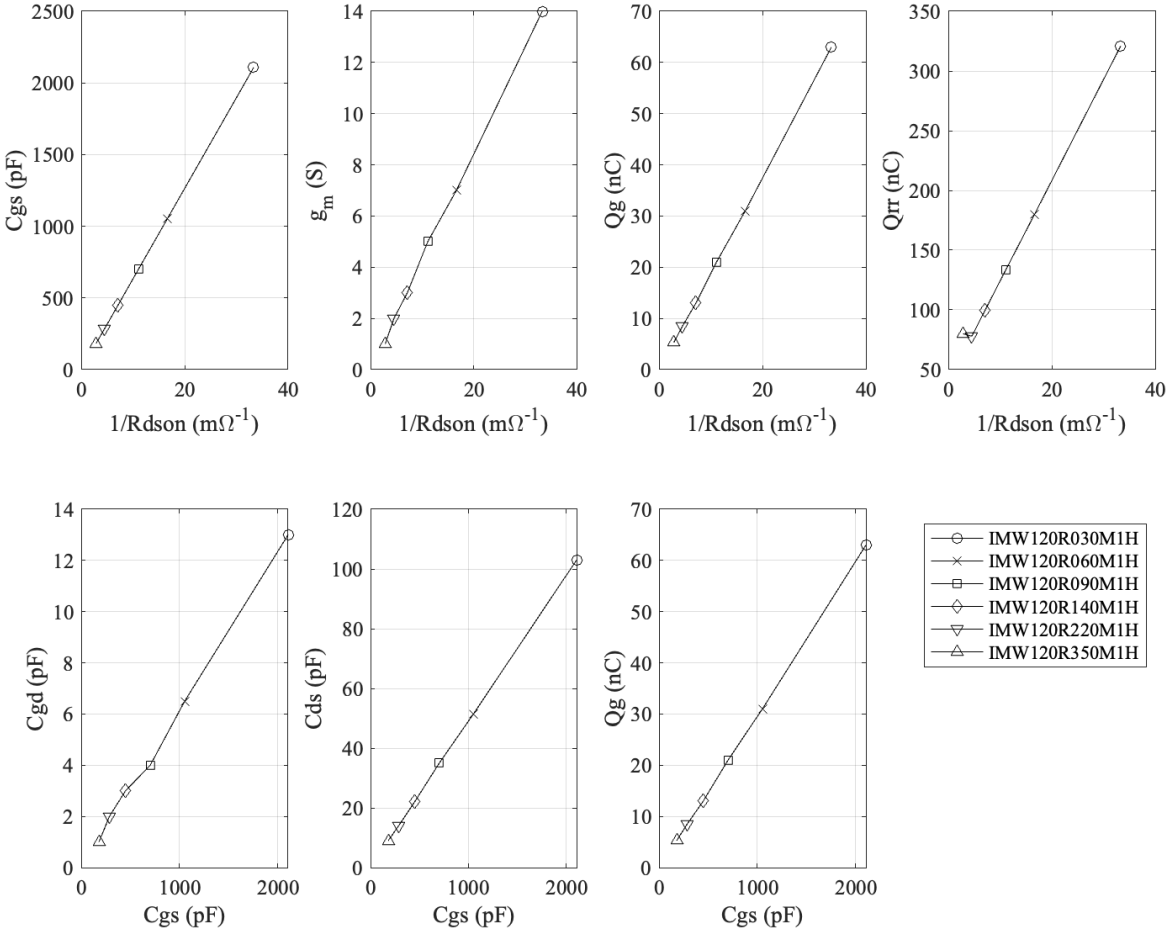


Fig. 3.7 Relationship between Infineon Series Datasheet Parameters showing linearity of quoted device characteristics

An important consideration is that the capacitances are functions not only of device parameters and sizing but also vary with the applied voltage, V_{DS}. However, this analysis is based on the quoted value on the datasheet which for these devices is 800 V. The change in capacitance due to V_{DS} is sufficiently similar in all investigated MOSFETs so that, at any value V_{DS} chosen, the plots and parameter relationships of the datasheet can be directly

compared. The non-linearity of the internal parasitic capacitances is nonetheless key to understanding the switching behaviour.

In this section, the experimental data is analysed to investigate switching speeds and losses, which are the key considerations when analysing SiC MOSFETs for the majority of power electronic applications. Another characteristic of the device available from the experimental data is the gate charge Q_G. Gate charge is representative of switching losses and will be investigated to analyse its suitability within the device selection tool. The on state resistance for the MOSFETs in the family range from 30 mΩ to 350 mΩ and are to be tested using the DPT fixture at 600 V (50% maximum voltage), for a range of load currents. This data will allow switching transients for the devices to be analysed and compared for a range of operating conditions.

3.4.1 Switching Speed Characterisation

Figure 3.8 shows a schematic representation of the switching time definitions used for the MOSFET switching waveforms.

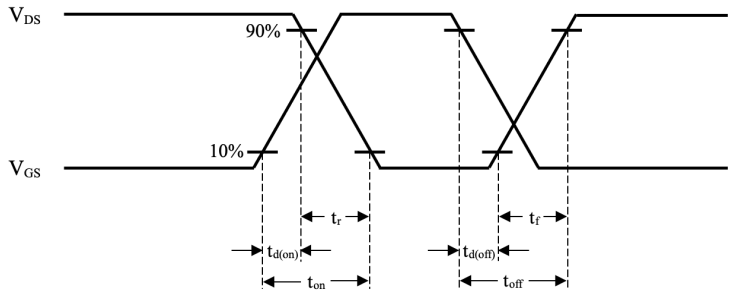


Fig. 3.8 Switching Times Definitions

The experimental waveforms in Figures 3.9 and 3.10 present waveform transient data for drain-source voltage, V_{DS}, and drain source current, I_{DS}, at turn-on and turn-off for the Infineon MOSFETs studied here, captured using the DPT fixture. The transients are aligned from the start of the gate pulse and plotted to enable a clear display of the differences between the devices under the same test conditions.

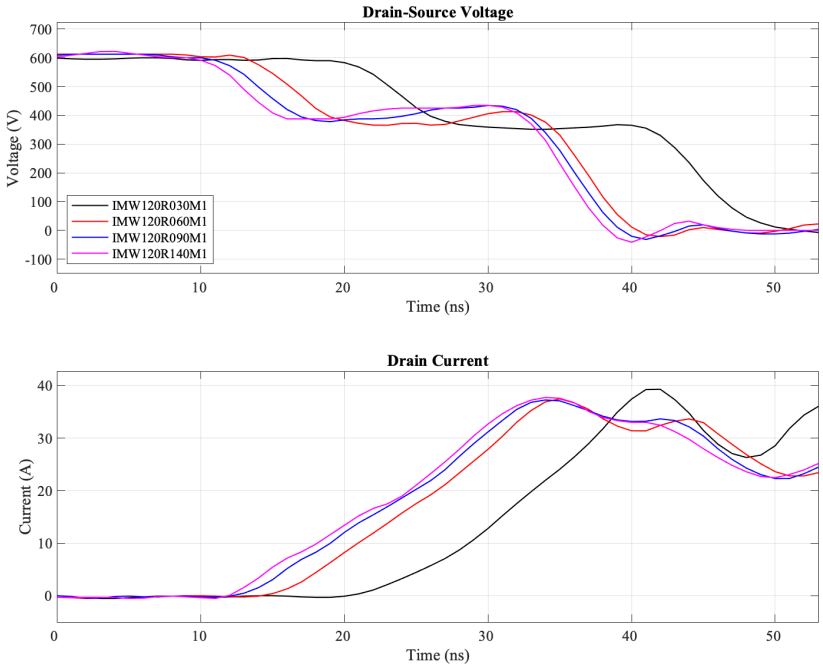


Fig. 3.9 Turn-On Transients Device Comparison

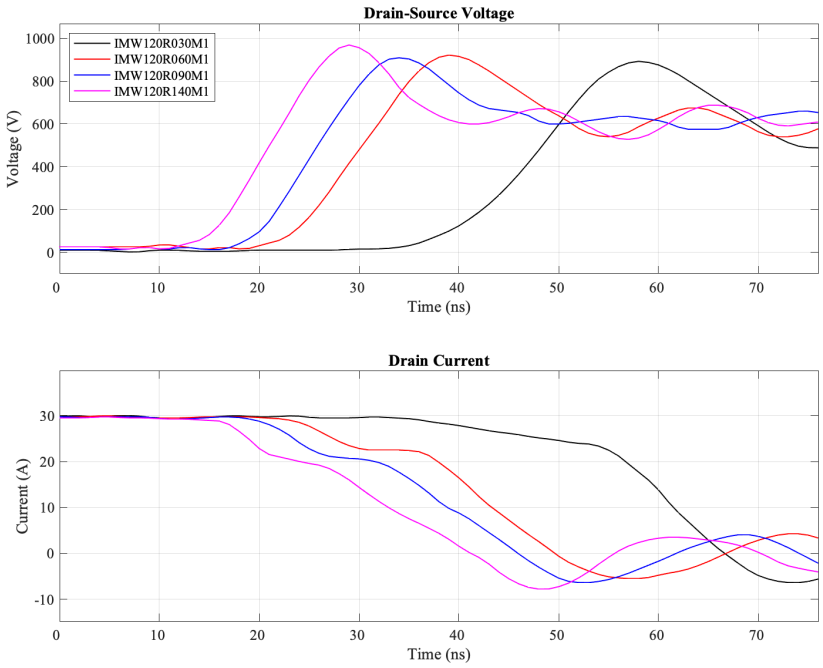


Fig. 3.10 Turn-Off Transients Device Comparison

From the experimental waveforms the key switching characteristics of the devices can be determined. Based on these switching waveforms, the switching times are calculated and plotted with respect to the drain-source current at a case temperature of 25°C with the

drain-source current varying between 9 A and 30 A. It should be noted that the maximum current rating of the device, as noted in Table 3.5, limits the experimental range for the 220 $m\Omega$ and 350 $m\Omega$ devices. The following Figures are a summary of data extracted from transients similar to the Figures 3.9 and 3.10. An important aspect shown in Figure 3.9 is the initial drop and plateau of V_{DS} during turn-on due to parasitic inductances in the DPT. However, this has a similar effect on all devices and therefore will not have a negative impact on the ability to make accurate comparisons during analysis.

The data in Figure 3.11 show the total switching times for each device at case temperature of 25 °C. Figure 3.12 then allows for a more detailed understanding of the plots by including the rise and fall values, as well as the delays at the turn-on and off.

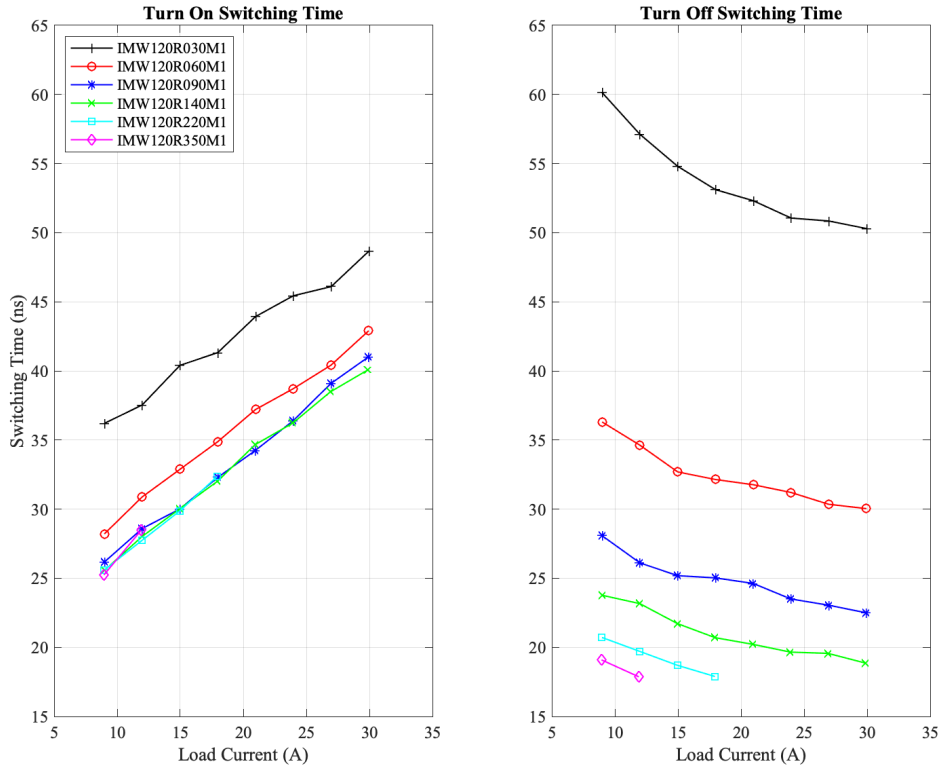


Fig. 3.11 Load Current Impact on Total Switching Time Device Comparison

Although conclusions can be made relating to device comparisons from the switching times against load current data, Figures 3.13 and 3.14 show the switching times for the Infineon devices while more clearly demonstrating the effect of the discussed parameters, shown in or based on the data in Table 3.5, on the behaviour. As the datasheet parameters

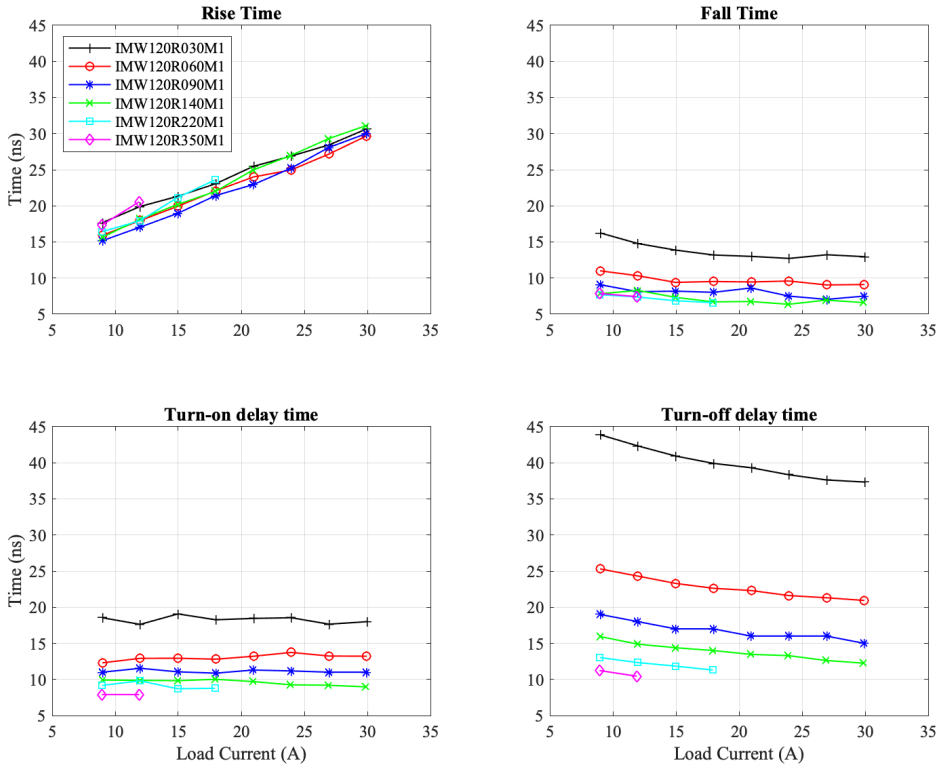


Fig. 3.12 Load Current Impact on Switching Time Components Device Comparison

are related to MOSFET design and sizing, and have linear relationships between themselves as shown in Figure 3.7, the trends between the parameter values and the switching times match. Only by fundamental understanding through analytical modelling and analysis can the effect of specific parameters be understood. However, by taking this approach, the relationship between parameters is known; therefore, the relationships between times and device characteristics can be assumed to be relevant to all the parameters in the figures, even if they do not have a direct influence on the specific behaviour.

It is clear that turn-on switching times increase linearly with load current, due to the increase in rise times, with the time delay at turn-on being unaffected by current. Increase of load current from 10 A to 30 A results in a increase in turn-on time of 35% for the 30 mΩ MOSFET. As can be observed in the switching analysis and the switching stage definitions in Chapter 2, $t_{d(on)}$ is determined by the device $V_{d(on)}$ and C_{iss}. It should be noted that C_{iss} is dominated by C_{GS}, when V_{DS} is close to the bus voltage. The rise time depends on the rate of

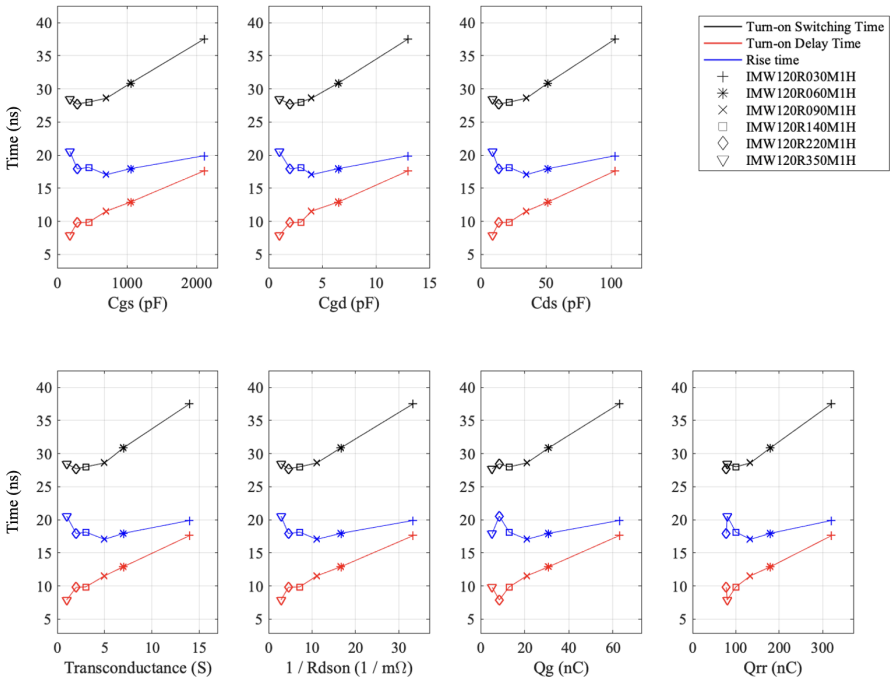


Fig. 3.13 Turn-On Switching Times Variation with Datasheet Parameters at 13 A

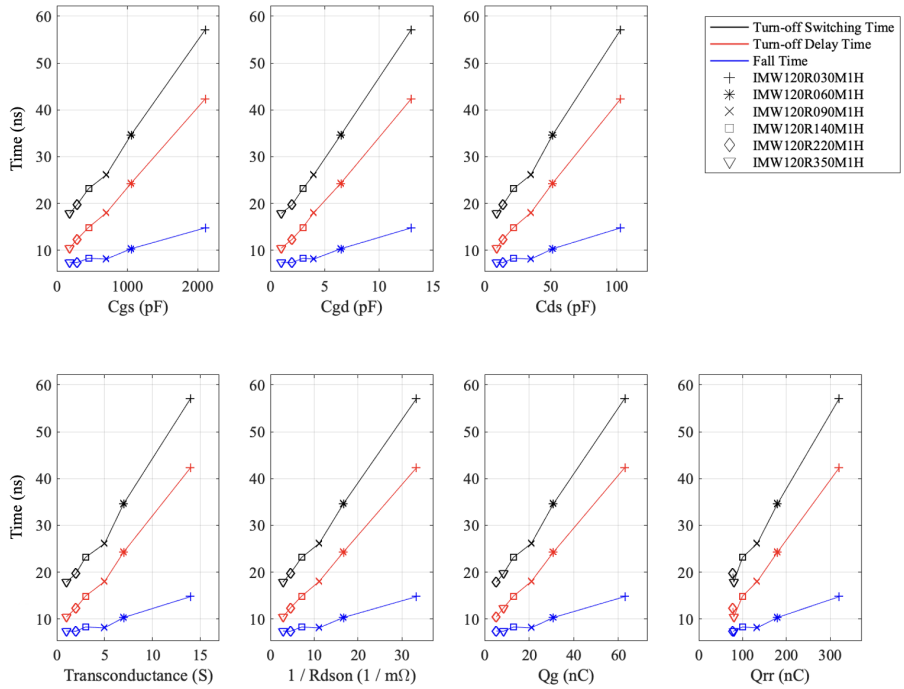


Fig. 3.14 Turn-Off Switching Times Variation with Datasheet Parameters at 13 A

change of the drain-source voltage at turn-on, $d\upsilon_{DS}/dt$, described in the equation:

$$\frac{d\upsilon_{DS}}{dt} = -\frac{V_{GG} - V_{miller}}{R_G C_{GD}} \tag{3.3}$$

where V_{Miller} is the Miller plateau voltage:

$$V_{miller} = \frac{I_{DD}}{g_m} + V_{th} \tag{3.4}$$

where V_{GG} is the input voltage of the gate drive, R_G is the gate resistance, and I_{DD} is the load current. Therefore, C_{GD} and g_m both have a proportional relationship to turn-on switching time, explaining the trends in Figure 3.13. Devices with higher $R_{DS(on)}$ have lower C_{GS}, C_{GD}, C_{DS} and g_m and hence have lower switching losses.

From the above equations, the increase in the rise time due to the higher load current can be explained by the decrease of $d\upsilon_{DS}/dt$, which can be observed experimentally in Figure 3.15. The full family of devices follows this trend, and the differences between each MOSFET will be discussed later in the section.

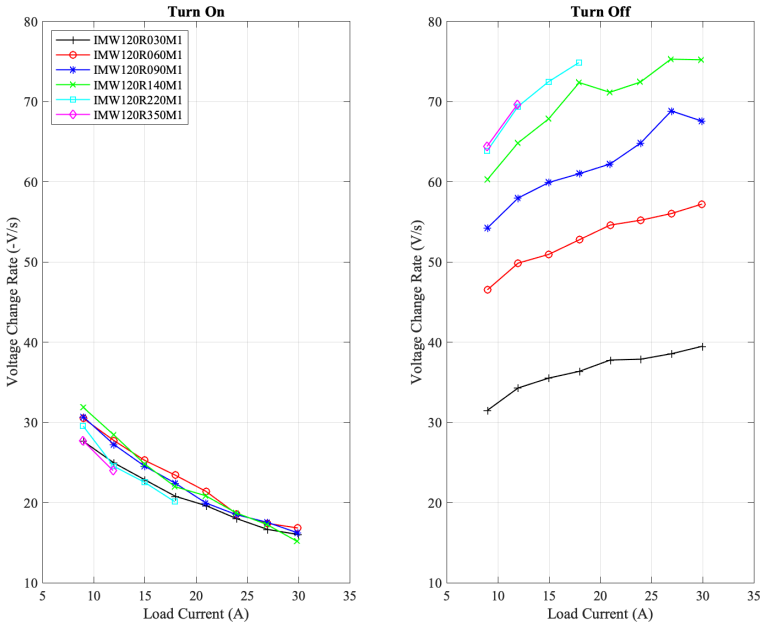


Fig. 3.15 Load Current Impact on Voltage Slew Rate Device Comparison

The turn-off switching times experience the opposite trends to turn-on; showing a decrease with increasing load current. However, the turn-off time decreases non-linearly, because of the decrease in time delay, while the fall time remains almost constant over the range of load currents. The time delay is again determined by C_{iss}, R_G, and the gate voltage. At turn-on this voltage is V_{th} which is constant for all load currents, however, at turn-off the gate voltage is equal to V_{Miller} which from equation 3.4 is known to be dependent on the load current. Therefore, the higher load current results in higher V_{Miller} and therefore V_{DS} begins to increase earlier. When V_{DS}=$V_{DS_{on}}$ as during the $t_{d(off)}$ transient, C_{GD} is still smaller than C_{GS} but significantly larger than the value of C_{GD} is during the $t_{d_{on}}$ transient. The fall time, t_f, is determined by C_{GD}, R_G and V_{Miller}. The first stage of the voltage rise is dependent on $\frac{d\upsilon_{DS}}{dt}$:

$$\frac{d\upsilon_{DS}}{dt} = \frac{i_g}{C_{GD}} = \frac{V_{GS}}{R_G C_{GD}} \tag{3.5}$$

where during fall time, $V_{GS} = V_{Miller}$, which means that t_f decreases with load current due to a higher V_{Miller}. However, the trend is weaker than at t_r related to the increased C_{GD} during the turn-off transient.

It is observed that turn-off delay is much longer than turn-on delay, because C_{GD}, is smaller under high V_{DS} as experienced during the turn-on stage. Furthermore, changes in C_{GD} will result in a notable variation in the voltage change rate at turn-off. The length of the miller plateau affects the rate of change of V_{DS} during turn-on and turn-off. The miller plateau is largely determined by C_{GD} and so the increase results in a noticeable decrease in the voltage slew rate. I_{DS} does not decrease until V_{DS} reaches the DC bus voltage, and any increase in C_{GD} results in a longer duration and so the drop in I_{DS} is delayed by the increase in C_{GD}. The value of C_{GD} is two orders of magnitude smaller than C_{GS}, and the influence on the rest of the switching waveform can be ignored.

3.4.2 Switching Losses Characterisation

Switching losses are of greatest interest when considering inverter design as the energy loss leads to inefficiency and heating in the devices. With a constant switching frequency, two

determine account for the switching loss: the duration of the switching transients, which is determined by the switching speed, and the magnitude of V_{DS} and I_d, both of which can be affected by the current and voltage stresses and drops. C_{GS}, C_{GD}, C_{DS}, L_s, and R_G increase the loss during switching by slowing the switching speed and prolonging the switching process, as discussed and experimentally shown in the previous section. Figure 3.16 shows the switching energy loss definitions used by Infineon and in this thesis.

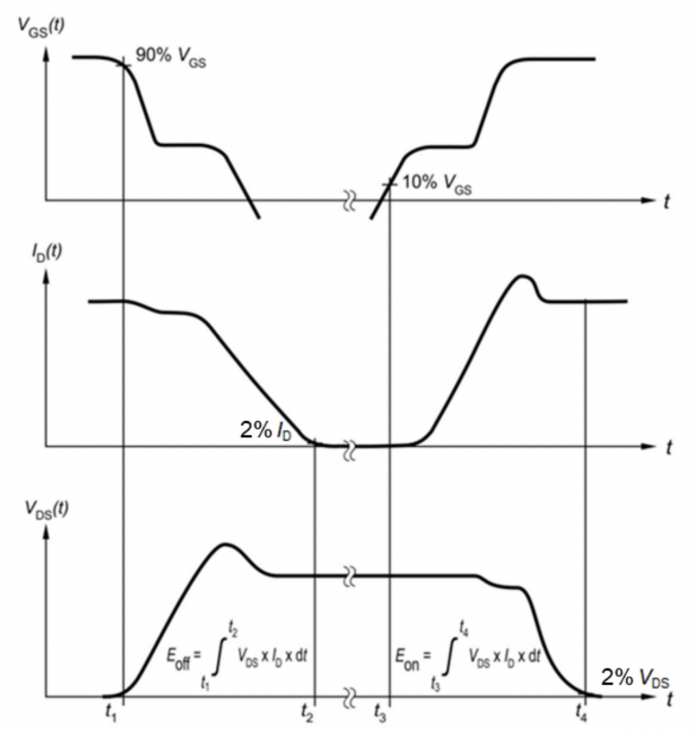


Fig. 3.16 Definitions for switching energy losses[12]

The instantaneous power losses during the switching transient can be calculated by multiplying the V_{DS} and I_d. An example of this is presented in Figure 3.17 using data from transients in Figures 3.9 and 3.10. In turn-on, the only clear result is the increase in turn-on delay time of the 30 mΩ MOSFET. However, at turn-off there is a clearer difference between the devices, with the lower $R_{DS(on)}$ MOSFETs experiencing a longer turn-off delay and a higher peak power loss, although the energy loss will require further analysis.

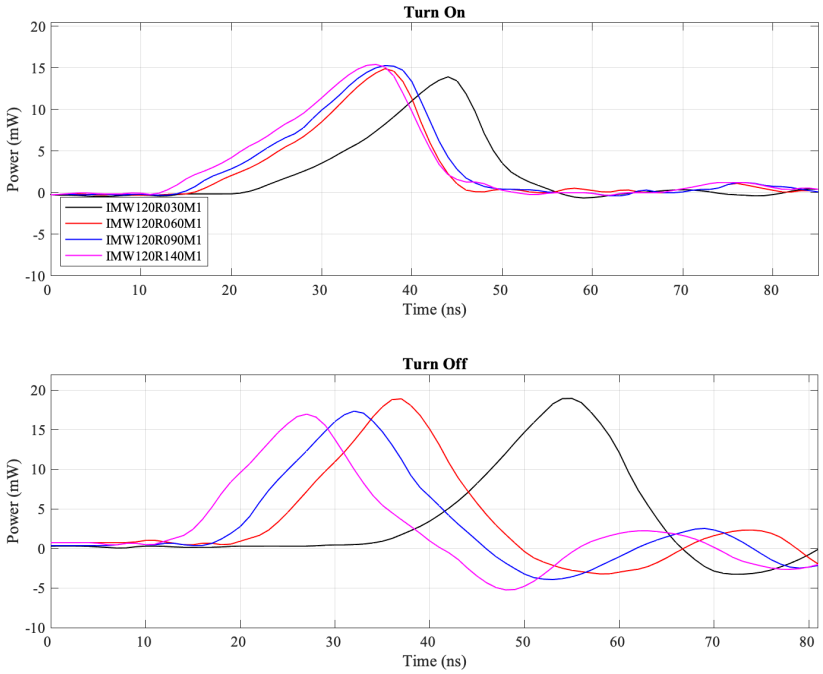


Fig. 3.17 Power Loss Transients Device Comparison

The data in Figure 3.18 demonstrates that for turn-on and turn-off transients, higher load current will increase losses. With the effect of load current on total swithcing losses shown in Figure 3.19.

The different losses between devices match what is seen in the data for the switching times, specifically for t_r and t_f, as during the delay times I_d or V_{DS} are very low, resulting in minimal energy loss during these periods. The difference between the different devices when considering switching losses is more clear than when considering switching times. The difference between switching times of the different devices has been described earlier, however as energy loss is the product of V_{DS} and I_d, a higher load current will naturally lead to greater losses. Minor differences in switching times between the devices therefore become exaggerated differences in switching losses, highlighting the importance of the parameters such as C_{iss} when considering MOSFET application in IMDs.

An increase in I_d does not increase the losses of the device proportionally. This can be explained by the higher current running through the inductor, which during turn-off results in more rapid charging of the internal capacitances of the device, thus reducing the switching times for a higher current.

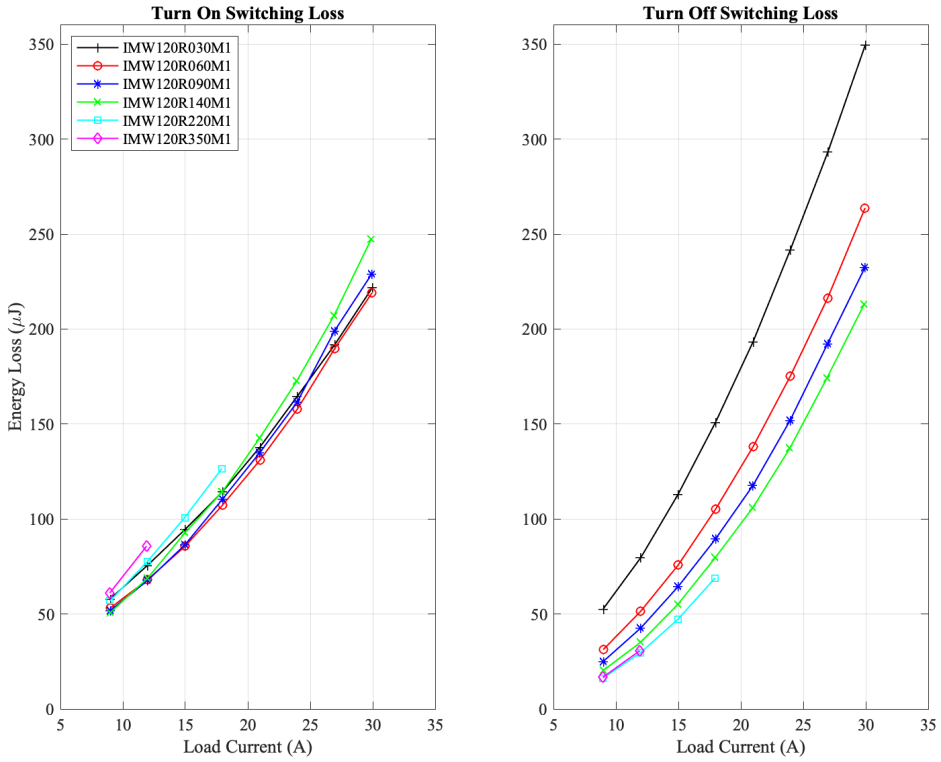


Fig. 3.18 Load Current Impact on Switching Energy Loss at Turn-On and Turn-Off Device Comparison

The data in Figures 3.20 and 3.21 then show the transients for 13 A and 30 A respectively. An interesting observation from Figure 3.20 is that for devices above an $R_{DS(on)}$ of 140 $m\Omega$, the total losses begin to increase with higher $R_{DS(on)}$. This occurs because of the relationship between the transconductance and the C_{GD} in the MOSFET family. Equation 3.3 shows that lower C_{GD} causes a faster rate of change of V_{DS}, while lower g_m has the opposite effect. The difference between the C_{GD} and g_m of the 30mΩ device and the 140mΩ device is 10 pF lower and 11 S lower respectively which results in very similar turn-on losses. The difference between the C_{GD} and g_m of the 140mΩ device and the 350mΩ device is 2 pF lower and 2 S lower respectively, therefore the smaller relative change in g_m compared to the C_{GD} change explains the increase in turn-on losses. This is an interesting observation when choosing the optimal SiC MOSFET, suggesting the relationship between datasheet parameters within the family requires more investigation.

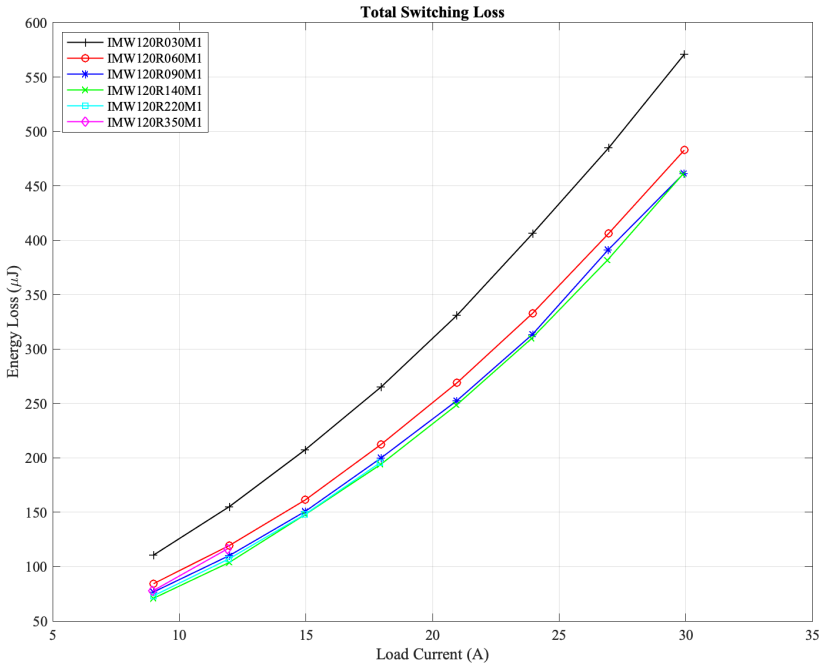


Fig. 3.19 Impact of load current on total switching energy loss device comparison

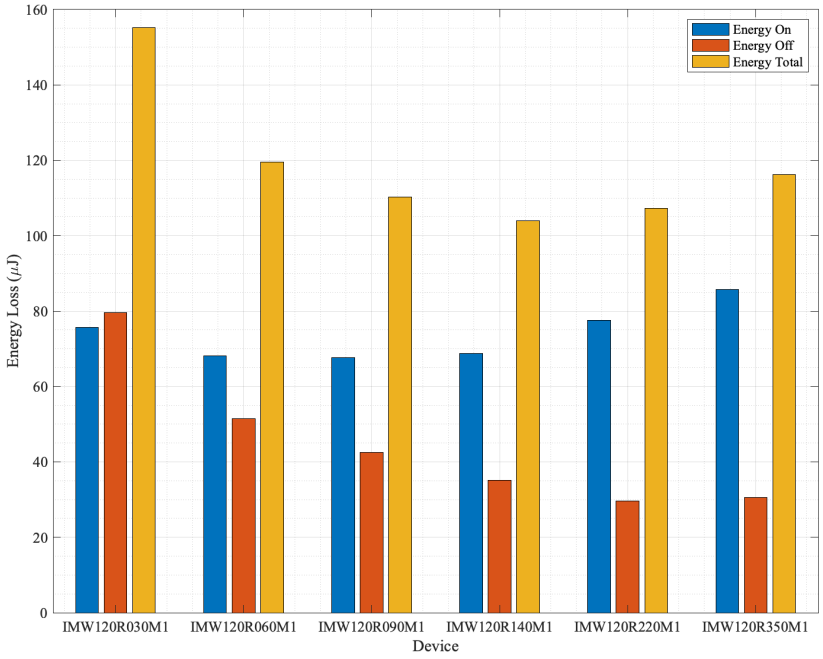


Fig. 3.20 Comparison of the Switching Energy Loss between Infineon Devices at 13 A

The data in Figures 3.22, 3.23 show a summary of the key parameters for the switching transients. The data shows that due to the relationships between the parameters, it may be possible to predict the general trends relating to device behaviour and device characteristics.

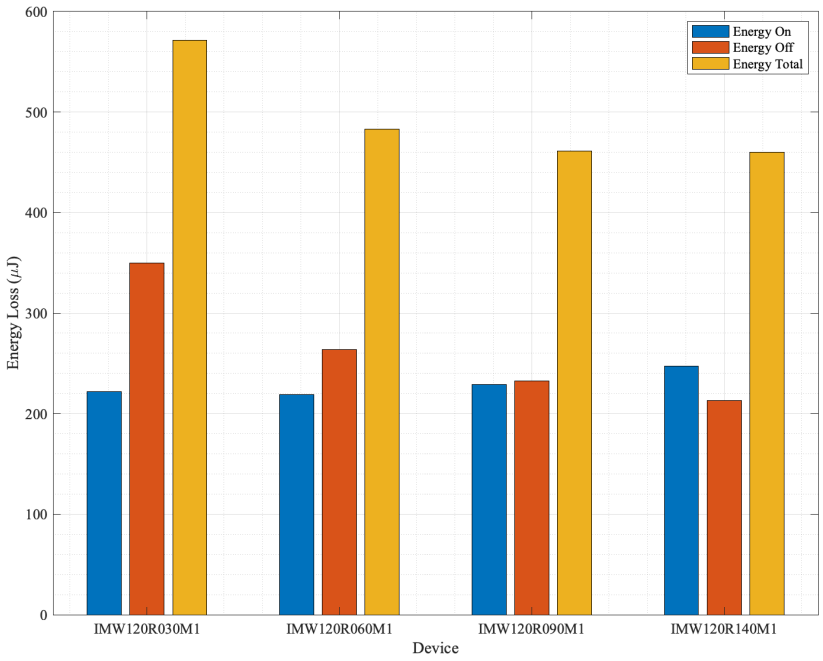


Fig. 3.21 Comparison of Switching Energy Loss between Infineon Devices at 30 A

The Figures show the strong relationship between the datasheet parameters and turn-off loss due to the differences in fall time. As C_{GD} increases $\frac{d\upsilon_{DS}}{dt}$ will decrease, as shown in equation 3.3, causing the overall switching loss to increase.

In 3.22, the turn-on losses at lower values of parasitic capacitance show the opposite trend, and there is a decrease in the turn-on losses. Lower capacitances in the devices result in circuit parasitics dominating and detrimentally influencing the data, causing large overshoots and ringing. This effect is reduced when the load current increases as the magnitude of the losses increases, and therefore the circuit effects become relatively small, as seen in Figure 3.23.

For an increase in C_{DS}, the turn-on losses barely change, while at turn-off, the losses increase for higher values of C_{DS}. There is a significant oscillation when I_d decreases to zero, and the amplitude of the oscillation increased with increasing C_{DS}, this was due to the resonance caused by L_d, L_s and C_{iss}. In summary, the load current increases losses during switching as described, and devices with lower $R_{DS(on)}$ have higher switching losses within the Infineon family due to longer switching times mainly caused by larger parasitic capacitances.

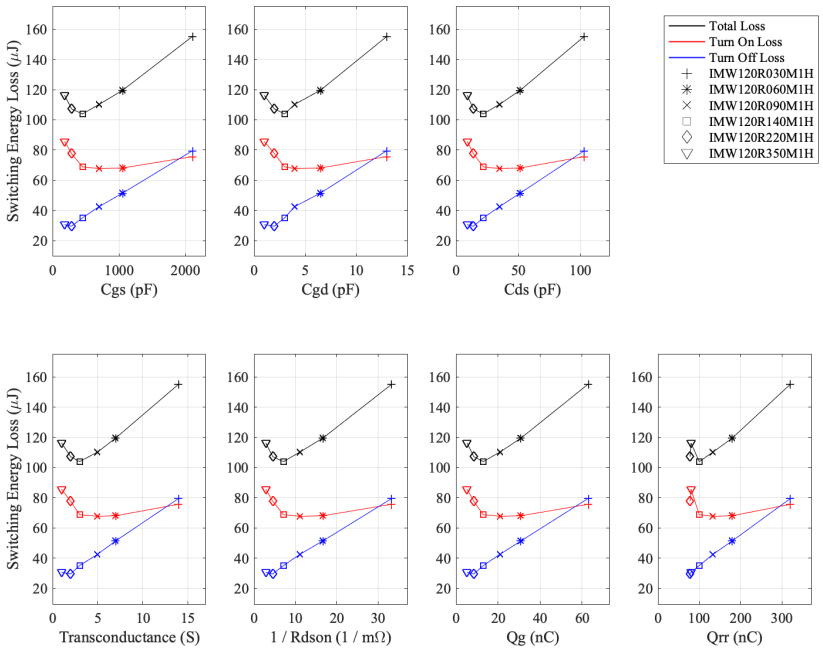


Fig. 3.22 Switching Loss Variation with Datasheet Parameters at 13 A

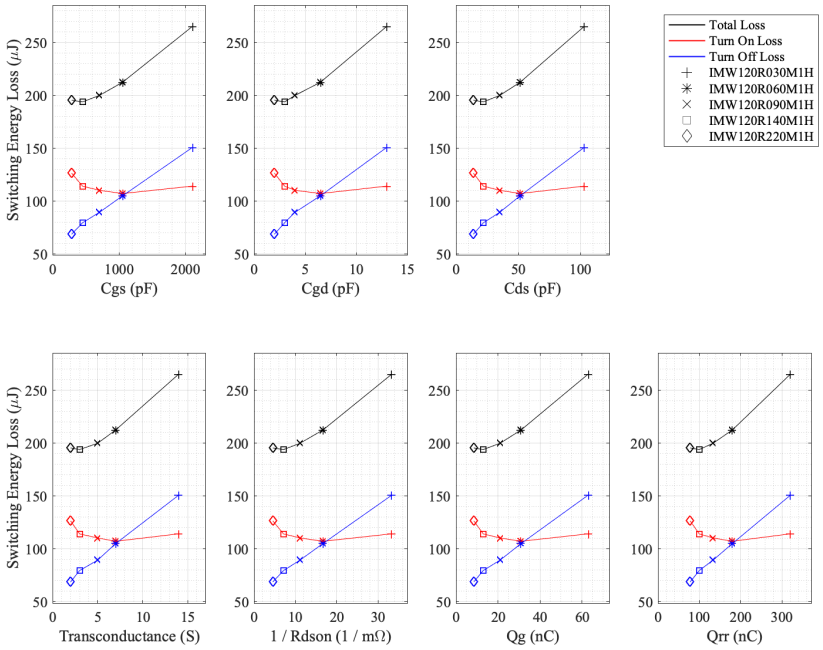


Fig. 3.23 Switching Loss Variation with Datasheet Parameters at 18 A

3.4.3 Gate Charge Analysis

Gate charge has been discussed previously in chapter 2 as being a good representation of switching losses for a device. The value of the gate charge is found through measurement of

the gate current, making its measurement circuit disconnected from the main DPT analysis system. Therefore, the load current will not influence the gate charge value. Figure 3.24 shows the gate current transient from the DPT.

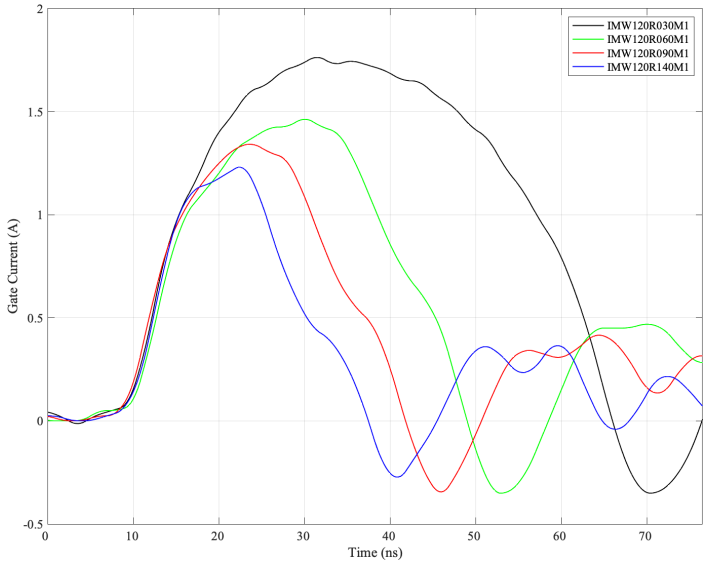


Fig. 3.24 Turn-Off Gate Current Transients Device Comparison

In the analysis done in Chapter 2, a constant current source of I_g is applied to the gate and charges the gate capacitances. In actual operating conditions in this project, the gate is supplied a voltage V_{GG} through the resistor R_G, so the variation of the current I_g is not constant as in the gate charge curve. The gate voltage grows exponentially with time constant given by the group RC related to input inner capacitances of device and gate resistance.

When a constant voltage gate drive is used, the peak value of gate current can be determined from:

$$I_{g(peak)} = \frac{V_{GG}}{R_G} \tag{3.6}$$

where R_G is the internal and external gate resistance. Devices with higher $R_{DS(on)}$ also have higher $R_{g_{int}}$, which explains why the peak gate currents in Figure 3.24 decrease as the $R_{DS(on)}$ of the device increases. The total value of gate charge depends on C_{iss}, C_{oss} and the transconductance. Larger capacitances require more charge during the switching stages of the MOSFET and the transconductance impacts the miller plateau voltage.

Taking into account the gate charge measured instead of switching losses directly, the same relationship between parameters is shown in Figure 3.25, showing the gate charge values for a load current of 13 A. This analysis shows that the gate charge values follow the same trends as the switching losses, and confirms the theory of the gate charge being representative of losses. The load current does not affect Q_G and is less affected by circuit parasitics, making the data more easily applicable for general comparisons of the devices than Figure 3.22.

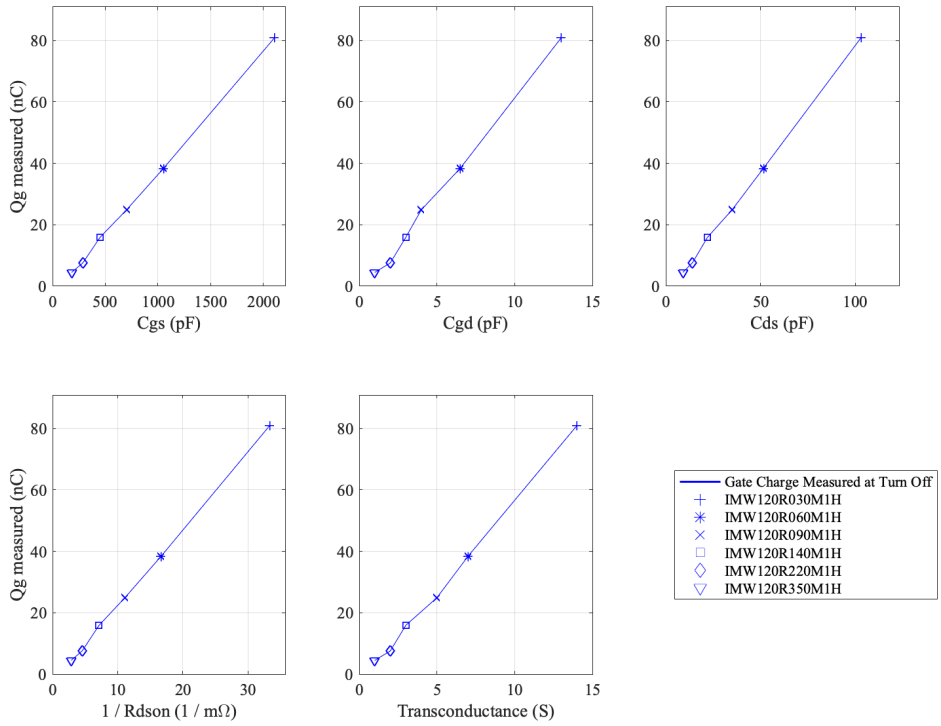


Fig. 3.25 Turn-Off Gate Charge Variation with Datasheet Parameters

3.4.4 Voltage and Current Stresses

The decrease in drain current at turn-off induces a voltage drop across the parasitic inductances, which will incur additional stress across the MOSFET, as a voltage overshoot, V_{os}, in V_{DS}. Overshoot is an important factor in inverter design, as it can cause damage to the

MOSFET or other circuit components. Its value can be predicted using equation 3.7.

$$V_{os} = V_{DD} - (L_s + L_d)\frac{di_d}{dt} \tag{3.7}$$

The voltage overshoot data during turn-off is shown in Figure 3.26 and increases with load current. V_{DD}, L_s and L_d are constant in the DPT, so the value of V_{os} is dependent on $\frac{di_d}{dt}$. The lower $R_{DS(on)}$ device have lower overshoot due to smaller $\frac{di_d}{dt}$ which results in them also having slower switching times as described previously. With higher load currents, the inverter has to deliver more power to the load, which can cause higher voltage overshoots.

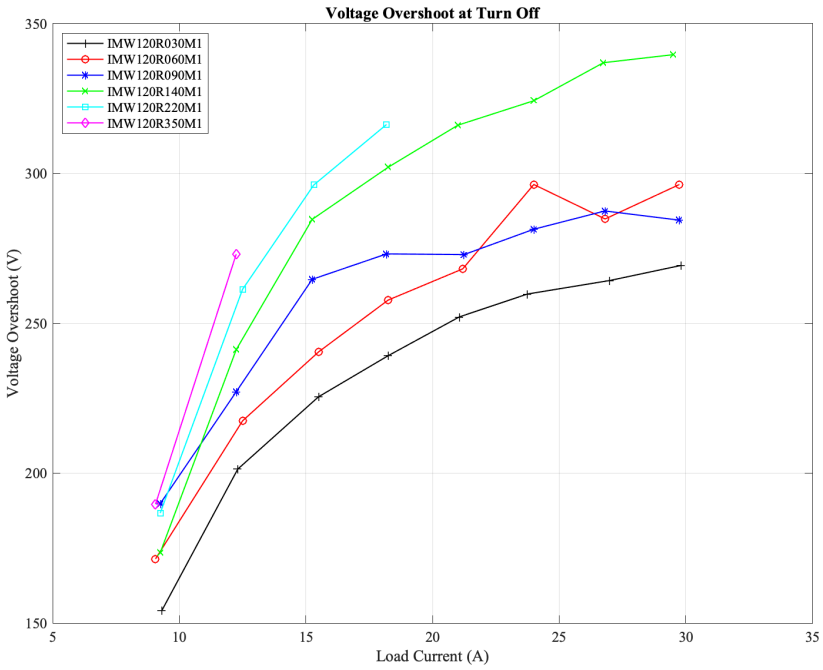


Fig. 3.26 Voltage Overshoot Device Comparison

3.4.5 Impact of Temperature

High temperature behaviour is one of the benefits of SiC devices and an important consideration of IMD design. The turn-on and off switching analysis for the MOSFETs for temperature between 25°C and 175°C for drain current of 30 A are shown in Figures 3.27, 3.28 and 3.29. As temperature increases, the $\frac{dI}{dt}$ and $\frac{dV}{dt}$ rates are increased during turn-on,

and decreased during turn-off. It can also be seen that the turn-on delay times decreased, whereas the turn-off delays increased.

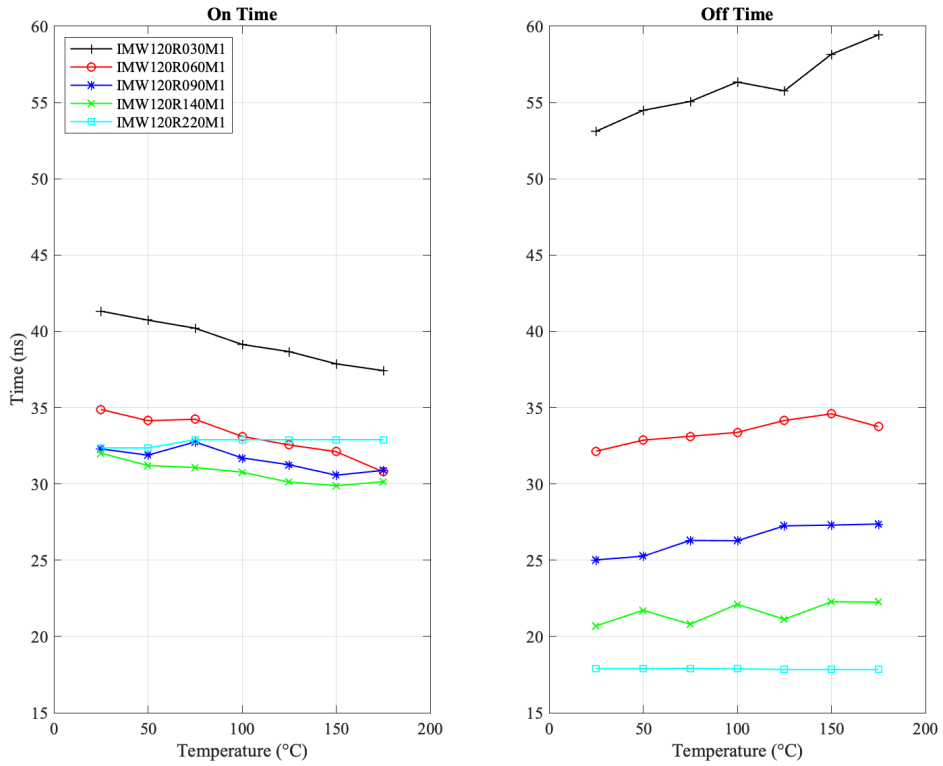


Fig. 3.27 Temperature Effect on Overall Switching Time

Considering that junction capacitances are not temperature sensitive, this behaviour is related to the temperature dependence of the transconductance and V_{th} of the SiC MOSFETs. Because the transconductance g_f increases with temperature for SiC MOSFET, V_{Miller} will decrease for a given load current. If temporarily neglecting the change of V_{th} due to temperature, the reduction of V_{pl} will result in smaller t_r and t_f, that is to say, faster $\frac{dI}{dt}$ and $\frac{dV}{dt}$ during the turn-on switching transients and slower during turn-off. This explains why the turn-on energy becomes smaller under higher temperature. The trend of energy loss at turn-off can also be explained in a similar way.

The change of V_{th} also plays an important role as the smaller turn-on delay is a result of the reduced V_{th} under higher temperature. V_{th} and V_{pl} change t_r in opposite directions. Therefore, the temperature dependence of $\frac{dI}{dt}$ depends on the combined effect of both. Consequently, the turn-on energy loss decreased with temperature, while the turn-off energy loss increased,

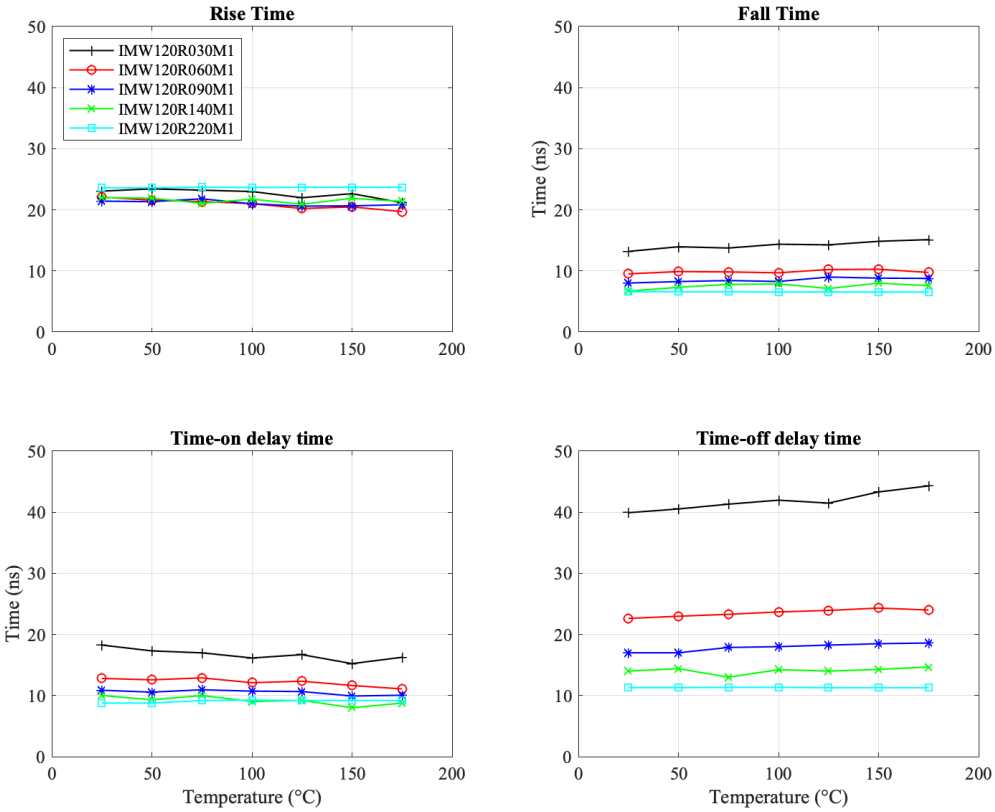


Fig. 3.28 Temperature Effect on Switching Times

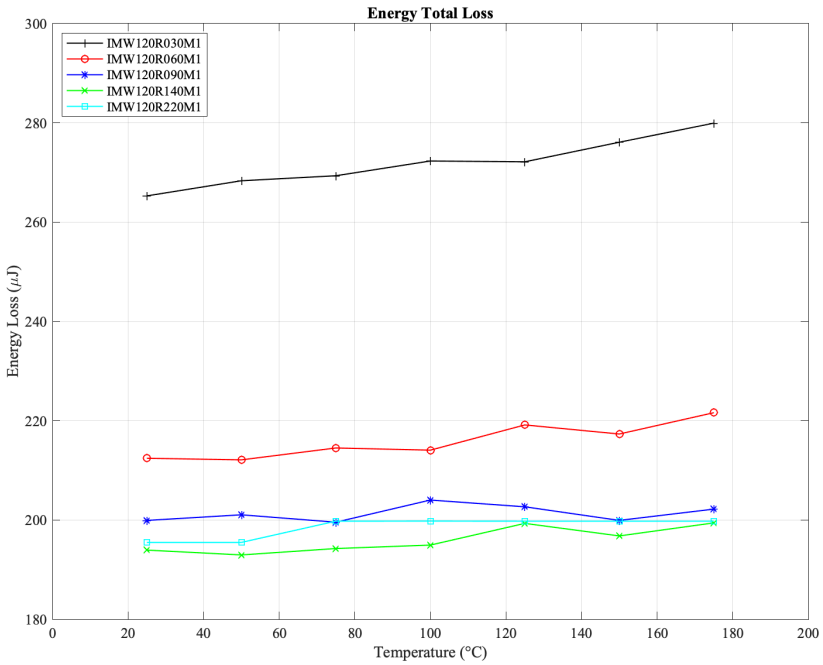


Fig. 3.29 Temperature Effect on Switching Losses

resulting in the total switching loss remaining almost constant for all but IMW120R030M1H, which has a small positive gradient.

3.5 Optimised Device Selection

For inverter design, the choice of the device depends on the operating conditions and the working environment. Understanding device parameters that impact the static and dynamic characteristics and behaviour of the MOSFET is a major asset for a circuit designer using SiC devices. A tool has been developed that makes use of experimental data to allow device comparisons for specific applications. The circuit designer can input load current, switching frequency, and temperature to find the most suitable Infineon device, and the tool automatically parallels the MOSFETs when necessary. The tool considers both power losses and the number of devices required when finding the optimal device, providing useful information and flexibility to the user. The diagram in Figure 3.30 shows how the device selection tool (DST) is used to process experimental data, datasheet data and user inputs to select an optimal device.

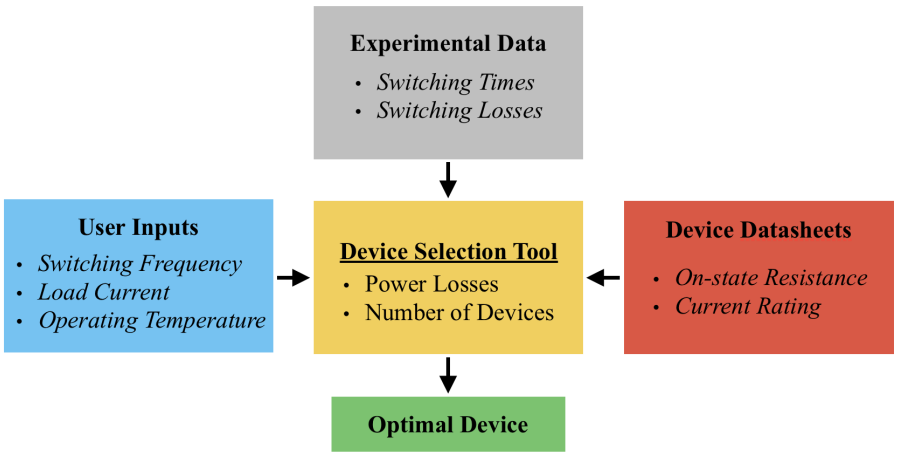


Fig. 3.30 Device Selection Tool Process

The tool is then further developed to allow a prediction of power losses for a SiC MOSFET input by the user and allows comparison of its entire device family with the investigated Infineon MOSFETs, enabling device selection to include non-Infineon models.

3.5.1 MOSFET Analysis and Paralleling

The exact power loss and suitability of the device can be determined by interpolation and extrapolation of the experimental data to the circuit specifications. If the load current input is higher than the current rating of the device the tool is capable of automatically paralleling the device and dividing the current through multiple devices before calculating the total power loss.

Previously, effects on switching energy loss were presented; however, here the effect on power loss can be seen at different switching frequencies. Figure 3.31 shows the power loss of the devices at a switching frequency of 100 kHz. The effect of increasing load current and paralleling MOSFETs on switching, conduction and total loss is clear.

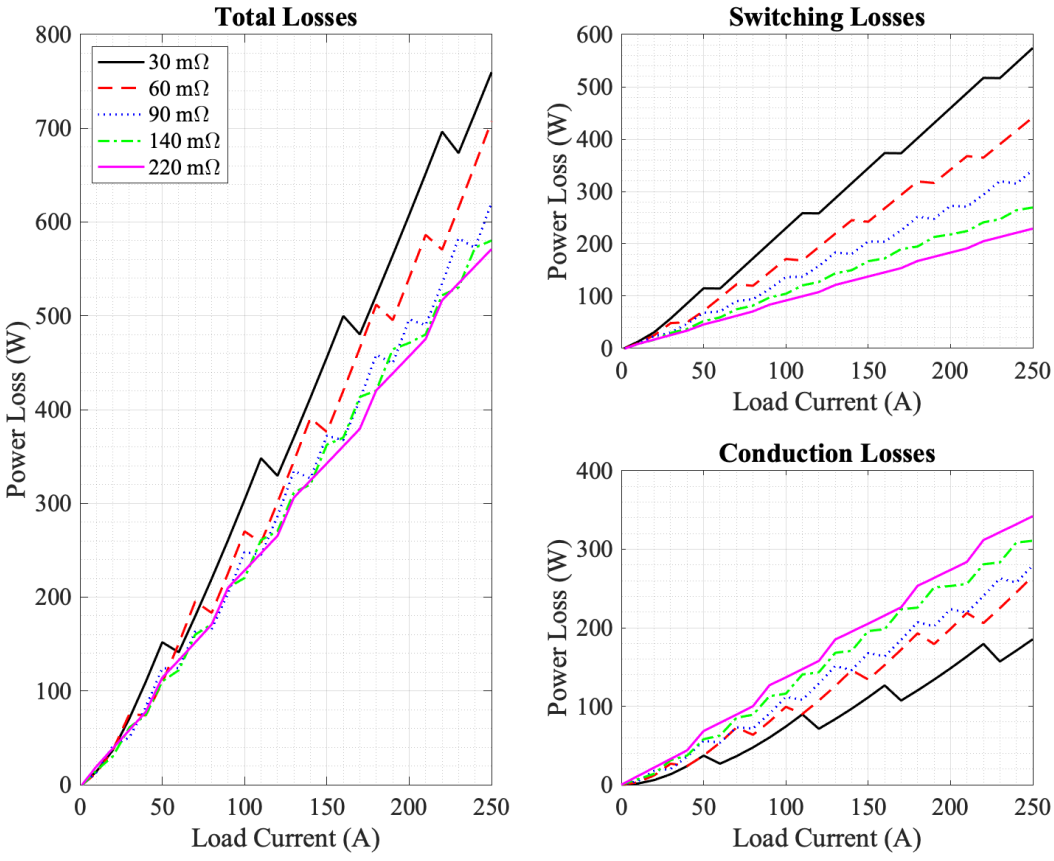


Fig. 3.31 Load Current Impact on Power Losses Device Comparison

When a device becomes paralleled the load current is split equally, resulting in a reduction in the total conduction losses which is proportional to I^2. Switching losses will also be

reduced because a lower load current reduces switching times, as seen previously. Therefore immediately after an extra device is needed Figure 3.31 shows a step like reduction in the total power loss. The chosen switching frequency will determine which device exhibits the lowest power loss for an application, as it determines the amount of conduction and switching losses.

Figure 3.32 shows the split of the switching and conduction power loss for a load current of 200 A for a range of switching frequencies. The graph of total power loss can be used to determine at what frequencies the higher switching losses of the lower $R_{DS(on)}$ devices overcome their lower conduction losses to produce a higher overall power loss.

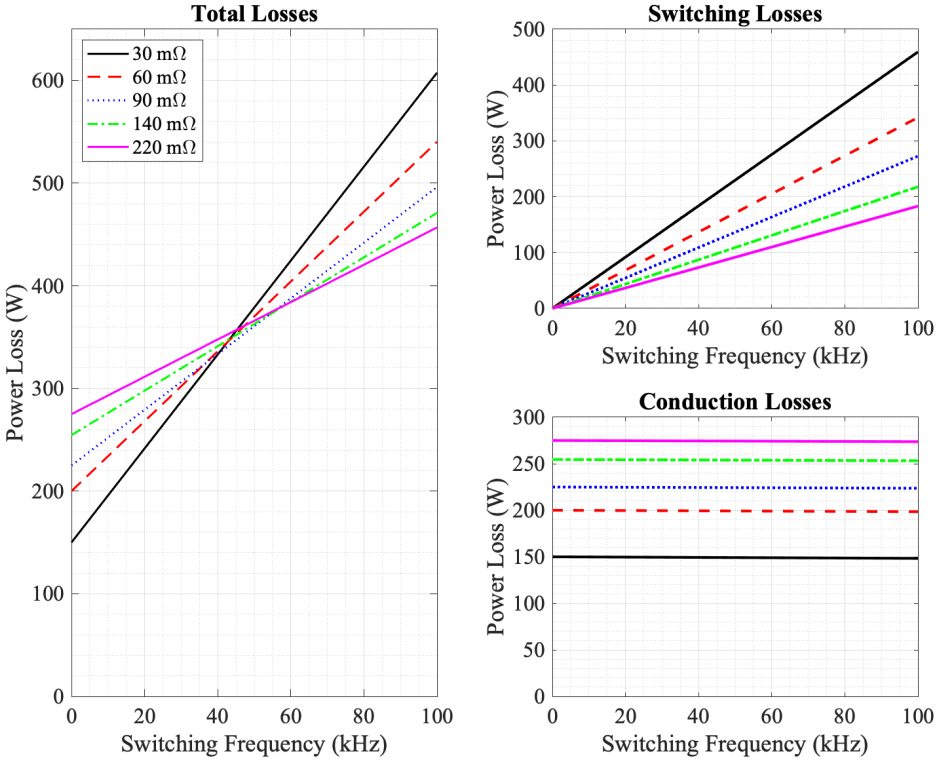


Fig. 3.32 Switching Frequency effect on Power Losses Device Comparison

This is useful when selecting a device for an application or tuning an application to suit a specific device. For example, at a switching frequency of 200 kHz, the IMW120R030M1H has the highest total power loss at all currents above 72 A. Table 3.6 below shows an example with input of 150 A load current and 40 kHz switching frequency and shows the 350 mΩ MOSFET has the lowest power losses for the specified application.

Table 3.6 Devices Ordered by Power loss at 150 A and 40 kHz

Device Name	Device No.	I_d per (A)	Power Loss (W)	Cond.Loss (W)	Switch.Loss (W)
IMW120R350M1H	32	4.7	150.8	122.8	28.0
IMW120R060M1H	5	30	231.5	134.6	96.9
IMW120R030M1H	3	50	249.8	112.0	137.8
IMW120R090M1H	6	25	250.1	168.3	81.8
IMW120R220M1H	12	12.5	260.8	205.9	55.0
IMW120R140M1H	8	18.8	263.2	196.5	66.7

However, in many applications using fewer devices is very important for reducing cost and volume. The designer must consider that the device with the lowest power losses may not be the most suitable.

Figure 3.33 presents data for IMW120R030M1H showing that at higher load current, the increased power loss at higher switching frequency is multiplied. This is due to increased switching loss at higher load current, as seen previously in Figure 3.19. Conduction loss will increase with load current but remains almost constant as switching frequency changes. The red line on the plot shows the maximum rated current of the device and the first point that more than one MOSFET is required in parallel to operate at the load current.

Figure 3.34 shows how C_{iss} impacts the power loss as a function of switching frequency at 100 A using the Infineon family data. The switching loss increases with C_{iss}, however at low frequency, the larger the C_{iss} the lower the power loss for the Infineon devices. In devices with higher C_{iss}, as switching frequency increases, power loss increases at a faster rate than those with a lower C_{iss}. Therefore, at 500 kHz, IMW120R030M1H, which has a C_{iss} of 2120 pF, has significantly higher losses than any other device. This process is repeatable for any of the datasheet parameters investigated in this chapter to observe the parameter trends and determine the optimal value for the conditions.

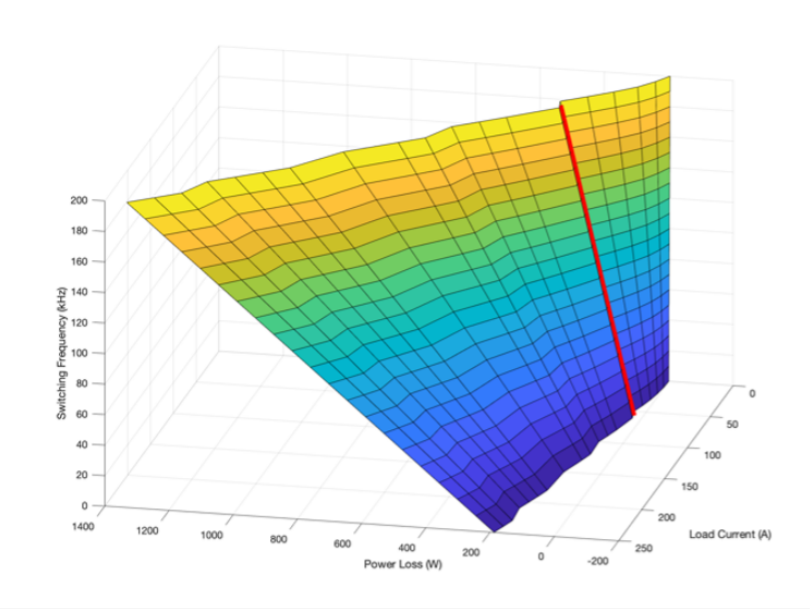


Fig. 3.33 Impact of load current on power losses in the switching frequency range for IMW120R030M1H

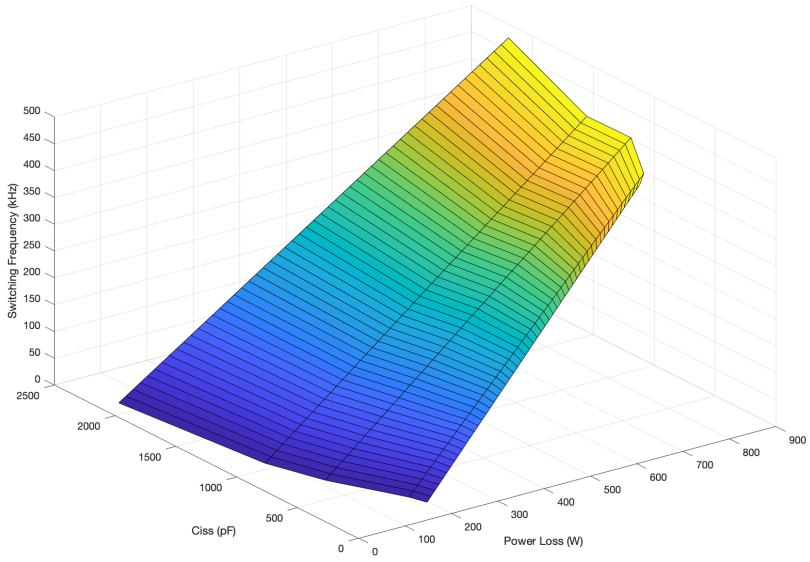


Fig. 3.34 Impact of Input Capacitance Rating on Power Losses at Range of Switching Frequency

3.5.2 Device Family Comparisons

The tool can also be used to predict the behaviour of a MOSFETs from other manufacturers in a manner similar to the calculation of a FOM, but based on experimental data under common conditions. This allows for a more accurate comparison for a specific application, input by the user, including paralleling of devices.

The relationship between C_{iss} and $R_{DS(on)}$ varies between families of devices and can be described by:

$$\alpha = \frac{C_{iss}}{R_{DS(on)}} \tag{3.8}$$

Data indicates α is constant within a family of devices. Therefore, from one device, α can be identified for the entire family. Figure 3.35 shows the relationship between C_{iss} and $1/R_{DS(on)}$ for the MOSFETs and the predicted relationship based on the $R_{DS(on)}$ and C_{iss} of an equivalent set of devices from two alternative manufacturers.

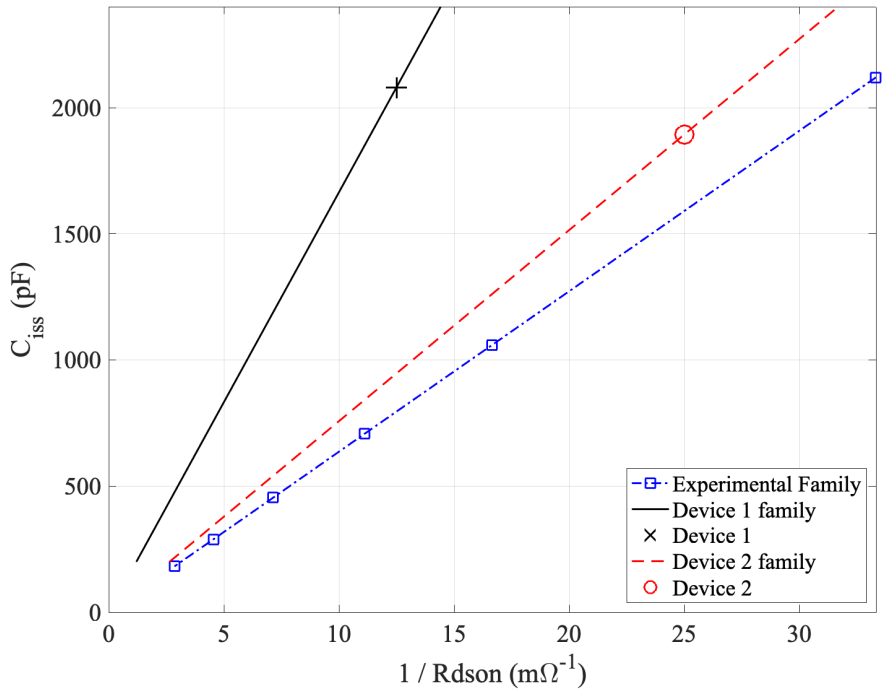


Fig. 3.35 Relationship between C_{iss} and $R_{DS(on)}$ for the Infineon family, and predicted relationships for test devices

The chosen devices and their parameters are shown in Table 3.7. These values for C_{iss}

Table 3.7 Alternative Manufacturer Devices

Manufacturer	Device Name	$R_{DS(on)}$ ($m\Omega$)	C_{iss} (pF)
ROHM	SCT2080K	80	2080
Wolfspeed	C2M0040120D	40	1893

and $R_{DS(on)}$ are then used to predict switching and conduction losses compared to the devices experimentally investigated.

By interpolating the switching energy losses based on the C_{iss} and $R_{DS(on)}$ values, the power loss is calculated using these new switching energy loss values. Figure 3.36 shows the predicted power losses for the Rohm SCT family and the Cree C2M family compared to the Infineon family of SiC MOSFETs. The data shows that the Infineon family is expected to perform with lower losses at the input conditions of 10 A and 100 kHz switching frequency for all devices with similar C_{iss}.

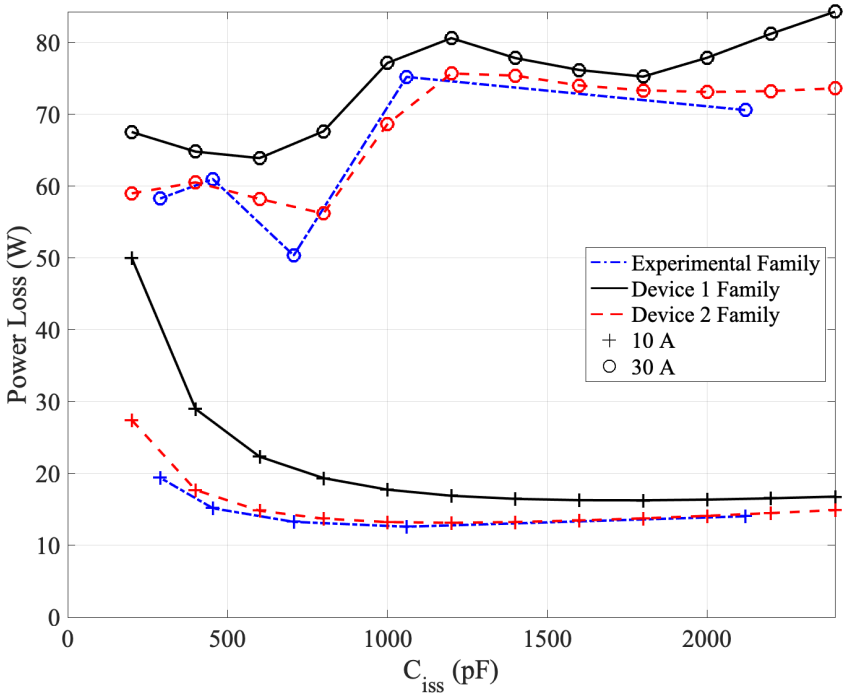


Fig. 3.36 Impact of Input Capacitance Rating on Power Losses for different manufacturers at 10 A and 30 A

However, many of the devices with higher values of C_{iss} in the other device families will operate with a lower power loss under these conditions than the Infineon with low values of C_{iss}. When the devices are considered at 30 A, these relationships change, due to the devices themselves and the required paralleling. This investigation can again be repeated for any of the investigated datasheet parameters instead of C_{iss}, however as has been presented, the relationships between them are linearly proportional so will have the same outcomes as C_{iss}.

3.6 Summary

This chapter has focused on the investigation of the electrical characteristics and device performance parameters of discrete SiC MOSFETs, with a focus on a 1.2 kV Infineon series. The knowledge gained and data presented was used to establish a device selection methodology for any application, but will be used in this thesis as part of the design of an integrated motor drive.

An initial, basic method of device comparison is presented for a range of discrete SiC devices in the form of the FOM, with an Infineon family of devices identified as the most suitable for high-switching-frequency operations, and it was therefore chosen to be investigated further. Several methods for analysing SiC MOSFETs were presented and compared to identify how these approaches can help identify and explain the reasons for the optimal device for an application.

An analytical model built in MATLAB, based on detailed descriptions of MOSFET switching, was presented, allowing the individual and combined effects of the changes in the parameters to be quickly identified and the expected differences in the characteristics of the devices to be theorised. LTspice models were experimentally validated, allowing their use in more complex circuit analysis in future work. The analytical model had an error of 9.8% and the LTspice model had an error of 8.5% when comparing turn-on switching energy from an experimental investigation, showing both are acceptable methods of modelling and analysis.

An experimental investigation of the dynamic characteristics of Infineon SiC MOSFETs is then presented. The impact of internal device characteristics and operating conditions

on device switching speeds, losses, and gate charge is summarised and explained through fundamental theory, as described in the analytical model. The purpose of investigating a single family of MOSFETs was to investigate the combined effect of the differences found between different devices from the same manufacturer. The relationships between datasheet parameters are presented and show that the values of the parasitic capacitances and transconductance have a positive linear relationship with current rating and negative linear relationship with $R_{DS(on)}$.

Finally, the experimental data and device comparisons were presented within a tool for optimising device selection that can be used in a range of circuit applications and conditions. The tool is designed to operate under a range of circuit inputs and therefore is capable of being used in high current systems that require paralleling of multiple devices. It was found that devices with higher $R_{DS(on)}$ have lower switching losses and higher conduction losses; therefore, the device with lowest total losses will be application dependent. Higher $R_{DS(on)}$ devices also have lower current ratings, meaning that for higher currents more devices are needed. The number of devices required and the total power loss are both of interest to designers of power electronic systems. The proposed device selection tool then uses fundamental understanding of the causes of losses within a family of SiC MOSFETs to compare it against devices from other manufacturers. The work chapter addresses the research question of this thesis as the MOSFET selection needs to be understood and optimised in order for the IMD system to be optimal.

Chapter 4

Reliability Optimisation of Integrated Three-Phase Voltage Source Inverter

4.1 Introduction

In this chapter, a system-level multi-objective optimisation has been comprehensively presented to maximise the volumetric power density and lifetime of a compact 60-120 kW inverter that will maximise the potential benefits of both the SiC devices and integrated motor drive (IMD). The device selection tool and the experimentally validated discrete SiC MOSFET models from the previous chapter are used to develop an accurate inverter simulation within Simulink and PLECS.

The individual design of machine components and converters using optimisation-based approaches is becoming more common [116, 103]. There is however a shortage of systematic approaches for the overall system optimisation of SiC-based converters that are computationally efficient and accurate enough to be employed in IMD optimisation [117], which this chapter addresses following on from the work in Chapter 3.

An axial-flux permanent magnet synchronous motor (PMSM) is used as the load within the simulation, and the aim is to design the inverter to operate in the harsh environments of an IMD under normal and peak operating modes for an automotive application. In PMSM drives, the power inverter is the most failure-prone component and in an IMD the power inverter

experiences unusually high thermal stress, so reliability is an important consideration. Recent studies have enabled lifetime modelling of individual discrete SiC devices, and therefore more accurate analysis, if the temperature, current, and voltage behaviour are known [68]

This chapter uses these new models in conjunction with electrothermal simulation software to adapt the converter to the thermal and mechanical demands of an IMD system using a novel multi-objective optimisation of a three-phase SiC-MOSFET automotive inverter, which can significantly increase the volumetric power density and reliability. A particular focus on minimising volume of passive components by increasing the switching frequency operation of the SiC MOSFETs, a detailed electrothermal simulation, and optimisation procedure have been presented.

4.2 Automotive Power-train

In IMD design processes, before physical prototyping and testing, modelling and simulation are required to assess the capabilities of SiC devices within a power train system for a range of operating conditions. The typical design workflow for a SiC power electronic system is shown in Figure 4.1. The flow chart demonstrates how simulation spanning different physical domains is needed and can support important early design decisions. This work focuses on the first four steps of the flowchart. SiC device modelling in Chapter 3 and electrical and thermal simulation and circuit design in this chapter and the rest of the thesis.

This section describes the system-level motor drive model developed for optimisation-based designs. A surface-mounted PMSM is employed to drive the mechanical load, with a two-level voltage-sourced inverter (VSI) for DC-AC power conversion. The model requires inputs for the system, including machine geometrical parameters, converter modulation parameters, and values of passive components. Outputs can be measured and analysed, for example motor-torque, machine and converter efficiency, MOSFET losses, temperature and measurement of current and voltage values.

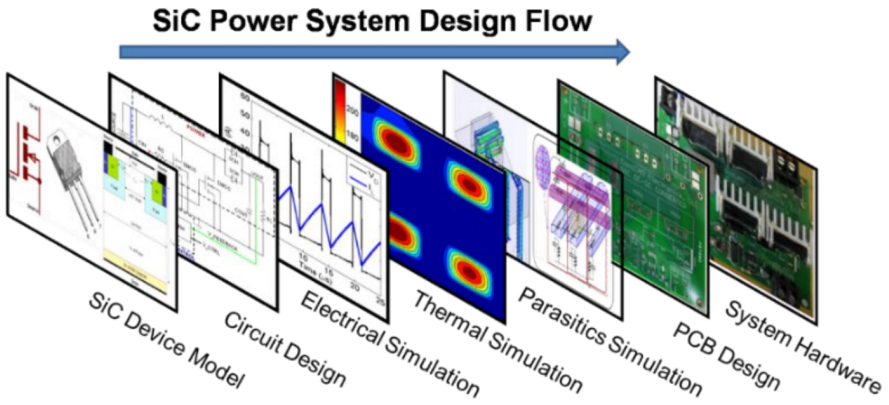


Fig. 4.1 SiC Power System Design Flow Chart [118]

4.2.1 Electrical Simulation Software

PLECS is a simulation platform for power electronic systems used for the modelling and simulation of complete power systems with a comprehensive component library for electrical, magnetic, thermal, and mechanical features of drive systems and control [119]. Importantly, the software allows combined simulations of electrical circuits modelled in PLECS with controls modelled in Simulink and script and tools from MATLAB.

A key part of the electrical simulation software choice is the speed and accuracy of modelling discrete SiC MOSFETs. In PLECS, power losses can be found by using manufacturer-provided look-up tables (LUT) for device thermal analysis and include temperature dependence of the electrical characteristics, for example the on-state resistance, $R_{DS(on)}$. The thermal equivalent circuit for the MOSFET is specified in either Cauer or Foster form in the provided Infineon model, and in PLECS thermal environment the temperature at the case and the junction temperature of the device can be measured.

Use of LUTs and thermal equivalent circuits increases the speed of simulation by up to fifty times compared to a Simulink model with LTSpice device models from the manufacturer. However, unlike the LTSpice and Simulink models, the PLECS device models cannot account for detailed circuit and package stray elements. The device models optimised in Chapter 3 are sufficiently accurate to enable their use in determining the electrical and thermal performance of the inverter. However, a Simulink-LTspice model can be used in conjunction with PLECS

to investigate voltage overshoot and other switching-specific events where appropriate as this analysis is not possible in PLECS simulation but is an important component of inverter design.

4.2.2 Permanent Magnet Synchronous Motor

The electric motor to be used in the holistic power train model is an axial flux permanent magnet synchronous machine, 350 mm in diameter and rated at 65 kW. The motor is designed for automotive applications with the key design parameters shown in Table 4.1.

Table 4.1 PMSM Parameters

Parameter		Value
Stator resistance	R_s ($m\Omega$)	72
D axis stator inductance	L_d (μH)	420
Q axis stator inductance	L_q (μH)	410
Stator leakage inductance	L_σ (μH)	10
Flux induced by magnets	ϕ'_m (Vs)	0.15
Number of pole pairs	p	5

Park's transformation transforms the physical parameters of three-phase machines to the dq rotor reference frame, simplifying analysis of AC systems. However, as the coordinate transformations are based on voltage-controlled current sources, interfacing the dq model with the external three-phase network is a challenge and inductances in the inverter cannot be directly connected to the stator terminals of the motor, reducing accuracy [120]. The two important motor outputs required when designing the IMD, torque and angular acceleration, can be defined by the equations:

$$T_e = \frac{3}{2} p(\phi_d i_q - \phi_q i_d) \tag{4.1}$$

$$\dot{\omega}_m = \frac{1}{J}(T_e - F\omega_m - T_m) \tag{4.2}$$

where T_e is the electromagnetic torque, ϕ_d and ϕ_q are the d and q axis flux and i_d, which is zero for a PMSM, and i_q are the flux current of the d and q axes of the rotor. J is the load

inertia, F is the friction constant, ω_m is the mechanical speed of the rotor and T_m is the load torque.

The PMSM model allows the user to observe in real time, the stator phase currents, stator flux (d and q), rotational speed, rotor position and electrical torque.

A forced cooling system runs water through the motors outer casing to cool the stators and due to the shared contact with the power electronics, this will determine the thermal environment and heat sink temperature of the inverter components in the simulation.

4.2.3 Busbars

The high current capability and power density of busbars makes them an attractive option for high-power inverters compared to printed circuit boards (PCB) or wired systems. However, they add complexity to the system and component dimensions, the thermal management system, the current density, and the operating environment need to be considered in busbar design. In this section, only parasitic inductance is considered due to its relevance of the interaction with SiC devices and other components on the powertrain.

The inverter DC bus voltage and aspects of PWM control, for example switching frequency and dead time, are restricted by the voltage overshoot resulting from the energy stored in the parasitic inductance of the busbar during MOSFET switching [121]. This parasitic inductance, L_σ, combined with current slew rate, di/dt, affects the power device voltage overshoot, which adds to the DC bus voltage, V_{bus}.

$$\Delta V_{overshoot} = -L_\sigma \frac{di}{dt} \tag{4.3}$$

This can constrain V_{bus} as it must be strictly less than the device rating:

$$V_{bus} + \Delta v_{0-peak} + \Delta V_{overshoot} \leq V_{rated} \tag{4.4}$$

where, Δv_{0-peak} is the maximum ripple of the DC voltage resulting from the AC current interacting with the equivalent series resistance (ESR) of the capacitor bank.

To limit the voltage overshoot, the current of the device must also be limited or slowed during turn-off to limit di/dt. This results in additional switching losses, having a negative effect on the device thermally and the overall system efficiency. Therefore, minimising the parasitic inductance of the laminated DC bus structure is important when designing inverters that contain SiC MOSFETs if they are to operate with high performance.

Overshoot Analysis

Due to the limitations of PLECS device modelling, the voltage overshoot in the simulation was analysed using LTspice MOSFET models within a Simulink circuit. The same circuit, control, and load were set up in Simulink with the MOSFET models imported. The package parasitic inductances and capacitances of the TO-247 detailed in Chapter 3, were included in the device models, allowing the maximum voltage overshoot during operation to be investigated. This combination of simulation software packages enables fast overall optimisation with higher accuracy compared to using only the PLECS-Simulink simulation or analytical methods, and is an important new consideration for IMD design optimisation, shown in Figure 4.6.

The voltage overshoot described in equation 4.3 and depends on the busbar design and the current slew rate, di/dt, which is dependent on the gate resistor, R_G, as described in Chapter 3.

Simulations allowed the evaluation of a range of circuit inductances and gate resistor values and it was found that using an R_G of 5 $m\Omega$, busbar inductance of 30 mΩ, and any loop inductance below 50 nH, which match with recent inverter design studies [122, 121], meant the voltage overshoot for a DC voltage value of 650 V was far below the 1200 V rating of the SiC MOSFETs used in the IMD. Hence, this was not considered necessary for further consideration in this design. Considerations of overshoots in designs using higher DC voltages is possible with this methodology, but is beyond the scope of this thesis.

4.2.4 Control System

Control of the system was based on Direct Flux Vector Control (DFVC) as proposed in [123]. DFVC operates in a synchronous frame aligned with the stator flux, where flux and torque are controlled directly by means of two basic PI regulators. The input to the control system in the IMD analysis is the required motor torque, with the speed dependent on the load conditions and inertia. Space Vector Pulse Width Modulation (SVPWM) is used, as despite its more intensive computational requirements, can achieve better performance by generating reduced THD compared to sine pulse width modulation (SPWM), improving the efficiency of the inverter and the PMSM.

4.3 Inverter Design

The focus on converters that are smaller, more efficient, and have higher power density has resulted in rapid advancements in converter technologies. An IMD system design process allows for an optimum motor-inverter matching in order to maximise the advantages of SiC devices. Only discrete semiconductor devices are considered due to a greater design flexibility, and a higher general availability than SiC modules. Together, inverter and thermal management targets lead to a challenging multi-domain system-level optimisation problem.

The inverter components in an IMDs are required to operate with high lifetime, efficiency and power in an extreme thermal, mechanical and electrical environment. The high-temperature environment due to the close proximity of the converter to heat sources such as the stator windings leads to complications in cooling and thermal management. Using high-temperature devices, such as the discrete SiC devices studied previously, will allow better performance and reliability in harsh environments in an IMD. The fast switching speed and low switching losses of SiC can reduce the volume of the passives, increasing the power density [124, 21]. However, the high dv/dt and di/dt during the switching transient may lead to severe electromagnetic interference (EMI) issues and can result in device failure [125].

The high switching speed of the SiC devices also poses thermal challenges. In the IMD to be investigated, a singular cooling system is adopted as the housing area is used as a heat sink for the converter. Localised high temperatures caused by MOSFET power losses, and thermal cycling at the device junction will significantly affect the reliability of the system so thermal management is a crucial part of IMD design. Vibration and mechanical stability also create issues with reliability and will be considered in the design process, but will not be the focus of this project [17, 37].

4.3.1 Device Selection

In Chapter 3 the device selection tool (DST) was developed to choose which of the Infineon series of devices was optimal in a specific application. It is possible to use this within a design optimisation, as each iteration has a specific load current, switching frequency, and environment temperature.

The tool determines the minimum number of paralleled devices required for the circuits load current based on the rated current of the MOSFETs from the manufacturer datasheet. Increasing the number of devices negatively impacts the volumetric power density, so, for this application, there has to be a trade-off between the number of devices and the losses. The higher switching losses of a low $R_{DS(on)}$ device that arise from the input capacitance may limit the switching frequency and therefore result in a larger DC-link capacitor so the overall inverter volume will increase.

In the optimisation, the switching frequency is to be varied, so a range is considered within the DST. The results of the tool for normal (130 A max. current) and peak operation (310 A max. current), at switching frequencies of 10 and 200 kHz are shown in Tables 4.2 and 4.3.

Using this data, the 30 $m\Omega$ device was chosen for the optimisation design. The power losses are only marginally higher than for the 60 $m\Omega$ devices across the range of frequencies studied here. It is worth noting the total number of MOSFETs for the inverter is six times the paralleling number. So using the 30 $m\Omega$ devices instead of the lower loss 90 $m\Omega$ devices requires 36 fewer MOSFETs, significantly reducing inverter volume. Using fewer

Table 4.2 Required paralleled device numbers and power losses using the DST at normal operation for min. and max. switching frequency

$R_{DS(on)}$(mΩ)	**Device no.**	$I_{D(rtd)}$(A)	**Loss** (W):	10kHz	200kHz
30	3	56		24	449
60	4	36		26	440
90	5	26		26	406
140	7	19		25	319
220	10	13		28	290

Table 4.3 Required paralleled device numbers and power losses using the DST at peak operation for min. and max. switching frequency

$R_{DS(on)}$(mΩ)	**Device no.**	$I_{D(rtd)}$(A)	**Loss** (W):	10kHz	200kHz
30	6	56		58	1071
60	9	36		61	1049
90	12	26		61	963
140	17	19		59	762
220	24	13		67	688

devices with individually greater losses will lead to a more challenging design environment, highlighting the need for optimisation of the design.

Because the inverter needs to operate under both normal and peak conditions, the DST suggests different required numbers of devices for each operating point. As the MOSFETs can operate above their rated values, although at an inferior level of performance, the optimal number may lie between the two. Changing the number of paralleled devices will be investigated later using the optimisation tool.

4.3.2 DC-link Capacitor

In conventional hard-switching three-phase inverters, the DC-link capacitor is required to protect both the battery and the power devices from large current and voltage spikes. The DC-link capacitance should be sufficient to mitigate the voltage ripple to the constraint set in the optimisation, in this study 1%, by providing a low impedance path for the ripple currents associated with a hard-switched inverter. The voltage ripple is caused by the pulsating current at the switching frequency which results in high-frequency voltage ripple. The value of this

ripple is linearly proportional to the switching frequency, output current amplitude and also related to the modulation method, modulation ratio, and load power factor. Unbalanced three-phase loads will also cause second harmonics on the DC-link voltage [126].

The DC-link capacitor occupies a significant amount of space in the inverter and 30% of the failures in PE systems are due to capacitor failure [17], therefore, capacitor selection will significantly affect the system power density and reliability.

Capacitor Type

In general, capacitors used in power electronics applications are usually electrolytic, metallised polypropylene film (MPPF), or ceramic. To fully utilise the high temperature performance of SiC MOSFETs, all of the components in the inverter must be tolerant to high temperatures.

Film capacitors combine the advantages of low losses and mechanical robustness with high volume capacitance, resulting in a more power-dense option. They also exhibit a longer lifetime and a higher ripple current capability than electrolytic capacitors [77]. MPPF capacitors exhibit a low equivalent series resistance (ESR) and low capacitance per unit volume and are therefore limited by the voltage ripple requirement, not by the ripple current rating [43]. Therefore, the amount of capacitance needed is lower for a film capacitor system, resulting in a lower volume solution.

Ceramic are suited to high-temperature and high-voltage applications [80], however, have high cost and brittle characteristics making them unsuitable for IMD traction applications where shock and vibration are prominent. Therefore, film capacitors will be used in the IMD system designed in this project.

KEMET are a leading capacitor manufacturer and have a series of automotive grade, radial film capacitors for DC-link applications which will be considered in this study. The datasheets for the C4AQ, C4AQ-M and C4AQ-P series were analysed as shown in Figure 4.2 [127]. It was important to fit trend lines that produce expected values for any capacitance value for each series so that any theoretical equivalent series resistance, ESR, thermal resistance, R_{th}, volume, and weight can be used within the optimisation.

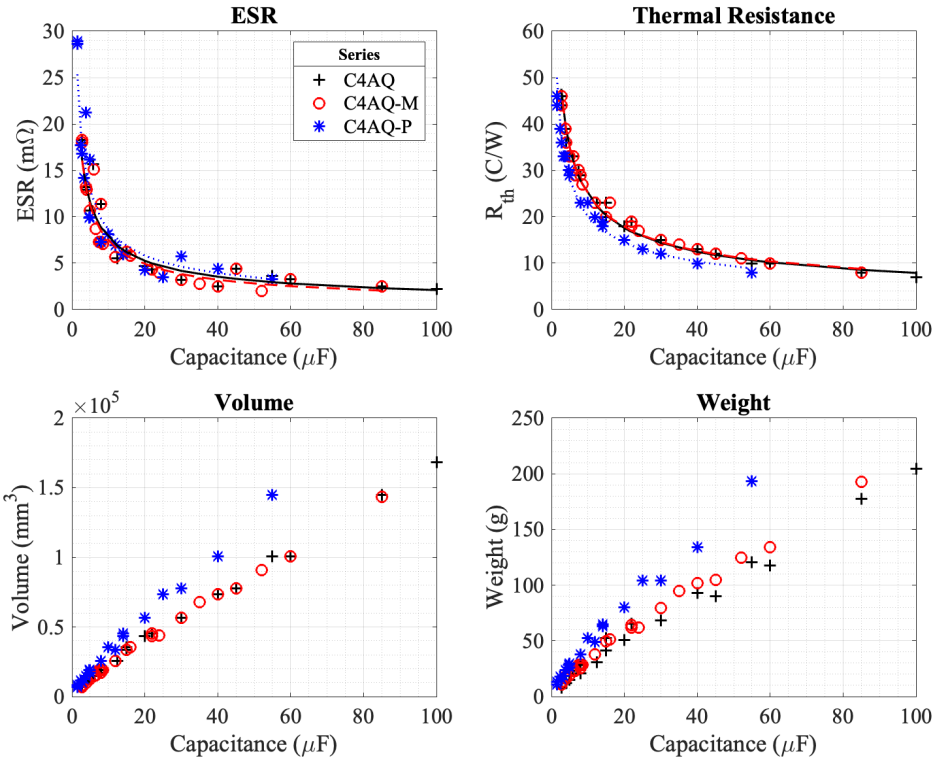


Fig. 4.2 ESR, thermal resistance, volume and weight as a function of capacitance for three different KEMET capacitor series

The C4AQ-P series is suited for high reliability systems, however it has a larger volume and weight so is not ideal for IMDs and the C4AQ series was taken forward in the analysis. The MOSFETs are the inverter component most prone to failure, so the volume of the capacitors is considered its most important parameter.

Operation

Although several studies have been conducted on the high temperature performance of SiC power devices, passive components capable of withstanding such temperatures have received relatively little attention. When considering the behaviour of a capacitor within the IMD system, there are two important considerations: the capacitor hot spot temperature and the lifetime. Equation 4.5 can be used to estimate the internal power loss of the capacitor.

$$P = I_{C(RMS)}^2 R_{ESR} \tag{4.5}$$

where $I_{C(RMS)}$ is the RMS current of the capacitor and R_{ESR} is the ESR of the capacitor. In general, the ESR is related to the current ripple frequency, and a higher current ripple frequency gives a lower ESR. However, at the frequencies considered in this design, the ESR can be considered to be constant.

The power losses within the capacitor increase the temperature as described in 4.6:

$$C_{ths} = T_a + P.R_{th,c-a} \tag{4.6}$$

where C_{ths} is the capacitor hot spot temperature, T_a is the ambient temperature, $R_{th,c-a}$ is the thermal resistance between the capacitor and the ambient temperature.

Sizing

The fundamental parameters affecting the size of a DC-link film capacitor are DC voltage requirement, the capacitance requirement due to voltage ripple, and RMS current rating requirement to achieve the desired current ripple. It is assumed in this study that the voltage ripple is the limiting design variable, not the current ripple limit of the DC-link capacitor as in electrolytic capacitors.

To determine the voltage ripple, ΔV_{pp}, the input current switching frequency component, which circulates through the DC-link capacitor, C, must be estimated. Assuming that capacitive reactance dominates the equivalent DC-link impedance, the whole current component ΔI circulates through the DC-link capacitor. In this case, the change in the corresponding DC voltage can be determined by integrating ΔI over the specific application time interval t_{pp}, determined by space vector pulse width modulation (SVPWM) and inversely proportional to the switching frequency. An effective simplification is obtained [128] assuming that Δi is constant within the application time interval, leading to:

$$\Delta V_{pp} = \frac{1}{C}|\Delta I|t_{pp} \tag{4.7}$$

where t_{pp} is the specific application time interval determined by the space vector equations and is inversely proportional to the switching frequency, f_{sw}.

The DC-link capacitance required to limit voltage ripple to 1% can be determined analytically. According to [128], for a film capacitor, the theoretical minimum DC-link capacitance, C_{min}, can be calculated using Equation 4.8.

$$C_{min} \geq \frac{I_0}{4 f_{sw} \Delta V_{pp}} \tag{4.8}$$

where I_0 is the output current amplitude.

The DC-link capacitance, which is proportional to the volume, is used as a design variable that should be minimised to increase the volumetric power density of the inverter. To support the calculations using equation 4.8 the power train simulation in PLECS will be used to determine the voltage ripple over a range of switching frequencies for the DC-link capacitance values studied. This will be part of the optimisation study to find the minimum required DC-link capacitance by identifying a switching frequency that meets the circuit design constraints, including a limit on the voltage ripple.

Paralleling

In many applications, it is beneficial to use a capacitor bank, a grouping of several capacitors of the same rating connected in series or parallel, instead of a single component. The effective ESR of the capacitor bank can be reduced which will reduce the power loss and therefore the C_{ths} of the capacitors. The physical constraints of the busbar or IMD enclosure may also allow multiple small parts to fit where a single large part will not, increasing the volumetric power density of the system. Using multiple smaller capacitors also improves the design flexibility, much like using discrete semiconductors instead of a power module.

The data shown in Figure4.2 shows that increasing the number of capacitors will reduce the ESR and therefore the C_{ths} but will increase the weight and volume, although it will reduce the capacitor height, so there is a trade-off to be considered.

4.3.3 Inverter Volume

The volume of the inverter not only depends on the volume of the individual components but also the physical layout and design of the system. The IMD in this project will be designed to fit on the 350 mm diameter plate of the PMSM. The aim is to therefore reduce the height required for the components to minimise the total volume of the system as the diameter is set. The component that will determine the height in an IMD is the DC-link capacitor, as the MOSFETs will be mounted directly to the cooling plate of the motor. However, the number of devices, which each have a volume of 1680 mm^3 and weight of 6 g, must also be considered as a factor that affects the total volume and weight of the IMD. Therefore, although perhaps not reflective of the true volume, in this chapter, the volume will be calculated as a sum of the capacitor volumes and the total MOSFET volume.

4.4 IMD Reliability Analysis

The general definition of reliability in engineering, as described in Chapter 2, is the probability that an item will perform a required function without failure under stated conditions for a specified period of time. In this work the reliability of the inverter is determined by its ability to maintain operation at the stress conditions defined in the inverter optimisation.

Failure analysis of PMSM drives shows that the power inverter is the most prone part to failure. 56% of drive failures are due to inverter faults [129] where PMSM drives in vehicles are considered. A questionnaire study reports 30% and 17.5% failure rates due to semiconductor devices and DC-link capacitors faults respectively, while also highlighting that in motor drive applications semiconductor devices are the most fragile components [86]. These values will increase substantially in IMDs because of the extreme environments and high temperatures the power electronics operate under. Reliability is often determined by semiconductor devices, although the capacitor is also considered in this system-level design study.

4.4.1 Semiconductor Device Lifetime Models

The literature is often critical of reliability handbooks, for example, MIL-HDBK-217 [90], because the lifetime prediction results are typically negative and these methods do not consider thermal cycling, which has been determined to be a crucial aspect of lifetime analysis.

Any empirical lifetime model based on power cycling testing will reflect the characteristics of the specific device type used in the study. The results of the development of a lifetime model for the TO-247 package using Infineon IGBTs were first investigated recently in [71]. The study found that the cause of failure was due to the bond wires in the device package, making the lifetime prediction model applicable to SiC discrete MOSFETs in the TO-247 package. From the power cycling results, the lifetime model, giving the number of cycles to failure, N_f, was calculated:

$$N_f = K.\Delta T_j^{\alpha}.e^{E_A/k.T_{jm}}.t_{on}^{\beta}.I_b^{\gamma} \tag{4.9}$$

where K is the basic constant, α is the Coffin-Manson exponent, ΔT_j is the junction temperature swing, E_A is the activation energy, k is the Boltzmann constant, $T_{j(mean)}$ is the mean junction temperature in Kelvin, β is the exponent for the duration of the load pulse, t_{on}, and γ is the exponent for the current per bond I_b.

Using the values in Table 4.4 from the study, allows for the first time the lifetime analysis of discrete TO-247 devices within a power train system, an important novel approach of this thesis. The Coffin-Manson exponent α is in a comparative range of the values from other publications [71] but the activation energy, E_A, was found to be higher in the TO-247 package than for power modules from recent publications. It can be seen from equation 4.9 that the mean junction temperature of the device and the junction temperature swing are critical parameters required for lifetime predictions. The current per bond wire is of interest as it will increase the junction temperature characteristics and also directly reduces the N_f, paralleling the MOSFETs will therefore increase the lifetime of the system.

Table 4.4 Summary of parameters in proposed lifetime model for TO-247 package [71]

Parameter	Symbol	TO-247
Basic constant	K	$4.0x10^{13}$
Coffin-Manson exponent	α	-3.75
Activation energy	E_A	0.168 eV
Exponent for t_{on} (1 s - 15 s)	β	-0.466
Exponent for I_b	γ	-2.36

The study shows that N_f is independent of values below 1s constant load pulse, t_{on}, so this variable and β will not be considered. In the optimisation, the PLECS electrothermal simulation determines the temperature profile of a device before the effect on lifetime of a particular operating point is evaluated.

4.4.2 DC-link Capacitor Reliability

The allowable operating temperature of film capacitors is usually referenced by the manufacturer. However as explained in [128] the working temperature has a significant influence on the lifetime of a film capacitor. The most widely used empirical model for an MPPF capacitor lifetime is described as follows [130]:

$$L = L_0 . \left(\frac{V}{V_0}\right)^{-n} .2^{\frac{T_0 - T}{10}} \tag{4.10}$$

where L is the lifetime, L_0 is the lifetime under test conditions, V is the voltage and V_0 is the applied voltage under test conditions, T is the core temperature and T_0 is the core temperature under test conditions. The voltage stress factor, n, is between 7 to 9.4 for leading film capacitor manufacturers [131]. The equation describes how the lifetime of an MPPF capacitor is dependent on both the applied voltage and core temperature.

Many manufacturers, including KEMET, provide graphical lifetime data for a capacitor in the form of the expected hours of operation before failure based on maximum voltage across the DC-link and the hotspot temperature, C_{ths}, from equation 4.6. These can be used instead of equation 4.10. An example plot is provided in Figure 4.3.

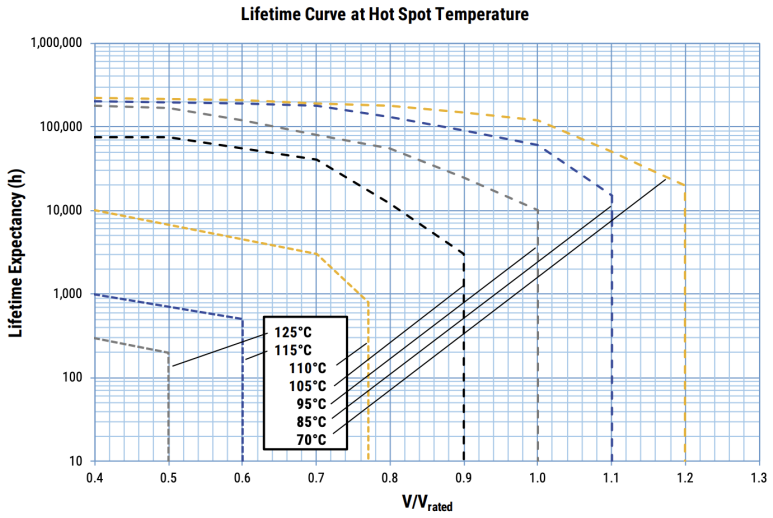


Fig. 4.3 Example capacitor lifetime expectancy data for KEMET C4AQ series [127]

As seen, the lifetime of an MPPF capacitor is greatly affected by the applied voltage, and the higher the applied voltage, the faster the decrease in the capacitor lifetime. The core temperature is directly related to the power dissipated, as described in equation 4.6, therefore reducing the current ripple in the DC-link capacitor current ripple or ESR of the capacitor results in a hugely increased capacitor lifetime.

It is worth noting that the thermal resistance of capacitors changes slightly with the core temperature, and the ESR is not fixed at different current harmonic frequencies and will increase during the degradation process. The data needed to consider these factors is also provided by KEMET and the thermal resistance change will be factored in to the calculations. However, for this study as the frequencies below 250 kHz the ESR can be considered constant.

4.5 Design Optimisation Procedure

For the complex multi-physics operation of IMDs, traditional design approaches use generic sizing equations that make significant simplifications and assumptions. These approaches can make it difficult to determine the optimal design when all the competing design criteria and interconnected component and circuit parameter relationships are considered. The

optimisation-based design approach is employed directly to the design environment using modern algorithms, to form an input-output problem, as illustrated in Figure 4.4 for an optimisation with two objective functions. A Pareto front represents the set of optimal solutions in a multi-objective optimisation problem where improving one objective inevitably leads to a trade-off with the other objective [132]. Equivalent results using traditional approaches would significantly increase time and limit accuracy.

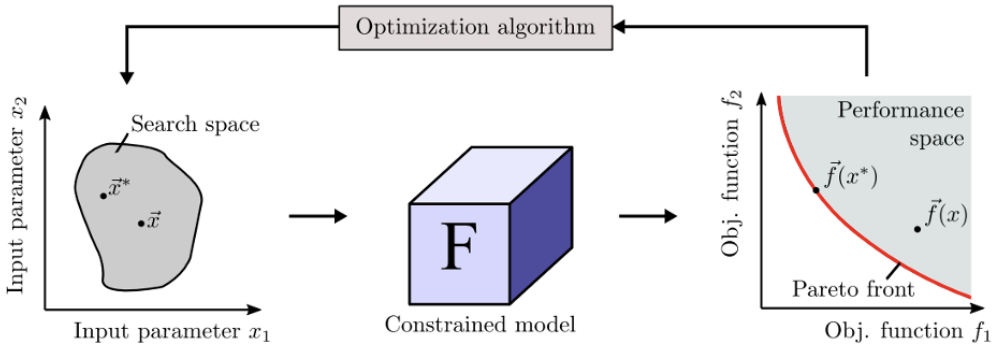


Fig. 4.4 Illustration of an optimisation-based design where complex models map a set of design variables from search space onto the design function space [133]

In recent literature for inverter design, optimisation combines interdependent component models, each of which are responsible for selecting and optimising a specific component of the converter [101]. An optimisation of the design of motor drives at the system level that considers all components specifications and constraints in combination will be essential. Through use of the automotive power train modelling, the complete power train simulation can be included in the optimisation model and the interdependencies between various components and machine-converter interactions can be observed and considered in the design.

4.5.1 Algorithm and Optimisation Tool

Optimisation techniques are used to find the optimal design parameters for a specified objective under a range of constraints. For example, the minimisation or maximisation of an objective function $f(x)$ which is dependent on system characteristics that are subjected to equality constraints, inequality constraints, or parameter bounds [134]. Deterministic

or gradient-based algorithms, illustrated in Figure 4.5 are very powerful tools for quickly analysing large design spaces with multiple constraints in a short amount of time, and are therefore suited to the complex multi-physics design of an IMD.

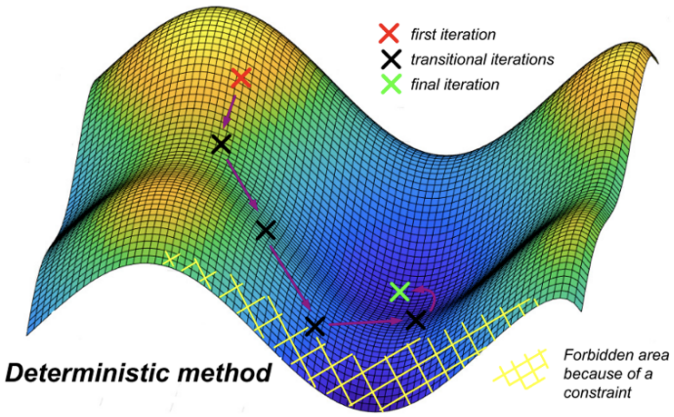


Fig. 4.5 Illustration of optimisation with a deterministic algorithm [116]

Computing the gradients of the system allows the algorithm to ignore solutions outside the bounds of the set constraints and converge quickly to the optimal solution. However, the solver in deterministic algorithms can become trapped in local optima so a multi-start procedure can be added to automatically change the starting point of the optimisation in cases where the result is highly sensitive to the initial conditions.

A sequential quadratic programming (SQP) method [135], a type of deterministic algorithm, was used to solve the global inverter design problem. SQP methods are available in the MATLAB optimisation toolbox and are a popular, state-of-the-art nonlinear programming method. The algorithm gives a theoretical optimum which is very useful in early-stage design as it allows fast and effective comparison of optimal designs [116].

A simplified flow diagram of the optimisation process is shown in Figure 4.6.

The mission profile, specified by the load torque and speed at normal and peak operation in this study, need to be defined by the user as the inputs to the model and the optimisation algorithm begins with the initial values of switching frequency, f_{sw}, and DC-link capacitance. The PLECS model simulates the conditions at steady state, outputting the electrothermal behaviour of the inverter and MOSFETs. If the user-defined constraints are all satisfied

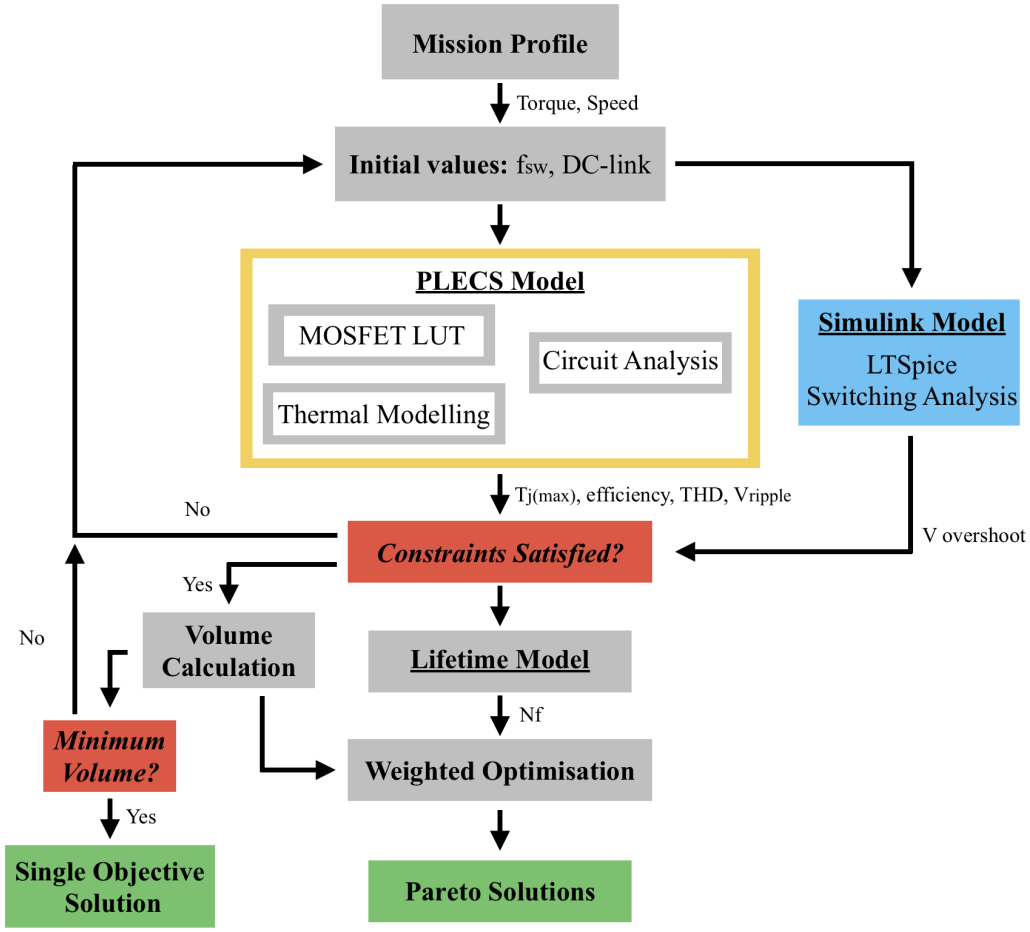


Fig. 4.6 Flow chart of the optimisation algorithm

the algorithm then runs the same conditions in the Simulink model to ensure the voltage overshoot, V_{os}, is also at an acceptable level. If the design does not meet the requirements, the process restarts with new values of f_{sw} and DC-link capacitance.

The next steps depend on the objective of the optimisation. It is possible to use the algorithm to minimise volume or provide a solution range that considers lifetime as well. For the single-objective process, if the design is feasible then the volume is calculated based on the number of MOSFETs and DC-link capacitance. The algorithm then uses the SQP algorithm to iterate through the design space and determine if the solution is optimal and the input conditions provide the smallest volume inverter that meets the set constraints.

For a multi-objective optimisation, a lifetime prediction is made based on the current and thermal conditions of the MOSFETs before a weighted optimisation procedure using the calculated volume and number of cycles to failure, N_f, is repeated to find the Pareto front that represents the optimal solutions for the design.

4.5.2 Operating Conditions

PMSMs operate in four modes, as shown in Figure 4.7 [22]. These are known as the maximum torque per ampere region (MTPA), region I, the field weakening region without and with torque reduction, regions II and III, respectively, and the maximum torque per volt region (MTPV), region IV. This study focuses on testing the inverter while the motor is operating in the MTPA region, as this is region is of particular interest when operating efficient motor drives [136].

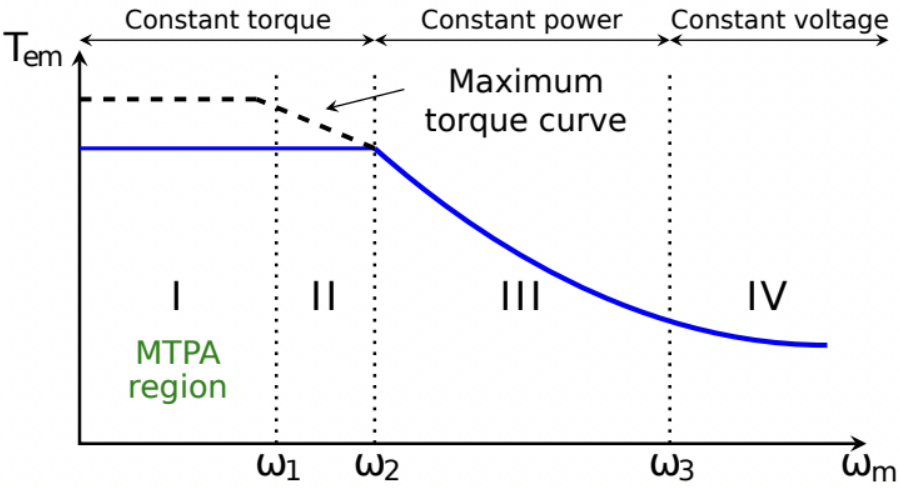


Fig. 4.7 Torque vs speed curve and operating regions of PMSMs [22]

In PMSM design the motor is tested at 'normal' and 'peak' conditions by the manufacturer to judge performance. Figure 4.8 shows the maximum torque curve of the PMSM in the IMD for normal and peak operation.

The highlighted points on the curves represent the MTPA point for the maximum torque curves. This is the point of maximum I_q current and therefore the maximum current stress for the inverter, so is a good test condition for the system. The inverter will be designed for both

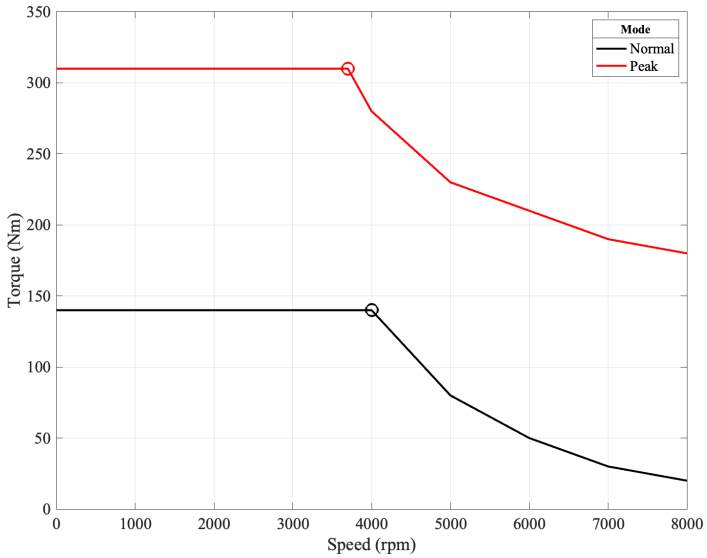


Fig. 4.8 PMSM Torque-Speed data for different Operating Modes

the normal and peak operating modes in this thesis, with the conditions determined using experimental motor data illustrated in Figure 4.8 and are detailed in Table 4.5.

Table 4.5 PMSM Operating Conditions

Operating Mode	**Normal**	**Peak**
Speed (rpm)	4000	3700
Torque (Nm)	140	310

In this design it was assumed the system would be operating under peak conditions 10% of the time. Using two conditions instead of a drive cycle is a common method in industry for testing traction machines and significantly speeds up the optimisation process. In the New European Drive Cycle (NEDC) the ratio of urban to highway driving is 4:1 with approximately 10% of the drive cycle at speeds greater than 70 km/hour.

4.5.3 Design Parameters and Constraints

The design parameters are the variables that define each version of the system and are modified during an optimisation process to achieve better fitness function values while meeting the problem constraints. In this study, the switching frequency and DC-link capacitance are

set as the design parameters and limits are set to restrict the solutions from the optimisation to those that are feasible.

To perform an optimisation run, the design specifications must first be set, including the PMSM and inverter power ratings, input voltages and temperature limits. In the case of automotive inverter optimisation, constraints on the inverter efficiency, the quality of output power and input voltage are required. If it is not possible to meet the constraints, the optimisation was setup to identify the design-limiting parameters to allow investigation and design improvement where possible. The design constraints in the optimisation problem are described in Table 4.6.

Table 4.6 Design Example Specification and Constraints

Specification	**Normal Operation**	**Peak Operation**
Rated Power	60 kW	120 kW
DC-link Voltage (V_{dc})	650 V	650 V
Maximum Junction temperature	175°C	175°C
Ambient temperature	70°C	70°C
Max. DC-link voltage ripple(ΔV_{dc})	1% of V_{dc}	2% of V_{dc}
THD limit	5%	10%
Minimum converter efficiency(η)	98.5%	97.5%

The THD of the current is a measure of the quality and the harmonic content of the current waveform relative to the fundamental frequency. Low THD in power systems can mean lower peak current and higher efficiency. There are international standards, for example the IEC 61000-3-2 for setting THD limits on various classes of power equipment.

In literature the DC-link voltage ripple limit for inverter design is usually between 0.5 [137] and 10 % [108] of the V_{dc}, with the EV optimisation in [100] using a limit of 2.5 %. High voltage ripple causes the DC-link capacitor and battery to deteriorate faster so a limit of 1% has been employed in this optimisation to maximise reliability. Additional optimisations can then be used to investigate further design parameters, for example, the number of paralleled devices in each inverter leg and the heat sink temperature.

4.6 Volumetric Power Density Optimisation

Firstly, with the aid of the optimisation tool, the DC to three-phase AC, 2-level converter design can be optimised to maximise the volumetric power density. To optimise the volumetric power density of the SiC inverter, design trade-offs among various components and subsystems have first been identified. Subsequently, the electrical and thermal domain interface interactions must be carefully considered because of the inherent coupling.

Optimal component selection, including the number of switching devices and the selection of the DC-link capacitor is the most critical factor when designing for improved volumetric power density. As discussed, the capacitor makes up a large volume of the inverter so minimising the capacitance while meeting the circuit constraints will lead to an inverter with higher volumetric power density. SiC MOSFETs increase the potential switching frequency range so determining the optimal switching frequency from the system power density perspective becomes an interesting design study. In this work the optimisation result is a theoretical optimum, that is to say the selection of components may not be possible with what is currently available to purchase, which allows fair and quick comparison of solutions, although it will not be necessarily possible using manufacturer components.

4.6.1 Effect of Switching Frequency on Inverter Operation

Variations in voltage ripple, ΔV_{pp}, total current harmonic distortion (THD), maximum junction temperature of SiC MOSFETs, $T_{j(max)}$, inverter efficiency, lifetime, capacitor hot spot temperature, C_{ths}, and inverter power loss with switching frequency f_{sw}, are shown in Figure 4.9 for normal and Figure 4.10 for peak operation for a circuit with 6 parallel MOSFETs. The data shows the impact of switching frequencies between 10 and 200 kHz and DC-link capacitor values between 50 and 750 μF. The black lines on each plot show the optimisation constraints to give an initial idea of the design variables that meet the circuit constraints and identify which parameters become limiting factors in the designs.

At any given frequency, the data shows significantly different values between the normal and peak operating conditions for all the circuit characteristics investigated. However, the

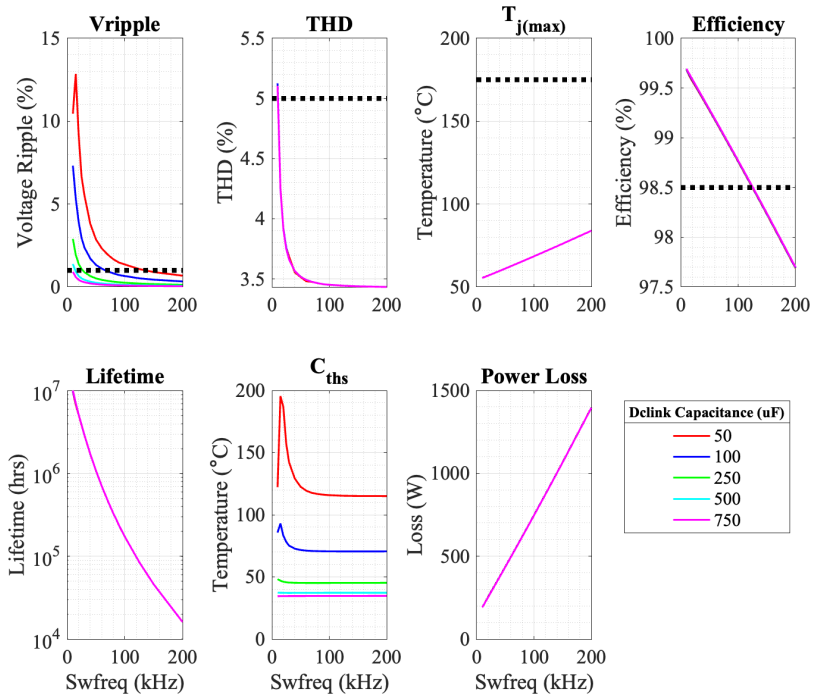


Fig. 4.9 Inverter parameters as functions of switching frequency with increasing DC-link capacitance under normal conditions

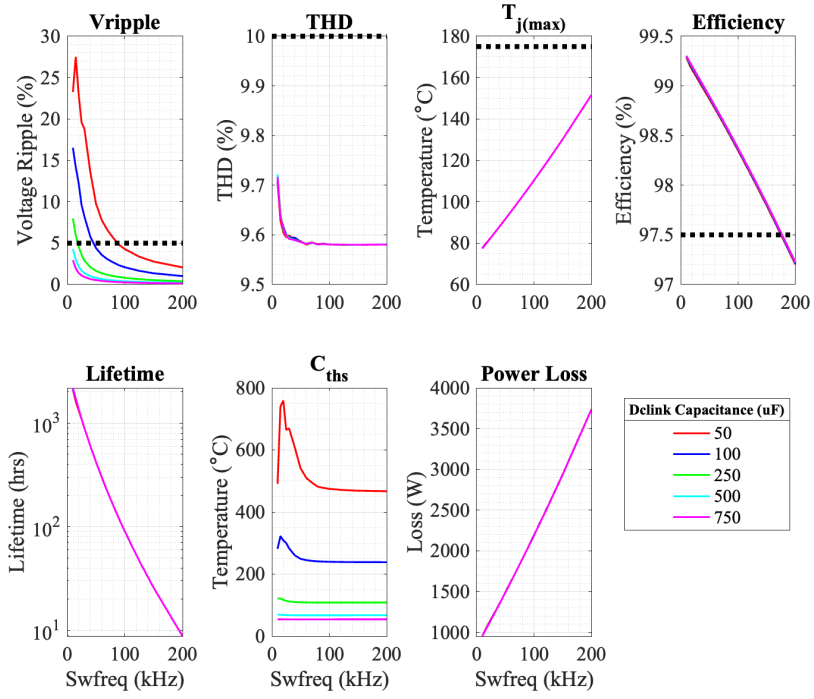


Fig. 4.10 Inverter parameters as functions of switching frequency with increasing DC-link capacitance under peak conditions

relationships between the variables to the switching frequency and the values of the DC-link capacitor are the same. The voltage ripple decreases as the switching frequency increases, and this effect is more severe with smaller DC-link capacitors. This can be explained by equation 4.7 as the SVPWM specific application time interval, t_{pp}, which is inversely proportional to f_{sw} [138]. The relationship is not linear and for capacitor values above 250 μF an increase in switching frequency above 100 kHz has minimal effect on voltage ripple. This means that increasing f_{sw} does not provide significant further volume reduction above 100 kHz, where the effect of f_{sw} on THD also saturates. At higher frequencies the current THD will be driven by the motor inductance, speed, and back emf and the DC-link electrical parameters. Above 12 kHz, under normal operation the minimum THD value is 3.5 % and at peak it is 9.6 % which is due to higher currents in the circuit. This determines the lower f_{sw} limit for the inverter design and ensures the motor is protected from damage from the inverter output waveforms.

The data show that efficiency is inversely proportional to the switching frequency, due to the linear increase in total power loss resulting from the increases in switching loss. These losses also increase the maximum junction temperature, $T_{j(max)}$, but are not sufficient at any frequency for the junction temperature to exceed the limit of 175°C. $T_{j(max)}$, efficiency, and power losses have linear relationships with the switching frequency, with negligible differences when using a larger DC-link capacitor.

The only other variable significantly impacted by changes in the DC-link capacitor is the C_{ths} which decreases for higher values of capacitance. This can be explained by the inversely proportional relationship between capacitance and ESR, as shown by the data in Figure 4.2. Capacitors with lower capacitance values have a higher ESR and, therefore, experience greater internal losses resulting in a higher C_{ths}. For small DC-link capacitors resonance occurs across the inductance of the DC busbar resulting in extremely high capacitor currents at low switching frequencies resulting in abnormally high C_{ths}. At higher f_{sw}, this resonance, as well as any further effects of f_{sw} on the C_{ths} is insignificant, especially for high DC-link values.

Lifetime is presented in terms of hours of operation and the lifetime of the SiC devices is assumed to represent the lifetime of the system as they are components most prone to failure. This is calculated using equation 4.9 and the measured temperatures and current of MOSFETs studied in the IMD simulation. N_f can then be converted into hours of operation by measuring the time of a single temperature cycle, with a frequency of 50 Hz for this study.

Parallel Capacitors

The model was modified to allow the user to automatically determine the minimum number of parallel capacitors required to keep capacitor RMS current, $i_{dc(rms)}$, low enough so that the increase in C_{ths} was sufficiently limited to ensure that the lifetime of the capacitor was always higher than the lifetime of discrete SiC devices. Hence, the lifetime of the drive train system investigated in this study depends on the characteristics of the MOSFETs. The largest KEMET capacitor available in the C4AQ series is 100 μF so this was the upper limit allowed in the optimisation. The $i_{dc(rms)}$, C_{ths} and the internal losses of the capacitor, C_{ploss}, are the only circuit parameters impacted due to changes in ESR and R_{th} when using multiple, smaller capacitors. It is worth noting there is only minimal change in total inverter power loss due to changes in C_{ploss} and it is only of interest when it comes to capacitor performance and lifetime. Figure 4.11 shows the difference in the data when implementing this new procedure.

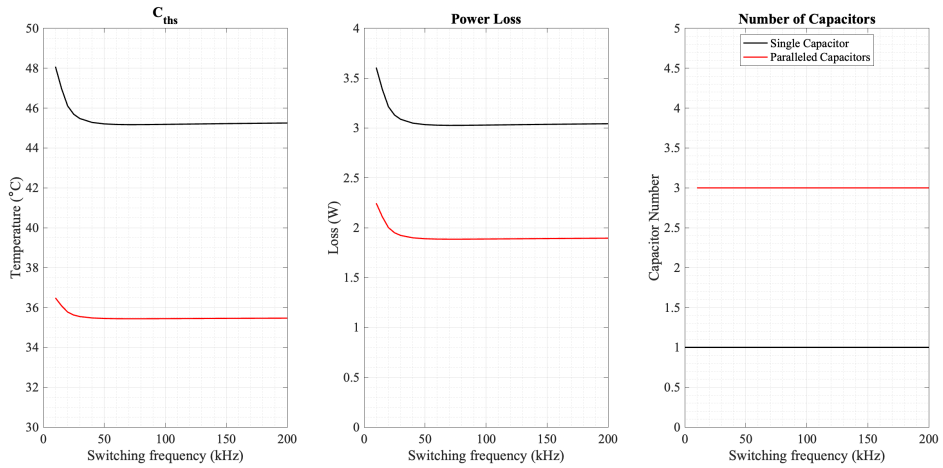


Fig. 4.11 Effect of paralleling capacitors on hot spot temperature and power loss as functions of switching frequency under normal operation

Minimum required capacitance

Equations 4.7 and 4.6 show the value of the DC-link capacitor reduces the voltage ripple and C_{ths}. As one of the optimisation design variables it is possible to initially study the impact of f_{sw} on the minimum required DC-link capacitance, C_{min}, to maintain the voltage ripple at a tolerable level, which is set as 1% in this study for normal operation. This is shown in Figure 4.12 and is presented alongside the calculated value of C_{min} from equation 4.8.

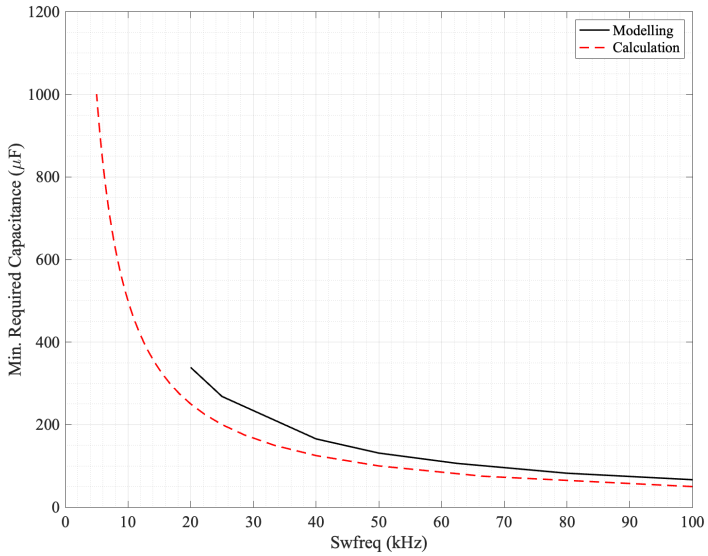


Fig. 4.12 Optimisation data for the minimum required capacitance as a function of switching frequency under normal operation, comparing calculated values with results from the optimisation using PLECS system model

Equation 4.8 or similar [137], is used in the majority of inverter optimisations from literature when calculating voltage ripple and the minimum DC-link capacitance. Using a fully simulation-based optimisation factors the circuit parasitics, and the load and source conditions. The data shows the greater required value from the simulation work, suggesting the analytical methods underestimate the required DC-link capacitance value.

Parallel MOSFETs

In addition to changing the number of paralleled capacitors, changing the number of paralleled MOSFETs in each leg is a major design consideration to be investigated. The number of devices used in the system impacts the volume, cost, and complexity of the IMD. The data in

Figure 4.13 shows how the circuit parameters change with switching frequency for 3, 4, 5 and 6 paralleled MOSFETs for normal operation.

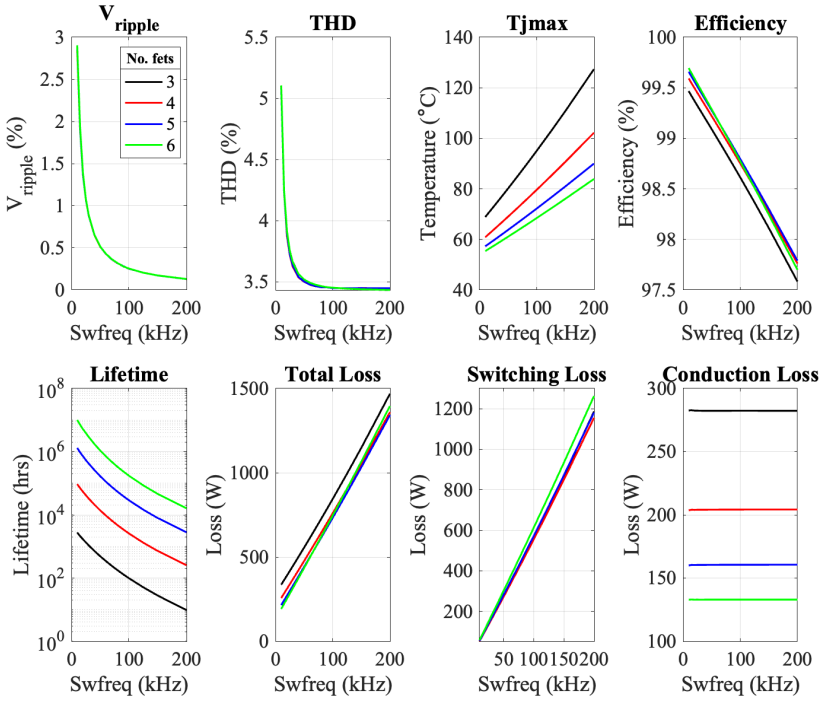


Fig. 4.13 Inverter parameters as functions of switching frequency under normal operating conditions, a heat sink temperature of 50°C and a 250 μF capacitor, for different numbers of paralleled MOSFETs

The data shows that increasing the number of devices improves the performance of the inverter by decreasing the power losses and $T_{j(max)}$. The losses caused by conduction are independent of f_{sw}, however, at higher frequency when paralleling extra devices the switching losses increase at a higher rate, so, at 200 kHz 6 paralleled devices experience greater losses than 4 or 5 devices. The load current is split equally between the MOSFETs, resulting in a reduction in the total conduction losses which is proportional to I^2 but total switching losses increase when more devices are used and therefore improves the lifetime from 2500 to 30000 when increasing the number of paralleled MOSFETs from 4 to 5.

The data in Figure 4.14 shows the effect of paralleling different numbers of devices for peak operation. The data shows that the higher currents during peak operation results in five fold increase in losses compared to normal operation. Paralleling 3 devices becomes a

non-feasible option at peak operation because the $T_{(j)max}$ values reached far exceed the limit of 175 °C.

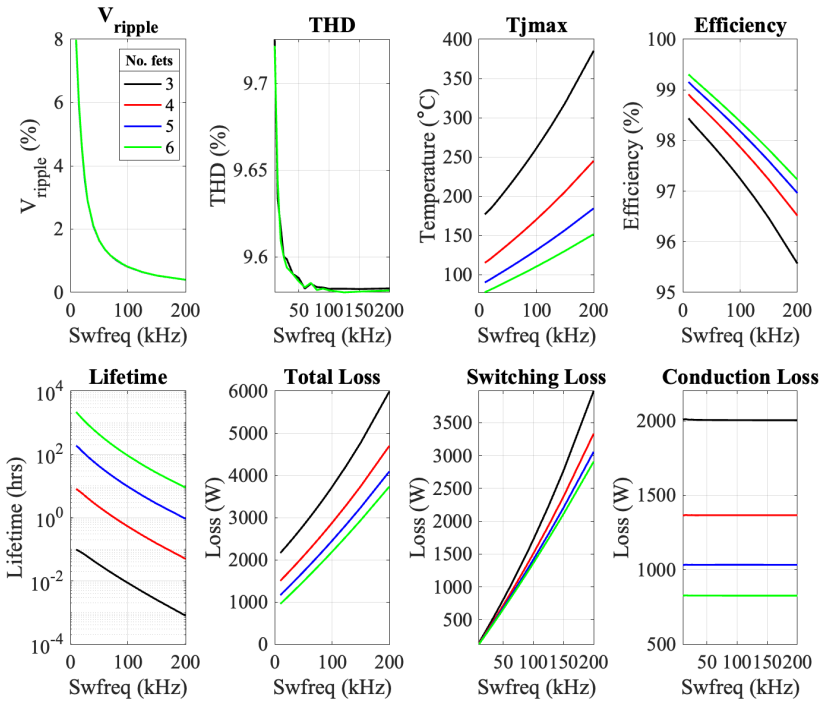


Fig. 4.14 Inverter parameters as functions of switching frequency with decreasing the number of paralleled MOSFETs under peak operating conditions, 50°C for a 250 μF capacitor

The number of devices must be considered when designing for the highest volumetric power density. Figure 4.15 illustrates the difference in the required DC-link capacitance and total inverter volume when different numbers of MOSFETs are paralleled, for a $T_{j(max)}$ limit of 175 °C.

The optimisation data shows that for normal operation the optimal number of devices is dependent on the temperature constraints of the system. For a heat sink temperature of 130 °C and below the limiting factor in the optimisation is the system efficiency and not the maximum junction temperature limit of 175 °C. A lower efficiency results in a greater increase in the junction temperature, however, Therefore, the number of MOSFETs has no effect on the minimum DC-link capacitance required and so the volume of the inverter actually increases due to the greater number of MOSFETs being used. As seen in Figure 4.13, fewer devices means higher junction temperatures and therefore at higher heat sink

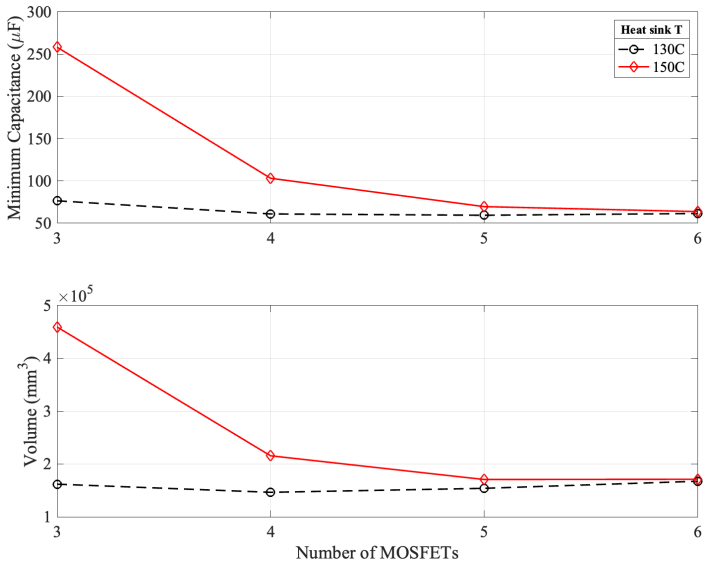


Fig. 4.15 Optimisation results for the minimum required capacitance and inverter volume as a function of number of inverter MOSFETs, for normal operation at different heat sink temperatures

temperatures, the $T_{j(max)}$ limit is reached at lower f_{sw} when using fewer devices. This results in larger C_{min} values required to meet the voltage ripple constraints. This leads to a larger total volume, as the reduced volume due to fewer MOSFETs is opposed by the increase in size of the capacitor.

4.6.2 Thermal Considerations

Another variable to consider when optimising the system is the environment in which it is operating. An IMD must operate in a high-temperature environment, resulting in unusually high thermal stresses on the component. In the system investigated in this project, the inverter is to be attached to the cooling plate of the PMSM motor. Therefore, the temperature of the inverter and its components depends on this thermal management system; the flow rate and temperature of the coolant, and the layout design of the inverter itself. The maximum coolant temperature and therefore the heat sink temperature, T_{hs}, of the traction inverter for an electric motor is usually 70 °C, but for an IMD the operating temperature of the power electronics can be higher, and it is of interest to investigate the performance at elevated temperatures. For this investigation, the ambient temperature of the heat sink is varied to

determine how this thermal management influence the optimal design. The effect of the heat sink temperature on the circuit parameters in a range of switching frequencies is shown in Figure 4.16.

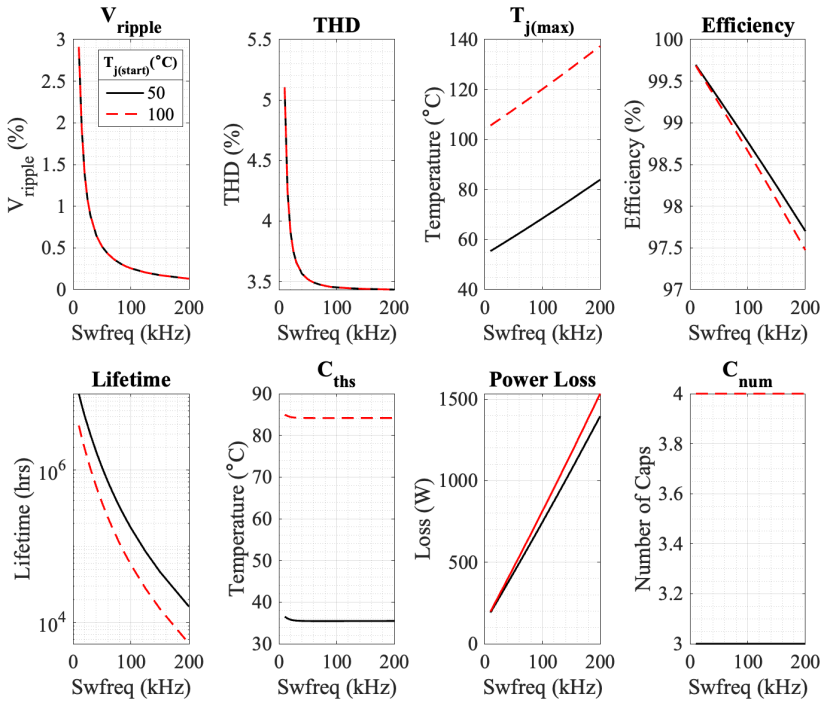


Fig. 4.16 Inverter parameters as functions of switching frequency with increasing heat sink temperature under normal operating conditions, DC-link capacitance of 250 μF

The data shows the effect on switching losses of operating the devices at higher temperature. $T_{j(max)}$ increases as expected, which partially explains the decreases in expected lifetime. The increased losses due to higher temperature operation are clear at high f_{sw}, with a 15 % increase in losses at 200 kHz when the heat sink temperature is increased from 50 to 100 °C. The number of parallel capacitors required to keep C_{ths} below a level where the lifetime of the capacitor is shorter than that of the devices also increases which may lead to higher inverter volume.

The designs produced by the model for heat sink temperatures between 50 and 90 are given in Table 4.7. The minimum DC-link capacitance required with the corresponding switching frequency is identified. For each optimisation, the parameters are measured for the optimal solution, making it possible to identify the limiting constraint. The limit to the C_{min}

is the maximum allowable voltage ripple which is defined as 1%. The limit to the switching frequency in this design is either the efficiency, η, or the $T_j(max)$ and is highlighted in blue in the table.

Table 4.7 Optimisation results for normal operation of six paralleled MOSFET inverter at a junction temperature limit of 100 °C at a range of heat sink temperature

T_{hs}(°C)	$C_{min}(\mu F)$	f_{sw}(kHz)	$\Delta V(\%)$	$T_{j(max)}$(°C)	**THD**(%)	$\eta(\%)$
50	53.5	126	1	72	3.4	98.5
60	54.2	123	1	82	3.4	98.5
70	55.5	121	1	92	3.4	98.5
80	64.8	103	1	100	3.4	98.7
90	172.4	39	1	100	3.6	99.4

Higher values of T_j reduce the performance of the inverter by increasing power losses and hence reducing the lifetime of the inverter. Constraint on the maximum junction temperature sets a limit on the amount of switching loss that a device can safely support and, therefore, limits the maximum switching frequency. Since the volume of the passive components in a converter tends to reduce in volume as the switching frequency increases, changes in the maximum junction temperature can impact the optimal design. By using the maximum T_j as a design variable instead of a set constraint in the optimisation, it can be observed from the data the effect of limiting the temperature on the volume of the IMD. Figure 4.17 presents optimisation data for a range of heat sink temperatures for an increasing $T_{j(max)}$ limit at normal operation.

The optimisation results show that if T_{hs} is approximately 20 °C below $T_{j(max)}$ limit then the temperature becomes the limiting factor in the optimisation. For example, at a $T_{j(max)}$ limit of 80 °C at a T_{hs} of 40 °C, C_{min} is 55 μF. However, at a $T_{j(max)}$ limit of 80 °C and T_{hs} of 60 °C the switching frequency is limited to 110 kHz due to the $T_{j(max)}$ limit constraint, which results in a larger C_{min} of 62 μF required to keep the voltage ripple below 1%. This effect becomes evident for higher T_{hs}, where the highest feasible T_{hs} is 70 °C for a $T_{j(max)}$ limit of 80 °C with a C_{min} of 162 μF.

It can be observed that for any $T_{j(max)}$ limit, as the heat sink temperature increases the C_{min} required slightly increases as the maximum allowable switching frequency decreases.

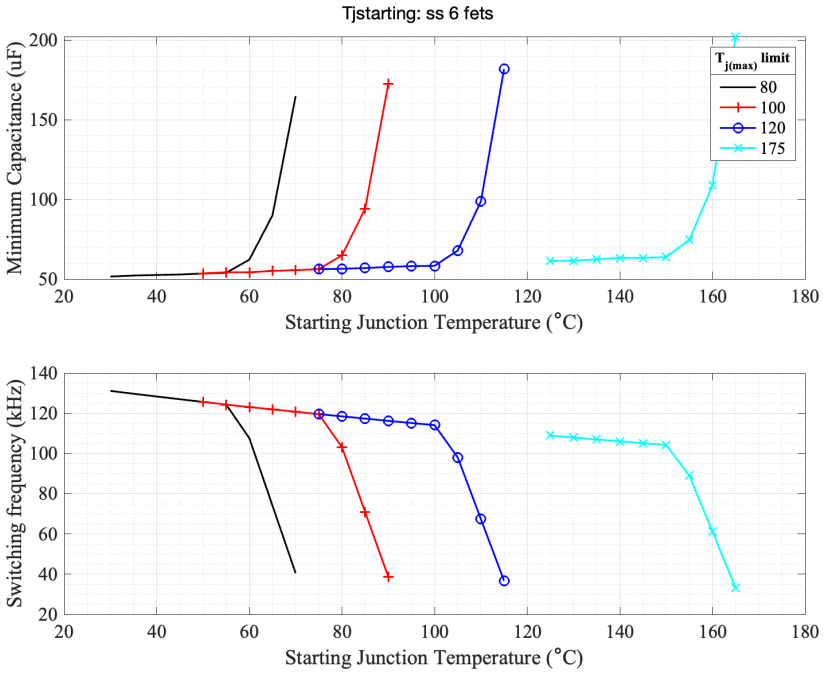


Fig. 4.17 Optimisation results for the minimum required capacitance and the corresponding switching frequency as a function of heat sink temperature for increasing MOSFET junction temperature limit for normal operating conditions

This can be explained by observing the data presented in Figure 4.16. At higher operating temperatures, power losses increase for a set f_{sw}, so efficiency becomes the significant constraint in the optimisation. To obtain the most optimal solution of 52 μF, T_{hs} has to be minimised.

A similar optimisation was performed out for an inverter under peak operation, using the design constraints in Table 4.6, with the results presented in Figure 4.18 .

In peak operation if the heat sink temperature is sufficiently low, the efficiency falls below the 97.5 % constraint before reaching the that the $T_{j(max)}$ limit of 175 °C. The minimum capacitance required is 62 μF, compared with 52 μF at normal operation because even though the voltage ripple constraint is higher for peak operation at 5%, the voltage ripple is higher for peak operation than normal operation at any given f_{sw}, leading to more stress on the battery and a larger required DC-link capacitance. In summary, for normal and peak operation, there is a minimum possible capacitance required of 52 μF and 62 μF respectively.

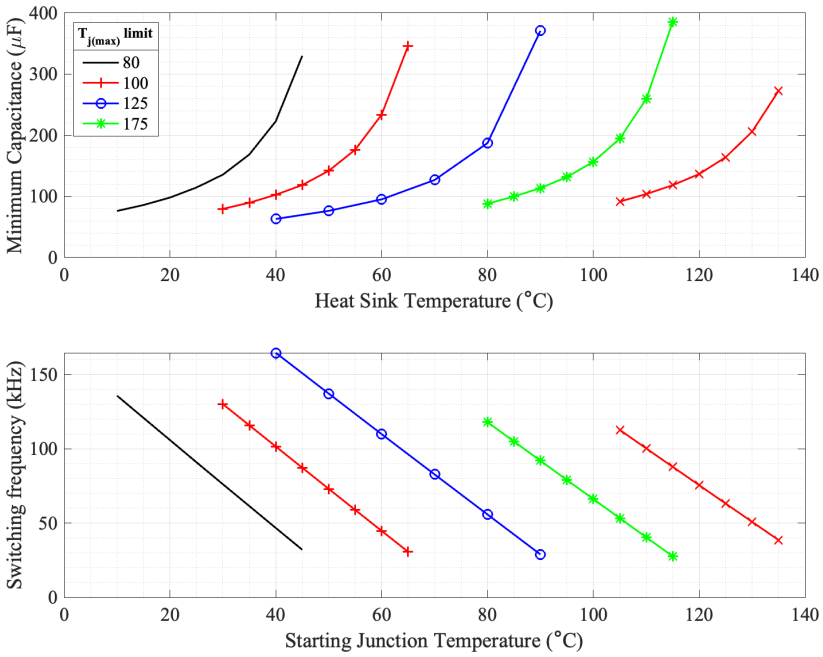


Fig. 4.18 Optimisation results for the minimum required capacitance and the corresponding switching frequency as a function of heat sink temperature for increasing MOSFET junction temperature limit for peak operating conditions

Therefore 62 μF is the smallest minimum capacitance required for this design, however, any changes to the thermal environment will change these results.

4.6.3 Reliability Optimisation

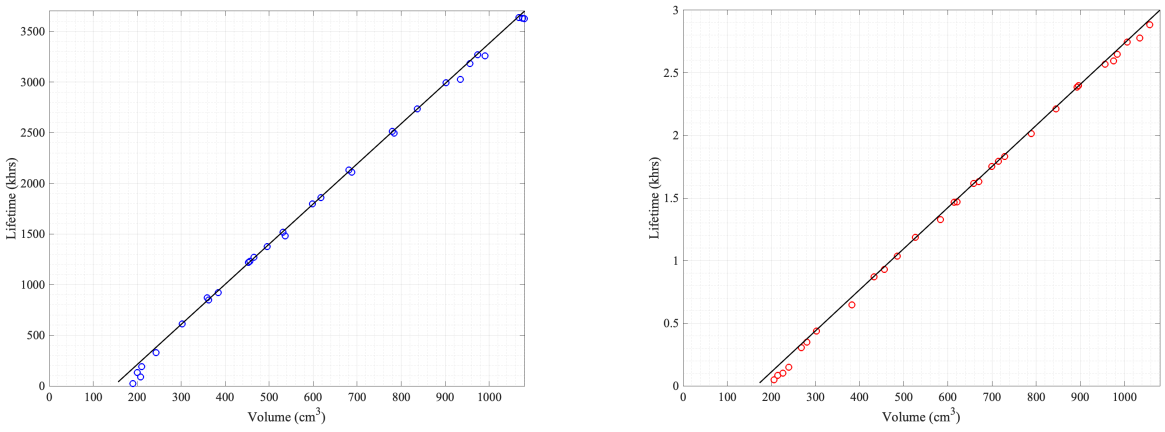
For a single-objective optimisation problem, improving the objective can mean reducing the performance of the system in other ways. Unlike single-objective optimisation, the solution of a multi-objective optimisation problem is not unique, but is composed of a set of solutions representing the best possible trade-offs among the objectives, which is called the Pareto optimal set or Pareto frontiers. The multi-objective problem can be transformed into a single objective, for example combining the contradictory objective functions of volumetric power density and lifetime, by multiplying them by a weighting factor to form a single function.

The multi-objective optimisation of power electronics enables designers to make a trade-off among multiple performance metrics. During the last decade, the efficiency and power density Pareto optimisations of multiple converter topologies have been presented [108].

The majority of the literature relating to the optimisation of power electronics considers performance indices such as converter efficiency, power density and cost, but rarely concern reliability.

This study uses a multi-objective optimisation at a system level in conjunction with a new TO-247 specific lifetime model to obtain accurate design results. The multi-objective optimisation problem is analysed to seek the Pareto optimal solutions, making it possible to evaluate the trade-off between power density and lifetime, and determine a number of optimal solutions.

The data in Figure 4.19a and 4.19b show the results for the multi-objective optimisation problem based on the optimisation solution procedure and the optimisation constraints described in Table 4.6 when each 'switch' in the inverter is six individual MOSFETs in parallel. The Pareto front for the converter is a line in two-dimensional space that represents the optimal relationship between the two objective functions, volume and lifetime. Any designs above the trend line are not feasible based on the design constraints and any below are non optimal designs.



(a) Normal Operation (b) Peak Operation

Fig. 4.19 Multi-objective optimisation results considering reliability and volume under normal and peak operation

As can be seen in both modes of operation, there is a linear relationship between the a inverter volume and lifetime. Volume is proportional to the DC-link capacitance which is determined by the voltage ripple. Reducing the size of the DC-link capacitor requires an

increase in switching frequency f_{sw} to reduce the voltage ripple, however, this leads to higher semiconductor switching losses causing an increase in $T_{j(mean)}$ and ΔT_j, resulting in a shorter lifetime using equation 5.7 discussed previously.

The higher output power of the inverter when operating in peak operating mode, results in higher load currents through the MOSFETs. This causes an increase in switching and conduction losses and has a direct effect in the calculation of N_f, as shown in equation 5.7. This explains the significantly lower lifetime prediction when comparing normal and peak operation. An inverter volume of 600 cm^3 will have a lifetime of 1,800,000 hours at normal operation or 1,400 hours at peak operation. This value of lifetime for normal operation seems very high, however when six MOSFETs are paralleled together and the inverter operates at at 20 kHz f_{sw} for the 600 cm^3 inverter, the ΔT_j is only 1.2 °C so the calculated number of cycles to failure is very large. Therefore, in this case a greater f_{sw} could be used to minimise volume while keeping an acceptable lifetime, however the combination of normal and peak conditions needs to calculated before the system lifetime can be considered.

Based on the Miner rule shown in equation 4.11, the damage, D, can be calculated to combine the normal and peak operation to determine an overall lifetime for the system.

$$D = \sum_i \frac{n_{(i)}}{N_{f(i)}} \tag{4.11}$$

where subscript i indicates different conditions, for example the normal and peak operation, n_i is the number of cycles at operating mode i, and $N_{f(i)}$ is the number of cycles to failure at operating mode i, as calculated in the optimisation.

The proportion of the overall operation under each mode was used in place of a given value for the number of cycles so the resulting damage, D, is calculated as damage per cycle. In this design it was assumed the system would be operating under peak conditions 10% of the time. The $N_{f(normal)}$ and $N_{f(peak)}$ are calculated for the same switching frequency and correspond to a required DC-link capacitance that is the larger value from the normal and peak modes optimisations.

The lifetime in hours can subsequently be calculated from the damage per cycle. The Pareto front of the overall lifetime and volume for the design with six paralleled MOSFETs is shown in Figure 4.20 and the data in Figure 4.21 show the corresponding switching frequencies.

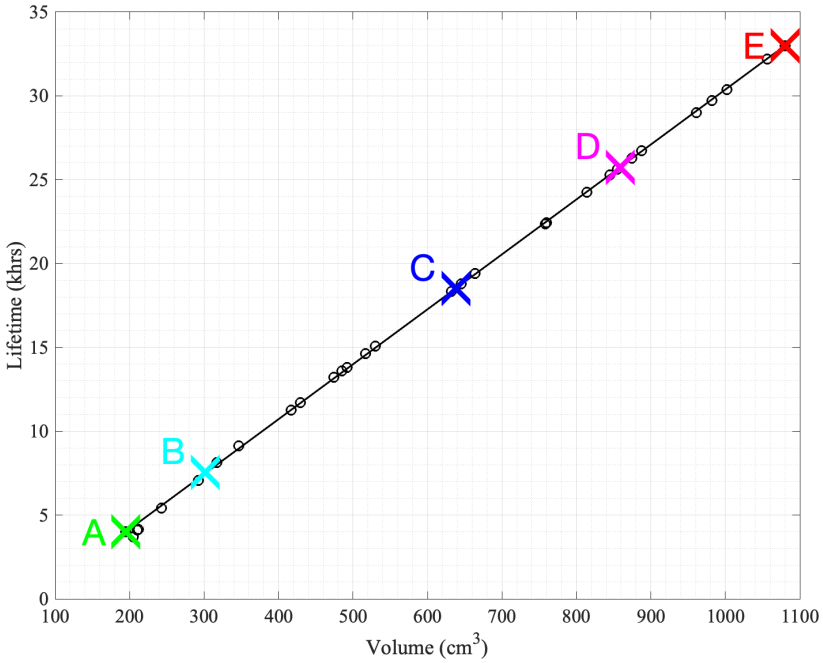


Fig. 4.20 Multi-objective optimisation results considering lifetime and volume for the combined operation of the system, with key points identified

The multi-objective solution is limited by two points labelled A and E. Point A represents the inverter design with the highest volumetric power density, while E is the most reliable and has the longest expected lifetime. The switching frequency limit is 118 kHz , point A , because the efficiency under normal operation at this point is 98.5 %. Point E is the lower limit of switching frequency at 13 kHz, any lower fails to meet the maximum THD limit of 5 % under normal operation. The increased switching frequency between points A and E results in a volume and lifetime decrease because they are both inversely proportional to f_{sw}.

For a multi-objective optimisation, the designer has to make decisions based on the data, with knowledge of the intended application of the inverter system, to determine the single optimal design. Point C represents a compromise of the fitness functions, and is given by weighting the scaled values of lifetime and volume equally in the optimisation. It has a

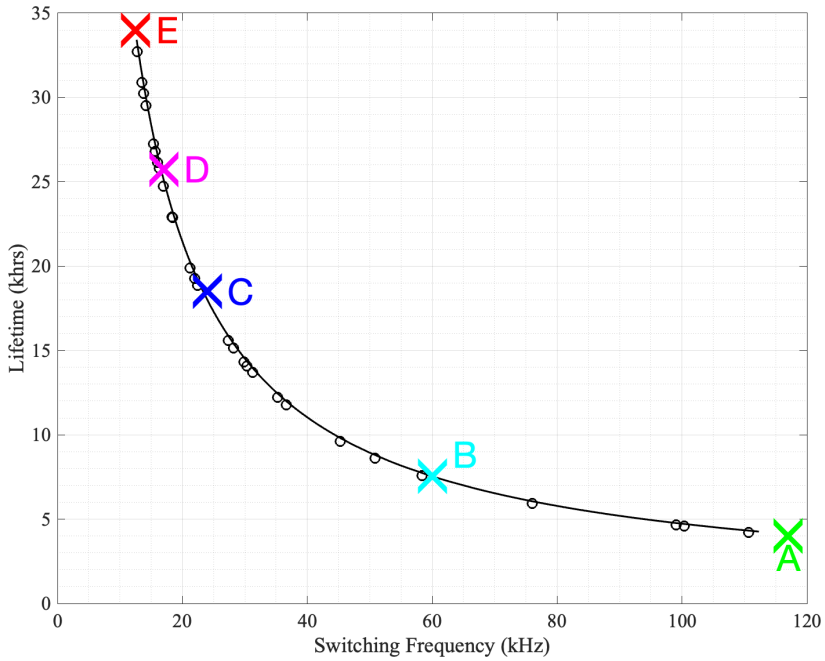


Fig. 4.21 Multi-objective optimisation results considering lifetime and switching for the combined operation of the system, with key points identified

volume of 640 cm^3 and a lifetime of 18,500 hours. Marginal increases in f_{sw} between point E, D and C result in significant reductions in lifetime, with the lifetime values dropping from 34,000 to 25,750 to 18,500 hours across a 12 kHz change in frequency. The corresponding volume decrease corresponding to the reduction in lifetime is proportional to the lifetime change, decreasing from 1080 to 860 to 640 cm^3.

Considering point C, the volume of the inverter can be halved by increasing the switching frequency to 60 kHz. Highlighted as point B in the data, this requires a DC-link capacitance of 110 μF, and the inverter will have a predicted lifetime of 7,500 hours at 60 kHz switching frequency. To decrease the volume from 300 cm^3 at point B to the 200 cm^3 limit at point A, the f_{sw} must double which corresponds to the lifetime reducing by 50%. This significant increase in f_{sw} increases $T_{j(max)}$ from 148 °C to 172 °C which is close to the maximum rated temperature of the SiC MOSFETs and may be considered too high when proposing a final design.

It was shown by the data in the previous section in Figure 4.13 and Figure 4.14 that using a greater number of discrete devices will increase inverter lifetime due to the current in each

device is reduced, leading to lower junction temperatures and stresses. Figure 4.22, compares the data for multi-objective optimisations when paralleling four, five and six MOSFETs in the inverter.

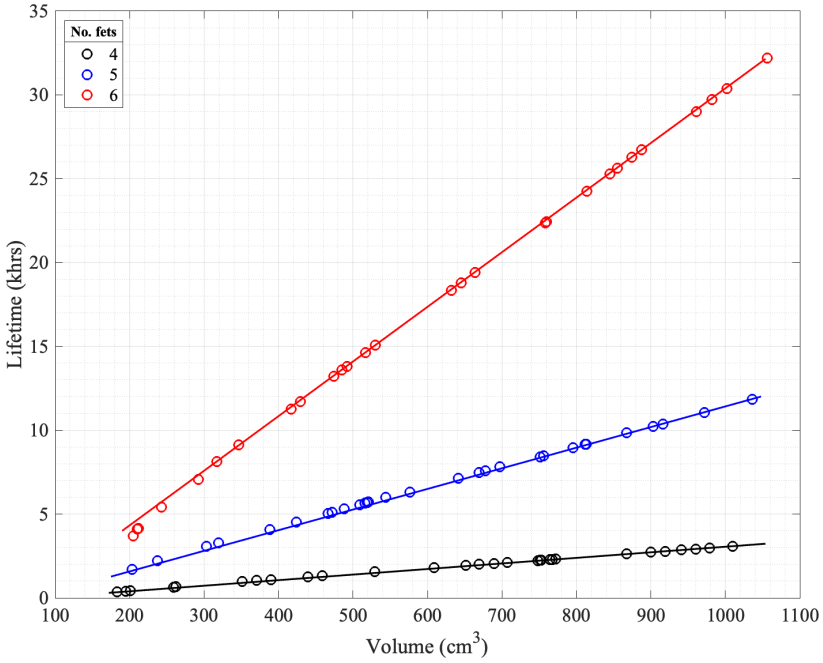


Fig. 4.22 Comparison of Pareto front between volume and lifetime for 4, 5 and 6 paralleled MOSFETs

Using fewer MOSFETs changes the relationship between the volume and the lifetime. In an inverter, the volume is dominated by the DC-link capacitor, for example in a design with a volume of 600 cm3 only 6.7 %, 8.4 % and 10 % of the volume is due to the MOSFETs for inverters with 4, 5 and 6 paralleled devices respectively. However for a 300 cm^3 design, the MOSFETs make up a much larger proportion of the volume, increasing to 13.5 %, 16.8 % and 20 %. Therefore, for a specified volume, the DC-link capacitor required to meet the voltage ripple constraints must be smaller when using a greater number of parallel MOSFETs. To reduce the required DC-link capacitance a higher switching frequency is used. However this increase in switching frequency does not cause sufficient increases in the MOSFET switching losses to negate the increase in lifetime caused by smaller current per device when using more MOSFETs.

4.6.4 Design Summary

There are numerous possible solutions when designing an IMD with a focus on volumetric power density and reliability, all of which can be considered optimal. To derive a unique design that meets specific requirements, further additional constraints need to be introduced. Firstly, the heat sink temperature has been shown to greatly impact the volume and lifetime of the IMD and therefore will impact the optimal design. A standard coolant temperature of the PMSM plate where the devices are mounted is 70 °C, however, as this is an IMD and the coolant plate will in reality not be all one temperature, it was assumed that the MOSFETs will need to operate at temperatures up to 100 °C. Therefore, this was used as the heat sink temperature in the final design.

The next required decision is the trade-off between volume and reliability. The data shown in the previous section in Figure 4.20 is the multi-objective optimisation for normal and peak operation at a heat sink temperature of 100°C using 6 MOSFETs in parallel. The data show the converter design that produces the smallest total volume, which for the design example is 195 cm^3, at a switching frequency of 118 kHz, however this design would have a lifetime of 4 years.

A reasonable value for inverter lifetime can be considered as anything above 10,000 hrs, or 10 years, as according to the UK Department for Transport's Vehicle Licensing Statistics report 2020 the average age of a car before being replaced is 8 years. Therefore, considering the data in Figure 4.22 only inverter circuits with 6 paralleled MOSFETs with a volume greater than 360 cm^3 or 5 paralleled MOSFETs with a greater volume than 900 cm^3 are feasible when considering 10 % peak operation.

In an IMD the volumetric power density is important, therefore the single optimised design selected is an inverter with a six paralleled MOSFETs in each leg, a DC-link capacitor of 190 μF , operating with a switching frequency of 45 kHz. This gives a volume of 440 cm^3 and a predicted lifetime of 12 years. These design values match with those published in the literature for IMDs [137], however the reliability of the system operating at 100 °C is often not considered in other previously published work. Accurately predicting and optimising

the lifetime of the TO-247 packaged SiC MOSFETs in the system allows a more informed decision to be made on the final design, allowing a more optimal solution to be found.

4.7 Summary

The challenges particular in designing reliable, compact integrated motor drives are presented in this chapter allowing an optimal IMD to be presented in terms of lifetime and volume. Specifically, the influence of SiC losses and the temperature of the PMSM machine on the inverter must be considered. An electrothermal model of the entire power train was built in PLECS allowing component interactions and inter-dependencies to be investigated. Validated SiC MOSFET models were used in the simulation of a three-phase inverter, allowing system-level simulation at a range of operating conditions.

An optimisation procedure to increase volumetric power density by reducing the size of the DC-link capacitor is presented and compared to analytical methods of individual component sizing and design. The influence of switching frequency has demonstrated the potential reduction in voltage ripple and total harmonic distortion, and the potential increase in losses in each MOSFET resulting in higher junction temperatures and lower reliability.

The reliability, calculated as the hours of operation until failure, is based on a recently developed lifetime model specific to transistors in a TO-247 package. The model requires detailed circuit electrical and thermal conditions from the PLECS simulation, enabling the MOSFET lifetime to be calculated within the optimisation. In the initial study at normal operation when six are paralleled in an inverter, the MOSFET lifetime, and therefore the lifetime of the IMD, decreases from 300,000 hours at 10 kHz switching frequency to 4000 hours at 200 kHz switching frequency.

The number of paralleled MOSFETs in each leg of the inverter, the heat sink temperature, and the number of parallel capacitors for the DC-link capacitor bank were investigated over a range of switching frequencies and within the optimisation to allow for optimal parameter selection while meeting the design constraints.

In the design process, both normal and peak operations need to be considered. A multi-objective optimisation allowed the lifetime to be considered as an objective function alongside the conflicting variable of inverter volume. A Pareto front identifies a range of possible solutions in a multi-objective optimisation procedure. Finally, further analysis of these possible solutions for normal and peak operation identified a single optimal solution for the system, using a DC-link capacitance of 190 μF at 45 kHz, giving a volume of 440 cm^3 and a lifetime of 12,000 hours.

Chapter 5

Design of Fault Tolerant Multi-phase IMD

5.1 Introduction

Despite the clear benefits discrete SiC MOSFETs can provide for three-phase IMDs and the industry focus on increasing power density, relatively few studies have been undertaken to study improving reliability. This chapter uses a multi-faceted approach to IMD improvements, with focuses on new topology and design as well as investigating more accurate and effective processes and analysis in optimisation-based design.

Improving the electrothermal simulation analysis and lifetime prediction facilitates more accurate and therefore valuable research. Detailed thermal analysis, such as computational fluid dynamics (CFD) is commonly used in late stage inverter design. Highly accurate modelling can evaluate the coolant flow and MOSFET arrangement and hence the thermal performance of the MOSFETs in an IMD environment.

Although the recent introduction of package specific lifetime prediction methods allows more accurate reliability analysis in IMD systems, relying solely on the calculated number of cycles to failure, N_f, is insufficient for comprehensive system lifetime analysis. New methods of calculating the reliability using the N_f of a MOSFET can be applied to full systems

and depends on the uncertainties and variations of individual devices and experimental or simulation data. However for fault tolerant inverter systems work is limited.

Fault tolerance is traditionally known as the property that enables a system to continue operating in the event of the failure of one or more faults within some of its components. Therefore a fault tolerant system ensures there is no possibility of sudden and unexpected failure which is an important consideration for automotive drives where safety is an important feature. This improves the reliability of the system based on the definition of reliability in this work as the ability of the inverter to maintain operation at either the normal or peak stress conditions defined in the optimisation.

An optimisation procedure has been previously used for design of a three-phase IMD to improve the reliability and volumetric power density. This chapter will investigate the performance of fault tolerant inverters and their potential advantages over traditional three-phase inverters. It will also explore how improving electrothermal simulations can be implemented in future optimisations to increase accuracy by integrating more detailed thermal analysis into the procedure. A novel method of lifetime prediction was performed in this section for fault tolerant systems including three-phase inverters with multiple paralleled MOSFETs. Optimal designs can be determined to compare the advantages and disadvantages of multi-phase fault tolerant IMDs with the traditional three-phase designs studied in Chapter 4.

5.2 Multi-phase Power Trains

Both multi-level inverters (MLIs) and multi-phase inverters (MPIs), have been widely investigated in literature to improve upon the traditional three-phase power train. MLIs are a viable solution when voltage is the limiting factor [50] and are therefore able to utilise MOSFETs with lower voltage ratings for the same DC-link voltage when compared to two-level inverters. Increasing the power train voltage can be an attractive prospect in automotive applications as it enables fast charging and reduces cabling footprint, which causes a reduction in filter requirements and therefore volume. However, it can lead to more frequent machine failures

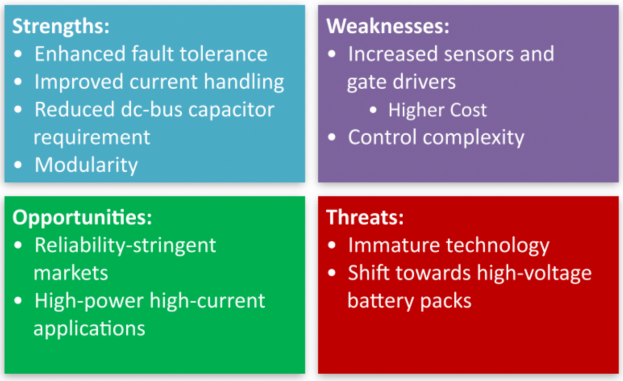


Fig. 5.1 Strengths, weaknesses, opportunities, and threats analysis of multi-phase inverters (MPIs) [53]

due to higher insulation requirements resulting in partial discharge [139]. As the inverter in this study is designed for a 650 V application and utilises 1200 V MOSFETs, voltage is not a limiting variable in the design, therefore, MLIs are not considered, although their application in power trains rated at and beyond 800 V is gaining significant attention [139].

Multi-phase inverters (MPIs) have enhanced fault-tolerance and reduced DC-link capacitor sizing compared to traditional three-phase inverter. However, the application of MPIs is application dependent and currently for automotive applications three-phase PMSMs are more frequently used due to their high torque density, efficiency, and availability. Figure 5.1 summarises the strengths and weaknesses of MPIs [53].

Combining the advantages of IMDs with the advantages of multi-phase drives is of great interest in research and industry but is currently early in it development [140, 7]. In [141] an inverters volume was reduced when using a five-phase air cooled IMD compared to a three-phase system because of a smaller DC-link capacitor. Another multi-phase inverter used nine-phases in [44] to increase power density to 35 kW/L by exploiting the reduced per-phase power handling of the MPI.

In multi-phase inverters (MPI), the spatial displacement between the phases, δ, can be symmetric or asymmetric. In symmetric systems, each two consecutive phases are $\delta = 2\pi/n$ apart. Figure 5.2 illustrates the general phase of three-phase systems with a displacement of $\delta = \pi/n$ distribution for symmetric and asymmetric MPIs [140].

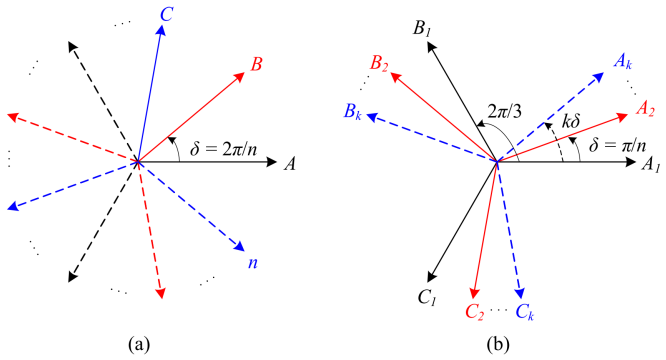


Fig. 5.2 General phase distribution in n-phase inverters for different spatial displacement configurations. (a) Symmetric: $\delta = 2\pi/n$ (b) Asymmetric: $\delta = \pi/n$, $k = (n-3)/3$ for n multiples of 3 [53]

5.2.1 Per-phase Requirements

One of the most notable features of MPIs is the reduced per-phase current. The phase current of MPIs can be defined with respect to their three-phase counterpart as:

$$I_{n-\phi} = \frac{3}{n} I_{3-\phi}, n \geq 3 \tag{5.1}$$

where n is the number of inverter phases, $I_{n-\phi}$ is the per-phase current for the n phase inverter, and $I_{3-\phi}$ is the per-phase current for the three-phase inverter.

Figure 5.3 shows how the per-phase current decreases with increasing phase number as the load current is split between the phases. However, there is reduction in the reduction in phase current made by increasing the phase number and there is a point where it is not beneficial to the system to add more phases because of the complexity required. The reduction in per-phase current mitigates the current limitation of the power semiconductor devices. In the family of SiC MOSFETs investigated in this project the maximum rated continuous current of the Infineon 30 mΩ MOSFET is 56 A and at the time of writing, the highest current rating of commercially available, automotive-grade discrete SiC MOSFETs is 225 A [12]. However, this high current MOSFET comes at five times the cost of the device used in this project and a C_{iss} of 9170 pF leading to large switching losses. Therefore for traction applications, paralleling of multiple discrete devices in three-phase inverters can be

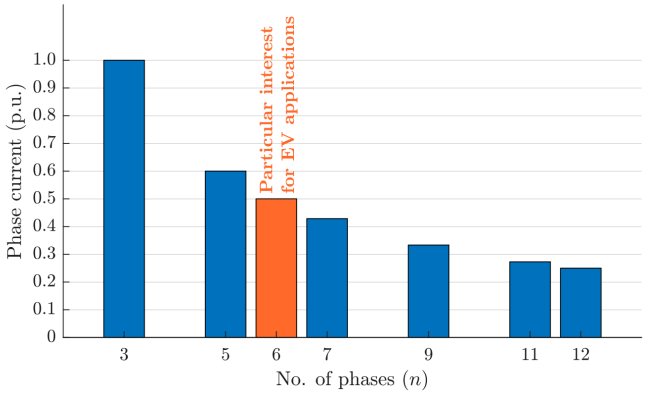


Fig. 5.3 Reduced per-phase current requirements in MPIs [142]

beneficial, as shown in previous chapters. Lower current per-phase allows simpler gate drives [143] as it becomes easier to maintain equal current per-device, avoiding localised heating and unreliability [144].

5.2.2 DC Capacitor Requirement Reduction

The equation for the minimum required DC-link capacitance, C_{min}, 4.8, discussed in Chapter 4, shows that it is dependent on current, voltage ripple and switching frequency in a three-phase inverter. It was shown in [142] that the required DC-link capacitance decreases with increasing phase number, with a 50% capacitance reduction achieved in six-phase VSI compared to a three-phase VSI, as shown in Figure 5.4. This chapter will investigate optimisation of an IMD, considering the potential reduction in capacitance and therefore volume of using multi-phase drives and inverters.

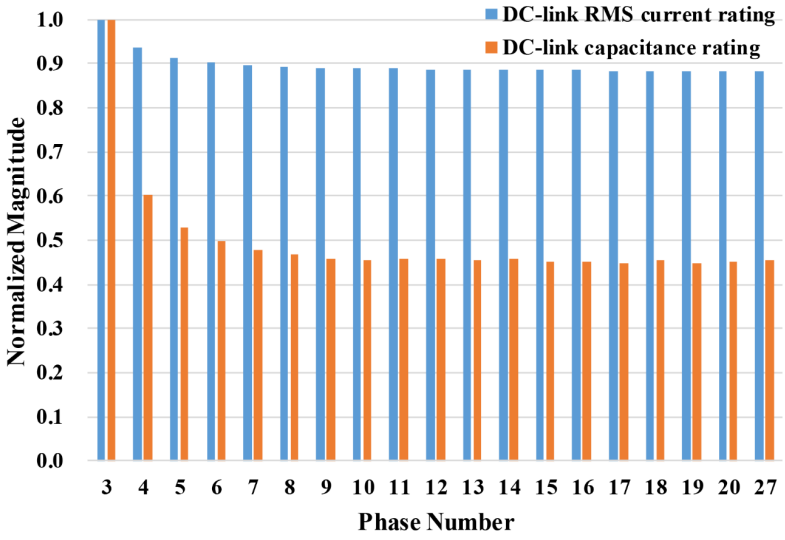


Fig. 5.4 DC-link capacitor capacitance and RMS current ratings comparison among different phase number VSIs [142]

5.3 Dual Inverter Motor Drive System

In literature, the most common multi-phase topology for high-power in traction applications is the dual three-phase inverter because of its high efficiency and its good reliability due to its modular design, characteristics that also make it suited to IMD design [145]. Figure 5.5 shows the typical configuration of the dual inverter traction system that will be investigated in this chapter, where two three-phase inverters are connected to a six-phase permanent magnet synchronous motor (PMSM).

5.3.1 Multi-phase PMSM Modelling

The six-phase dual star electrical machine model is provided in PLECS and is modelled with two sets of dq rotor reference frames [120].

Dual three-phase machines consist of two isolated neutral star connected three-phase sets that share a common rotor with windings that have been spatially shifted by either 0° (split), 30° (asymmetric) or 60° (symmetric), as shown schematically in Figure 5.6. Symmetric six-phase machines have superior fault-tolerance compared to asymmetric six-phase machines, which are common due to their reduced torque ripple [114, 147]. The

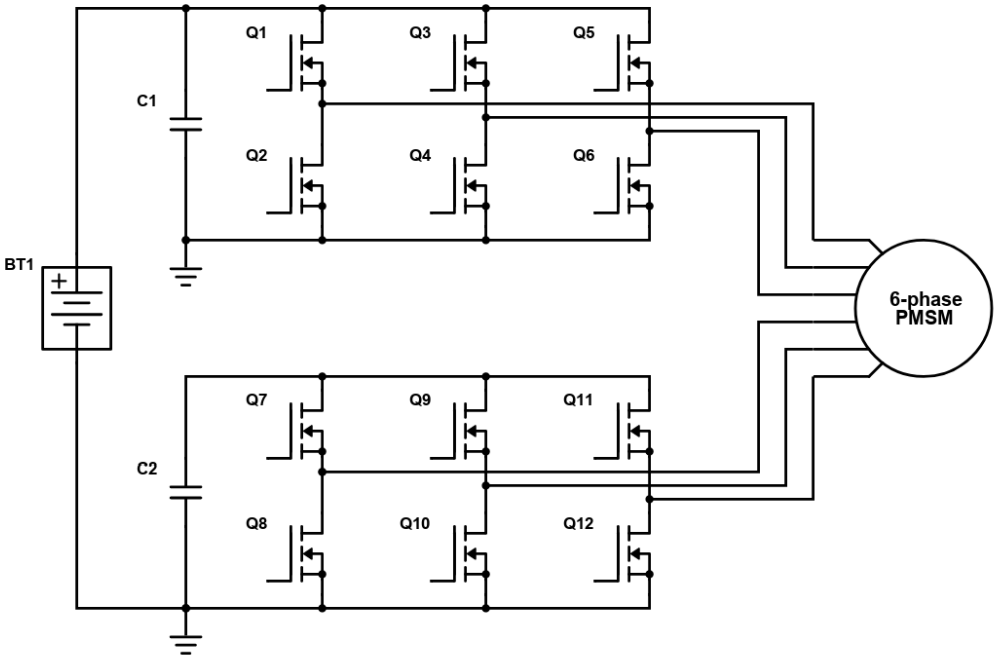


Fig. 5.5 Schematic of dual inverter traction drive system

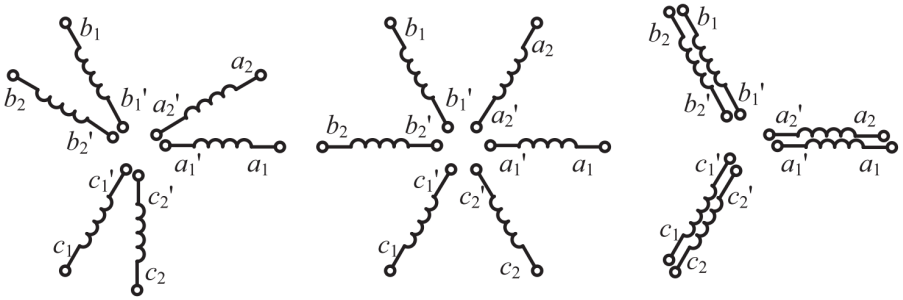


Fig. 5.6 Stator winding arrangement for (a) asymmetrical six-phase, (b) symmetrical six-phase, and (c) dual three-phase machines [146]

symmetric configuration was chosen in this study because it can be observed in PLECS simulation that the DC-link capacitor experiences a 15% decrease in voltage ripple compared to an asymmetric load. This is because the symmetric six-phase PMSM has a more balanced load distribution on the inverter, resulting in a more uniform and stable DC-link voltage.

The symmetric distribution therefore allows a more reliable system with a higher volumetric power density to be achieved.

5.3.2 Control

The cascaded speed and current control scheme model follows the diagram presented and is explained in detail in PLECS documentation [120].

The main modulation techniques: carrier-based PWM (CBPWM) and space vector PWM (SVPWM) are applicable to inverter of any phase number. CBPWM is the most advantageous for multi-phase inverters because SVPWM can require complexity and computing power for multi-phase systems. A comparison between CBPWM and SVPWM in 2L seven-phase VSI in [148], demonstrated that both exhibit similar THD and voltage ripple. Additionally, extension beyond the traditional SVPWM to interleaved multi-carrier techniques for multi-phase inverters is possible with CBPWM and has been suggested for n multiples of three [149]. Therefore, CBPWM is deemed a simpler yet effective technique for multi-phase systems and so is implemented in the dual inverter inverter studied in this chapter.

Interleaving

Interleaving is widely used in power converters to decrease capacitor current ripple and DC-link voltage ripple for passive component size reduction [150]. In a two-level inverter, the DC-link capacitors carry load currents, resulting in unbalanced capacitor voltages. Dual inverter IMD systems are suitable for the application of interleaving, as there are two converter modules with independent control. In interleaved multi-carrier PWM for the dual inverter, each inverter has a dedicated carrier wave, which can be independently shifted with respect to the other.

Thus, with a properly designed modulation scheme, the DC-link ripple current that flows through the dc-link capacitor can be reduced, which means the DC-link voltage ripple can decrease. As [151] pointed out, the DC-link ripple current can be reduced by inserting a phase shift angle in the carriers of those two inverters to achieve interleaving operation, as shown in Figure 5.7, where the carriers are the carrier waveforms that are used to generate

the PWM signals, f_s is the switching frequency, and ϕ is the phase-shift angle. When the load power factor is high, a 90° phase-shift angle can minimise the DC-link ripple current [151].

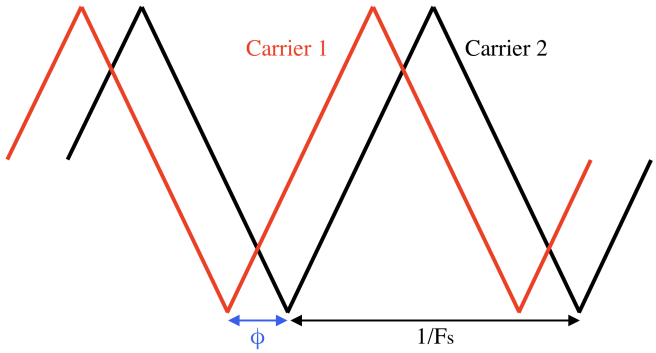


Fig. 5.7 Interleaved carriers of dual inverter system

Because the duty ratios are identical, the output sinusoidal voltages at the fundamental frequency are the same. However, shifted gate signals will create shifted current and voltage ripples. Therefore, when the ripples are combined, they cancel each other and result in smaller total ripple voltage on DC-link. In [152], it is experimentally verified that this interleaving technique allows to reduce both the DC-link capacitance and the DC-link capacitor volume of a 55 kW inverter prototype by 60%, while reducing the capacitor ripple current by 55%–75%.

The optimal interleaving phase angle for a symmetric six-phase machine, where the angle between phases is 60° is typically considered to be 30°. This allows for 30° interleaving between adjacent phases, resulting in an optimal balance between current ripple reduction and torque ripple reduction. To analyse the DC-link current and voltage ripples, simulations were carried out, with the data shown in Figure 5.8.

When the proposed interleaving scheme is applied, the maximum reductions of current and voltage ripple are 65% and 25% respectively showing one of the benefits of using a dual inverter system.

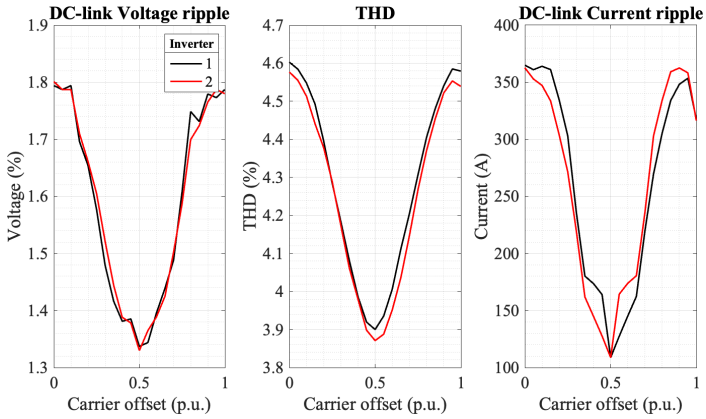


Fig. 5.8 Effect of interleaving on circuit parameters in the dual inverter system, at 40 kHz switching frequency with 100 μF DC-link capacitance

5.3.3 Operating Conditions

The normal and peak operating conditions are shown in Table 5.1. These conditions are the same as the optimisation in Chapter 4, allowing a direct comparison between the new inverter and the previously designed three-phase system. The external thermal conditions are independent of the motor and inverter type in this study, as it is assumed the motor losses and therefore the cool plate temperature are the same for both three-phase and six-phase PMSM.

Table 5.1 PMSM Operating Conditions

Operating Mode	Normal	Peak
Speed (rpm)	4000	3700
Torque (Nm)	140	310

The power train system is designed to operate for 1000 hours per year, 10% of which is at peak conditions. This equates to a total of 19 hours driving per week which is well above the 4.4 hours per week UK average according to the 2019 National Travel Survey conducted by the UK Department for Transport, but below that expected of a commercial driver.

5.4 Fault Tolerant Operation

Fault-tolerance enables a system to continue operating in the event of failures of its components, increasing system reliability. Partitioning and redundancy are the most common

measures for implementing fault-tolerant hardware. Partitioning splits a system into several subsystems, when a part fails the remaining subsystems can perform the reduced power function. Redundancy applies if more than the necessary components are present which is a contradiction to maximising the volumetric power density, another aim of this thesis.

In literature, mostly open mode failures are addressed, because they are simpler to handle and enable the operation with only one phase less [153]. For real fault-tolerance short-on failures have been regarded [154–156]. Normally, short-on failures of semiconductors as well as machine windings require separation elements or an active short-circuit (ASC) . An ASC can be applied to a system under fault, if the remaining sub-systems are still operational. This thesis will not go into detail about the ASC system and the failure modes are investigated through different simulation control designs.

By adopting a fault-tolerant design approach, reliability goals can be met without relying on excessive redundancy or system over-sizing. This section concentrates on how the dual inverter system can be designed to operate with fault-tolerant control to continue motor operation in the case of MOSFET faults. Fault conditions of the inverter studied and dynamic behaviour of the dual inverter IMD under three conditions are analysed and simulated:

- MOSFET failure
- Phase failure
- Inverter failure

MOSFET failure

Failure of a single device will not cause the phase to fail when there are multiple MOSFETs paralleled in the inverter. However, the load current will be split between the remaining devices, significantly reducing their remaining lifetime compared to the other MOSFETs in the inverter. It is therefore much more likely that after one devices fails it will be the another device in the same phase that will be the next in the system to fail. In a dual inverter system operating under normal conditions with 3 paralleled MOSFETs, if one device fails

the remaining MOSFETs experience a maximum load current of 66 A, up from 45 A, and hence the lifetime will decrease from 18 years to 4 years at a switching frequency of 50 kHz.

Phase failure

When sufficient MOSFETs in one phase fail, usually at the point that causes the load current per device to exceed the maximum rated current, the phase is considered to fail and the IMD begins operating as a five-phase system.

In the six-phase balanced system before the fault, there are six voltage references generated by the controllers, V_1-V_6. After a fault in one of the phases, V_6, in order to avoid torque oscillations the control is modified to supply the remaining five phases. The non-fault phase voltages are modified to create a new reference voltage, allowing new gate signals to be generated that will produce the same line-to-line voltages at the terminals of the stator windings.

$$V_{j(new)} = V_j - V_6 \tag{5.2}$$

where j is the phase number and $V_{j(new)}$ is the new reference voltage for phase j. Adding a zero-sequence signal reduces the magnitude of these voltage references. The zero sequence signal can be calculated as:

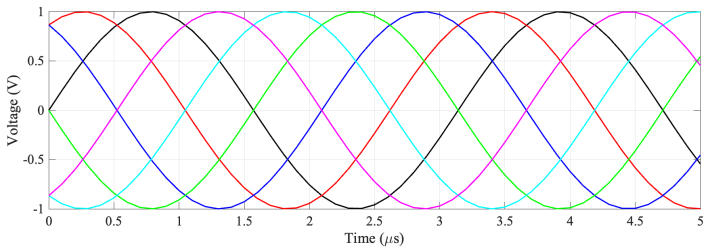
$$V_{sz} = -\frac{1}{2}(max(\Sigma V_j) + min(\Sigma V_j)) \tag{5.3}$$

And the updated new references can be calculated as:

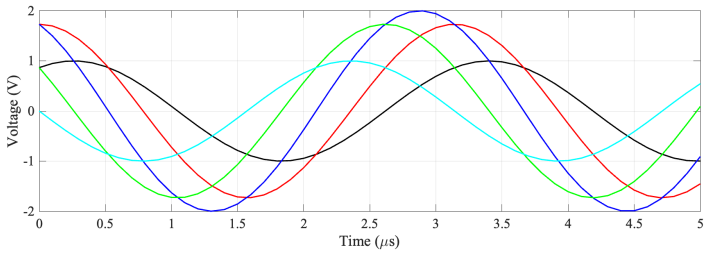
$$V_{j*} = V_{j_{new}} + V_{zs} \tag{5.4}$$

The waveforms of the different stages of the conversion from six-phase to five-phase voltage are shown in Figure 5.9 and the an example of the motor voltage waveforms for the inverter operating under a single phase failure is shown in Figure 5.10.

The data in Figure 5.10 shows that after the fault of one phase, there is greater stress on the MOSFETs in phase 3, 4 and 5 which at normal operation will now operate with a



(a)



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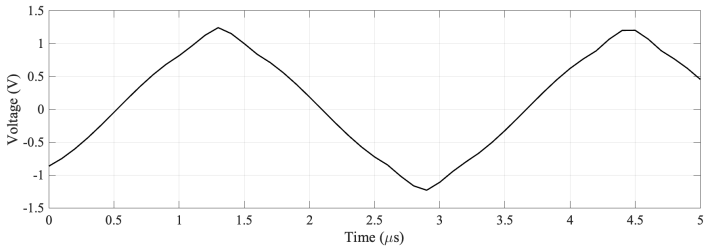

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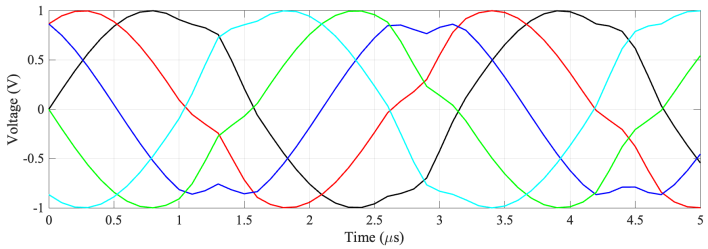


(d)

Fig. 5.9 Six-phase to five-phase voltage conversion. (a) Original six-phase waveform (b) Voltage reference signals (c) Zero sequence signal (d) Five-phase waveform

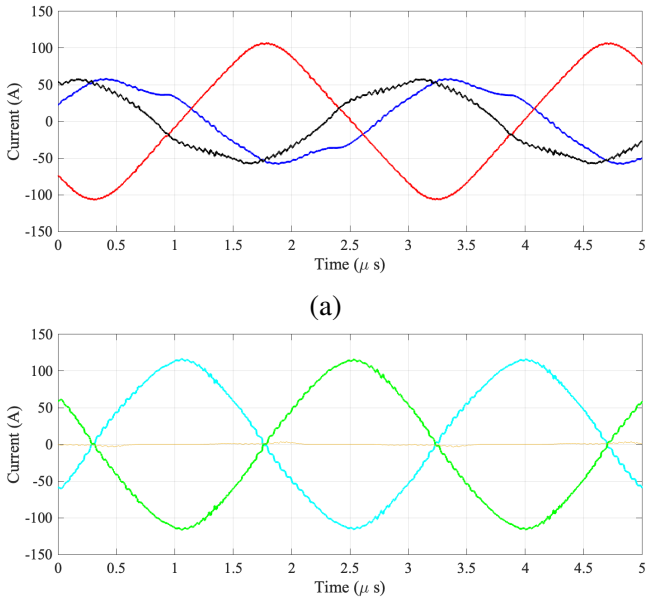


Fig. 5.10 Dual inverter current outputs after fault in phase 6 (a) Inverter 1 - phases 1 to 3 (b) Inverter 2 - phases 4 to 6

maximum current of 105, 122 and 122 A respectively. However, phases 1 and 2 will stay at the same current level as before the fault.

One inverter failure

The higher stresses in the dual inverter with a single phase failure will eventually lead to another phase in the subsystem failing. Assuming this is in the inverter that has already lost a phase, the system is converted so only the other fully operating three-phase inverter is powering its corresponding star machine within the six-phase PMSM. As the control of each inverter is independent, this failure mode is possible using the same control method that is used for each inverter at pre-fault operation.

The system operates similar to the three-phase IMD investigated in Chapter 4, however the dual inverter is designed with fewer paralleled MOSFETs so the current per device will be higher.

A summary of MOSFET required performance is provided in Table 5.2 for healthy and faulted conditions.

The phases are required to handle the current at peak operation under pre-fault conditions and therefore are capable of operating under the higher required per-phase current post-fault. Enabling the IMD to deliver the required torque and speed for normal operation after a fault has occurred. However, to maximise lifetime, the post-fault configurations are not designed to operate under peak conditions.

Table 5.2 Fault Conditions of the dual inverter system

Operation	**Max. Current per-phase (A)**		**Device current sharing**
	Normal	**Peak**	
Pre-fault	65	110	Equal
Phase failure	130	-	Unequal
Inverter failure	130	-	Equal

5.5 Electrothermal Analysis and Design Improvement

Implementing the end winding mounted IMD concept, where the inverter is positioned on the machine housing poses a complicated thermal problem. The MOSFETs in the inverter and the machine windings are heat sources; therefore, placing them in close proximity creates a thermal distribution problem. In Chapter 4 the optimisation problem assumes a constant temperature across the inverter MOSFETs and a constant heat sink temperature due to the inverter of 100°C. The detailed electrothermal design for a three-phase and dual three-phase inverter for a radially stator-mounted (RSM) axial flux integrated drive is introduced in this section. Improvements and redesigns are compared regarding thermal resistance, temperature uniformity of chips and overall temperatures.

5.5.1 Thermal Modelling

Thermal analysis, or thermal simulation, employs computational fluid dynamics (CFD), heat transfer, and finite element analysis to simulate and analyse heat distribution and thermal stress concentration [157]. The maximum operating temperature of the system is determined through heat distribution analysis to ensure that the MOSFETs junction temperature remains

within an acceptable range. Stress concentration analysis is performed to evaluate whether the study's reliability is affected. The thermal model proposed in this study is based on the thermal resistance network (TRN) and considers the physical integration of the motor and drive. It reveals that the integration leads to a significant thermal coupling between the motor and drive.

The impact of heat sink temperature on inverter volumetric power density and lifetime was shown previously in Chapter 4 . Using thermal analysis to more accurately predict the heat sink temperature at the surface contact points between base plate and the MOSFETs and redesign for more efficient thermal management can increase design accuracy and effectiveness.

Figure 5.11 shows the thermal model of the inverter system. The diagram illustrates how the junction temperature, T_j and the case temperature, T_c, the inlet coolant temperature, T_w are dependent on power loss from the MOSFET, P_{loss} and the thermal resistances of the MOSFET, thermal paste (or thermal interface materials (TIM)), and cold plate, $R_{th,j-c}$, $R_{th,t-p}$, and $R_{th,c-p}$, respectively. To simplify analysis, only the thermal behaviour of the MOSFET in the drive is analysed.

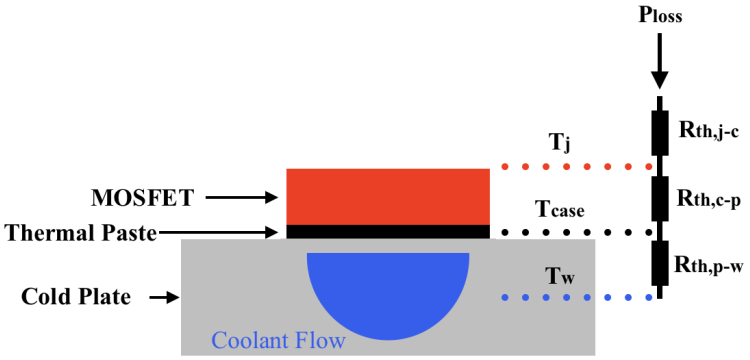


Fig. 5.11 Thermal resistance of the cold plate with different flow rate

It should be noticed that the thermal model shown in Figure 5.11 is a lumped one-dimensional thermal model, as is used in the PLECS simulation, which assumes all the MOSFETs having the same junction temperature. The case and junction temperature of the

module can be written as:

$$T_j = T_c + R_{th,j-c} P_{loss}/2 \tag{5.5}$$

$$T_c = T_w + (R_{th,t-p} + R_{th,c-p}) P_{loss} \tag{5.6}$$

It can be seen from 5.5 that the junction temperature is a function of coolant temperature, MOSFET power loss, and thermal resistances. Furthermore, the on-state resistance of the MOSFET, as well as the switching energy, is affected by the junction temperature, which means the junction temperature, in turn, determines the inverter power loss.

Although it is accurate to calculate the thermal resistances based on the materials of the MOSFET, the composition of the MOSFET is unknown. So, the $R_{th,j-c}$ and $R_{th,t-p}$ used are from the MOSFET datasheet. The system is tested at a switching frequency of 118 kHz, identified as the maximum feasible switching frequency in Chapter 4, to show the system under maximum thermal stress. The MOSFET losses under these conditions are modelled from the PLECS simulation and device look-up tables. Fig 5.12 shows an example of the losses during each switching cycle that is inputted into the CFD analysis as a steady thermal load. Using this cycle of losses allows the mean temperature, $T_{j(mean)}$, and the temperature swing, ΔT_j, to be analysed in the thermal investigation.

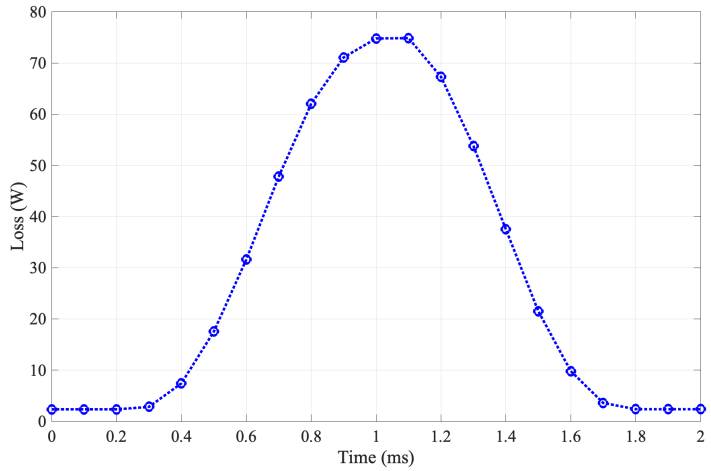
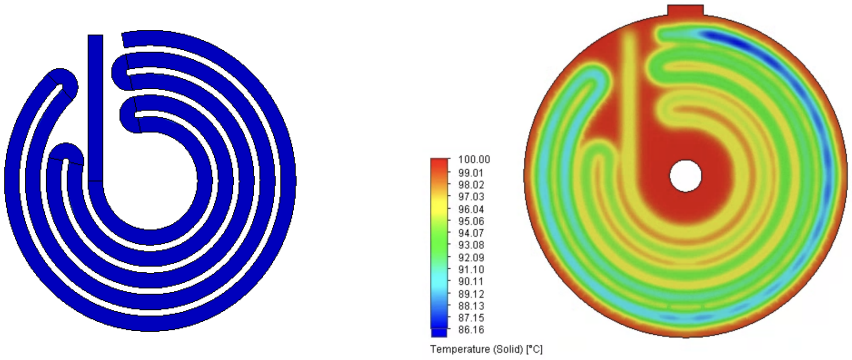


Fig. 5.12 MOSFET power Loss during one thermal cycle

5.5.2 Cooling System

The machine cooling system, shown in Fig 5.13a, circulates water to cool the outer plate of the motor which is shared by the inverter. In electric vehicles, the temperature the coolant usually enters the cold plate is approximately 70 °C [158]. Fig 5.13b shows the cold plate temperature when the machine is at 100 °C and the coolant water is at the input is 70 °C at a flow rate of 15 L/min. The simulation shows that the coolant temperature increases inside the cold plate, with the maximum and minimum plate temperature 100 °C and 86 °C respectively. The MOSFETs mounted to the board at higher temperature will experience higher junction temperatures and therefore lower lifetime.



(a) (b)

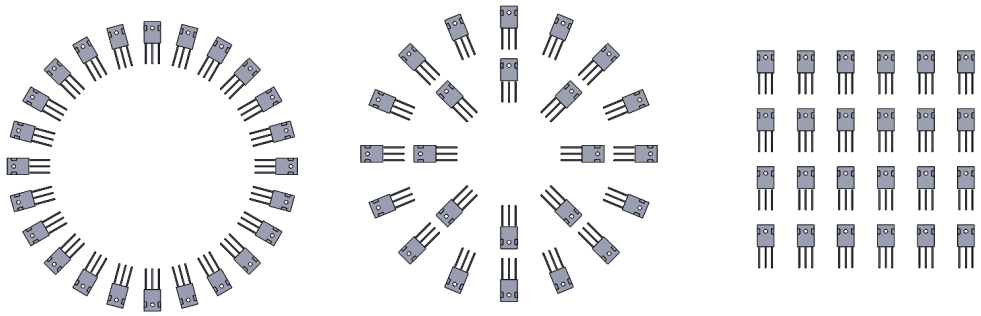
Fig. 5.13 PMSM cooling system (a) Shape (300mm diameter) (b) temperature profile with 100°C wall temperature and 70 °C coolant flowing at 15 L/min

5.5.3 Physical Layout

From the steady-state thermal analysis result shown in Figure 5.13b, it can be seen that the temperature distribution on the cool plate surface is not uniform due to the large size of the heat sink and the heat convection from the machine and coolant. To build a more accurate electrothermal model, the thermal characteristics of MOSFETs at different locations and arrangements on the cool plate needs to be evaluated.

The SiC MOSFETs are mounted on the 300mm diameter cold plate in three arrangements, shown in Figure 5.14 for an inverter system with 24 MOSFETs. The same arrangements are

used for any number of MOSFETs and the designs can be applied to both three-phase and dual three-phase inverter systems. In Figure 5.14b, the number of devices on the outer ring is always two-thirds of the total.



(a) (b) (c)

Fig. 5.14 MOSFET arrangements (a) Concentric (b) Concentric-2 (c) Square

Figures 5.15 shows how the concentric and concentric-2 arrangements change the junction temperature of the MOSFETs. $T_{j(min)}$, $T_{j(avg)}$ and $T_{j(max)}$ give the minimum, average and maximum junction temperature of the 24 MOSFETs on the cold plate in this example of a three-phase inverter with four paralleled MOSFETs or a dual inverter with two paralleled MOSFETs. The variation is down to the cooling flow interaction with the devices and the motor, shown in Figure 5.16.

Increasing the number of MOSFETs reduces the current per device, and therefore the device power loss. However, having to fit more MOSFETs on the cold plate will also result in smaller distances between devices, which can create problems with heat sharing, which was not considered in the previous thermal analysis in Chapter 4.

In analysis it was found that despite being closer together, the lower current per device when using more MOSFETs still results in lower $T_{j(mean)}$, ΔT_j and enhanced lifetime.

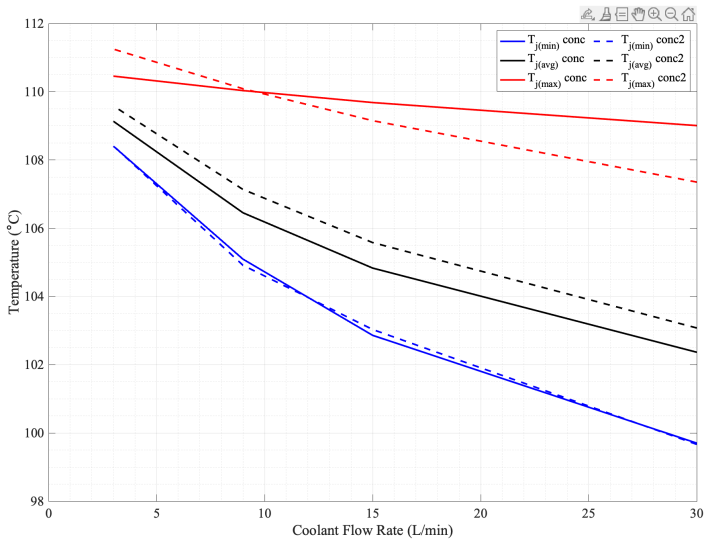


Fig. 5.15 Effect of coolant flow on MOSFET junction temperatures in the concentric and concentric-2 arrangements, for 70 °C coolant temperature

5.5.4 Method Comparison

Thermal analysis allows the optimal layout to be chosen for the IMD. An inverter set up in a concentric-2 arrangement on the cold plate with a forced water cooling system flowing at 15 L/min.

The higher accuracy that CFD analysis provides for the cooling allows more trustworthy results for the inverter design and its parameters. Table 5.3 compares the PLECS thermal results to the CFD simulation for 6 paralleled MOSFETs during normal operation with a switching frequency of 115 kHz for 15 L/min flow rate. The data show a decrease in expected maximum junction temperatures of 7.4 % and junction temperature swing of 4.8 %, resulting in an increase in lifetime for the analysis. This suggests the decrease in board temperature due to coolant flow will improve the performance of the inverter.

Table 5.3 Thermal analysis method comparison

	PLECS	**Solidworks**
$T_{j(max)}$ (°C)	123.2	114.1
ΔT_j (°C)	10.4	9.9
Lifetime (years)	30	42

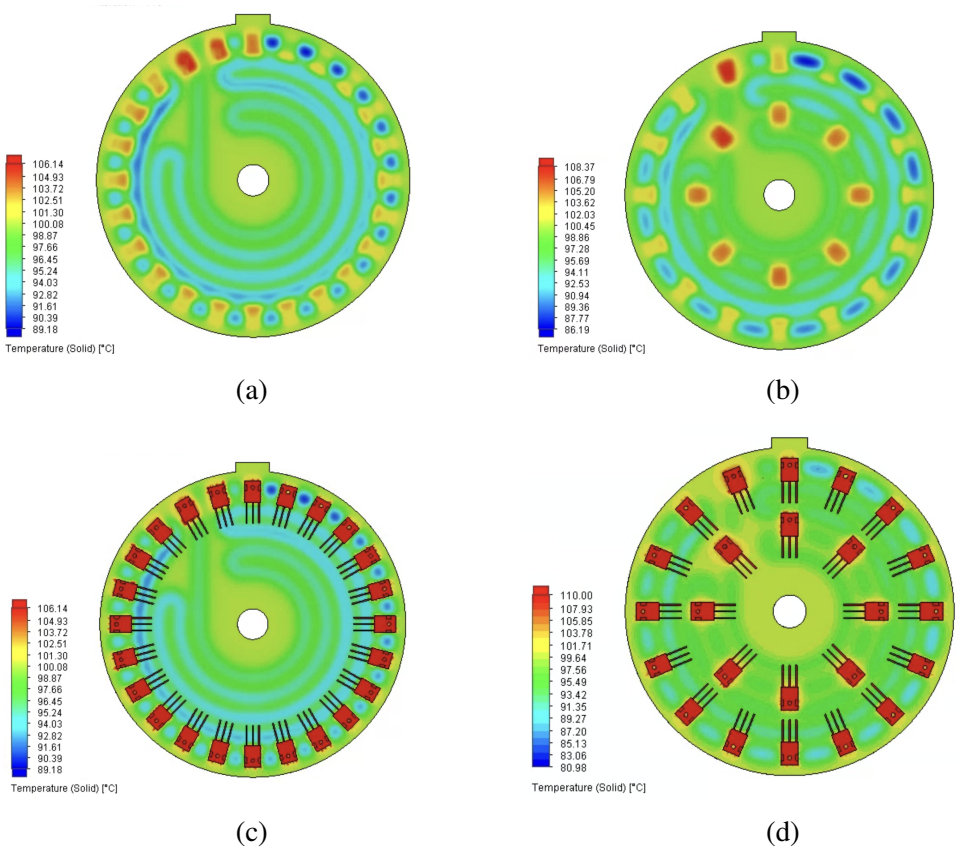


Fig. 5.16 Thermal analysis of the concentric and concentric-2 arrangements for 24 MOSFETs showing board and MOSFET irregularity, at a flow rate of 15 L/min and flow temperature of 70 °C

5.6 New Reliability Considerations

The Chapter 4 the lifetime model results in a fixed time to failure for the SiC MOSFETs due to bond wire fatigue. Therefore, failure of a single MOSFET was considered as failure of the entire power train system, as the lifetime of each was identical, resulting in simultaneous failure. In reality, differences in physical parameters and experienced stresses results in variance in the time to failure for the devices[159, 160]. Therefore, it is better to use percentile lifetime. B_x is the time when a group of samples has x probability of failure, to quantify the lifetime of a system or component. In the most recent reliability analysis the time when 1% of components will fail, B_1 time for 1% and the time when 10% of components will fail B_{10} are used to present lifetime of a component or system.

Monte Carlo simulation is presented to statistically analyse the lifetime subject to variations in relevant parameters. The subsequent step involves estimating the time-to-failure distribution of the power MOSFET considering these parameter variations. Finally, the system-level reliability is assessed using existing and novel approaches involving Markov chains and fault tolerance [161, 162].

5.6.1 Component Level Reliability Profiles

The lifetime model in [71] , expresses the cycles to failure N_f as:

$$N_f = K.\Delta T_j^{\alpha}.e^{E_A/k.T_{jm}} I_b^{\gamma} \tag{5.7}$$

where K is the basic constant, α is the Coffin-Manson exponent, ΔT_j is the junction temperature swing, E_A is the activation energy, k is the Boltzmann constant, $T_{j(mean)}$ is the mean junction temperature in Kelvin, β is the exponent for the duration of the load pulse, t_{on}, and γ is the exponent for the current per bond I_b.

With the assumption of linear cumulative damage, Miner's rule is applied to enable the analysis of the accumulated damage of the SiC MOSFETs [163, 164]. The entire life cycle can be divided into fractions for the different operating conditions of the mission profile. Based on the Miner rule, annual damage D can be calculated by

$$D = \sum \frac{n_{(i)}}{N_{f(i)}} \tag{5.8}$$

where n_i is the annual number of cycles for loading condition i, such as normal and peak operation, and $N_{f(i)}$ is the corresponding number of cycles to failure.

Variations in the lifetime model: Each lifetime model has its limitations due to the specific test conditions, device technologies, and the failure mechanism considered. As the lifetime model is based on power cycling data there is a level of uncertainty in the derived constant parameters. The uncertainty of the fitting coefficients corresponding to the junction temperature and its fluctuation are taken into account.

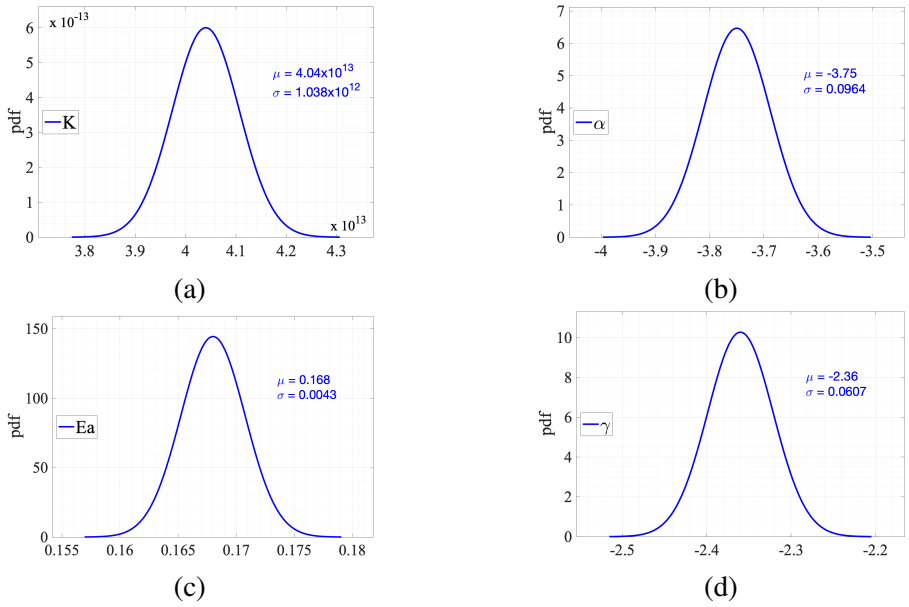


Fig. 5.17 Normal distribution of the factors from the strength model. (a) K, basic constant, (b) α, Coffin-Manson exponent (c) E_a, activation energy (d) γ, exponent for the current per bond

The parameters are modelled by normal probability distribution functions (PDF) assuming that K, α, E_a and γ experience a variation of 5% [165]. The data in Figure 5.17 shows the PDFs alongside the the mean value of the distribution, μ, and the standard deviation, σ. A sensitivity analysis is presented considering the effect on the annual damage of individual parameter variations, with the other parameters held at the mean value of their distributions. The distribution is sampled using Monte Carlo simulations with 10,000 samples to establish the accumulated damage distribution.

The annual damage distribution of a SiC MOSFET from the three-phase optimal inverter, considering variation to four parameters in the applied lifetime model, is shown in Figure 5.18. The red probability density function (PDF) can fit to the frequency occurrence data from the Monte Carlo simulations, showing a normal distribution. The sensitivity of the accumulated damage to K, α, E_a and γ can be evaluated both individually or collectively. Variation of α leads to the largest standard deviation of annual damage indicating that the lifetime model is more sensitive to this factor, demonstrating the importance of accurate simulation of the current per bond in this study. The lifetime distribution can be obtained

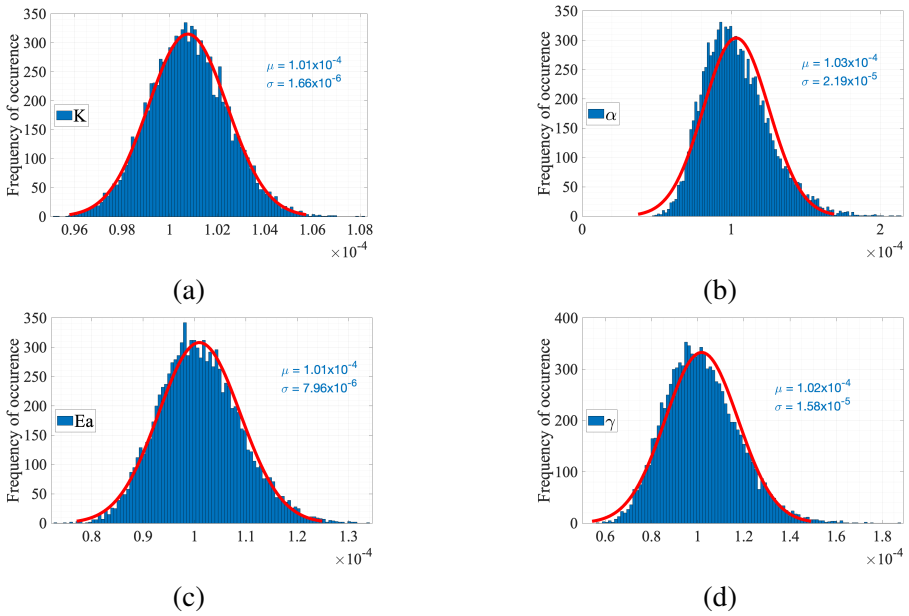


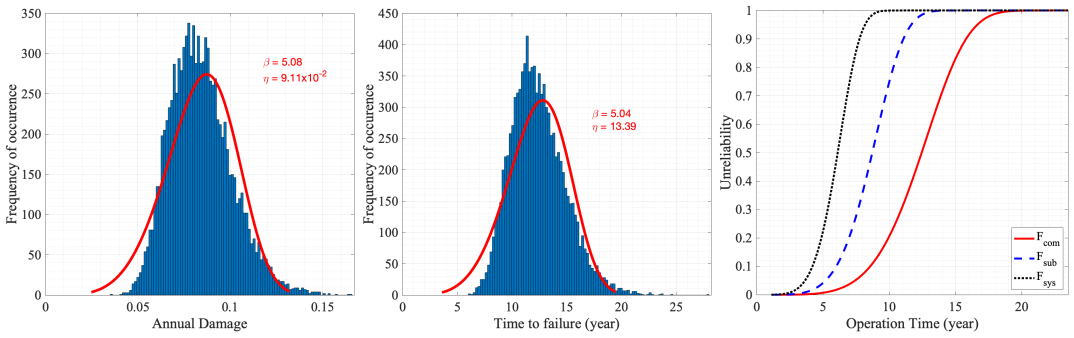
Fig. 5.18 Annual damage distribution considering the parameter variation in the lifetime model. (a) K, basic constant, (b) α, Coffin-Manson exponent (c) E_a, activation energy (d) γ, exponent for the current per bond

taking into account all parameter variations using Monte Carlo simulation. The time-to failure data is known to follow a Weibull distribution [162],

$$f(t) = \frac{\beta}{\eta}(\frac{t}{\eta})^{\beta-1}.exp[-(\frac{t}{\eta})^{\beta}] \tag{5.9}$$

where η denotes the scale parameter and β denotes the shape parameter.

The annual damage distribution is depicted with the Weibull parameters presented in Figure 5.19a. Figure 5.19b shows the expected lifetime distribution if the mission profile is repeated annually and finally, the unreliability or failure of the power switch, F_{com}, can be calculated. The cumulative distribution function (CDF), shown in Figure 5.19c is the integration of the PDF . It is noted that 10% and 1% of MOSFETs are predicted to have a failed after 8.6 and 5.4 years of operation.



(a) (b) (c)

Fig. 5.19 Monte Carlo analysis for lifetime calculation combining all parameter variation (a) Annual damage; (b) Time-to-failure distribution; (c) Unreliability

5.6.2 System Level Reliability Profiles

To assess the reliability of the IMD, the system can be divided into each set of paralleled MOSFETs in a 'switch', F_{sub}, and the entire system, F_{sys}. The failure of any MOSFET results in abnormal operation of the inverter. The failure function of the sub-system can be expressed by the component failure function, F_{com} [164, 166],

$$F_{sub}(t) = 1 - \prod_{i}(1 - F_{com(i)}(t)) \tag{5.10}$$

The reliability analysis of the inverter can then be estimated from the combination of the reliability analysis of each 'switch', where six are connected in a three-phase inverter. The cumulative distribution functions of the sub-system and system have been added to Figure 5.19c.

From literature, the case of m-out-of-n redundancy, the failure function of the system, F_{sys}, can be expressed as [161],

$$F_{sys}(t) = \sum_{i=0}^{m-1} \frac{n!}{i!(n-1)!}.(1 - F_{sub}(t))^{i}.F_{sub}(t)^{n-1} \tag{5.11}$$

The dual three-phase inverter is fault tolerant, however contains no redundancy so the equation is not applicable. The equations also do not consider changes in operating conditions

of the remaining MOSFETs after a failure, or the damage of the MOSFETs up to the point of initial failure so cannot be applied here.

Markov Chain methods

Another method for reliability analysis of fault tolerant power converters is using Markov Chains (MC), where each state in the MC model represents a separate system configuration, e.g., pre-fault operation, post-fault operation, and failure. For example, the FT power converter comprising three system configurations can be easily constructed into a three-state MC model as shown in Figure 5.20.

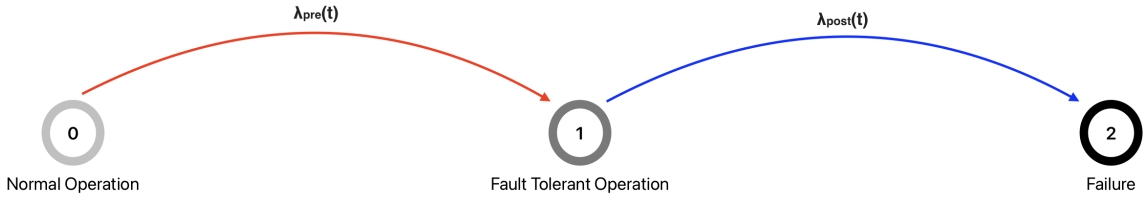


Fig. 5.20 Proposed reliability evaluation method based on Markov Chain model applied to fault-tolerant power converter with non-constant failure rates (i.e., $\lambda_{pre}(t)$ and $\lambda_{post}(t)$)

One important constraint when applying the MC model is that the failure rate between each state is time invariant, e.g., $\lambda(t) = \lambda$. This is applied to the system where the failure density function $f_{exp}(t)$ follows an exponential distribution as

$$f_{exp}(t) = \lambda \exp(-\lambda t) \tag{5.12}$$

$$\lambda_{exp}(t) = \frac{f_{exp}(t)}{\int_t^{\infty} f_{exp}(t)dt} = \lambda \tag{5.13}$$

where it can be seen from equation 5.12 that the failure rate $\lambda_{exp}(t)$ of the exponential distribution is constant.

Assuming a constant failure rate the MC model of the FT power converter in Figure 5.20 can be constructed with the following state equations:

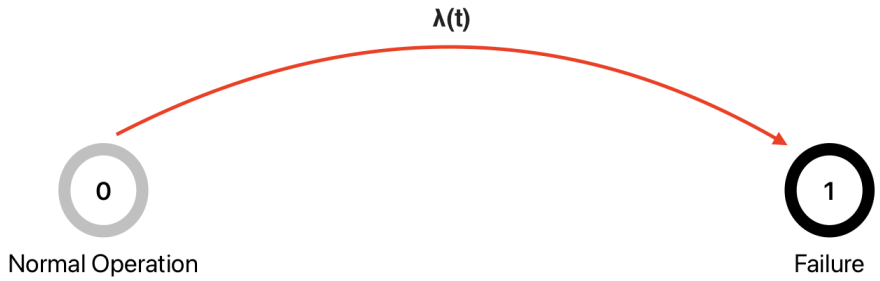
$$\begin{bmatrix} \dot{P}_0(t) \\ \dot{P}_1(t) \\ \dot{P}_2(t) \end{bmatrix} = \begin{bmatrix} -\lambda_{pre} & 0 & 0 \\ \lambda_{pre} & -\lambda_{post} & 0 \\ 0 & \lambda_{post} & 0 \end{bmatrix} \cdot \begin{bmatrix} P_0(t) \\ P_1(t) \\ P_2(t) \end{bmatrix} \tag{5.14}$$

By solving the state equations in 5.14, the time-dependent probability of the system being in State 0, $P_0(t)$, State 1, $P_1(t)$, and State 2, $P_2(t)$ corresponds to the probability that the power converter will be in normal operation, fault tolerant operation, and failure, respectively. Since the power converter is in operation when the system is in either State 0 or State 1, the reliability of the power converter, $R(t)$, can be determined as:

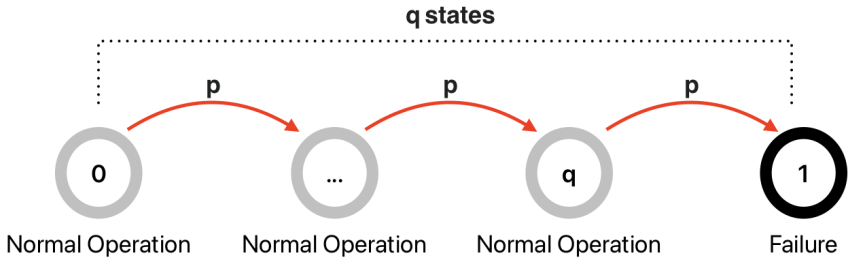
$$R(t) = P_0(t) + P_1(t) = 1 - P_2(t) \tag{5.15}$$

Conventional Monte Carlo simulation does not determine the damage level of any samples remaining after initial failure [12]. Therefore it has low accuracy in fault tolerant systems as they have multiple states of operation and the accumulated damage during pre-fault operation must be taken into account as an initial damage during the post-fault operation.

To solve this problem, a method based on MC theory and an incremental damage concept known as the method of stages was proposed to incorporate a non-constant failure rate in the MC model [167]. For this method, the accumulated damage of each sample is periodically increased annually. It has been demonstrated in [165] that the failure rate with the Weibull distribution in Figure 5.21a can be represented by a series combination of multiple states with an exponential failure rate, as shown in Figure 5.21b.



(a)



(b)

Fig. 5.21 Markov Chain model of non fault-tolerant power converter represented by: a) Weibull distribution failure rate $\lambda_{wb}(t)$ and b) method of stages with q states with exponential distribution failure rate of p

If all the q states that are connected in series are identical (e.g., with the same failure rate p), the total failure density function of the series combination in Figure 5.21b becomes the Special Erlangian distribution $f_{se}(t)$ as

$$f_{se}(t) = \frac{p(pt)^{q-1}}{(q-1)!}\exp(-pt) \tag{5.16}$$

where p is the failure rate of each exponential state and q is the number of states connected in series.

To represent the Weibull distribution with the Special Erlangian distribution, the first and the second moments of the two distributions need to be identical. From 5.16, the first and second moments of the Special Erlangian distribution, m_1 and m_2, can be expressed as:

$$m_1 = \frac{q}{p}, \qquad m_2 = \frac{q(q+1)}{p^2} \tag{5.17}$$

while the first two moments of the Weibull distribution, M_1 and M_2, can be obtained from 5.16 as:

$$M_1 = \eta\Gamma\left(\frac{\beta+1}{\beta}\right), \qquad M_2 = \eta^2\Gamma\left(\frac{\beta+2}{\beta}\right) \tag{5.18}$$

By solving $m_1 = M_1$ and $m_2 = M_2$, the number of states in the series combination q and the constant failure rate of each state p can be identified as

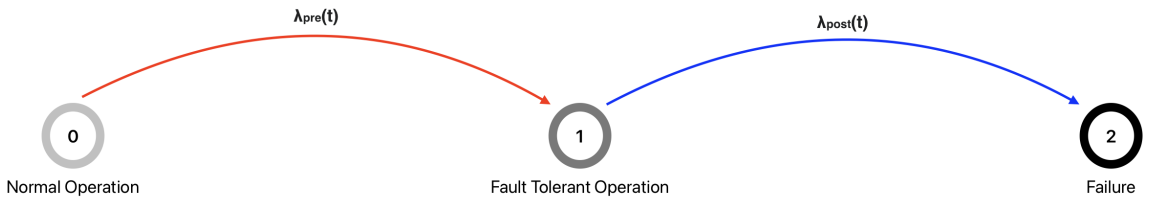
$$q = \frac{M_1}{M_2 - M_1^2}, \qquad p = \frac{M_1^2}{M_2 - M_1^2} \tag{5.19}$$

where it should be noted that the number of states q may need to be rounded up to the nearest integer number.

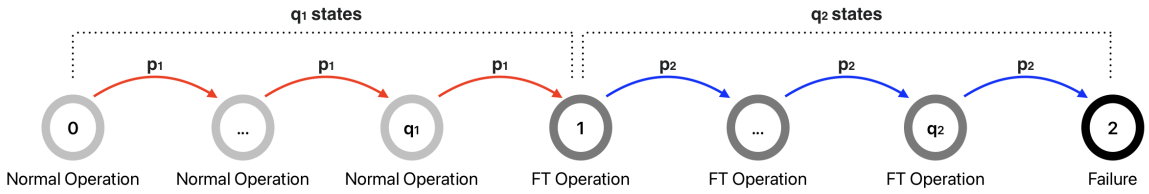
Multi-state models

The MC model of an inverter with three operating states is illustrated in Figure 5.22a.

The method of stages can be applied to the MC model of the FT power converter by substituting the state described by a Weibull distribution with a series combination of states with exponential distribution, as illustrated in Figure 5.22b. Then, the state equations of the



(a)



(b)

Fig. 5.22 Markov Chain model of fault-tolerant power converter represented by: a) Weibull distribution where $\lambda_{pre}(t)$ and $\lambda_{post}(t)$ are the failure rates during pre-fault and post-fault operation, respectively, and b) method of stages with $q1$ states representing the pre-fault operation with exponential distribution failure rate of $p1$ and $q2$ states representing the post-fault operation with an exponential distribution failure rate of $p2$

MC model can be constructed and solved in a manner similar way to that demonstrated in 5.14. However, it should be noted that the dimension of the transition rate matrix in the state equations now becomes $(q_1+q_2+1)\times(q_1+q_2+1)$ instead of 3×3 as in 5.14. By solving the state equations, the reliability of the FT power converter can be determined by taking into account all the states that correspond to operation (e.g., normal and FT operations) of the power converter as

$$R(t)=\sum_{i=1}^{q_1}P_{1,i}(t)+\sum_{j=2}^{q_2}P_{2,j}(t)=1-P_3(t) \tag{5.20}$$

where $P_{1,i}(t)$ is the probability of being in the i^{th} state of the pre-fault operation while $P_{2,j}(t)$ is the probability of being in the j^{th} state of the post-fault operation.

Three-Phase Case Study

In the optimised three-phase inverter studied in Chapter 4, as six MOSFETs are paralleled in each ‘switch’, when one MOSFET fails the remaining paralleled devices allow the system

to continue operating. However, the remaining devices experience higher load currents and therefore increased stress. The MC for one of the six 'switches' is shown in Figure 5.23. In this example study the inverter is operating at 50 kHz and the thermal environment is based on the CFD thermal analysis for a coolant flow of 70°C at 15 L/min.

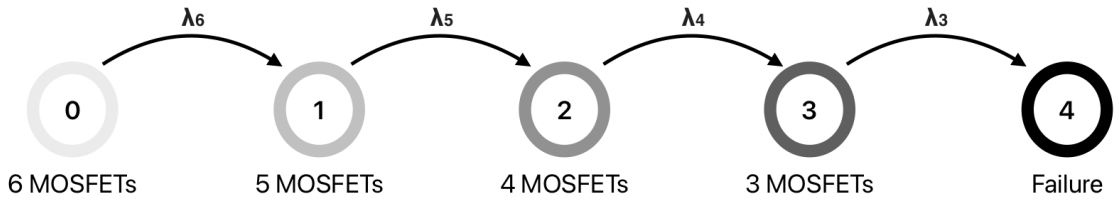


Fig. 5.23 Markov chain for three-phase inverter 'switch' with six paralleled MOSFETs

Pre-fault operation: In the pre-fault operation, when all six paralleled MOSFETs are operating normally, the proposed Monte Carlo simulation method is applied to periodically increase the damage on the yearly basis. Figure 5.24 shows the accumulated damage after 10 years, showing the proportion of samples that have failed as those with a damage greater than 1. This process can keep repeating until all the samples reach its end-of-life.

Post-fault operation: When the first MOSFET fails, which is assumed to be when $1/6^{th}$ of the samples have failed in the Monte Carlo simulation, the conditions for the remaining five MOSFETs change and a there is a new failure rate. During the post-fault configuration, the initial damage of the power devices that have survived the failure is taken from the accumulated damage when the fault occurs. Therefore, the devices fail more rapidly after the initial fault due to the increased stress and previously accumulated damage. This is reflected in the shorter lifetime distribution of 5 paralleled MOSFETs, shown in Figure 5.25.

A comparison between the unreliability function of the 6 MOSFET and 5 MOSFET operation is shown in Figure 5.26.

The method of stages can be applied to convert the states with Weibull distribution into an equivalent series combination of states with exponential distribution following Figure 5.25. Then, the reliability of the three-phase inverter can be determined from the MC model shown

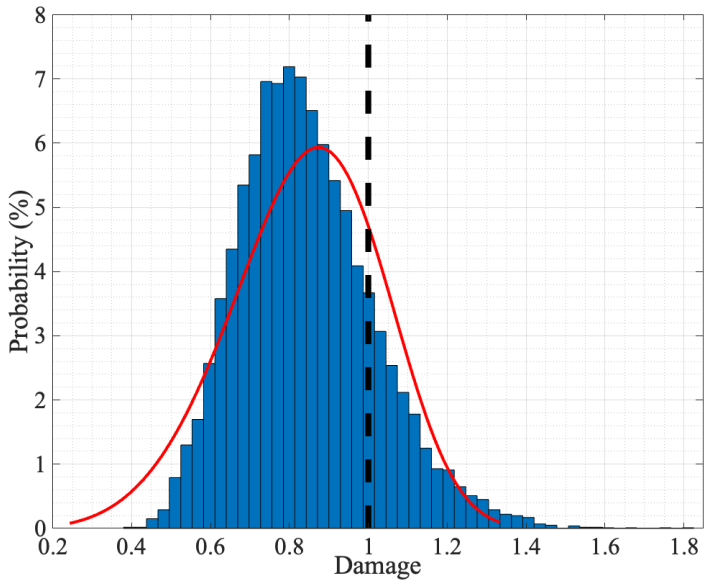


Fig. 5.24 Reliability analysis of three-phase inverter with the proposed Monte Carlo simulation method showing accumulated damage distribution after 10 years. Where the failed devices, those with damage over 1 are highlighted.

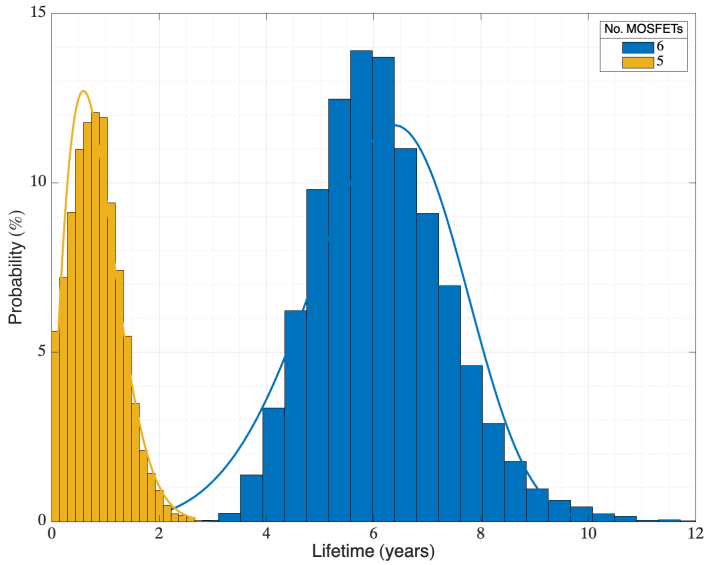


Fig. 5.25 Reliability analysis of three-phase inverter with the proposed Monte Carlo simulation method showing accumulated damage distribution after 10 years

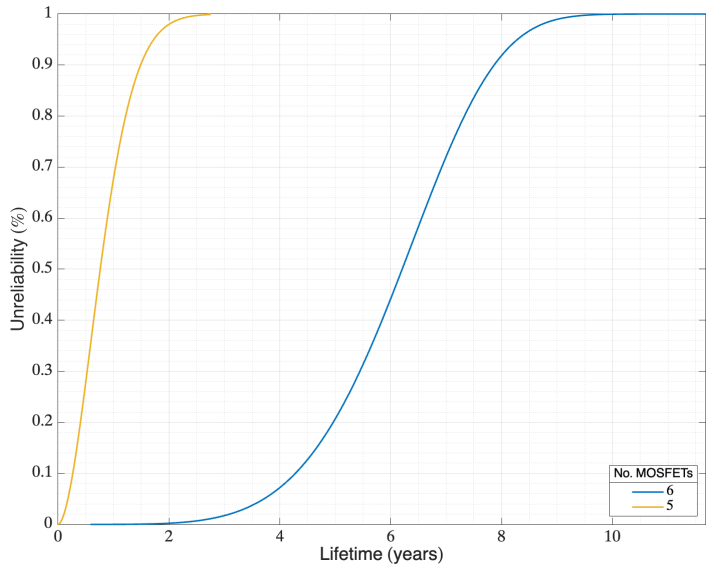


Fig. 5.26 Unreliability of pre-fault (6 MOSFETs functioning) and post fault (5 MOSFETs functioning) operation

in Figure 5.23. By solving the state equations, the reliability of the 'switch' sub-system can be obtained. Equation 5.10 is then used to calculate the reliability of six of these subsystems in the inverter.

Figure 5.27 shows the failure distribution data for the component, F_{com}, and for the three-phase system using equation 5.10 for the subsystem, F_{sub} and the system, F_{sys} and using the new incremental damage method for the subsystem and system.

The new method takes into account the fault tolerance of paralleling MOSFETs and therefore the system has a much higher lifetime. The B_{10} lifetime of one MOSFET is 8.4 years which reduces to 4 years when considering the full system with no fault tolerance. Using the new MC and incremental damage model the system B_{10} lifetime is more than double, at 9.7 years because of the fault tolerant nature of paralleling MOSFETs.

5.6.3 Dual three-phase Case Study

The MC for the dual three-phase inverter with three paralleled MOSFETs is shown in Figure 5.28. Unlike the three-phase, the dual inverter can operate after a subsystem 'switch' has failed and has multiple levels of fault tolerance.

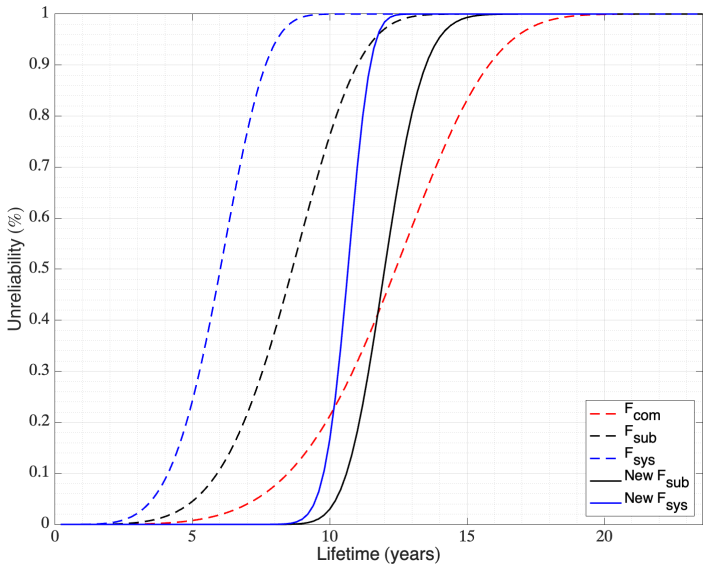


Fig. 5.27 Reliability analysis of three-phase inverter with the proposed Monte Carlo simulation method showing accumulated damage distribution after 10 years

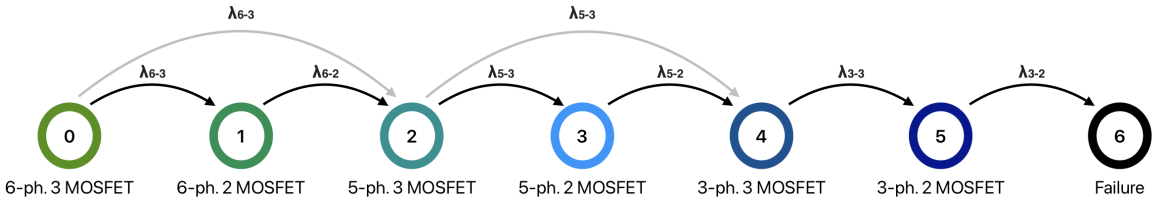


Fig. 5.28 Markov chain for dual three-phase inverter, with fault tolerant conditions

When the first MOSFET fails, the remaining 2 devices operate under new conditions and, due to this increased stress, are assumed in this work to be the next components in the system to fail. When the next MOSFET fails, the inverter begins to operate as a five-phase inverter. The cumulative damage to the MOSFETs in the five remaining operating phases depends on the expected time for two MOSFETs in the failed phase to fail and the failure rate based on the conditions of six-phase operation with 3 parallel MOSFETs, λ_{6-3}.

A similar process occurs, with the inverter converting from five-phase to three-phase before eventually failing. The time of each change of state is reduced because of the previously accumulated damage and the increased stress on the MOSFETs when fewer phases are operational.

The new method for reliability calculation can be used to calculate a more accurate lifetime for any converter system, allowing the effect of system design and the number of devices used to be investigated. The calculation requires conditions for the MOSFETs under each operating mode which are taken from the PLECS simulation in this project.

5.7 Optimisation of Dual Inverter IMD

The dual three-phase inverter configuration, shown in Figure 5.5, has been shown to offer several advantages over traditional three-phase inverters, such as increased fault tolerance and improved efficiency. However, there is still a need for further investigation to determine the extent of these benefits and how they compare to traditional three-phase inverters within the developed optimisation procedure. To maximise the volumetric power density, the selection of the DC-link capacitor and the switching frequency need to be optimised for both while considering the effect on lifetime. The new reliability calculations are used in the optimisation procedure to identify more accurately an optimal design for each fault tolerant power train system, allowing the best suited topology for the IMD application to be determined.

5.7.1 Effect of Switching Frequency on Inverter Operation

Many of the comparisons observed in this section are due to the same electrical processes and relationships as in the three-phase inverter analysis from Chapter 4. The data in Figure 5.29 show the variation in voltage ripple, ΔV_{pp}, total current harmonic distortion (THD), maximum junction temperature of SiC MOSFETs, $T_{j(max)}$, inverter efficiency and lifetime with switching frequency, f_{sw}, for operation of a dual three-phase inverter with two and three paralleled MOSFETs under normal and peak operating conditions. The lifetime data is presented in terms of hours of operation until failure, calculated from the mean number of cycles to failure for the MOSFET in the inverter experiencing the highest stress.

The voltage ripple, and current THD caused by high-frequency currents as a result of MOSFET switching, both decreases as the switching frequency increases because shorter

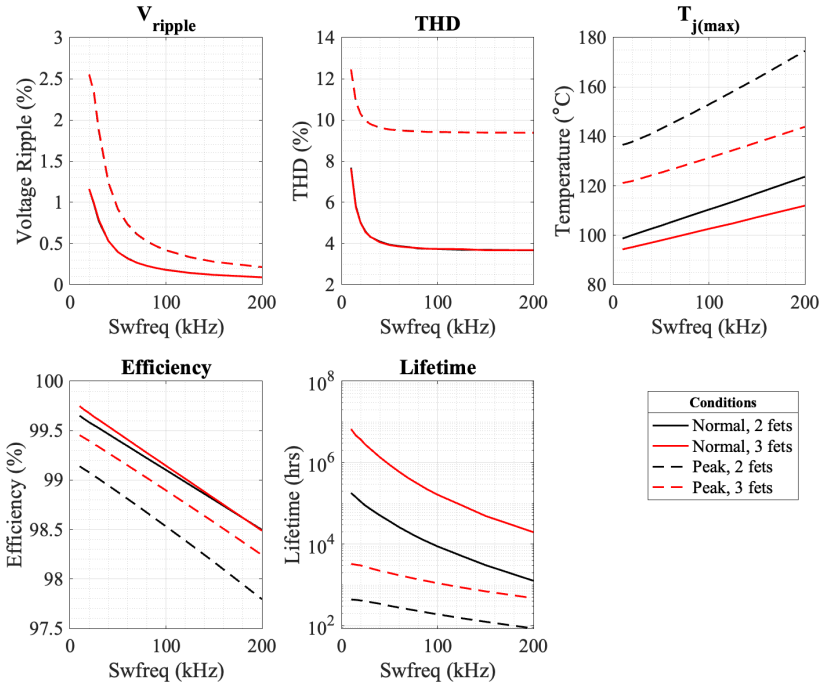


Fig. 5.29 Inverter parameters as functions of switching frequency for a 250 μF capacitor at each inverter, comparing number of paralleled MOSFETs and operating conditions

switching times mean less time for the ripple to affect the DC voltage. However, the effect of the switching frequency diminishes, especially for the THD, with no effect above 70 kHz.

As in the conventional three-phase inverter, the data show that efficiency is inversely proportional to the switching frequency. This is attributed to the increase in overall power loss as a result of the increase in switching losses. These losses have a direct impact on the maximum junction temperature $T_{j(max)}$, and are also partially responsible for variations in the lifetime. The data shows that $T_{j(max)}$, efficiency, and power losses are linked linearly to the switching frequency, with minimal variations due to DC-link capacitance.

The data shows that increasing the number of devices improves the performance of the inverter by decreasing the power losses and $T_{j(max)}$ and therefore improves the lifetime a factor of twenty times under 100 kHz at normal operation when increasing from 2 to 3 MOSFETs. This large difference in lifetime can be explained by the lower load current per device when 3 MOSFETs are used which directly decreases the N_f calculation by 62 % due to the i_b^γ factor. The higher load current also leads to greater $T_{j(max)}$ and ΔT_j explaining the further increase. It is worth noting that with fewer devices, the system is less fault tolerant as

a phase will fail after only one device failure if only two are paralleled. This is because the load current will be well beyond the rating of a single MOSFET leading to very short lifetime. Using fewer devices reduces the statistical probability of failure in a single device in the system but the increased stress is a more important factor in the design due to its significant effect on lifetime.

The total power loss, and therefore efficiency is similar when using 2 or 3 MOSFETs at normal operation due to the relationship between conduction and switching losses. The conduction losses are equal to $R_{ds(on)}I^2$ and when more devices are used, the total resistance decreases, resulting in lower conduction losses.

Switching losses are dependent on MOSFET capacitances, as discussed in detail in Chapter 3. With more devices in parallel the total gate charge and capacitance increases resulting in higher switching losses; however, this effect is less significant than the decrease in conduction losses.

The losses caused by conduction are independent of f_{sw}, however, at higher frequency when paralleling extra devices the switching losses increase at a higher rate, so above 185 kHz 3 paralleled devices experience greater losses than 2 devices. The difference under peak conditions shows these relationships change depending on the load current and it is important to investigate through simulation under the specific testing conditions the design is based on.

Fault Conditions

Figure 5.30 shows how the electrical characteristics of the inverter with 3 paralleled MOSFETs compare for pre-fault and fault-tolerant operating modes for normal operation. The data shows the impact of switching frequencies between 10 and 200 kHz and DC-link capacitor value of 250 μF in each inverter subsystem. The voltage ripple, THD and $T_{j(max)}$ are maximum values from system if the dual inverters are nonidentical in post-fault conditions. The THD during inverter operation after a one-phase fault is significantly higher than during pre-fault operation or after the failure of single three-phase inverter. When the inverter is operating with a one-phase failure, the symmetric six-phase PMSM now requires nonidentical inputs in each phase to balance the torque and speed of the load. This can cause voltage

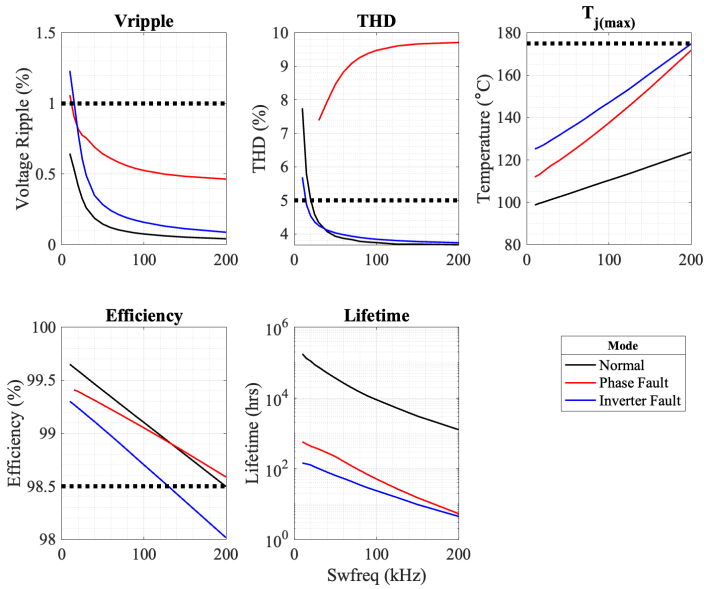


Fig. 5.30 Inverter parameters as functions of switching frequency for a 250 μF DC-link capacitance, comparing normal and fault tolerant modes

imbalances and increase voltage ripple and current THD as the inverter's output current is affected by voltage fluctuations.

In an unbalanced system, the phase currents are not equal in magnitude or phase angle resulting in uneven switching of the MOSFETs. This can generate harmonics in the output current leading to an increase in the THD. At higher switching frequencies, the pulse width of each switching cycle decreases, which can result in an increase in the high-frequency harmonic content in the current waveform. Therefore, increasing the switching frequency can increase the THD of the output current in an unbalanced system. After another fault, the system operates as a balanced three-phase system and the current THD becomes similar again to the pre-fault operation although the voltage ripple is higher as the load current per phase is double.

Comparisons with three-phase IMD

The six-phase PMSM and dual inverter system is used in literature for higher fault tolerance and efficiency. The data in Figure 5.31 and 5.32 shows the differences in the circuit charac-

teristics between the three-phase system and six-phase system for a DC-link of total DC-link capacitance of 500 μF across a range of switching frequencies for normal operation.

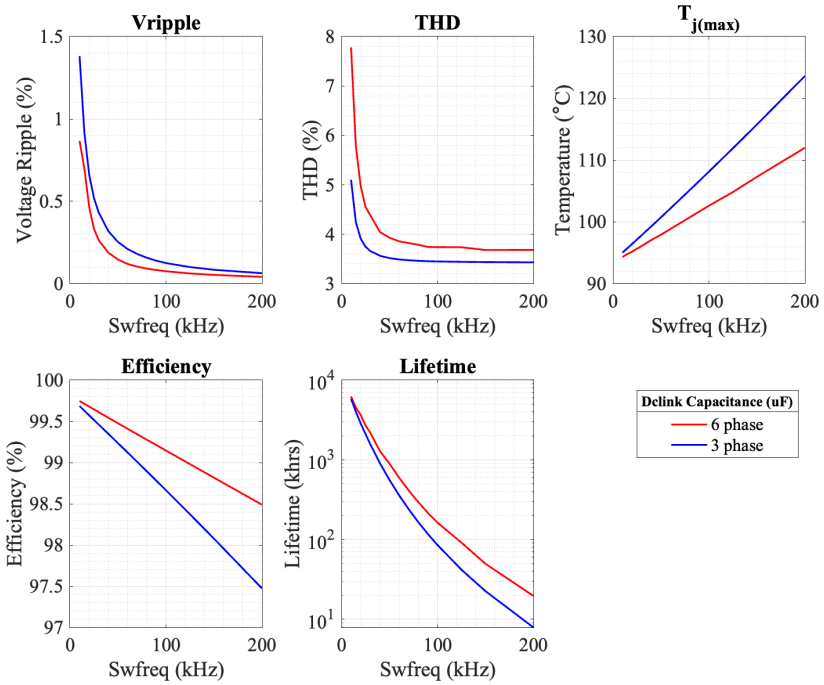


Fig. 5.31 Inverter parameters as functions of switching frequency with decreasing the number of paralleled MOSFETs under normal operating conditions, 50°C for a 250 μF capacitor

The DC-link voltage ripple in a six-phase inverter is generally smaller than that in a traditional three-phase inverter because increasing the number of phases results in a smoother voltage output and waveforms with less distortion and smaller current harmonics [39]. A smaller DC-link voltage ripple in the six-phase inverter means a smaller capacitance is required to meet to optimisation constraints.

In general, the current THD is lower in a six-phase inverter system compared to an equivalent three-phase system because the dual three-phase inverters provide a more balanced and symmetrical waveform with less distortion. Additionally, the dual inverter system provides better control over the motor, resulting in improved efficiency and reduced losses.

The same number of MOSFETs are used in both systems, so the current per device will be identical. However, the efficiency of the six-phase inverter is higher. The lower voltage ripple and THD are factors, and the control systems that have been described previously will also impact the power losses in the system. The control allows matching outputs from the

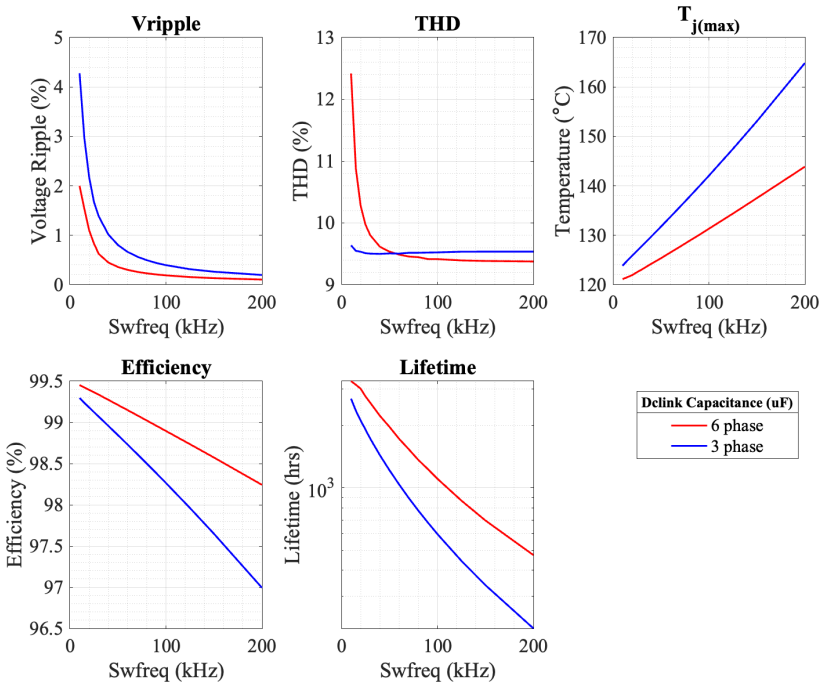


Fig. 5.32 Inverter parameters as functions of switching frequency with decreasing the number of paralleled MOSFETs under normal operating conditions, 50°C for a 250 μF capacitor

motors and has been chosen based on literature recommendations for IMDs and multi-phase systems. For example, decreasing the dead time in the dual inverter control will increase MOSFET power losses and change the relationship between many of the parameters of interest in the two systems.

In summary, the six-phase PMSM system with dual three-phase inverters provides a more efficient and balanced power output, leading to lower THD, reduced DC-link voltage ripple, lower device power losses, and higher efficiency. However, optimisation of both the six-phase and three-phase systems using the new thermal and reliability procedures should be completed to compare the systems overall and determine which is more suitable for a highly reliable IMD.

5.7.2 Multi-objective Optimisation with System-level Reliability

The multi-objective deterministic optimisation procedure developed in Chapter 4 was utilised to determine the relationship between volume and reliability, when lifetime is calculated

using the new process involving Markov chains. The multi-objective optimisation problem is analysed to seek the Pareto optimal solutions, making it possible to visualise the trade-off between power density and lifetime, and determine a number of optimal solutions and compare the three-phase to the dual inverter. The constraints on the optimisation are the same as in Chapter 4 and are shown in Table 5.4. The same constraints are put on the post-fault operation of the dual inverter as peak operation of the three-phase inverter. Volume is calculated from the summation of the DC-link capacitor volume and the SiC in TO-247 package used in the inverter. This makes it useful for comparison but does not reflect the true system volume. Once an optimal design has been identified a calculation of power density based on the PMSM cold plate diameter and height of the capacitors is possible to compare to other IMDs from literature. The Pareto front of the lifetime and volume for the three-phase

Table 5.4 Design Example Specification and Constraints

Specification	**Normal Operation**	**Peak/Post-fault Operation**
Rated Power	60 kW	120 kW
DC-link Voltage (V_{dc})	650 V	650 V
Maximum Junction temperature	175°C	175°C
Ambient temperature	70°C	70°C
Max. DC-link voltage ripple(ΔV_{dc})	1% of V_{dc}	2% of V_{dc}
THD limit	5%	10%
Minimum converter efficiency(η)	98.5%	97.5%

design with six parallel MOSFETs and dual inverter with three parallel MOSFETs is shown in Figure 5.33 and the data in Figure 5.34 show the corresponding switching frequencies. The lifetime has been calculated using the developed incremental damage method, requiring input of the device junction temperature and current from the PLECS and Solidworks simulations.

The multi-objective solution is limited by the points *A* and *C*. Point *A* represents the inverter design with the highest volumetric power density, while *C* is the most reliable and has the longest expected lifetime. The switching frequency limit for the three-phase inverter is 118 kHz , point 3*A* , because the efficiency under normal operation at this point is at the constraint on efficiency of 98.5 %. The dual inverter has a higher efficiency, as shown in Figure 5.31, and therefore has feasible designs at a higher switching frequencies, up to point 6*A* at 185 kHz. Point 3*C* is the lower limit of switching frequency at 13 kHz, any lower

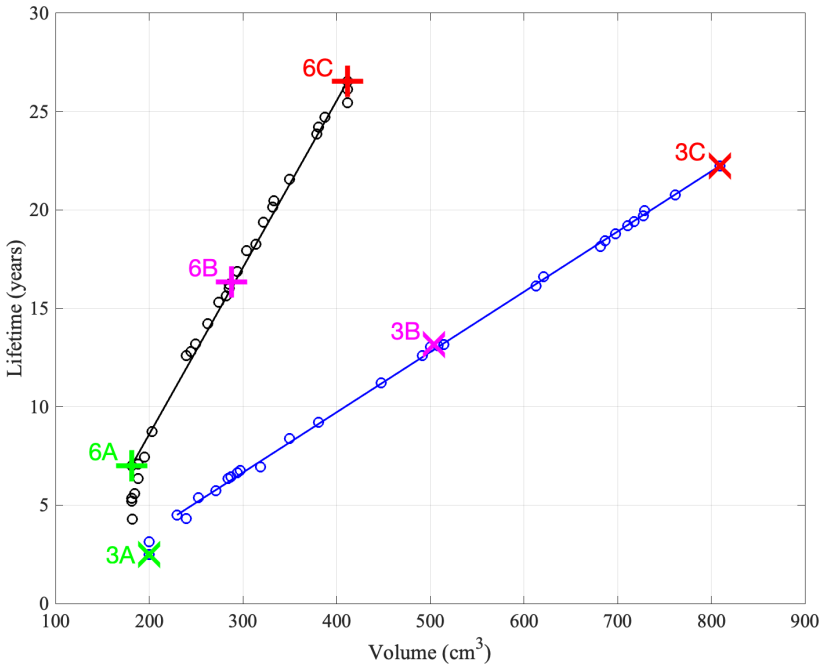


Fig. 5.33 Multi-objective optimisation results considering lifetime and volume for the combined operation of the system, comparing three-phase and dual inverter, with key points identified

fails to meet the maximum THD limit of 5 % under normal operation. Although at high switching frequencies the current THD is lower in the dual inverter system. The THD only falls below 5% at 29 kHz. The increased switching frequency between points *A* and *C* results in a volume and lifetime decrease because they are both inversely proportional to f_{sw}.

The lifetime of the dual inverter is higher than the three-phase inverter for any given switching frequency. The calculated number of cycles to failure for both inverters is similar under normal operation but the significantly higher lifetime at peak operation and the fault tolerant nature of the dual inverter means the expected lifetime is much greater. For example, at 60 kHz the dual inverter has a lifetime of 12.5 years, double that of the three-phase, and a volume of 250 cm^3, which is a decrease of 16 % in comparison to a three-phase system of equivalent rating.

In multi-objective optimisation, the designer must employ data-driven decision-making strategies that take into account the intended application of the inverter system in order to arrive at an optimal design solution. Point 3*B* and 6*B* represent a compromise of the

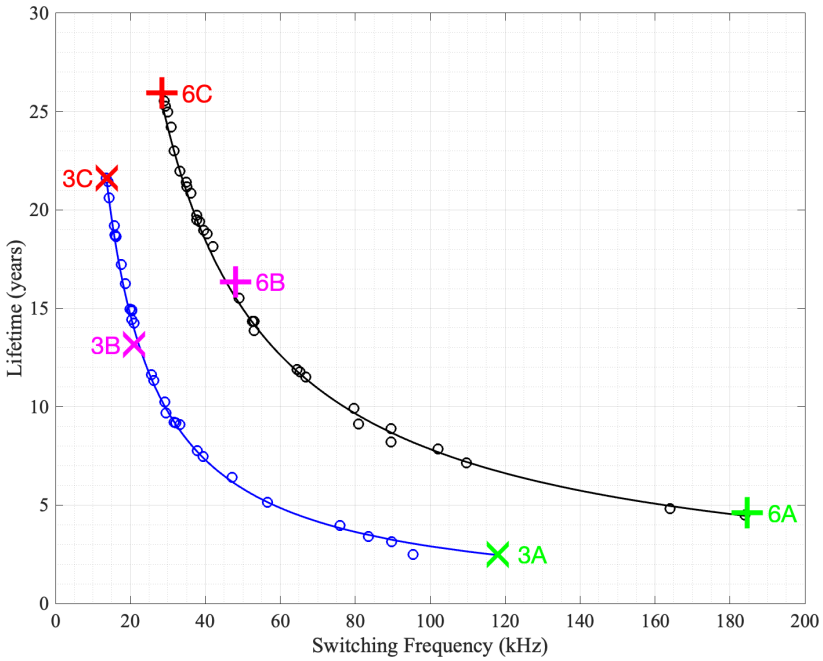


Fig. 5.34 Multi-objective optimisation results considering lifetime and switching frequency for the combined operation of the system, comparing three-phase and dual inverter, with key points identified

fitness functions, given by weighting lifetime and volume equally in the optimisation for both inverters. Point $3B$ is a design with a volume of 505 cm^3 and a lifetime of 13.2 years, requiring a switching frequency of 22 kHz and a DC-link capacitance of 260 μF. Point $6B$ is a design with a volume of 286 cm^3 and a lifetime of 16.3 years, requiring a higher switching frequency of 45 kHz and therefore a DC-link capacitance of 136 μF, or 68 μF for each of the dual inverters.

5.7.3 Design Summary

From Chapter 4 the optimal design was a DC-link capacitor of 190 μF, operating with a switching frequency of 45 kHz giving a volume of 440 cm^3 and a mean lifetime of 12,000 hours of operation, or 12 years when considering the weekly use assumed in this work. Using the new reliability and thermal analysis, a 45 kHz, 440 cm^3 design gives a predicted B_{10} lifetime of 12.8 years. This value is similar however the process to arrive at this value is very

different and the B_{10} value is much more useful, accurate and reliable in novel reliability analysis.

The dual inverter system is clearly superior in terms of performance for an IMD using the same number of discrete MOSFETs. However, not all systems are suited to a six-phase PMSM over a three-phase PMSM and for automotive applications three-phase PMSMs are more frequently used due to their high torque density and efficiency. This methodology allows the designer to choose the optimal inverter for both. It is useful and novel information to accurately compare the inverters themselves as has been done in this chapter.

The optimal inverter considering the design constraints for the dual inverter system, shown by point 6*B*, has a DC-link capacitance of 136 μF, operating with a switching frequency of 46 kHz giving a theoretical volume of 286 cm^3 and a lifetime of 16.3 years. The capacitor bank can be implemented using four 40 μF KEMET film capacitors, two in series in each three-phase inverter, giving a final volume that includes the 36 SiC MOSFETs of 300 cm^3. This results in a capacitor hot spot temperature of 86 °C, therefore the capacitor lifetime is comfortably above those of the MOSFETs at just under 20,000 hours. For a designer considering only a three-phase motor, for the same inverter volume, the lifetime is 58% shorter at 6.8 years, which is a significant disadvantage in an IMD system.

When considering the true inverter volumetric power density for the system to compare to other IMDs it is pertinent to consider the height of the capacitors. The 40 μF KEMET film capacitors have a height of 50mm and therefore the volume of the inverter through this method is 3.5 litres, giving a volumetric power density of 40 kW/l.

5.8 Summary

A multi-phase integrated drive system is investigated and optimised using PLECS simulation, detailed thermal analysis and a novel lifetime prediction procedure in this chapter. These studies allow optimal parameter selection alongside other important design decisions such as control methods, including fault tolerant designs, as well as thermal management and

physical layout considerations. Therefore, new optimal IMD systems are identified and compared in this chapter which is the focus of the research in this thesis.

The potential benefits of multi-phase systems and dual inverters have been covered in literature, but rarely have they been applied in IMDs. Lower per-phase current, interleaving strategies and fault tolerance were found to improve the performance compared to equivalent three-phase systems. The development of two post-fault operating modes, a five-phase system and a three-phase system consisting of one of the dual inverters was investigated to greatly increase reliability, a highly attractive prospect in an IMD where lifetime may be restricted due need for low volume and high-temperature environment.

A Cauer network is used to model the transient thermal behaviour of the MOSFETs in PLECS simulations up to this point. A CFD and 3D finite element thermal modelling are designed to study the inverter behaviour based on the thermal analysis of its shared cooling plate with a 300 mm diameter axial flux PMSM. This allows improved accuracy which can be used in the optimisation of the system but also allowed design considerations such as MOSFET positioning and effect of coolant flow rate to be investigated.

A new method for lifetime prediction of systems with paralleled MOSFETs or fault tolerance capabilities is developed based on TO-247 lifetime calculations, component-level reliability profiles using Monte Carlo analysis and the recently developed incremental damage model. The method means that more accurate B_{10} lifetimes can be presented for the three-phase and dual inverter systems that incorporates multiple failure states.

Finally, the multi-objective optimisation method from Chapter 4 is used with a PLECS simulation of the dual inverter six-phase system to investigate the effect of switching frequency, DC-link capacitance, and MOSFET number. Several feasible designs are identified to optimise for IMD volume and lifetime, with direct comparisons made between the multi-phase and three-phase system. The dual inverter was found to outperform the three-phase inverter with smaller required DC-link capacitance, higher efficiency and increased lifetime in part due to its fault-tolerant nature. The optimal dual inverter chosen in this chapter, considering the design constraints and other considerations regarding specified user preferences towards volume and lifetime, consists of four 40 μF KEMET film capacitors operating with

a switching frequency of 46 kHz giving an inverter volume of 300 cm^3 and a lifetime of 16.3 years.

Chapter 6

Conclusions

This thesis has investigated the use of SiC discrete MOSFETs in the design optimisation of highly reliable integrated motor drives (IMDs) and identified optimal inverter systems for an automotive application. The research question in this thesis was presented in the introduction as: "How can an integrated motor drive be designed for an application so that it is optimal?". Each chapter has therefore focused on developing methodologies to improve the accuracy of IMD system modelling or improve IMD performance.

Integrated motor drives (IMDs) have been identified as a promising technology with the potential to improve performance of electric vehicles (EVs). However, there are many design issues to solve to design a effective, reliable and compact IMD. As such, the use of SiC discrete MOSFETs has been recognised as an enabling technology and new design methodologies and analysis have been identified as important areas of research to determine accurately optimal IMD designs.

While SiC MOSFET performance has been thoroughly examined, there's potential for improvement and optimisation in the way devices are selected in inverters. A review of the relevant literature concluded that IMD optimisation has not been widely investigated with many of the optimisation procedures using analytical studies and calculations without considering a holistic approach to the inverter design. The IMD optimisations in literature also failed to consider reliability, with lifetime modelling specific to discrete MOSFETs only recently being investigated. In response, a system-level model using experimentally

validated SiC MOSFET models was proposed which allows real-time electrothermal analysis, optimisation, and lifetime prediction.

The work in this thesis emphasised several novel methods for optimisation and analysis of high reliability IMDs to answer the research question, these are important considerations for future IMD design:

- A tool was developed for optimising device selection capable of being used in high current systems that require paralleling of multiple discrete SiC MOSFETs.
- The proposed device selection tool uses the interdependent nature of internal parameters of SiC MOSFETs to compare devices from a number of manufacturers.
- PLECS electrothermal analysis and LTSpice transient modelling were combined using MATLAB Simulink to obtain an effective, full system model of an IMD to investigate the system-level performance.
- An optimisation procedure to increase volumetric power density is presented and compared to analytical methods of individual component sizing and design.
- MOSFET lifetime was calculated using a recently developed lifetime model specific to transistors in a TO-247 package within an optimisation for the first time.
- Use of these methods identified a single optimal solution for the system, using a DC-link capacitance of 190 μF at 45 kHz, giving a volume of 440 cm^3 and a lifetime of 12,000 hours.
- A novel method for lifetime prediction of systems with paralleled MOSFETs or fault tolerance capabilities is developed based on TO-247 lifetime calculations, component-level reliability profiles using Monte Carlo analysis and the recently developed incremental damage model.
- The PLECS simulation is used alongside a CFD thermal model to develop a multi-objective optimisation method for finding the optimal IMD under specified conditions for a range of topologies, including multi-phase inverters.

The entire process, from device selection to detailed thermal analysis and optimisation is repeatable under different environmental conditions, inverter inputs, outputs and topologies. Furthermore, the multi-objective methodology identifies a series of solutions that can be chosen depending on the specific aims and priorities of the design project. The optimal dual inverter chosen consists of four 40 μF KEMET film capacitors operating with a switching frequency of 46 kHz giving an inverter volume of 300 cm^3 and a lifetime of 16.3 years.

6.1 Future Work

This thesis focused on the design processes involved in optimising integrated motor drive for automotive applications. System-level simulations are presented employing SiC MOSFET models validated experimentally to analyse electrothermal performance. Values for the volumetric power density are provided however these are an estimation and more useful for comparing designs. An experimental prototype of the optimal design would be required to validate the true performance and characteristics of IMD designs from this thesis, although lifetime is more difficult to validate, hence its importance in this work.

The optimal three-phase and dual inverter designs are customised for the axial flux PMSMs and the corresponding power and torque of the operating conditions presented in this thesis. It is, therefore, challenging to employ standardised motor and converter components. This higher level of integration increases manufacturing costs. The next generation IMD, known as the integrated Modular Motor Drive (IMMD) is made up of several modular components. Each modular unit comprises a single motor stator pole, the matching converter, and the controller. The modular architecture reduces manufacturing and design costs by facilitating manufacture and assembly and enabling a more comprehensive supply chain.

In this work the benefits of the dual inverter are demonstrated, and despite modularity of the inverter this would not be considered an IMMD. An interesting next step for the research could be to investigate further the capability of axial flux PMSMs to increase power by combining multiple machines on a single axis. This presents an interesting modular design problem for IMDs that would benefit from optimisation.

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