

THE DEVELOPMENT OF A FULLY BALANCED CURRENT-TUNABLE ACTIVE-RC ALL-PASS FILTER

Samran Lertkonsarn
Faculty of Engineering¹

Chadarat Khwunnak
Faculty of Science¹

Sittisak Roungrid ✉
Faculty of Engineering and Industrial Technology
Kalasin University
Kasetsomboon Road, Muang District Kalasin, Thailand, 46000
sittisak.ro@ksu.ac.th

¹*Pitchayabundit College*
Muang District Nong Bua Lamphu, Thailand, 39000

✉ **Corresponding author**

Abstract

This research paper presents a symmetrical current-tunable active-RC all-pass filter that uses an active BJT coupled with R and C . The circuit's symmetrical structure ensures that the differential signals are treated equally, resulting in improved performance. Furthermore, the filter's ability to adjust the frequency by bias current makes it suitable for a wide range of applications, such as improving phase properties and creating other types of filters. The simulation results obtained through the Pspice program show that the value of the operating frequency can be adjusted by bias current, which is the highlight of this research. The transfer function of the circuit shows a response of about 0 dB and -90° respectively, indicating that the circuit can change the phase of the input signal without changing its magnitude. This feature is particularly useful in signal processing applications where phase changes are required. In addition, the paper discusses how the operating frequency can be increased by decreasing the capacitor. The transfer function of the circuit analyzed shows that the operating frequency (f_0) is inversely proportional to the product of the capacitors. Therefore, decreasing the value of C increases the operating frequency of the circuit. Monte Carlo analysis results are also presented for resistors, capacitors, and transistors with error values. This analysis helps determine the effect of errors on the output signal of the circuit. The results show that the output signal is sensitive to changes in the resistor values, which can affect the accuracy of the filter. Therefore, it is important to select high-quality resistors to ensure that the filter operates accurately.

Keywords: Fully-balanced, Phase-lag, all-pass filter, current-tunable, active-RC filter, Monte Carlo analysis.

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1. Introduction

Filters are crucial components in electronic systems that are used to selectively amplify or attenuate certain frequencies from the input signal [1]. They play a key role in applications such as audio processing, telecommunications, and sensor systems [2, 3]. The functionality of filters is determined by their frequency response characteristics, which include low-pass, high-pass, band-pass, and band-stop filters [4, 5]. Low-pass filters allow frequencies below a cutoff frequency to pass through, while high-pass filters allow frequencies above the cutoff frequency to pass through. Band-pass filters permit a range of frequencies to pass through, while band-stop filters attenuate a specific range of frequencies. These types of filters are widely used in audio processing, RF communication, and signal conditioning applications [6].

In recent years, the all-pass filter, also known as the phase shift circuit, has gained significant attention in the field. This circuit has been extensively studied and documented in international journals over the past decade, with notable contributions from various researchers [7–10]. Additionally, specific work by [11–13] has focused on designing an all-pass filter tailored for configuring the frequency of a sinusoidal quadrature circuit. Researchers have explored a wide range of configurations for all-pass filter structures, including those incorporating active components, which offer distinct advantages

over passive device synthesizer circuits. These active filters are renowned for their higher precision, compact size, and energy efficiency, making them versatile for a variety of applications [14, 15]. Furthermore, [16–18] have proposed an all-pass filter utilizing an operational amplifier (Op-Amp) as its active component. It is worth noting that Op-Amp-based filters may pose challenges when adapting to different electronic applications. In contrast, active filters operating in current mode offer the advantage of higher frequency capabilities compared to voltage mode filters. This is because current mode circuits have fewer internal nodes and exhibit enhanced accuracy when handling current signals [19–21].

Recent advancements in all-pass filter design have included the utilization of a current-mode bipolar junction transistor (BJT) as an active component [22]. This innovative circuit has demonstrated remarkable effectiveness in the design of intricate filter systems, offering the essential flexibility required for precise control of both frequency and phase shift, particularly in the context of high-frequency signal processing. An integrator circuit, incorporating an active BJT component in conjunction with a capacitor (C), has been introduced to the circuitry [23]. The circuit's inherent balance and versatility make it suitable for a wide array of applications. Additionally, meticulous attention has been paid to the design of a bandpass filter, featuring a BJT as the active component, in tandem with a capacitor (C) [24]. A standout feature of this circuit design is its adjustable center frequency (f_0), which can be finely tuned across three discrete levels via bias control. This adaptability renders the designed circuits particularly noteworthy, as they possess the potential to address a diverse spectrum of applications. It is worth noting that the quality factor (Q) of these circuits is impressively high, standing at 267, thus underscoring their substantial advantages.

Following a discussion of various circuit designs, this study focuses on a comprehensive investigation, analysis, synthesis, and simulation of an all-pass filter utilizing an active BJT in conjunction with resistors (R) and capacitors (C). The circuit exhibits complete symmetry and facilitates frequency adjustment via bias current control. This property extends its versatility for diverse applications, including phase enhancement and integration with adder and buffer circuits to create various filter configurations.

2. Materials and methods

2.1. Circuit description

Fig. 1 shows a fully balanced current-tunable active-RC all-pass filter with a symmetrical structure, whose frequency can be adjusted by biasing the current.

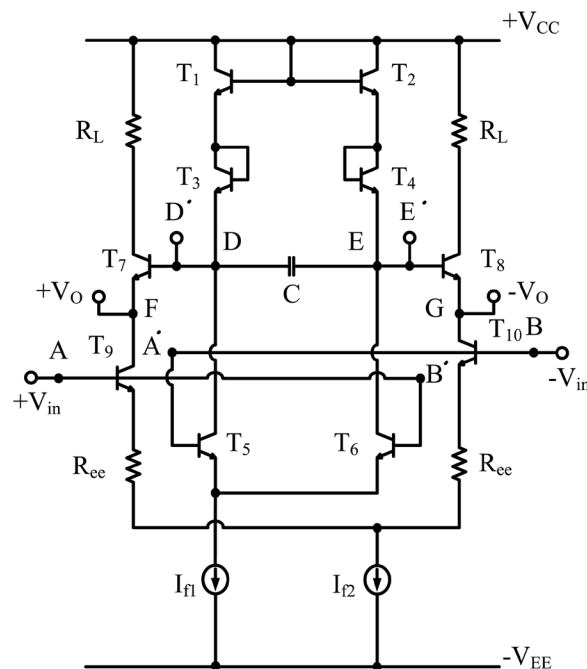


Fig. 1. A fully-balanced current tunable active-RC all-pass filter

The circuit comprises ten identical NPN junction transistors (BJTs) (T_1 to T_{10}) connected to one capacitor (C), four resistors ($2R_{ee}$ and $2R_L$ where R_{ee} and R_L have equal value), and two bias currents (I_{f1} and I_{f2}). The small differential signal (V_{in}) is fed to the base pin of transistor pairs T_5 – T_6 (node A and B) and T_9 – T_{10} (node A' and B'), and the output small differential voltage at the output point (V_O) is across the emitter pin of transistors T_7 – T_8 at node F and node G , respectively.

2. 2. Ideal analysis

Firstly, let's consider Fig. 2, *a* where it is assumed that the base legs of the transistors T_7 and T_8 connected to node D' and node E' must be removed as shown. Then, they are connected to the bias voltage (V_{bias}) as shown in Fig. 2, *b* from Fig. 2, *a*, a small differential voltage V_{O1} appears across node D and node E .

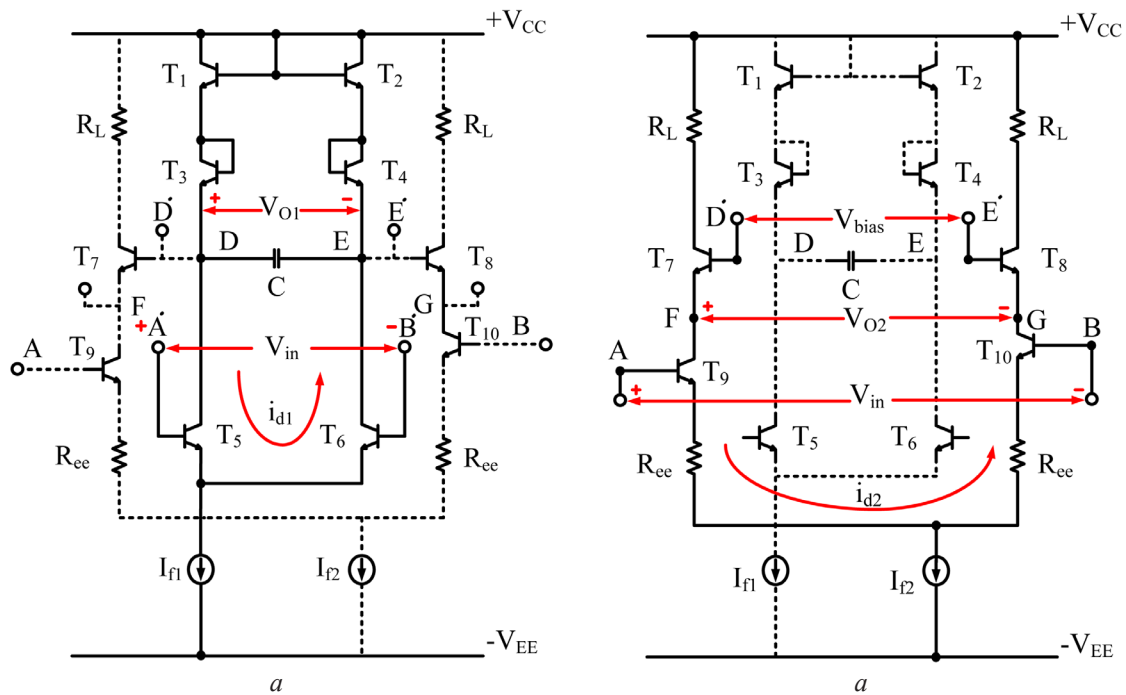


Fig. 2. Proposed circuit realization of ideal analysis:

a – the V_{in} is fed to the base pin of the transistor pair T_5 – T_6 ; *b* – the V_{in} is fed to the base pin of the transistor pair T_9 – T_{10}

A small differential voltage at the input V_{in} (node A' and B') causes a differential current to flow at the output point i_{d1} show as in equation (1):

$$i_{d1} = \frac{V_{in}}{2r_e} \tag{1}$$

From Fig. 2, *a* the current i_{d1} flows through the load resistance Z this is caused by the transistors T_1 – T_4 and the capacitor (C) between node D and node E , herein designated as Z , so as shown in equation (2):

$$Z = 4r_e / \frac{1}{Cs}, \tag{2}$$

or rearrange the equation as:

$$Z = \frac{4r_e}{(1 + s\tau)}; \tau = 4r_e C. \tag{3}$$

and the equation of τ can be written as shown in the equation (4):

$$\tau = 4r_e C = \frac{4V_T C}{I_f}. \quad (4)$$

V_T is the thermal voltage of the $p-n$ junction of a semiconductor, typically 25 mV at room temperature. Therefore, the pressure value $V_{O1} = i_{d1}Z$, the transfer function is obtained in the form of a low-pass filter as shown in equation (6):

$$V_{O1} = i_{d1}Z = \left[\frac{4r_e}{(1+s\tau)} \right] \left[\frac{V_{in}}{2r_e} \right], \quad (5)$$

or rearrange the equation as:

$$\frac{V_{O1}}{V_{in}} = \frac{2}{(1+s\tau)}. \quad (6)$$

In the second case, consider **Fig. 2, b** the input point voltage V_{in} (node A and node B) induces a differential current at the output point i_{d2} which it is possible to calculate from equation (7):

$$i_{d2} = \frac{V_{in}}{2r_e + 2R_{ee}} = \frac{V_{in}}{2(r_e + R_{ee})}. \quad (7)$$

The current i_{d2} will flow through a load resistor of value $2(r_e + R_L)$ made up of transistors T_5 , T_6 and the resistor R_L between node F and node G , voltage will be obtained at the output point $V_{O2} = i_{d2}2(r_e + R_L)$ and the transfer function is obtained in the form of a buffer as shown in equation (8):

$$V_{O2} = i_{d2}2(r_e + R_L). \quad (8)$$

Substitute the value of i_{d2} from equation (7) into equation (9). Here, R_{ee} and R_L are equal:

$$V_{O2} = \left(\frac{V_{in}}{2(r_e + R_{ee})} \right) (2(r_e + R_L)). \quad (9)$$

Rearrange the equation to get:

$$\frac{V_{O2}}{V_{in}} = 1. \quad (10)$$

By returning the base legs of transistors T_5 and T_6 to node D and node E as shown in **Fig. 2**, a small differential output voltage V_O across node G and node F is obtained by applying theory superposition is $V_O = V_{O1} - V_{O2}$ and will get the V_O/V_{in} transfer function is:

$$\frac{V_O}{V_{in}} = \frac{(1-s\tau)}{(1+s\tau)}. \quad (11)$$

Equation (11) shows the transfer function of phase-lag all-pass filter. The corner frequency form of this filter has the following form (12):

$$\omega_0 = \frac{1}{\tau} = \frac{I_f}{4V_T C}. \quad (12)$$

Equation (13) shows that the phase response is shifted from 0° to -180° .

$$\theta = -2 \tan^{-1}(\omega_0 4r_e C). \quad (13)$$

3. Results and discussion

Refer to **Fig. 1**, which shows a fully balanced current-tunable active-RC all-pass filter simulated using Pspice [25]. The circuit elements were synthesized using an NPN bipolar junction transistor (BJT) of the type Q2N2222A, with an f_T of 300 MHz [26]. R_{ee} and R_L are resistances, and **Fig. 3**, shows the kinetic response. The V_O/V_{in} frequency was measured at room temperature, with R_{ee} and R_L set at $50\ \Omega$ and the capacitor (C) set at $0.1\ \mu\text{F}$. I_{f1} was set to $150\ \mu\text{A}$, $300\ \mu\text{A}$, $500\ \mu\text{A}$, $1\ \text{mA}$ and $2\ \text{mA}$ respectively while I_{f2} was set at $100\ \mu\text{A}$. From **Fig. 3**, it can be seen that the phase shift is -90 degrees. The filter operates at $\omega_0/2\pi$ which are $1.24\ \text{kHz}$, $2.489\ \text{kHz}$, $4.151\ \text{kHz}$, $8.300\ \text{kHz}$ and $16.571\ \text{kHz}$ respectively with the corresponding magnitude of approximately $0\ \text{dB}$.

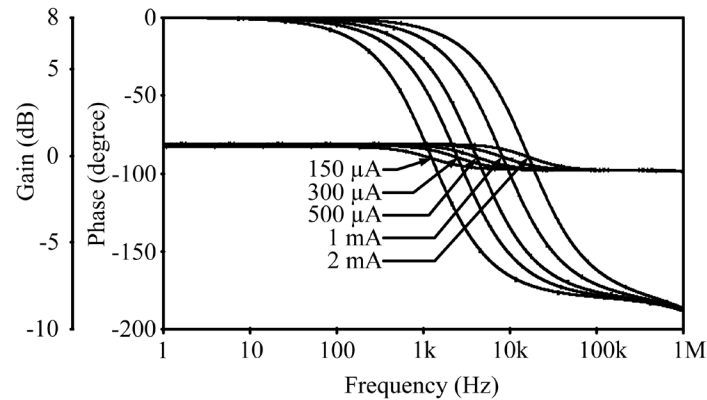


Fig. 3. Gain (dB) and phase shift (degree) of V_O/V_{in} versus frequency (Hz) using the $C = 0.01\ \mu\text{F}$, R_{ee} and $R_L = 50\ \Omega$, $I_{f1} = 150\ \mu\text{A}$, $300\ \mu\text{A}$, $500\ \mu\text{A}$, $1\ \text{mA}$, $2\ \text{mA}$ and $I_{f2} = 100\ \mu\text{A}$

Fig. 4, shows the simulation results of the signal response by setting the current values of I_{f1} and I_{f2} to $100\ \mu\text{A}$, using the resistors R_L and R_{ee} at $50\ \Omega$ with zero percent error in the capacitor section, and setting the gain of the transistor (β) to 0 percent. The transient response at the pole frequency value is shown in **Fig. 4**, which indicates a 180° phase shift between the input and output voltages.

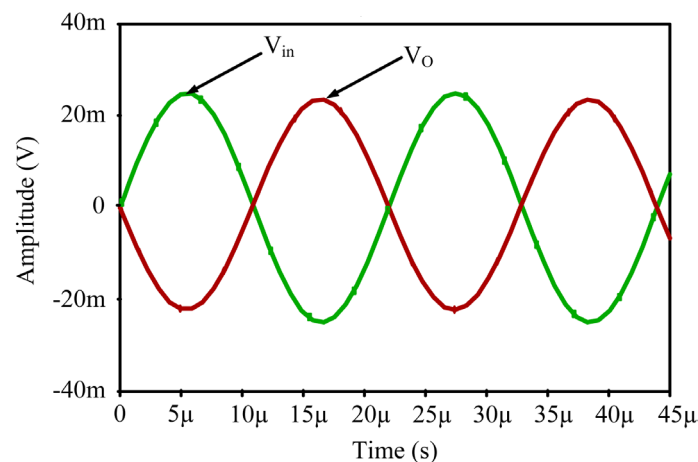


Fig. 4. Filter response to a $45.5\ \text{kHz}$ sinusoidal input signal, using the $C = 0.1\ \mu\text{F}$, R_{ee} and $R_L = 50\ \Omega$, $I_{f1} = 100\ \mu\text{A}$ and $I_{f2} = 100\ \mu\text{A}$

Fig. 5, a, illustrates the use of the Monte Carlo (MC) method for error checking of a resistor device (R_L and R_{ee}) shown in **Fig. 1**. The I_{f1} bias current is $100\ \mu\text{A}$, and the I_{f2} bias current is $100\ \mu\text{A}$. A Monte Carlo simulation was performed on 100 samples with the resistor error set at 10 percent. **Fig. 5, a**, shows the Monte Carlo analysis of the magnitude response, while **Fig. 5, b**, shows the histograms of the magnitude response. The magnitude response in **Fig. 5, b**, has a mean magnitude

response of 0.453 dB, a median value of 0.454, and a standard deviation of 0.028. **Fig. 5, c**, shows the Monte Carlo analysis of the phase response, and **Fig. 5, d**, shows the histograms of the phase response. The phase response in **Fig. 5, d**, has a mean phase response of -0.139 degrees, a median value of -0.139 , and a standard deviation of 0.000429.

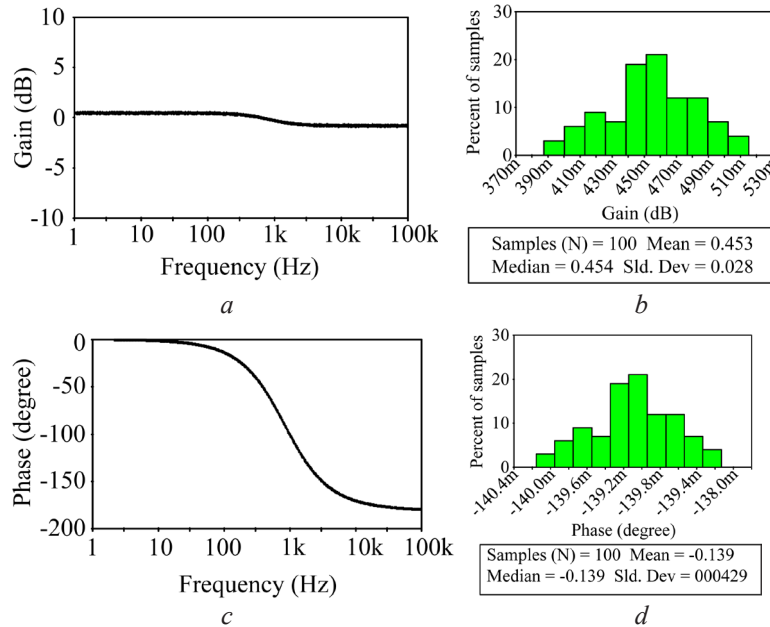


Fig. 5. The Monte Carlo analysis of the magnitude and phase response of the proposed circuit, with the error of the resistor is set to 10 percent in the capacitor section and the gain of the transistor (β) is set to 0 percent: *a* – Monte Carlo analysis of magnitude response; *b* – histograms of the magnitude response; *c* – Monte Carlo analysis of phase response; *d* – histograms of the phase response

Fig. 6, a, illustrates the use of the Monte Carlo (MC) method for error checking of a capacitor device (C) shown in **Fig. 1**. The I_{f1} bias current is $100 \mu\text{A}$, and the I_{f2} bias current is $100 \mu\text{A}$. A Monte Carlo simulation was performed on 100 samples with the capacitor error set at 10 percent. **Fig. 6, a**, shows the Monte Carlo analysis of the magnitude response, while **Fig. 6, b**, shows the histograms of the magnitude response. The magnitude response in **Fig. 6, b**, has a mean magnitude response of 0.451 dB, a median value of 0.451, and a standard deviation of 6.246×10^{-7} . **Fig. 6, c**, shows the Monte Carlo analysis of the phase response, and **Fig. 6, d**, shows the histograms of the phase response. The phase response in **Fig. 6, d**, has a mean phase response of 75.583 degrees, a median value of -0.029 , and a standard deviation of 87.583.

Fig. 7, a, illustrates the use of the Monte Carlo (MC) method for error checking of the gain of transistors (T_1 to T_{10}): β shown in **Fig. 1**. The I_{f1} bias current is $100 \mu\text{A}$, and the I_{f2} bias current is $100 \mu\text{A}$. A Monte Carlo simulation was performed on 100 samples with the error of the gain of the transistor (β) set at 50 percent. **Fig. 7, a**, shows the Monte Carlo analysis of the magnitude response, while **Fig. 7, b**, shows the histograms of the magnitude response. The magnitude response in **Fig. 7, b**, has a mean magnitude response of 0.444 dB, a median value of 0.448, and a standard deviation of 0.0244. **Fig. 7, c**, shows the Monte Carlo analysis of the phase response, and **Fig. 7, d**, shows the histograms of the phase response. The phase response in **Fig. 7, d**, has a mean phase response of -0.139 degrees, a median value of -0.139 , and a standard deviation of 0.00015.

Fig. 8, displays the voltage output (V) levels of the fundamental frequency and subsequent harmonics of the V_{out} oscillogram, obtained using a commercially available fast Fourier transform (FFT) program. It is evident from **Fig. 8**, that the magnitudes remain constant throughout the entire operational bias-current range, with $I_{f1} = 100 \mu\text{A}$ and $I_{f2} = 100 \mu\text{A}$, and the error values of

the resistor, capacitor, and transistor set to 0 percent. The total harmonic distortions (THD) of the output waveforms, as depicted in Fig. 8, are measured to be below 9.206 percent.

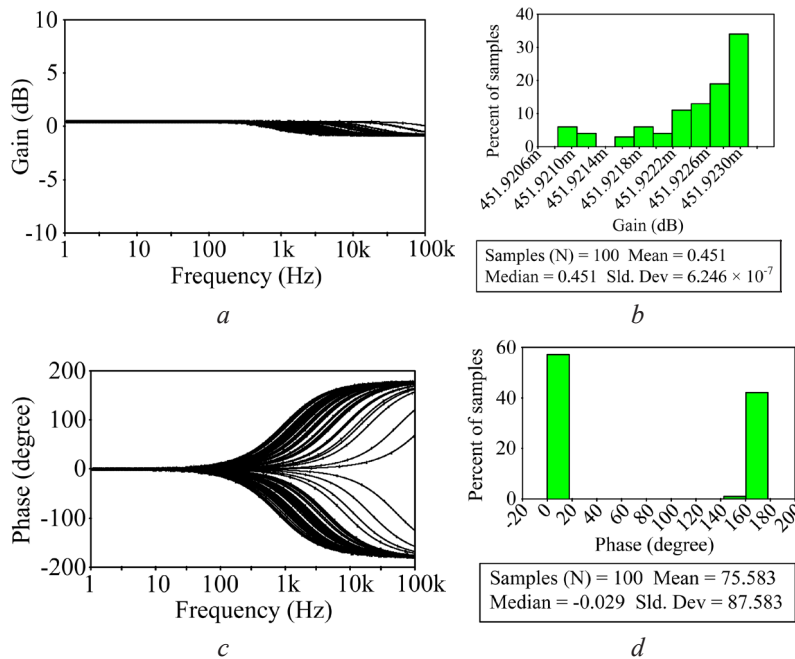


Fig. 6. The Monte Carlo analysis of the magnitude and phase response of the proposed circuit, with the error of the capacitor is set to 10 percent in the resistor section and the gain of the transistor (β) is set to 0 percent: *a* – Monte Carlo analysis of magnitude response; *b* – histograms of the magnitude response; *c* – Monte Carlo analysis of phase response; *d* – histograms of the phase response

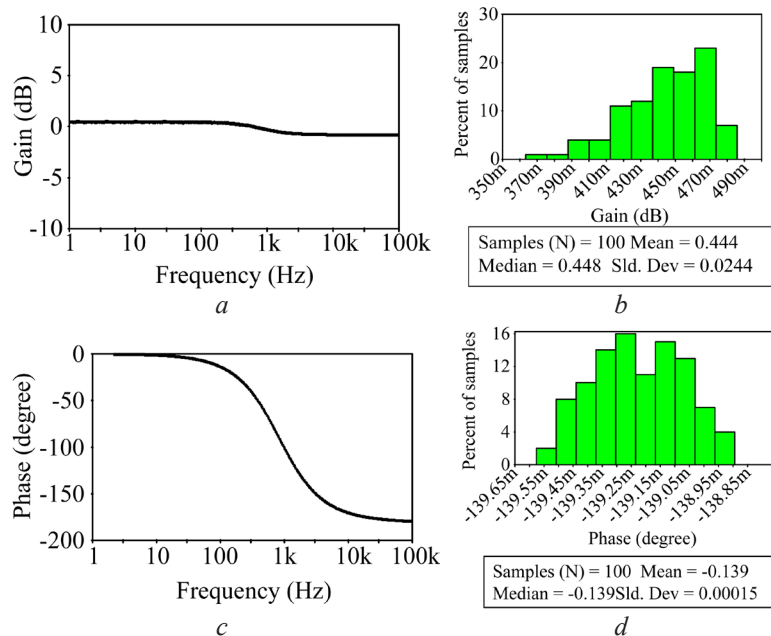


Fig. 7. The Monte Carlo analysis of the magnitude and phase response of the proposed circuit, with the error of the gain of the transistor (β) set at 50 percent in the resistor and capacitor is set to 0 percent: *a* – Monte Carlo analysis of magnitude response; *b* – histograms of the magnitude response; *c* – Monte Carlo analysis of phase response; *d* – histograms of the phase response

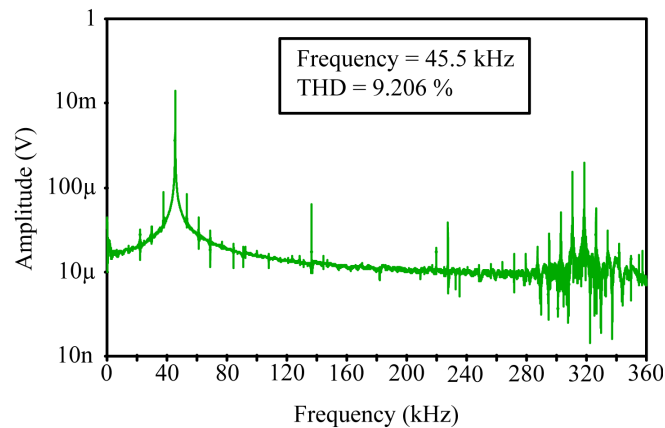


Fig. 8. The harmonic spectra of the output (V_{out}) waveform when using $C = 0.1 \mu\text{F}$, R_{ee} , and $R_L = 50 \Omega$

However, there are limitations to this study:

- while the Monte Carlo analysis provides valuable insights into the circuit's performance under component variations, it's essential to acknowledge that real-world component tolerances may extend beyond the simulated ranges. Therefore, practical reproducibility should be carefully considered when implementing the circuit;

- the presented study does not address the impact of temperature variations or environmental conditions on the circuit's performance. In real-world applications, these factors can significantly influence circuit behavior and should be investigated in further research or practical implementations;

Suggestions for further development of this research include:

- validating the circuit's performance through physical prototyping and testing under various operating conditions to assess its practical applicability;

- expanding the study by conducting a comprehensive noise analysis to evaluate the circuit's sensitivity to external disturbances and explore noise-reduction techniques;

- exploring opportunities to integrate the circuit into larger systems or applications where precise phase control is required, such as audio processing or communication systems.

4. Conclusions

This paper introduces a fully balanced current-tunable active-RC all-pass filter. The designed circuit comprises an active component utilizing a bipolar junction transistor (BJT) connected to a resistor and a capacitor. The capacitor, a passive component, features a straightforward circuit structure symmetrically designed for differential signals. Simulation results generated using the P_{spice} program demonstrate the circuit's response, specifically, the capability to adjust the operating frequency (f_0) of the transfer function by varying the bias current (I_f). This ability serves as the primary focus and highlight of this research. Notably, the transfer function exhibits responses of approximately 0 dB and -90 degrees, respectively. The analysis in section (12) reveals that the operating frequency (f_0) can be increased by reducing the capacitor's value (C). Additionally, Monte Carlo analysis results illustrate the output signal (V_O) generated under the influence of component tolerances, encompassing resistors, capacitors, and transistors with error values. This information holds practical utility for the circuit's development and application in various fields, such as enhancing phase properties or integrating it with an adder and buffer circuit to create various filter types, among other potential applications.

Conflict of interest

The authors declare that they have no conflict of interest in relation to this research, whether financial, personal, authorship or otherwise, that could affect the research and its results presented in this paper.

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The study was performed without financial support.

Data availability

Manuscript has no associated data.

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