Measurement 221 (2023) 113512

Contents lists available at ScienceDirect

Measurement

journal homepage: www.elsevier.com/locate/measurement

A simple interface circuit for digital readout of lossy capacitive sensors

José A. Hidalgo-López

Departamento de Electrónica, Universidad de Málaga, Andalucía Tech, Campus de Teatinos, Málaga 29071, Spain

ARTICLE INFO

Keywords:
Lossy capacitive sensor
Sensor interface electronics
Time-based measurement
Direct interface circuits

ABSTRACT

Direct Interface Circuits (DICs) allow straightforward digital reading from a range of sensors. Their architecture consists of a few passive components that help a digital processor (DP) perform a series of charge and discharge processes that provide time measurements to determine the sensor's resistive, capacitive, or inductive magnitudes. This article presents a new DIC that only requires two resistors for the digital readout of a group of sensors with a wide range of applications, namely lossy capacitive sensors. The DP does not need any analog element in its architecture, and the arithmetic operations involved are simple additions and multiplications. Apart from its simplicity, the new circuit brings significant improvements compared to other DICs proposed in the literature for the same type of sensors. Thus, the systematic errors in the capacitance estimates are only 0.30% for a wider range (100 pF − 95.92 nF), and the measurement time is 34% shorter.

1. Introduction

Smart sensors are integrated platforms fitted with physical sensors to monitor the variables of interest, along with a digital processor (DP) that works on this information. Microprocessors, FPGAs, or ASICs are generally used as DPs. Several sensors are typically connected to a single DP that processes their information. Each sensor will need an interface circuit to transform the analog information from the sensor into the digital format used by the DPs. Interface circuits are, therefore, critical elements in the design of smart sensors and must meet the requirements of these devices, i.e., simplicity, low cost, and low energy consumption (due to the increasing number of portable and remote applications).

Capacitive sensors are extensively used for measurement in a wide range of physical and chemical processes. Several capacitive sensors could be modeled as a simple capacitor, C_x, while others need a resistor, R_x, in parallel as a shunt. The latter, known as lossy capacitive sensors, can be used to measure humidity [1–3], as flow measurement sensors [4], to measure the quality of edible oils [5], as gas sensors for atmospheric pollutant monitoring [6,7], to check fruit quality [8], as tactile and proximity sensors [9,10], to identify ice on road surfaces [11], etc.

A classic approach to the digital readout of a lossy capacitive sensor consists of a signal conditioning circuit that transforms the information in the C_x capacitor into a voltage that will be translated into a digital value using an analog-to-digital converter (ADC) [12–15]. These designs generally require a sinusoidal voltage source, a variable number of operational amplifiers (OAs), and multiple switches and passive components. Therefore, these circuits are unattractive options in terms of hardware requirements and power consumption.

Other designs bypass ADCs by performing a capacitance-to-time-to-digital conversion through phase-sensitive circuits. For example, in [16], an active bridge circuit is used, followed by phase-sensitive detection (PSD) circuit. A PSD block is also necessary in [5], but several peak detectors precede it in this case. In [3], different outputs of a modified dual-slope circuit control a PSD module. In a more complex design [17], an auto-tuning quadrature phase generator with a PSD and a null detector are used together. In [18], a similar design philosophy is maintained with a modified Martin relaxation oscillator instead of the PSD. Although these designs avoid using ADCs, they also comprise multiple OAs, switches, and passive components and again require a sinusoidal voltage source. It is important to note that all these circuits also need a digital block to control the different phases of the conversion process.

Other proposals that perform a capacitance-to-time-to-digital conversion reduce the components needed for the readout of lossy capacitive sensors by including an additional reference voltage source. For example, in [19], the time measurement that provides the value of C_x is obtained using four single-pole double-throw switches (SPDT), an OA, a comparator, and two extra-capacitors, in addition to the reference voltage source and the digital control block. A different proposal [20] needs two SPDTs, two OAs, two additional resistors, and an extra capacitor. Although the reduction in the number of components in this approach is significant, the need for a reference voltage source, active components, and switches limits the applicability of the designs.

In all previous proposals, including design with ADCs, different

E-mail address: jahidalgo@uma.es.

https://doi.org/10.1016/j.measurement.2023.113512
Received 8 May 2023; Received in revised form 19 August 2023; Accepted 30 August 2023
Available online 30 August 2023

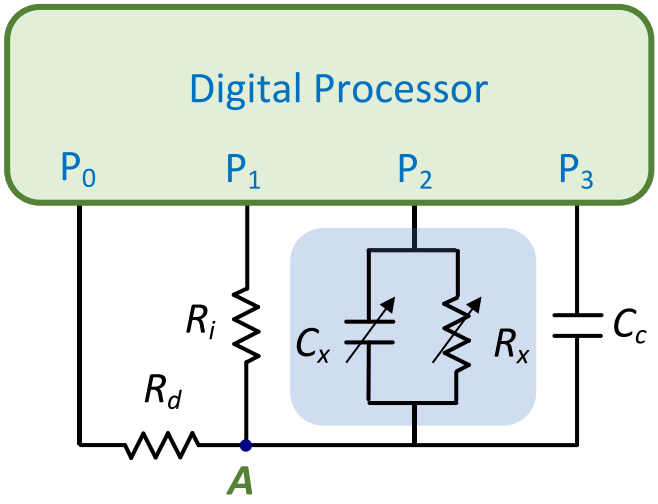


Fig. 1. Direct Interface Circuit for lossy capacitive sensors proposed in [25].

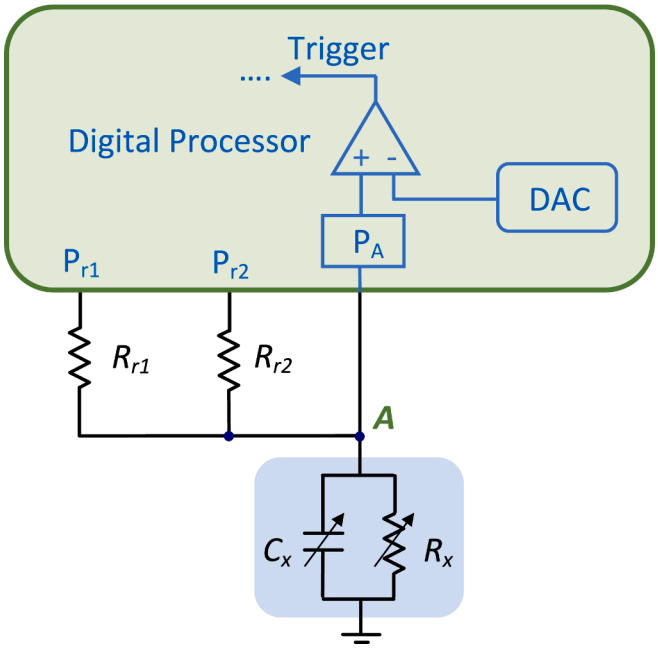


Fig. 2. Alternative Direct Interface Circuit for lossy capacitive sensors proposed in [27].

arithmetic operations are necessary on the digital data initially provided by the circuits to get the final value of C_x. Therefore, although not explicitly discussed, all of these designs require a DP.

A different design approach allows the reading of purely capacitive sensors using just a few passive components and a DP. These are known as Direct Interface Circuits, DICs. Such circuits generally perform several sensor charge and discharge processes. In [21,22], discharge is performed through a different resistor (always of known value) after each charge, then measuring the time used in the discharges to determine the capacitance value. A variant of this technique [23] uses different time measurements in the charge and discharge processes through a single resistor. Recently, [24] has simplified the process by performing all time measurements in a single discharge (in this circuit, only two time measurements are necessary to obtain an estimate of C_x). The functions of the digital control block are performed in all these proposals by a DP without special hardware requirements.

DICs have also been proposed for reading lossy capacitive sensors. These circuits are more complex than those used for reading purely capacitive and resistive sensors due to the very structure of the sensor and to the fact that it is sometimes necessary to provide an estimate not only of C_x but also of R_x (increasing both the hardware used, as well as the charge and discharge processes required to obtain the estimates). Nevertheless, they still use only one DP and a few passive components.

The DIC proposed in [25] is shown in Fig. 1. The circuit needs two resistors and a calibration capacitor, C_c, as passive components (all these components of known value). DP pins must be bidirectional, so they have a low output resistance (say *ro*) when configured as an output, and they must be in a high impedance (HZ) state when configured as an input. When charging, pin P_1 provides a logical 1 output, and the pins of the capacitor (or capacitors) that will be subsequently discharged are configured as logical 0 outputs. P_0 must be set as HZ. The circuit performs four charging-discharging processes to take the four time measurements, which, following a series of algebraic operations, result in the estimates of C_x and R_x. P_0 is set as output '0′ and P_1 as HZ in all discharges. The capacitor to be discharged is selected by setting its corresponding pin as output '0′. If a capacitor is not to be discharged, its pin is selected as HZ. Discharge takes place through C_x, C_c, and $C_x + C_c$. Finally, an additional discharge is carried out through the stray capacitor associated with node A in Fig. 1 (configuring P_2 and P_3 as HZ during this discharge). For all discharges, P_1 detects the trigger instant at which the voltage in node A, V_A, goes from a logical 1 to a logical 0 (with this voltage being called V_{TL}).

By using four time measurements, the designer attempts to improve the accuracy of the estimates. Notwithstanding, the errors are 6% in the estimate of C_x, with C_x in the range 150–206 pF and R_x in the range 1–10 MΩ (errors in the R_x estimate are not provided). Stray capacitors partially cause these errors in pins P_0-P_3. However, the main cause of these errors is that the pin connected to the capacitors and configured as output '0′ must supply current from inside the DP when discharging. This implies that the voltage at the pin's output is negative, causing its protection diode to turn on. In this situation, the pin cannot be considered to work as a small, constant output resistor, *ro*, which negatively affects the accuracy of the estimates. Errors in [25] can be excessive for various applications in which the variation range of C_x is even greater.

Maintaining a similar procedure, in [26], these errors in the estimate of C_x are reduced to 1.5% for the range 100 pF – 2.2 nF (no errors are provided for the R_x estimate either). Nonetheless, this comes at a cost: new bipolar DC sources, two OAs, and several switches and resistors, meaning the design is not a true DIC.

A different DIC is proposed in [27], Fig. 2. This circuit only requires, apart from the DP, two resistors of known value: R_{r1} and R_{r2}. The circuit has several advantages over the one in Fig. 1. Firstly, only two time measurements are needed to obtain the estimates of C_x and R_x. These measurements only require two charge–discharge processes, reducing both power consumption and the total time needed for the estimates, T_M. Operation of the circuit also prevents the protection diodes from being activated. One discharge is through $R_{r1}\|R_x$ and another through $R_{r2}\|R_x$, determining the trigger instants in each of them. The problem with these discharges is that, unlike [25], the designer requires precise knowledge of both the initial voltage stored in the capacitor, V_{Amax}, and the final voltage, V_{TL}. However, the designer is unlikely to know V_{Amax} with great precision, and the exact value of V_{TL} is certainly not known. The latter requires a digital-to-analog converter (DAC) to generate a trigger voltage (known precisely by the designer) and an analog comparator shown in Fig. 2. Although there are DPs with these elements, they are not commonly found, and such elements also increase cost and power consumption. Finally, the calculations to find C_x and R_x are tedious for the DPs and include logarithmic and exponential functions, meaning T_M increases. A complex offline calibration process is also required to compensate for errors. In this process, 20 parameters must be generated and stored in the DP to correct the estimates initially made with the two time measurements. The result is that the C_x estimates have maximum errors of 0.71% in a reduced range 100 – 286 pF, while the R_x estimates

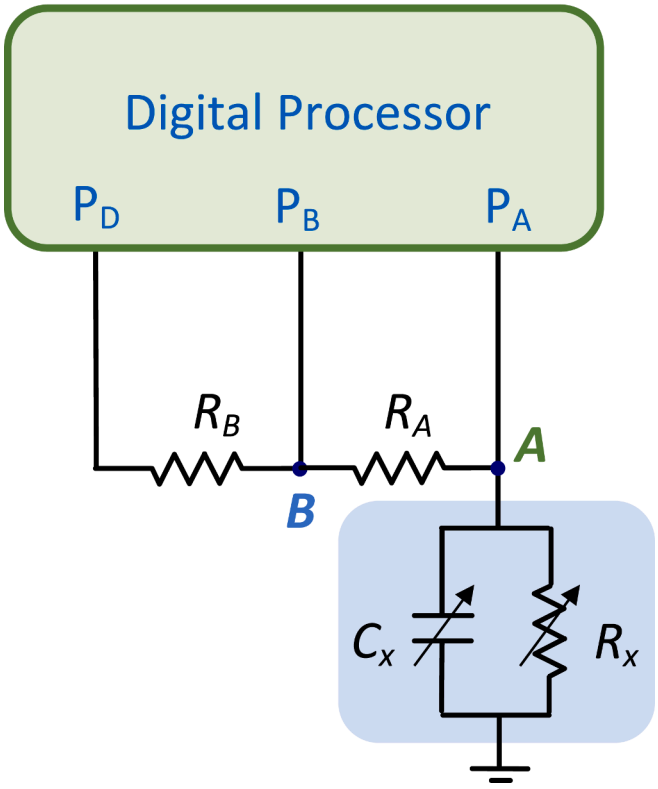


Fig. 3. The new proposed DIC for lossy capacitive sensors.

Table 1
Steps to obtain time measurements in the new DIC.

STEPS	STATE OF PINS		
	P_A	P_B	P_D
1. Charging C_x	'1'	'HZ'	'0'
2. Dischargingthrough $(R_A + R_B) \parallel R_x$	'HZ'	'HZ'	'0'
3. Charging C_x	'1'	'HZ'	'0'
4. Discharging through R_x	'HZ'	'HZ'	'HZ'

show maximum errors of 0.74% in a 1 – 10 MΩ range.

We can therefore conclude that there is no DIC for lossy capacitive sensors that combines a reduced number of charge–discharge processes, simplicity in hardware components and arithmetic operations, acceptable accuracy in estimates, and application to a wide range of C_x values. In this article, we propose a new DIC that has all these characteristics, as discussed below. Furthermore, energy consumption is minimal thanks to the simplicity of the circuit and method.

2. New Direct Interface circuit for lossy capacitive sensors

The proposed DIC is shown in Fig. 3. Apart from the DP and the sensor, the circuit only uses two resistors and requires two charge–discharge processes, as in [27]. However, unlike this proposal, the DP does not need any analog element included in the DP for its operation, thus reducing overall hardware and power consumption. This also increases the number of candidates that can be used as DPs. The steps necessary to estimate C_x and R_x are shown in Table 1, while the waveforms for the voltages of nodes A and B in Fig. 3 (V_A and V_B) can be seen in Fig. 4.

In steps 1 and 3 of Table 1 and Fig. 4, a charging process of C_x is carried out for a time T_{ch} (this time should be enough to stabilize V_A at its maximum value, V_{Amax}). The P_B pin (configured as input) must detect a '1' at the beginning of the discharge process in step 2 for the circuit to work correctly. The final voltage of the charging process in node B, V_{Bmax} in Fig. 4, must therefore verify $V_{Bmax} > V_{TL}$:

$$V_{Bmax} = \frac{R_B}{R_A + R_B} V_{Amax} > V_{TL} \tag{1}$$

R_A and R_B should therefore be selected such that:

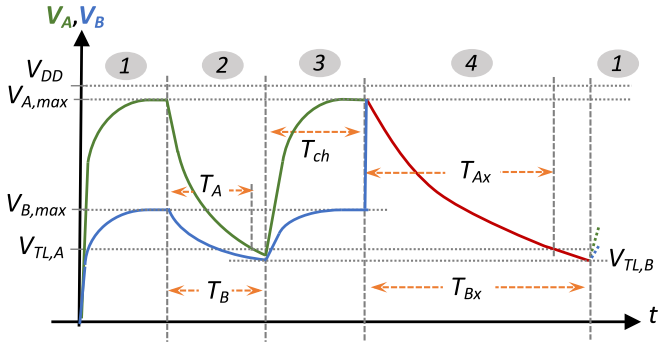


Fig. 5. Voltage waveforms and time measurements in the different steps of Table 1 if $V_{TL,A} \neq V_{TL,B}$.

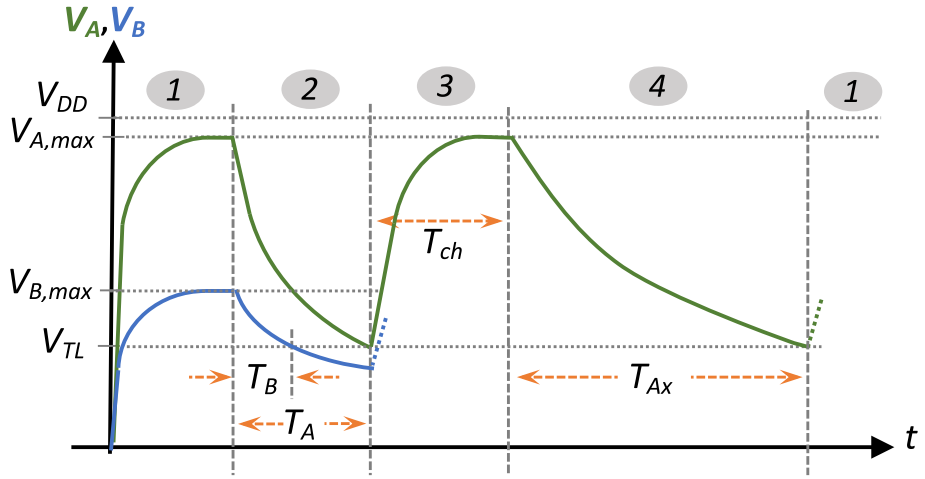


Fig. 4. Voltage waveforms in the different steps of Table 1 for nodes A and B in the circuit in Fig. 3. V_{DD} is the maximum voltage an output pin of the DP can provide.

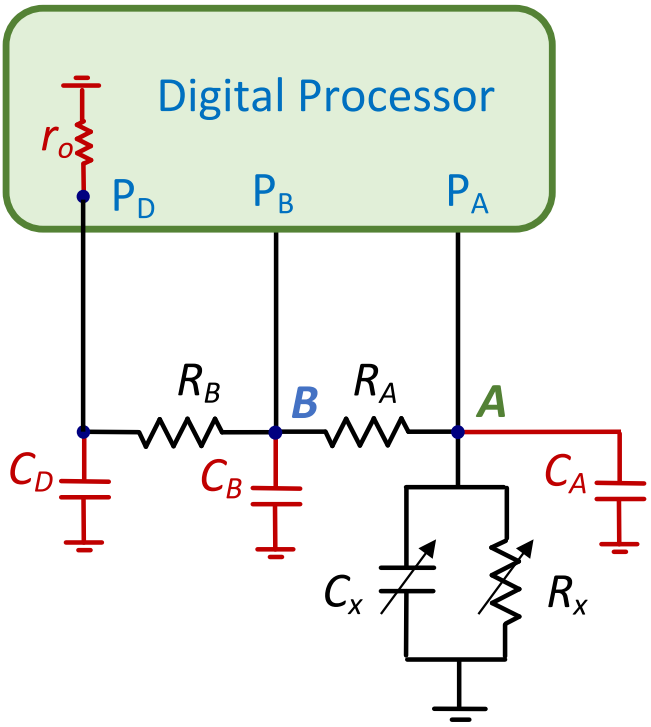


Fig. 6. Parasitic elements (shown in red) in the proposed circuit. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$$\frac{R_B}{R_A + R_B} > \frac{V_{TL}}{V_{Amax}} \tag{2}$$

R_A and R_B can always be chosen such that the term on the left in (2) is greater than the term on the right and there is sufficient safety margin (V_{Amax} and V_{TL} are not precisely known or vary slightly in value during normal circuit operation).

Fig. 4 shows the three time measurements needed to obtain the estimates. In the first discharge, step 2, P_B detects the instant, T_B, at which $V_B = V_{TL}$, while P_A detects the instant, T_A, at which $V_A = V_{TL}$. Once T_A is determined, discharge can end, and a new charge start, step 3. In the second discharge, step 4, the instant at which $V_A = V_{TL}$ is again detected provides the third time measurement, T_{Ax}. From this point on, all steps can be repeated to obtain a new estimate.

Bearing in mind the exponential discharge equation of an RC circuit, the time measurements can be expressed as:

$$T_A = [(R_A + R_B) \| R_x] C_x \ln\left(\frac{V_{Amax}}{V_{TL}}\right) \tag{3}$$

$$T_B = [(R_A + R_B) \| R_x] C_x \ln\left(\frac{R_B}{R_A + R_B}\frac{V_{Amax}}{V_{TL}}\right) \tag{4}$$

$$T_{Ax} = R_x C_x \ln\left(\frac{V_{Amax}}{V_{TL}}\right) \tag{5}$$

Dividing the right and left members of (3) and (5) gives:

$$\frac{T_{Ax}}{T_A} = 1 + \frac{R_x}{R_A + R_B} \tag{6}$$

Finally, if $R_A + R_B$ is stored in the DP, R_x can be determined by

$$R_x = (R_A + R_B)\left(\frac{T_{Ax}}{T_A} - 1\right) \tag{7}$$

On the other hand, subtracting (3) and (4) gives the following result

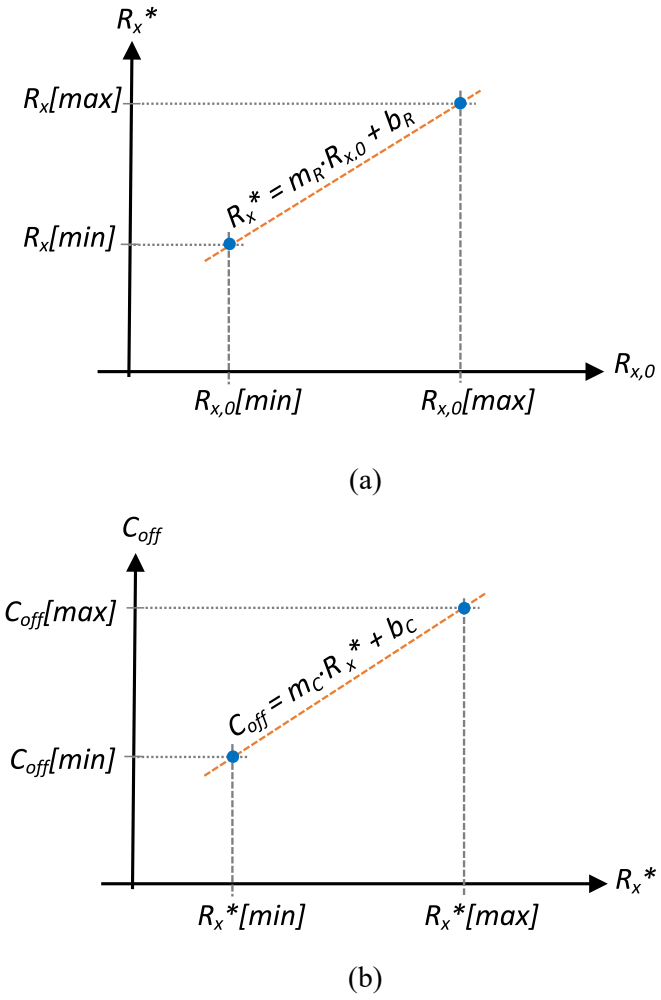


Fig. 7. Calibration points (in blue) and their associated calibration lines (in orange) to obtain parameters m_R, b_R, m_C and b_C. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

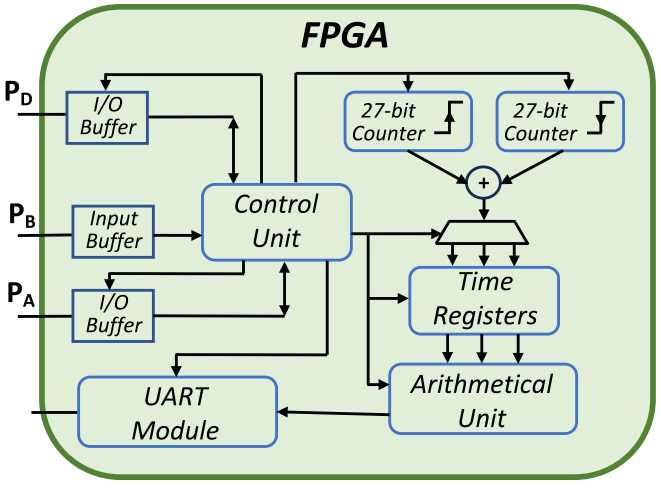


Fig. 8. Block diagram implemented in the FPGA.

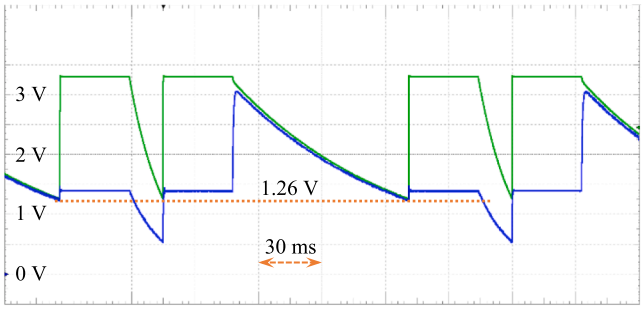


Fig. 9. Observed experimental waveforms for the circuit in Fig. 3. V_A is in green, and V_B is in blue. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$$T_A - T_B = [(R_A + R_B)\|R_x]C_x \ln\left(\frac{R_A + R_B}{R_B}\right) \tag{8}$$

and substituting R_x for its value in (7) will give us C_x:

$$C_x = \frac{T_A - T_B}{(R_A + R_B)\ln\left(\frac{R_A+R_B}{R_B}\right)\left(1 - \frac{T_A}{T_{Ax}}\right)} \tag{9}$$

Since R_A and R_B are known, a constant, k, can be stored in the DP:

$$k = \frac{1}{(R_A + R_B)\ln\left(\frac{R_A+R_B}{R_B}\right)} \tag{10}$$

such that finally:

$$C_x = k \cdot T_{Ax} \cdot \frac{T_A - T_B}{T_{Ax} - T_A} \tag{11}$$

Equations (7) and (11), together with the steps outlined in Table 1, form the basis of the method for estimating R_x and C_x. The method requires three time measurements and the storage of two constants in the DP.

A. Modification of the method for different V_{TL} values in the pins

For most DPs, the values of V_{TL} are very similar in pins with the same characteristics, with differences being in the order of a millivolt or less. Consequently, systematic errors in the estimates of C_x due to these differences can be neglected. Furthermore, it is certain that the estimate of R_x is not affected by these differences since (7) only involves time measurements taken in the same pin. However, the situation may change if the transistors in the input buffers associated with the pins have a small area [28], as may occur in some ASICs. In this case, (11) must be modified to take into account different threshold voltages, $V_{TL,A}$ and $V_{TL,B}$, in pins P_A and P_B, respectively.

The new estimate of C_x uses the same steps as shown in Table 1, but with a fourth measurement, T_{Bx}, being taken in the trigger instant in P_B during the second discharge, step 4. The new situation is shown in Fig. 5, where the V_A and V_B waveforms appear, together with the four measurements to take if $V_{TL,A} \neq V_{TL,B}$. It is important to note that in this figure, at the beginning of step 4 V_B rapidly increases until it reaches the same value as V_A (due to the HZ state of the three pins). From there, V_A and V_B appear superimposed in Fig. 5 (both are shown in red) until $V_B = V_{TL,B}$.

Four equations are used to determine C_x. The first three come from replacing V_{TL} with $V_{TL,A}$ in (3) and (5), and V_{TL} with $V_{TL,B}$ in (4). The fourth, corresponding to T_{Bx}, is given by:

$$T_{Bx} = R_x C_x \ln\left(\frac{V_{Amax}}{V_{TL,B}}\right) \tag{12}$$

Equation (12) has been determined by considering that no current flows through R_A and R_B, meaning $V_A = V_B$ during the second discharge. Following some simple algebraic operations, these new equations provide the new estimate of C_x:

$$C_x = k \cdot \frac{T_{Bx} \cdot T_A - T_{Ax} \cdot T_B}{T_{Ax} - T_A} \tag{13}$$

Compensating for any differences in V_{TL} comes at the expense of an additional measurement, without increasing the number of discharges, and an additional multiplication in the estimate equation of C_x.

B. Considering the parasitic elements

To obtain accurate estimates of C_x and R_x, the method must consider the parasitic elements appearing in the circuit, especially if the C_x values are small. These elements are shown in Fig. 6. The influence on the estimates of the output resistance of the P_D pin, *ro*, will be minimal whenever the designer chooses $R_A + R_B \gg ro$. Typical values of *ro* are in the range 10–20 Ω, meaning that values of R_A and R_B of a few tens of kilohms may be enough to disregard errors due to *ro*.

Meanwhile, Fig. 6 shows the stray capacitors associated with nodes A, B, and the one corresponding to pin P_D. If C_x is large enough and the circuit is designed with care to ensure the stray capacitors are as small as possible, the influence of these capacitors on the three time measurements could also be negligible. However, there are several lossy capacitive sensors in which C_x is in the range of one hundred picofarads (which is only one order of magnitude larger than the capacitance that can appear in a printed circuit board, PCB, for the schematic in Fig. 6). In this case, the errors introduced by stray capacitors cannot be ignored.

These errors create significant difficulty since circuit analysis generates higher-order differential equations. An attempt is made in [25] to compensate for these errors by introducing an additional time measurement in which only the stray capacitor associated with node A of the circuit in Fig. 1 is discharged. The drawback of this online approach is that, as shown in the results, errors remain high, and both T_M and power consumption increase due to the additional charge processes.

In contrast, the calibration in [27] involves a complex offline process that generates 20 parameters (stored in the DP) that help transform the time measurements into more accurate C_x and R_x estimates. However, even with these 20 parameters, errors are only small if the range of C_x is also small ([27] estimates in the range 100–286 pF).

The new DIC proposes a simpler offline calibration. The procedure involves replacing the sensor with a resistor and a capacitor with the minimum sensor range values, R_x*[min]* and C_x *[min]*. These values are then measured using (7) and (11) or (13), depending on the DP used, obtaining two estimates: $R_{x,0}$*[min]* and $C_{x,0}$*[min]*. In the next step, R_x*[min]* is replaced with a resistor with the highest sensor range value, R_x*[max]*, obtaining two new estimates: $R_{x,0}$*[max]*, $C_{x,0}$*[min]*. The pairs of points (R_x*[min]*, $R_{x,0}$*[min]*) and (R_x*[max]*, $R_{x,0}$*[max]*) determine a calibration line defined by the multiplier, m_R, and the offset, b_R; see Fig. 7a. With these parameters, a new calibrated estimate is obtained for any sensor resistance value during normal circuit operation, R_x*

$$R_x^* = m_R \cdot R_{x,0} + b_R \tag{14}$$

where $R_{x,0}$ is the estimate provided by (7) for R_x.

The procedure to obtain the new calibrated estimate of C_x, C_x* differs slightly. In this case, the aim is to obtain an offset value, C_{off}, such that

$$C_x = C_{x,0} + C_{off} \tag{15}$$

where $C_{x,0}$ is the estimate provided by (11) or (13) for a capacitance of the sensor C_x. Two values of C_{off}, C_{off}*[min]* and C_{off}*[max]*, respectively, are obtained (again experimentally) for the combination of discrete impedances R_x*[min]* - C_x*[min]* and R_x*[max]* - C_x*[min]*. These two values, together with the estimates provided by (14), generate a calibration line for C_{off}. This calibration line is defined by the multiplier, m_C, and by the offset, b_C, see Fig. 7b. Finally, a calibrated estimate of C_x, C_x*, is obtained using

$$C_x^* = C_{x,0} + m_C R_x^* + b_C \tag{16}$$

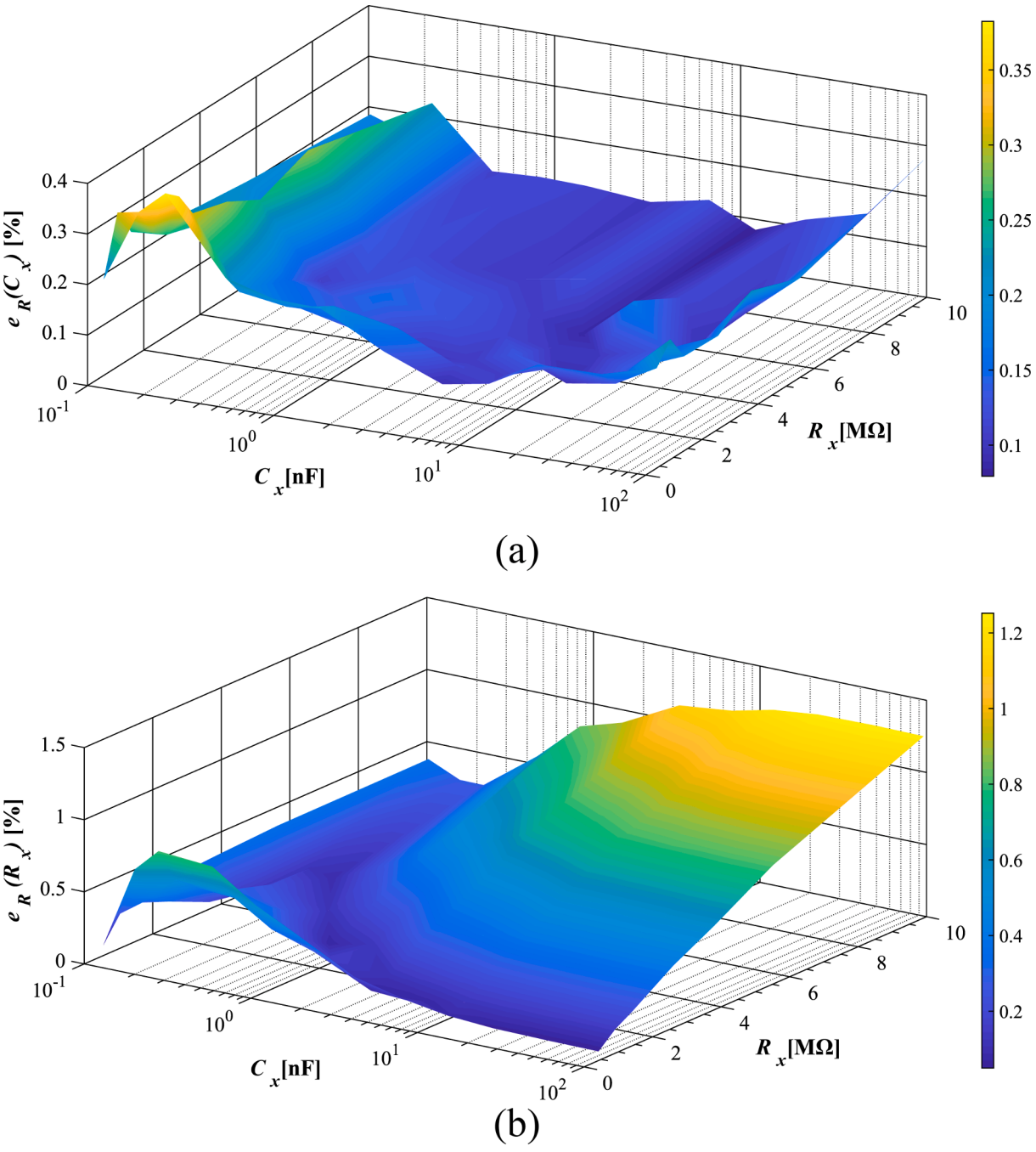


Fig. 10. Maximum relative errors for the experimental configuration of the circuit in Fig. 3. (a) for C_x, $e_R(C_x)$ (b) for R_x, $e_R(R_x)$.

Note that the calibrated estimate of R_x, R_x*, does not really depend on the value of C_x. However, the calibrated estimate of C_x, C_x*, depend on R_x (via R_x*).

The designer will only need to store four parameters in the DP, besides k

$$\lambda_i = m_i \cdot (R_A + R_B); \quad i \in \{R, C\} \tag{17}$$

$$\mu_i = b_i - \lambda_i; \quad i \in \{R, C\} \tag{18}$$

meaning R_x* and C_x* can be expressed:

$$R_x^* = \lambda_R \cdot \frac{T_{Ax}}{T_A} + \mu_R \tag{19}$$

$$C_x^* = C_{x,0} + \lambda_C \cdot \frac{T_{Ax}}{T_A} + \mu_C \tag{20}$$

The new estimate equations, (19) and (20), are similar in complexity to those used in [25], and are much simpler than those used in [27]. In any case, the DP must store three parameters more than [25], although 15 fewer than [27].

3. Experimental results and discussion

A commercial PCB has been selected for implementation, namely, the Digilent CMOD A7 (Pullman, Washington), to verify the proposed circuit's experimental operation. The system uses an advanced FPGA (Xilinx Artix 7 XC7A35T) as the DP, which allows multiple tasks to be performed in parallel, particularly the digital readout of different

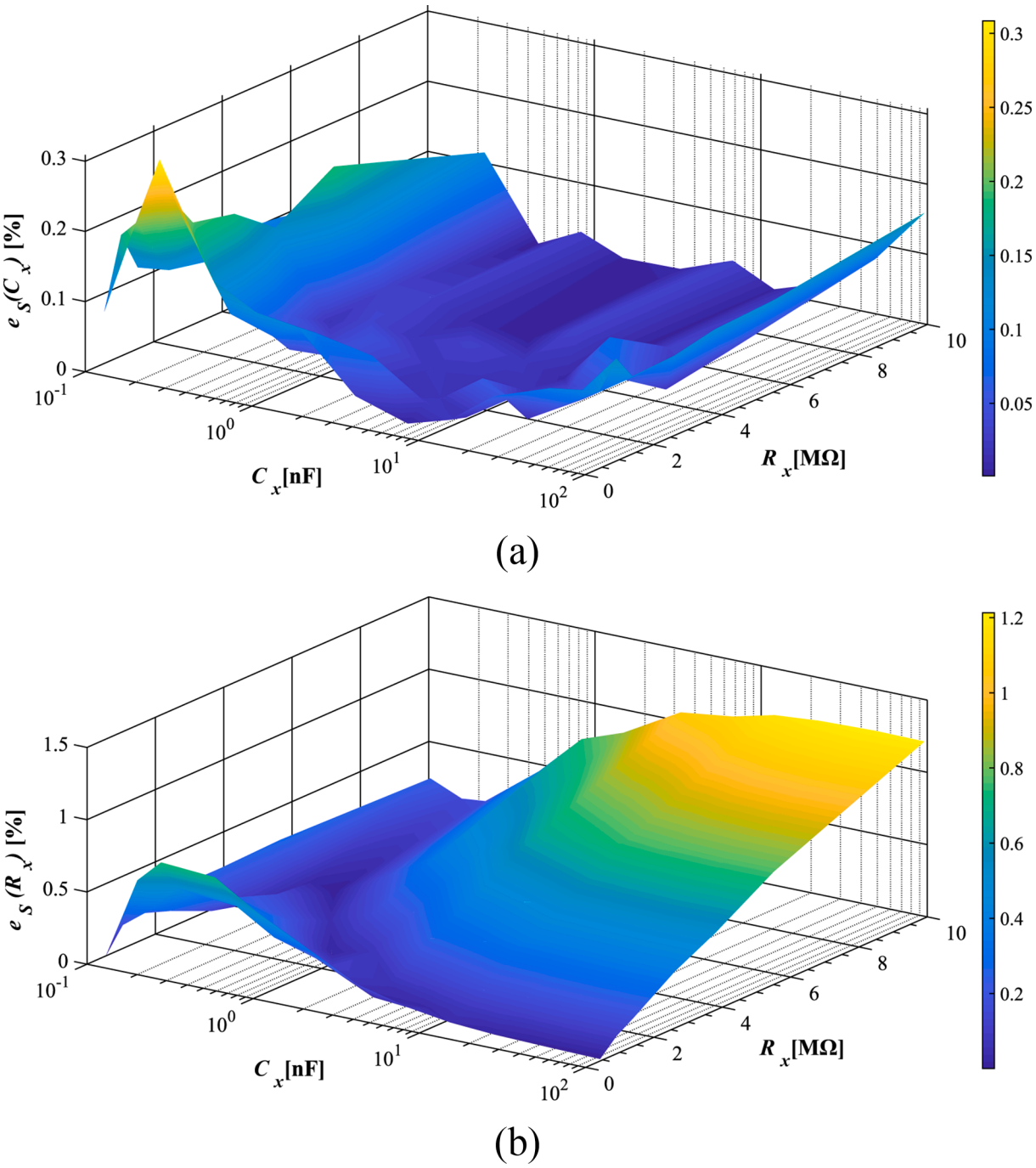
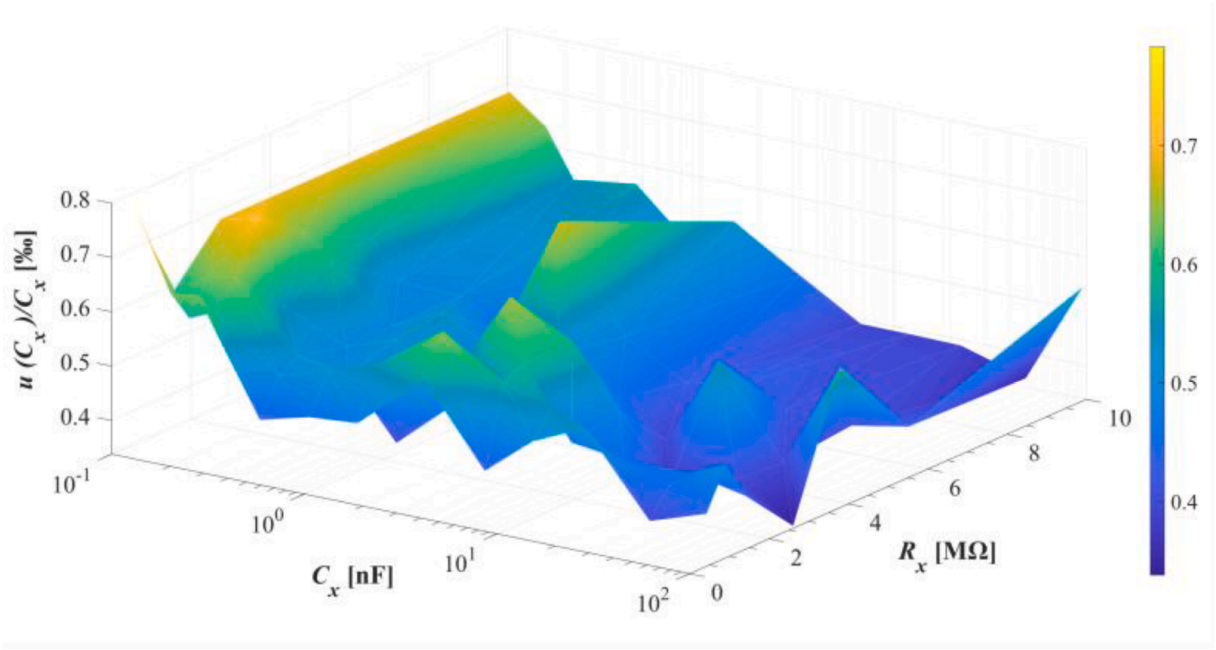


Fig. 11. Maximum systematic errors for the experimental configuration of the circuit in Fig. 3. (a) for C_x, $e_S(C_x)$ (b) for R_x, $e_S(R_x)$.

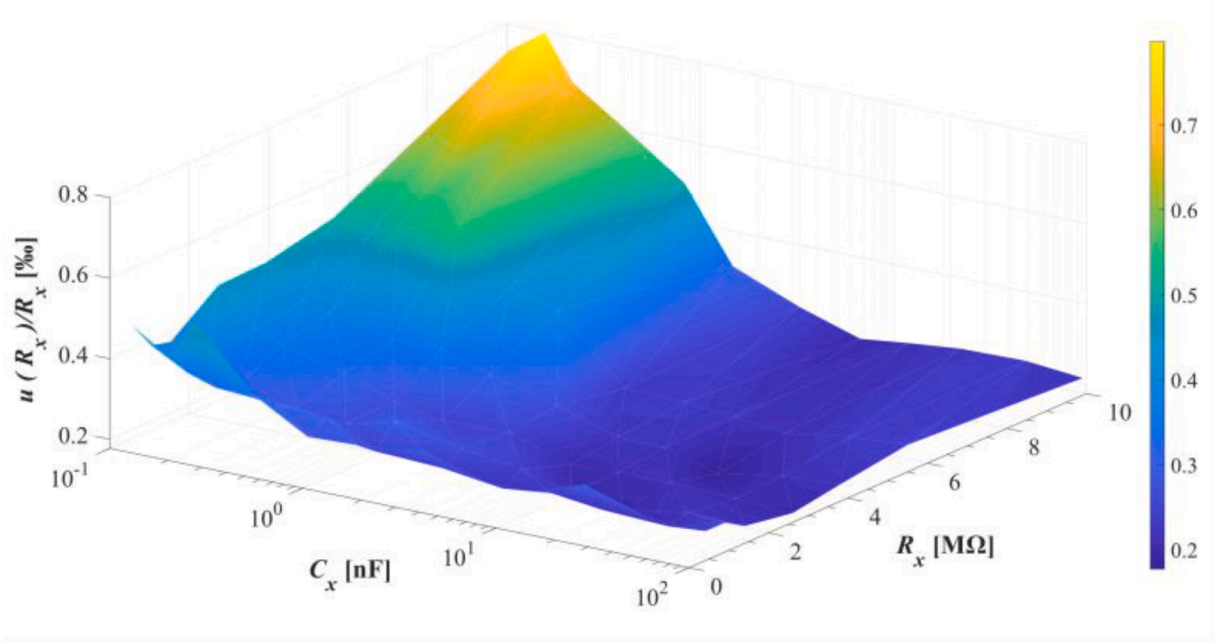
sensors. The design also includes a clock source, a communications port, additional external RAM controlled by the FPGA for increased data storage capacity, and several I/O from the FPGA that are routed to 100-mil-spaced through-hole pins. The passive components in the new DIC are connected to these pins. The voltage for the I/O pins of the FPGA is 3.3 V, which is the value of V_{DD} in Fig. 4. The threshold voltage, V_{TL}, measured experimentally, is approximately 1.26 V. Clock frequency is 50 MHz, and, thanks to the versatility of the FPGA, both the rise and fall edges of the clock have been used to detect the trigger instant.

The block diagram of the design implemented in the FPGA is shown in Fig. 8, where the two 27-bit counters used to obtain T_A, T_B, and T_{Ax} appear (each counter increments the count with a different clock edge). Thus, the final values of these measurements are expressed with 28 bits. Fig. 8 also shows the UART (Universal Asynchronous Receiver/Transmitter) module used to communicate the FPGA with a laptop receiving the results. The control unit is responsible for carrying out the steps shown in Table 1, controlling the arithmetic operations performed on the data provided by the counters, and the UART module.

On the other hand, $R_A = 75{,}028\ \Omega$ and $R_B = 54{,}915\ \Omega$ have been chosen such that they verify (2), with the left-hand member being $R_B/(R_A + R_B) = 0.42$ and the right-hand member being $V_{TL}/V_{Amax} \approx V_{TL}/V_{DD} \approx 0.38$. The ratio between R_A and R_B has been selected so the left member in (2) is as small as possible while also maintaining a sufficient safety margin with the right member. The individual values of R_A and R_B have been chosen so that $R_A + R_B \ll R_x$, which, according to (3) and (5), maximizes the quotient T_{Ax}/T_A, and, therefore, also the resolution in the estimate of R_x obtained with (7). $R_A + R_B \gg ro$ is also verified, which is true in this implementation because the FPGA pins configured as outputs



(a)



(b)

Fig. 12. Normalised uncertainty of the estimates. (a) For C_x, $u_N(C_x)$ (b) for R_x, $u_N(R_x)$.

have output resistance values around 15 Ω.

The ranges selected for the estimates are 100 pF − 95.92 nF and 500 kΩ − 10 MΩ. These ranges include those of several lossy capacitive sensors and are wider than those estimated in [25,27]. Twelve capacitors and seven discrete resistors have been used to achieve these ranges. All resistance and capacitance values were measured with an LCR-6300 meter from RS PRO.

Selecting $T_{ch} = 0.5$ ms ensures that voltages V_A and V_B are stable at the end of the charge processes (regardless of the values of C_x and R_x. Meanwhile, as the maximum experimental values of T_{Ax} and T_A (obtained for $C_x = 95.92$ nF, $R_x = 10$ MΩ) are 912.5 ms and 11.8 ms, respectively, T_M is:

$$T_M = 2{\cdot}T_{ch} + T_{Ax} + T_A = 925.3 \text{ ms} \tag{21}$$

Fig. 9 shows the real waveforms of V_A and V_B in the circuit in Fig. 3, as obtained in a Digilent Analog Discovery 2 data acquisition system with $C_x = 1.47$ nF and $R_x = 1$ MΩ. The horizontal dashed line shows the value $V_{TL} = 1.26$ V. For better visualization, the T_{ch} value has been

Table 2
Comparison.

	Work		
	[25]	[27]	This Work
C_x Range	150 – 206 pF	100 – 286 pF	100 pF – 95.92 nF
R_x Range	1 – 10 MΩ	1 – 10 MΩ	511 kΩ – 10 MΩ
DP type / Used Pins	μC / 4	μC / 3	FPGA / 3
Extra Hardware Requirements	2 Resistors, 1 Capacitor	DAC, Comparator, 2 Resistors	2 Resistors
Arithmetic Operations	Addition, Division	Addition, Division Logarithmic, Exponential	Addition, Division
Calibration	Online	Offline	Offline
Stored Parameters	2	20	2 or 5
Charging-Discharging Processes	4	2	2
Normalized T_M	1.46	2.34	0.96
$e_S(C_x)$	6%	0.71%	0.30%
$e_S(R_x)$	–	0.74%	1.21%

increased to approximately 35 ms.

To find the results presented below, a series of two hundred estimates have been made for each combination of C_x and R_x. The number of estimates made was therefore 200 × 12 × 7. Various figures of merit have been derived from these measurements, characterizing the performance of the new circuit. The first one is *Maximum Relative Error* for the estimate of X,$e_R(X)$, where X is R_x or C_x, defined by:

$$e_R(X) = \text{Max}\left(\frac{|X(j) - X_a|}{X_a} \times 100\%\right); \quad j = \{1, 2, ..., 200\} \tag{22}$$

$X(j)$ is each of the estimates of R_x or C_x, and X_a is the actual value of R_x or C_x.

Two components determine the value of $e_R(X)$. The first component is the systematic error for the estimate of C_x or R_x, $e_S(X)$, defined by

$$e_S(X) = \frac{|\overline{X} - X_a|}{X_a} \times 100\% \tag{23}$$

where $\overline{X}$ is the average of all $X(j)$. This error is mainly caused by the parasitic elements of the circuit in Fig. 6.

The second component is uncertainty in the estimates, caused by quantization errors and uncertainty in determining the trigger instant at which the time measurements are obtained. Errors due to quantification in clock cycles of the time measurements are very small in the selected experimental setup since, in the worst case (minimum R_x and C_x), the result of T_A - T_B is approximately 1200 (12 μs). Trigger uncertainty is fundamentally determined by electronic noise in nodes A and B of the circuit in Fig. 3. Total uncertainty due to these two components will be represented through the normalized uncertainty of the estimates, $u_N(X)$, obtained as a normalized standard deviation of the series of 200 measurements:

$$u_N(X) = \frac{sd(X(j))}{X_a} \times 1000‰; \quad j = \{1, 2, ..., 200\} \tag{24}$$

Fig. 10 shows the experimentally obtained values for $e_R(C_x)$ and $e_R(R_x)$. The values of $e_R(C_x)$ move in a narrow range, with a maximum of 0.38%. The area near the minimum values of C_x and R_x shows the largest errors, while in the rest of the plane, the errors are generally similar. This situation is logical since, for smaller values of C_x, the relative errors introduced by the presence of the stray capacitors in Fig. 5 should be maximum.

Moreover, although quantization errors are small when the product R_x·C_x is minimum, they can be important in calculating $e_R(C_x)$ (if R_x·C_x is a small value, as in the analyzed implementation). However, the results also show that the simple calibration process presented in section III works adequately, limiting $e_R(C_x)$ to 0.38%, as mentioned above. These errors also decrease by half from 400 pF, indicating the limit at which the calibration process would not be necessary.

$e_R(R_x)$ presents higher values than $e_R(C_x)$, reaching a maximum of 1.25%. The fact that $e_R(R_x) > e_R(C_x)$ is due to the equivalent resistor through which one of the discharges is made being the parallel of R_x with another resistor, thus limiting the resolution. Fig. 10b also shows that the largest errors generally occur when increasing the product R_x·C_x. However, it is also observed that there are local maximums of $e_R(R_x)$ for smaller values of C_x due to the quantization.

Fig. 11 shows the results for $e_S(C_x)$ and $e_S(R_x)$. The surfaces obtained in both cases have similar shapes to those found for $e_R(C_x)$ and $e_R(R_x)$, respectively. The surfaces of Fig. 11 show a generally uniform reduction of systematic errors regarding relative errors. As the maximum of $e_S(C_x)$ is 0.30% and the maximum of $e_S(R_x)$ is 1.21%, these reductions are small, showing that systematic errors are the main causes of error in the estimates.

Fig. 12, which shows the other error components, $u_N(C_x)$ and $u_N(R_x)$, confirms this analysis. The first thing that is striking in Fig. 12 is the much smaller values of these uncertainties when compared to e_S. The maximum for $u_N(C_x)$ is 0.078%, while the maximum for $u_N(R_x)$ is 0.079%. Since these errors are small, analyzing the form of the curves in Fig. 12 does not make much sense (beyond the expected local maximums for the minimums of C_x and R_x).

Finally, Table 2 compares the characteristics of the new proposal and the other DICs presented in the literature for reading lossy capacitive sensors. The range of values of R_x is greater in the new proposal than in the rest. In particular, the range of C_x significantly expands the method's applicability to more sensors. The following rows of Table 2 show the hardware's characteristics, demonstrating that the new proposal is the best option except for the number of stored parameters.

Table II also shows a more appropriate figure of merit to compare time performances, namely *Normalized* T_M. This parameter results from the quotient between the time required to estimate the combination of C_x and R_x that produces the highest time constant and the value of this time constant. The new circuit presents *Normalized* T_M values with 34% and 59% reductions compared to the other proposals.

Finally, errors in the estimates are compared using systematic error as the figure of merit since this is the parameter provided in [25,27]. Although the capacitance range is much larger in the new proposal, the value of $e_S(C_x)$ is the smallest, reducing the smallest error in the other proposals by 58%. The last row in Table 2 shows that $e_S(R_x)$ is larger than in [27]. However, this is not necessarily a drawback since the estimate of this parameter is generally not so important in a lossy capacitive sensor ([25] does not even provide this parameter).

4. Conclusions

A new type of Direct Interface Circuit (DIC) has been proposed for the digital readout of lossy capacitive sensors. In addition to the sensor, the circuit only needs two resistors connected to a Digital Processor (DP) that performs a magnitude-to-time-to-digital conversion.

The circuit performs only two charge–discharge processes to obtain an estimate of the sensor's capacitance and resistance values. The estimates are calculated using simple arithmetic operations performed on the three or four time measurements obtained in the discharge processes. A simple offline calibration process has also been presented to reduce estimate errors due to parasitic circuit elements.

A design based on an FPGA has been implemented as a proof of concept. The results have been compared with the other DICs proposed in the literature for reading lossy capacitive sensors. The comparison shows that, despite the simplicity of the proposal, the normalized measurement time is only 0.96 (which implies reductions of between 34% and 58% compared to other proposals). The systematic error in estimating the sensor capacitance is 0.3% over a wide range of values

100 pF – 95.92 nF.

CRediT authorship contribution statement

José A. Hidalgo-López: Conceptualization, Methodology, Software, Validation, Investigation, Writing – original draft, Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

This work was supported by the Spanish Government under contract PID2021-125091OB-I00.

References

[1] A. Oprea, N. Bârsan, U. Weimar, M.L. Bauersfeld, D. Ebling, J. Wöllenstein, Capacitive humidity sensors on flexible RFID labels, Sens. Actuat., B Chem. 132 (2) (2008) 404–410.
[2] A. Rivadeneyra, J. Fernández-Salmerón, M. Agudo-Acemel, J.A. López-Villanueva, L.F. Capitan-Vallvey, A.J. Palma, Printed electrodes structures as capacitive humidity sensors: A comparison, Sens. Actuat. A 244 (2016) 56–65.
[3] P. Vooka, B. George, A direct digital readout circuit for impedance sensors, IEEE Trans. Instrum. Meas. 64 (4) (2014) 902–912.
[4] S.C. Bera, H. Mandal, A flow measurement technique using a noncontact capacitance-type orifice transducer for a conducting liquid, IEEE Trans. Instrum. Meas. 61 (9) (2012) 2553–2559.
[5] A. Fendri, A.Y. Kallel, H. Nouri, H. Ghariani, O. Kanoun, Measurement system for lossy capacitive sensors: Application to edible oils quality assessment, Sensors (Switzerland) 19 (19) (2019) 1–19.
[6] M.C. Carotta, G. Martinelli, L. Crema, C. Malagù, M. Merli, G. Ghiotti, E. Traversa, Nanostructured thick-film gas sensors for atmospheric pollutant monitoring: Quantitative analysis on field tests, Sens. Actuat. B Chem. 76 (1-3) (2001) 336–342.
[7] L. Bissi, M. Cicioni, P. Placidi, S. Zampolli, I. Elmi, A. Scorzoni, A programmable interface circuit for an ultralow power gas sensor, IEEE Trans. Instrum. Meas. 60 (1) (2011) 282–289.
[8] A. Vergara, E. Llobet, J. Ramirez, P. Ivanov, L. Fonseca, S. Zampolli, A. Scorzoni, T. Becker, S. Marco, J. Wollenstein, An RFID reader with onboard sensing capability for monitoring fruit quality, Sens. Actuat. B Chem. 127 (1) (2007) 143–149.
[9] D. Goeger, M. Blankertz, and H. Woern, A tactile proximity sensor, Proc. IEEE Sensors, pp. 589–594, 2010.
[10] J. Castellanos-Ramos, et al., Adding proximity sensing capability to tactile array based on off-the-shelf FSR and PSoC, IEEE Trans. Instrum. Meas. 69 (7) (2020) 4238–4250.
[11] A. Troiano, E. Pasero, L. Mesin, New system for detecting road ice formation, IEEE Trans. Instrum. Meas. 60 (3) (2011) 1091–1101.
[12] A.K.R. Segundo, É.S. Pinto, G.A. Santos, P.M. De Barros Monteiro, Capacitive impedance measurement: dual-frequency approach, Sensors (Switzerland) 19 (11) (2019) pp.
[13] A. Depari, A. Flammini, D. Marioli, and E. Sisinni, A fast-readout interface circuit for high-value and wide-range resistive chemical sensors, 2010 IEEE Int. Instrum. Meas. Technol. Conf. I2MTC 2010 - Proc., vol. 59, no. 5, pp. 116–120, 2010.
[14] S. Malik, L. Somappa, M. Ahmad, T. Islam, M.S. Baghini, An accurate digital converter for lossy capacitive sensors, Sens. Actuat. A Phys. 331 (2021), 112958.
[15] A.U. Khan, T. Islam, B. George, M. Rehman, An efficient interface circuit for lossy capacitive sensors, IEEE Trans. Instrum. Meas. 68 (3) (2019) 829–836.
[16] S. Malik, K. Kishore, T. Islam, Z.H. Zargar, S.A. Akbar, A time domain bridge-based impedance measurement technique for wide-range lossy capacitive sensors, Sens. Actuat. A 234 (2015) 248–262.
[17] S. Malik, M. Ahmad, L. Somappa, T. Islam, M.S. Baghini, AN-Z2V: Autonulling-based multimode signal conditioning circuit for R-C sensors, IEEE Trans. Instrum. Meas. 69 (11) (2020) 8763–8772.
[18] X. Li, G.C.M. Meijer, Elimination of shunting conductance effects in a low-cost capacitive-sensor interface, IEEE Trans. Instrum. Meas. 49 (3) (2000) 531–534.
[19] V. Sreenath, B. George, A direct-digital interface circuit for sensors representable using parallel R-C model, Conf. Rec. - IEEE Instrum. Meas. Technol. Conf. vol. 2016-July (2016) 3–7.
[20] K. Elangovan, C.S. Anoop, A digital readout suitable for resistive sensors affected with a parasitic capacitance element, Conf. Rec. - IEEE Instrum. Meas. Technol. Conf., vol. 2021-May, no. 1, pp. 3–7, 2021.
[21] F. Reverter, M. Gasulla, R. Pallàs-Areny, A low-cost microcontroller interface for low-value capacitive sensors, Conf. Rec. - IEEE Instrum. Meas. Technol. Conf. 3 (May) (2004) 1771–1775.
[22] Z. Czaja, "A measurement method for capacitive sensors based on a versatile direct sensor-to-microcontroller interface circuit, Meas. J. Int. Meas. Confed. 155(2020) 107547.
[23] O. Lopez-Lapeña, E. Serrano-Finetti, O. Casas, Calibration-less direct capacitor-to-microcontroller interface, Electron. Lett 52 (4) (2016) 289–291.
[24] J. A. Hidalgo-Lopez, J. Castellanos-Ramos, Simplifying capacitive sensor readout using a new direct interface circuit, IEEE Trans. Instrum. Meas. 72 (2022) 1–1.
[25] F. Reverter, Ò. Casas, A microcontroller-based interface circuit for lossy capacitive sensors, Meas. Sci. Technol. 21 (6) (2010) pp.
[26] Y. Wang, C. Zhou, H. Lu, "An enhanced method for measuring capacitance based on the direct interface circuit", in, Chinese Control Conference (CCC) 2019 (2019) 7028–7032.
[27] Z. Czaja, A measurement method for lossy capacitive relative humidity sensors based on a direct sensor-to-microcontroller interface circuit, Measurement 170 (2021), 108702.
[28] M.J.M. Pelgrom, Accuracy: Deterministic and Random Errors, in: M.J.M. Pelgrom (Ed.), Analog-to-Digital Conversion, Springer International Publishing, Cham, 2022, pp. 247–316.