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DESIGN OF A BURST MODE ULTRA HIGH-SPEED LOW-NOISE CMOS IMAGE SENSOR

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DESIGN OF A BURST MODE ULTRA HIGH-SPEED LOW-NOISE CMOS IMAGE SENSOR

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by Xin Yue

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Abstract

Ultra-high-speed (UHS) image sensors have been extensively used in various fields such as medical, scientific, and industrial applications to visualize and understand UHS phenomena. Recently, several published studies have successfully achieved frame rates of up to millions of frames per second (Mfps) for these specialized sensors. However, these studies have primarily relied on advanced processes like 130nm backside illumination (BSI) or customized processes to meet the specific design requirements of UHS image sensors. Therefore, there is a general interest in reducing image sensor fabrication costs and improving process compatibility.

This thesis presents an ultra-high-speed high conversion-gain CMOS image sensor (CIS) based on charge-sweep transfer gates in a standard 180nm CIS process. By optimizing the photodiode geometry and utilizing charge-sweep transfer gates, the proposed pixels achieve charge transfer time of less than 10ns without process modification. Additionally, the gate structure significantly reduces the floating diffusion capacitance, thus increasing the conversion gain. To demonstrate the effectiveness of the proposed design, a few pixels were modeled and simulated in TCAD. Finally, a proof-of-concept CMOS image sensor was designed, taped out and characterized.

This thesis covers the development and characterization of the burst mode UHS high conversion-gain image sensor and emphasizes the reduction of charge transfer time, improvement of pixel conversion gain in a standard process. The projected performance of this pixel enables the burst mode image sensor to run at 20 Mfps with better than state-of-art noise (<<8.4e-), which shows great potential in the cost-sensitive niche market.

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First and foremost, I would like to express my utmost gratitude to Prof. Eric Fossum for accepting me as his Ph.D. student at Dartmouth College three years ago. His unparalleled support to my research work, and his world-class experience and expertise, have been invaluable throughout this amazing journey. At every stage, he has shown unquestioning faith in me and provided constant encouragement, making it possible for me to realize my Ph.D. dream.

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List of Acronyms

AC	Alternating Current
ADC	Analog to Digital Convertor
APS	Active-Pixel Image Sensor
BCCD	Buried-channel CCD
BSI	Back Side Illumination
CCD	Charge-Coupled Device
CDS	Correlated-Double-Sampling
CG	Conversion Gain
CIS	CMOS-Image-Sensor
CMOS	Complementary Metal Oxide Semiconductor
CML	Current-Mode-Logic
CTE	Charge Transfer Efficiency
CTI	Charge Transfer Inefficiency
DC	Direct Current
DDS	Double Delta Sampling
DIBL	Drain Induced Barrier Lowering
DRAM	Dynamic Random-Access Memory
DSLR	Digital Single-Lens Reflex

DNW	Deep N-Well
DN	Digital Number
FD	Floating Diffusion
FPS	Frames Per Second
FPN	Fixed Pattern Noise
FPGA	Field Programmable Gate Arrays
ILT-CCD	Interline Transfer CCD
LDD	Light Doped Drain
LSB	Least Significant Bit
LGA	Land Grid Array
MC	Monte-Carlo
MOM	Metal Oxide Metal
MPW	Multi Project Wafer
NMOS	N-type Metal Oxide Semiconductor
NDA	Non-disclosure Agreement
PAL	Photon Attenuation Layer
PCB	Printed Circuit Board
PCH	Photon Counting Histogram
PTC	Photon Transfer Curve

PPD	Pinned Photodiode
PGA	Programmer Gain Amplifier
QE	Quantum Efficiency
QIS	Quanta Image Sensor
RMS	Root Mean Square
RST	Reset Transistor
RSEL	Row-Select Transistor
SAR ADC	Successive Approximation ADC
SCCD	Surface-channel Charge-Coupled-Device
SDL	Sub Diffraction Limit
SF	Source Follower
SiO_2	Silicon Dioxide
SNR	Signal to Noise Ratio
SoA	State-of-the-Art
SOI	Silicon On Insulator
SW	Storage Well
TCAD	Technology Computer Aided Design
TSV	Through Silicon Vias
TX	Transfer Transistor

1 Introduction

The invention of the charge-coupled device (CCD) image sensor in 1969 and, most significantly, of the complementary metal oxide semiconductor (CMOS) active-pixel image sensor (APS) in 1993 has greatly impacted and influenced modern life through solid-state imaging technology. Nowadays, solid-state image sensors are ubiquitous, found in the "eyes" of self-driving vehicles, on the back of smartphones, and in X-ray sensors for medical instruments. In 2022, global shipments of CMOS-Image-Sensors (CIS) for mobile phones reached 1.21 billion units, equivalent to 3.3 million units per day [3].

1.1 Motivation

The objective of this research is to provide an observation instrument of the dynamic response exhibited by materials when subjected to different stress levels. The dynamic response of interest occurs typically within a time frame of microseconds or less. To gain insight into the material properties under examination, high-speed videos or images capturing the changes under a bright X-ray source with millions of frames per second are necessary. Such observations may lead to potential improvements in the material's characteristics. For this purpose, three CMOS image sensors have been designed and fabricated over the last three and a half years.

The phase one chip is a 3T CMOS image sensor that operates at 500 frames per second (fps) and serves as a test vehicle to validate the Photon Attenuation Layer (PAL) developed by Prof. Jifeng Liu's group [4] at Dartmouth College. In phase two, a continuous-mode global shutter CMOS image sensor with 78 thousand frames per second

(Kfps) is introduced, and in phase three, a low-noise burst-mode CMOS image sensor is designed, operating at 20 million frames per second (Mfps).

In Chapter 3 of this thesis, a comprehensive investigation into state-of-the-art burst-mode image sensors reveals that designers use either an advanced or customized process to meet the design requirements of ultra-high-speed image sensors. This study began right after the breakout of the global COVID-19 pandemic, which compelled many people to work remotely and significantly heightened demand for consumer electronics. Semiconductor foundries were hampered by production capacity limitations or were hesitant to experiment with non-standard processes for small-volume designs, including a simple process that required no additional masks.

Despite the unavailability of advanced or customized processes, this thesis presents the development, design, simulation, and characterization of an ultra-high-speed burst mode image sensor based on a standard 180nm PPD process and incorporating a novel charge-sweep transfer gate. The device structure is optimized to achieve similar or better performance than state-of-the-art works.

1.2 Introduction of the Burst Mode Image Sensor

In contrast to the general-purpose CMOS image sensors utilized in consumer electronics, ultra-high-speed image sensors are commonly employed in scientific imaging to capture and examine ultra-high-speed phenomena. One example is the characterization of material properties during high-speed, high-energy particle impact. While conventional image sensors work in continuous mode, where they repetitively conduct sampling and reading operations, the frame rate of such sensors is typically limited to a few thousand frames per second due to factors such as in-pixel source follower

bandwidth, on-chip ADC conversion rate, or output transmitter bit rate (further discussed in Chapter 3). However, the burst-mode image sensor, which was first introduced by Walter F. Kosonocky, Guang Yang, and others [5, 86, 87, 88] in 1994, offers a solution that can efficiently operate at millions of frames per second by first sampling and continuously storing images on-chip for multiple frames before gradually reading out the stored data. Depending on the sensor's design, the sampled information may be stored in in-pixel or off-pixel storage units, and the number of storage units per pixel typically determines the recording length for the burst-mode image sensor. According to [6], 100 frames are generally sufficient for analyzing high-speed events. Recent studies of burst-mode image sensors [7, 8, 9, 10, 11, 12, 13, 14] have boosted the frame rate to over 100 Mfps with recording lengths ranging from 5 to 1220 frames.

1.3 Thesis Organization

This dissertation is organized into eight chapters.

In Chapter 2, the history of solid-state image sensors is explored, from the inception in charge-coupled device (CCD) to the evolution into CMOS image sensors, and eventually, the third generation of sensors known as quanta image sensors (QIS). Understanding the strengths and limitations of each type of sensor is crucial for system-level trade-offs in image sensor design.

Chapter 3 focuses on the frame rate limitations of high-speed image sensors, examining different approaches to high-speed imaging such as continuous mode, burst mode, and compressive-sampling mode. The chapter also discusses the advantages and limitations of state-of-the-art works.

Based on the analysis in Chapter 3, Chapter 4 delves into the design and simulation of high-speed pixels. The chapter explores the optimization of charge transfer time and pixel conversion gain in a standard process, presenting four different variants of pixel design.

Chapter 5 models the entire image sensor chip based on the pixels designed in Chapter 4. The chapter discusses system-level trade-offs and design considerations, presenting details of the circuitry such as the correlated-double-sampling (CDS) circuit, row drivers, and in-pixel storage network. Additionally, system-level parameters like total input-referred temporal noise and average power consumption are estimated.

In Chapter 6, the dissertation describes the prototype test system design, the methodology for sensor characterization and measurement results, and analyzes discrepancies from theoretical calculations.

Chapter 7 explores the potential for process improvements if a customized process is accessible, as well as future work for X-ray imaging applications. The chapter also discusses more applications of charge sweep transfer gate and the potential commercialization of this sensor.

Finally, Chapter 8 presents the conclusion of this dissertation, summarizing the key findings and contributions to the field of ultra-high speed CMOS image sensor.

2 Introduction of Solid-State Imaging

2.1 Charge-Coupled Device

The charge-coupled device (CCD) is widely acknowledged as the first-generation solid-state image sensor. Its basic concept involves a series of CMOS capacitors connected in a chain, as shown in Figure 2-1. By applying various control voltages to the electrodes, the CMOS capacitors can switch between accumulation, depletion, and inversion modes. Figure 2-2 provides electrostatic potential diagrams depicting the different working modes.

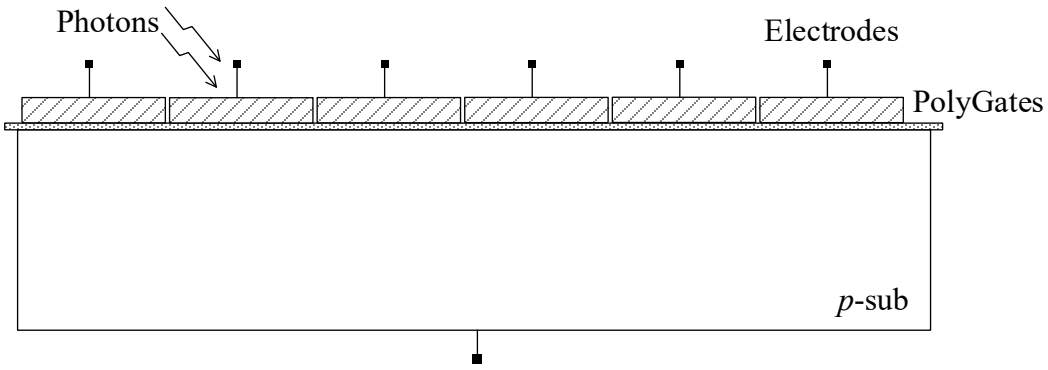
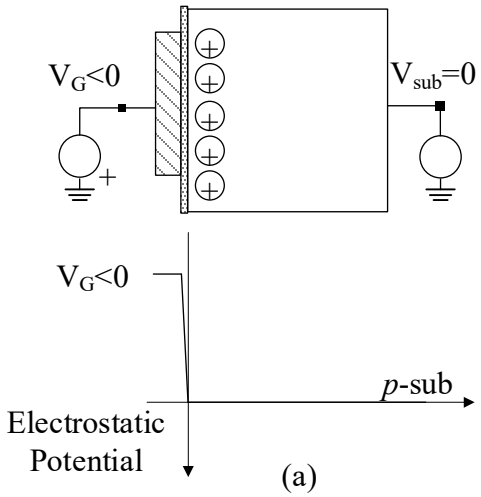


Figure 2-1 Schematic view of a surface channel CCD



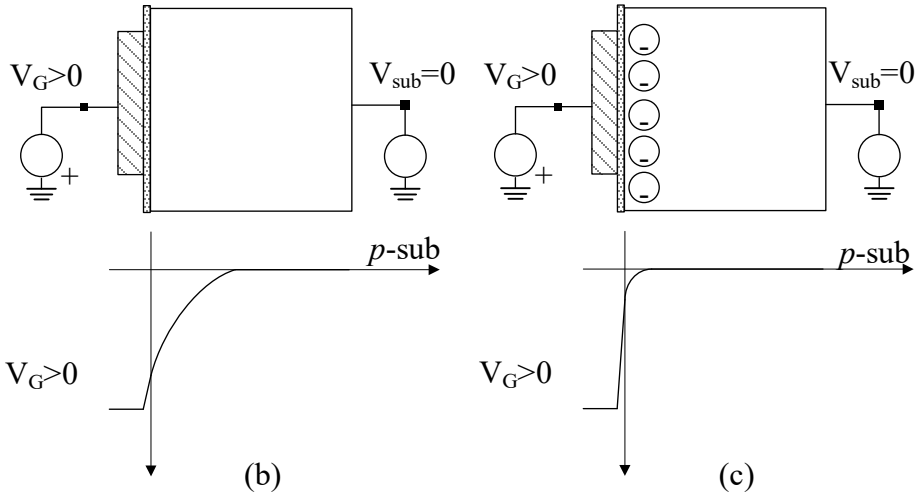


Figure 2-2 Various working modes and electrostatic potential diagrams of a CMOS capacitor: (a) accumulation, (b) depletion, (c) inversion

The working principle of CCD is illustrated in Figure 2-3. Assume the poly-gate gap between two adjacent CMOS capacitors is negligible. During the inversion mode, photon-generated charges (electrons in this case) are collected and confined at the interface between the bulk and silicon dioxide, where the highest electrostatic potential in the bulk is as shown in Figure 2-2 (c) and Figure 2-3 (a). With an "On" voltage applied on the adjacent CMOS capacitor, these electrons start to flow to the adjacent capacitors, as Figure 2-3 (b) depicts. With an "Off" voltage applied on the current CMOS capacitor, these electrons are forced to leave the current capacitor and stay at the adjacent capacitor, as Figure 2-3 (c) depicts.

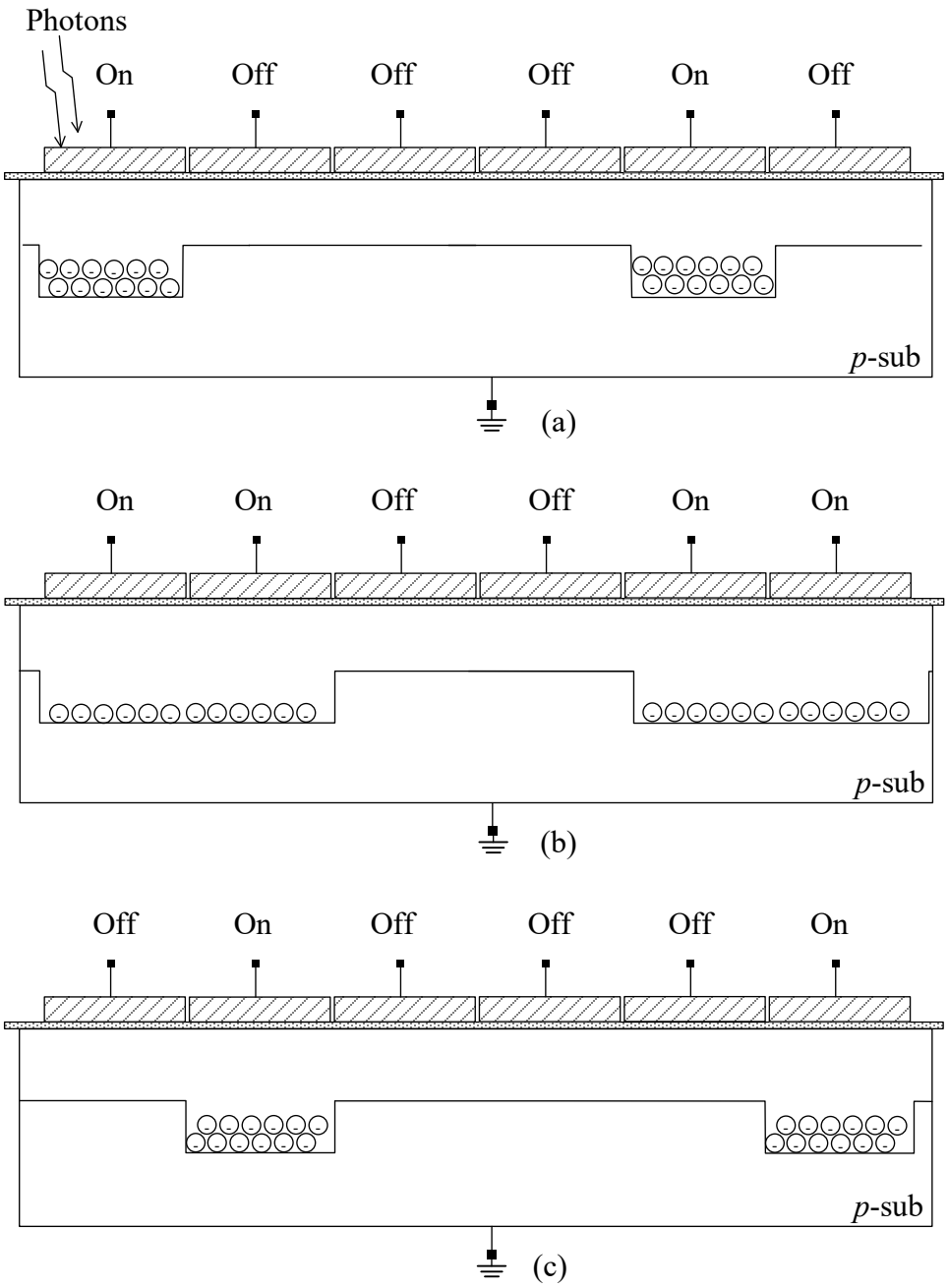


Figure 2-3 Working principles of a CCD image sensor

As chargers are transferred at the bulk surface, this kind of CCD is classified as surface-channel charge-coupled-device (SCCD). The early SCCDs suffered from large dark currents and considerable charge transfer inefficiency due to unsuppressed surface states at the interface between silicon and silicon dioxide. Two years after SCCD was

invented, Bell Labs introduced the buried-channel CCD (BCCD), as shown in the Figure 2-4. An *n*-type layer is deposited on top of the *p*-type substrate, and the doping concentration of the *n*-type layer is carefully chosen so that the *n*-type layer can be fully depleted during the operation of BCCD.

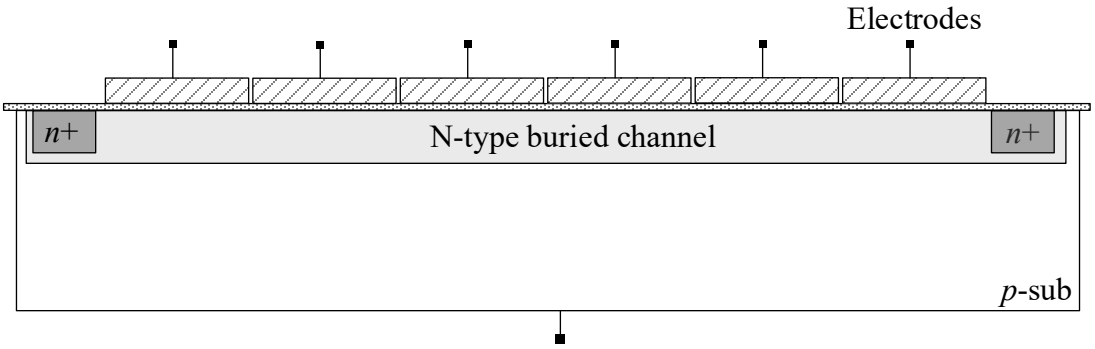


Figure 2-4 Schematic view of buried channel CCD

Figure 2-5 (a) and Figure 2-5 (b) show the electrostatic potential diagram of BCCD when the channel is empty and filled, respectively. Compared to SCCD, the highest potential of BCCD in bulk is in the channel instead of the surface. If the "voltage distance" from the channel to the surface is larger than a few kT/q (-26mV at room temperature), the interaction of charges with the surface state can be negligible [16]

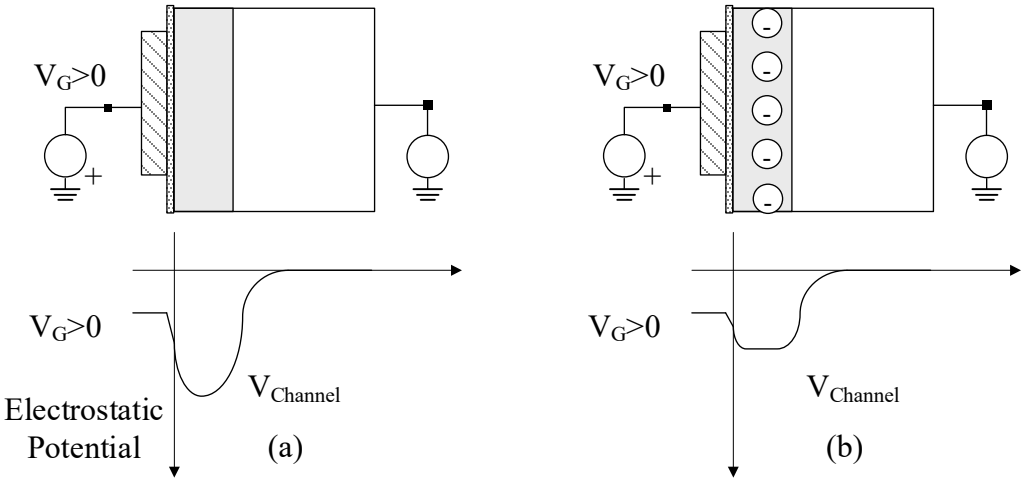


Figure 2-5 Various working modes and electrostatic potential diagrams of a BCCD cell: (a) depleted, (b) filled

The early CCD image sensors utilized a full-frame transfer architecture, which employed CCD cells as photodetectors and charge-coupled devices. When the mechanical shutter is open, photons strike silicon, generating electron-hole pairs. Holes move away to the substrate while electrons get collected by the CCD cells. Upon closing the mechanical shutter, ideally, no more photons can strike the photodetectors. Previously collected charges are then shifted by CCD cells from top to bottom and left to right, ending up at the floating diffusion (FD), without being affected by photons. The charges are then converted into voltage at FD and read out by the following circuit, which, in this case, happens to be an operational amplifier. Figure 2-6 displays the block diagram of the full-frame CCD image sensor.

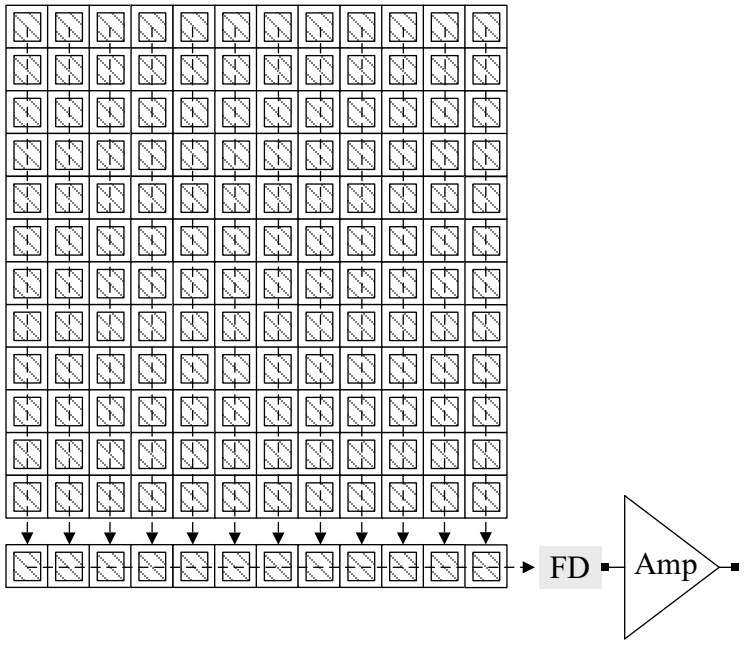


Figure 2-6 Block diagram of a frame-transfer CCD image sensor

In 1973, the interline transfer (ILT) CCD image sensor was proposed [17] to eliminate the need for a mechanical shutter. The ILT-CCD design incorporates one photodiode and one charge-coupled device in each unit cell, as illustrated in Figure 2-7. During the integration period, CCD cells are biased with an “Off” voltage, and with metal shielding covering them, photon-generated electrons are only collected in the photodiodes. During the readout period, CCD cells transfer charges from the photodiodes and move them from top to bottom and left to right CCD cells until they reach the floating diffusion (FD), where they are then read out.

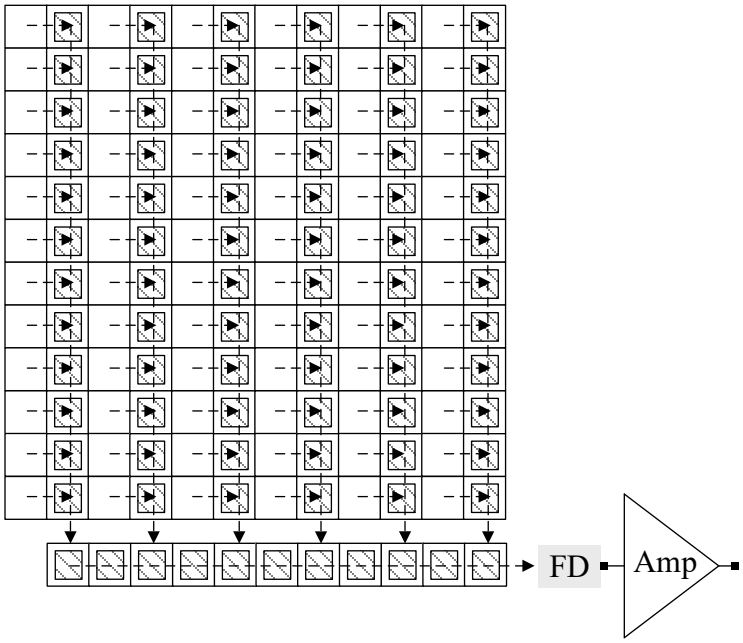


Figure 2-7 Block diagram of a interline-transfer CCD image sensor

Early ILT-CCD image sensors used *an n+/p* junction as a photodetector. However, due to the heavily doped *n*-type dopant present in the photodetector, the electrons cannot be completely depleted during the charge transfer phase. This results in the carryover of residual signal charges from previous frames into subsequent ones, leading to "image lag" and hindering the performance of ITL-CCD imaging. To illustrate

this phenomenon, Figure 2-8 displays the potential-well diagram before, during, and after photoelectrons are transferred.

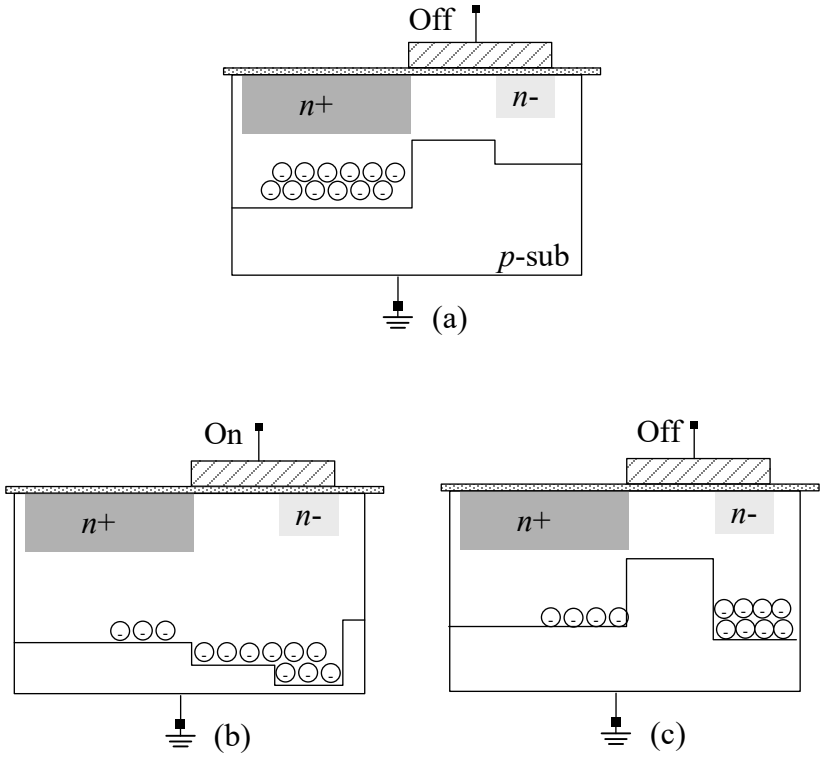


Figure 2-8 Potential-well diagrams of a ILT-CCD cell: (a) before charge transfer, (b) during charge transfer and (c) after charge transfer

In 1980, Teranishi et al. from NEC [18, 102] developed a buried photodiode structure, as illustrated in Figure 2-9, which includes a heavily doped *p*+ layer on top of the *n* layer. This structure allows for full depletion of the *n*-layer during charge transfer, eliminating the "image lag" common to ITL-CCDs and pinning the surface potential, hence its name "pinned-photodiode (PPD)," which has become prevalent in solid-state image sensors. Additionally, the pinned photodiode structure has been shown to reduce dark current originating from surface states and enhance the quantum efficiency (QE) for blue-light.

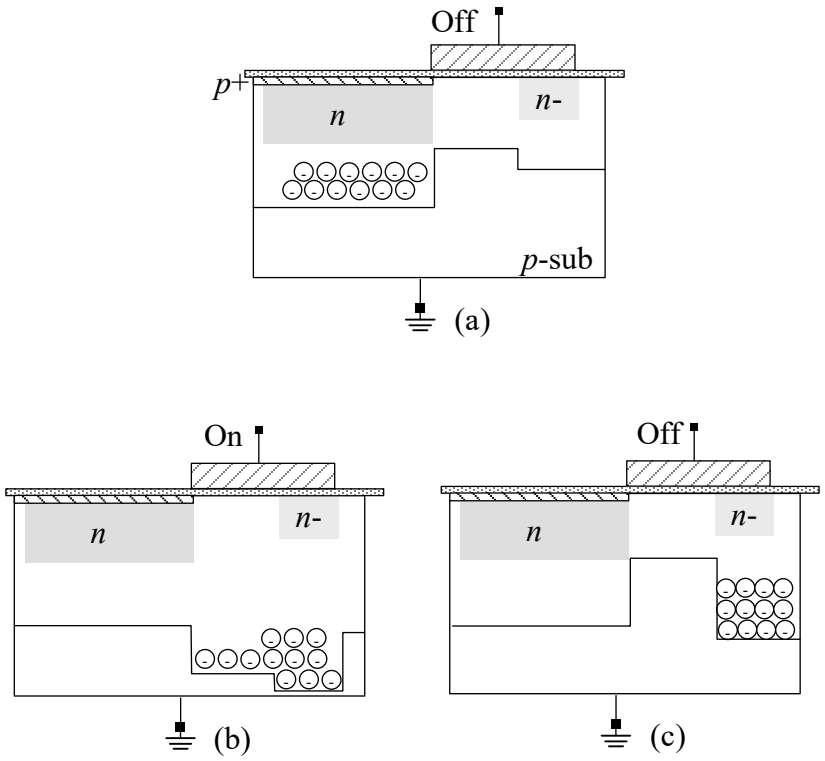


Figure 2-9 Potential-well diagrams of a PPD based ILT-CCD cell: (a) before charge transfer, (b) during charge transfer and (c) after charge transfer

2.2 CMOS Image Sensor

Although the imaging performance of CCD is constantly evolving, it is difficult for CCD image sensors to take advantage of advanced CMOS technologies due to their specialized process requirements, such as double ploy layers and high control voltage tolerance (>5V). Therefore, in 1993, Dr. Eric R. Fossum introduced a CMOS-based image sensor [2] that has been widely accepted as the second-generation solid-state image sensor. The CMOS image sensor integrates photo-detectors, analog buffers, column readout circuit, analog-to-digital converters (ADC), and digital timing control blocks into a single chip, as shown in Figure 2-10, and is known as "Camera on a Chip" [73]. Moreover, with the continuous scaling of CMOS technology, the imaging quality of CMOS image sensors is consistently improving.

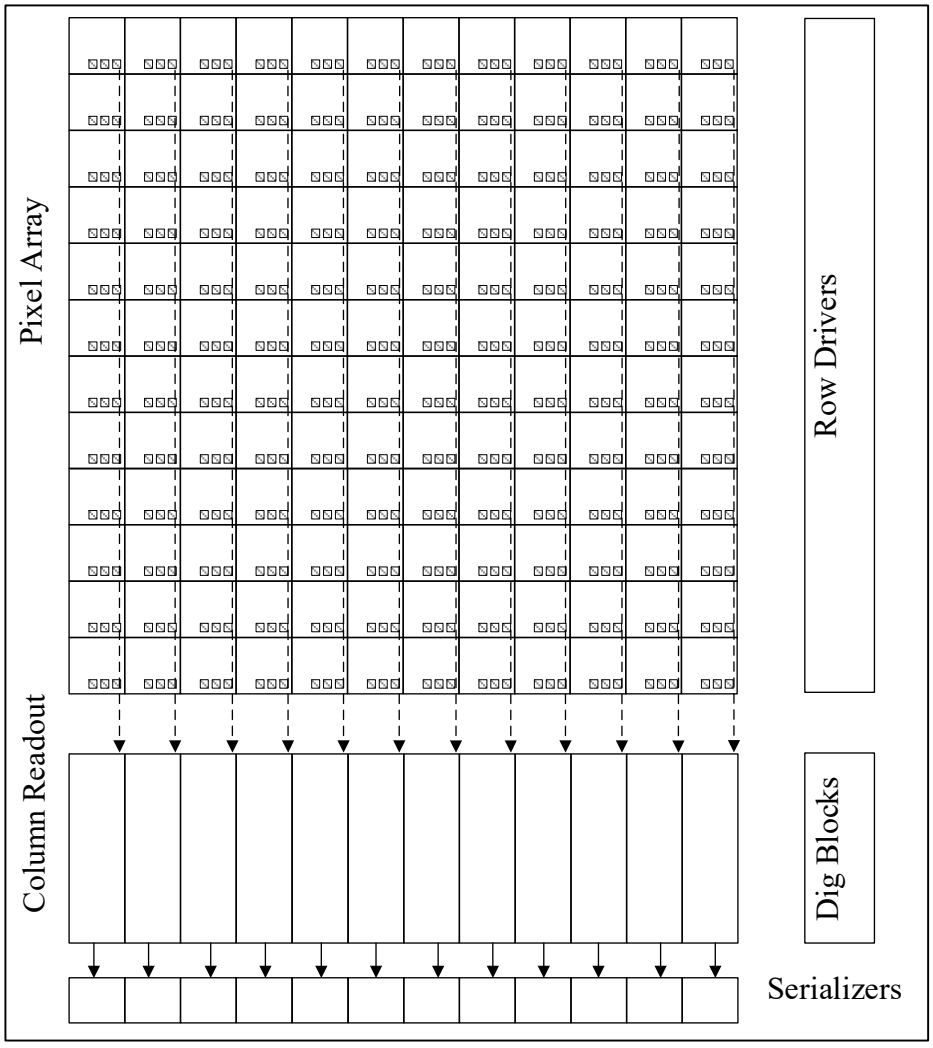


Figure 2-10 Block diagram of CMOS image sensor

Figure 2-11 displays the schematic of a 3T CMOS pixel consisting of three NMOS transistors from left to right: Reset Transistor (RST), Source Follower (SF), and Row-Select Transistor (RSEL). During the pixel integration period, the RST transistor is turned on to reset the photodiode cathode to a high voltage and then left floating. Photon-generated electrons accumulate in the photodiode storage well (SW), while the photon-generated holes are pushed towards the substrate. As the photodiode cathode is left floating, the voltage of the cathode varies according to the number of electrons accumulated in SW. At the end of the integration period, the cathode voltage is buffered

out through the in-pixel SF and sampled by the column circuit, referred to as V_{sig}. Subsequently, the photodiode is reset again by turning on the RST transistor, and the cathode voltage is sampled again by the column circuit, referred to as V_{rst}. Figure 2-12 demonstrates a detailed timing diagram of 3T pixel operation.

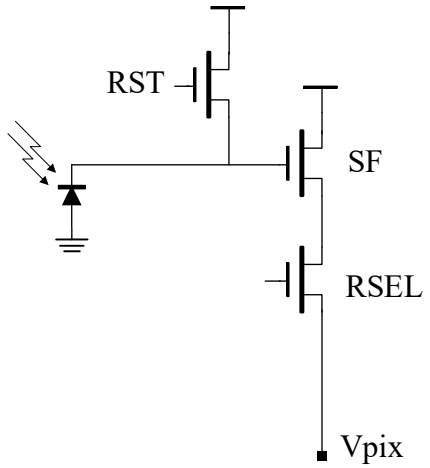


Figure 2-11 Schematic of a 3T CMOS pixel

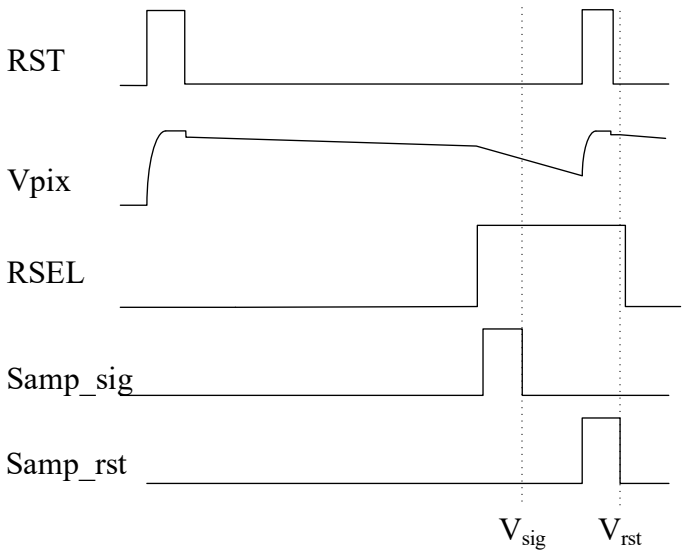


Figure 2-12 Timing diagram for a 3T CMOS pixel

To the first order, V_{sig}, $V_{rst,}$ and number of collected electrons (n) follow:

$$V_{rst} - V_{sig} = \frac{n \cdot q}{C_{PD}} \quad (2-1)$$

Here, C_{PD} denotes photodiode capacitance, and q represents the elementary charge. The voltage difference between V_{rst} and V_{sig} is directly proportional to the number of electrons collected in SW during the integration period. Consequently, the column circuit can "interpret" the object sensed by a pixel based on the voltage difference between V_{rst} and V_{sig}.

However, since V_{rst} is reset and sampled after V_{sig}, there is little correlation between these two signals. This makes it difficult for a 3T pixel image sensor to implement an effective correlated-double-sampling (CDS), which is an essential technique used to reduce low-frequency thermal and flicker noise of pixel (More details about CDS will be discussed in later chapters.) [103, 104, 105, 106, 107] have reported various techniques to reduce 3T pixel reset noise. However, these methods usually involve hardware complexity and other constraints. As a result, the 3T CMOS image sensor's overall temporal noise is generally dominated by pixel reset KT/C noise.

Despite its limitations, the 3T pixel remains a popular choice for certain applications due to its low cost and ease of fabrication. For example, it is commonly used in scenarios where a fully depleted photodiode is not achievable, such as with organic [75] and microbolometer infrared image sensors [74]. An early-developed 500 fps 3T CMOS image sensor in this project designed for X-ray applications is depicted in Figure 2-13. This sensor utilized a photon attenuation layer (PAL) that was deposited over the 3T pixels. The PAL is capable of down-converting high-energy incident X-ray photons and re-emitting them as low-energy photons, thereby significantly improving the image sensor's quantum efficiency (QE)."

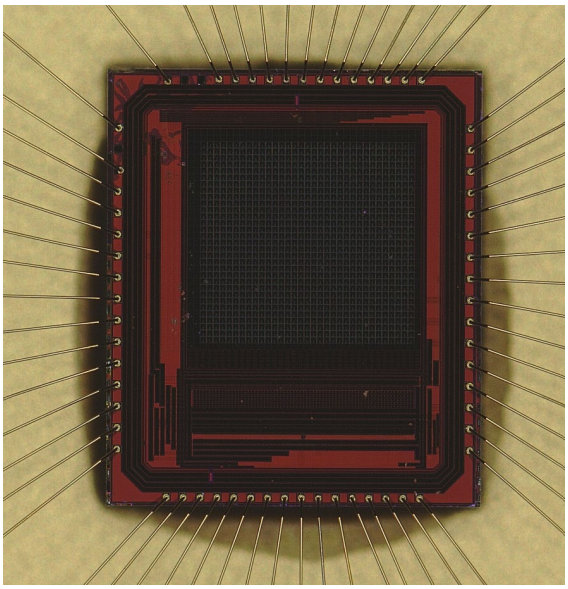


Figure 2-13 Image of the early-developed 500 fps 3T X-ray image sensor

In 1993, Dr. Fossum et al. introduced a CMOS active pixel image sensor (APS) with an in-pixel charge transfer transistor, commonly known as the 4T pixel, at JPL [108]. Figure 2-14 depicts the schematic of the 4T pixel, which consists of four transistors arranged from left to right: Transfer Transistor (TX), Reset Transistor (RST), Source Follower (SF), and Row-Select Transistor (RSEL).

During the pixel integration period, the RST and TX transistors are turned on to reset the floating diffusion (FD) to a high voltage, which also clears electrons from the photo-diode. Similar to the 3T pixel, electrons generated by photons are collected in the photodiode storage well (SW), while photon-generated holes are pushed away toward the substrate. Toward the end of the integration period, the RST gate resets the FD, and the column circuit samples the buffered FD voltage, referred to as V_{rst}. Subsequently, the TX gate turns on, transferring photoelectrons to the FD, and the column circuit samples the pixel output voltage, referred as V_{sig}. The 4T pixel operation timing is detailed in Figure 2-15. Notably, the FD reset voltage is sampled just before charge transfer, enabling

effective CDS operation and cancellation of FD kTC noise, which also reduces SF low-frequency noise.

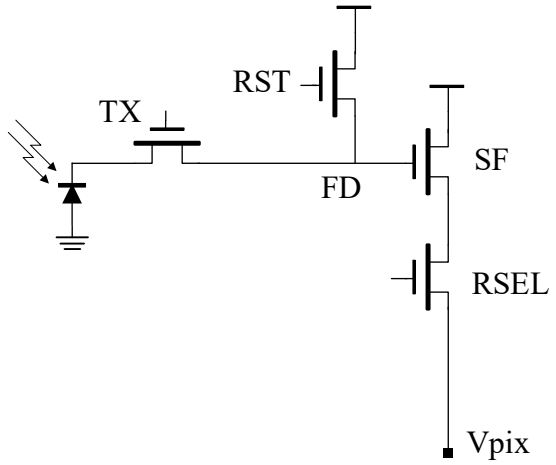


Figure 2-14 Schematic of a 4T CMOS pixel

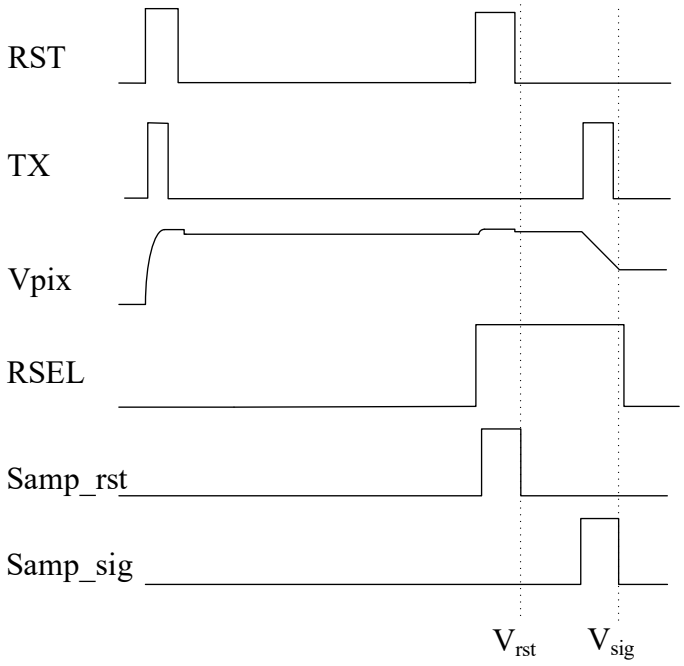


Figure 2-15 Timing diagram for a 4T CMOS pixel

Figure 2-16 displays an image of early-developed 78 Kfps 12T global shutter CMOS image sensor in the project based on a 180nm process. Each pixel of the sensor

includes two in-situ sample/hold capacitors, which store V_{sig} and V_{rst} in the voltage domain, as shown in Figure 2-17. Additionally, high-speed asynchronous SAR ADCs on the chip convert the difference between V_{rst} and V_{sig} into 10-bit digital codes with 2 extra bits for redundancy. Subsequently, high-speed serializers are used to serialize the digital codes and transmit them directly to an external device, such as an FPGA.

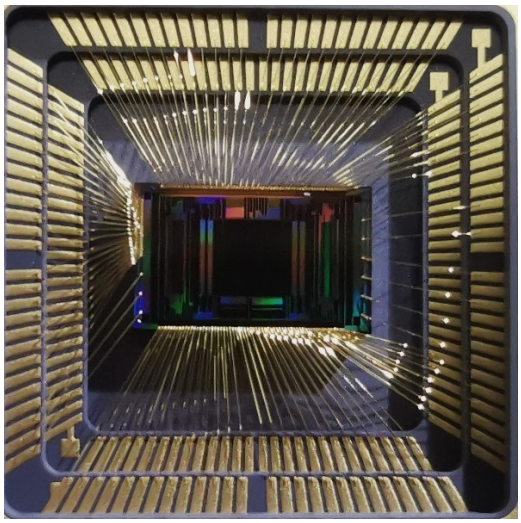


Figure 2-16 Image of the 78 Kfps global shutter CMOS image sensor

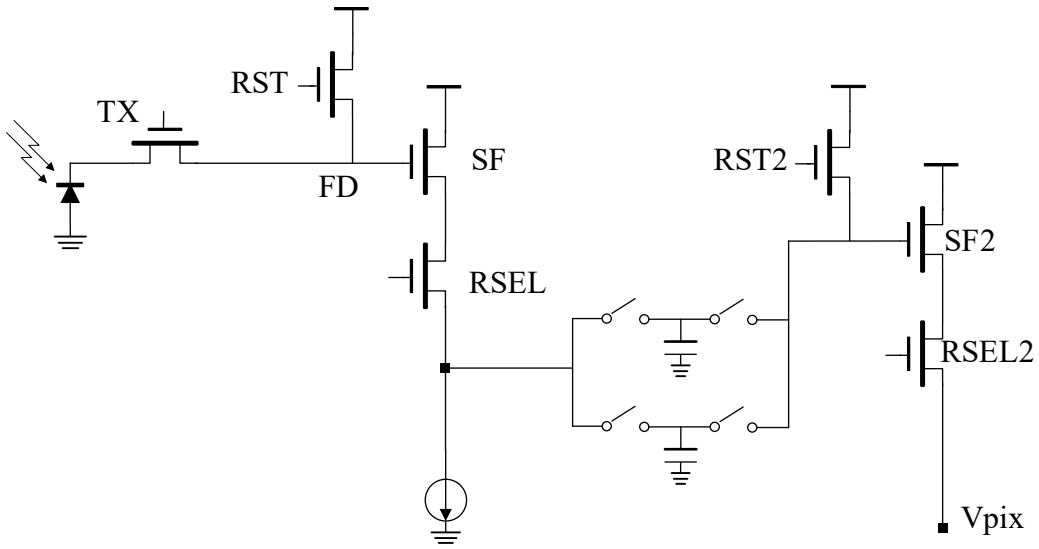


Figure 2-17 Schematic of the global shutter pixel in the 78 Kfps image sensor

Thanks to the low power consumption, and advanced high-speed CMOS technologies, CMOS solid-state image sensors have surpassed the performance of the CCD image sensors in terms of noise, pixel resolution, power consumption, and frame rate and dominate. As a result, they now dominate the solid-state image sensor market.

The relentless demand for higher image resolution keeps driving CMOS image sensor pixels to scale. Figure 2-18 from [19] shows CMOS image sensor pixel pitches and CMOS process nodes for published works in recent years. It clearly demonstrates that the CMOS image sensor pixel pitch is typically 10X to 20X larger than the CMOS process node. In 2022, Samsung and OmniVision even claimed the smallest camera pixels at 0.56um [76].

More technical challenges will arise with the smaller pixels. For example, the parasitic light crosstalk between adjacent pixels might be increased due to smaller spacing between adjacent pixels; Signal to noise ratio (SNR) might be reduced due to a smaller light-sensitive area in each pixel. More importantly, the image sensor resolution will eventually be limited by the optical lens due to the sub-diffraction limit. The smallest light point that a perfect lens can focus on due to diffraction-limit is known as an Airy disk. The Airy disk diameter DA [20] is given by the equation:

$$\mathrm{DA} = 2.44 \cdot \lambda \cdot \mathrm{F} \qquad (2-2)$$

where λ is the wavelength and F is the F-number of the optical system. For example, the latest iPhone 14 main camera has F-number to be 1.5 to 1.79, then the minimal spatial resolution of green light (550nm) is 2um.

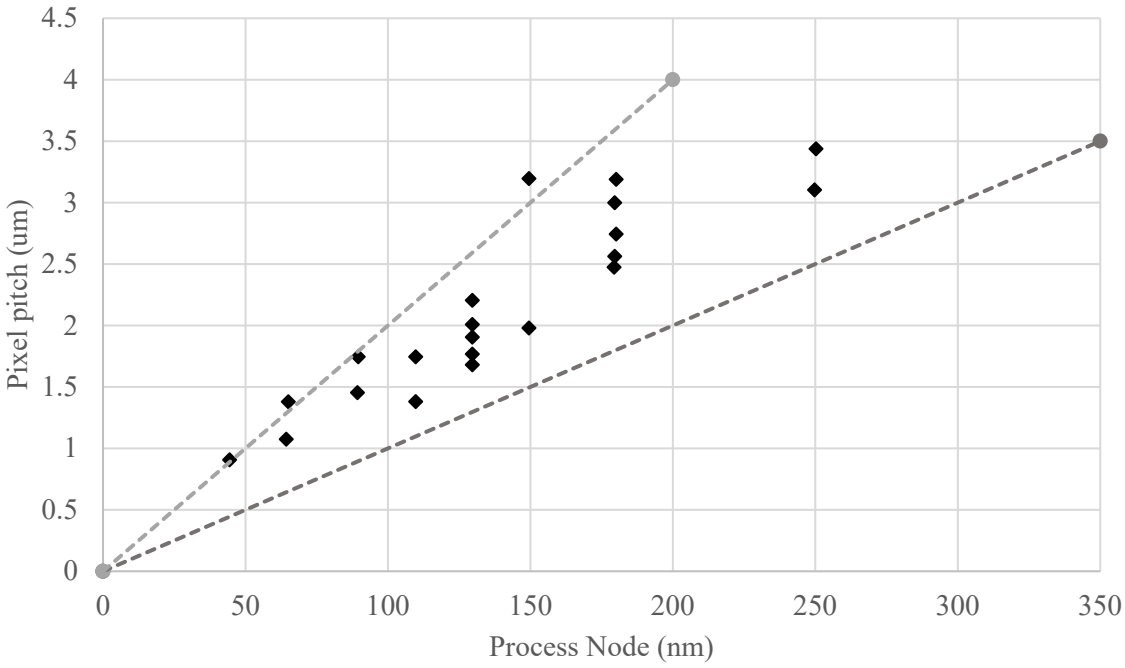


Figure 2-18 Pixel pitch (μm) versus CMOS process node (nm) plot

2.3 Quanta Image Sensor

In 2005, Dr. Eric. R. Fossum [20] [21] proposed the concept of a Quanta Image Sensor (QIS) as a potential next-generation CMOS solid-state image sensor with a sub-diffraction-limit (SDL). The basic idea is to oversample the image both spatially and temporally by single-photon-sensitive pixels within the Airy disk and reconstruct the image with a reconfigurable data cloud. This specialized pixel is called "Jot" as Figure 2-19 illustrates.

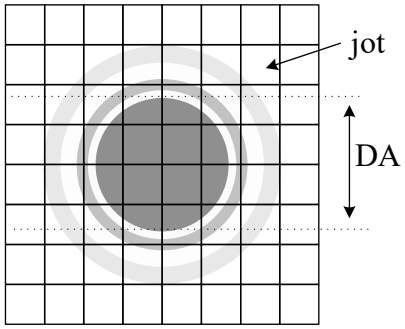


Figure 2-19 Conceptual schematic of QIS jot

In a QIS, each jot can be considered as a 1-bit photon ADC, with a digital output of "0" when no photon strikes occur and a "1" when they are present. Since jots are single-bit, the QIS can operate at high frame rates to prevent inaccuracies caused by multiple photons striking the same jot.

Unlike conventional CMOS image sensors with pre-fixed resolution and depth, the QIS enables reconfigurable resolution and depth. The QIS grain size can be adjusted to 2(jots) x 2(jots) x 1(frames), as shown in Figure 2-20(a), which corresponds to 2 bits in light intensity, with each LSB representing one photon. Alternatively, the grain size can also be configured as 4(jots) x 4(jots) x 4(frames), as in Figure 2-20(b), which equates to 6 bits in light intensity, with each LSB still representing one photon. In other words, the QIS allows for flexible trade-offs between image resolution, sensitivity, and frame rate, making it aptly named "digital film" [20]. The first QIS was introduced by Dr. J. Ma and Dr. Eric R. Fossum in 2015 at Dartmouth [22,97,98].

(a)

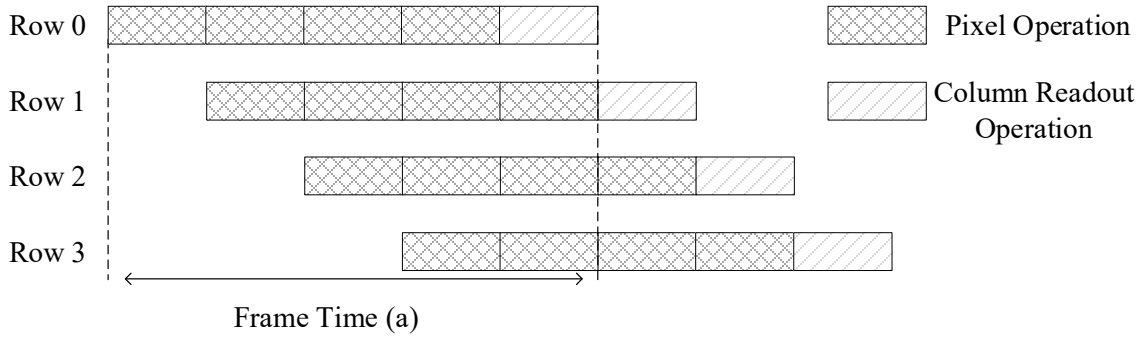
(b)

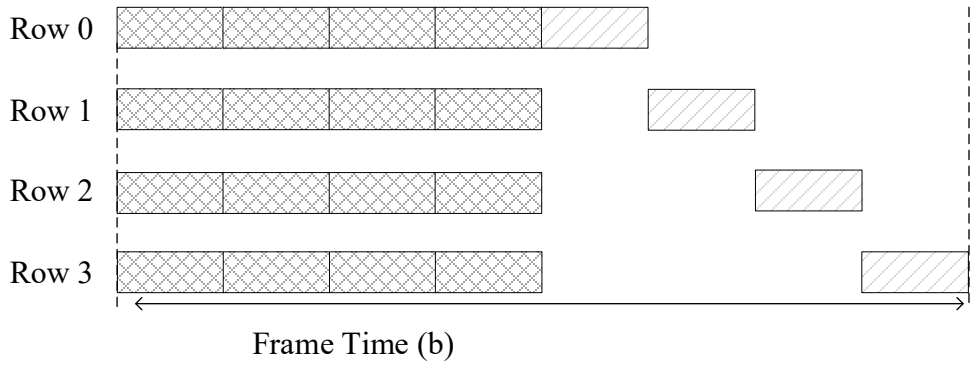
Figure 2-20 Image reconstructed using (a) 2x2x1 jot data, and (b) 4x4x4 jot data

3 Ultra-High-Speed Image Sensor

3.1 Overview

The frame rate of rolling shutter CMOS image sensors has been limited to tens to a few hundred frames per second (fps) since the introduction of active CMOS image sensors. Figure 3-1(a) illustrates the typical operation timing of a rolling shutter image sensor where each row of pixels initiates the integration of photo-generated electrons at different times, resulting in the rolling shutter artifact when capturing high-speed moving objects [23, 99]. To address this issue, [24] proposed global shutter image sensors, as shown in Figure 3-1(b), where all pixels in the frame simultaneously begin integrating electrons for the same duration.





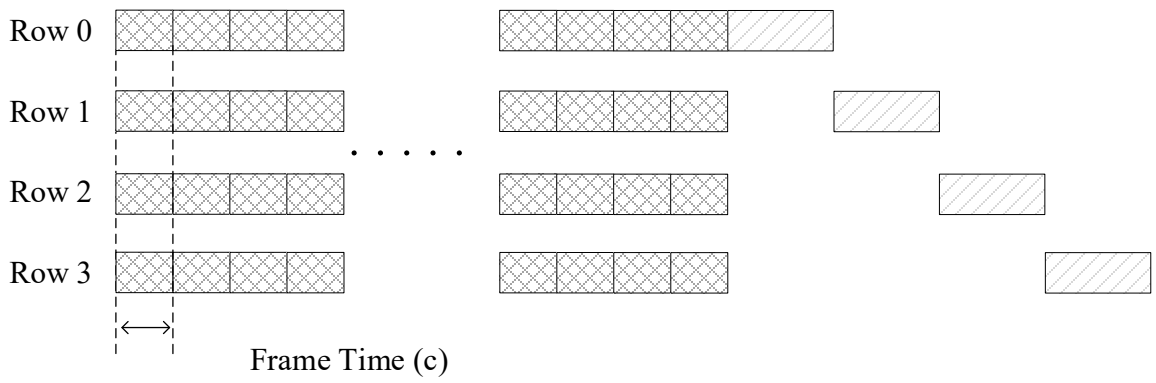


Figure 3-1 Operation timing diagrams of (a) rolling-shutter sensor, (b) global shutter sensor, and (c) global-shutter burst mode sensor

Figure 3-1 (a) and (b) demonstrate that both rolling and global shutter image sensors utilize on-chip readout circuits that continuously read pixel information and transmit data through high-speed data links. However, this column readout operation can ultimately limit the sensor frame rate. To address this limitation, a burst-mode image sensor can be utilized, as illustrated in Figure 3-1(c). This sensor operates by simultaneously and continuously sampling and storing incident photon information into on-chip memories. Once all on-chip memories are filled, the readout circuit reads out the stored images. Therefore, the frame rate is determined solely by the pixel operation. The following sections will provide a detailed analysis of each operation mode mentioned above.

3.2 Continuous-Mode Image Sensor

Figure 3-2 in [25] depicts the typical signal chain of a continuous-mode image sensor. The signal chain involves several steps: A) The photodiode collects the photon-generated electrons and transfers them to a sense node. B) An in-pixel amplifier samples the settled voltage at the sense node and buffers it out to the column bus. C) The column

bus delivers the voltage from the pixel array to the column readout circuit, which is usually located at the edge of the pixel array. D) The column circuit processes the voltage, either by amplifying or digitizing it. E) The output circuit delivers the processed signal to receivers through high-speed digital transmitters or high-speed analog buffers. Based on reference [25], Equation 3-1 outlines the typical processing and readout time required for the above-mentioned steps. In this equation, the symbol $t(A)$, $t(B)$, $t(C)$ $t(D)$, and $t(E)$ represent the time required for executing steps A, B, C, D, and E, respectively.

$$t(A) < \{t(B), t(C), t(D)\} \ll t(E) \qquad (3-1)$$

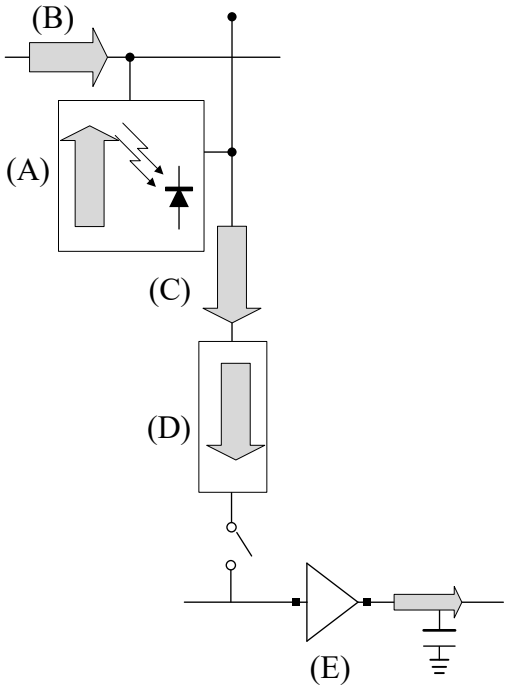


Figure 3-2 A typical signal chain for a continues-mode image sensor

For continuous model image sensors, the frame rate is typically limited by the speed of the output transmitter, as indicated by Equation 3-1. The transmitter can operate in either analog or digital format. Equation 3-2 provides a simple calculation for

determining the sensor frame rate in relation to the digital transmitter data rate. In this equation, F_{rate} represents the sensor frame rate, N represents the number of output data transmitters, D_{rate} represents the transmitter's data rate, Row represents the number of rows in the image array that need to be read out, Col represents the number of columns in the image array that need to be read out, and D represents the bit depth of the ADC.

$$F_{rate} = \frac{N \times D_{rate}}{Row \times Col \times D} \qquad (3-2)$$

For a modern 65nm CMOS process, a current-mode-logic (CML) based high-speed data transmitter can reliably operate around 6.4 Giga bits per second (Gbps) [100]. Assuming a 1000 (pixel) x1000 (pixel) sensor array and 10-bit ADC depth with one output port, the maximum frame rate will be limited to 640 frames per second (fps). Adding more output ports can definitely increase the frame rate, but with a reasonable power budget, continuous mode image sensors can hardly exceed 1 Mfps.

At the time of writing this thesis, one of the CMOS image sensors with the highest reported frame rate is [26], which operates at 80 kfps in continuous mode. Figure 3-3 depicts the block diagram of this chip, which is divided into 40 identical superblocks. Each superblock consists of a 64-column x 416-row pixel array, column readout circuitry, ADC, and output data transmitters. To achieve the 80 kfps frame rate, a total of 160 high speed data transmitters are integrated on the chip, with each transmitter operating at 6.25 Gbps. As a result, the sensor utilizes approximately 40 watts of power, with the majority of power consumption attributed to the data transmitters. The significant power consumption poses challenges in integrated circuit design, PCB design, and thermal management. Developing a functioning chip requires considerable engineering effort and time.

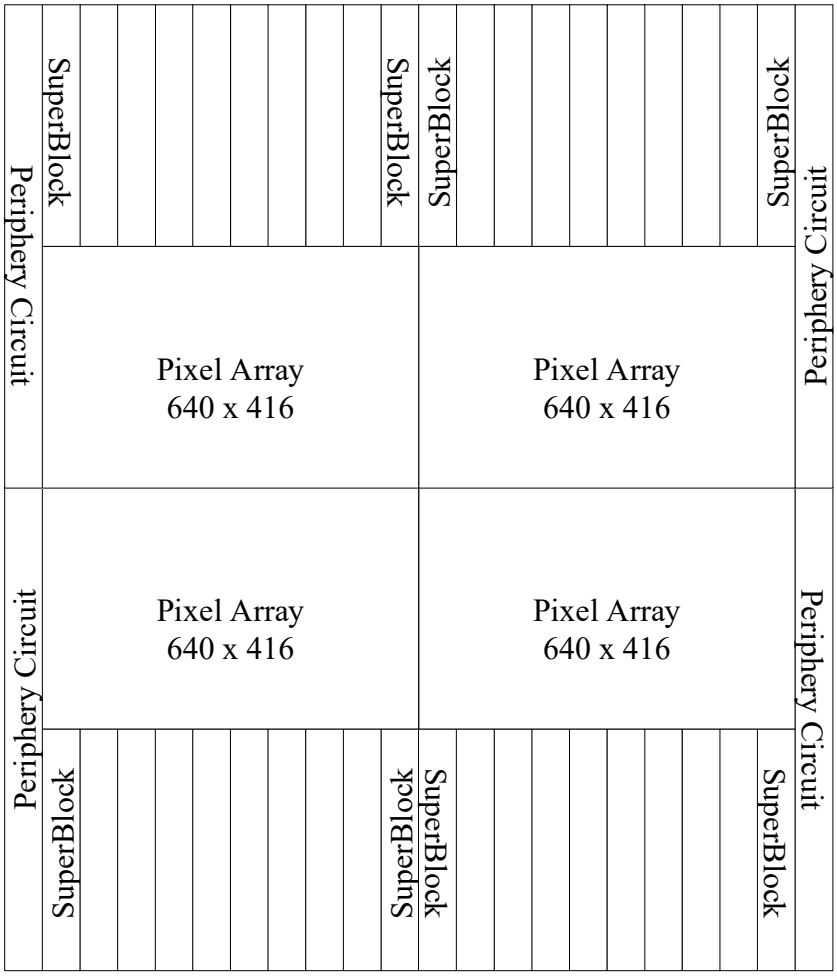


Figure 3-3 Block diagram of the 80 Kfps CMOS image sensor with 1M pixels, as described in [26].

In [28], a 4K resolution, 1 Kfps high-speed CMOS image sensor based on 3D stacked process is presented. Figure 3-4 depicts the block diagram of the image sensor, illustrating that the pixel array and ASIC readout circuitry are implemented on two distinct dies and connected through direct-bonding. This arrangement enables separate process optimization for the two dies. However, to accommodate the high frame rate, the bottom chip requires 48 output ports, each operating at 4.8Gbps, as indicated in the figure.

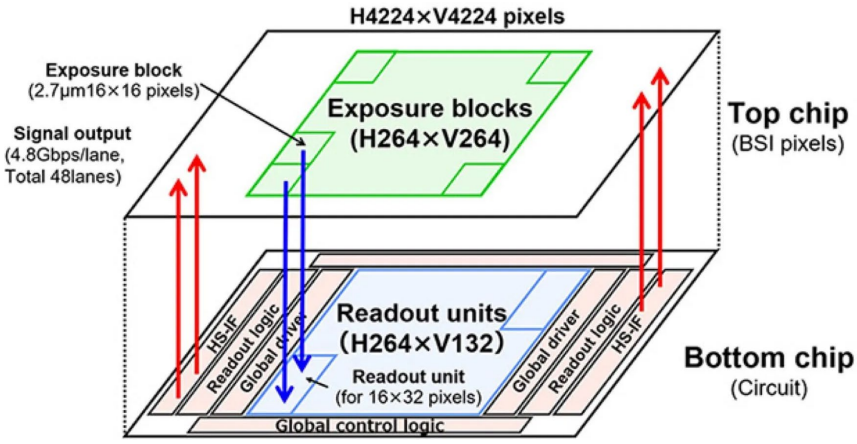


Figure 3-4 Block diagram of the 1 Kfps high-speed CMOS image sensor with 4K resolution, as described in [28]

3.3 Direct-Sampling Burst-Mode Image Sensor

The signal chain of a direct sampling burst mode image sensor is similar to that of a continuous mode image sensor and can be depicted in Figure 3-5.

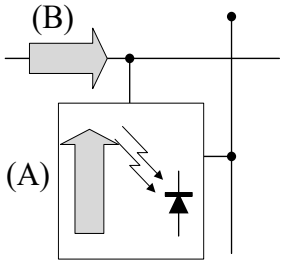
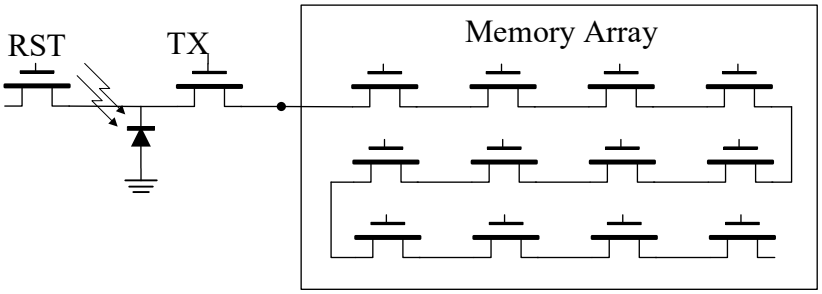
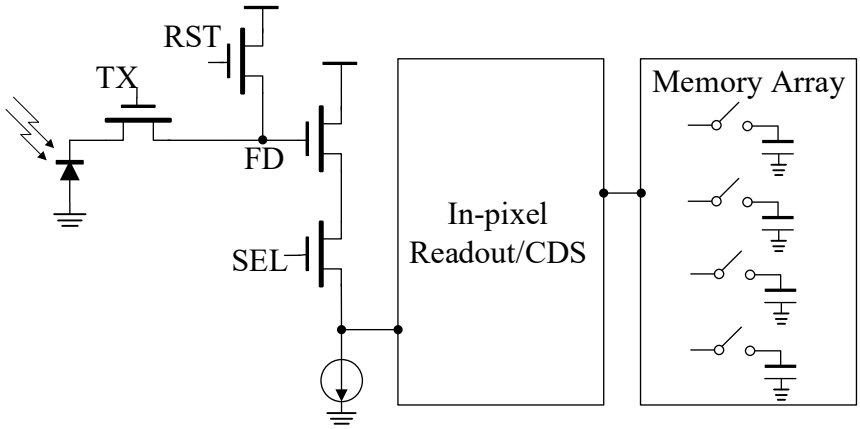


Figure 3-5 Signal chain for a burst-mode image sensor

Usually, the signal chain consists of either one step for charge domain storage or two steps for voltage domain storage. Initially, the photodiode collects photon-generated electrons and transfers them to the subsequent charge storage, as shown in Figure 3-6 (a). In the case of voltage domain storage, the electrons are transferred to a sense node, as depicted in Figure 3-6 (b). Afterward, the in-pixel buffer records the voltage of the sense node into a capacitor.



Charge domain storage (a)



Voltage domain storage (b)

Figure 3-6 Block diagrams of: (a) charge domain storage burst-mode image sensor and (b) voltage domain storage burst-mode image sensor

Since the in-pixel buffer is only required to drive local capacitors within the pixel, there is no need for a long column bus, as depicted in Figure 3-2. As a result, the settling time is reduced to a few nanoseconds and power consumption is also reduced. Hence, in burst mode image sensors, the frame rate is primarily determined by the speed of charge collection. It is widely recognized that charges can achieve higher velocity in a strong electric field, which will be discussed in detail in Chapter 4. In recent years, by engineering the in-pixel electric field, extremely fast burst mode image sensors have reportedly been developed.

According to [10], an upside-down pyramid-shaped electric field can be created within the pixel by combining multiple doping concentrations and multiple implantation energies. This electric field drives the photon-generated electrons toward the apex of the pyramid, where the transfer gate is located. By utilizing this pixel design, the imager can achieve an impressive frame rate of 25 Mfps. Furthermore, when implemented it in CCD process, the sensor can capture and store 1220 frames of information within each pixel. However, CCD cells typically suffer from high operation voltage and significant power dissipation, especially at high frame rates. Figure 3-7 illustrates the conceptual layout (left) and potential profile (right) of the pixel.

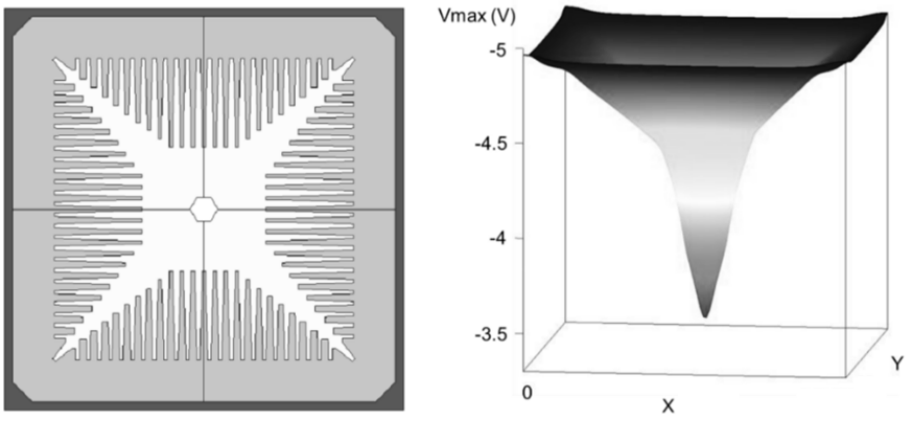


Figure 3-7 Conceptual layout (on the left) and electrostatic potential profile (on the right) of the pixel in [10]

The paper [7] presents a burst mode image sensor in the voltage domain, based on 180 nm CMOS technology. This sensor achieves a speed exceeding 100 Mfps by employing multi-doping concentration and a multi-finger shaped photodiode to establish an electric field of 500 V/cm in each pixel. Additionally, deep trench capacitors [27], commonly found in DRAM designs, are integrated into the pixel to enhance the sensor's recording length. With these capacitors, each pixel can store a maximum of 368 frames

within a 70 μm × 35 μm area. Figure 3-8 illustrates the conceptual layout of the pixel (on the left) and the cross-section of the deep trench capacitor (on the right) within the pixel.

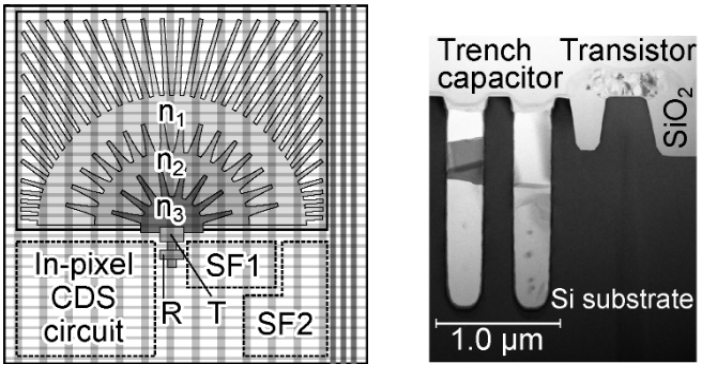


Figure 3-8 Conceptual layout of the pixel (on the left) and cross-section of the deep trench capacitor (on the right) in [7]

3.4 Compressive-Sampling Burst-Mode Image Sensor

In addition to direct-sampling image sensors that show dependence and redundancy between neighboring pixels, computational image sensors provide an alternative option. Figure 3-9 in [29] illustrates the concept of compressive-sampling ultra-high-speed burst-mode image sensors.

The entire image sensor comprises multiple sub-imagers, and the incident image is optically replicated by a lens array onto the apertures of these sub-imagers. The shutter of each sub-imager is coded to sample at different times. As a result, the photo-generated electrons are temporally modulated by the shutter pattern. After completing the sampling phase, the original time-resolved images can be reconstructed by demodulating the sampled image.

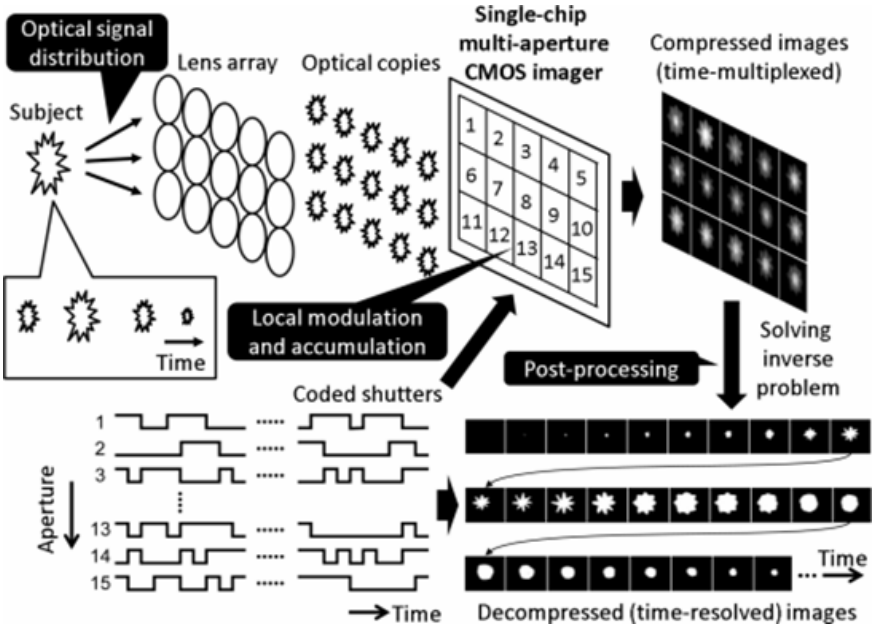


Figure 3-9 The overall flow of the compressive imager described in [29]

In the compressive-sampling burst-mode image sensor, the sensing node can also function as the frame storage. This means that the frame rate is determined solely by the speed of charge transfer from the photodiode to a single stage of the storage, as shown in Figure 3-10 with nodes FD1~FD4. This is in contrast to the charge transfer speed of multiple stages of storage in Figure 3-6 (a). The transfer speed in this mode can be extremely fast, reaching just a few nanoseconds.

Previous studies have demonstrated impressive results with compressive sampling. For example, [30] presented a 5x3 aperture compressive imager that achieved a frame rate of 200 Mfps. Similarly, [13] reported a frame rate of 303 Mfps using compressive-sampling. However, the number of frames that can be recorded is typically limited to a few due to physical implementation constraints.

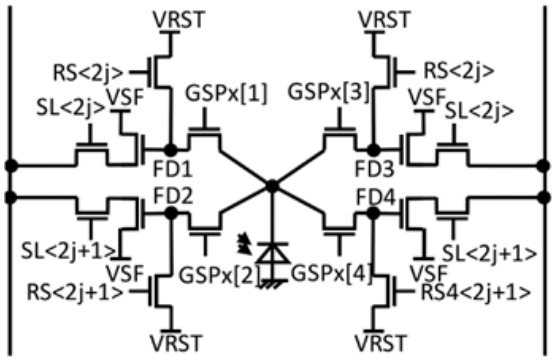


Figure 3-10 Schematic of the pixel based on floating diffusion storage, as reported in [13]

4 High-Speed Pixel Design

4.1 Overview

It is widely known that there are two main mechanisms for transporting carriers in semiconductors [31]: diffusion current, which is caused by concentration gradient, and drifting current, which is due to the electric field.

Equation 4-1 [31] describes the diffusion current density, where q represents elementary charge, D_n is the diffusion constant, and Q_n is the carrier distribution as a function of place (x) and time (t). When combined with equation 4-2, equation 4-3 [31] can be obtained, which describes the time required to transport $Q_n(0)$ over a distance L, where $Q_n(0)$ represents the total charges at $t = 0$, L represents the distance, and t represents the time. For instance, suppose that 1000 electrons need to be transported by 8.5 μm due to diffusion current. In that case, it would take 49 *ns* to achieve 99% charge transfer efficiency (CTE) and 75 *ns* to achieve 99.9% CTE by calculation, which is too slow for this project.

$$J_{diff} = q \cdot D_n \cdot \frac{\partial Q_n(x \cdot t)}{\partial x} \qquad (4-1)$$

$$\frac{\partial Q_n(x \cdot t)}{\partial t} = \frac{\partial J_{diff}(x \cdot t)}{\partial x} \qquad (4-2)$$

$$Q_n(t) = \frac{8}{\pi^2} \cdot Q_n(0) \cdot e^{-\frac{\pi^2 \cdot Dn \cdot t}{4L^2}} \qquad (4-3)$$

Equation 4-4 [31] describes the drifting current density, where Q_n also denotes the carrier distribution, u_n stands for the carrier mobility, and E denotes the electrical field. When combined with Equation 4-5, Equation 4-6 [31] can be derived, which describes the time needed to transport $Q_n(0)$ over a distance L within electric field. For

example, suppose that 1000 electrons need to be transported by 8.5um due to 800 *V/cm* electric field. In such a case, the calculation shows that it would take 1.06 ns, which is significantly faster than in the previous scenario. This demonstrates that, for high-speed pixel design, a strong electric field is necessary to facilitate the quick transfer of electrons.

$$J_{drift} = Q_n(x \cdot t) \cdot u_n \cdot E \qquad (4-4)$$

$$\frac{\partial Q_n(x \cdot t)}{\partial t} = \frac{\partial J_{drift}(x \cdot t)}{\partial x} \qquad (4-5)$$

$$Q_n(t) = \frac{Q_n(0)}{L} \cdot u_n \cdot E \cdot t \qquad (4-6)$$

The upcoming section in this chapter will discuss the method of implementing a strong electric field and optimizing other pixel specifications.

4.2 Charge Transfer Time

4.2.1 Charge Transfer Time Analysis

In modern pinned photo diodes (PPD) [18], the p+ layer deposited on top of the n region plays a crucial role in pinning the surface potential and reducing dark current, depleting the free electrons in the photodiode, and reducing image lag. As pointed out analytically by [32,33,35], the pinned voltage can be modulated by the photodiode width for small-size pixels due to the short-photodiode effect.

Figure 4-1 (a) depicts a simplified cross-section of a pinned-photodiode, where *n* represents the doping concentration of the photodiode. When considering 3D photodiode effects, for a fully depleted n-region, the electrostatic potential along the red-dashed line can be plotted in Figure 4-1 (b). This potential is described by Equation 4-7 [34], which

provides a simplified relationship between the maximum electrostatic potential (ψ_{max}) in the photodiode, the elementary charge (q), the doping concentration of the photodiode (N_D), the doping concentration of the substrate (N_A), and the photodiode half-width (X_n).

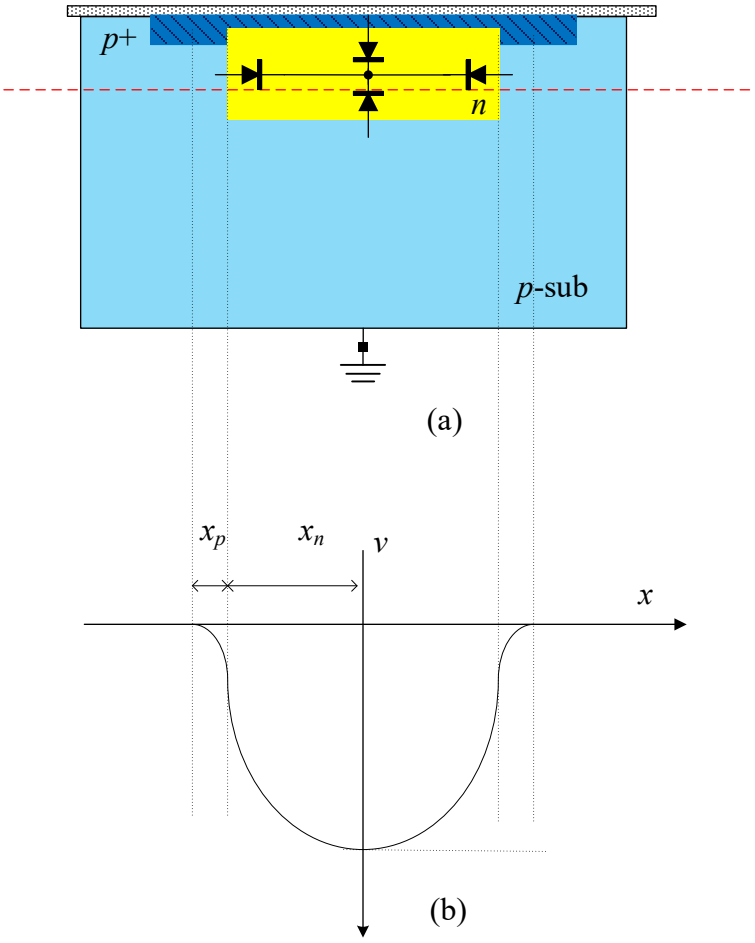


Figure 4-1 (a) Cross-section of PPD and (b) its electrostatic potential along the red-dashed line

$$\psi_{max} \approx \frac{q.N_D.\boldsymbol{X_n^2}}{2.\varepsilon_0.\varepsilon_r}\left(1+\frac{N_D}{N_A}\right) \qquad (4-7)$$

A more sophisticated 2D model, which considers the effects of all four PN junctions in a pinned photodiode, can be found in [35]. However, for quick analysis of the electric field, the simplified 1D model is sufficient. By adjusting the width of the

photodiode, it is possible to establish a constant and strong electric field within the photodiode, as shown in Equation 4-8. In this equation, *x* and *y* represent the coordinates of the photodiode's envelope, *E* represents the constant electric field, and C_0 is a constant.

$$y = -\frac{q \cdot N_D \cdot x^2}{2 \cdot E \cdot \varepsilon_0 \cdot \varepsilon_r}\left(1 + \frac{N_D}{N_A}\right) + C_0 \qquad (4-8)$$

Based on the design requirements, a pixel pitch of approximately 20 µm is preferred. When the transfer gate is placed at the center of the pixel, the longest electron transfer distance is about14 µm, as illustrated in the black dashed line in Figure 4-2.

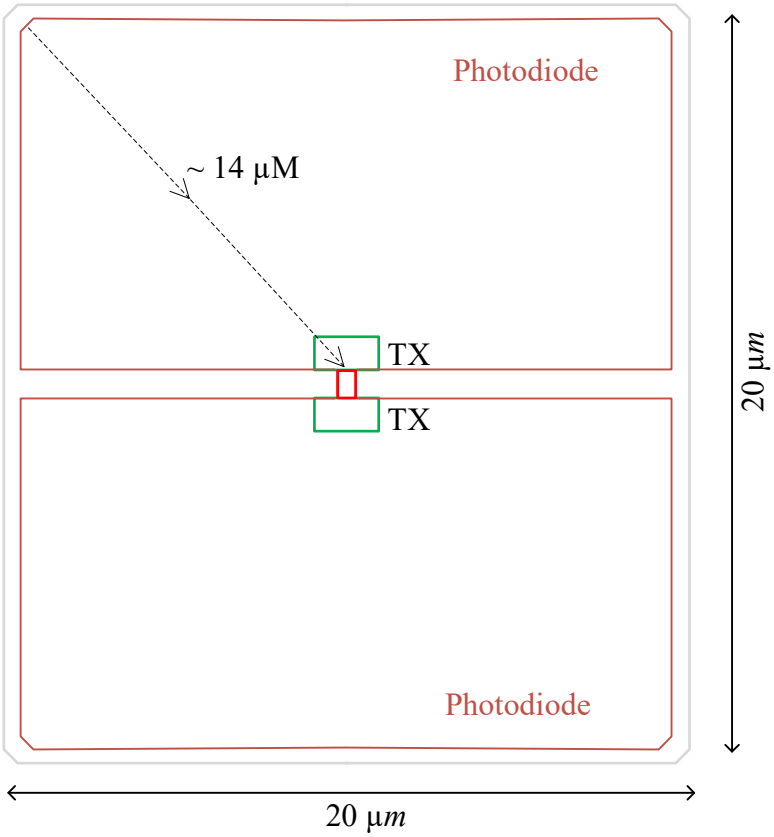


Figure 4-2 The longest electron transfer distance in the sample pixel

Assuming a medium doping concentration at room temperature and an electron mobility of 1500 cm^2/Vs [36], and with a charge transfer time not exceeding 2.5 ns, the

constant electrical field is calculated to be > 370 V/cm. To account for process variation and the possibility of high dark currents resulting from strong electrical fields [37], the electric field in the photodiode along the charge transfer direction varies between 400 V/cm to 900 V/cm. Consequently, different photodiode geometry shapes, labeled E400 to E900, can be obtained, as shown in Figure 4-3.

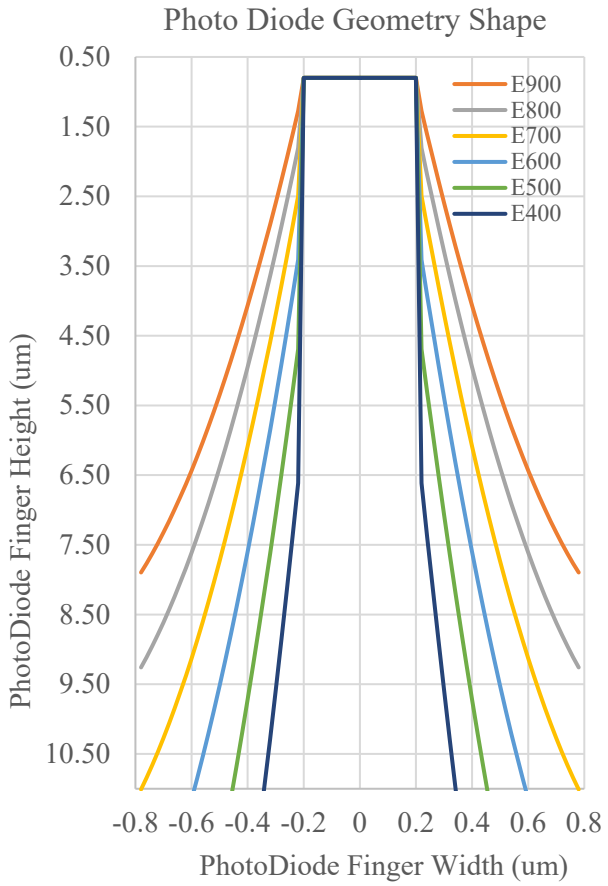


Figure 4-3 Photodiode finger shapes with different electric fields

4.2.2 Charge Transfer Time Simulation

Figure 4-4 presents a conceptual pixel layout based on the E900 photodiode shown in Figure 4-3. By calculations, the photodiode will have a built-in electric field of 900 V/cm. For simulation simplicity, this sample pixel model includes only the

photodiode (PD), transfer gate (TX), floating diffusion (FD), reset gate (RST), and reset drain (VDD).

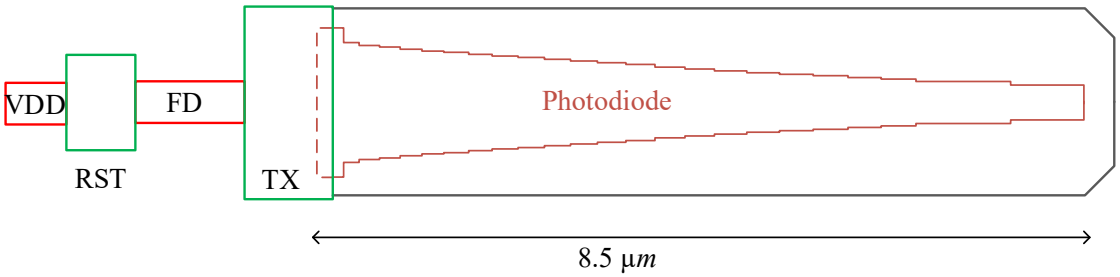


Figure 4-4 Conceptual layout of a pixel with built-in 900 *V/cm* electric filed

The left side of Figure 4-5 presents the 3D Technology Computer-Aided Design (TCAD) model based on the pixel layout mentioned above. It shows the TX, FD, RST, and VDD electrodes, but the buried photodiode in the epi layer is not visible in this figure. To ensure that only the tip of the photodiode is illuminated, this 3D pixel model includes a light shield consisting of two metal layers over the photodiode, creating a small aperture. This design directs all the photo-generated electrons to follow the longest path from the photodiode to the FD once the TX gate is turned on. On the right side of Figure 4-5, a cross-section along the grey cut plane is displayed, where the yellow region represents the *n* region of the photodiode. Although the shape of the photodiode may appear triangular, its two longer sides follow the parabolic relationship expressed in Equation 4-8.

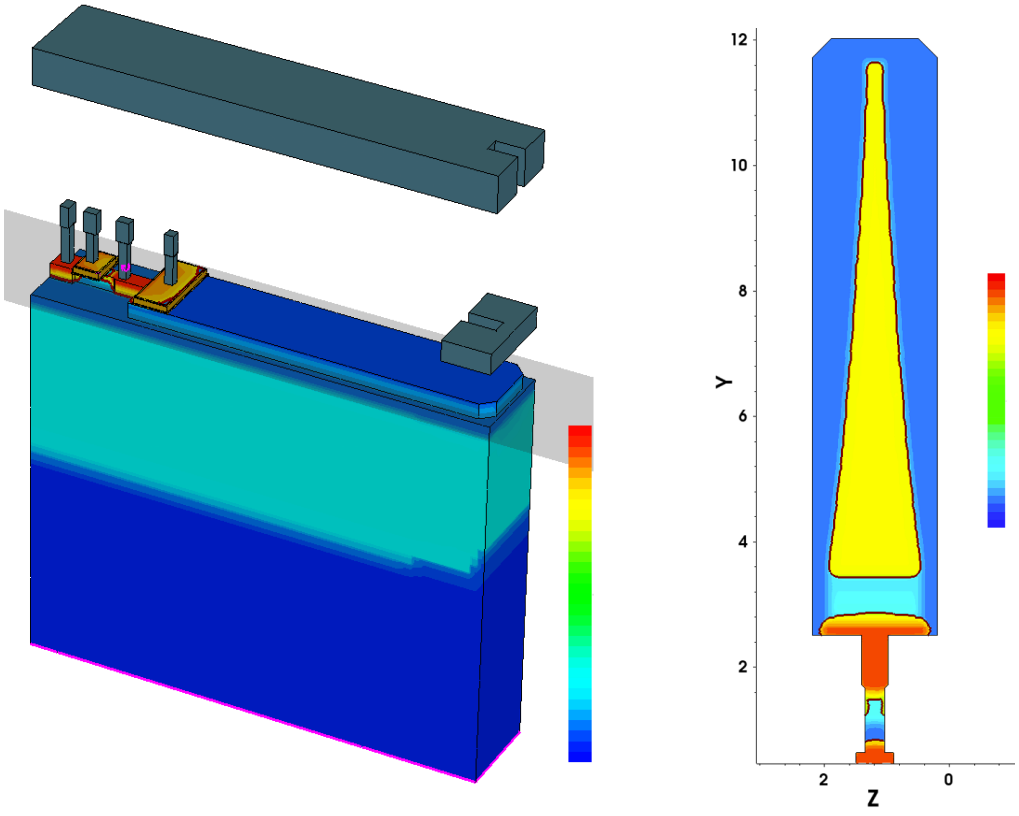


Figure 4-5 3D TCAD model of the sample pixel (on the left) and its cross-section along the cut-plane (on the right)

Figure 4-6 illustrates the electrostatic potentials along the charge transfer path for various photodiode designs. The electrostatic potential diagram indicates a monotonically increasing trend in each design, and importantly, highlights the establishment of a strong electrical field in the E600, E700, E800, and E900 designs.

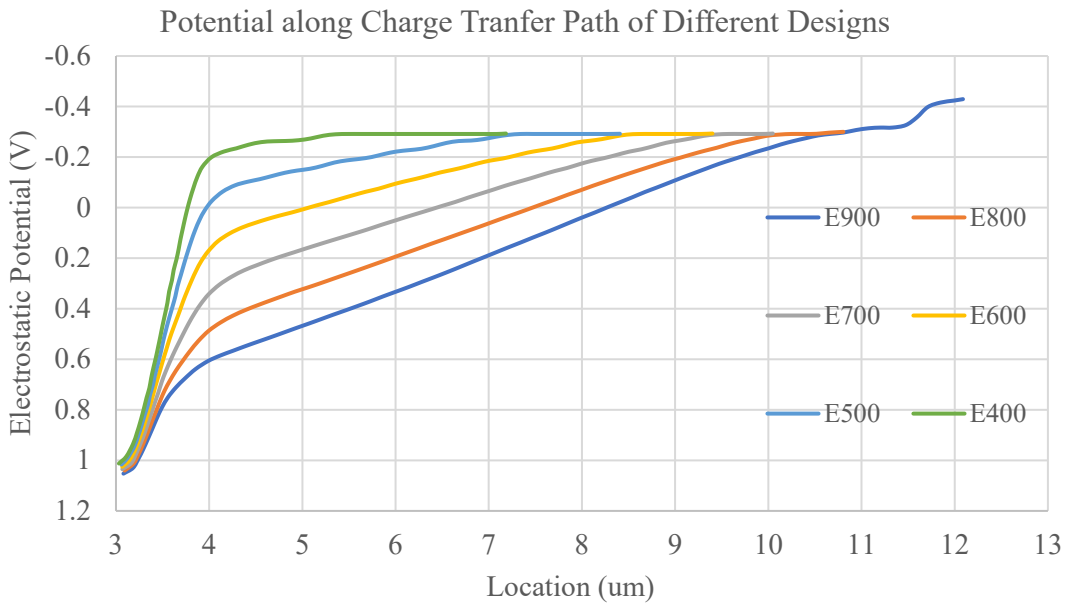


Figure 4-6 Electrostatic potential plots along charge transfer path for various photodiode designs

The TCAD transient simulation was used to measure the charge transfer time in the designs. Figure 4-7 presents the simulation results for E900 design where the orange curve represents the total number of electrons collected in the photodiode, the blue curve stands for the TX gate voltage, and the grey curve represents the light pulse. In this simulation, the light pulse illuminated the tip of the photodiode figure from 20 ns to 50 ns, as shown by the grey curve. A total of 40 *e-* were collected in the photodiode when light is on. At 50 ns, the light turned off and the TX gate turned on, causing electrons to rapidly move out of the photodiode and into the floating diffusion, thereby quickly reducing the number of electrons in the photodiode to less than 1. The simulation results indicate that it takes 1.3 ns to achieve 1% charge transfer inefficiency (CTI) and 13.6 ns to achieve 0.1% CTI. CTI is defined as the number of remaining charges over the total number of charges required to be transferred.

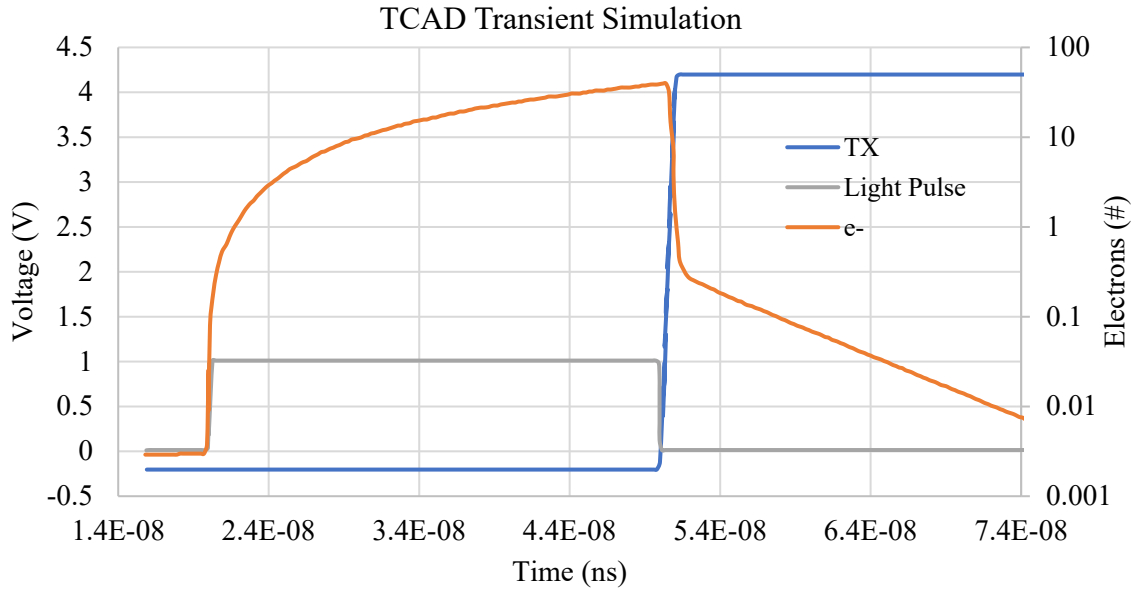


Figure 4-7 TCAD transient simulation result of the sample pixel (E900)

To determine the optimal design for the photodiode, simulations were conducted in TCAD to evaluate the charge transfer time for all six designs. The resulting data can be found in Table 4-1. For this application, a CTI of 0.5% was selected as the criterion for image lag performance. The system level requirements, which will be discussed in Chapter 5, dictate that the TX pulse width should not exceed 10 ns. Consequently, only the E700, E800, and E900 designs meet this requirement. Considering factors such as dark current, fill-factor, and process variation, the E800 design is ultimately chosen as the high-speed photodiode design for the remainder of this thesis.

Charge Transfer Time of Different Designs					
CTI	10%	1%	0.50%	0.10%	unit
E400	10.2	41.2	51.3	75.2	ns
E500	0.6	17.4	25.8	47.0	ns
E600	0.6	5.0	11.0	28.3	ns
E700	0.7	1.5	**5.1**	19.3	ns
E800	0.8	1.1	**3.7**	15.5	ns
E900	0.9	1.3	**3.6**	13.6	ns

Table 4-1 Charge transfer time of different photo diode designs

4.2.3 Pixel Variant 1

Several high-speed prototype pixels were simulated and measured, as shown in Figure 4-8 by research [38]. The research indicates that all the pixels feature a triangular-shaped finger and a built-in electric field to enhance the charge transfer process. Design (c) exhibits superior image lag performance compared to the other two designs with the same pixel size, owing to its shorter charge transfer path length. Inspired by this finding, the conceptual layout for variant 1 high-speed pixel design in this project is presented in Figure 4-9.

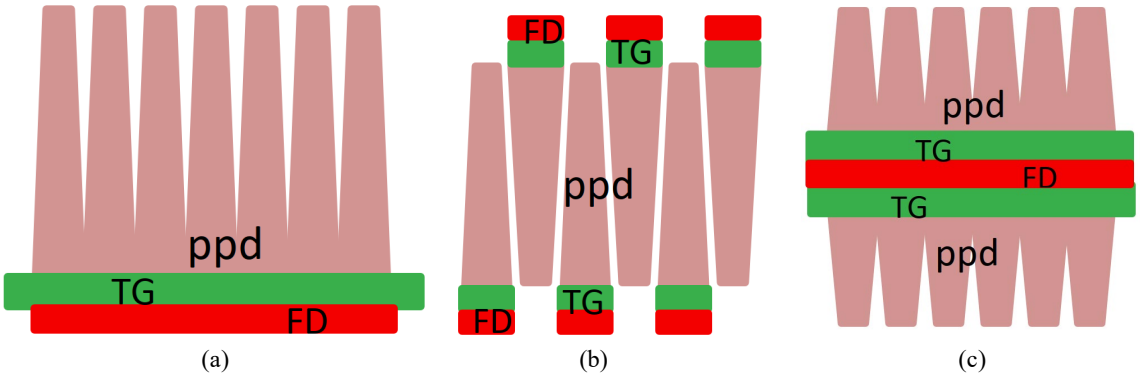


Figure 4-8 Highspeed prototype pixels, as reported in [38]

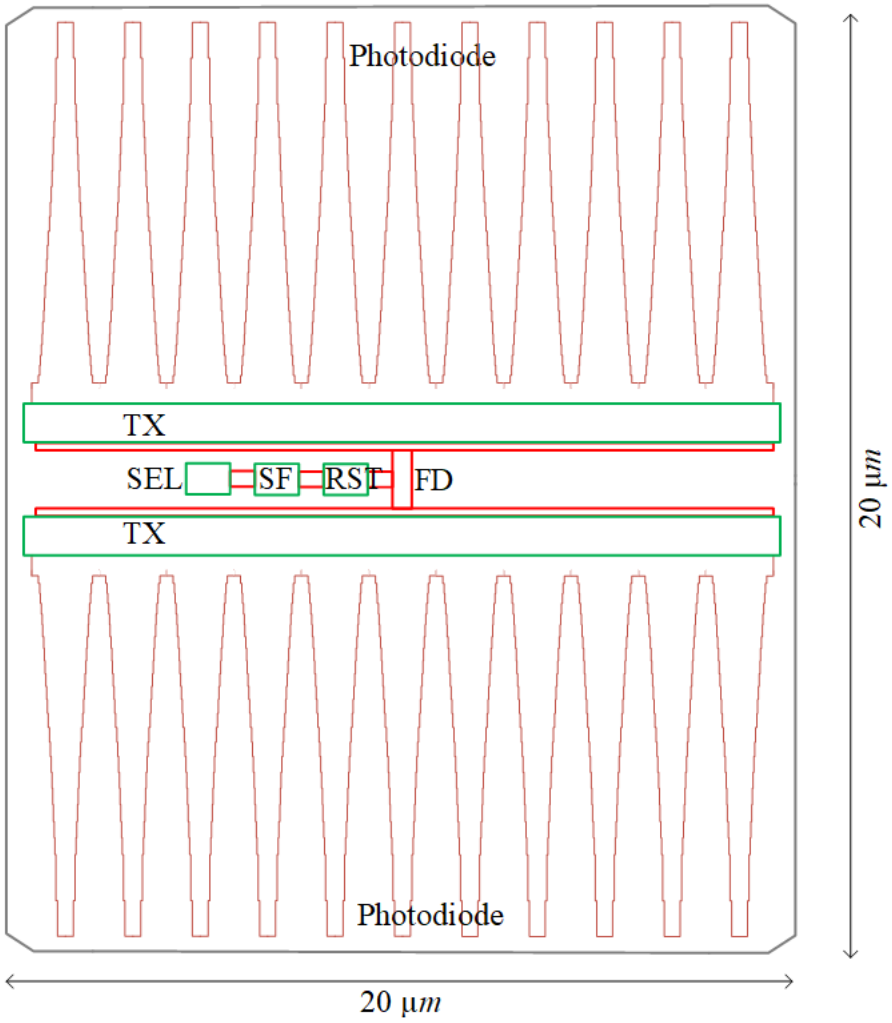


Figure 4-9 Conceptual layout of variant 1 high-speed pixel

To accurately simulate the behavior of the pixel, Figure 4-9 presents a comprehensive layout of the 4T variant 1 pixel. In the figure, the transfer gate is labeled as TX, the selection gate as SEL, the source follower gate as SF, the reset gate as RST, and the floating diffusion as FD.

4.2.4 TCAD Simulation of Pixel Variant 1

To simulate the device, variant 1 pixel is modeled in TCAD, as the 3D model shown in Figure 4-10. For clarity, the silicon dioxide (SiO_2) that fully covers the pixel is not displayed. But TX, RST, SF, SEL, and their respective metal connections are visible.

The top layer metal is utilized as a shield to fully cover the floating diffusion, ensuring it remains insensitive to incident photons.

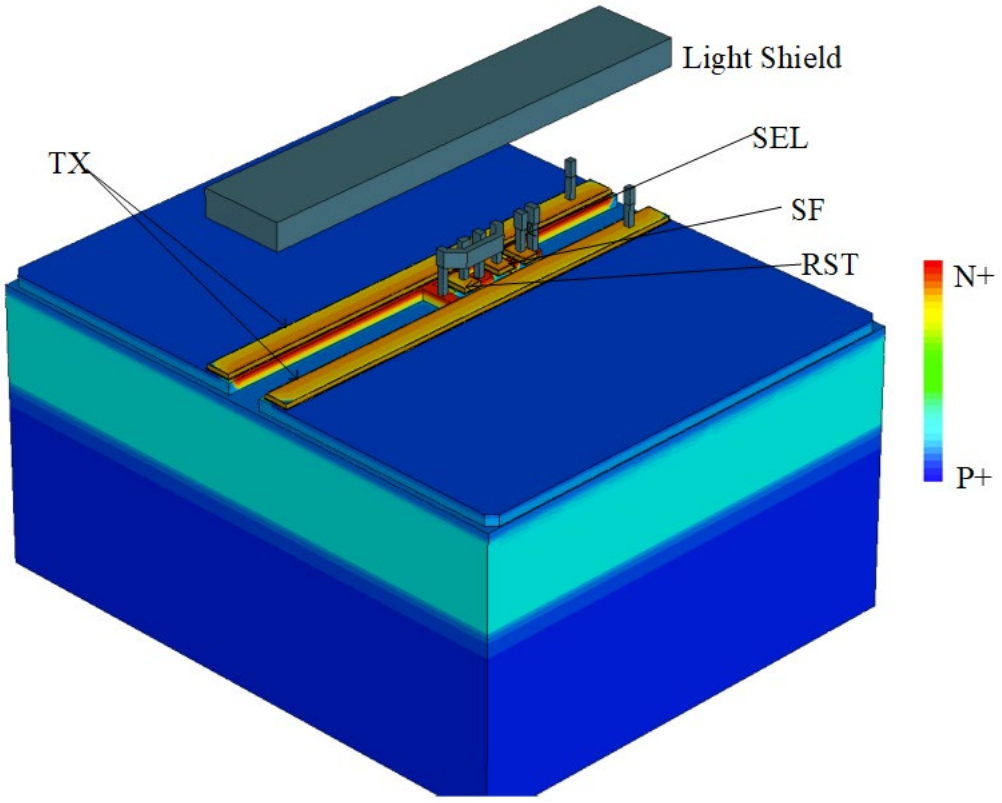


Figure 4-10 3D TCAD model of the variant 1 pixel

Figure 4-11 depicts the electrostatic potential of the cut plane beneath the epi surface by about 200nm when the TX gate is on. The figure illustrates a gradual rise in the electrostatic potential along the charge transfer path (highlighted in red dash line), with no noticeable potential barrier or pocket present.

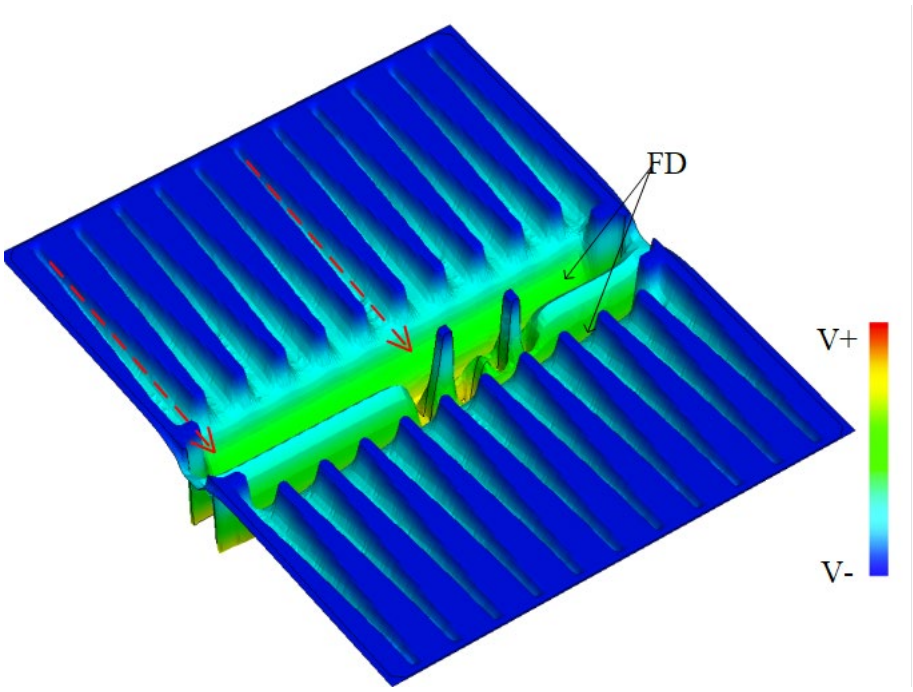


Figure 4-11 Electrostatic potential surface plot of variant 1 pixel

To verify the charge transfer time and conversion gain of the design, a TCAD transient simulation was conducted. Figure 4-12 presents the simulation result, wherein the TX gate is pulsed on from 100 ns to 108 ns, as indicated by the red curve. It is evident that the total number of electrons in the upper (eTotal1) and lower (eTotal2) photodiode rapidly decreases from over 300 electrons to less than 1 electron within 6 ns. The simulation result confirms that complete charge transfer is achieved within 6 ns, which closely aligns with the theoretical analysis presented in the previous chapter.

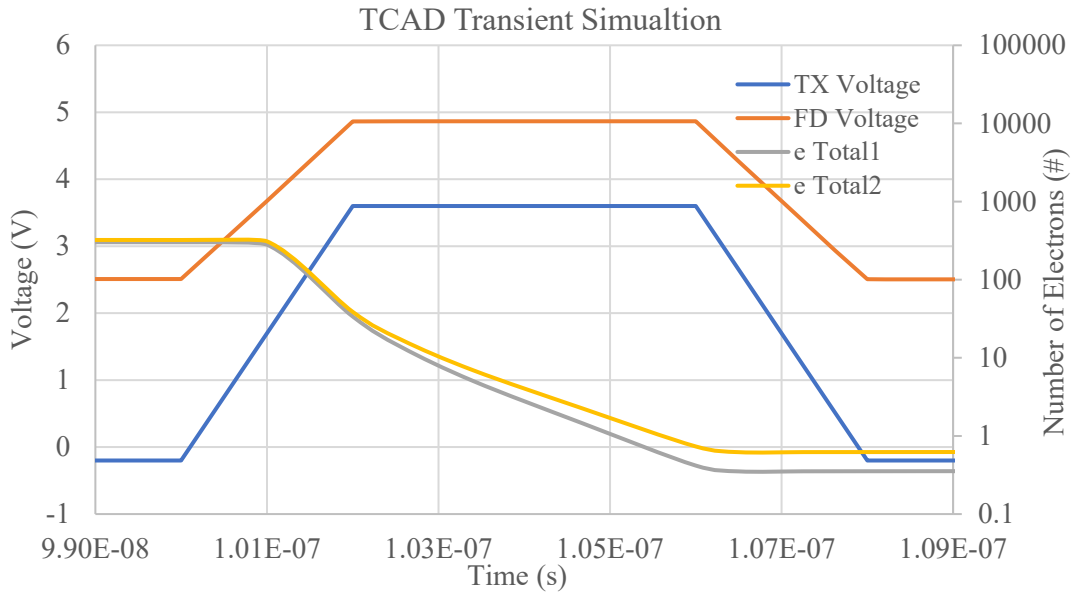


Figure 4-12 TCAD transient simulation result of variant 1 pixel

The conversion gain (CG) of a pixel is defined as the voltage change at the floating diffusion node (ΔV_{FD}) before and after charge transfer, divided by the total number of charges transferred (Δe). Equation 4-9 shows this calculation.

$$CG = \frac{\Delta V_{FD}}{\Delta e} \qquad (4-9)$$

The CG value of variant 1 pixel is found to be only 7.9 uV/e-. However, as will be discussed in the system-level analysis in Chapter 5, this conversion gain value is too small to be useful. Therefore, the upcoming sections will focus on improving the CG of the high-speed pixel.

4.3 Conversion Gain

4.3.1 Conversion Gain Analysis

Equation 4-9 provides the definition of pixel conversion gain, while Equation 4-10 shows its calculation. Here, q represents the elementary charge, and C_{total} represents

the total capacitance lumped at the FD node. As observed, the CG tends to be small with a higher capacitance at the FD node.

$$CG = \frac{q}{C_{total}} \qquad (4-10)$$

Figure 4-13 illustrates the distribution of capacitance associated with the FD node in a typical 4T pixel. In this figure, C_{TX_FD} represents the overlap capacitance from the TX gate to the FD node, C_{RST_FD} represents the overlap capacitance from the RST gate to the FD node, and C_{FD_GND} stands for the total lumped capacitance from the FD node to ground, which includes the FD node PN junction capacitance, the TX transistor drain to ground capacitance, and the RST transistor source to ground capacitance. Moreover, C_{SFD_FD} represents the source follower gate to drain capacitance, while C_{SFS_FD} represents the source follower gate to source capacitance. The Miller Effect [109, 110] is taken into consideration.

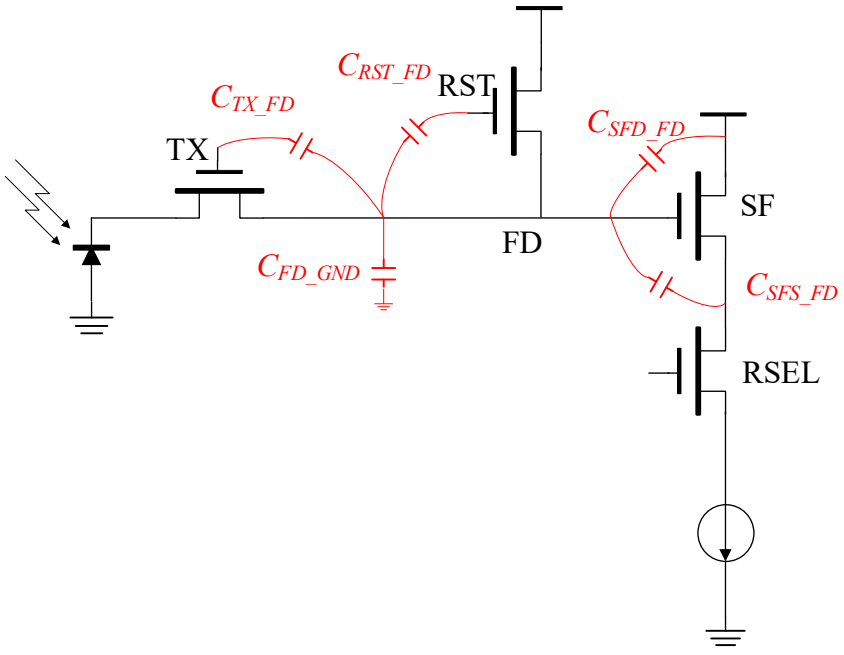


Figure 4-13 FD node capacitance distribution of a typical 4T pixel

Equation 4-11 [41] provides a detailed calculation of C_{total}, where A_{SF} stands for the low frequency gain of pixel source follower. In the current *p*-type substrate process, the bodies of NMOS transistors are directly connected to the *p*-type substrate. This connection results in the body-effect regulating the SF threshold voltage of sub-micron NMOS transistors, unless a deep n-well (DNW) process [43] or a Silicon-On-Insulator (SOI) process [42] is used. Consequently, the DC gain of source follower in pixel is usually around 0.7 ~ 0.8 V/V.

$$C_{total} = C_{TX\_FD} + C_{RST\_FD} + C_{FD\_GND} + C_{SFD\_FD} + C_{SFS\_FD} \times (1 - A_{SF}) \quad (4-11)$$

4.3.2 Conversion Gain Optimization and Pixel Variant 2

By observing the variant 1 pixel layout, it becomes apparent that the width of the TX gate is similar to the pixel pitch [35, 38, 39, 40]. Consequently, the TX gate width is as large as 20 μm. This, in turn, leads to the dominance of the large capacitance of C_{TX_FD} (TX gate to FD) and C_{FD_GND} (FD to ground) in the total capacitance C_total. Although the double photodiode design reduces the length of the charge transfer path, it also doubles the capacitance of C_{TX_FD}, resulting in a worse conversion gain. Therefore, optimizing the TX gate structure is necessary to achieve a higher conversion gain.

Figure 4-14 illustrates the conceptual layout for variant 2 of the high-speed pixel design, which introduces the charge sweep transfer gates, inspired by the concept of CCD in CMOS [113, 114, 115, 116, 117] and charge sweep device [118].

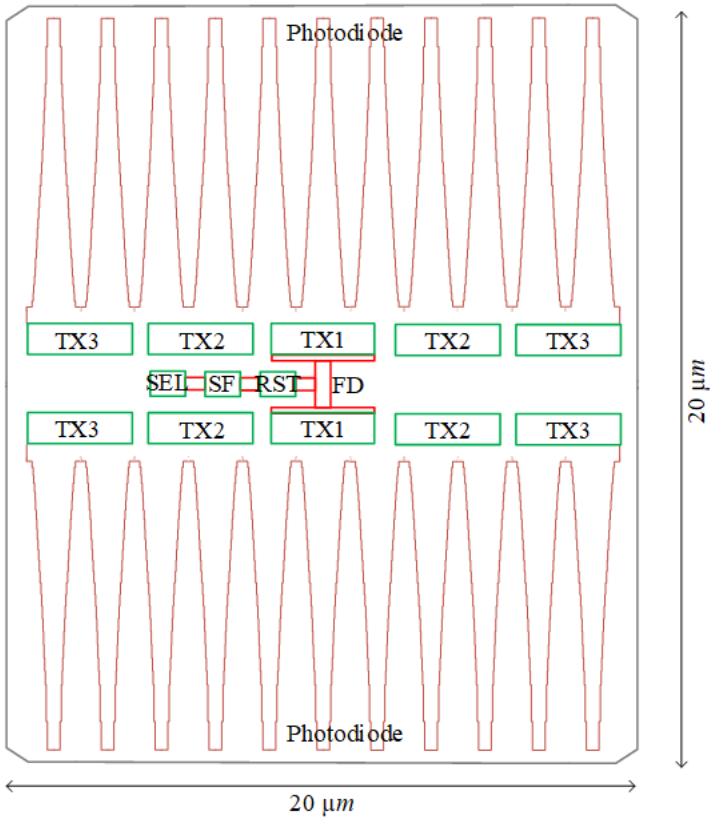


Figure 4-14 Conceptual layout of variant 2 high-speed pixel

The new design presented here differs from the traditional transfer gate in Figure 4-9. Instead of a single long transfer gate, the new design utilizes multiple smaller gates, namely TX3, TX2, and TX1. It is easy to observe that the C_{TX_FD} is reduced to about 1/5 of the previous design due to the smaller size of the transfer gate. Simultaneously, the C_{FD_GND} is also greatly reduced, due to smaller FD area, as highlighted in red boxes in Figure 4-14.

Figure 4-15 depicts the timing of the three transfer gates. At the beginning of the charger transfer phase, TX1, TX2, and TX3 are all turned on simultaneously, with TX1's voltage being higher than that of TX2, and TX2's voltage being higher than that of TX3. At the end of the charger transfer, TX3 gate turns off first, followed by TX2 and

eventually TX1. This sequential process effectively pushes electrons from TX3 to TX2, and ultimately to FD. In the simulation setup, the longest duration of the TX pulse is maintained at 12 ns.

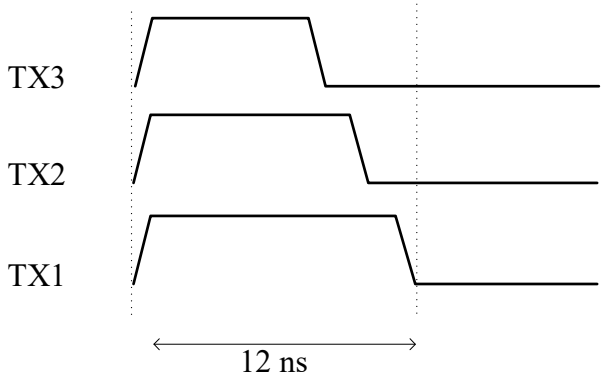


Figure 4-15 Charge sweep transfer gate timing

4.3.3 TCAD Simulation of Pixel Variant 2

To simulate the device, variant 2 pixel is modeled in TCAD, as the 3D model shown in Figure 4-16. Again, for clarity, the silicon dioxide (SiO_2) that fully covers the pixel is not displayed, but TX1, TX2, TX3, RST, SF, SEL, and their respective metal connections are visible.

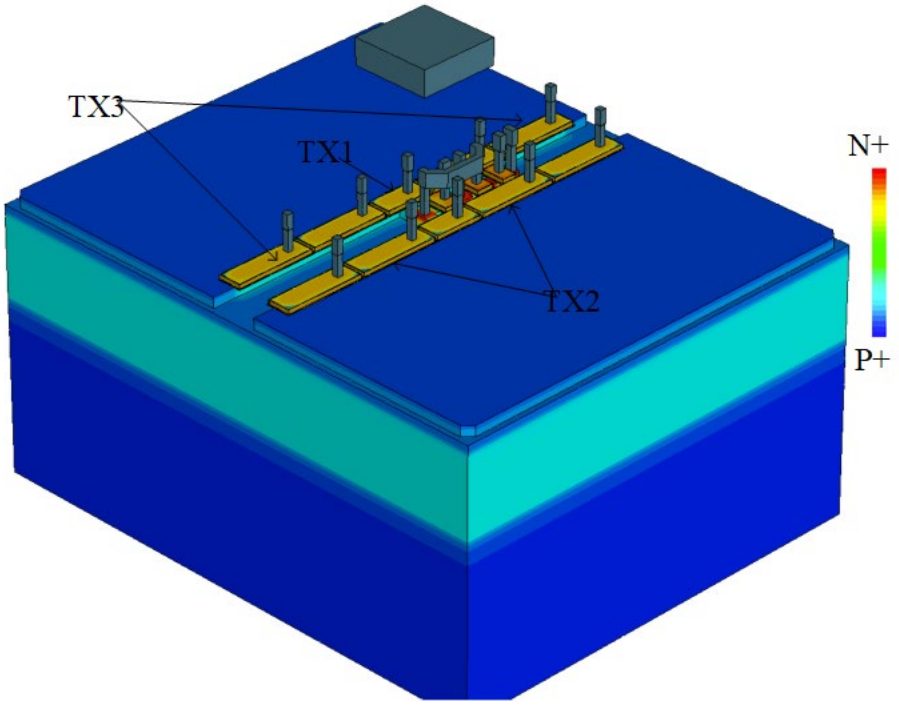
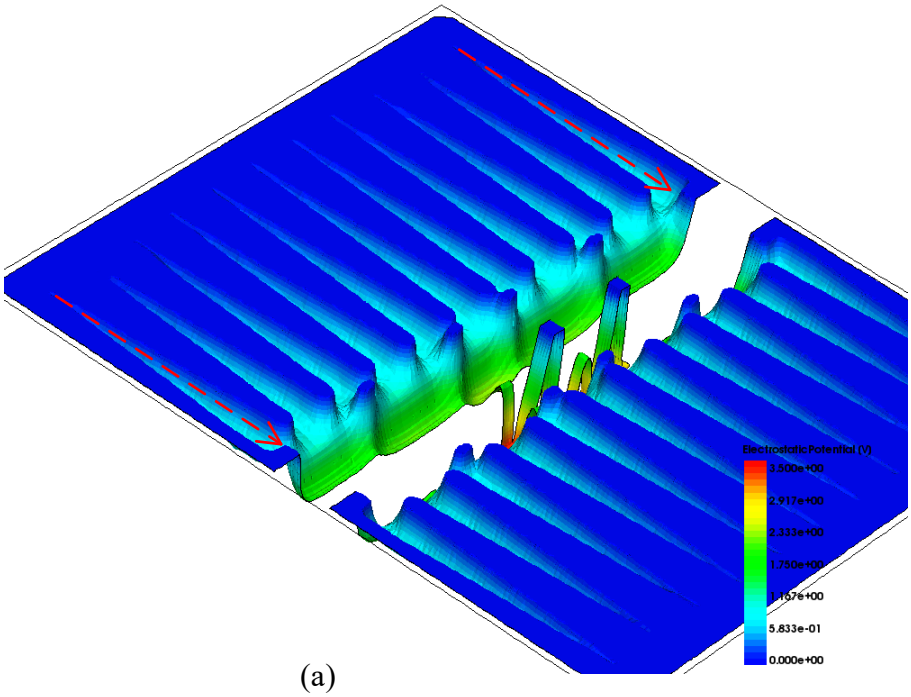
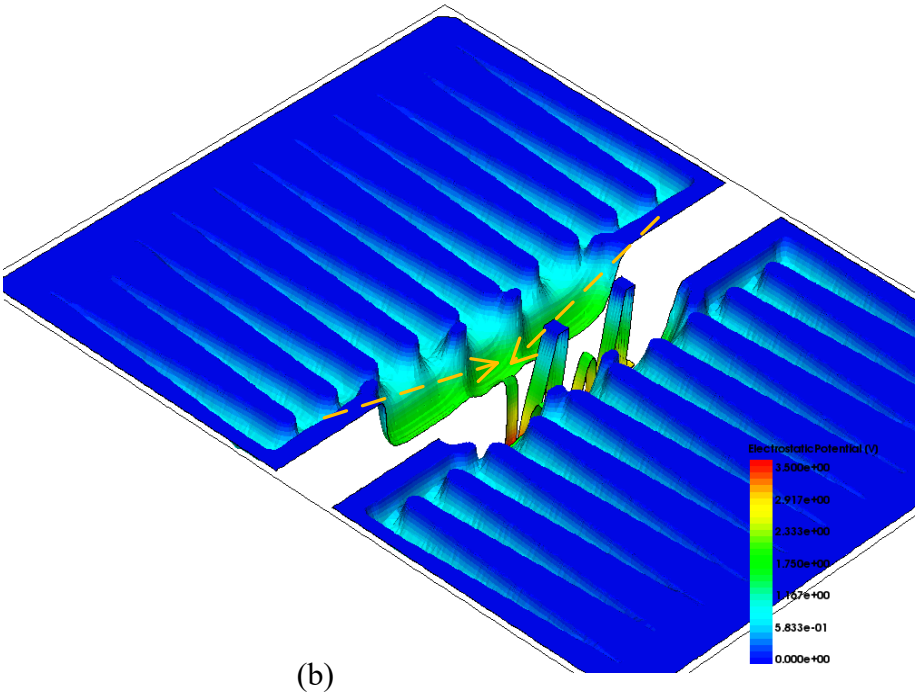


Figure 4-16 3D TCAD model of the variant 2 pixel

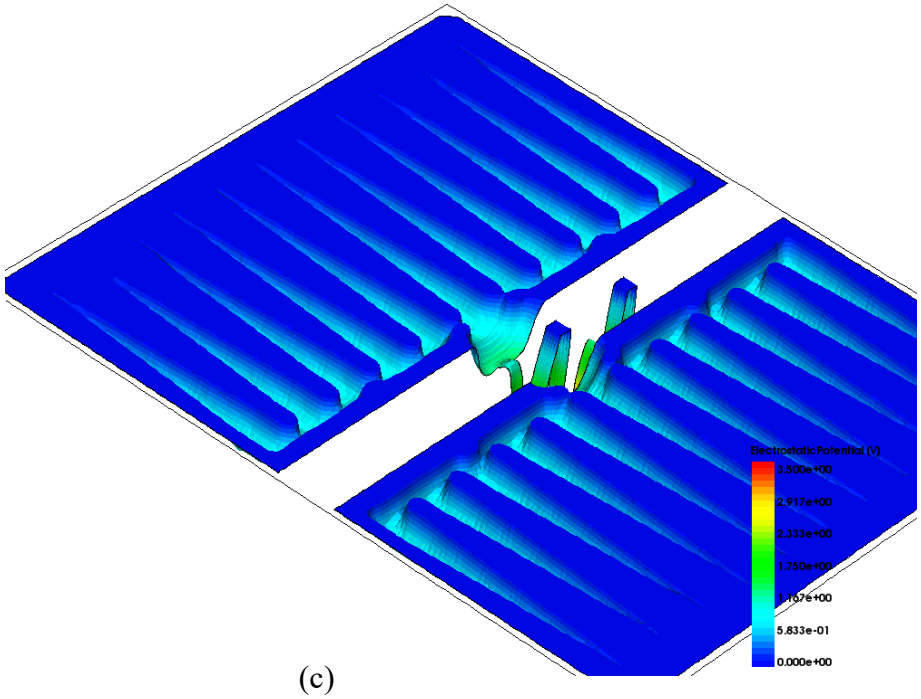
Figure 4-17 illustrates the electrostatic potentials during the charge transfer process, where one can observe that the movement of electrons can be divided into two steps. Firstly, electrons move from the tip of photodiode fingers to the bottom of the fingers where transfer gates are located (highlighted in red dash line in Figure 4-17 (a)). Next, electrons move from the channel beneath the TX3 gate to the channel beneath the TX2 gate. Finally, as TX1 turns off, all the electrons are expected to leave the TX1 channel and be driven towards the FD node (highlighted in yellow dash line in Figure 4-17 (b)).


ElectrostaticPotential (V)
3.500e+00
2.917e+00
2.333e+00
1.750e+00
1.167e+00
5.833e-01
0.000e+00

(a)


ElectrostaticPotential (V)
3.500e+00
2.917e+00
2.333e+00
1.750e+00
1.167e+00
5.833e-01
0.000e+00

(b)



(c)

Figure 4-17 Electrostatic potentials surface plots of variant 2 pixel at different states (a) TX3=on, TX2=on, TX1=on, (b) Tx3=off, TX2=on, TX1=on, (c) TX3=off, TX2=off, TX1=on

To confirm the conversion gain of variant 2 pixels, a TCAD transient simulation was conducted, and the result is presented in Figure 4-18. The plot depicts the TX gates voltage, FD node voltage, and the total number of electrons in the upper (*e*Total1) and lower (*e*Total2) photodiode, similar to that in Figure 4-12. Based on the calculations, the CG is found to be 93 μV/*e*-, which is over 10 times better than the CG of the variant 1 design.

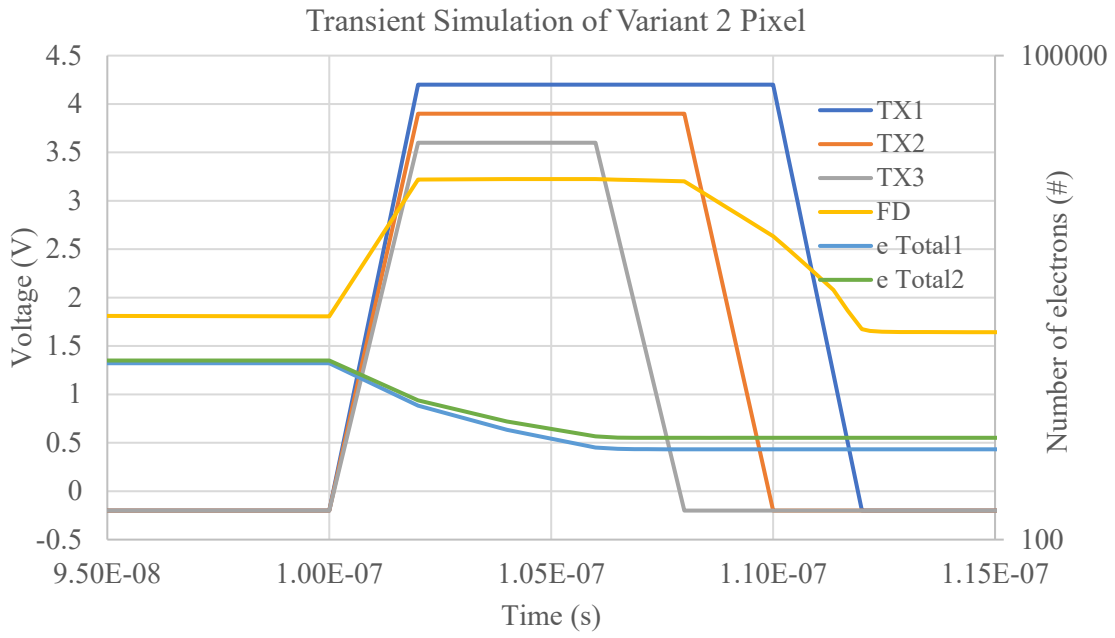


Figure 4-18 TCAD transient simulation result of variant 2 pixel

Although there has been a significant improvement in CG, it is worth noting that a considerable amount of charge remains in the photodiode after the charge transfer phase, leading to an image lag. Therefore, it is crucial to identify the root cause of incomplete charge transfer and optimize it. This will be discussed in the following section.

4.4 Further Optimization on Charger Transfer Time

Figure 4-19 displays the electrostatic potential of the TX channels in the variant 2 pixel under different gate voltage conditions. When all the TX gates are on, the potential barriers (~0.4 V) are clearly visible at the center of the TX gate and the gap between two adjacent channels. These potential barriers significantly impede the transfer of charge.

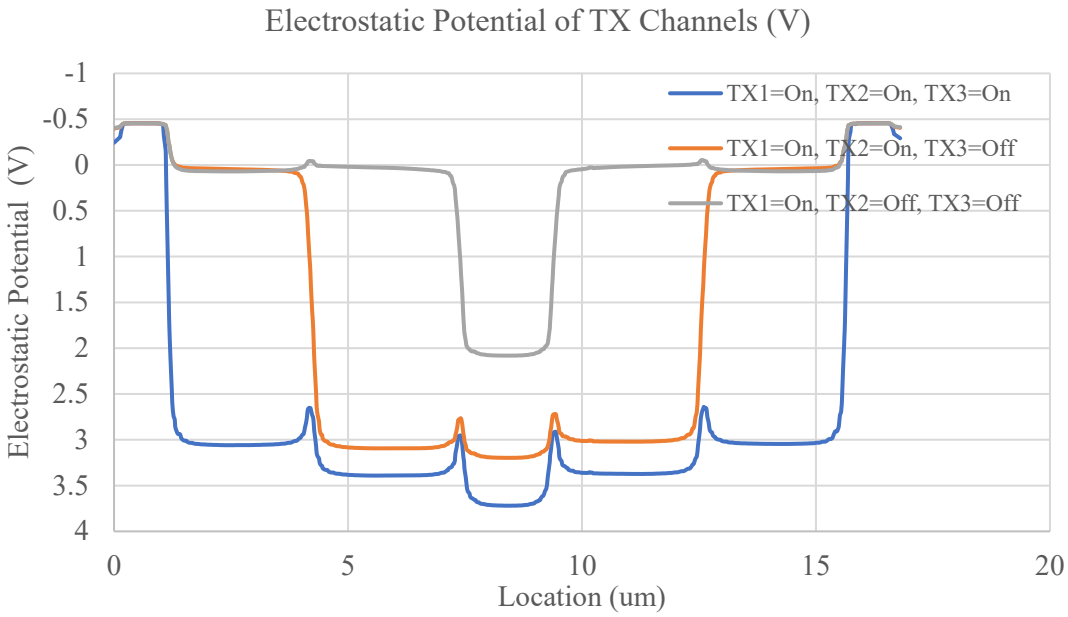


Figure 4-19 Electrostatic potential plot along the TX channels

Figure 4-20 illustrates the electron density in the channel of three TX gates after the charge transfer phase. It is apparent that a considerable number of electrons remain in TX gate channels due to the potential barriers mentioned above. The early CCD image sensors faced a similar issue, which was addressed through the development of a double-poly gate or buried channel [44] to create lateral electric fields [45] between channels, thereby facilitating the transfer of charges. However, none of these techniques are available in this project due to process limitations. Therefore, innovation is required to resolve the issue of insufficient charge transfer.

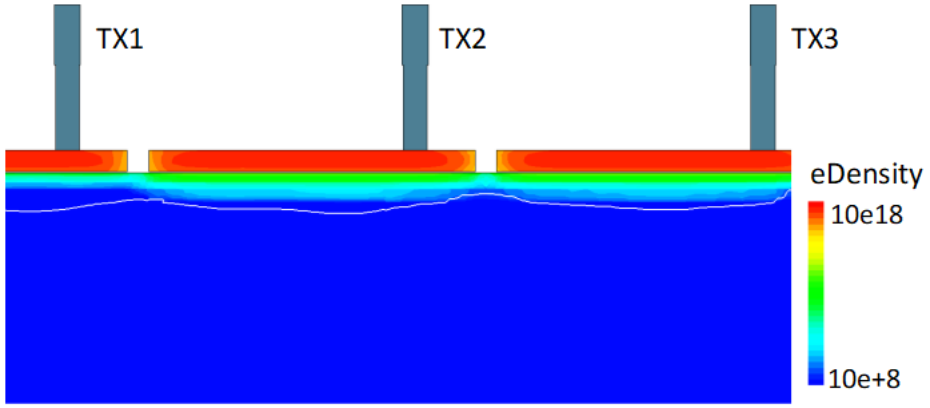


Figure 4-20 Electron density in TX channels after TX gates are off

Inspired by the simple Equation 4-12, where E represents the electric field, ΔV represents the voltage, and ΔL represents the distance, one can establish an electric field to facilitate charge transfer. This can be achieved by either increasing the voltage difference between two adjacent transfer gates or reducing the distance that electrons travel between them.

$$E = \frac{\Delta V}{\Delta L} \qquad (4-12)$$

It is generally not advisable to increase the control voltage significantly beyond the value recommended by the foundry due to reliability concerns. Therefore, the only feasible solution, without process modification, is to decrease the distance that electrons travel in the TX channel. In the variant 2 pixel, electrons move in the direction of the TX gate width as Figure 4-17 (b) yellow dash line indicated, which spans over 3um. In the subsequent section, Figure 4-21 displays the variant 3 pixel, where electrons move in the direction of the TX gate length, spanning only 0.8 um.

4.4.1 Pixel Variant 3

Inspired by the rising sun shape pixel in [7], the conceptual layout for variant 3 high-speed pixel design based on charge-sweep transfer gate in this project is presented in Figure 4-21. Similar to the variant 2 design, TX3, TX2 and TX1 stands for the charge-sweep transfer gates. Each gate features a smaller geometry size than the prior one, resulting in a smaller floating diffusion node, as highlighted in the red rectangle.

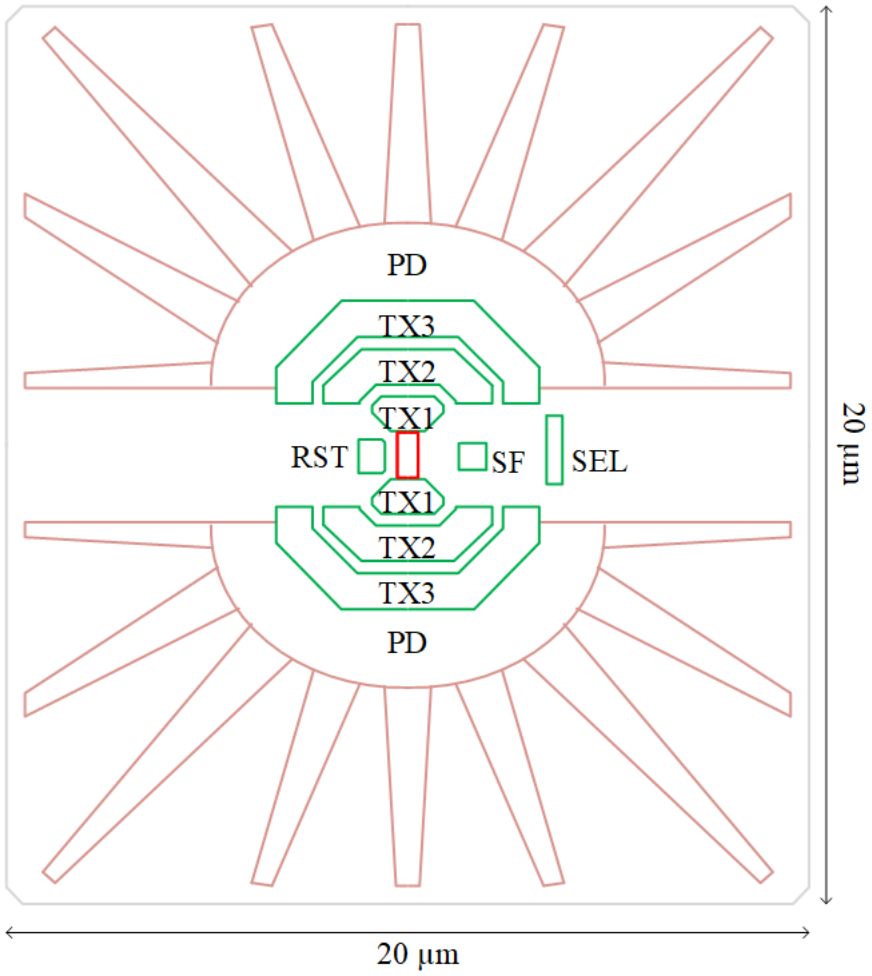


Figure 4-21 Conceptual layout of the variant 3 high-speed pixel

4.4.2 TCAD Simulation of Pixel Variant 3

To simulate the device, the variant 3 pixel is also modeled in TCAD, as the 3D model shown in Figure 4-22. Again, for clarity, the silicon dioxide (SiO_2) that fully covers the entire pixel is not displayed, but TX1, TX2, TX3, RST, SF, SEL, and their respective metal connections are visible.

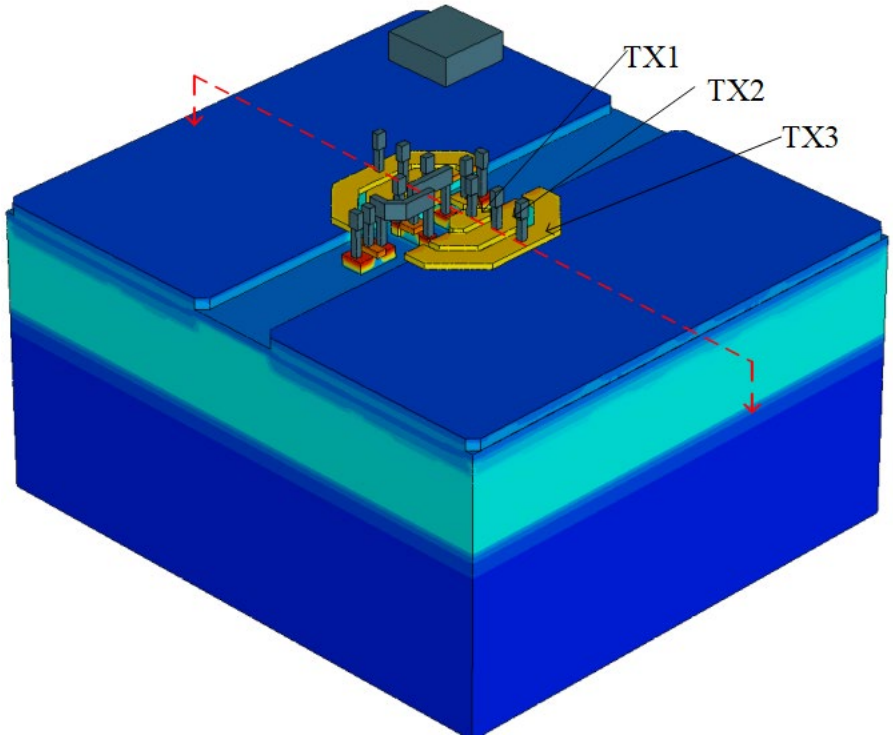


Figure 4-22 3D TCAD model of the variant 3 pixel

For a 180 nm process, the typical distance between two poly gates varies from 0.2 μm to 0.3 μm. Figure 4-23 depicts two timing sequences that were developed to overcome the potential barrier and achieve full charge transfer from the photodiode to the floating diffusion node.

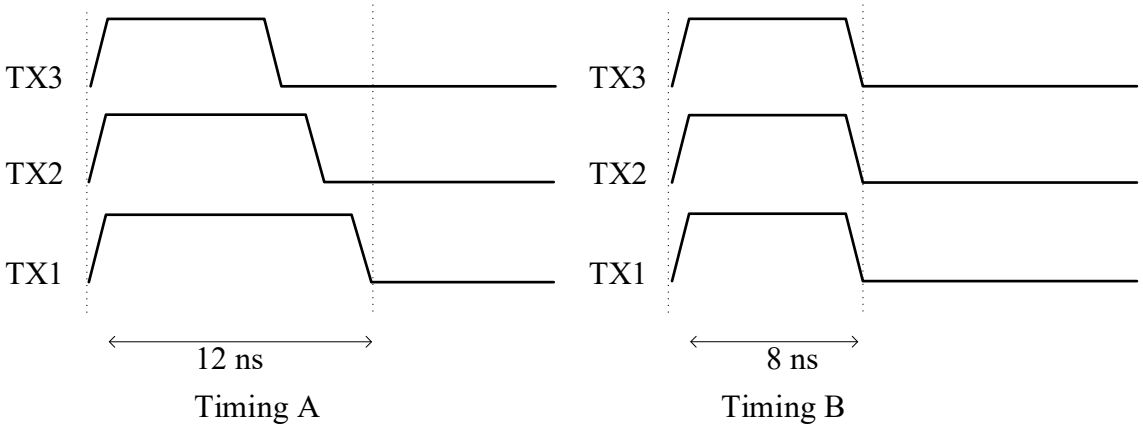
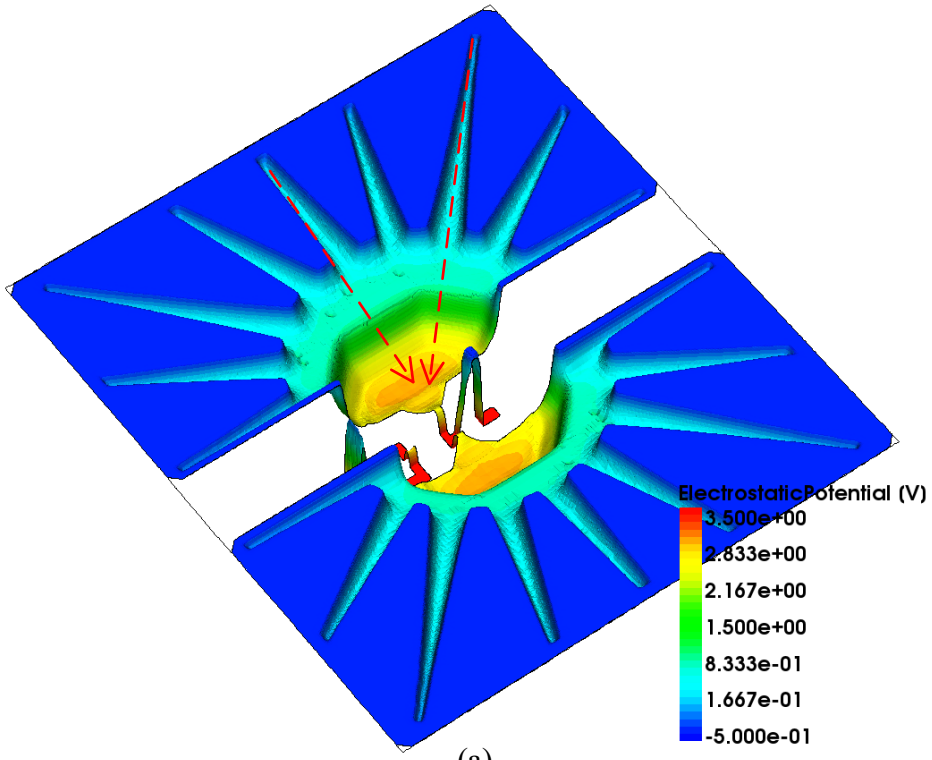
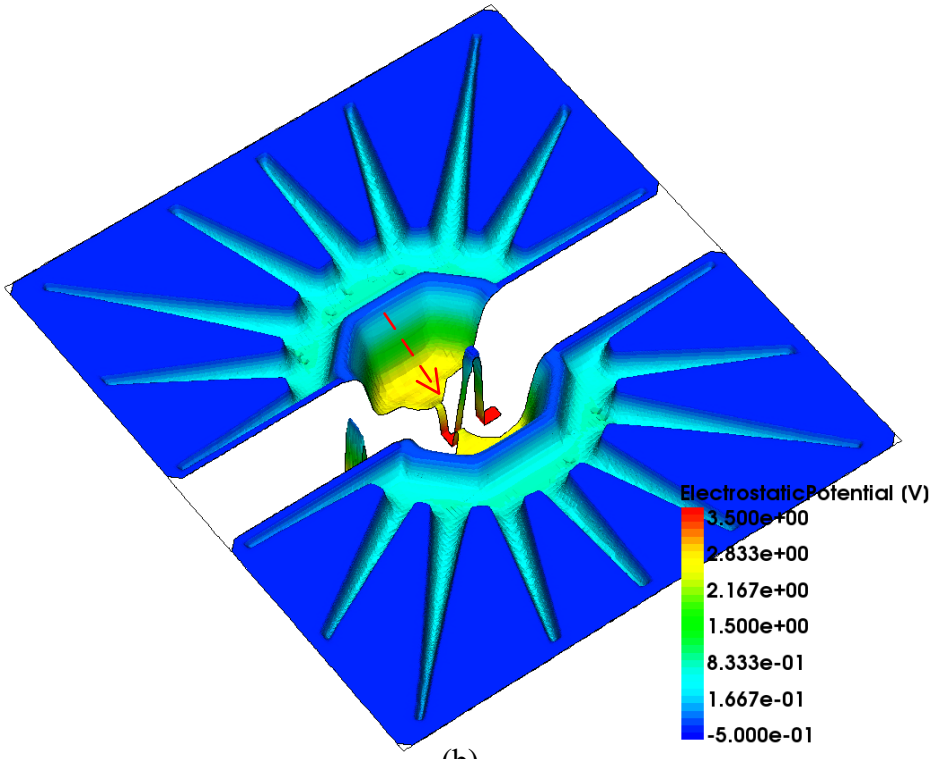


Figure 4-23 Two operation timing sequencies of charge sweep gate

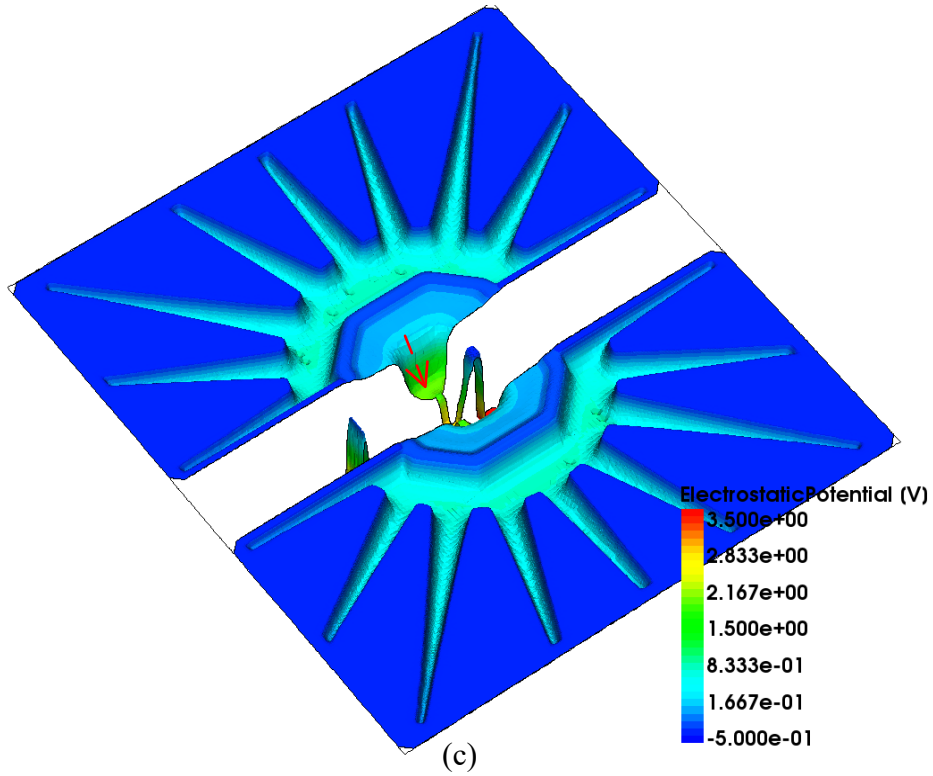
In timing sequence A, TX1's on voltage is slightly higher than that of TX2, while TX2's on voltage is slightly higher than that of TX3. Figure 4-24 illustrates the electrostatic potentials during the charge transfer process, where one can observe that the movement of electrons as the red dashed lines indicated.



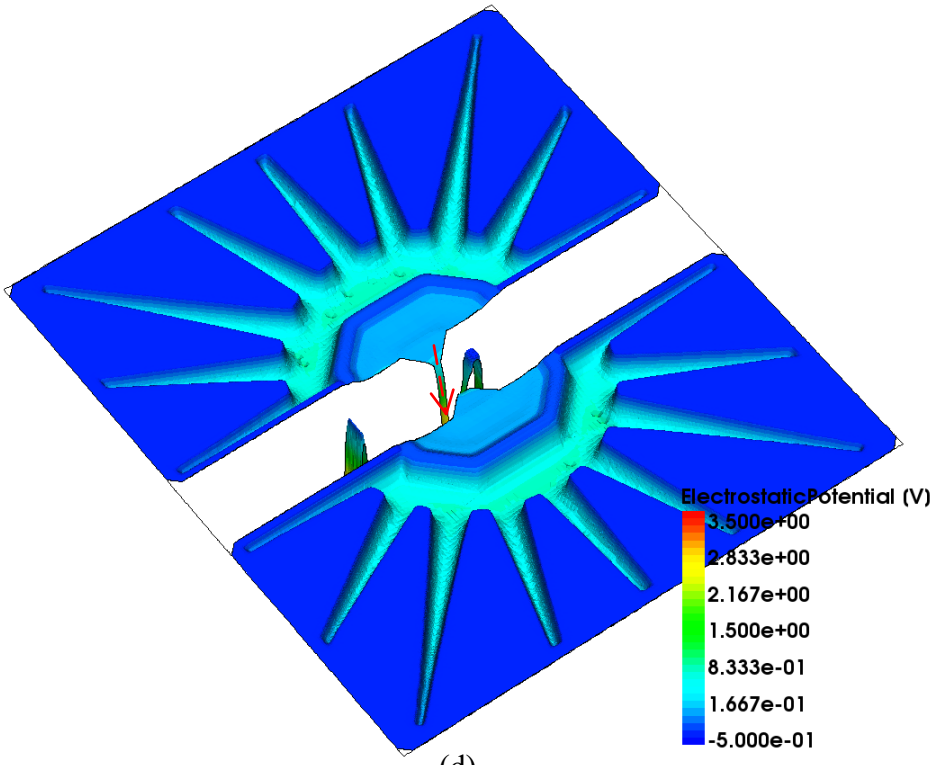
(a)


ElectrostaticPotential (V)
3.500e+00
2.833e+00
2.167e+00
1.500e+00
8.333e-01
1.667e-01
-5.000e-01

(b)


ElectrostaticPotential (V)
3.500e+00
2.833e+00
2.167e+00
1.500e+00
8.333e-01
1.667e-01
-5.000e-01

(c)



(d)

Figure 4-24 Electrostatic potential surface plots of the variant 3 pixel at different states with timing sequency A: (a) TX3=on, TX2=on, TX1=on, (b) TX3=off, TX2=on, TX1=on, (c) TX3=off, TX2=off, TX1=on, (d) TX3=off, TX2=off, TX1=off

At the beginning of the charge transfer, all three gates - TX1, TX2, and TX3 - are switched on. As the charge transfer nears completion, TX3 turns off first, followed by TX2, and finally, TX1. Taking into account the rise and fall times of the TX pulses, the entire charge transfer sequence takes 12 ns in simulation. Figure 4-25 depicts an electrostatic potential plot along the charge transfer path of this timing. The plot clearly shows that the potential barrier (~ 0.1 V) between two adjacent gates is significantly lower than the one in Figure 4-19.

Moreover, by controlling the falling edge slew rate of the TX gate, it is possible to eliminate the potential barrier that exists between two gates during the falling transition

of the TX gates. This process establishes a monotonically increasing electrostatic potential profile and creates a strong electrical field that rapidly sweeps previously trapped electrons to the next channel. In the end, complete charge transfer can be accomplished.

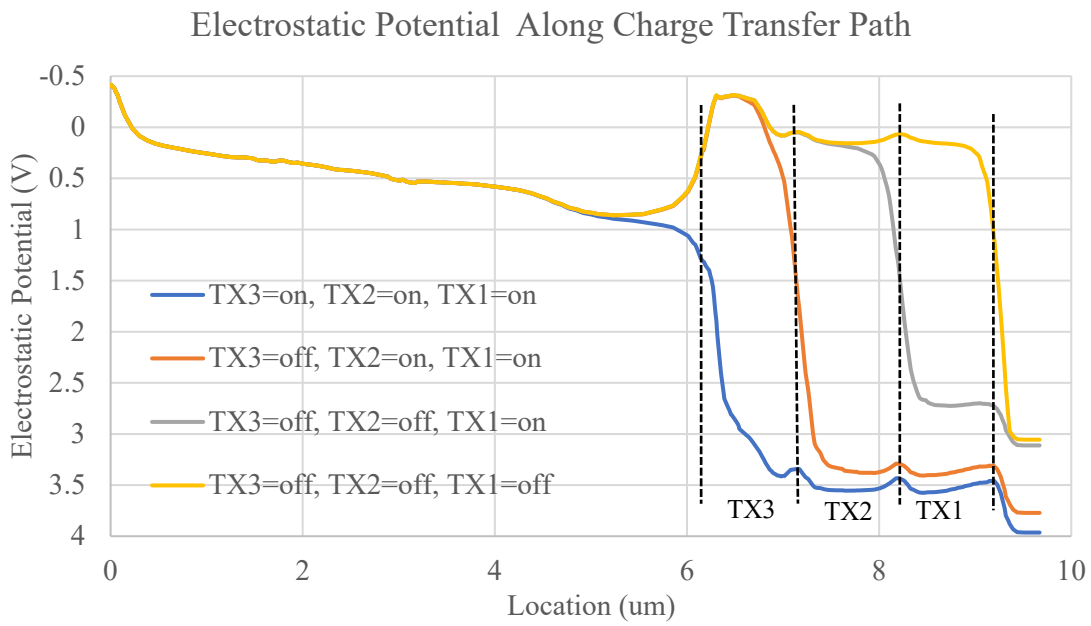


Figure 4-25 Electrostatic potential plots along the charge transfer path of the variant 3 pixel with timing sequency A

A TCAD transient simulation was conducted to confirm the complete charge transfer of variant 3 pixels in timing A, and the results are presented in Figure 4-26. The plot illustrates the voltage of the TX gates and the total number of electrons in the upper (eTotal1) and lower (eTotal2) photodiodes. The simulation clearly demonstrates that complete charge transfer is achieved within 12 ns.

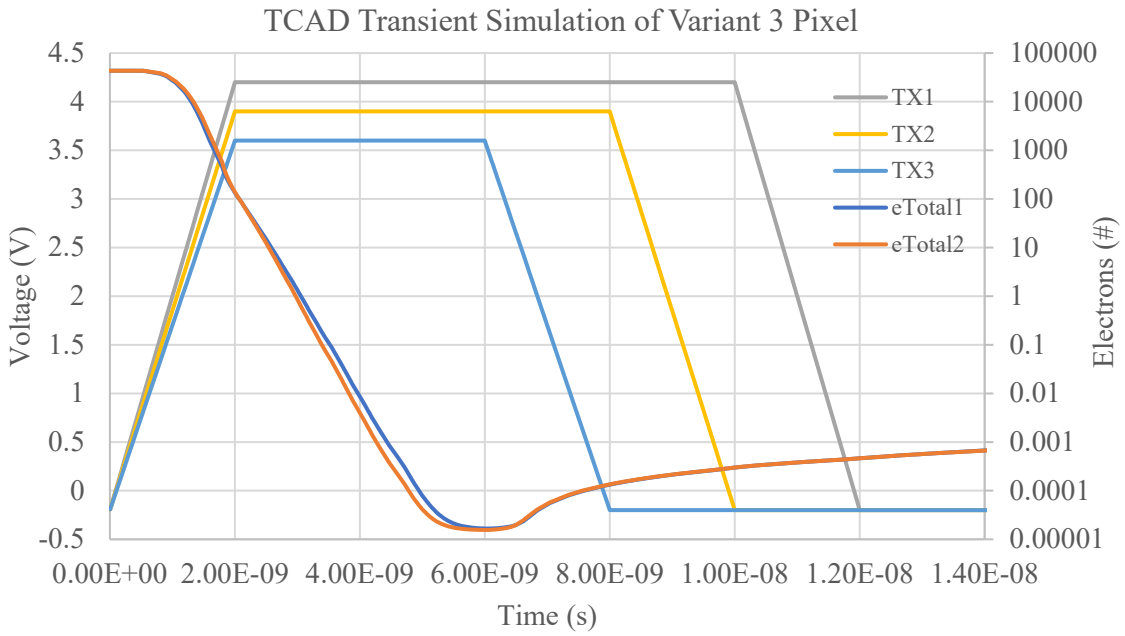


Figure 4-26 TCAD transient simulation result of the variant 3 pixel with timing sequency A

In Figure 4-23 timing sequence B, the on voltage of TX1 is considerably higher than that of TX2, while the on voltage of TX2 is significantly higher than that of TX3. This leads to the elimination of the potential barrier between the adjacent gates when they are turned on. During the charge transfer process, all three gates (TX1, TX2, and TX3) are initially switched on. Subsequently, all three gates are simultaneously turned off upon the completion of the charge transfer. According to simulation results, the complete charge transfer sequence takes only 8 ns. Electrostatic potentials during the charge transfer process are illustrated in Figure 4-27.

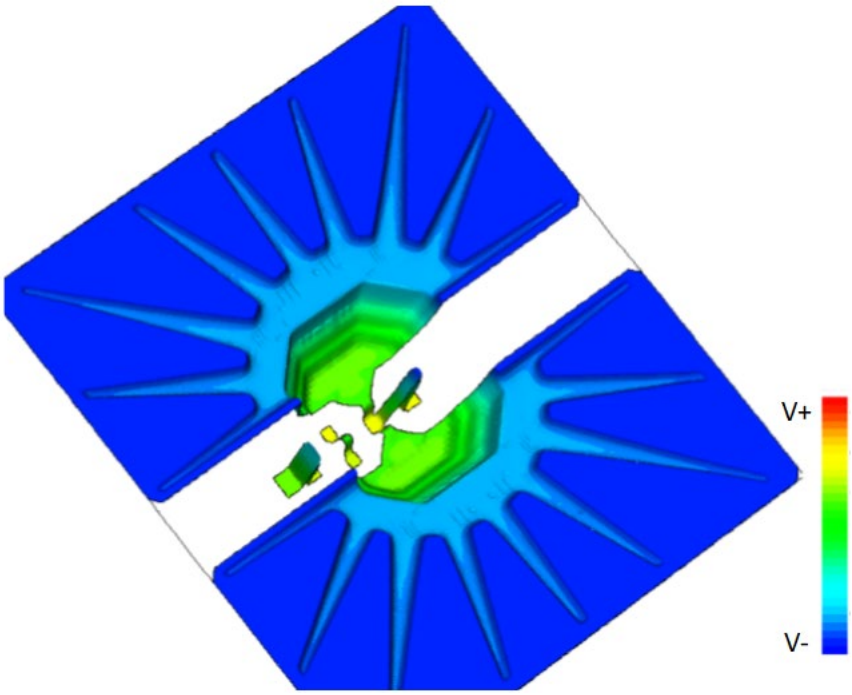


Figure 4-27 Electrostatic potential surface plot of variant 3 pixel by timing sequency B when TX3=on, TX2=on, TX1=on

Figure 4-28 depicts an electrostatic potential plot along the charge transfer path of this timing. The plot clearly shows that no significant potential barrier present between two adjacent gates. However, one can observe a potential barrier between the FD and TX1 channel that can trap some electrons. Nevertheless, once the TX1 gate turns off, the potential barrier will be eliminated, allowing all electrons to be transferred to PD, thereby achieving complete charge transfer.

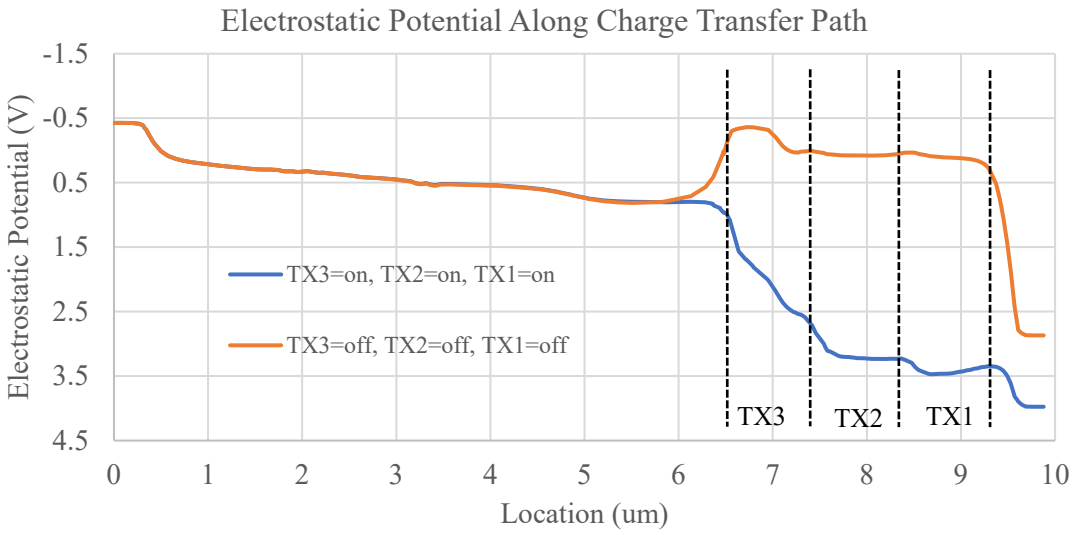


Figure 4-28 Electrostatic potential along the charge transfer path of the variant 3 pixel with timing sequency B

A TCAD transient simulation was conducted to confirm the complete charge transfer of the variant 3 pixels in timing B, and the results are presented in Figure 4-29. The simulation demonstrates that complete charge transfer is achieved within 8 ns.

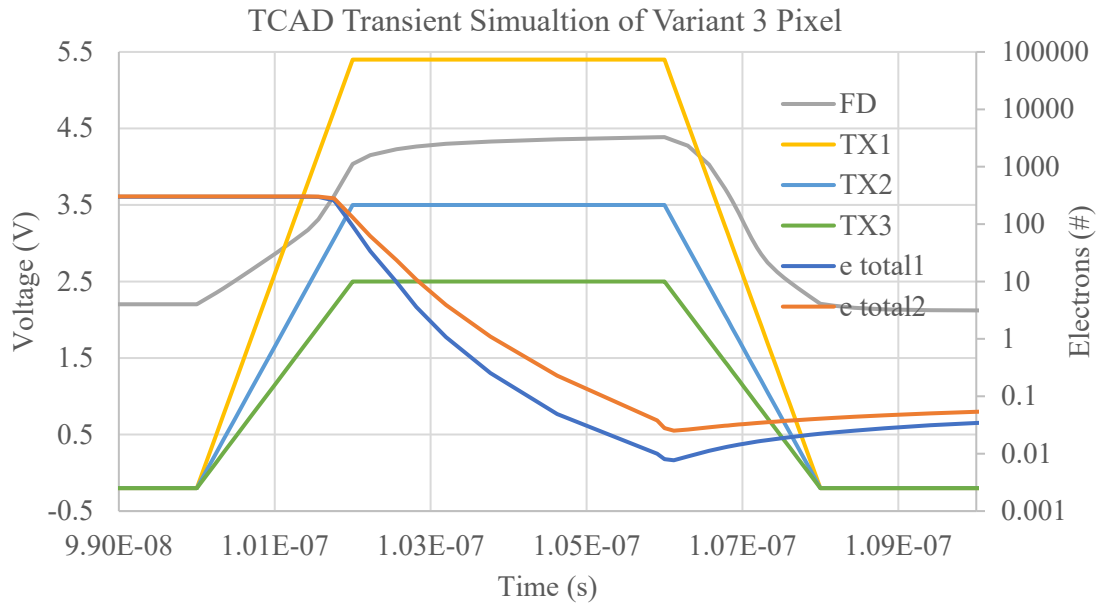


Figure 4-29 TCAD transient simulation result of the variant 3 pixel with timing sequency B

Having achieved full charge transfer, it is advisable to re-check the conversion gain. The transfer of electrons in the charge sweep transfer gate pixel does not occur directly from the photodiode to the floating diffusion, which makes it possible to move the floating diffusion slightly away from the TX gate and reduce the overlap capacitance C_{TX_FD}. A similar idea has been previously reported in [46,47,48]. Figure 4-30 shows a cross-sectional doping profile of the FD node and adjacent TX gates.

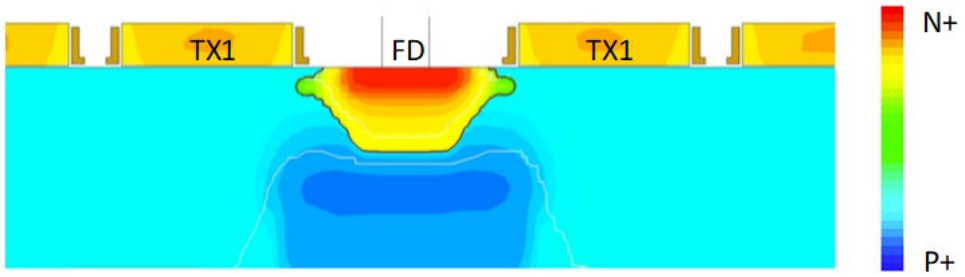


Figure 4-30 Cross-section of doping profile around FD node

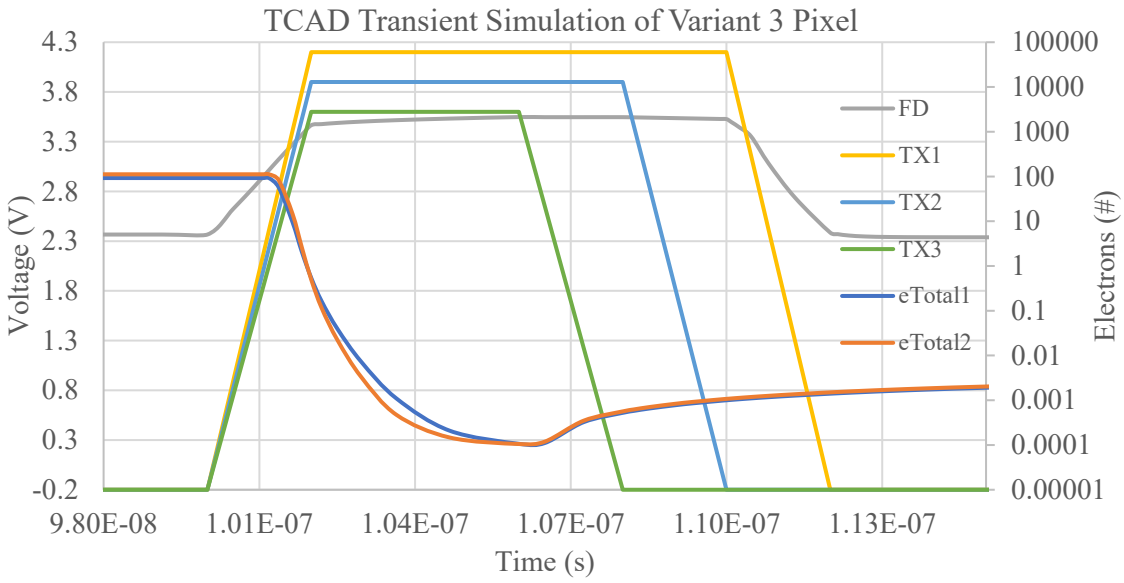


Figure 4-31 Transient simulation result of variant 3 pixel

The TCAD transient simulation result is displayed in Figure 4-31. Based on the calculations, the CG is found to be 138 μV/e-. This result shows a further improvement compared to the variant 2 pixel. The smaller FD node area and enhanced charge sweep gate design have contributed to this improvement.

As mentioned earlier, high-speed CMOS image sensors are more susceptible to noise due to the trade-off between the design requirements for fast readout speed and lower thermal noise. Fast readout speed requires smaller capacitance, while lower thermal noise necessitates larger capacitance. In an effort to address this issue, [12] proposed a passive correlated double sampling (CDS) amplifier to reduce input-referred noise. However, the gain of the passive CDS amplifier is determined by the capacitance ratio of the NMOS capacitor at depletion mode versus inversion mode, which depends on both the process and voltage. This introduces unavoidable non-linearity to the entire image sensor, estimated to be around 3% [12]. Furthermore, the settling of the amplified voltage limits the frame rate of the burst mode image sensor.

Hence, there is a need for a process-independent technique to decrease the input-referred noise without compromising the rapid charge transfer and high frame rates. The following section will delve into the specifics of improving the image sensor's CG to minimize the input-referred noise.

4.5 Further Optimization on Conversion Gain

As indicated by Equation 4-11, the pixel conversion gain is determined by the overall lumped capacitance at the FD node. Figure 4-32 shows the capacitors that contributes to CG for a charge sweep transfer gate pixel.

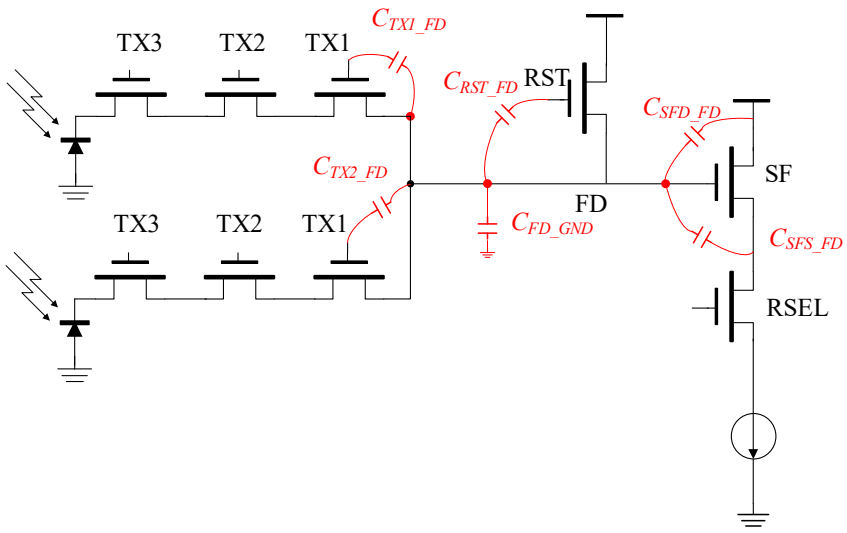


Figure 4-32 FD node capacitance distribution of charge-sweep-gate based pixel

A TCAD AC simulation is run to analyze the contribution of each component in the variant 3 pixel and the result is shown in the pie diagram in Figure 4-33. It shows that the total capacitance at FD is 1.19fF.

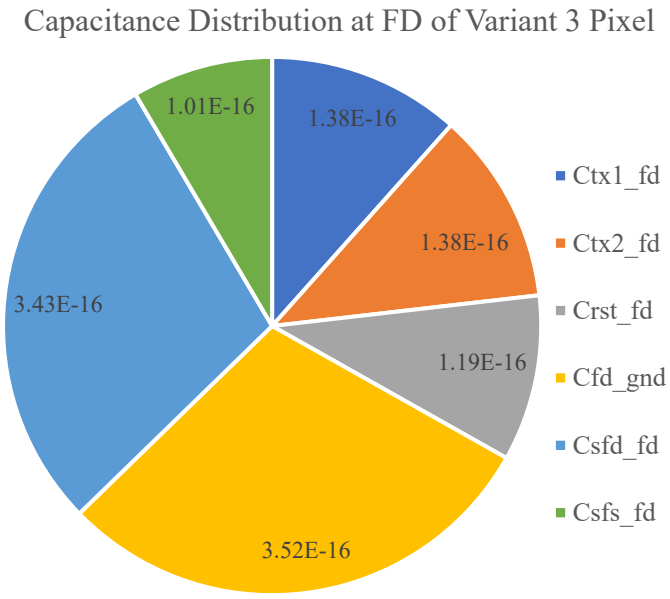


Figure 4-33 Distribution of lumped capacitance at FD of variant 3 pixel

Two TX-to-FD capacitors (C_{tx1_fd}, C_{tx2_fd}) each contributes 11.5% of the total capacitance, which is significantly less than that in the variant 1 and variant 2. Increasing the gap between TX gates and the FD node may further reduce the C_{tx_fd}. However, such a modification comes with the risk of insufficient charge transfer.

The FD-to-ground capacitor (C_{fd_gnd}) contributes 29.5%, and its dominance comes from the PN junction depletion capacitance, which can be modeled as a parallel-plate capacitor, as shown in Equation 4-13 [49]. Here, ε_s denotes the silicon dielectric constant, A represents the PN junction area, and W_{dep} stands for the depletion width.

$$C = \frac{\varepsilon_s * A}{W_{dep}} \qquad (4-13)$$

According to Equation 4-14 [49], the PN junction lightly-doped side's doping concentration primarily determines the W_{dep}, where ϕ denotes the PN junction built-in voltage, V_r represents the reversed-biased voltage, and N denotes the doping concentration of the lightly-doped side.

$$W_{dep} = \sqrt{\frac{2 * \varepsilon_s * (\phi + V_r)}{q * N}} \qquad (4-14)$$

Due to foundry requirements, modifying the doping concentration of the photodiode is not allowed in this project. Therefore, the only adjustable parameter is the PN junction area. However, it should be noted that the 180nm fabrication process imposes lithography limitations, making it challenging to create an active area smaller than the design rule. Attempting to do so may cause a misalignment of contact, resulting in PN junction leakage [50] and an increase in resistance, as shown in Figure 4-34.

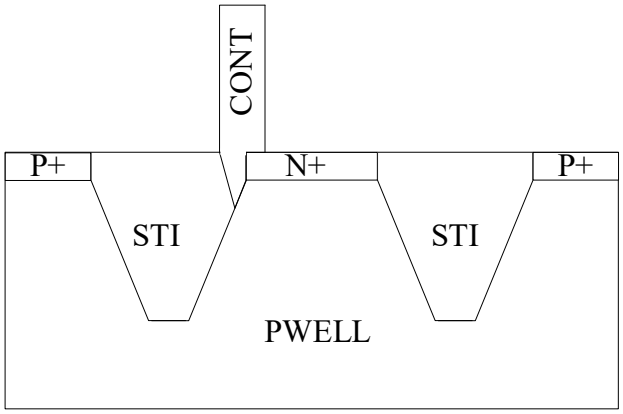


Figure 4-34 Conceptual schematic of contact mis-alignment

The source follower gate-to-ground capacitor also contributes to the FD-to-ground capacitance. To reduce noise, the pixel source follower in this project utilizes a buried-channel NMOS (BCH), with a default size of W/L=0.3/0.6 (μm/μm). This leaves room for further optimization.

The FD-to-source follower drain capacitor (C_{sfd_fd}) contributes 28% to the total capacitance, mainly due to the overlap capacitance between the gate and drain of the source follower. Inspired from the pump gate design, there is potential for optimizing this capacitance. In the next section, we will discuss the improvements made to CG based on the above analysis.

4.5.1 Source Follower Analysis and Optimization

Figure 4-35 (a) presents a 3D TCAD model for the default buried channel NMOS in this process, and Figure 4-35 (b) depicts its cross-section. It is apparent that the effective channel length much is shorter than the gate length due to the diffusion of source and drain *n* dopant, hindering the transistor gate length shrinkage. If the transistor gate length is directly reduced beyond the design rule limit, it may result in an increase in leakage current between the drain and source because of drain-induced barrier lowering

(DIBL) [51]. Additionally, it can lead to other short channel effects [77] or result in a direct short circuit. Inspired by [41,70], the light-doped-drain (LDD) is proposed to be removed and enable further shrinkage of the transistor, as illustrated in Figure 4-36.

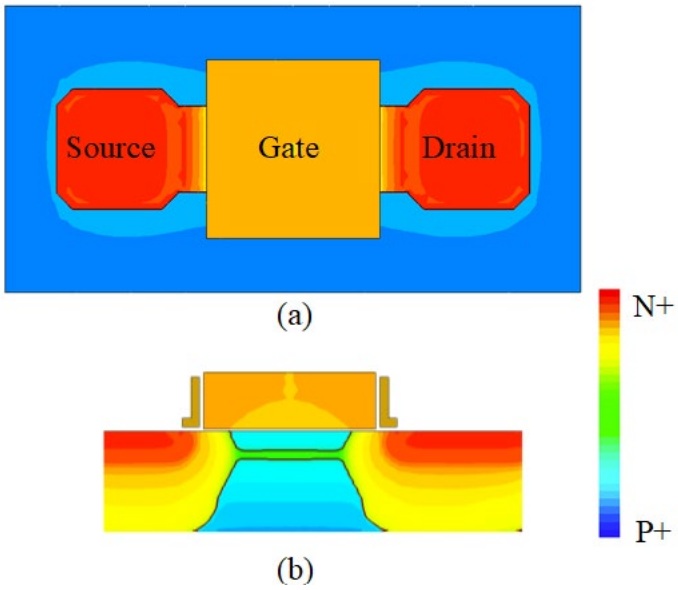


Figure 4-35 (a) 3D TCAD model of the default buried channel NMOS and (b) the doping profile of its cross-section

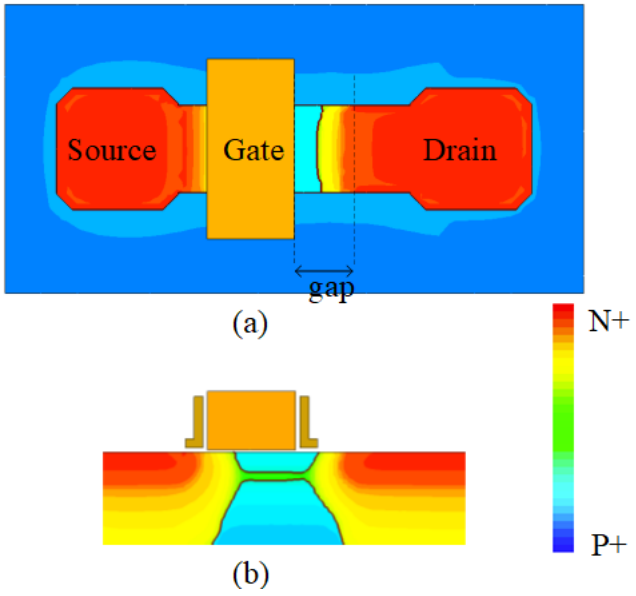
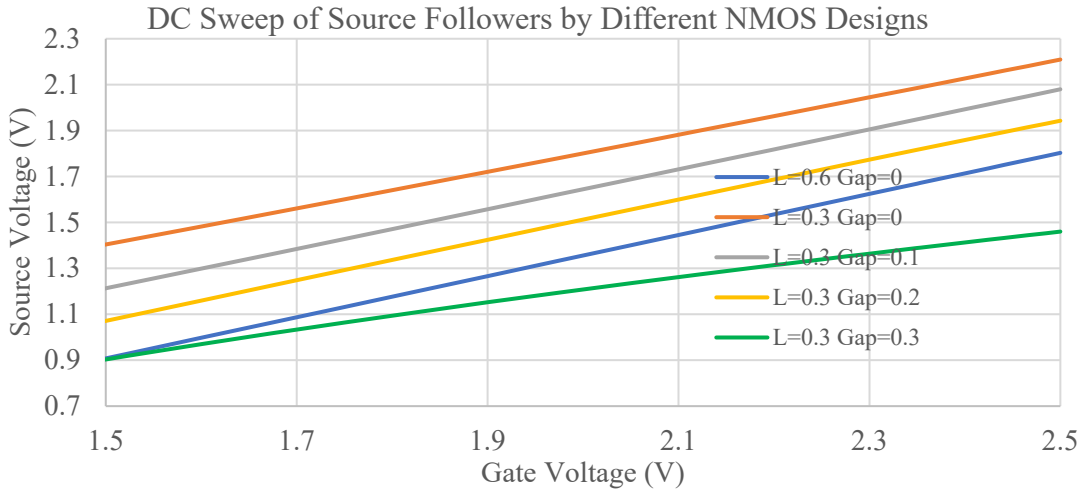


Figure 4-36 (a) 3D TCAD model of the proposed buried channel NMOS and (b) the doping profile of its cross-section

Due to the concern of an increase in channel resistance [71], the LDD at the source side is maintained, while the LDD at the drain side is removed. The removal results in the compensation of the diffusion effect of *n* dopant towards the transistor channel. Consequently, the gate length of the transistor can be reduced down to 0.3 µm. Additionally, the optimal design is determined by exploring the gap distance between 0 µm to 0.3 µm, as shown in Figure 4-36(a). Both of the proposed buried channel NMOS transistor (L=0.3 µm, gap=0 µm~0.3 µm) and the default one (L=0.6 µm, gap=0 µm) are configured as a source follower biased with an ideal DC current sink. The gate voltage is swept from 1.5 V to 2.5 V, and the DC sweep results are plotted in Figure 4-37 (up) and the first order derivative results are plotted in Figure 4-37 (bottom).



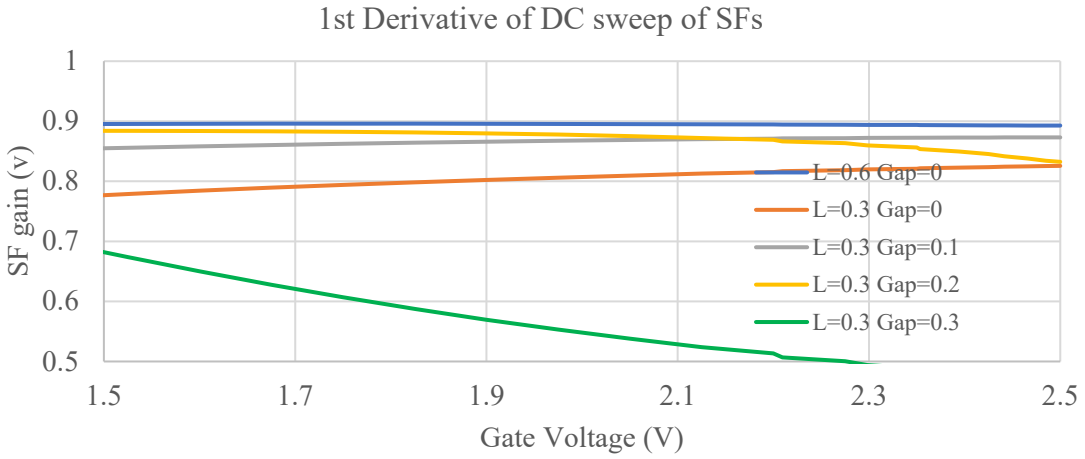


Figure 4-37 DC sweep simulation result of buried channel NMOSs (on the up) and its first derivative plots (on the bottom)

It is evident that both L=0.3 Gap=0, L=0.3 Gap=0.1 and L=0.6 Gap =0 designs exhibit superior linearity in comparison to the others. As mentioned in the previous analysis, the removal of the LDD region leads to a significant reduction in the overlap capacitance between the gate and drain. Table 4-2 lists the values of Cgd along with other AC parameters for various designs.

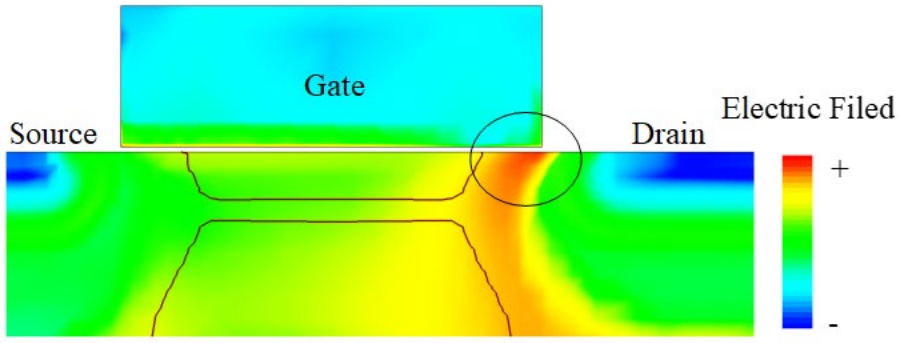
AC Performance of Different SF Designs					
SF Length (μm)	Gap Dist (μm)	Gain@Vg=2.5V (V/V)	Gain@Vg=1.5V (V/V)	Cgs (fF)	Cgd (fF)
0.3	0	0.825	0.777	0.52	0.22
0.3	0.1	0.873	0.855	0.57	0.17
0.3	0.2	0.838	0.884	0.66	0.15
0.3	0.3	0.472	0.682	0.68	0.12
0.6	0	0.893	0.895	0.79	0.26

Table 4-2 AC performance comparison between different source follower designs

Taking the Miller effect into consideration, the design with L=0.3 and gap=0.1 yields the smallest lumped capacitance at FD. Therefore, this design will be used in the variant 4 pixel.

Concerns may arise regarding the increased flicker noise resulting from smaller gate geometry sizes [52]. As pointed out by [53] and to be discussed in Chapter 5, the smaller SF gate will lead to a higher conversion gain and reduced input-referred noise, especially when using a fast CDS circuit.

One may also be concerned about the hot electron effect that can arise in the absence of lightly doped drain (LDD) regions [54]. The LDD region was first introduced to gradually reduce the strong electric field between the drain and channel, which in turn reduces the likelihood of high-energy collisions between electrons and the silicon lattice. As illustrated in Figure 4-36, a "lightly doped" region still exists on the drain side due to the diffusion effect, and it is actually distanced from the channel. Consequently, in terms of the electrical field, the proposed new design shows a lower peak electric field, highlighted in the circle, as compared to the default design when biased at the same conditions, as demonstrated in Figure 4-38. As a result, the proposed new design actually has a lower likelihood of high-energy collision than the default design.



(a)

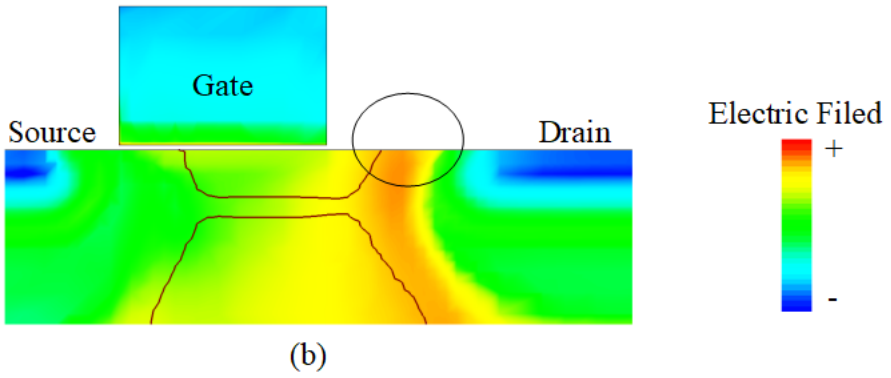


Figure 4-38 Electric field of: (a) default source follower and (b) proposed source follower in the same scale

4.5.2 Pixel Variant 4

As mentioned earlier, the default source follower in the variant 3 pixel has been replaced with the proposed source follower in the variant 4 pixel. Apart from this alteration, the design of variant 3 and variant 4 is identical. Consequently, the conceptual layout for the variant 4 pixel will not be presented here.

4.5.3 TCAD Simulation of Pixel Variant 4

To confirm the improvement in CG resulting from the new source follower, an AC simulation was performed again to analyze the contribution of each component at the FD node in variant 4 pixel. For comparison, the results of the variant 3 are also presented in Figure 4-39. Simulation shows that the C_{total} at FD is reduced from 1.19 fF to 0.895 fF, and CG is expected to increase to 178 μV/e-.

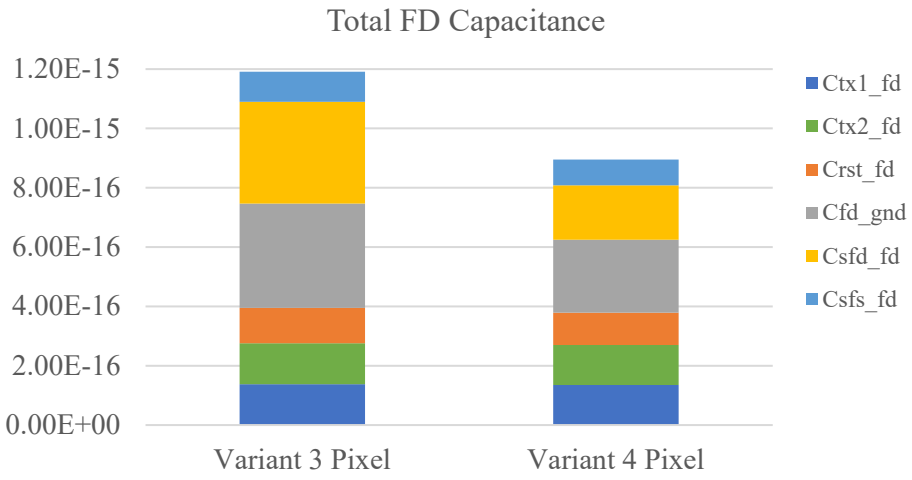


Figure 4-39 Capacitance distribution lumped at FD node of variant 3 pixel and variant 4 pixel

Figure 4-40 presents the results of the TCAD transient simulation for the variant 4 pixel. According to the simulation results, the pixel can transfer electrons completely within 12 ns same as the variant 3 pixel, and the CG value is found to be 174 µv/e-. This value is in close agreement with the AC simulation results and close to the highest CG (188 µV/e-) ever reported in 180 nm process with process modification [41].

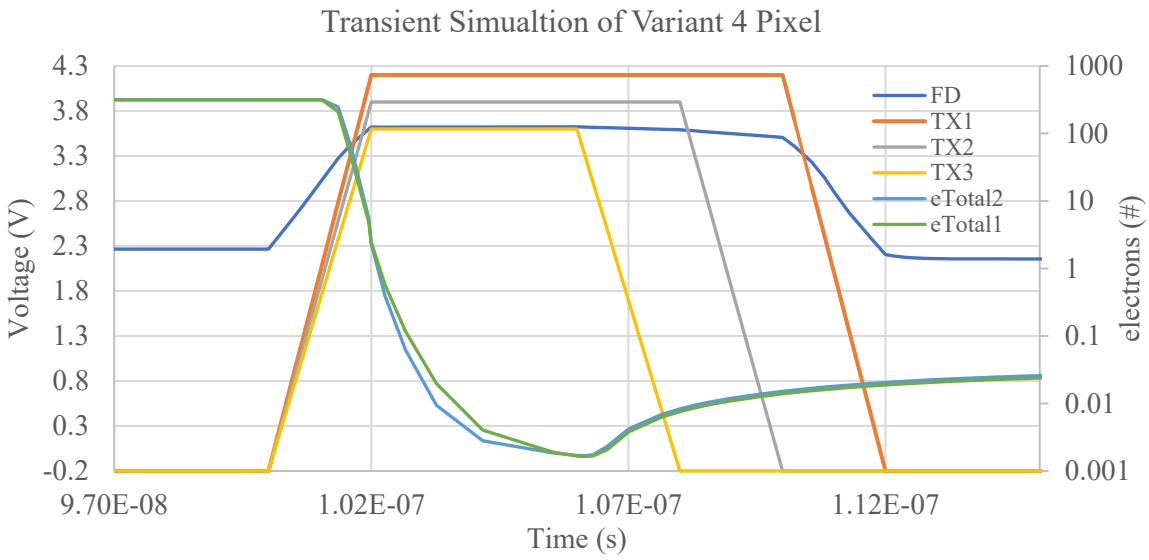


Figure 4-40 TCAD transient simulation result of the variant 4 pixel

After verifying the charge transfer time and conversion gain, it is recommended to also check the pixel dark current, particularly for this high-speed pixel design, where a strong electrical field has been built-in. The dark current can be determined by the recombination rate of the classical Shockley-Read-Hall process described by Equation 4-15 [79, 93,94], where σ represents the electron and hole capture cross-section, v_{th} denotes the thermal velocity, N_t represents the trap state density, and E_t is the trap level. It is evident that the trap distribution, density, and level all impact the net recombination rate. Without accurate information on the aforementioned factors, accurately simulating dark current can be highly challenging.

$$U = \sigma \times v_{th} \times N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kt}\right)} \qquad (4-15)$$

The pixel will be fabricated in a pinned-photodiode process, which will allow for proper passivation/isolation of defect on the silicon surface. To estimate the dark current, simulations were conducted in TCAD based on the default trap density at silicon and silicon dioxide interface provided by the foundry. The simulation result is illustrated in Figure 4-41.

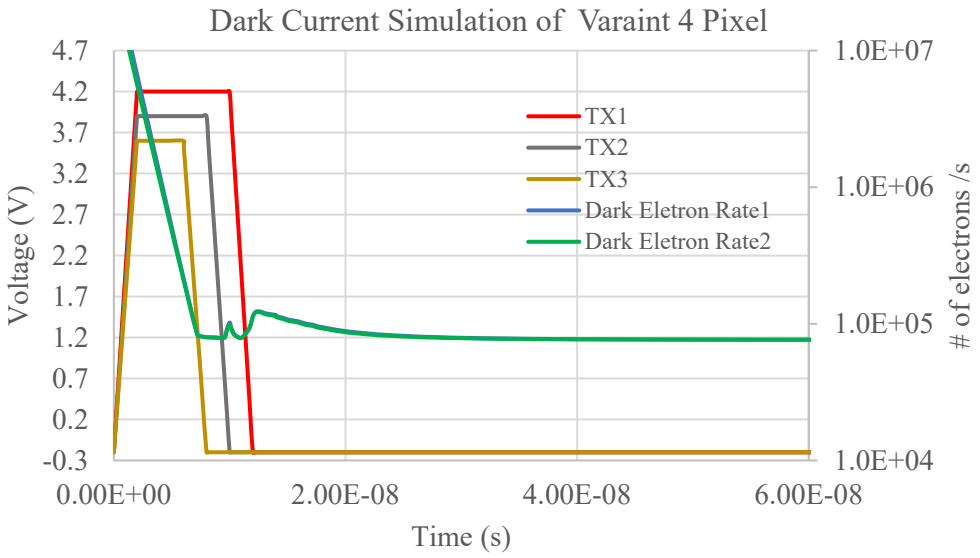


Figure 4-41 Dark current simulation result of variant 4 pixel

According to Figure 4-41, once the initial charge transfer is complete at 12 ns, the photodiode becomes fully depleted and un-equilibrium. Equation 4-15 suggests that once $pn - n_i^2 < 0$, resulting in a negative net recombination rate, indicating generation. In Figure 4-40, the blue and green curves represent dark electron rate, which is $8x10^4$ e-/s after TX gates are closed. Therefor the dark electron rate for the pixel is found to be $1.6x10^{-4}$ e-/ns/pixel, which is much higher than dark current in typical image sensors.

Concerns may arise regarding the high dark current simulated in this pixel. However, for the intended application with a frame rate of 20 Mfps, the maximum theoretical integration time is only 50 ns. Within this range, the maximum number of dark photons per frame is only $8x10^{-3}$ *e-*, significantly below the sensor noise floor. As a result, the dark current's impact can be considered negligible.

4.6 Summary

Table 4 - 3 summarizes the performance of the four simulated pixels. The comparison shows that only variant 3 and variant 4 are suitable candidates for this project. Consequently, in the next chapter, the design of an ultra-high speed burst mode image sensor will be based on these two variants. In the remainder of this thesis, variant 3 and variant 4 will be respectively referred to as the baseline pixel and the high-conversion-gain (HCG) pixel.

Pixel Performance Comparison					
	Transfer Time (ns)	Image Lag (%)	CG (μv/e)	SF Noise (μV)	Full Well Capacitary (e-)
Variant 1	<10	<0.5	<10	374	>>10000
Variant 2	>12	>>0.5	93	374	~ 10000
Variant 3	<12	<0.5	138	374	~ 7000
Variant 4	<12	<0.5	178	~374	~ 5500

Table 4-3 Performance comparison between 4 variants of pixel

5 System Design and Simulation of Burst Model CIS

5.1 System Architecture

As mentioned in the previous chapter, one of the distinguishing features of the ultra-fast burst mode image sensor, compared to the normal continuous mode image sensor, is its in-pixel storage capability. To accommodate at least 100 recording lengths, each pixel requires a minimum of 100 sample/hold capacitors. Considering that the pixel's active area measures 20 μm × 20 μm, Figure 5-1 illustrates the initial pixel floorplan with a recording capability of 108 frames..

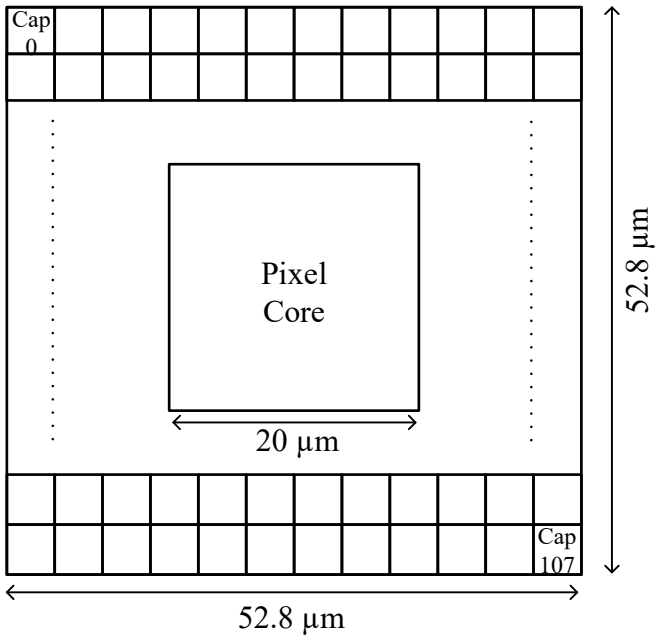


Figure 5-1 Initial floorplan for the pixel

In this prototype chip, the signal flow is straightforward. The pixel output voltage will be directly buffered out to the receiver without on-chip analog-to-digital conversion. Hence, the analog column readout circuit can be as simple as unity gain buffers. The remaining circuits of this chip will be peripheral, such as the pixel row drivers, pixel

memory drivers, current references, and pad frame. Figure 5-2 depicts the block diagram of the signal flow in this sensor.

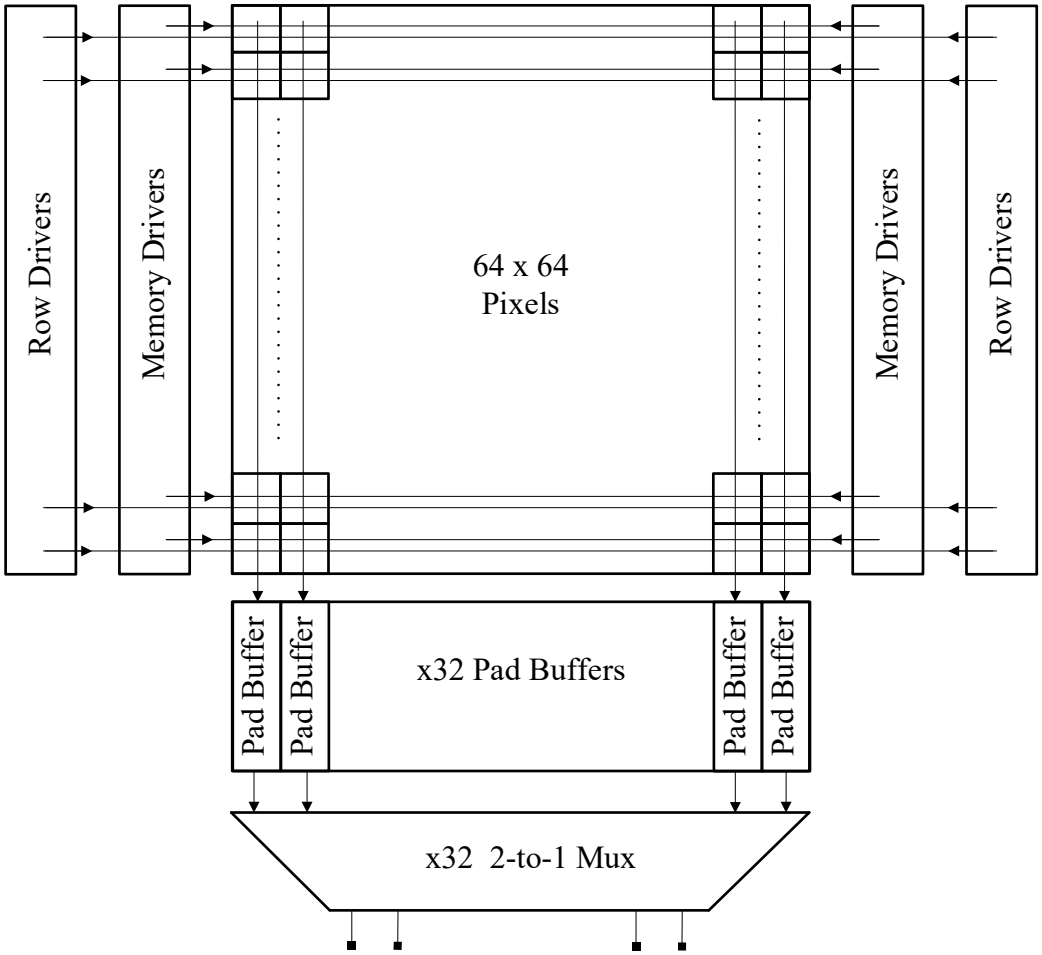


Figure 5-2 Block diagram illustrating the signal flow within this sensor

Based on my several years of industry experience, it is easy to estimate the aspect ratio and area of each major block. Consequently, the initial floorplan of the sensor is depicted in Figure 5-3. However, due to the foundry's multi-project-wafer (MPW) limitation, the size of the die is restricted to 6400 µm x 4500 µm. The pad frame consists of a total of 208 pads, with power, ground, and reference voltage pads grouped on both sides to minimize routing resistance. In order to ensure noise isolation and symmetric propagation delay [60], the digital input controls are grouped on the top side of the pad

frame and buffered to two sides. Analog outputs, on the other hand, are grouped on the bottom side of the pad frame. The subsequent sections of this chapter will provide details of each major building block of the sensor.

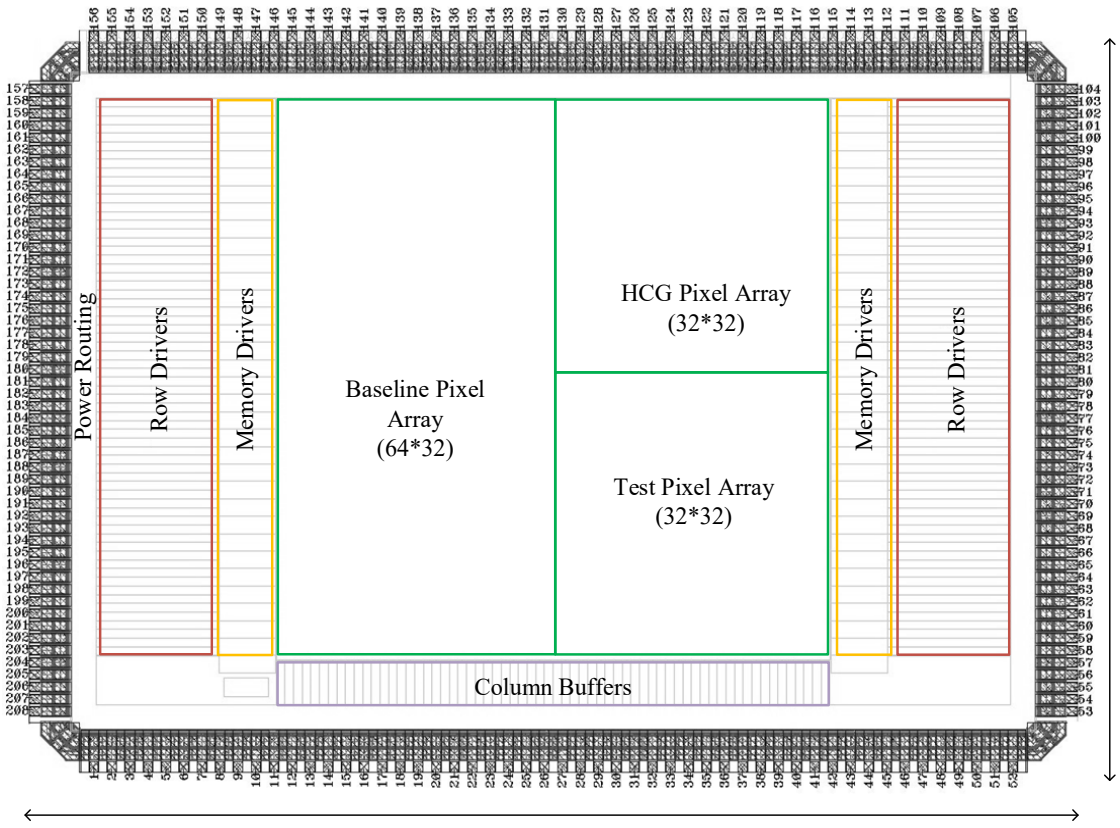


Figure 5-3 Proposed sensor floorplan

5.2 Pixel

5.2.1 In-Pixel CDS Circuit

Similar to most CMOS image sensors, even for QIS [52], the pixel noise is typically dominated by in-pixel SF thermal and flicker noise, assuming no charge transfer noise [55]. To suppress low-frequency noise from pixel source follower, pixel reset KT/C noise, and fixed-pattern noise (FPN) in image sensors, the correlated-double-sampling (CDS) circuit was introduced [56]. Equation 5-1 [57] represents the transfer function.

$$H_{CDS}(f) = 2 \times \sin(\ \pi \times f \times \Delta t) \qquad (5-1)$$

where Δt refers to the time difference between CDS circuit sampling rest (V_{rst}) and sampling signal (V_{sig}), as Figure 5-4 shows. In this project, as this time interval (Δt) is typically in the range of a few tens of nanoseconds, the low-frequency (<KHz) noise from the pixel source follower will be greatly filtered out [78].

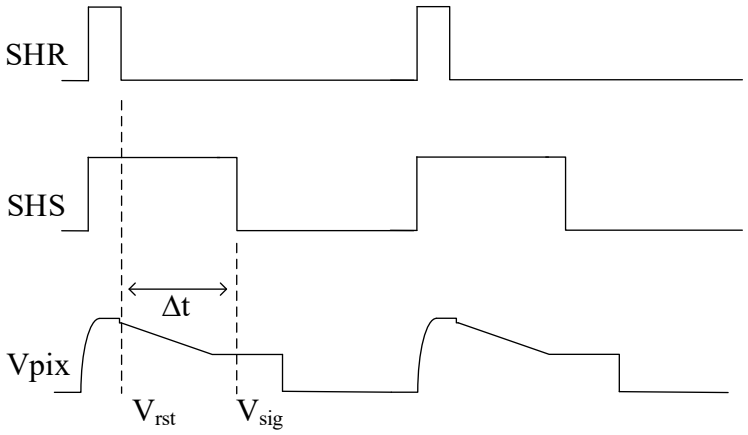


Figure 5-4 CDS Timing

Figure 5-5 depicts the double delta sampling (DDS) circuit used in [56], which uses four sample-and-hold capacitors for a complete DDS operation. Specifically, one capacitor stores the sampled V_{rst} voltage, while the other capacitor stores the sampled V_{sig} voltage, the remaining two capacitors are for AC coupling. However, for a compact CDS design where the sample and hold capacitors are placed in-pixel, this structure may not be a suitable option.

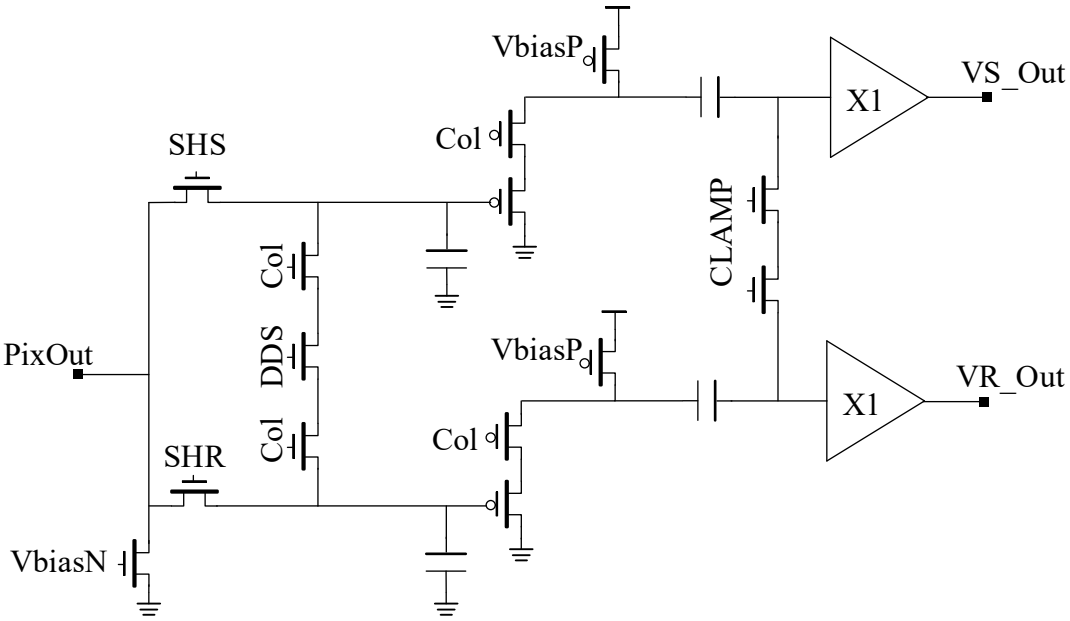


Figure 5-5 The CDS circuit, as described in [56]

Figure 5-6 illustrates the CDS circuit introduced in [58], where the AC coupling capacitor C_c serves as the CDS capacitor, and the voltage difference between V_{rst} and V_{sig} is stored on the C_{SH}. However, as Equation 5-2 indicates, this configuration unavoidably causes significant attenuation in the signal path, leading to an increase in input-referred noise [72].

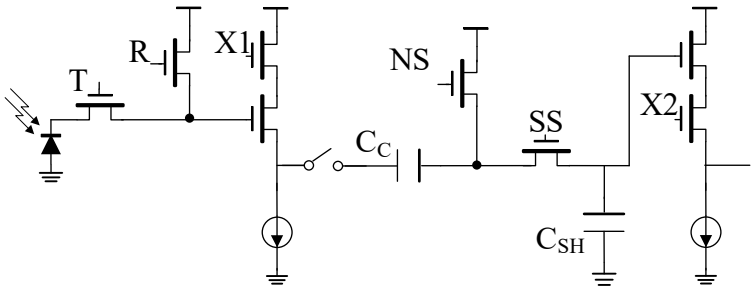


Figure 5-6 The CDS circuit, as described in [58]

$$Attenuation = \frac{C_C}{C_C + C_{SH}} \qquad (5-2)$$

The CDS circuit [59] in Figure 5-7 is implemented in this project to minimize the voltage gain attenuation in the signal chain. Specifically, the C_{SH} is positioned at the output of the first-stage source-follower instead of the input of the second-stage source-follower, as described in [58]. This arrangement reduces the voltage attenuation in the signal chain to $C_{CDS}/(C_{CDS}+C_P)$, where C_{CDS} represents the AC CDS capacitor, and C_P represents the parasitic capacitor. It is worth noting that C_P is significantly smaller than C_{CDS}.

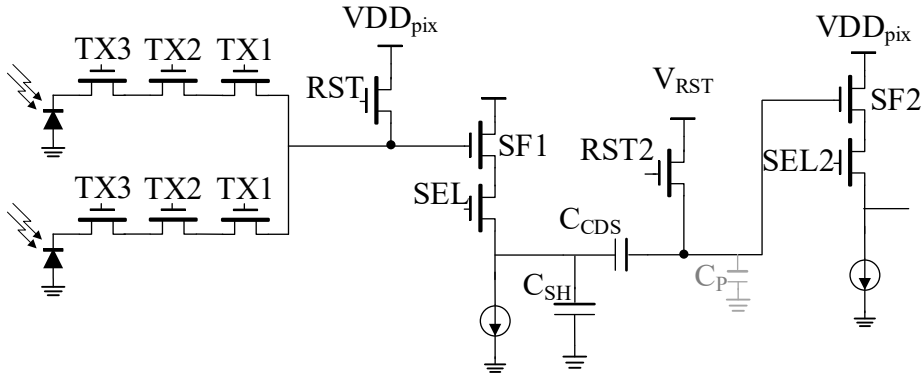


Figure 5-7 The CDS circuit proposed in this project

The operational timing of the CDS circuit is illustrated in Figure 5-8. In this circuit, the pixel reset voltage V_{rst} is sampled by the falling edge of RST2, while the voltage difference between the pixel reset voltage V_{rst} and the signal voltage V_{sig} is sampled by the falling edge of SAMP. The sampled voltage is stored in a sample and hold capacitor.

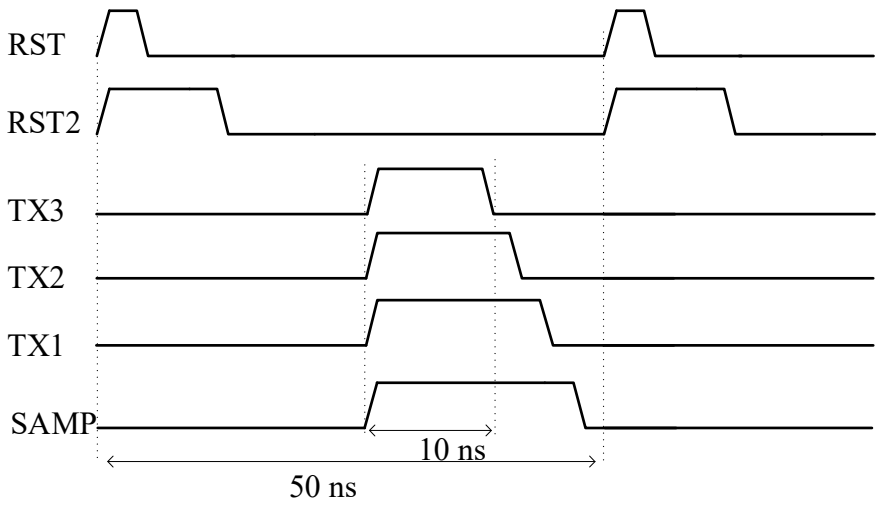


Figure 5-8 CDS operation timing

The following section will elaborate on the 1.8 V thin gate sample/hold capacitor bank. In order to safeguard the 1.8 V thin gate devices while operating in a 3.3 V environment, the V_{RST} voltage is segregated from VDDpix and can be autonomously adjusted. Typically, the V_{RST} voltage is set to $1.8+V_{GS\_SF2}$ to ensure that the SF2's maximum output voltage remains below 1.8 V.

5.2.2 In-Pixel Storage and Switches Network

For design simplicity and durability in a 3.3 V environment, it is advisable to use thick-gate 3.3 V devices. However, using thick gate 3.3 V NMOS capacitors results in a lower capacitance density, typically ranging from 0.25 to 0.5 of that of 1.8 V thin gate NMOS capacitors, and an increase in thermal noise due to the difference in dielectric layer thickness.

To address this issue, this pixel employs 1.8 V NMOS capacitors in the sample and hold capacitor bank. The schematic in Figures 5-9 (a) illustrates a sample-and-hold pair consisting of two 1.8V NMOS capacitors and two 3.3V NMOS switches. This combination is chosen to ensure layout symmetry and best linearity.

In order to increase the capacitance density, a customized Metal-1 (M1) Metal-Oxide-Metal (MOM) capacitor is positioned on the poly gate of the NMOS capacitor. Moreover, a Metal-2 (M2) layer is added as a shielding layer above the M1 MOM capacitor, as shown in Figure 5-9 (b). This design allows for the accommodation of 108 units of sample and hold capacitors, each with a capacitance of 78 fF, within a 52.8 µm pixel in the final layout.

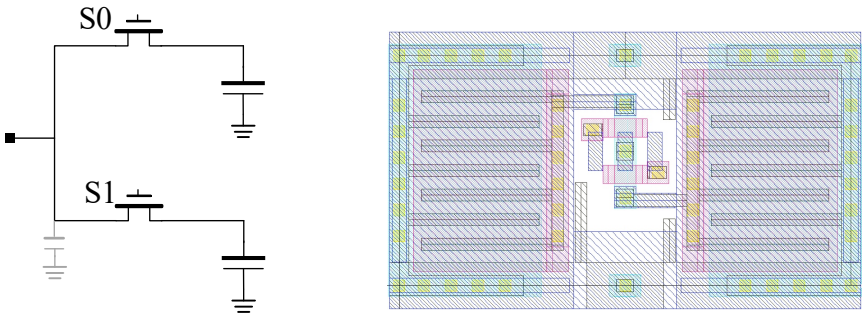
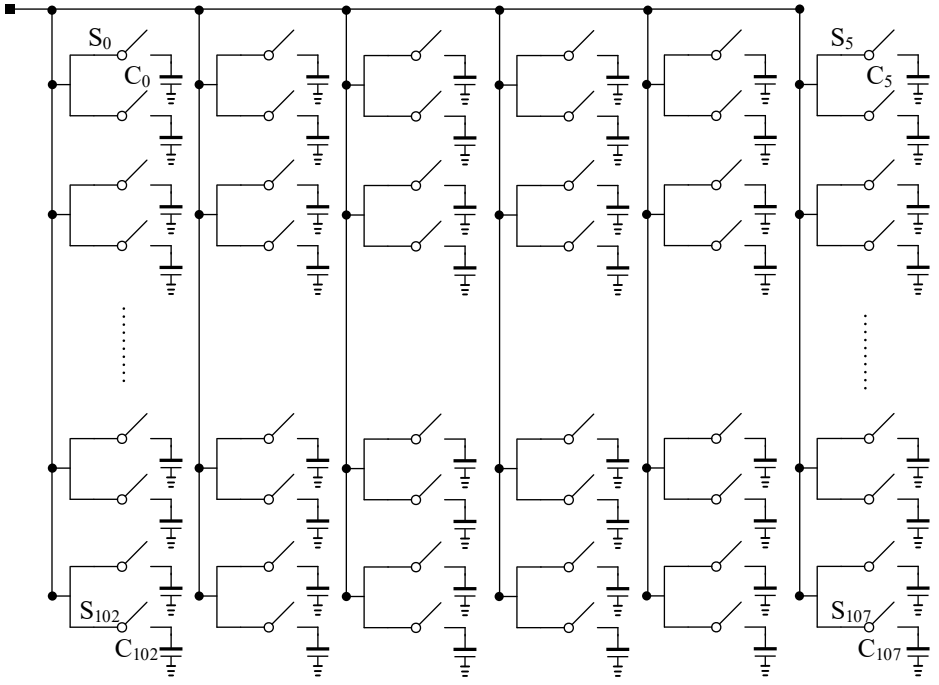


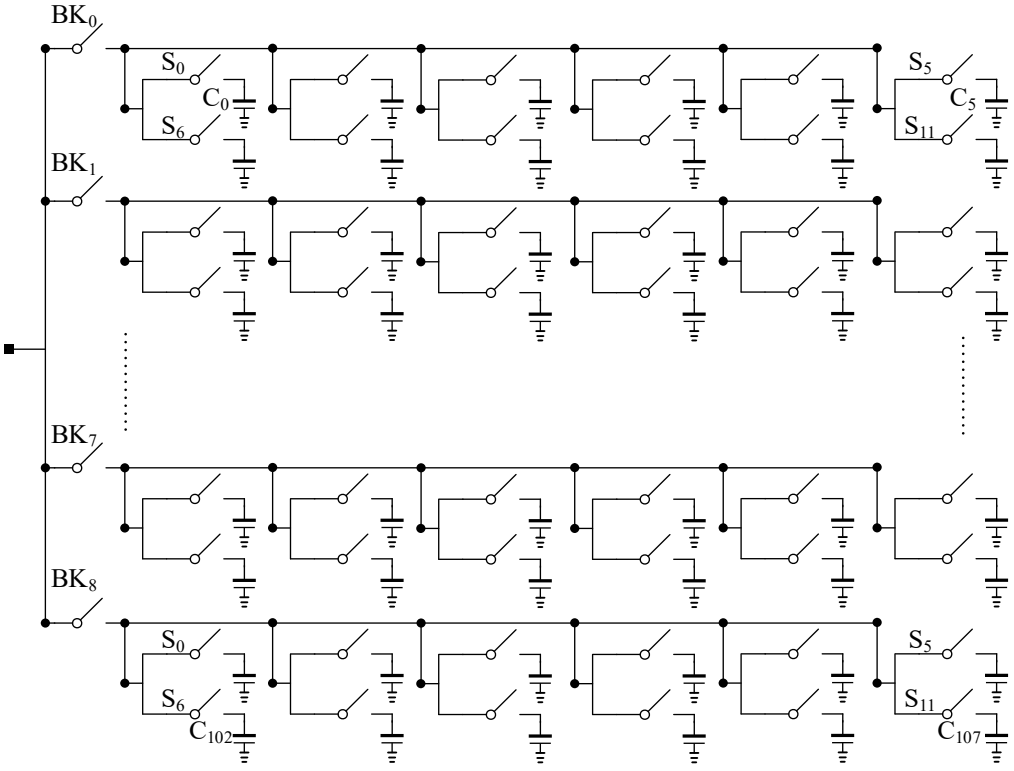
Figure 5-9 (a) schematic and (b) layout of in-pixel storage unit

The junction and parasitic capacitance (C_p) at drain node in an NMOS switch is approximately 1fF. Connecting all 54 sample-and-hold pairs (108 units) directly would result in significant parasitic capacitance being added to the SF2 loading, ultimately slowing down its settling behavior, as shown in Figure 5-10 (a).

Figure 5-10 (b) illustrates a purposed hierarchical switches network. This network divides the 108 units into 9 capacitor banks, each bank consisting of 12 sample-and-hold units and shared control signals S_0 to S_{11}. The connectivity of all 9 banks is ensured through bank switches, BK_0 to BK_8.



(a)



(b)

Figure 5-10 In-pixel storage network with (a) direct connection and (b) hierarchical connection

The hierarchical network illustrated in Figure 5-10 (b) is usually sufficient provided that the C_P of a NMOS switch is significantly smaller than that of the sample-and-hold capacitor (C_{SH}), and the drain node PN junction's leakage current is negligible. However, in this process, the leakage current is considerably high, and capacitance of C_P and C_{SH} are on the same order. Sharing control signals among different sample-and-hold units as depicted in Figure 5-10 (b) introduces extra image artifacts caused by charge sharing and voltage-dependent leakage. Unfortunately, these artifacts are hardly correctable though post-processing. Figure 5-11 displays an example of this artifact, where C_{107} in Figure 5-10 (b) is accessed multiple times before the actual $Frame_{107}$ readout, resulting in charge corruption on C_{107}.

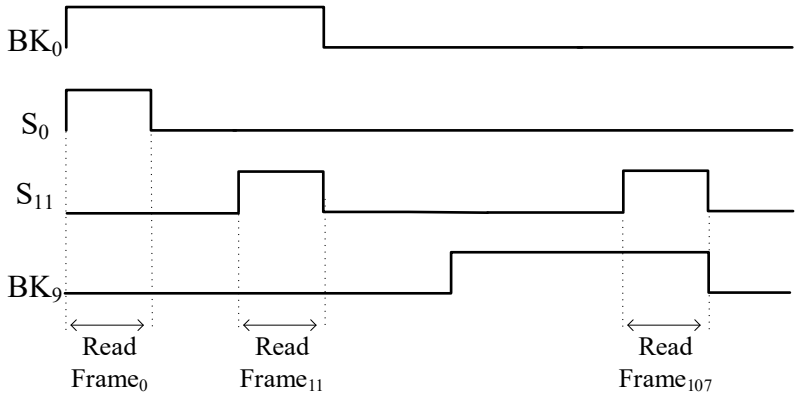


Figure 5-11 An example of corrupted stored charge

To address the aforementioned concerns, this project utilizes a storage network featuring hierarchical switches and individual controls, as depicted in Figure 5-12. The 108 units are divided into 10 capacitor banks, with each bank containing either 12 or 6 units controlled by BK_0 to BK_9. Furthermore, each unit is equipped with its own control line, denoted as S_0 to S_{107}. This design combination effectively overcomes process imperfections and enables the rapid and secure sampling and storage of pixel

information. However, it is important to note that accommodating the 108 individual control signals within the 52.8 μm pitch pixel, using the 180 nm process, poses a significant challenge in layout. Sophisticated layout skills and meticulous calculations are necessary to ensure all control lines fit within the tight pitch without obstructing the pixel photodiode.

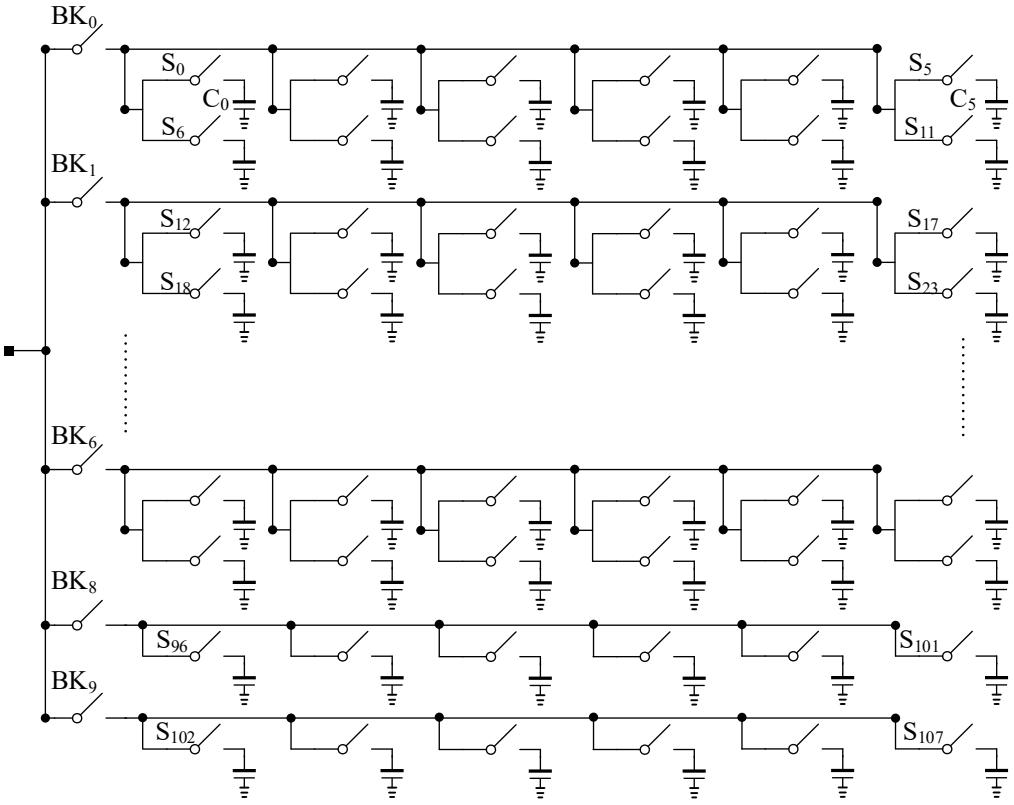


Figure 5-12 The in-pixel storage network used in this project

The complete schematic of one pixel, which includes the pixel core, in-pixel correlated double sampling (CDS), in-pixel sample and hold network, and column output buffer, is illustrated in Figure 5-13. The components are arranged in a 52.8 μm pitch, and the final layout of the pixel is shown in Figure 5-14.

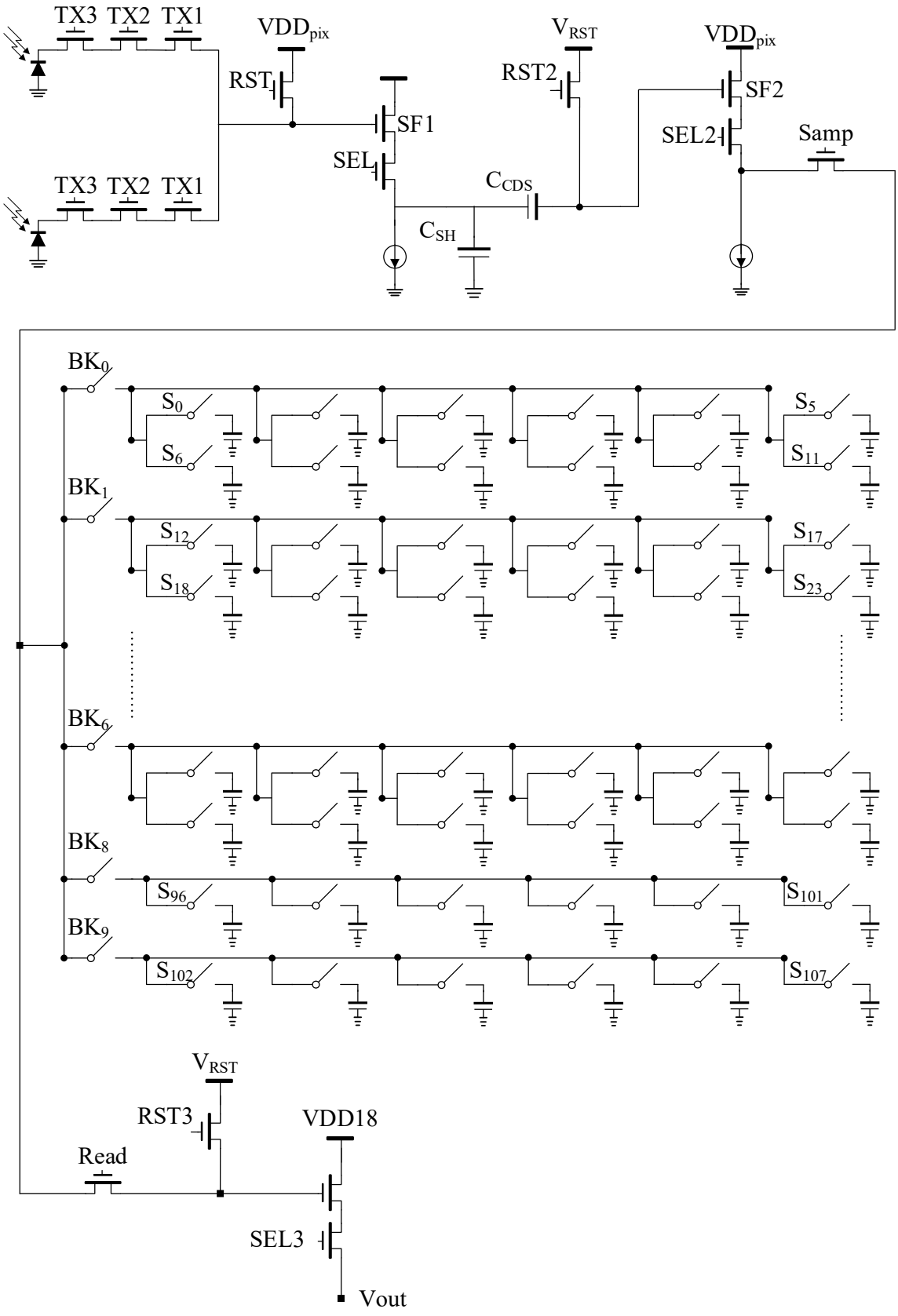


Figure 5-13 The complete schematic of one pixel in this sensor

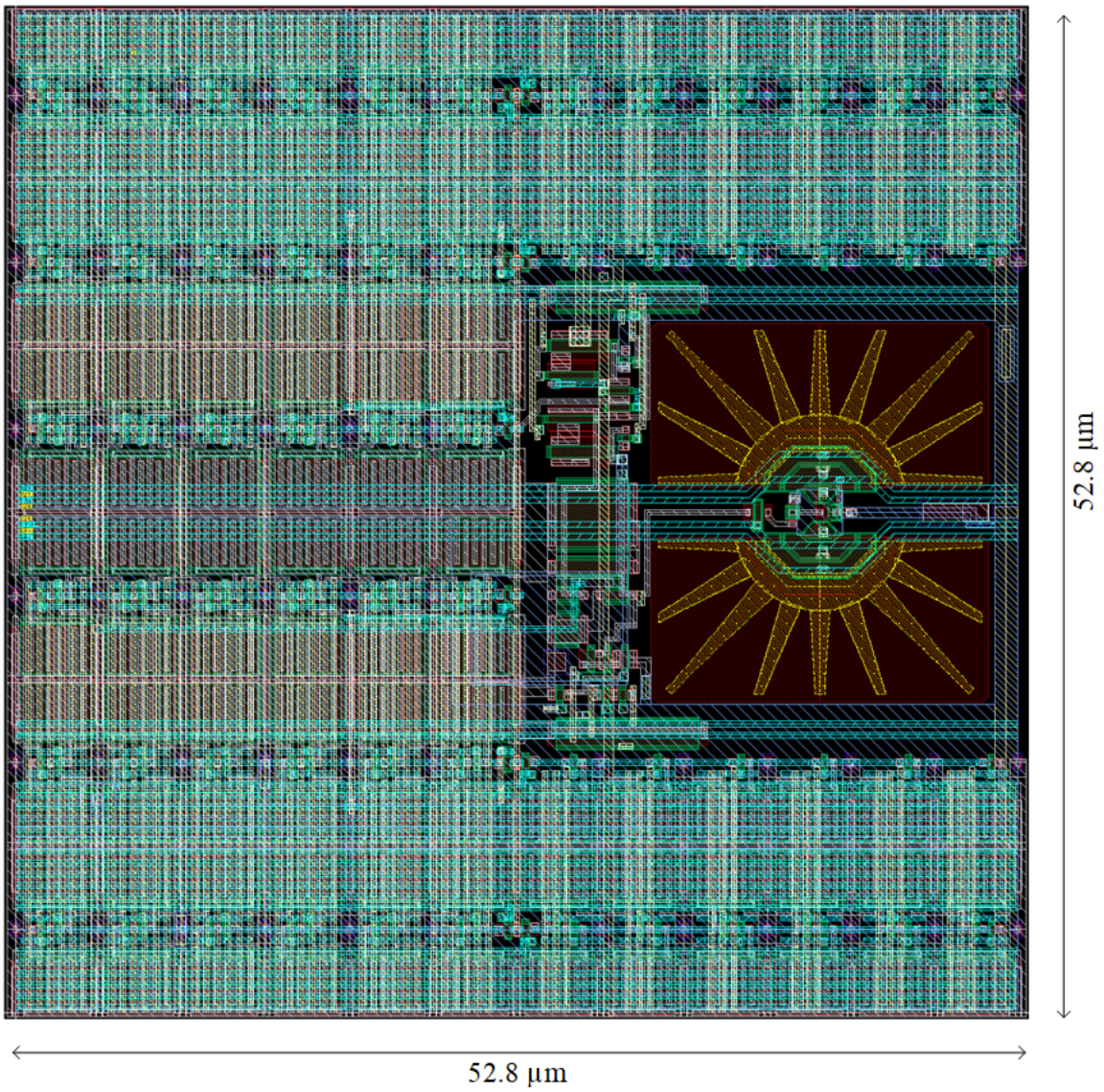


Figure 5-14 The layout of final pixel

5.3 Column Readout Circuit

In the subsequent sections, the input-referenced noise of the sensor, which is mainly dominated by the in-pixel source follower and sample-and-hold capacitor, will be further elaborated. The noise originates from the preceding stage of the column readout circuit. Therefore, incorporating a programmer-gain-amplifier (PGA) will not alleviate the input-referenced noise [61]. To simplify the column readout circuit, a straightforward

unit-gain buffer is employed. This buffer directly receives the pixel's Vout voltage, as shown in Figure 5-13, and drives the output pad.

Figure 5-13 illustrates that the Vout voltage can reach a maximum of 1.8V, which is the same as the power supply voltage of in-pixel 3rd stage source follower. To avoid potential headroom problems, a NMOS input pair is required when powering the unity-gain buffer with 1.8V. However, without an auto-zero or CDS circuit, NMOS input-pair based amplifier is believed to have greater flicker noise than PMOS one, as indicated by reference [62]. To balance design simplicity and noise performance, this project uses a 3.3V unit-gain-buffer with a PMOS input pair, as presented in Figure 5-15.

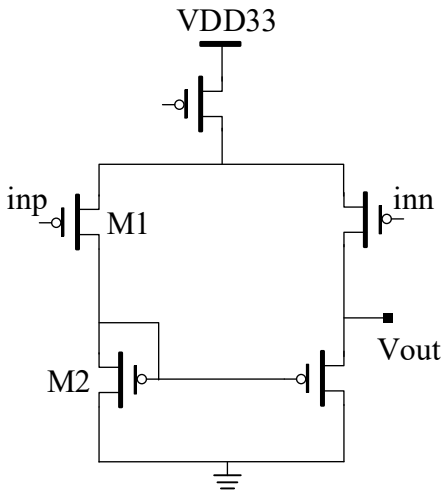


Figure 5-15 Schematic of column readout buffer

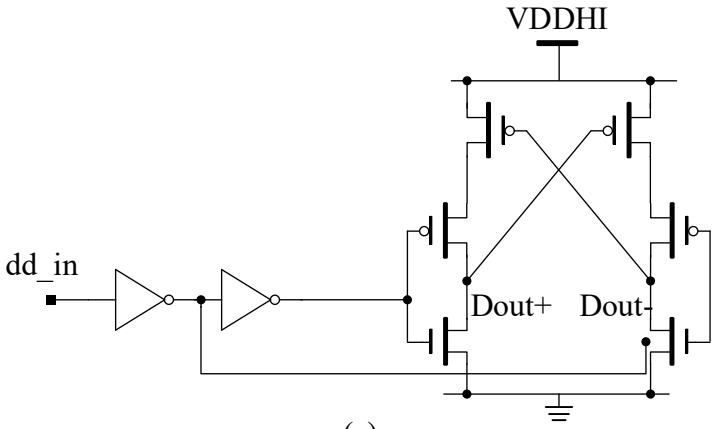
5.4 Row-Driver Circuit

Small negative voltage applied to the charge transfer gate is discovered during the CCD era [63, 64, 65] to help suppress surface state at the transfer channel and reduce the dark current of the image sensor. Additionally, as depicted in Figure 4-22, the positive voltage applied to the charge sweep transfer gate is typically above the 3.3V supply. Thus, to drive the charge sweep transfer gate, the row-driver circuit must be capable of

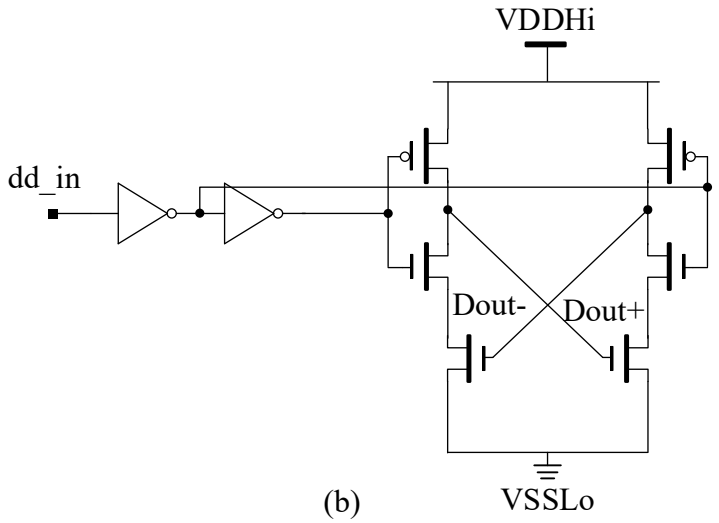
producing an output swing higher than 3.3V and lower than 0V. To optimize pixel performance, a voltage level shift-up and shift-down circuit are required.

Inspired by [66], the level shifter circuits are utilized in the row driver circuit, as depicted in Figure 5-16 (a) and (b). In Figure 5-16 (a), the 3.3V input control (dd_in) is buffered and converted into complementary signals, which are employed to drive the shift-up circuit. In the output stage, both the PMOS and NMOS transistors experience a higher V_{DS} voltage than their rated value. Consequently, it is essential to increase the size of these transistors in a relatively longer and wider manner to ensure durability.

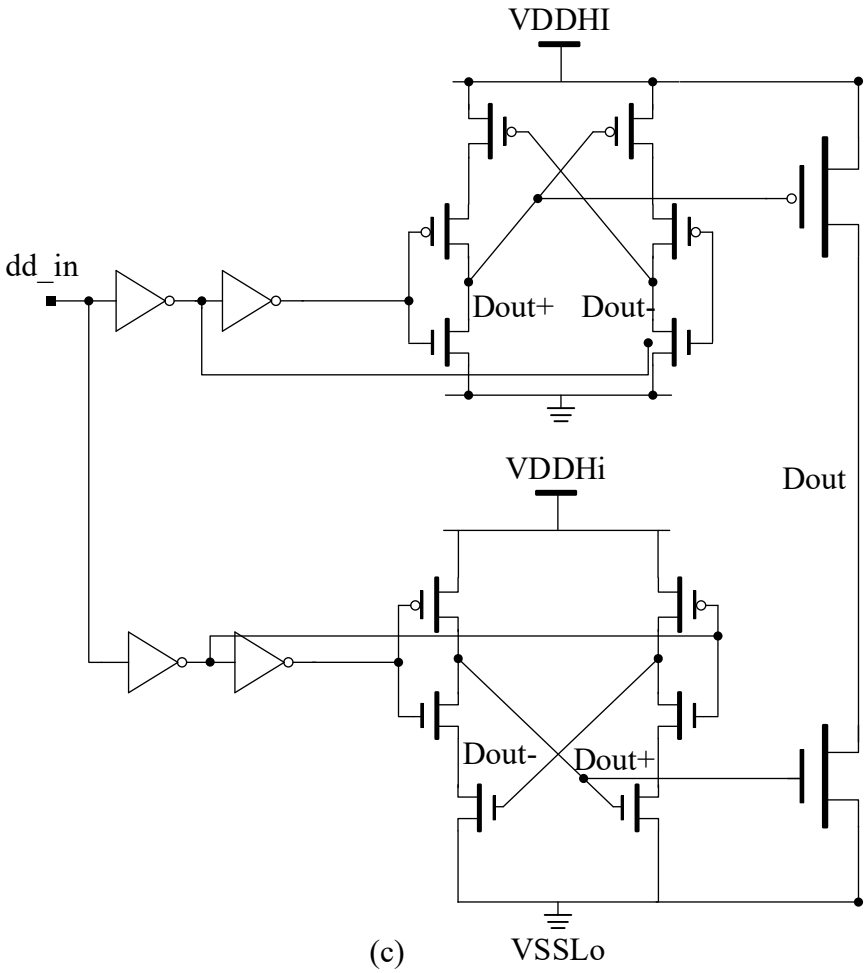
The circuit shown in Figure 5-16 (b) converts a 3.3 V input control (dd_in) into complementary signals for driving the shift-down circuit. It is important to note that in order to avoid forward biasing the body-to-source PN junction caused by the negative voltage (VSSLo) in this circuit, the NMOS in the output stage should be positioned in a deep-n-well [67].



(a)



(b)



(c)

Figure 5-16 Schematic of: (a) level shift-up circuit, (b) level shift-down circuit and (c) row driver unit

5.5 Built-in Test Circuit

In addition to the major building blocks discussed in the previous chapter, this sensor also has several built-in test (BIT) circuits. These circuits include the pixel-direct injection circuit, which bypasses the real pixel circuit and injects a known test voltage into the pixel output, as well as the analog-test-bus circuit, which directly probes the internal analog voltage or current, and the digital-test-bus circuit, which directly probes the internal digital waveform. However, the details regarding these BIT circuits exceed the scope of this thesis and will not be further discussed.

5.6 Digital Blocks

To meet the deadline for the foundry's multi-project-wafer (MPW) shuttle, this project has only four and a half months to complete the design, verification, and tape out. In order to minimize design risks within this tight timeframe, the main digital blocks, including the frame-timer, register-space, data-acquisition, and serial-communication, have been implemented in an off-chip FPGA after the tape-out. These specific blocks will not be discussed in this thesis.

5.7 Sensor Timing

Figure 5-17 illustrates the operation timing of the proposed image sensor. As mentioned earlier, the desired frame rate is 20 million frames per second (20Mfps), and the preliminary frame time is set to 50 ns. It is important to note that the TX3 pulse width fixed at 10 ns, as shown in Figure 4-22 (a), allowing the pixel to integrate for 40 ns. The row readout time is tentatively set to a minimum of 150 ns, but this value may be adjusted based on the speed of the off-chip ADC and the leakage of the sample-and-hold bank.

Being a burst mode image sensor, it first samples all 108 frames of the image before reading out the stored images. It is estimated that one cycle will take approximately 1.04 ms.

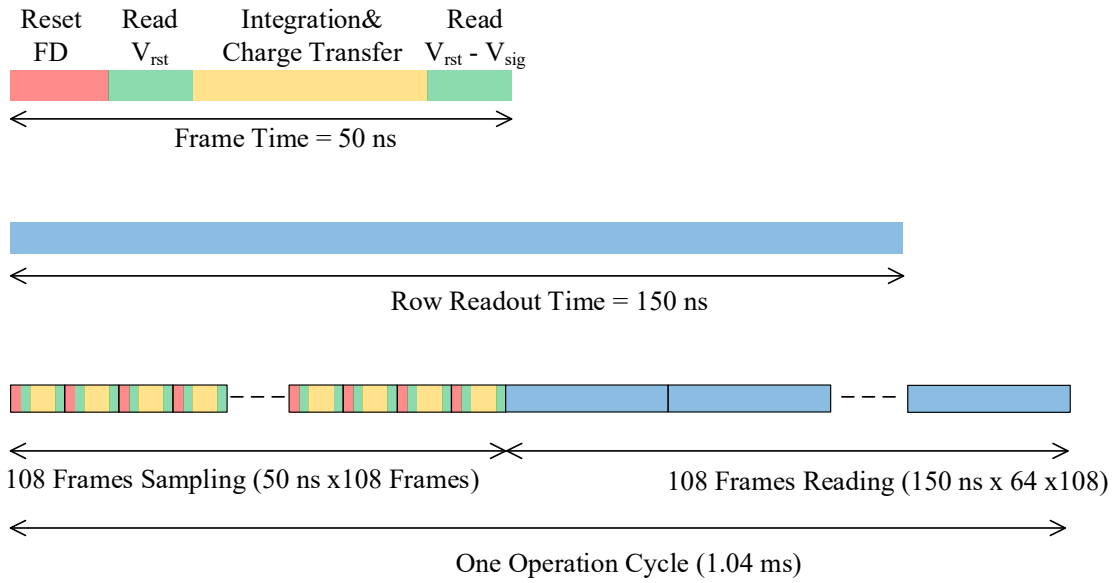


Figure 5-17 Sensor operation timing

5.8 Power Estimation

Unlike the continuously mode image sensor, the proposed one does not require a high-speed data transmitter, thus significantly reducing its overall power consumption. Table 5-1 illustrates the estimated whole chip power consumption based on the timing diagram presented in Figure 5-17, which is estimated to be 147 mW.

Blocks	Current (uA)	Unit	Duty Cycle	Supply (V)	Power (mW)	Percentage
In Pixel 1st stage SF	25	4096	0.005	3.3	2	1%
In Pixel 2nd stage SF	25	4096	0.005	3.3	2	1%
In Pixel 3rd stage SF	25	64	0.995	3.3	5	4%
Col Readout Buffer	500	64	0.995	3.3	105	71%
Row Drivers	24000	2	0.005	3.3	1	1%
Mis Dig Buffers	10000	1	1.000	3.3	33	22%
Total					147	

Table 5-1 Power consumption estimation

5.9 Noise Estimation

Despite the higher pixel conversion gain designed for this image sensor, it is still important to carefully estimate and analyze the signal chain noise. Therefore, a simplified signal chain schematic, highlighting major noise contributors in red, is presented in Figure 5-18 for the purpose of noise analysis.

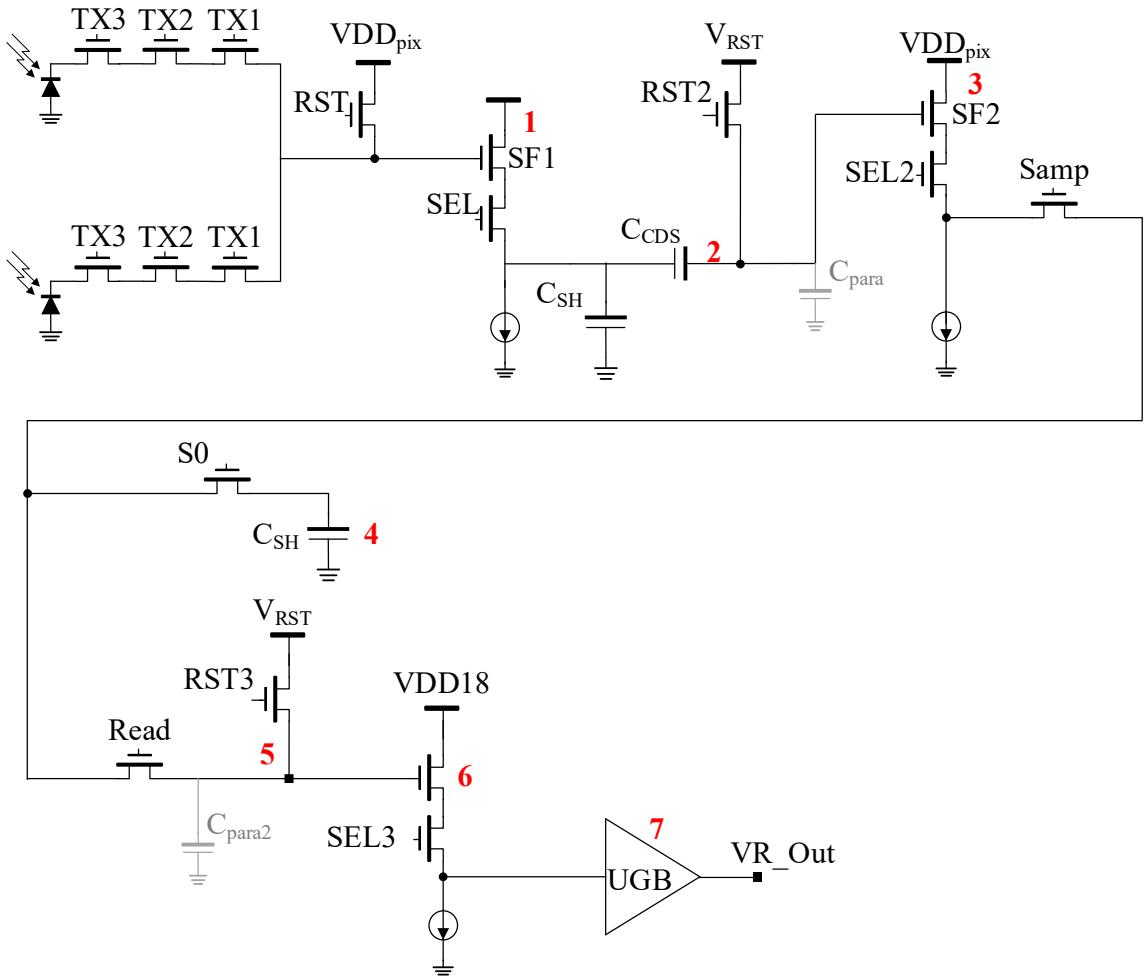


Figure 5-18 Simplified sensor signal chain

Contributor 1 stands for the flicker noise and thermal noise from in-pixel 1st stage source follower (SF1). [52] did detailed measuring and validation of flicker noise model for TSMC process and find out that Hooge mobility fluctuation mode matched experimental measurements. Even though a different process is used in this design, the model can still be used for quick calculation. The normalized power spectrum density (PSD) of flicker noise is as Equation 5-3 shows [52].

$$\frac{S_{I_{b\_flicker}(f)}}{I_b^2} = \frac{\alpha_H}{f} \times \frac{2q}{C_{ox}WL \times (V_{GS} - V_{th})} \qquad (5-3)$$

The SF biasing current is represented by I_b. Hooge's parameter is denoted by α_H, while C_{ox} refers to the oxide capacitance per unit area. The transistor width and length are represented by W and L, respectively. The gate-source voltage is denoted by V_{GS}, and the threshold voltage is represented by V_{th}. Based on the classical semiconductor theory, Equation 5-4 presents the thermal noise spectrum of a SF, where g_m denotes the transconductance of the source follower, r represents the excess noise factor, and k is Boltzmann's constant.

$$s_{I_{b\_thermal}(f)} = 4kTrg_m \qquad (5-4)$$

Considering the limited bandwidth of a SF, the transfer function of in-pixel SF can be regarded as a low-pass filter, which is illustrated by Equation 5-5, where f_c represents the cutoff frequency.

$$H_{LP(f)} = \sqrt{\frac{1}{1+(f\,/\,f_c)^2}} \qquad (5-5)$$

Hence, the overall noise voltage contribution from contributor 1 at its output can be derived by combining equations 5-5, 5-4, 5-3, and 5-1, resulting in Equation 5-6, where A_{SF} is the source follower gain.

$$V_{n1}^2 = \int_0^\infty \frac{s_{I_{b1\_thermal}(f)} + s_{I_{b1\_flicker}(f)}}{g_{m1}^2} \times A_{SF1}^2 \times H_{LP1(f)}^2 \times H_{CDS}^2(f) \qquad (5-6)$$

Contributor 2 represents the KTC noise caused by the Brownian motion of carriers in the RST2 switch. According to classical theory, Equation 5-7 [69] gives the kTC voltage noise, where C denotes the capacitance of the CDS capacitor (C_{CDS}).

$$V_{n2}^2 = \frac{kT}{C} \qquad (5-7)$$

Contributor 3 represents the flicker noise and thermal noise generated by the in-pixel 2nd-stage source follower (SF2). It is worth noting that due to the absence of CDS noise cancellation, a relatively larger transistor size is required to reduce the flicker noise. Its overall noise contribution is similar to that of contributor 1, as presented in Equation 5-8.

$$V_{n3}^2 = \int_0^\infty \frac{S_{I_{b2\_thermal}(f)} + S_{I_{b2\_flicker}(f)}}{g_{m2}^2} \times A_{SF2}^2 \times H_{LP2(f)}^2 \qquad (5-8)$$

Contributor 4 denotes the kTC noise attributed to the Brownian motion of carriers within the sample-and-hold switch. Like contributor 2, we can derive the voltage noise of this noise source using Equation 5-9, where C_{SH} represents the capacitance of the sample-and-hold capacitor.

$$V_{n4}^2 = \frac{kT}{C_{SH}} \qquad (5-9)$$

Contributor 5 represents the kTC noise that arises from the RST3 switch. However, this noise will be attenuated by the sample-and-hold capacitor. The equivalent total noise at the sample-and-hold capacitor can be determined using Equation 5-10.

$$V_{n5}^2 = \frac{kT}{C_{para2}} \times \left(\frac{C_{para2}}{C_{para2} + C_{SH}}\right)^2 \qquad (5-10)$$

Contributor 6 represents the flicker noise and thermal noise generated by the in-pixel 3rd-stage source follower (SF3). Like contributor 3, its overall noise at output is given by Equation 5-11.

$$V_{n6}^2 = \int_0^\infty \frac{S_{I_{b3\_thermal}(f)} + S_{I_{b3\_flicker}(f)}}{g_{m3}^2} \times A_{SF3}^2 \times H_{LP3(f)}^2 \qquad (5-11)$$

Contributor 7 represents the thermal noise generated by the column output buffer. Due to the relatively larger size of the input pair, its contribution to flicker noise is negligible. The total output noise of the buffer can be determined using Equation 5-12.

$$V_{n7}^2 = 2(4kTrg_{m1} + 4kTrg_{m2}) \times R_{out}^2 \times BW^2 \qquad (5-12)$$

where g_{m1} denotes the transconductance of input pairs M1 in Figure 5-15, g_{m2} denotes the transconductance of current mirror M2 in Figure 5-15, R_{out} is the output impedance of the buffer and BW stands for the bandwidth of column output buffer.

The total output voltage noise of the entire image sensor can be estimated using Equation 5-13. It is important to note that in this calculation, any additional bandwidth limiting introduced by later stages has been ignored for quick calculation.

$$\begin{aligned} V_{n_{output}}^2 = {} & V_{n1}^2 \times A_{CDS}^2 \times A_{SF2}^2 \times A_{SH}^2 \times A_{SF3}^2 \times A_{UGB}^2 \\ & + V_{n2}^2 \times A_{SF2}^2 \times A_{SH}^2 \times A_{SF3}^2 \times A_{UGB}^2 + V_{n3}^2 \times A_{SH}^2 \times A_{SF3}^2 \times A_{UGB}^2 \\ & + V_{n4}^2 \times A_{SF3}^2 \times A_{UGB}^2 + V_{n5}^2 \times A_{SF3}^2 \times A_{UGB}^2 + V_{n6}^2 \times A_{UGB}^2 \\ & + V_{n7}^2 \qquad (5-13) \end{aligned}$$

The variables used in this equation include A_{CDS}, which represents the voltage attenuation introduced by the CDS capacitor, A_{SF2}, the low frequency gain of the 2nd stage source follower, A_{SH}, the attenuation introduced by the sample-and-hold capacitor and C_{para2}, A_{SF3}, the low frequency gain of the 3rd stage source follower, and A_{UGB}, the low frequency gain of the column output buffer.

The Spectre AC noise simulation is used for quick noise estimation. Table 5-2 presents the simulated values for V_{n1} to V_{n7} and the gain of each stage. Based on the simulation results, the estimated output-referred noise at the pad is 414 uV root-mean-

square (rms), while the input-referred noise at the floating diffusion node is 5.8 *e*-, assuming a CG of 138 uV/*e*-. In this design, the input-referred noise is primarily influenced by the in-pixel 1st stage source follower.

Baseline Pixel Total Noise Estimation (Input Referred)					
Noise Contributor	**Cap (pF)**	**Stage Noise (uV)**	**Stage Gain (V/V)**	**Noise Contribution (uV^2)**	**Noise Percentage**
1. In-pixel 1nd Stg SF		374	0.81	213193	33%
2. Rst2 kTC	0.080	233	0.96	082819	13%
3. In-pixel 2nd Stg SF		191	0.90	074485	12%
4. S/H Cap kTC	0.078	236	0.78	113788	18%
5. Rst3 kTC		169	1.00	095849	15%
6. In-Pixel 3rd Stg SF		095	0.89	038237	6%
7. Col Output Buffer		082	1.00	028488	4%
Total Noise				804	µV rms
Total Noise @ FD				**5.8**	e-
Baseline Pixel Total Noise Estimation (Output Referred)					
Noise Contributor				**Noise Contribution (uV^2)**	**Percentage**
1. In-pixel 1nd Stg SF				50320	29%
2. Rst2 kTC				21211	12%
3. In-pixel 2nd Stg SF				17581	10%
4. S/H Cap kTC				44144	26%
5. Rst3 kTC				22623	13%
6. In-Pixel 3rd Stg SF				09025	5%
7. Col Output Buffer				06724	4%
Total Noise @ Pad				**414**	µV rms

Table 5-2 Total noise estimation based on baseline pixel by AC simulation

The AC simulations were used to estimate the total noise for the high-conversion gain (HCG) pixel as well. Although there is currently no available Simulation Program with Integrated Circuit Emphasis (SPICE) model for the newly proposed source follower, the flicker noise and thermal contribution can still be estimated using equations 5-3 and 5-4. The total noise for the HCG pixel is presented in Table 5-3.

HCG Pixel Total Noise Estimation (Input Referred)					
Noise Contributor	**Cap (pF)**	**Stage Noise (uV)**	**Stage Gain (V/V)**	**Noise Contribution (uV^2)**	**Noise Percentage**
1. In-pixel 1nd Stg SF		385	0.81	225918	34%
2. Rst2 kTC	0.080	233	0.96	082819	13%
3. In-pixel 2nd Stg SF		191	0.90	074485	11%
4. S/H Cap kTC	0.078	236	0.78	113788	17%
5. Rst3 kTC		169	1.00	095849	15%
6. In-Pixel 3rd Stg SF		095	0.89	038237	6%
7. Col Output Buffer		082	1.00	028488	4%
Total Noise				812	µV rms
Total Noise @ FD				**4.6**	**e-**
HCG Pixel Total Noise Estimation (Output Referred)					
Noise Contributor				**Noise Contribution (uV^2)**	**Percentage**
1. In-pixel 1nd Stg SF				53323	31%
2. Rst2 kTC				21211	12%
3. In-pixel 2nd Stg SF				17581	10%
4. S/H Cap kTC				44144	25%
5. Rst3 kTC				22623	13%
6. In-Pixel 3rd Stg SF				09025	5%
7. Col Output Buffer				06724	4%
Total Noise@ Pad				**418**	µV rms

Table 5-3 Total noise estimation based on HCG pixel by AC simulation

Obviously, the proposed smaller source follower benefits significantly from the short CDS interval because its flicker noise does not dominate the overall noise. This is due to the input-referred voltage noise being almost the same as the baseline pixel. Additionally, the introduction of high CG provides an advantage, resulting in the input-referred noise being approximately 20% lower in terms of electrons.

5.10 Simulation

The Cadence Virtuoso has been used to conduct extensive and detailed simulations for each building block, such as the pixel source followers, CDS circuit, column output driver, row driver, and pad frame. Table 5-4 shows the simulation and verification matrix for major blocks in this project. However, block-level simulation and verification are not in the scope of this thesis, details will not be discussed here.

Block Name	Task Description	Sch	Cext	RCext	AC	NS	TR	CRN	MC	ARR	PSS	PN
Pixel Core	Check FUNC and PERF	X		X	X	X	X	X	X	X		
Pixel CDS	Check FUNC and PERF	X		X		X	X	X	X		X	X
S/H Unit	Check FUNC	X	X				X	X	X			
Pixel Unit Top	Check FUNC and PERF	X	X			X	X	X	X		X	X
Pixel Array	Check PERF	X		X			X	X		X		
Level Shifter	Check FUNC	X	X				X	X	X			
Row Driver Unit	Check FUNC	X					X	X				
Row Drivers Array	Check FUNC		X				X	X		X		
Memory Driver Unit	Check FUNC											
Memory Driver Array	Check FUNC		X				X	X		X		
Column Output Buffer	Check PERF	X	X		X	X	X	X	X	X		
Row Decoder	Check FUNC	X	X				X	X				
Column Decoder	Check FUNC	X	X				X	X				
Biasing Generator	Check FUNC and PERF	X	X		X		X	X	X			
Signal Chain	Check PERF	X	X			X	X	X			X	X
Pad Frame	Check FUNC	X					X					
Pad Buffer	Check PERF	X		X			X	X				
Top Chip	Check FUNC	X					X					

Table 5-4 Simulation and verification matrix of this project

The table contains various simulation types and their abbreviations. Specifically, Sch stands for schematic level simulation, Cext stands for post layout simulation with extracted parasitic capacitance, RCext stands for post layout simulation with extracted parasitic capacitance and resistance, AC stands for AC simulation, NS stands for AC noise simulation, TR stands for transient simulation, CRN stands for simulation with process corners, MC stands for Monte-Carlo simulation, ARR stands for array simulation, and PSS and PN stand for periodic-small-signal simulation and periodic-small-signal noise simulation, respectively.

5.10.1 Signal Chain Simulation

As Table 5-4 indicates, simulation at the signal-chain level is crucial for verifying the sensor's performance, particularly in terms of total noise and linearity. Figure 5-19 displays the test bench configuration for transient simulation of the signal chain, which includes a detailed pixel model and column readout circuit. The results of the transient simulation are shown in Figure 5-20, where the blue curve represents the test voltage applied at the FD node, and the purple curve represents the voltage measured at the pad.

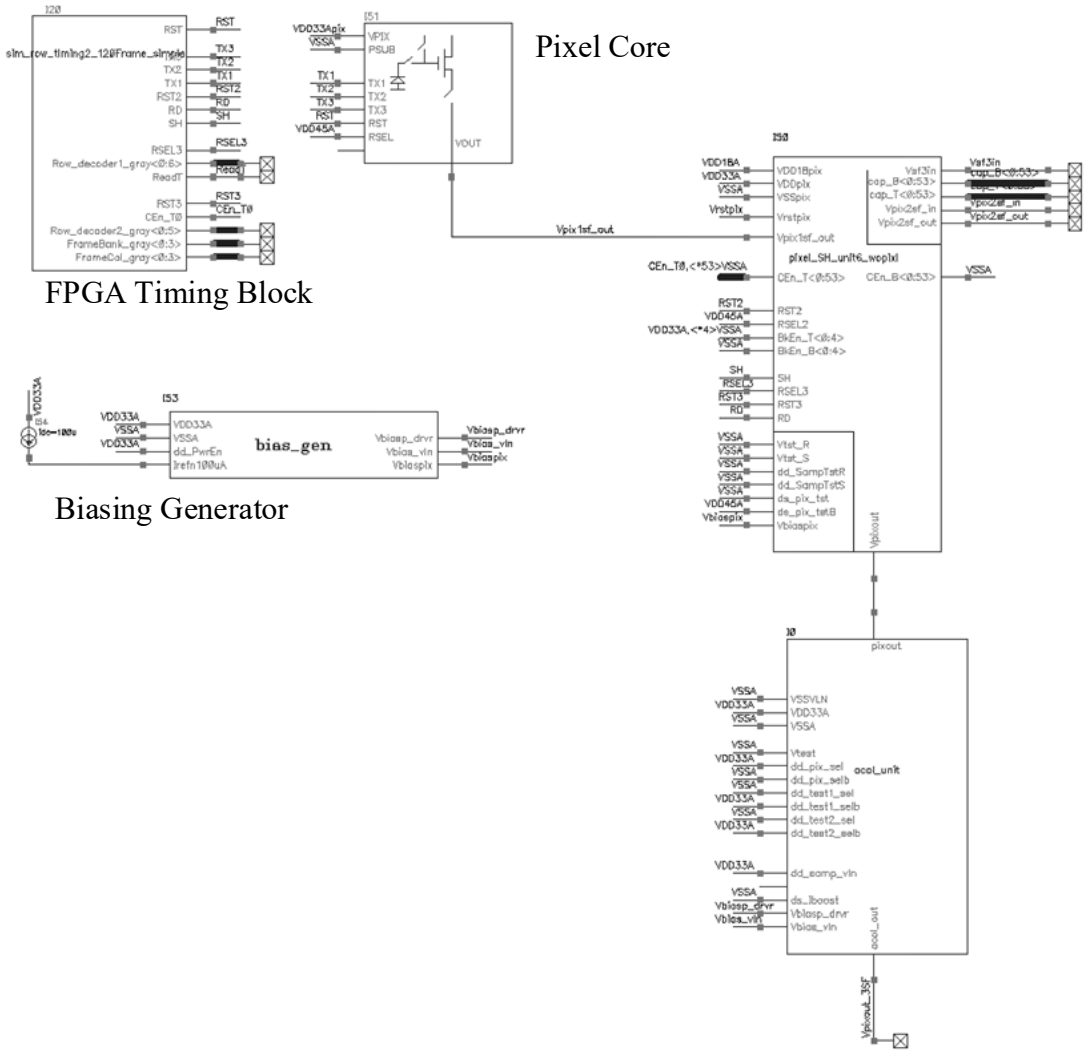


Figure 5-19 Test bench for signal chain simulation

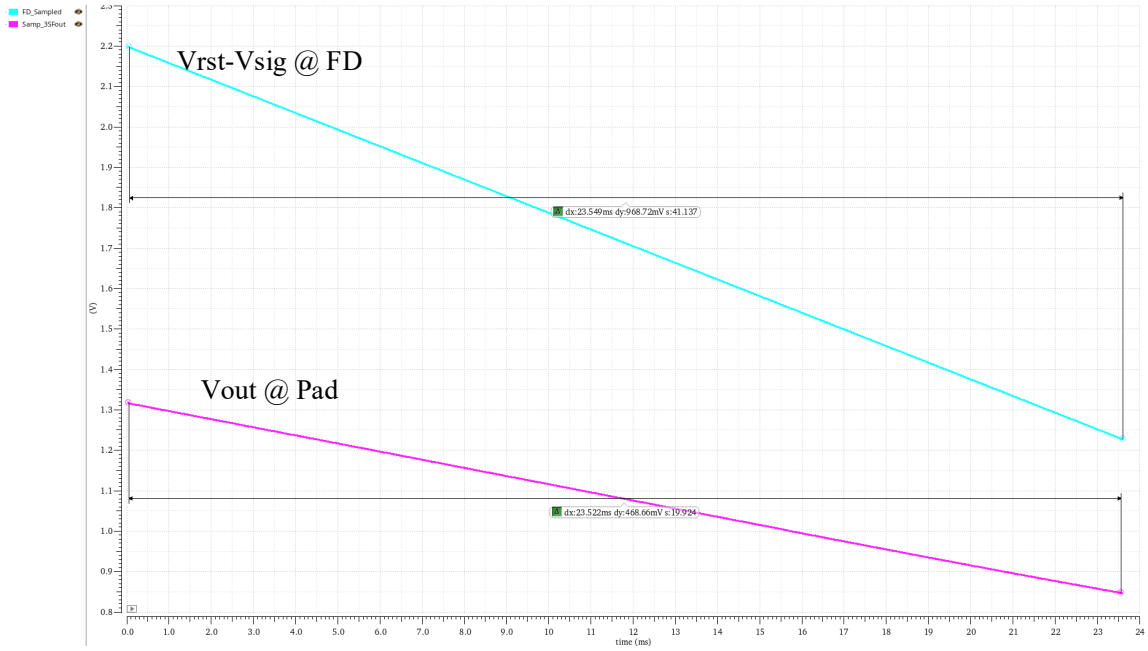


Figure 5-20 Transient simulation result of signal chain

The linearity of the entire signal chain is analyzed, and the results are presented in Figure 5-21. Despite the use of three stages of source followers in the signal chain, simulations demonstrate excellent linearity across the entire signal chain, particularly under low light conditions, with an INL of less than ±0.2%.

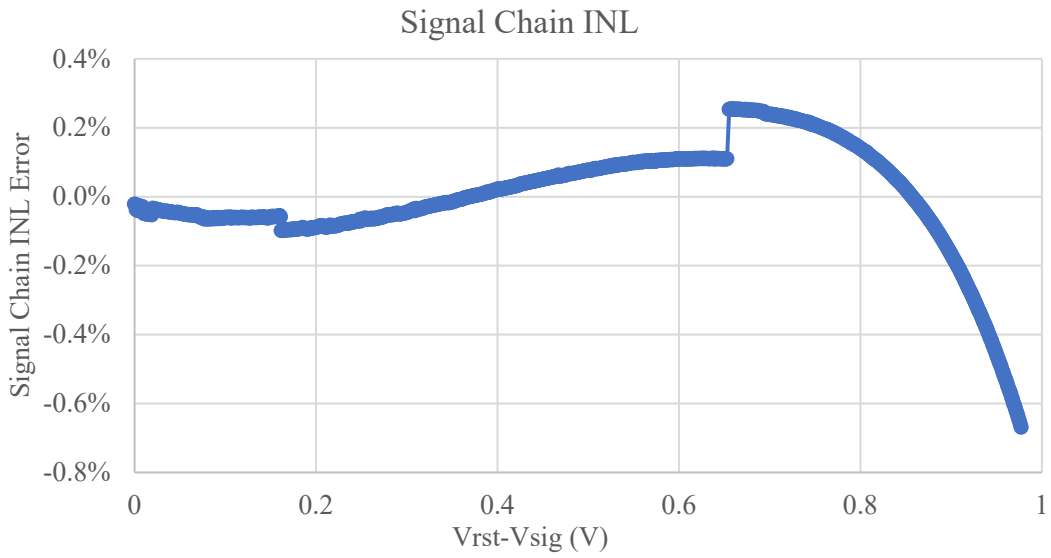


Figure 5-21 Signal chain INL simulation result

Based on the same setup in Figure 5-19, the signal chain transient noise is also simulated and the result is shown in Figure 5-22, where the red curve stands for the voltage waveform at output pad.

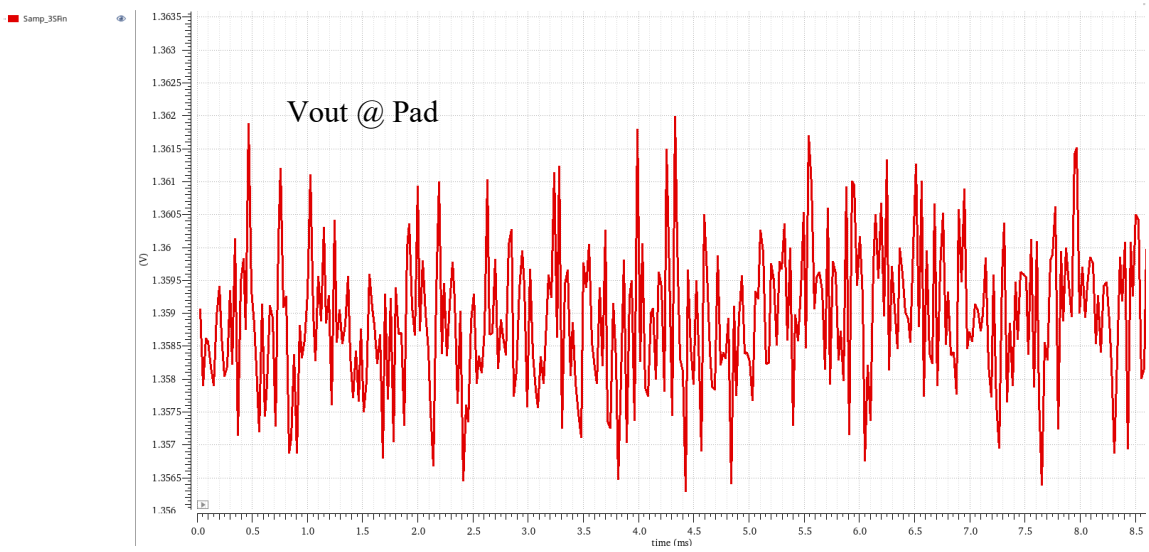


Figure 5-22 Signal chain transient noise simulation result

The Spectre transient simulation reveals a total output-referred noise of 387 μV, which is slightly lower than the estimated AC noise (414 μV) mentioned in Table 5-2. This discrepancy arises from the noise bandwidth configuration used in the transient simulation. Expanding the noise bandwidth setup would improve simulation accuracy, but it would also result in a significant increase in simulation time.

5.10.2 Top Chip Simulation

A top chip simulation is necessary to ensure the functionality of the entire image sensor in various scenarios, including power-up, imaging, and data transmission. Screenshots of the analog core schematic, top chip schematic and simulation testbench setup are presented in Figure 5-23, Figure 5-24 and Figure 5-25.

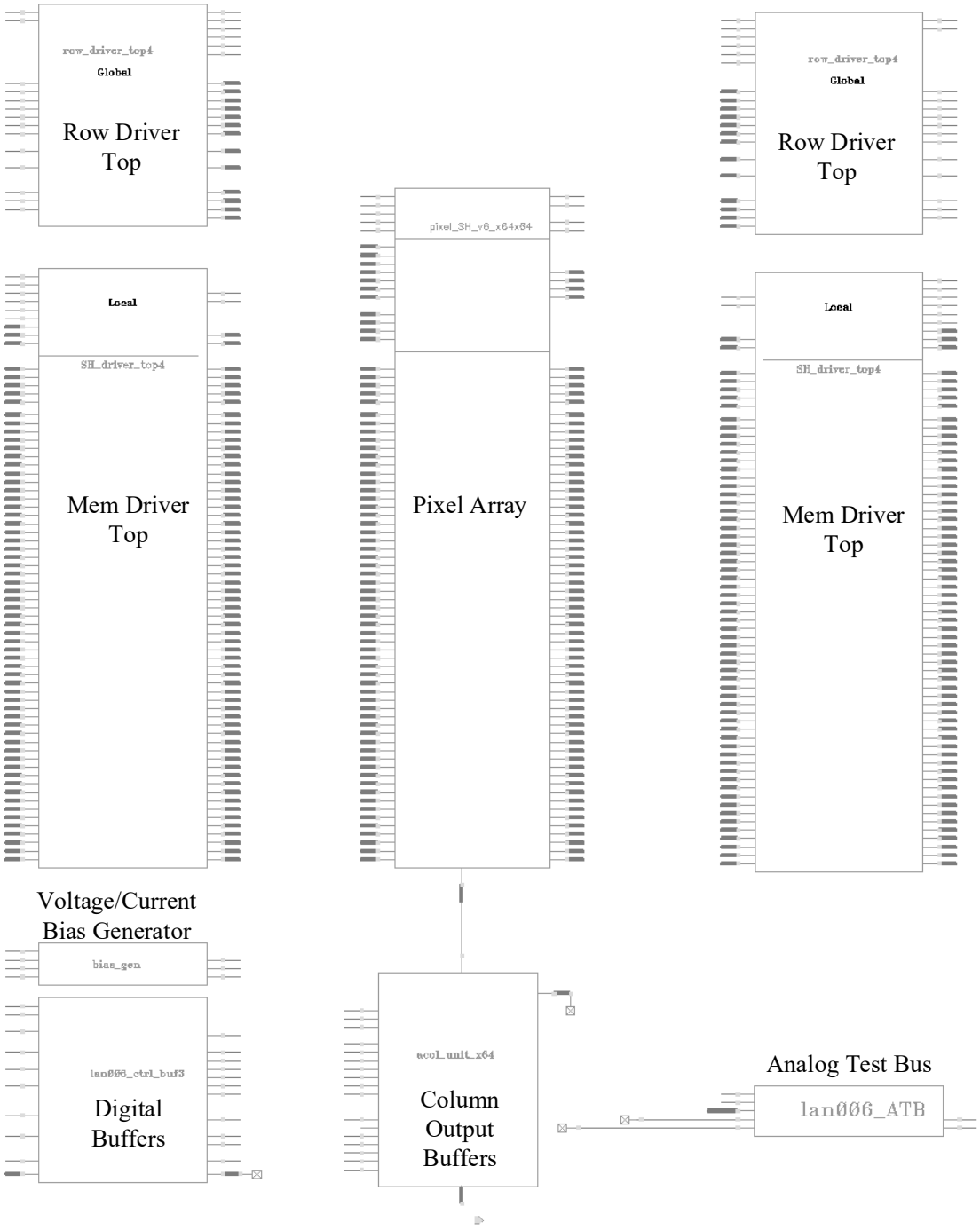


Figure 5-23 Schematic of analog core

Figure 5-24 Schematic of whole chip

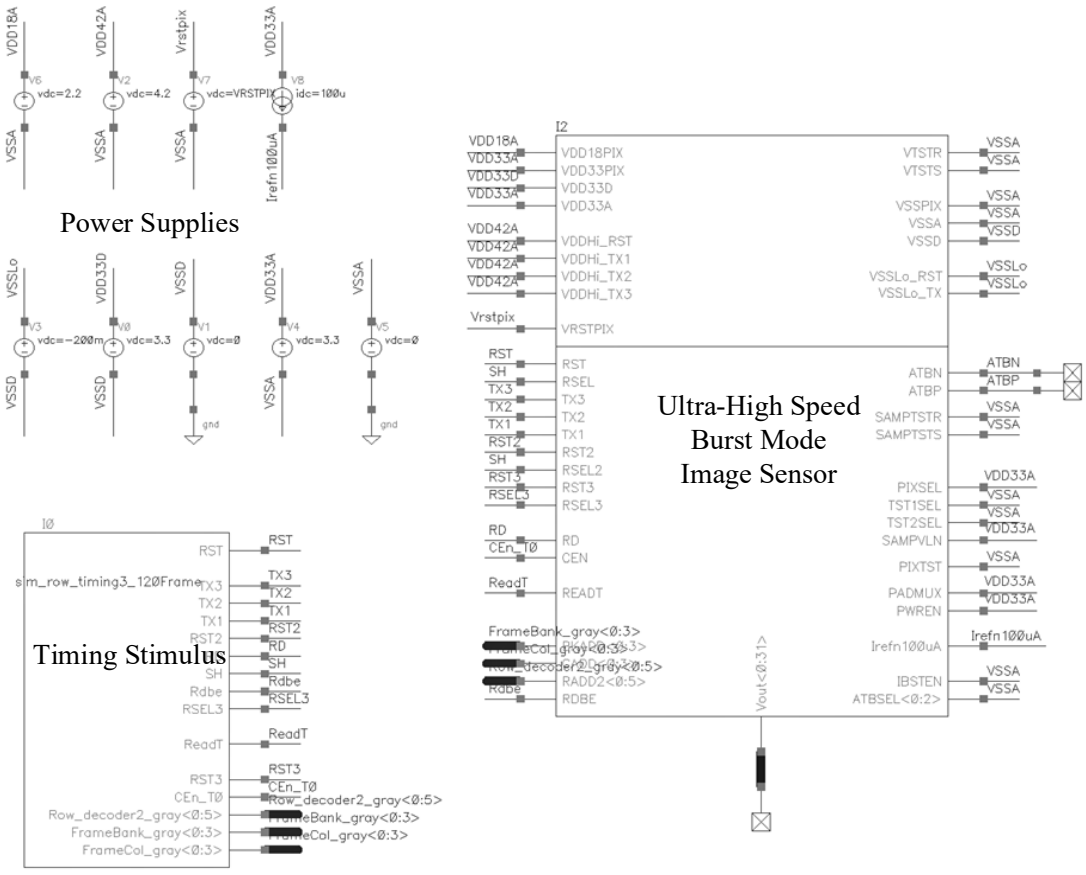


Figure 5-25 Test bench of top chip functional stimulation

To accelerate the simulation process in the top-chip simulation, the entire pixel array of 64 rows and 64 columns was reduced to 4 rows and 16 columns. Because Cadence Spectre can only simulate electrical signals, the photodiodes were replaced with DC voltage sources. The voltage difference between the pixel reset voltage and signal voltage was pre-set at 0.5V and 1V for even row-index pixels and odd row-index pixels, respectively.

The following figures in this section show the top-chip simulation result, where Figure 5-26 shows the pixel control trimming. One complete pixel sampling operation takes 50ns.

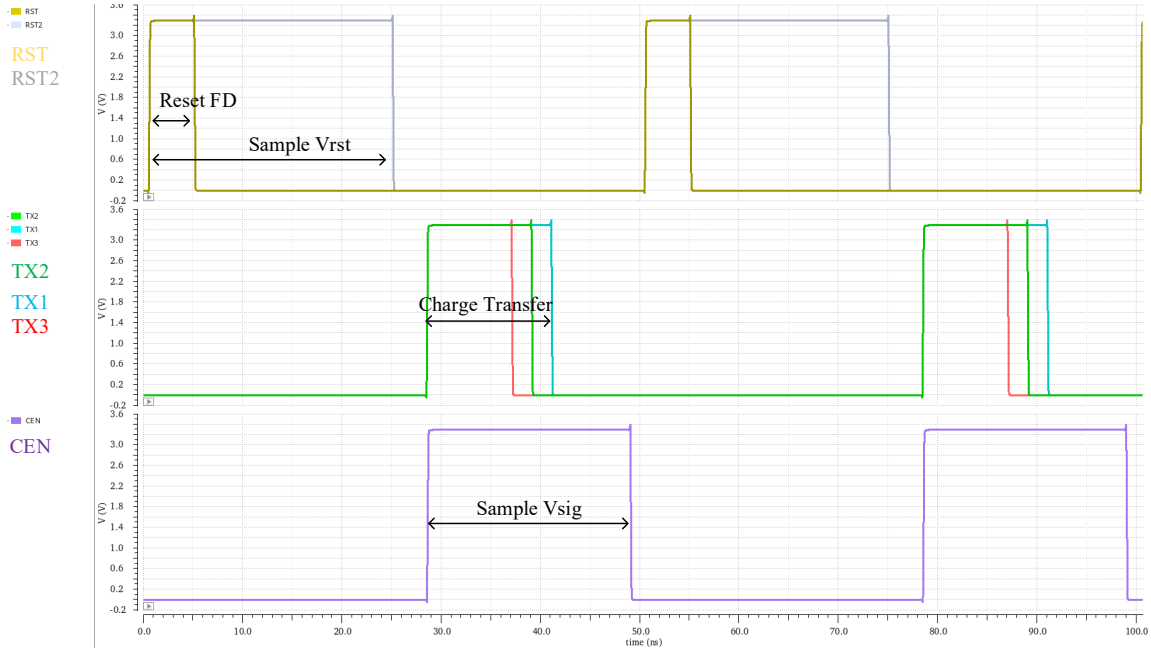


Figure 5-26 Top-chip simulation result 1

Figure 5-27 illustrates the voltage stored on the capacitors for the pixels in frame$_0$ row$_0$ and row$_1$, as well as the stored voltages on the capacitors for the pixels in frame$_1$ row$_0$ and row$_1$.

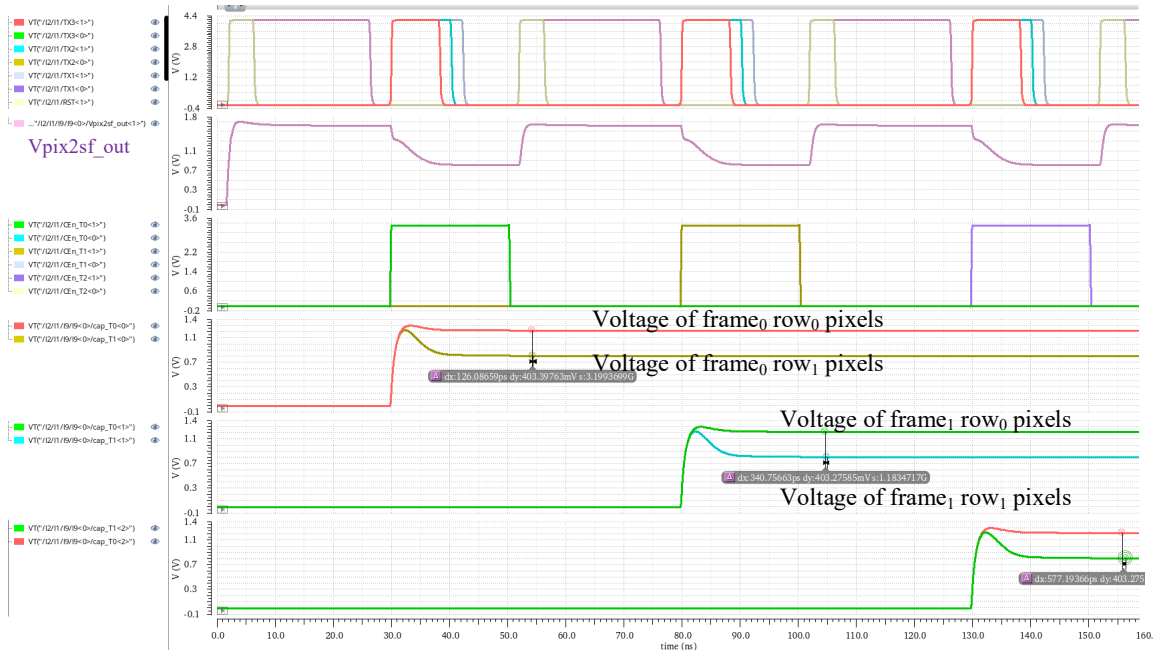


Figure 5-27 Top-chip simulation result 2

Figure 5-28 displays the end of the 108 frames sampling phase and the beginning of the reading phase. The information stored in the memory banks will be sequentially read out from row_0 to row_{63} of $frame_0$ and continue until $frame_{107}$. The difference in pad output between even and odd rows is 0.267 V. This value was divided by the signal chain gain of 0.485 V/V, as shown in Table 5-2, resulting in a voltage of 0.55 V, which matches the simulation stimulus setting.

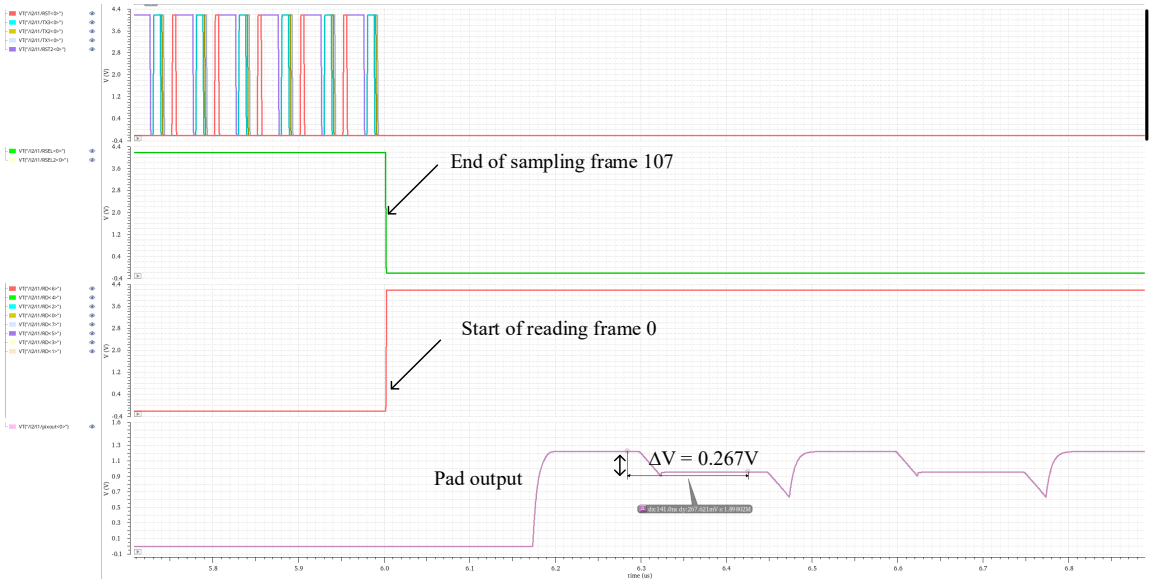


Figure 5-28 Top-chip simulation result 3

5.11 Tape Out

The entire design of the image sensor chip, from the initial pixel concept to the final GDS release, was completed within four and a half months. The final layout of the image sensor, which was taped out in September 2022, is presented in Figure 5-21.

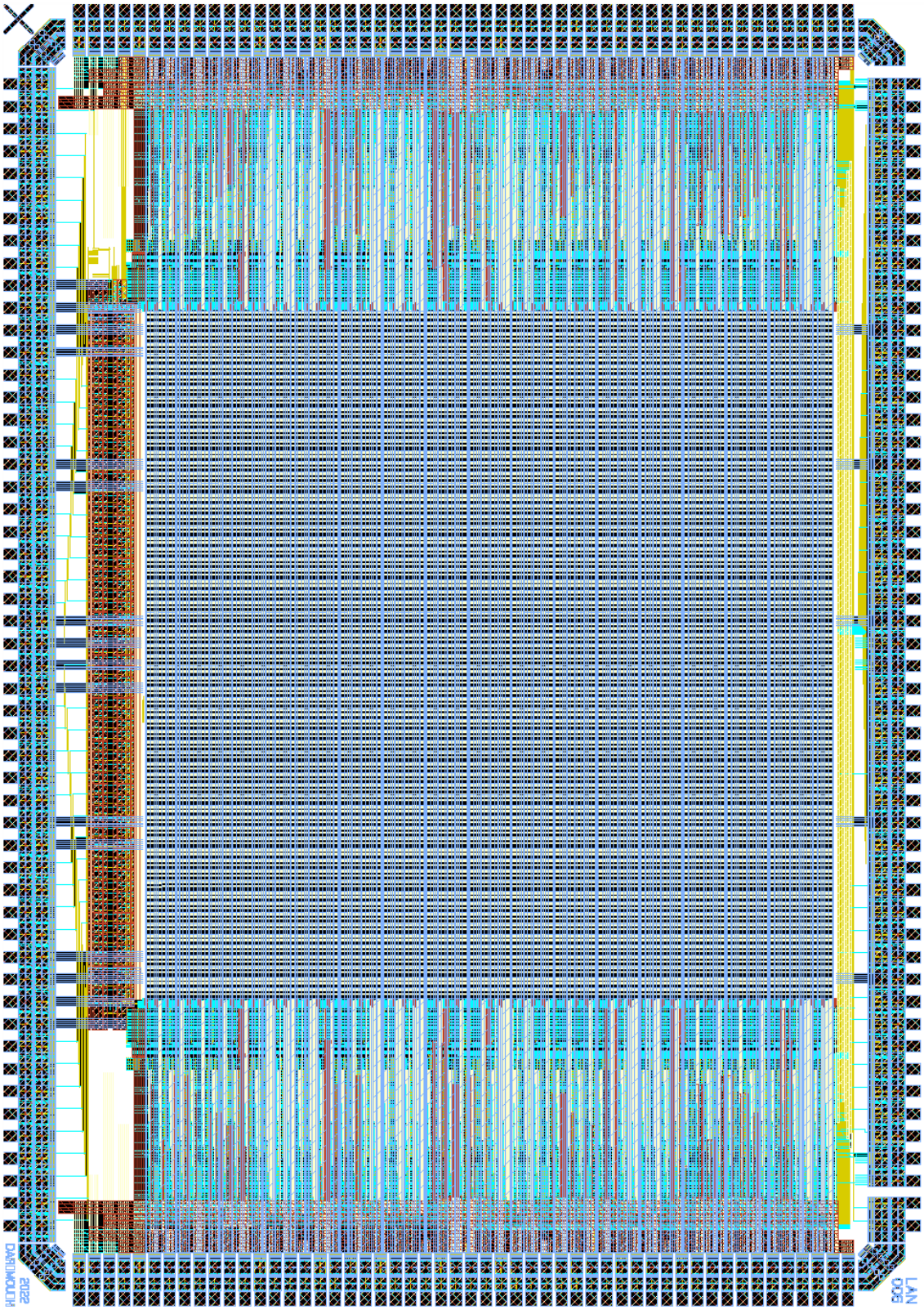


Figure 5-29 Final layout of the whole image sensor

5.12 Summary

In conclusion, Table 5-5 provides a comparison between the anticipated major specifications of the proposed image sensor and some of the state-of-the-art works in its category. It is noteworthy that the proposed image sensor is expected to achieve the lowest input-referred noise level ever reported, without requiring any process modification.

Ref	Year	Process (nm)	Process Modify?	Array (H×V)	Pixel Pitch (μm)	CG (uV/e-)	FWC (*ke*-)	Frame Rate (Mfps)	Record length	Noise (*e*-)
[7]	2019	180 FSI	Yes	50×108	35	99	11	100	368	N/R
[8]	2013	180 FSI	Yes	400×256	32	74	N/R	10	128	N/R
[9]	2017	180 FSI	Yes	96×128	32	112	10	10	480	N/R
[10]	2018	130 BSI	Yes	32×32	72.5	N/R	N/R	25	1220	N/R
[11]	2019	130 CCD	Yes	512×575	12.7	N/R	7	100	5	N/R
[12]	2018	130 BSI	N/R	32×84	30	105	6	20	108	8.4
[13]	2022	110 FSI	Yes	212×188	22.4	32	33	303	12	85
[14]	2016	110 FSI	Yes	320×324	11.2	N/R	10	200	15	>167
[119]	2018	90 40	N/R	20×20	50	7.3	137	5	52	>81
This work	2022	180 FSI	**No**	64×64	52.8	138	8	>20	108	**~5.6**

Table 5-5 Performance comparison between SoAs and estimations of this work

6 Characterization

The bare sensor dies, as depicted in Figure 6-1, were shipped out from the foundry in late March 2023. The upcoming sections will discuss the design of the sensor test system, as well as its methodology and results for characterization.

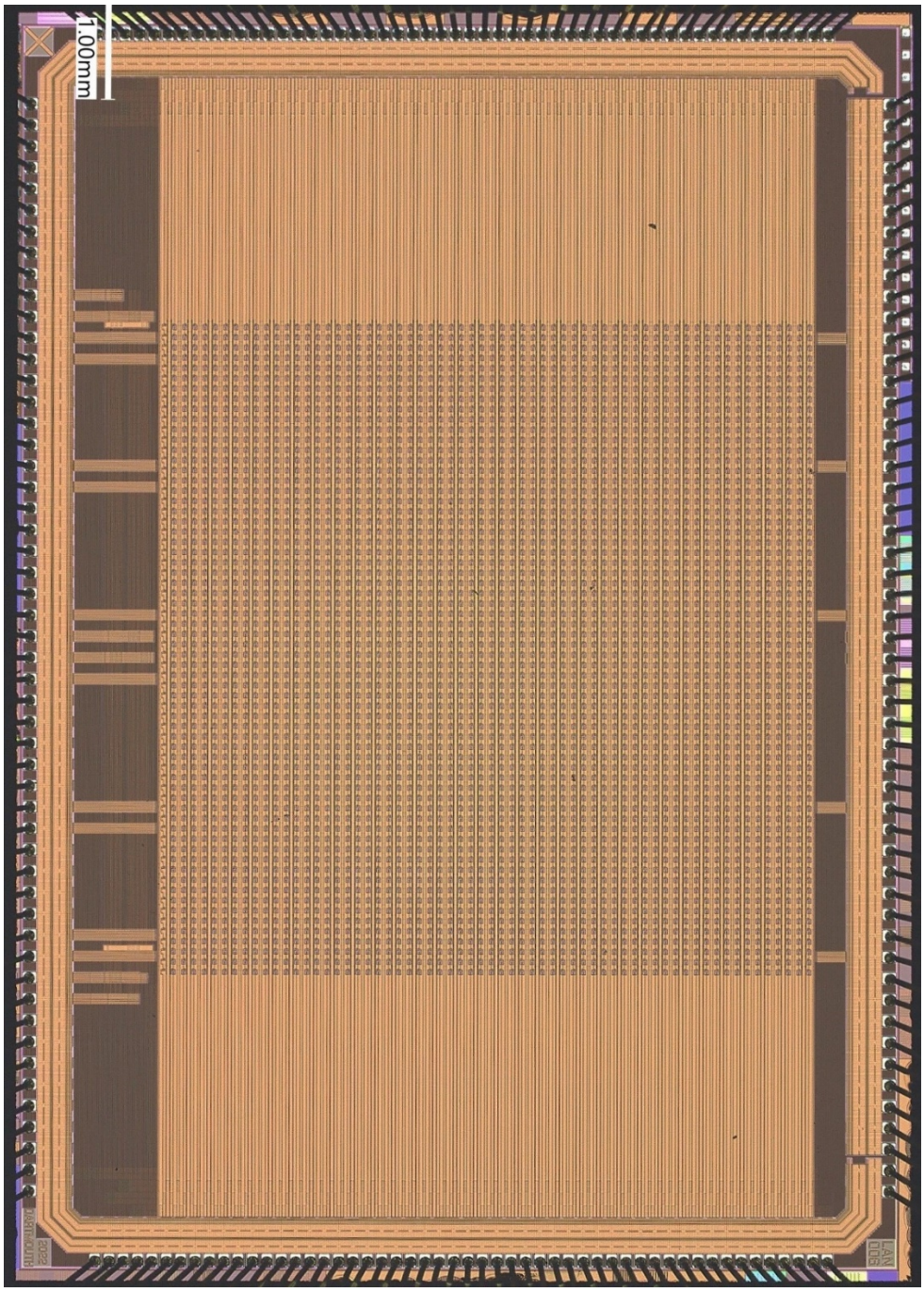


Figure 6-1 The microscopic image of the designed sensor chip

6.1 Prototype Test System

As previously mentioned, peripheral circuits, such as LDOs, have been placed off-chip due to the tight schedule of this project. Therefore, the test system needs to regulate the positive raw supply to several different voltages, including $VDD18_{PIX}$, $VDD33_{PIX}$, VDD33D, VDD33A, VDDHi_RST, VDDHi_TX1, VDDHi_TX2, VDDHi_TX3, and VrstPix, as well as the negative supply for VSSLo_TX and VSSLo_RST. Moreover, the sensor output will be analog voltages, and ADCs are required to convert these voltages.

To meet the low noise requirement, it is crucial for the ADC quantization noise to be significantly less than the sensor output noise (411 μV). As a result, a 16-bit ADC with an LSB of 38.1 μV has been used in this design. Additionally, to conform with the naming convention in the image sensor industry, this thesis will use the term "digital number" (DN) instead of LSB. For the remainder of this thesis, 1 DN will be equivalent to 38.1 uV.

The simplified block diagram of the system is shown in Figure 6-2. In order to achieve optimal noise isolation, the power and ground of the entire system are segregated into analog and digital domains, indicated by grey and blue colors, respectively. The board is equipped with 32 16-bit ADCs for sampling the sensor outputs and transmitting the results to an FPGA. The FPGA then processes the input data, adds a file header and frame index, and temporarily stores the frame data in a DRAM. Once all 108 frames of the image have been stored, the FPGA transmits the data to a PC via a USB 3.0 port. Figure 6-3 displays the prototype test system.

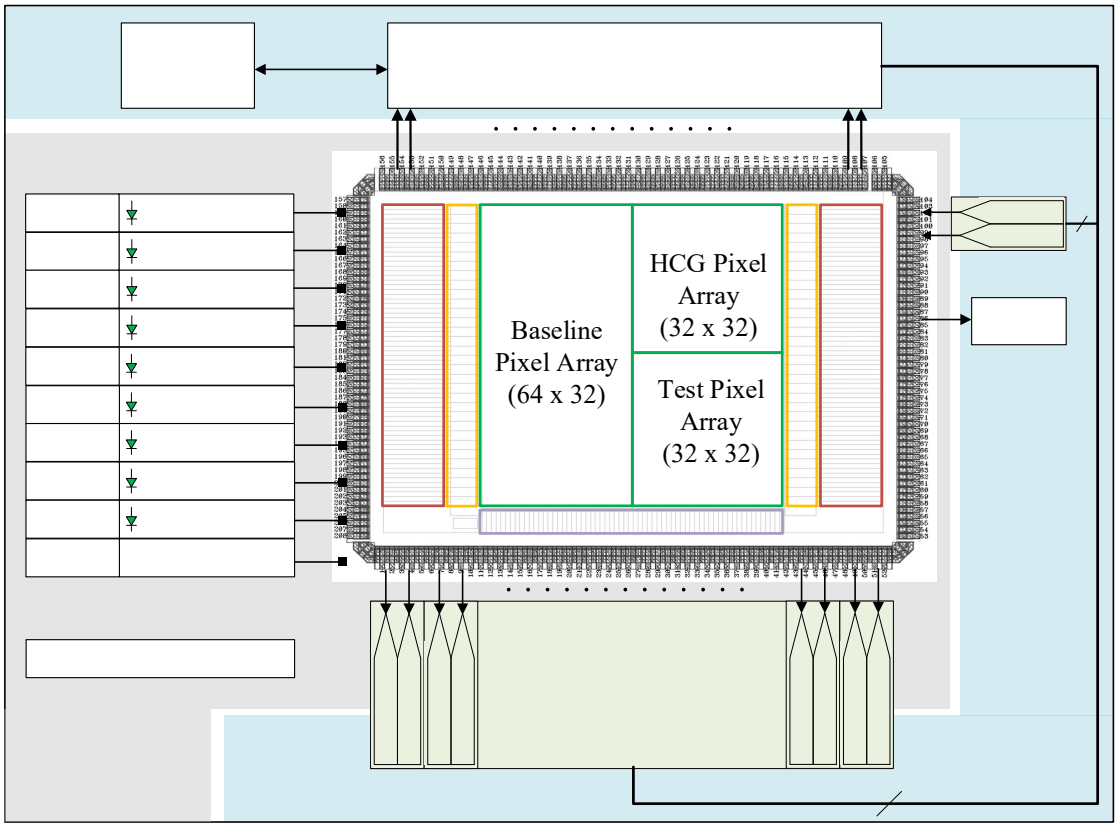


Figure 6-2 Block diagram of prototype test system

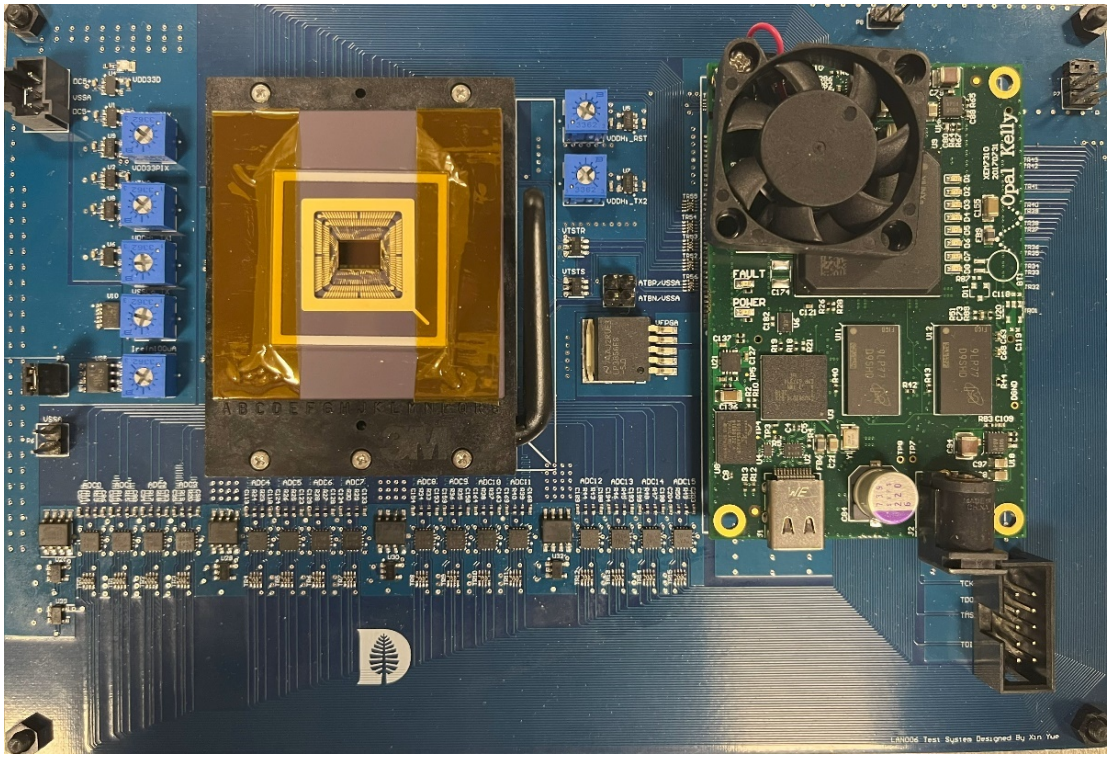


Figure 6-3 Photo of prototype test system

6.2 FPN Correction

As illustrated in Figure 5-13, the in-pixel 2nd stage source follower and 3rd stage source follower do not have a built-in CDS function. This absence leads to the presence of signal-independent fixed pattern noise (FPN) caused by transistor threshold mismatch, power and ground IR drop, and offset of off-chip ADCs. In order to ensure accurate measurement of imager performance, it is crucial to first eliminate FPN.

Figure 6-4 presents a raw dark image prior to FPN correction, containing constant and column-to-column offsets embedded in each pixel column. The pattern of bright and dark columns is clearly visible across the entire array. It is important to note that a darker image results in a higher ADC output code due to the readout circuit's structure, while a brighter image results in a lower ADC output code. Following the FPN/Dark subtraction [112] process, the polarity will be reversed, and lower digital numbers will indicate the darker pixels.

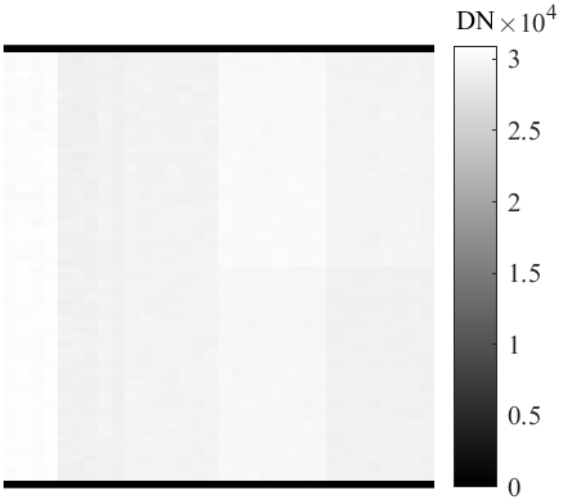


Figure 6-4 Raw dark Image

In the FPN/Dark subtraction algorithm, 200 frames of raw dark images are utilized. The averaging of these 200 frames per pixel helps in reducing the temporal noise by approximately $\sqrt{200}$ times, thereby leaving only the low-frequency component (FPN). The averaged result is illustrated in Figure 6-5, and as shown in the floor plan of Figure 5-3, the image can be divided into three distinct sections as the red line shows. The left half represents the output of baseline pixels, while the output of high conversion gain (HCG) pixels is shown in the top right quarter. The bottom right quarter shows the output of test pixels, but their details will not be discussed in this thesis.

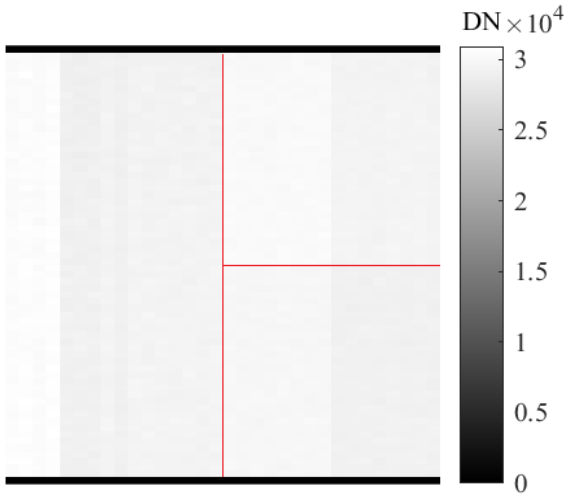


Figure 6-5 FPN/Dark averaged image

Then, the raw dark image is subtracted from the FPN/Dark averaged image. To prevent possible data overflow, a constant of 100 DN is added to each pixel of the averaged image. The resulting image, which is presented in Figure 6-6, exhibits a classical snowflake appearance, and FPN is no longer discernible. It is worth noting that, here, lower digital codes correspond to darker pixel outputs.

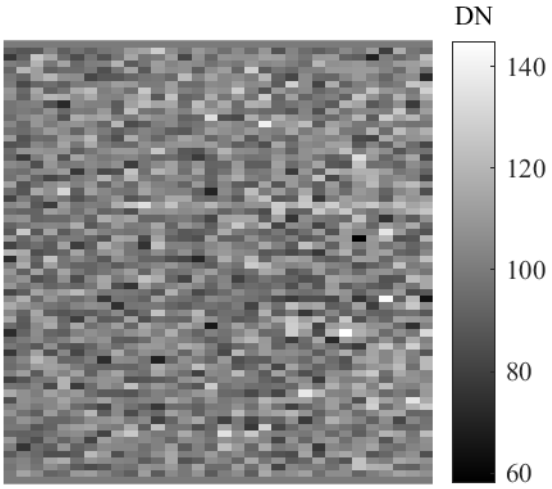


Figure 6-6 Dark image after FPN correction

To facilitate characterization, the FPN correction algorithm has been incorporated into the PC-side software. As a result, all images presented in the rest of this thesis will have FPN correction automatically applied.

6.3 Noise

In the previous chapter, it was demonstrated through TCAD simulations that the sensor can operate at least at a speed of 20 Mfps [111]. However, the current prototype test system is limited by the hardware capabilities of the FPGA, prototype PCB, and chip carrier, which restrict reliable operation to a maximum of 15.6 Mfps. The prototype system utilizes a CPGA-208 package and a zero-insertion-force (ZIF) socket that introduce parasitic inductances. These parasitic inductances cause significant ringing on the power supply V_{RST} of Figure 5-13 during pixel reset operations. This ringing can result in CDS errors and increased noise if the power supply and reference voltage have not fully settled before the end of CDS sampling.

Given the constraints of not being able to customize a package to minimize parasitic inductance, the most effective method to suppress this artifact is by increasing

the width of the CDS reset pulse (Rst2 in Figure 5-8). Unfortunately, this approach also reduces the frame rate of the sensor. Consequently, for now, to achieve optimal noise performance, the imager noise is measured at 4 Mfps.

It is worth noting that typical image sensors measure noise under complete dark conditions to minimize the contribution of photon shot noise. However, for this ultra-high-speed image sensor, in addition to the aforementioned shot noise source, the dark current's contribution must also be considered and eliminated due to the presence of a strong built-in electric field [37, 79, 89]. Consequently, during noise measurement, the TX1 pulse will remain low (Section 6.7 will provide further noise testing results, including the effect of dark current). Therefor the dark electrons accumulated in the photodiode will not transfer to FD. Figure 6-7 and Figure 6-8 show the noise histograms for the baseline pixel and HCG under this condition, respectively.

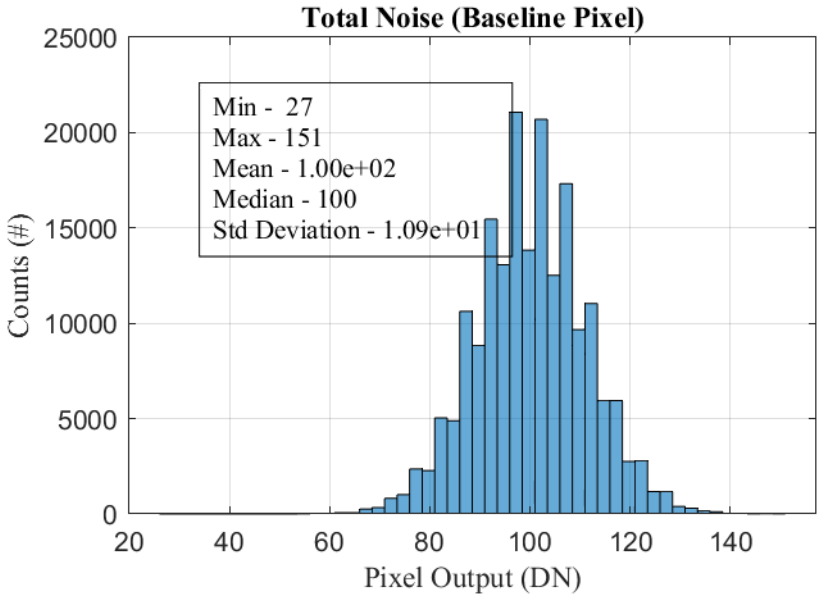


Figure 6-7 Noise histogram of baseline pixels (TX1=off)

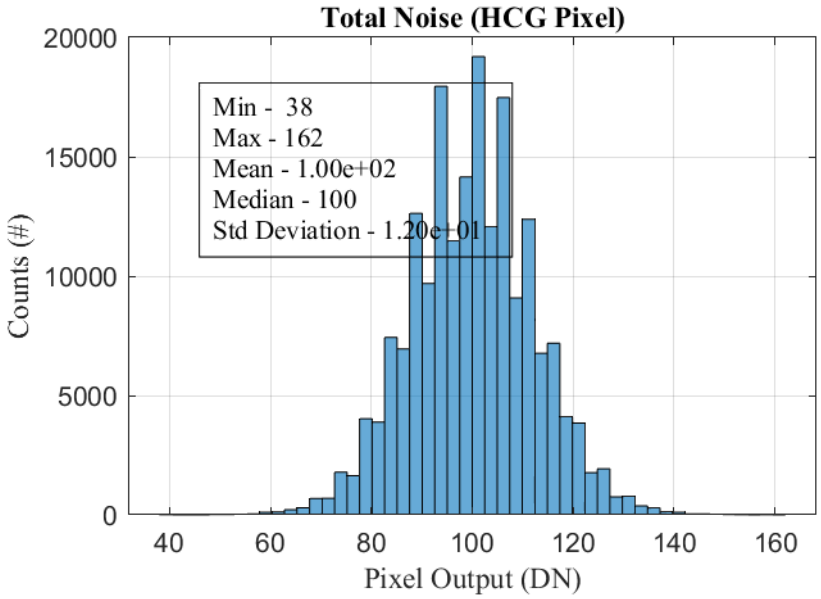


Figure 6-8 Noise histogram of HCG pixels (TX1=off)

The standard deviations in histograms indicate that the output-referred noise measured at the pad is 10.9 DN for baseline pixels, which is equivalent to 415 µV, and 12.0 DN for HCG pixels, which is equivalent to 457 µV. Both of these voltage noise values are in close agreement with the initial estimations reported in Tables 5-2 and 5-3. The baseline version was estimated to have 414 µV noise at the pad, and the HCG version was estimated to have 418 µV.

6.4 Conversion Gain

There are two primary techniques for measuring the conversion gain (CG) of an image sensor. The first method is based on the photon-transfer-curve (PTC) [80,81], which assumes that photons from a light source with a constant intensity follow a Poisson distribution. When photon shot noise dominates the overall noise of an image sensor, the standard deviation of the sensor's output is equal/close to the square root of its mean output value. The second method, which is used for low-noise quanta image sensors,

relies on the photon-counting histogram (PCH) [82, 83, 84, 85], and also assumes that photons follow a Poisson distribution.

Although the noise level of this image sensor is expected to be considerably lower than that of other state-of-the-art sensors in the ultra-high-speed category, it cannot achieve photon counting unless all 108 frames are used for averaging. Consequently, the PTC method is suitable for measuring the CG of this sensor. Figures 6-9, 6-10, 6-11, and 6-12 depict the initial PTC and CG measurements for the baseline and HCG pixels, respectively.

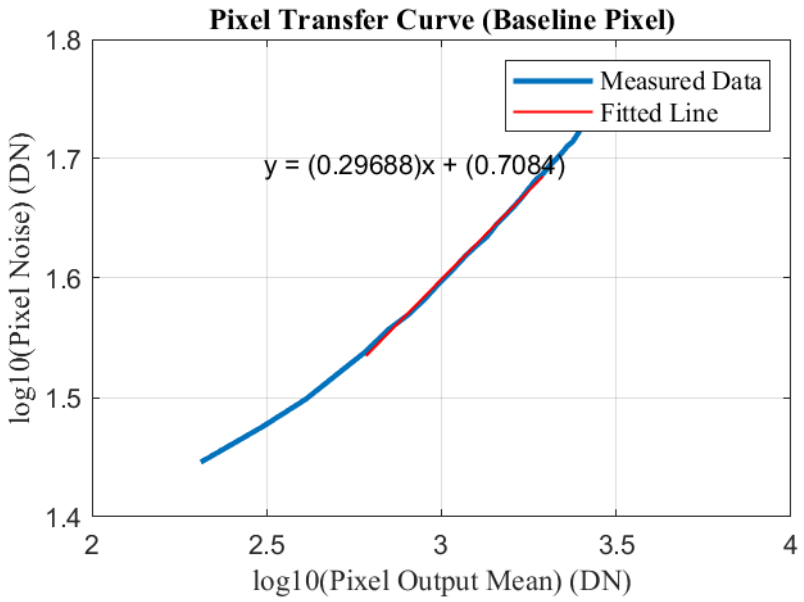


Figure 6-9 Initial PTC measurement result of baseline pixels

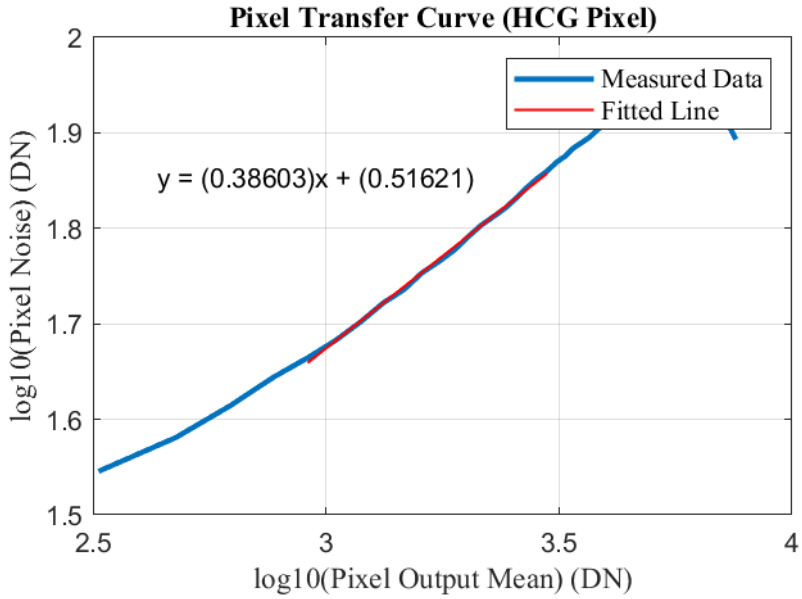


Figure 6-10 Initial PTC measurement result of HCG pixels

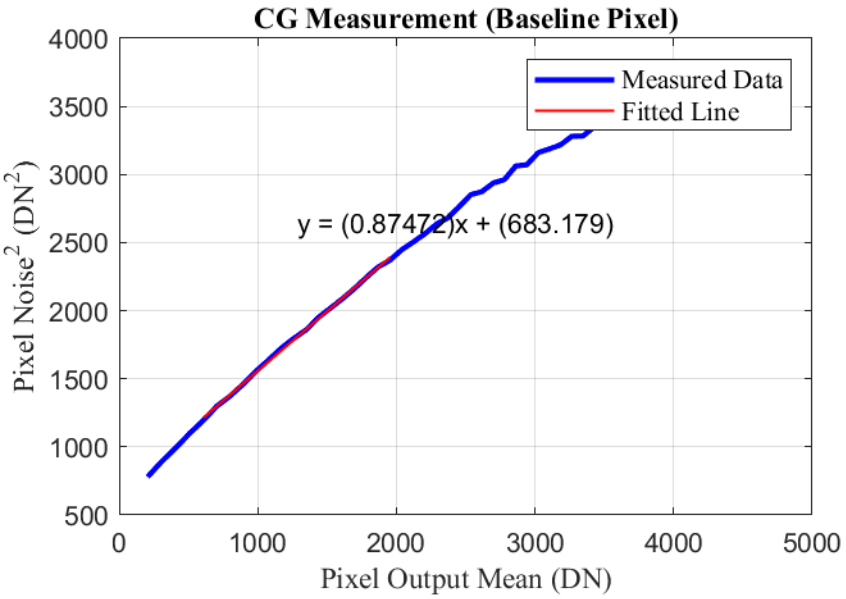


Figure 6-11 Initial CG measurement result of baseline pixels

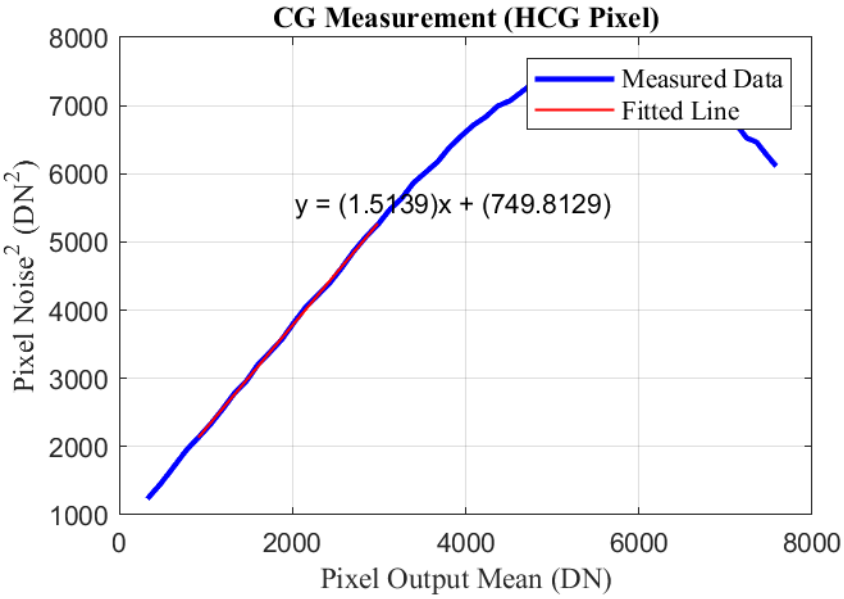


Figure 6-12 Initial CG measurement result of HCG pixels

Based on the analysis presented in the previous section, when the pixel noise is dominated by photon shot noise, the standard deviation of the sensor's output should be equal to or close to the square root of its mean output value. Therefore, in this regime, the slope of the PTC should be close to 0.5 [90]. However, in Figures 6-9 and 6-10, the slopes (0.29 for baseline pixel and 0.38 for HCG pixel) deviate from the ideal value. Therefore, the CG values measured in Figures 6-11 and Figure 6-12 may not be accurate and are very likely to be underestimated.

After a thorough examination of the characterization setup, it was found out that the high level of dark signal significantly impacts the accuracy of PTC measurements. In this measurement, an integrating sphere is used to diffuse and even out the incident light before it reaches the image sensor. However, the integrating sphere also significantly reduces the intensity of the light. Therefore, to ensure sufficient photons are collected in each photodiode during PTC measurements, the integration time of the image sensor

must be increased beyond its designed value. This extended integration time, in turn, increases both the mean level of dark signal and the noise level.

An improved configuration was implemented that utilizes significantly higher light intensity and reduced integration time to reevaluate the PTC and CG. Figures 6-13 and Figure 6-14 illustrate the PTC measurement results obtained from the new setup for both baseline and HCG pixels.

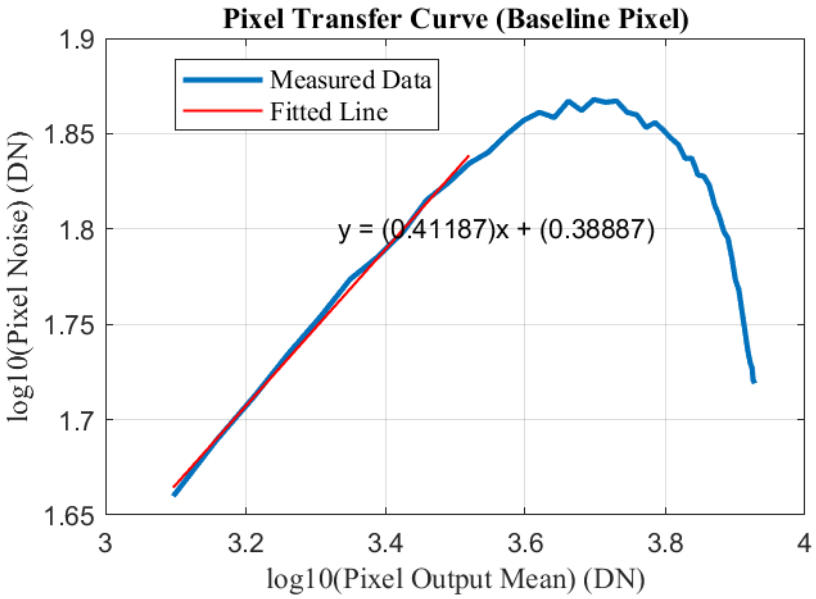


Figure 6-13 PTC measurement result of baseline pixels

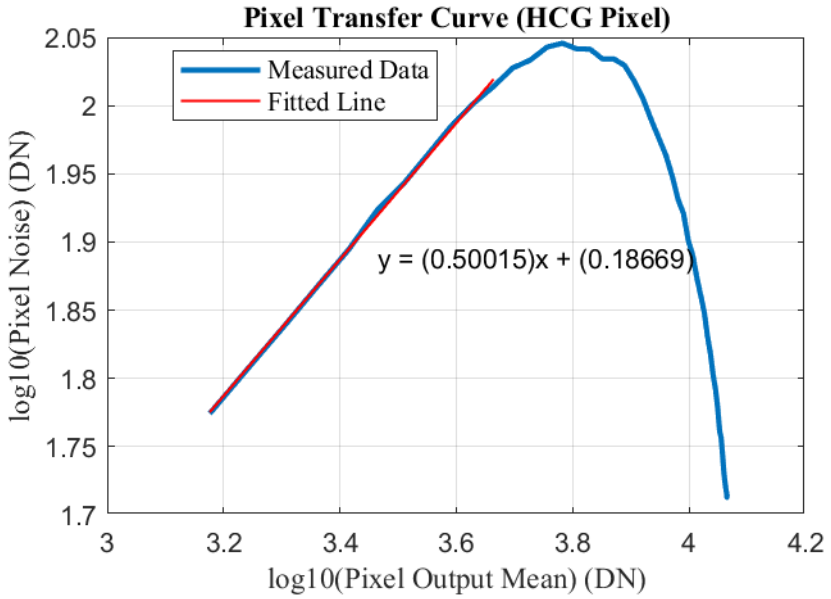


Figure 6-14 PTC measurement result of HCG pixels

The updated configuration resulted in PTC slopes of 0.41 and 0.50 for the baseline pixel and HCG pixels, respectively, in the region dominated by photon shot noise. These values are much closer to the ideal value. Therefore, it is safe and accurate to measure the pixel CG under these conditions. The results are displayed in Figure 6-15 and Figure 6-16.

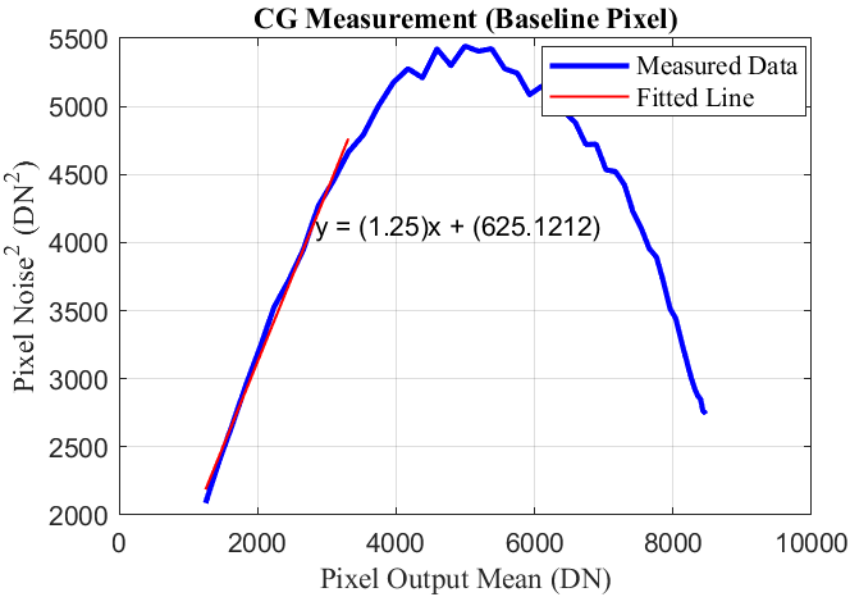


Figure 6-15 CG measurement result of baseline pixels

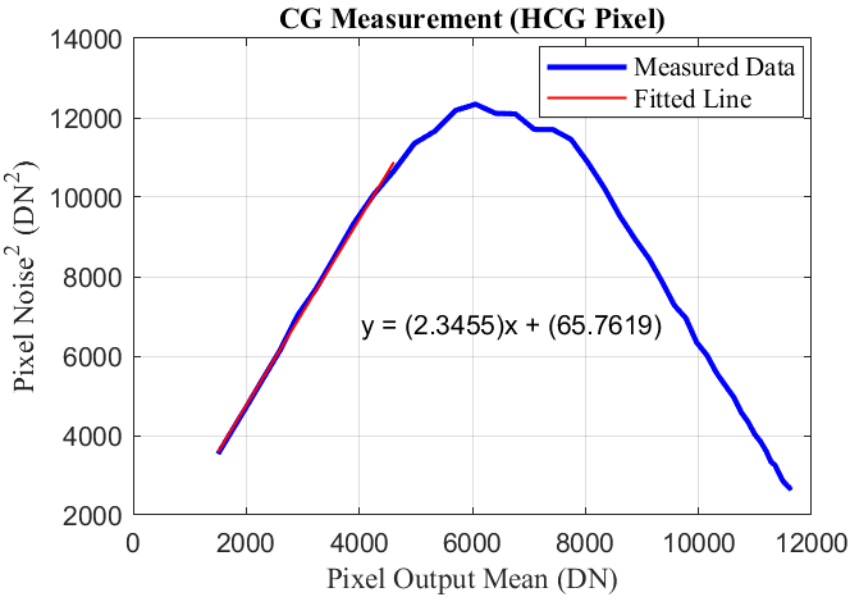


Figure 6-16 CG measurement result of HCG pixels

Adjusted by the signal chain gain of 0.485 V/V, the baseline pixel CG was calculated to be 98 μV/e- using equation 6-1. On the other hand, equation 6-2 determined the CG of the HCG pixel to be 183 μV/e-. Based on the above measurements, the sensor input-referred noise for the baseline pixel and HCG pixel are calculated at 8.7 *e*- and 5.1 *e*-, respectively.

$$CG_{baseline} = \frac{1.25\ DN/e}{0.485\ V/V} \times\ 38.1 \frac{uV}{DN} = 98\ \ \mu V/e \qquad (6-1)$$

$$CG_{HCG} = \frac{2.34\ DN/e}{0.485\ V/V} \times\ 38.1 \frac{uV}{DN} = 183\ \ \mu V/e \qquad (6-2)$$

Based on the same dataset, the distribution of CG per pixel was also calculated, as shown in Figures 6-17 and 6-18. The results indicate that there is a significant variation in CG in this process, which may be attributed to variations in the fabrication process, despite adhering closely to the recommended design rules for spacing and dimensions for

the baseline pixel. Additionally, contamination causing white blemish pixels [79] could also be responsible for this variation, which can considerably affect the level of dark current and affect CG measurement.

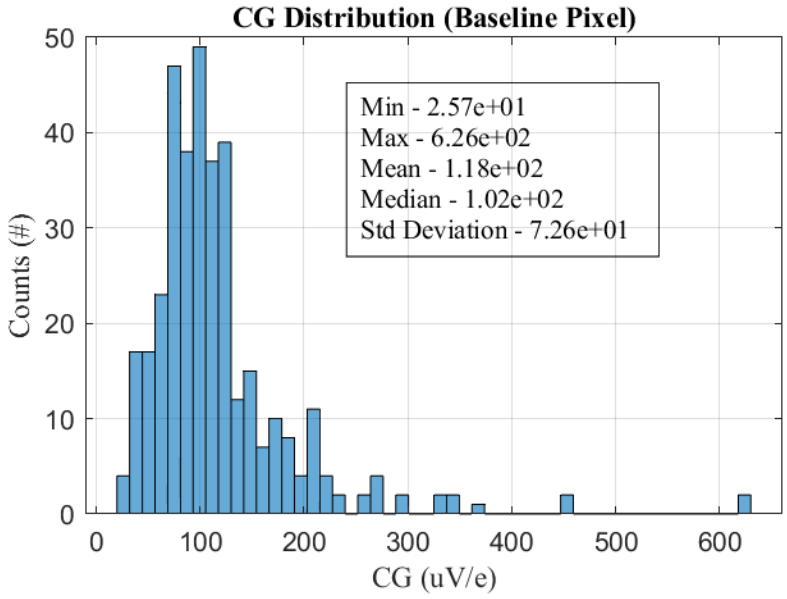


Figure 6-17 CG distribution of baseline pixel

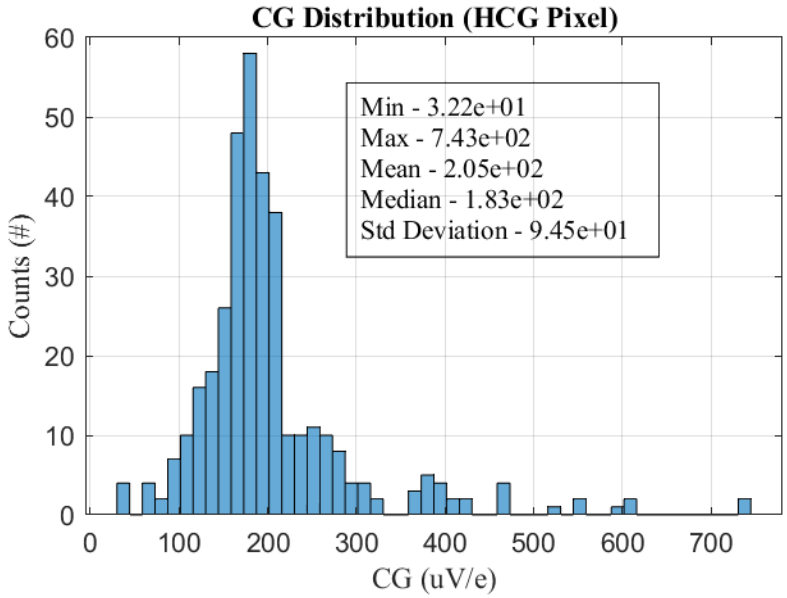


Figure 6-18 CG distribution of HCG pixel

6.5 Full Well Capacity

Based on the same dataset, the full well capacity of two pixels was also computed. Figures 6-19 and 6-20 display the mean pixel output as a function of integration time.

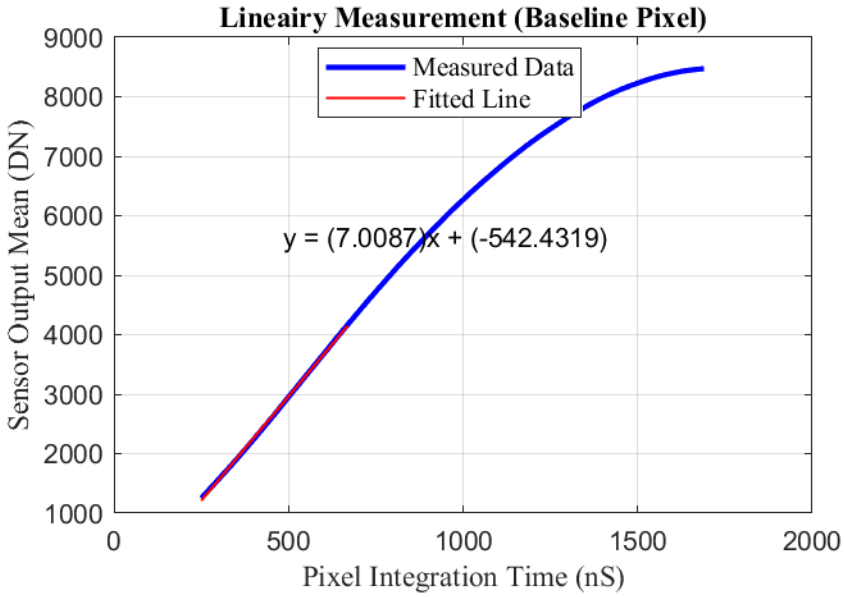


Figure 6-19 Full well capacity of baseline pixel

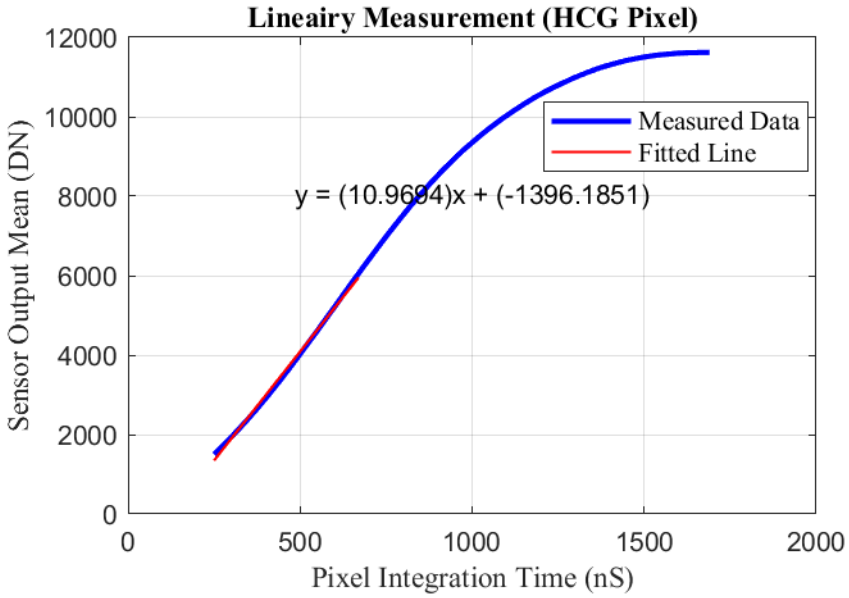


Figure 6-20 Full well capacity of HCG pixel

The baseline pixel output reaches saturation at approximately 8500 DN, equivalent to 6800 *e*-. The HCG pixel output, on the other hand, saturates at around 11600 DN, which corresponds to 5000 *e*-.

6.6 Low Light Linearity

The burst mode pixel employs three stages of source followers, and the linearity of the pixel signal chain has been carefully designed and optimized. Figures 6-21 and 6-22 present the results of the low light (<1000 photons) INL measurement for both the baseline pixel and HCG pixel. The results of both measurements indicate that the low light INL is < ± 0.5%.

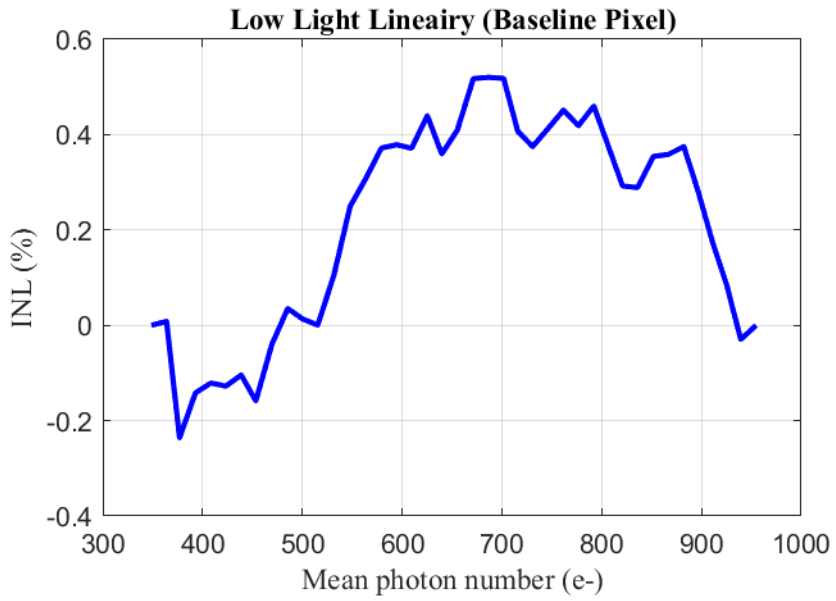


Figure 6-21 Low light linearity of baseline pixel

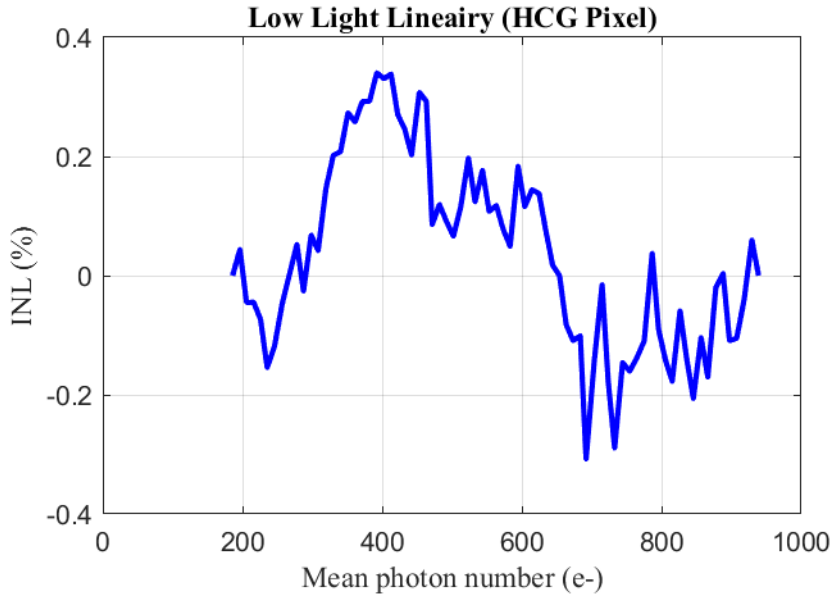


Figure 6-22 Low light linearity of HCG pixel

6.7 Dark Current

The TCAD transient simulation indicates a dark electron rate of $1.6x10^{-4}$ *e-*/ns/pixel in Figure 4-41. However, accurately simulating dark current can be challenging due to the lack of knowledge regarding the actual defect state density, level, and distribution, especially in areas with acute angles, as pointed out in [92]. According to references [79, 89, 91], the Pool-Frankel effect, tunneling effect and impact ionization increase dark current under large electric fields, exacerbating the situation. As a result, the dark currents in this sensor are not expected to be comparable to those of a typical 60 fps image sensor, and to the date this thesis was written, no reported dark current number is available for direct comparison in the category of ultra-high-speed image sensors, to the best of my knowledge.

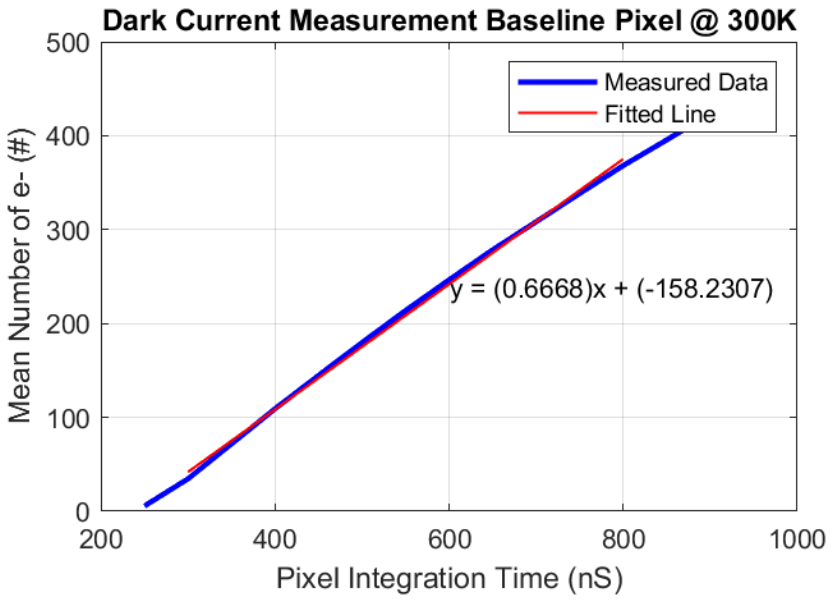


Figure 6-23 Dark current of baseline pixel at T=300K

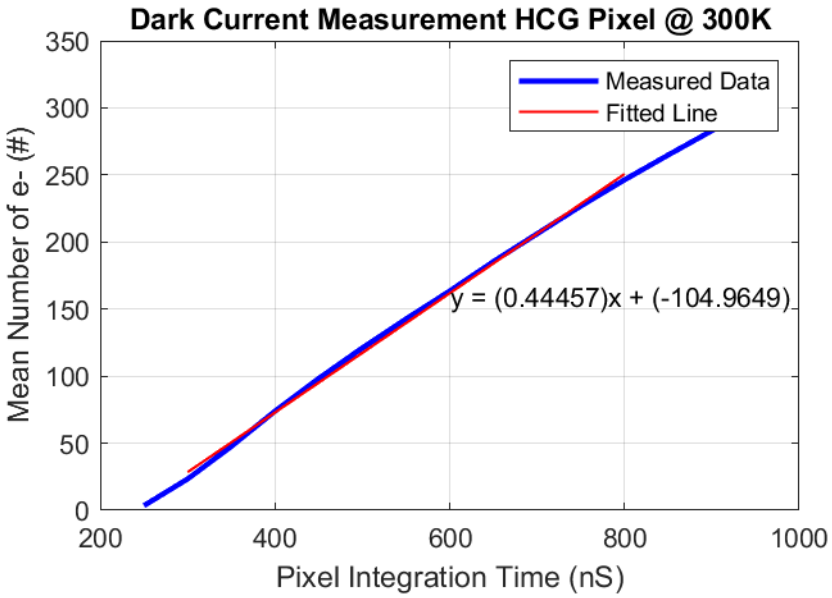


Figure 6-24 Dark current of HCG pixel at T=300K

Figures 6-23 and 6-24 display the dark current measurements at room temperature (300 K) for the baseline pixel and the HCG pixel, respectively. The baseline pixel exhibits a dark current of 0.66 *e*-/ns/pixel, while the HCG pixel has a lower dark current of 0.46 *e*-/ns/pixel. It is also necessary to examine the distribution of dark current. Figure

6-25 and Figure 6-26 depict histograms of dark current measurement per pixel for both baseline and HCG pixels. A few peaks at the tail of the histograms are noticed, suggesting potential white blemish caused by contamination [79].

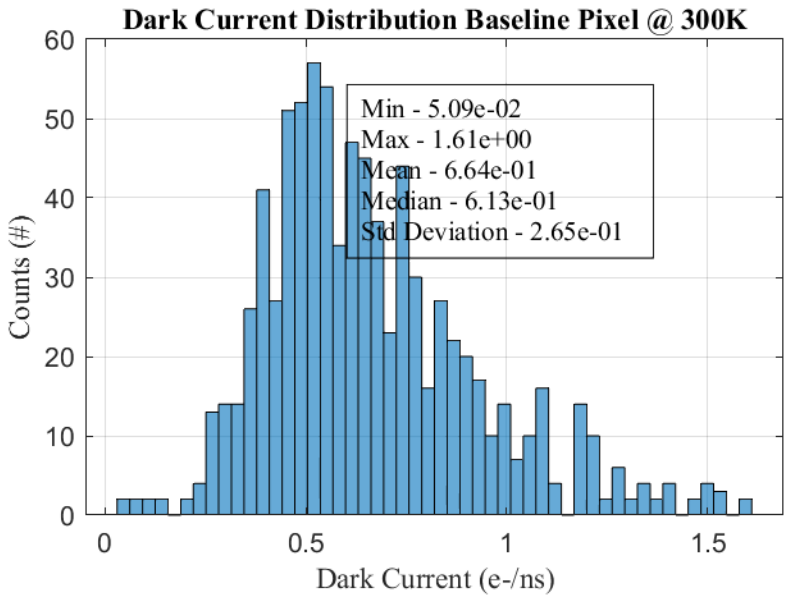


Figure 6-25 Histogram of dark current of baseline pixels at T=300K

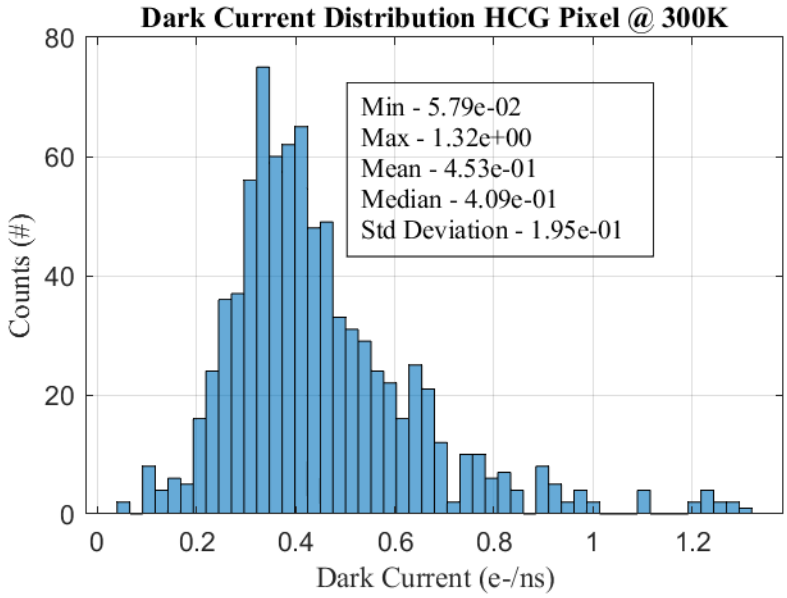


Figure 6-26 Histogram of dark current of HCG pixels at T=300K

The dark current measurement result significantly exceeds the simulated prediction. Subsequent investigation indicates the presence of a trap state density in the silicon bulk that exceeds the initial expectations. In light of this evidence, the TCAD simulations have been reevaluated, incorporating the trap state into the silicon bulk. As depicted in Figure 6-27, the revised TCAD simulation yields improved correlation. New simulation result shows 6.9 *e*-/ns/pixel.

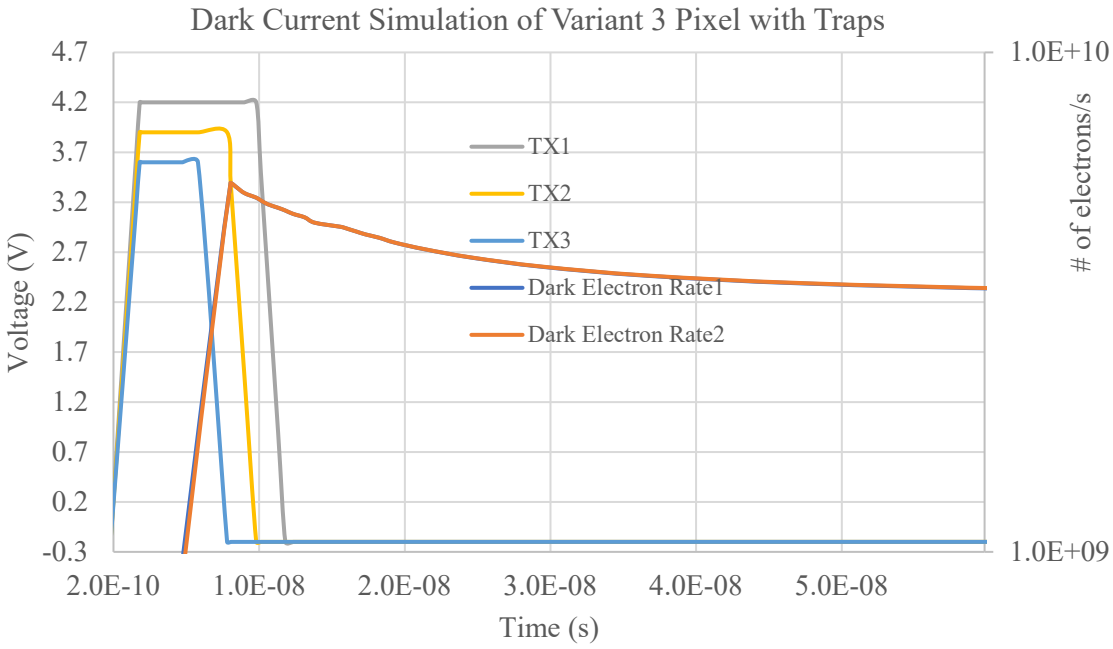


Figure 6-27 Dark current simulation result of HCG pixel with traps

At the same time, to gain a comprehensive understanding of this disparity, additional measurements are conducted under varying temperature conditions. Dark current measurements at 277 K are depicted in Figure 6-28 and Figure 6-29..

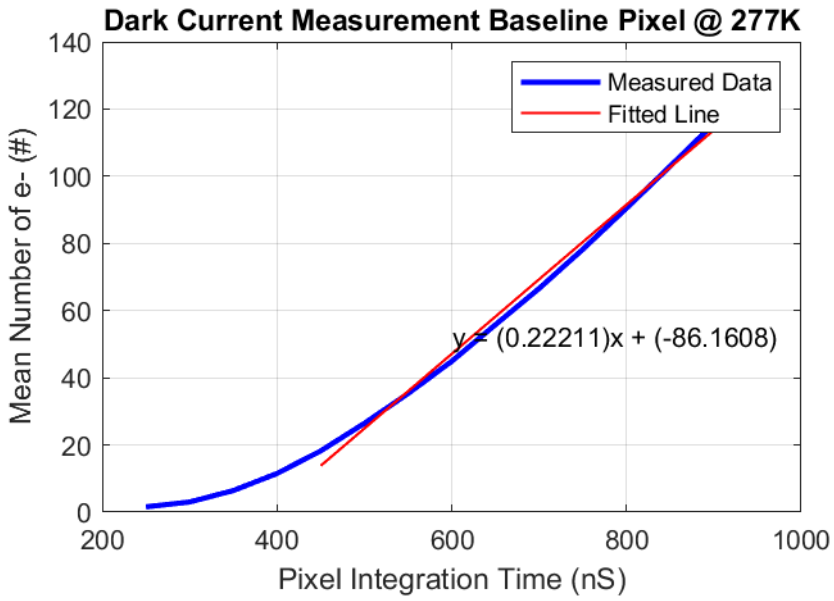


Figure 6-28 Dark current of baseline pixel at T=277K

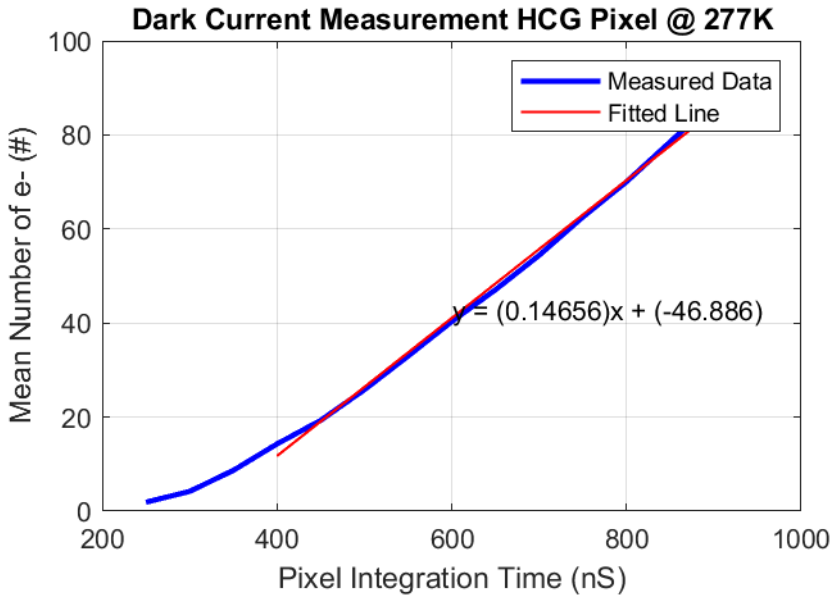


Figure 6-29 Dark current of HCG pixel at T=277K

Two observations can be made in above measurement. Firstly, both the baseline pixel and HCG pixel exhibit a significant reduction in the dark electron rate, as predicted by Equation 4-15. Secondly, when comparing the dark current measurements obtained at room temperature (300 K) to those taken at 277 K, clear non-linearity is observed for

short integration times, specifically for integration periods less than 400 ns. This non-linearity suggests that the number of dark electrons approaches the sensor's noise floor (5.1 *e*-), leading to measurement inaccuracies. Moreover, these findings indicate that the impact of dark current could be negligible at even lower temperatures. Figure 6-30 and Figure 6-31 illustrates the dark current measurement for the baseline pixel and HCG pixel, both conducted at a temperature of 256 k.

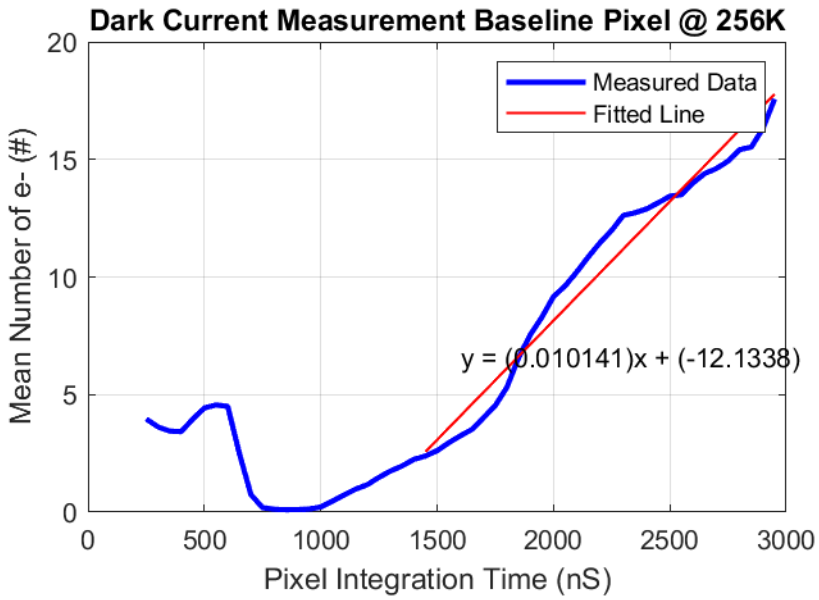


Figure 6-30 Dark current of baseline pixel at T=256K

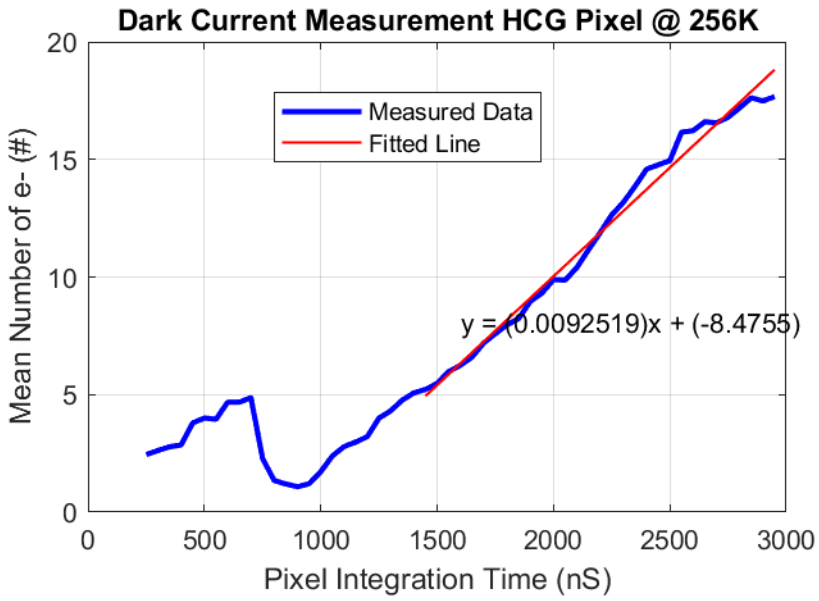


Figure 6-31 Dark current of HCG pixel at T=256K

At a temperature of 256K, the dark electron rate for both the baseline pixel and HCG pixel decreases to less than 0.01 *e*-/ns/pixel. In the intended application, with a frame rate of 20 Mfps, the maximum achievable integration time is 40 ns. Therefore, the maximum number of dark electrons is only 0.4, which is significantly smaller than the sensor's noise floor. This observation is further supported by the pronounced non-linear curve observed at shorter integration times in Figure 6-29 and Figure 6-30.

In order to further support this observation, the read noise of the sensor was measured once again. Unlike the approach described in section 6.3, where the TX1 pulse was kept low to eliminate the influence of dark current, all control signals, including the three TXs, were set to normal imaging-mode timing. Figure 6-32 and Figure 6-33 show the measurement of sensor noise under dark conditions at a temperature of 256K with a frame rate of 4 Mfps for both the baseline pixel and the HCG pixel, respectively.

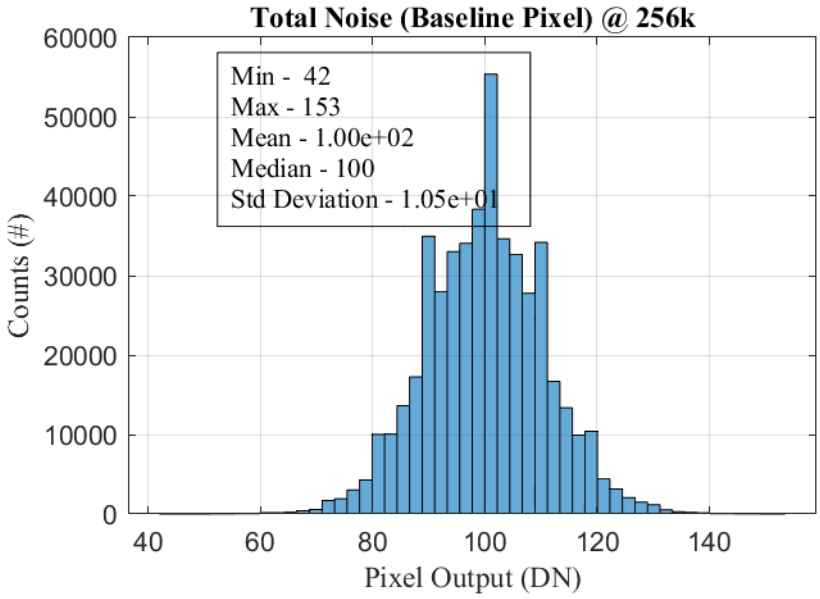


Figure 6-32 Noise histogram of baseline pixels at T=256K

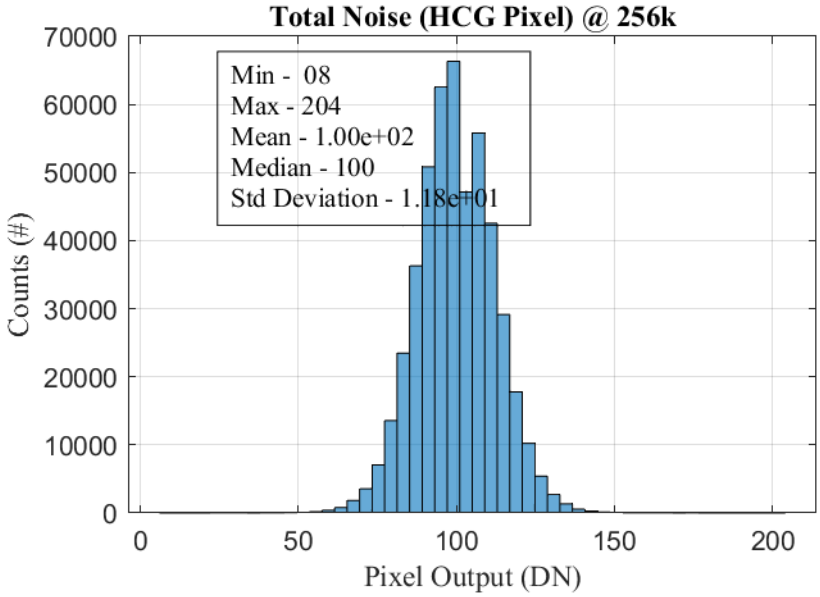


Figure 6-33 Noise histogram of HCG pixels at T=256K

The measurements reveal that the baseline pixel exhibits a total noise of 10.5 DN at the pad. Similarly, the HCG pixel exhibits a total noise of 11.8 DN, which closely aligns with the measurements described in section 6.3. In that section, the baseline pixel

and HCG pixel were measured at 10.9 DN and 12.0 DN, respectively. However, the measurements in section 6.3 did not account for the influence of dark current.

6.8 Lag

The sensor is designed to capture ultra-high-speed events happening within microseconds, and it is crucial to ensure that the image lag remains negligible. However, due to limited testing equipment, a super-fast and bright light source was unavailable during the characterization process. To address this, a bright LED array controlled by an array of BJTs was designed to fulfill this measurement, as illustrated in Figure 6-34. Due to limited slew rate of the falling edge of BJT control signals, the lag test was performed at 142 kfps, while the pixel TX3 pulse was fixed at 10 ns. The results of the lag test are presented in Figure 6-36 and 6-37, respectively.

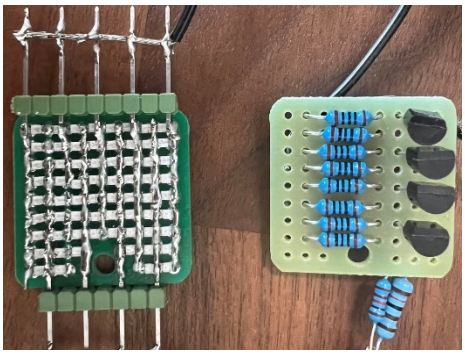


Figure 6-34 Photo of hand-made LED array and LED driver

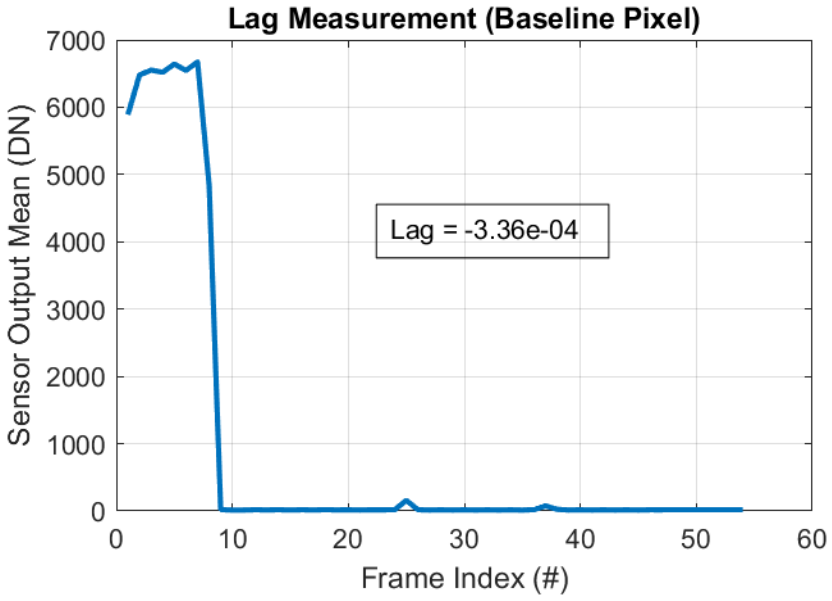


Figure 6-35 Lag measurement result of baseline pixel at 142 kfps

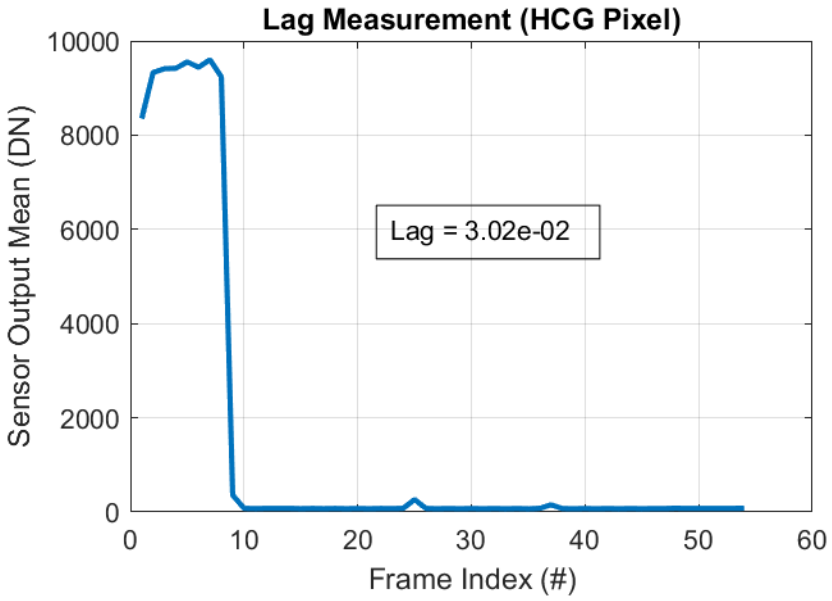


Figure 6-36 Lag measurement result of HCG pixel at 142 kfps

Based on the measurement results, it is evident that the baseline pixel exhibits a negligible lag of only 0.03%. In contrast, the HCG pixel shows a lag of approximately 3%, which is due to the overflow at the floating diffusion. Adjusting the TX gate negative voltage helped to reduce lag.

As can be inferred, if the sensor is operating at a higher speed, it should be capable of characterizing the falling time of an LED array. Therefore, the lag test was conducted again at 4 Mfps, and the falling characteristics of the LED array were clearly observed in Figure 6-37 and Figure 6-38.

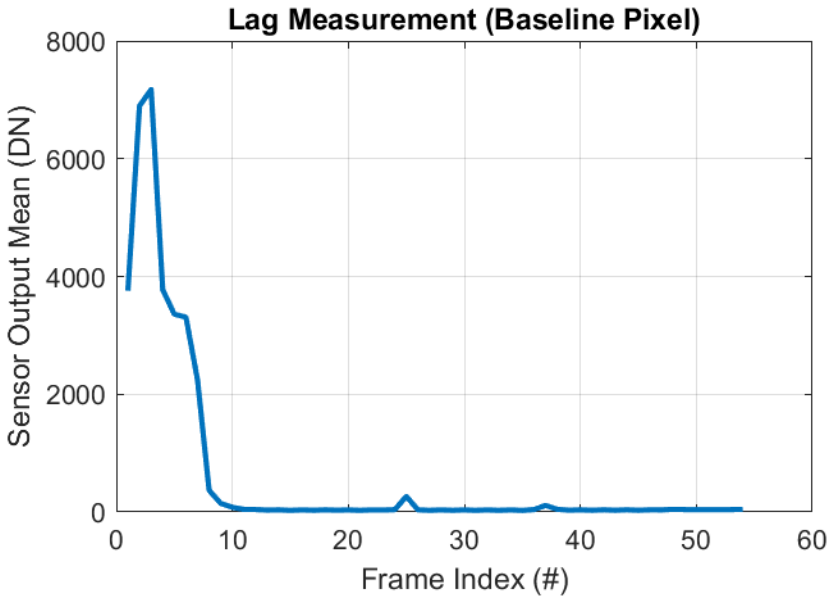


Figure 6-37 Falling edge of LED array captured by baseline pixel at 4 Mfps

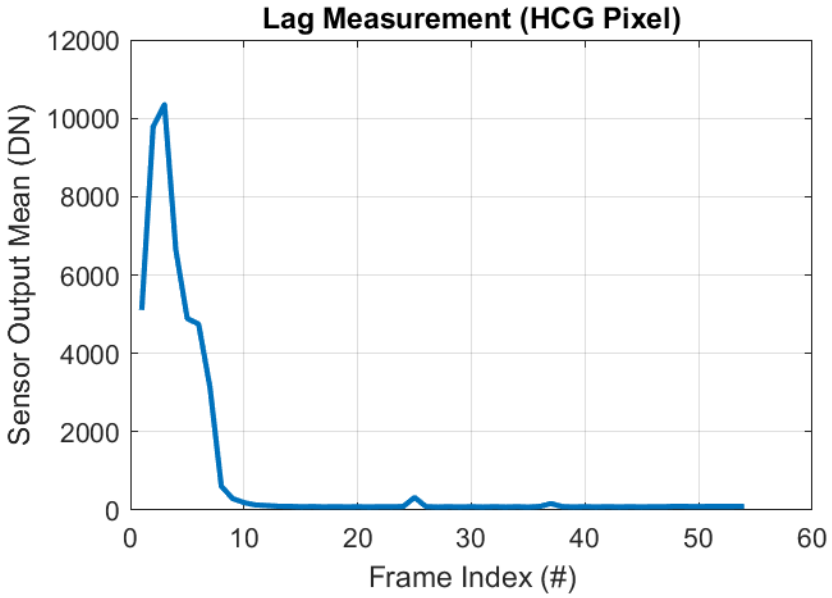


Figure 6-38 Falling edge of LED array captured by HCG pixel at 4 Mfps

6.9 Video Demonstration

This section is a video demonstration, comprising 108 frames, showing the falling edge of the focused LED array as shown in Figure 6-40. The video clip showcases the functionality of the ultra-high-speed image sensor that was designed. The entire setup is depicted in Figure 6-39, while Figure 6-40 displays the reflection of the LED array through the lens. It is important to note that the LED array has a limited light intensity. Therefore, to collect an enough number of photons per frame, the image sensor needs to slow down to 400 Kfps for this test.

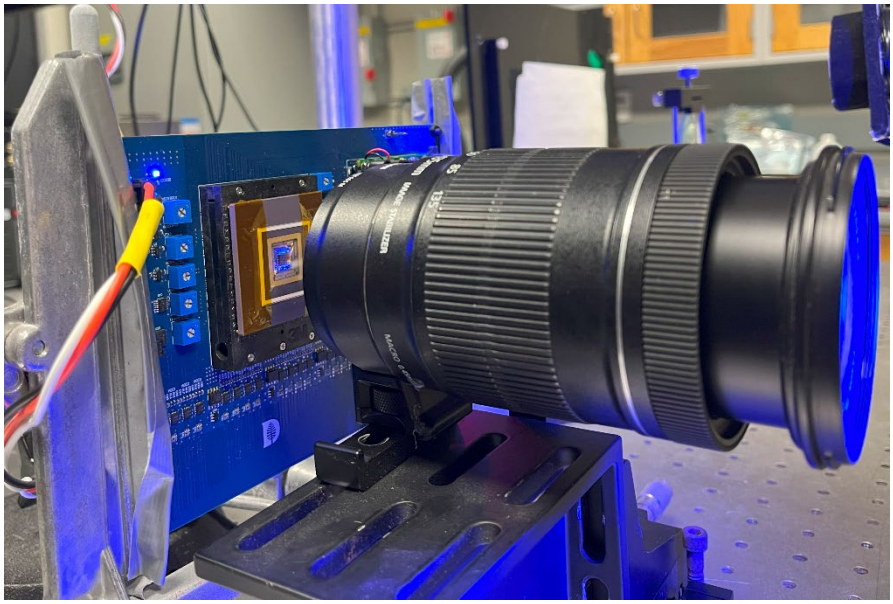


Figure 6-39 Photo of the test setup

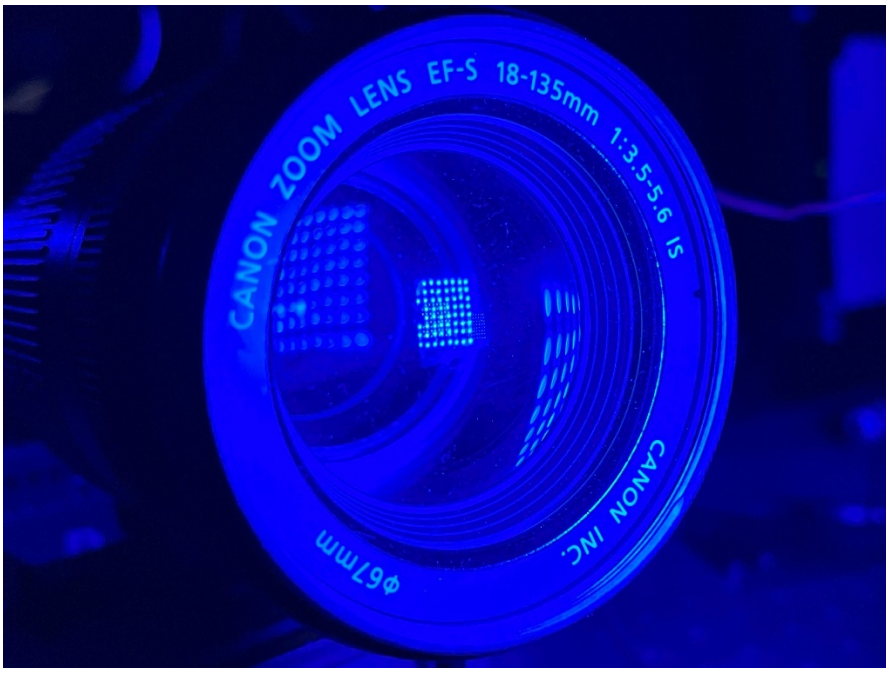


Figure 6-40 Reflection of object through the lens

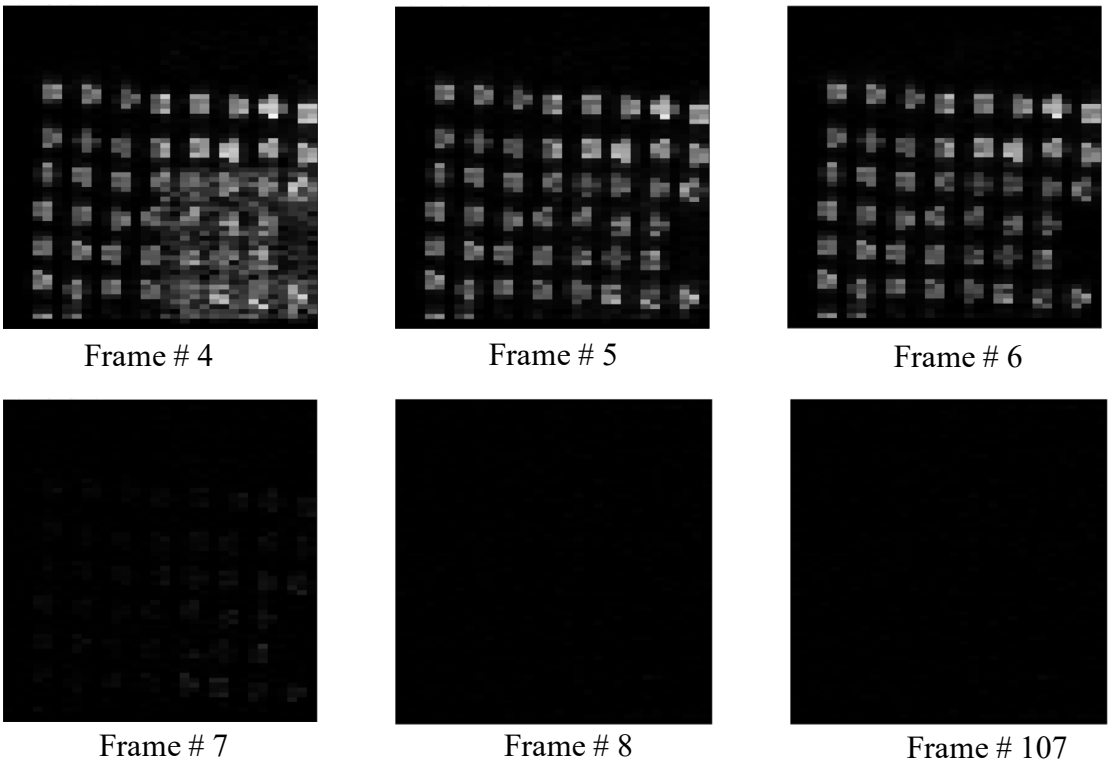


Figure 6-41 Video clips captured at 400 Kfps

6.10 Sensor Characteristics Summary

The final section of this chapter presents a summary of the characterization result, which are compared to the simulation results, as illustrated in Table 6-1. All pixel specifications, except for the dark current, exhibit a good match between measurement and simulation results. As mentioned in Section 6.7, a higher-than-expected dark current is suspected to be caused by defect states in the photodiode. Further investigation is necessary in the future.

Sensor Characteristics Summary					
Process	180 nm standard PPD CMOS				unit
Pixel Pitch	52.8 × 52.8				µm x µm
Pixel Fill Factor	9.7				%
Pixel Array Size	64 × 64				pix x pix
Recording Length	108				frames
Pixel Variant	Baseline		HCG		
Measurement/Simulation	*Mea.*	*Sim.*	*Mea.*	*Sim.*	
Charge Transfer Time	≤10	≤10	≤10	≤10	ns
Conversion Gain	98	*138*	183	*178*	µV/*e*-
Output Noise	415	*414*	457	*418*	µV
Input-Referred Noise	8.7	*5.8*	5.1	4.6	*e*-
Image Lag	≤ 0.1	≤ 0.5	≤ 3	≤ 0.1	%
FWC	6.0	7.0	5.0	5.6	k*e*-
Low Light Linearity	± 0.5	± 0.2	± 0.5	± 0.2	%
Dark Current (300K)	6.9E-01	1.6E-04	4.6E-01	1.6E-04	*e*-/ns/pixel
Dark Current (256K)	1.0E-02	N/A	9.2E-03	N/A	*e*-/ns/pixel

Table 6-1 Sensor performance summary

Table 6-2 gives the performance comparison between this work and SoA works in this category.

Ref	Process (nm)	Process Modify?	Array (H×V)	Pixel Pitch (μm)	CG (uV/e-)	FWC (*ke*-)	Frame Rate (Mfps)	Record length	Noise (*e*-)
[7]	180 FSI	Yes	50×108	35	99	11	100	368	N/R
[8]	180 FSI	Yes	400×256	32	74	N/R	10	128	N/R
[9]	180 FSI	Yes	96×128	32	112	10	10	480	N/R
[10]	130 BSI	Yes	32×32	72.5	N/R	N/R	25	1220	N/R
[11]	130 CCD	Yes	512×575	12.7	N/R	7	100	5	N/R
[12]	130 BSI	N/R	32×84	30	105	6	20	108	8.4
[13]	110 FSI	Yes	212×188	22.4	32	33	303	12	85
[14]	110 FSI	Yes	320×324	11.2	N/R	10	200	15	>167
[119]	90 40	N/R	20×20	50	7.3	137	5	52	>81
This work	180 FSI	**No**	64×64	52.8	**183**	5	20	108	**5.1**

Table 6-2 Performance comparison between SoAs and measurements of this work

7 Improvement and Future Work

7.1 Test System Optimization

As mentioned in Section 6.3, the current prototype test system imposes limitations on the sensor's frame rate. It is suspected that these limitations are caused by the parasitic inductance of the long pins in the CPGA package (shown on the left in Figure 7-1) and the through-holes of the zero-insertion-force (ZIF) socket (depicted on the right in Figure 7-1).

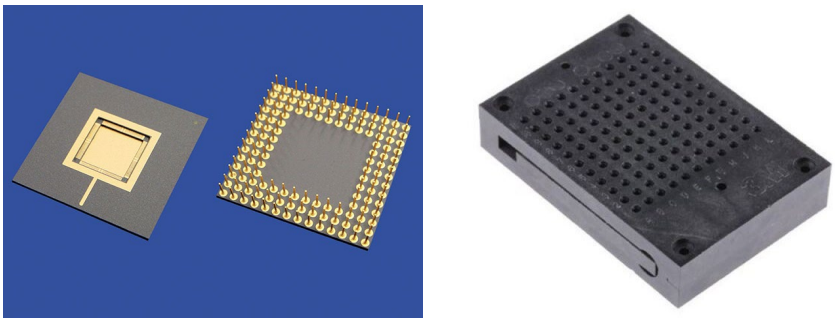


Figure 7-1 Example of CPGA package and ZIF socket

These factors contribute to the ring of power supply V_{RST} during CDS operation, which subsequently slows down the frame rate. For future test system, it is recommended to utilize a customized Land Grid Array (LGA) package, as depicted in Figure 7-2. This approach aims to minimize both bonding wire resistance and package parasitic inductance.

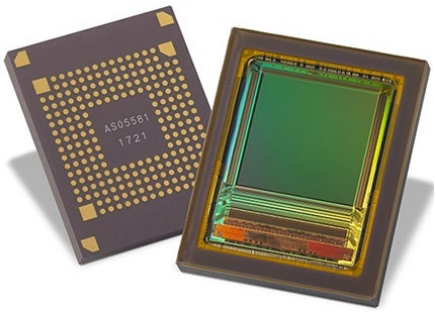


Figure 7-2 Examples of a high pin count CMOS image sensor packaged in LGA package

7.2 Circuit Optimization

As mentioned in section 5.5, the original intention was to include a feature that would allow the bypassing of the actual pixel circuit. This feature would enable the injection of two programmable voltages, namely V_{tst_S} and V_{tst_R}. These voltages would simulate the pixel reset voltage and pixel signal voltage, respectively. The purpose of this feature was to facilitate testing of the pixel readout signal chain, as depicted in Figure 7-3 with the grey circuit.

However, a minor design mistake resulted in the accidental disabling of this functionality during the schematic design phase. Regrettably, this misconnection went unnoticed in the top-chip functional simulation. While this minor bug does not impact the normal imaging function of the sensor, it is recommended to rectify it in the next version of the sensor design.

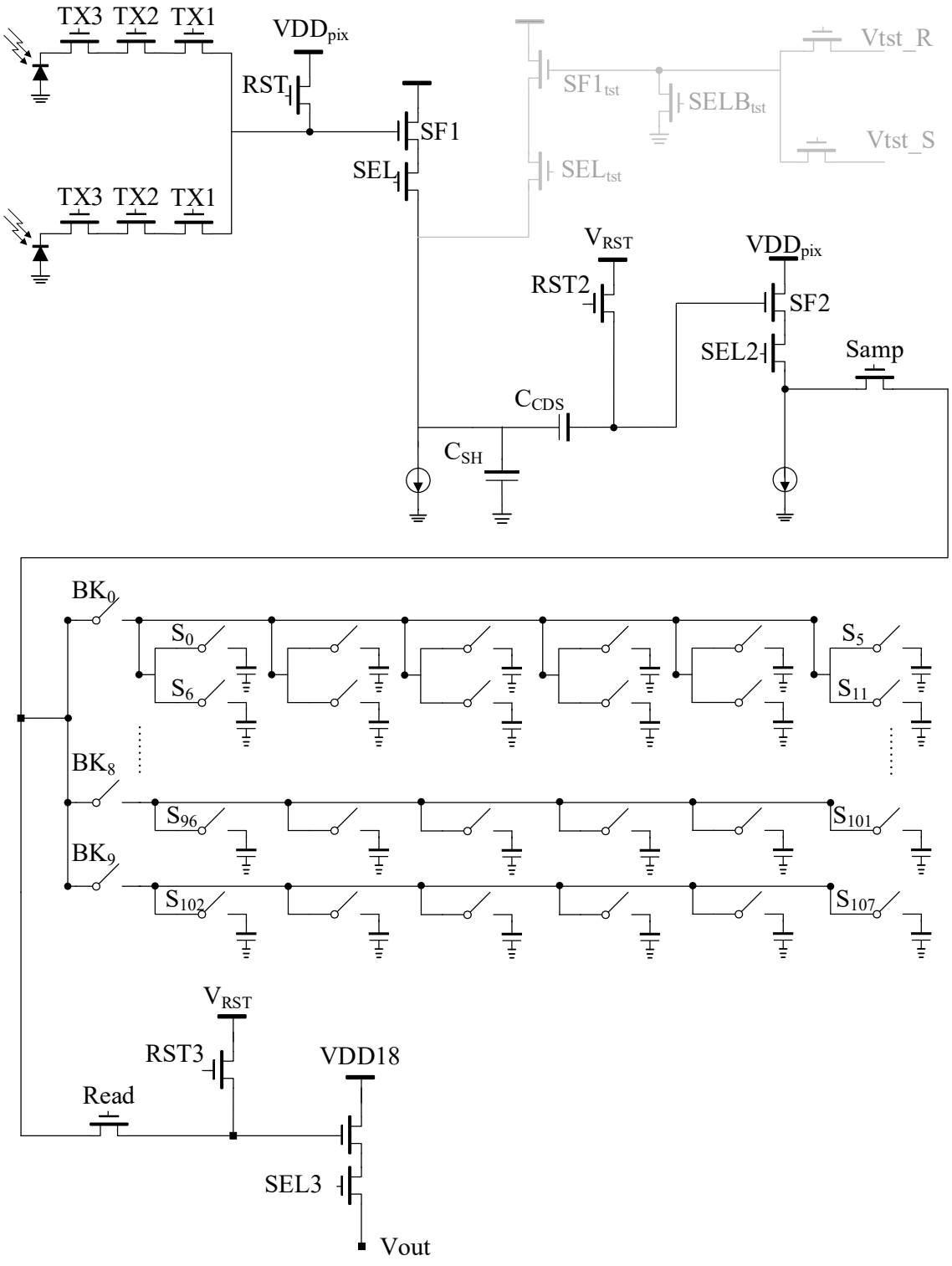


Figure 7-3 Schematic of the pixel with built-in test circuit

7.3 Process Optimization

Although the current process is not allowed to be modified, there is still room for future process optimization if an opportunity arises. During the TCAD process simulation, it was observed that the depletion depth of the default photodiode is relatively shallow, as depicted in Figure 7-4, indicated by the white curves. The actual depletion depth remains undisclosed to the public due to a non-disclosure agreement (NDA) with the foundry.

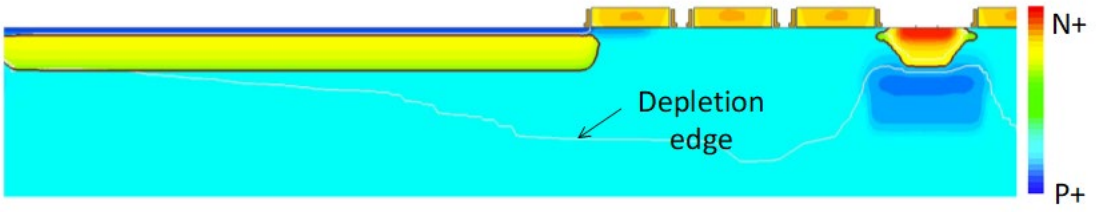


Figure 7-4 Cross-section of the pixel in this process

Equation 7-1 in [95] indicates that the light intensity in silicon (I) follows an exponential decay, where x stands for the depth and α represents the absorption coefficient, inversely proportional to the photon wavelength (λ), as stated in Equation 7-2. Photons with longer wavelengths will generate electron-hole pairs outside the depletion region and may not be collected. Consequently, it is recommended to increase the depletion width of the default photodiode in order to enhance the quantum efficiency (QE) for longer wavelength photons.

$$I = I_0 e^{-\alpha x} \qquad (7-1)$$

$$\alpha = \frac{4\pi k}{\lambda} \qquad (7-2)$$

7.4 Photon Attenuation Layer Integration

In conventional indirect X-ray image sensors, a scintillator is commonly used to convert high-energy X-ray photons into photons in the visible region. However, this method often faces challenges, particularly in terms of low conversion efficiencies for photons with energies exceeding 10 KeV, resulting in fewer photoelectrons. Additionally, the thickness of the scintillator may compromise the spatial resolution of the image sensor.

The thin high-energy X-ray photon energy attenuation layer (PAL), developed at Dartmouth College [96], effectively attenuates high-energy X-ray photons through inelastic scattering to a level of $\leqslant$ 10 KeV. This leads to an increase in the quantum efficiency of the indirect silicon image sensor by over 10 times [4]. Figure 7-5 in [4] illustrates the schematic of the X-ray image sensor based on PAL, with EGL representing the electron generation layer. The next phase of this project is to deposit the PAL onto the sensor.

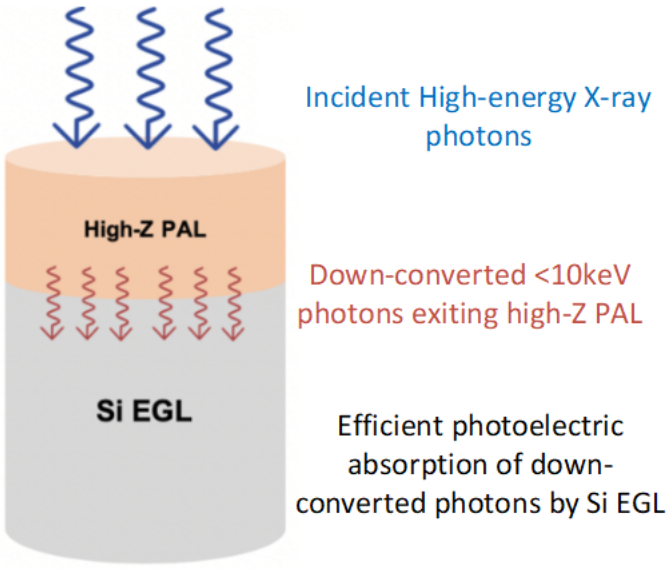


Figure 7-5 Schematic of PAL based X-ray image sensor

7.5 Applications of Charge Sweep Transfer Gate

The introduction and development of the charge sweep transfer gate in this design aimed to create a strong electrical field between the photodiode and the floating diffusion. This design facilitates fast and complete charge transfer and improves pixel conversion gain. However, during the project's development, additional applications for the charge sweep transfer gate were discovered.

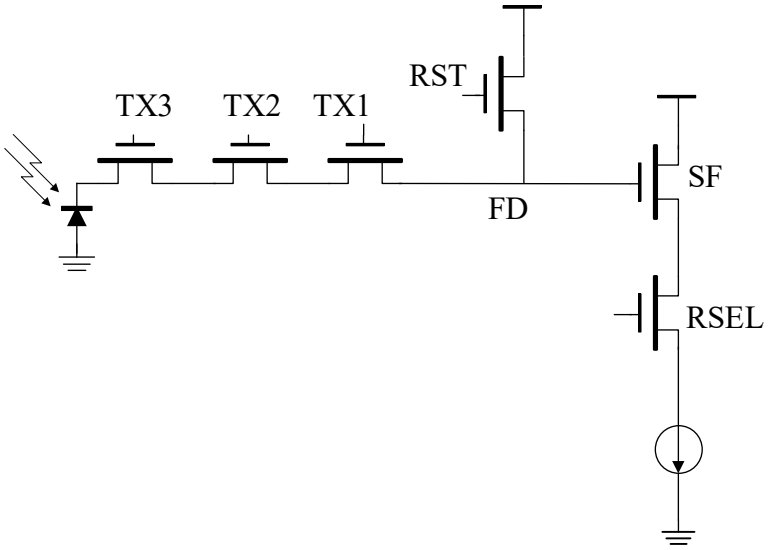


Figure 7-6 A charge-domain storage global shutter pixel based on charge sweep transfer gate

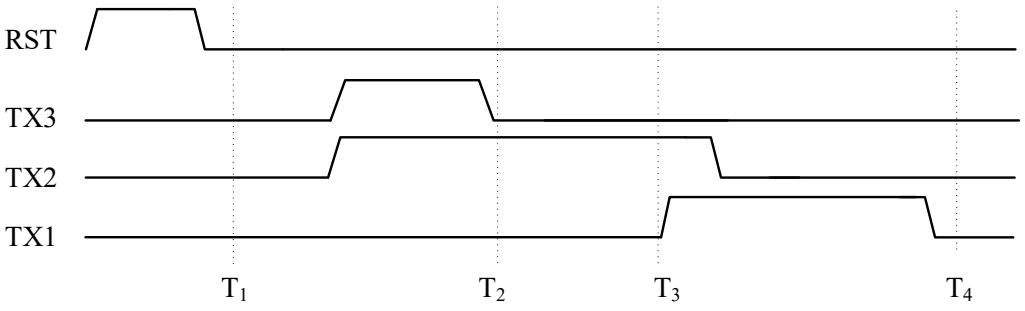


Figure 7-7 Operation timing of the proposed global shutter pixel

Figure 7-6 illustrates a charge domain global shutter pixel that utilizes a charge sweep transfer gate in a standard 4T PPD process. The operational timing of this pixel is demonstrated in Figure 7-7. During the time interval from T_2 to T_3, only TX2 is activated, serving as a temporary charge storage node. Consequently, all pixels can start integration simultaneously, transferring signal charges into the channel beneath the TX2 gate. Then, these charges are read out by sequentially turning off the TX2 gate followed by the TX1 gate. As analyzed in section 5.9, the adoption of charge domain storage can eliminate the kTC noise contribution from the sample and hold capacitor, facilitating further reduction in noise. Furthermore, this design does not require any additional process modifications and can be implemented in a standard 4T PPD process.

Figure 7-8 shows an alternative implementation of the charge sweep transfer gate in order to improve the conversion gain. This is achieved by increasing the separation distance between the FD and TX gate while simultaneously reducing the FD area. The conceptual layouts of a typical 4T pixel and the proposed pixel with the charge sweep transfer gate are depicted in Figure 7-9, clearly illustrating a significant reduction in the FD area for the latter. The operation timing of this approach is shown in Figure 7-10.

It is worth noting that this design shares similarities with the pump gate design discussed in [101], where the FD and TX gates are separated. However, it differs from the pump gate design in that the careful design of the falling edge of the pump gate control signal is not necessary to ensure complete charge transfer. In the case of the charge sweep transfer gate, the channel potential can be conveniently adjusted through the gate's On and Off voltage. Therefore, achieving full charge transfer relies not on the control signal's falling edge but rather on the On and Off voltage of TX2 and TX1, as discussed in section 4.4.

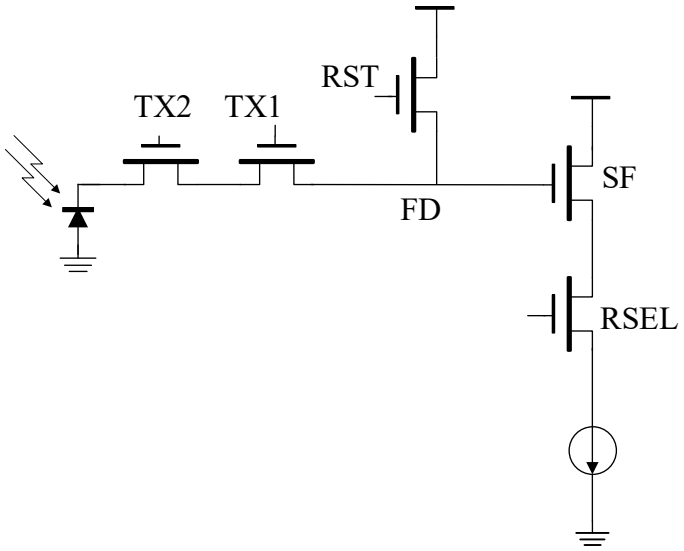


Figure 7-8 Application of charge sweep transfer gate to improve pixel conversion gain

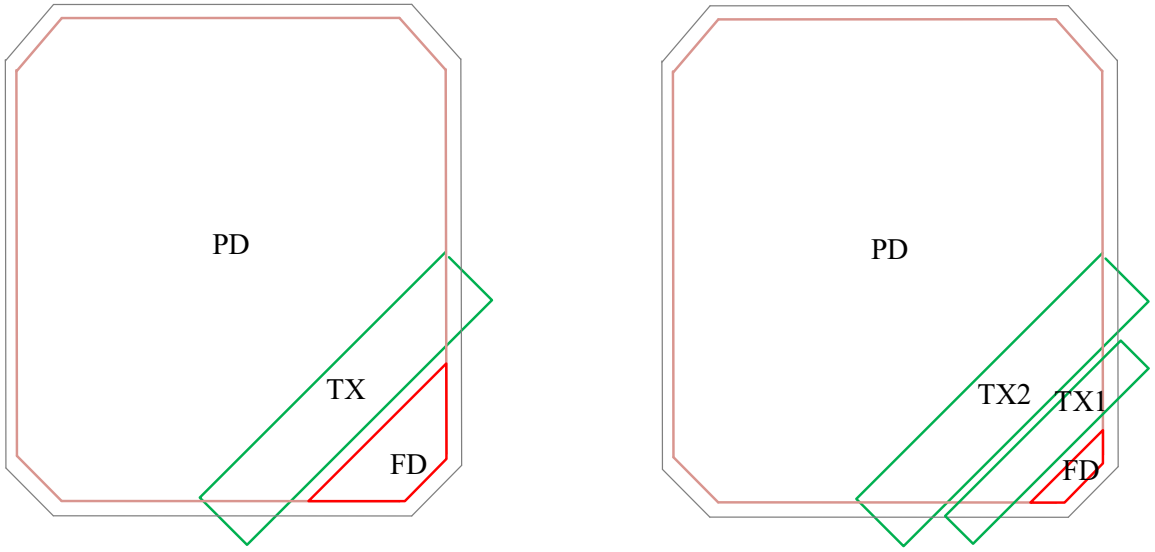


Figure 7-9 Conceptual layout of typical 4T pixel (on the left) and pixel with charge sweep transfer gate (on the right)

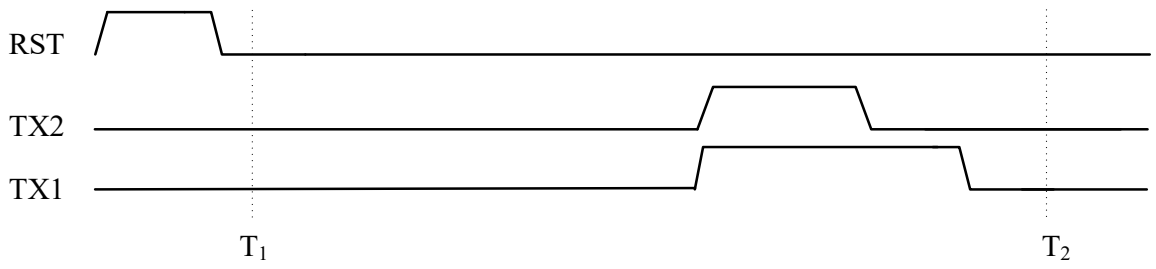


Figure 7-10 Operation timing of the proposed charge sweep-transfer-gate based pixel

7.6 Commercialization

Based on publicly online information, the TMX7510 from Version Research is currently the highest frame rate camera (80 Kfps) commercially available on the market. It is estimated to retail for over $250,000.

The image sensor presented in this thesis is fabricated using a cost-effective 180 nm process without requiring any modifications. Its prototype test system has demonstrated remarkable noise performance at 4 Mfps, making it the image sensor with the lowest noise based on current knowledge. With the future implementation of a customized chip package and optimized software, achieving stable operation at a rate of 20 Mfps becomes highly feasible.

Considering these advantages, there is a viable market for the sensor presented in this thesis if it is commercialized.

8 Conclusions

This thesis presents the development, design, and characterization of an ultra-high-speed burst-mode low-noise CMOS image sensor. The most challenging aspect of the design is implementing the high-speed pixel in a standard 180nm PPD process. Overcoming this challenge involves achieving full charge transfer within 10 ns and minimizing floating diffusion capacitance without any process modifications. To address this, the concept of a process-independent charge sweep transfer gate was invented and optimized. The simulation and measurement results demonstrate a good match in terms of noise, pixel conversion gain, and charge transfer time.

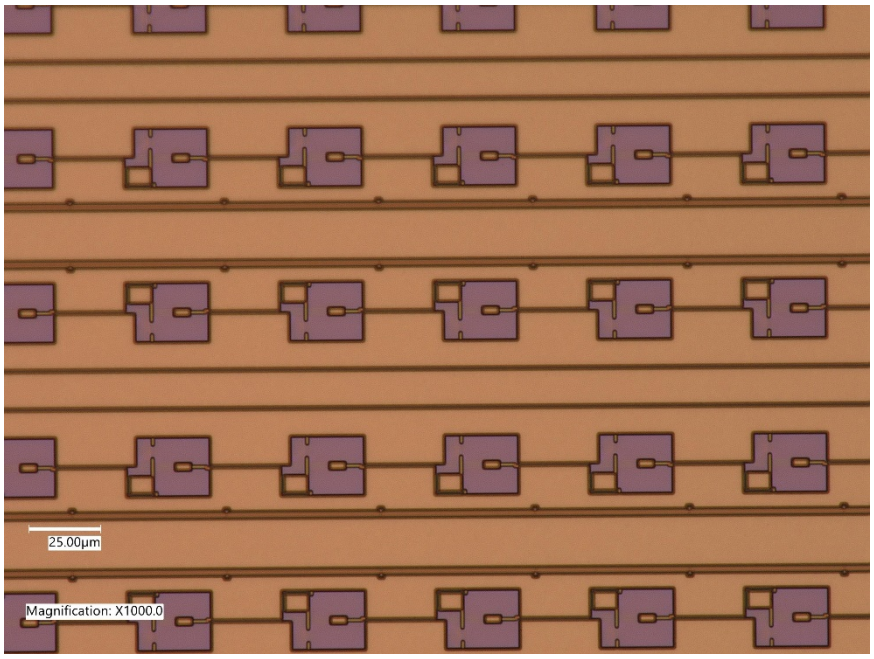
While the dark current of the pixel at room temperature is higher than expected, cooling the system to -17°C significantly reduces the dark current to a negligible level. Current evidence suggests that traps in the silicon body cause the dark current. A better annealing process may potentially resolve the issue of dark current at room temperature.

Despite limitations imposed by the current testing system, the prototype system, including software and hardware, effectively demonstrates its functionality and performance at 4 Mfps. Currently, no commercially available camera system can achieve higher frame rate with lower noise than this work. However, it should be acknowledged that there is still a long way to go from the prototype stage to full commercialization.

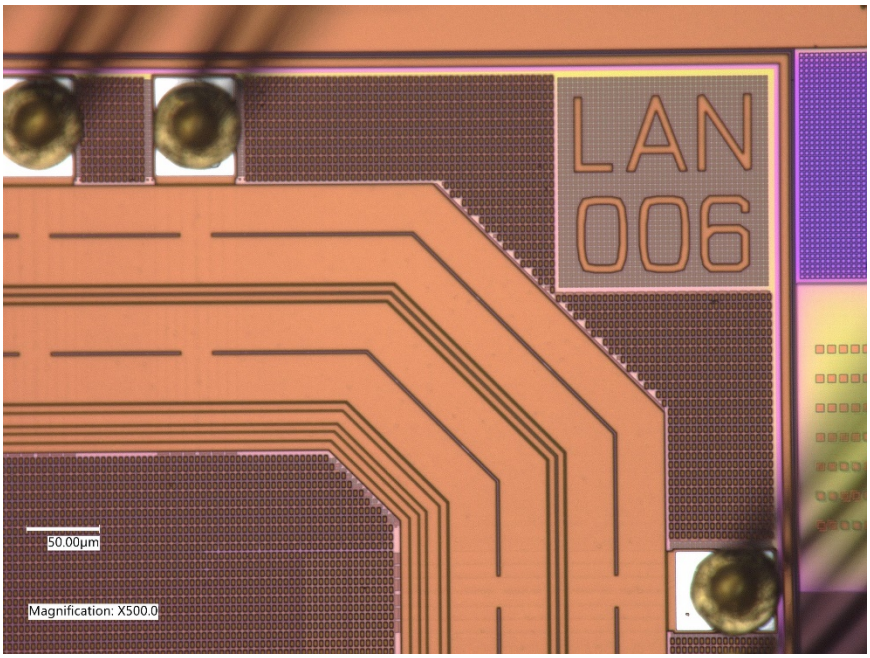
Appendices

Appendix A - Microscopic Images of the Chip

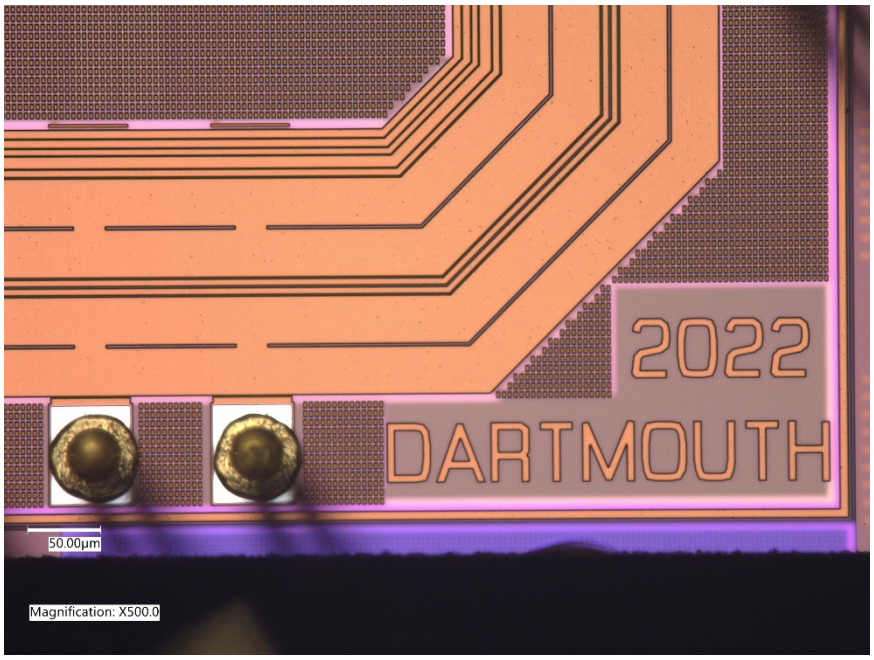
The following figures present high-resolution microscopic images of the image sensor die, showing the pixel array, project code, school logo and author's initial.



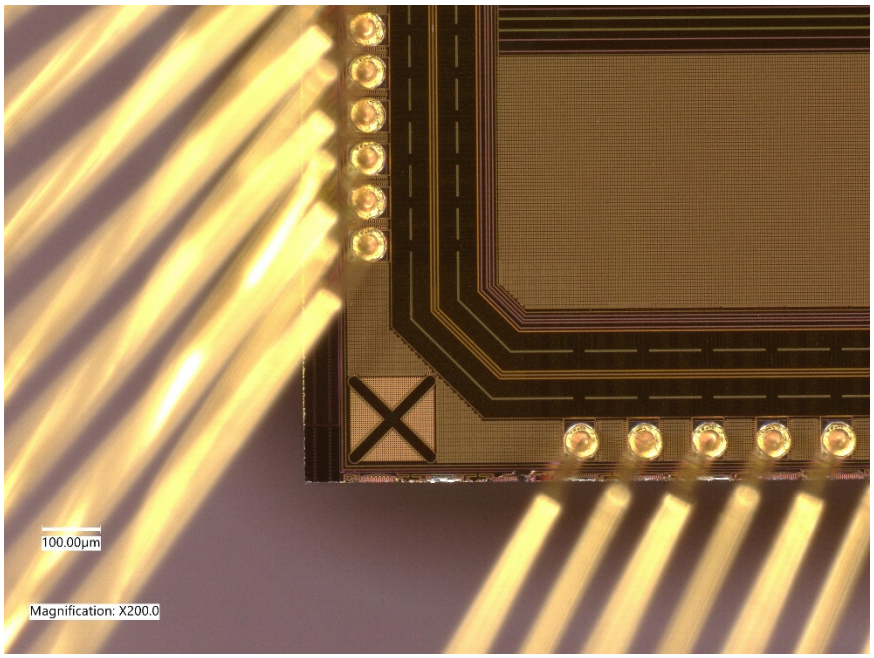
Microscopic image of pixel array



Microscopic image of die corner showing project code



Microscopic image of die corner showing school name



Microscopic image of die corner showing author's initial

Appendix B - Simple Home Lab Setup

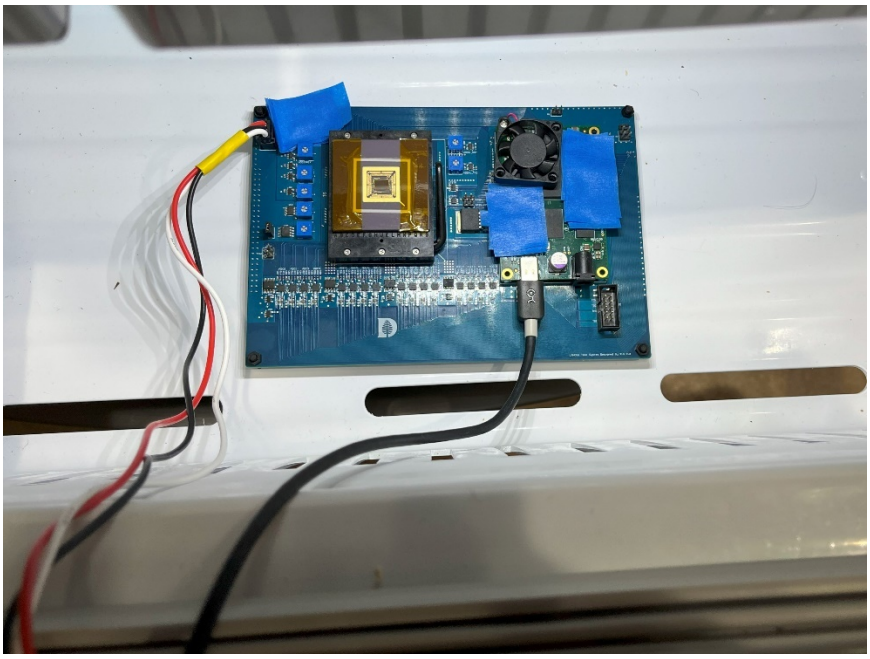
Some of the characterizations are conducted at my home. Due to limited testing equipment, a few daily items have been modified to facilitate the characterization process. The following figures presents the home lab setup.

For the PTC test, an inner cylinder shell of a kitchen paper towel is modified to blend the light emitted by a desk lamp. A translucent water bottle is cut to create a diffusion lens and a closet is been used as the dark room.

For the dark current test, a residential refrigerator is employed as a temperature chamber. Although it can only provide two temperature environments (277 K and 256 K), the test results are satisfactory.

Home lab setup with integrating cylinder, diffusion lens and desk lamp

Home lab setup for dark current measurement (test system in the refrigerator)



Test system in the refrigerator

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