Multilevel Multiphase Space Vector PWM Algorithm

Óscar López, *Member, IEEE*, Jacobo Álvarez, Jesús Doval-Gandoy, *Member, IEEE*, and Francisco D. Freijedo, *Member, IEEE*

***Abstract*—In the last few years, interest in multiphase converter technology has increased due to the benefits of using more than three phases in drive applications. Besides, multilevel converter technology permits the achievement of high power ratings with voltage limited devices. Multilevel multiphase technology combines the benefits of both technologies, but new modulation techniques must be developed in order to take advantage of multilevel multiphase converters. In this paper, a novel space vector pulsewidth modulation (SVPWM) algorithm for multilevel multiphase voltage source converters is presented. This algorithm is the result of the two main contributions of this paper: the demonstration that a multilevel multiphase modulator can be realized from a two-level multiphase modulator, and the development of a new two-level multiphase SVPWM algorithm. The multiphase SVPWM algorithm presented in this paper can be applied to most multilevel topologies; it has low computational complexity and it is suitable for hardware implementations. Finally, the algorithm was implemented in a low-cost field-programmable gate array and it was tested in a laboratory with a real prototype using a five-level five-phase inverter.**

***Index Terms*—Field-programmable gate array (FPGA), modulation algorithm, multilevel multiphase converter, space vector pulsewidth modulation (SVPWM).**

I. Introduction

MOST OF the variable-speed electric drives use three-phase machines. Nevertheless, since variable-speed ac drives include a power electronic converter, the number of machine phases can be higher than three. Major advantages of using a multiphase machine instead of a standard three-phase one are [1], [2]:

1) improved reliability and increased fault tolerance;
2) greater efficiency;
3) higher torque density and reduced torque pulsations;
4) lower per phase power handling requirements;
5) enhanced modularity;
6) improved noise characteristics.

Some recent applications of multiphase systems include high-torque low-speed brushless machines applied to electric vehicle propulsion [3], permanent-magnet motor drives for ship propulsion [4], permanent-magnet motors with low torque pulsation [5], and series-connected two-motor drives with a single inverter supply [6], [7].

Manuscript received February 26, 2007; revised December 11, 2007. This work was supported by the Spanish Ministry of Science and Technology under Project ENE2006-02930.

The authors are with the Department of Electronic Technology, University of Vigo, 36310 Vigo, Spain.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2008.918466

Multilevel converter technology is based on the synthesis of a voltage waveform from several dc voltage levels. As the number of levels increases, the synthesized output voltage gets more steps and produces a waveform which approaches the reference more accurately. The major advantages of using multilevel inverters are [8], [9]:

1) high voltage capability with voltage limited devices;
2) low harmonic distortion;
3) reduced switching losses;
4) increased efficiency;
5) good electromagnetic compatibility.

Multilevel converters have been extensively studied in a wide variety of applications. Recent industrial applications of multilevel inverters include induction machine drives [10], active rectifiers [11], interface of renewable energy sources to the utility grid [12] and static synchronous compensators [13]. Recently, an initial attempt to integrate a multilevel inverter with a multiphase machine was carried out which demonstrated the advantages of combining both technologies [14].

The space vector pulsewidth modulation (SVPWM) technique offers significant performance benefits and has proved to be very popular in three-phase systems [15]. In [16], a simple SVPWM algorithm for multilevel three-phase topologies was presented. The method introduced in [17], for three-phase inverters with neutral, was later extended to four-wire topologies in [18]. Recently, in [19], a new SVPWM method for single-phase converters has been presented. With regard to multilevel multiphase SVPWM, an algorithm for a neutral clamped five-phase inverter was proposed in [20]. However, it does not address the extension of the method for a higher number of levels or phases or its application to other multilevel topologies. In this paper, a generic algorithm to perform the SVPWM for multiphase inverters is presented. This algorithm, which is valid for the typical multilevel topologies, is the result of the two main contributions of this paper: the demonstration that a multilevel multiphase modulator can be realized from a two-level multiphase modulator and the development of a new two-level multiphase SVPWM algorithm.

Some researchers [21]–[25] have proposed multilevel modulation by using the two-level concept for three phase inverters. A new method for the switching time calculation, where the three-level space vector diagram is divided into six two-level space vector diagrams, is introduced in [21]. However, this paper does not include the extension of the method for a number of levels higher than three. In [22], a similar scheme is also presented for a three-level inverter. This scheme cannot be directly applied to a multilevel inverter; nevertheless the principle explained in this paper permits making an N-level SVPWM from

six $(N-1)$-level SVPWM. Therefore, that implies that as the number of levels increases, both complexity and computation cost increase exponentially. In [23], the multilevel space vector diagram is divided into all possible two-level space vector hexagons. After that, a linear transformation is used to find the center of one of those hexagons to calculate the switching times. In [24], a general solution is presented to adapt an existing two-level modulator to a multilevel inverter. This technique requires the storage of switching states with a memory requirement that grows exponentially with the number of inverter levels. A new expression for the duty cycle calculation in two-level inverters is proposed in [25]. The method is also extended to multilevel inverters by adding an offset in the duty-cycle expression. The technique presented in this paper for implementing a multilevel modulator using a two-level modulator can be applied to any number of phases or levels. It has a very low computational cost, which is independent of the number of levels, and it does not require lookup tables.

Most of the two-level SVPWM algorithms [26]–[30] for multiphase voltage converters use a decomposition of voltage vectors in multiple dq planes instead of using original coordinates in the nontransformed space. Although the decomposition offers interesting information about producing-torque and nonproducing-torque components of the voltage [31], the change of the reference frame implies additional calculations. Besides, this representation of the switching vectors in many different planes is complex and difficult to handle in hardware implementations. Although the vector space decomposition approach is valid, it was shown in [32] that SVPWM in multiphase converters is inherently a multidimensional problem and that the vector selection can be formulated directly in a multidimensional space. The new two-level SVPWM algorithm presented in this paper is formulated in the nontransformed multidimensional space for a generic number of phases. The computational cost of the proposed method is low, it does not use trigonometric functions or lookup tables, and it is well suited for real-time hardware implementations.

The proposed multilevel multiphase SVPWM algorithm is the result of combining the new two-level multiphase SVPWM algorithm with the introduced technique to carry out the multilevel modulation by using a two-level modulator. Consequently, it is also valid for any number of phases, it has a low computational cost, and it is well suited for hardware implementations. Moreover, it can be used with a wide variety of multilevel topologies with any number of levels.

The multilevel multiphase SVPWM algorithm was implemented for a five-level five-phase inverter in a low-cost field-programmable gate array (FPGA). The model of the proposed hardware implementation was verified by simulation with Simulink. Finally, the real performance of the modulator was evaluated in the laboratory using a cascaded full-bridge inverter supplying an inductive and resistive load.

This paper is organized as follows. Section II describes the mathematical justification of the SVPWM algorithm in depth. This includes the problem formulation, the demonstration of multilevel modulation in multiphase systems by using the two-level concept and the development of the new two-level multiphase SVPWM algorithm. Additionally, from mathematical treatment, the new multilevel multiphase SVPWM algorithm is obtained. Section III addresses the practical implementation of the algorithm in an FPGA. In Section IV, the implementation is verified by comparing experimental measurements with simulation results. Some experimental results are also given to evaluate the real performance of the implemented modulation algorithm. Section V includes the conclusions of this paper.

II. Algorithm Development

A. Algorithm Formulation

Since the switching states of any power converter topology stay at discrete states, the SVPWM is used to approximate a reference voltage vector $\mathbf{V}_r$ by means of a sequence of space vectors $S_l = \{\mathbf{V}_{s1}, \mathbf{V}_{s2}, \ldots, \mathbf{V}_{sl}\}$ during each modulation cycle. To achieve a proper synthesis of the reference vector, each switching vector $\mathbf{V}_{sj}$ must be applied during an interval T_j in accordance with the following modulation law:

$$\mathbf{V}_r = \frac{1}{T}\sum_{j=1}^{l} \mathbf{V}_{sj} T_j \tag{1}$$

where the sum of the intervals T_j must be equal to the modulation period T

$$\sum_{j=1}^{l} T_j = T. \tag{2}$$

The reference vector summarizes the voltage reference for each phase of the system, whereas each switching vector summarizes the switching state of each phase of the converter

$$\mathbf{V}_r = \left[V_r^1, V_r^2, \ldots, V_r^P\right]^{\mathrm{T}} \in \mathbb{R}^P \tag{3}$$

$$\mathbf{V}_{sj} = \left[V_{sj}^1, V_{sj}^2, \ldots, V_{sj}^P\right]^{\mathrm{T}} \in \mathbb{R}^P. \tag{4}$$

Therefore, the reference vector and the switching vectors belong to the multidimensional space $\mathbb{R}^P$, where P is the number of phases of the converter.

In most common multilevel topologies such as flying capacitor, diode-clamped, cascaded full-bridge or hybrid converters, the output level of every phase V_s is an integer multiple of a fixed voltage step V_{dc} [9], [33]

$$V_s = nV_{\mathrm{dc}}, \qquad n \in \mathbb{Z}. \tag{5}$$

Therefore, vectors and switching times can be normalized by using the voltage step and the switching period, respectively, to nondimensionalize (1) and (2)

$$\mathbf{v}_r = \frac{\mathbf{V}_r}{V_{\mathrm{dc}}} \in \mathbb{R}^P \tag{6}$$

$$\mathbf{v}_{sj} = \frac{\mathbf{V}_{sj}}{V_{\mathrm{dc}}} \in \mathbb{Z}^P \tag{7}$$

$$t_j = \frac{T_j}{T}. \tag{8}$$

It is important to remark that new normalized switching vectors $\mathbf{v}_{sj}$ now belong to the multidimensional space of integer numbers $\mathbb{Z}^P$. If the above expressions are substituted in (1) and (2), the modulation law can be rewritten in terms of the new normalized variables as

$$\mathbf{v}_r = \sum_{j=1}^{l} \mathbf{v}_{sj} t_j \tag{9}$$

$$\sum_{j=1}^{l} t_j = 1. \tag{10}$$

If the reference and the switching normalized vectors are expressed as follows:

$$\mathbf{v}_r = \left[{v_r}^1, {v_r}^2, \ldots, {v_r}^P\right]^{\mathrm{T}} \tag{11}$$

$$\mathbf{v}_{sj} = \left[{v_{sj}}^1, {v_{sj}}^2, \ldots, {v_{sj}}^P\right]^{\mathrm{T}} \tag{12}$$

then (9) and (10) can be rewritten in matrix format as

$$\begin{bmatrix} 1 \\ {v_r}^1 \\ {v_r}^2 \\ \vdots \\ {v_r}^P \end{bmatrix} = \begin{bmatrix} 1 & 1 & \ldots & 1 \\ v_{s1}^1 & v_{s2}^1 & \ldots & v_{sl}^1 \\ v_{s1}^2 & v_{s2}^2 & \ldots & v_{sl}^2 \\ \vdots & \vdots & \ddots & \vdots \\ v_{s1}^P & v_{s2}^P & \ldots & v_{sl}^P \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ \vdots \\ t_l \end{bmatrix}. \tag{13}$$

The above system of linear equations constitutes the modulation law, which must be solved by the multilevel multiphase SVPWM algorithm. The problem solving includes three main steps:

1) searching a set of integer coefficients for the matrix that permits solving the linear system;
2) solving the system of linear equations to calculate the switching times;
3) extracting the switching vector sequence from the coefficient matrix.

The multilevel multiphase SVPWM problem can be simplified if it is decomposed into the sum of a displacement plus a two-level SVPWM problem with the same number of phases.

B. Algorithm Decomposition

The reference vector can be decomposed into the sum of its integer and fractional parts

$$\mathbf{v}_r = \mathbf{v}_i + \mathbf{v}_f, \qquad \mathbf{v}_i = \mathrm{integ}(\mathbf{v}_r) \in \mathbb{Z}^P. \tag{14}$$

Components of the new vector $\mathbf{v}_i$ are integer numbers, and therefore it belongs to the same space $\mathbb{Z}^P$ of the switching vectors and it could be directly synthesized with one of them. The fractional part $\mathbf{v}_r$ still belongs to the space $\mathbb{R}^P$ and it cannot be directly synthesized by means of a single switching vector. It has to be approximated with a sequence of switching vectors.

Besides, a new set of switching vectors is obtained by displacing all switching vectors the distance given by $\mathbf{v}_i$

$$\mathbf{v}_{dj} = \mathbf{v}_{sj} - \mathbf{v}_i. \tag{15}$$

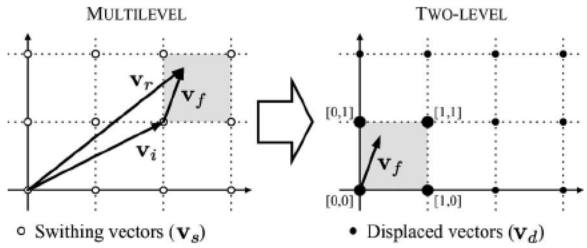


Fig. 1. Example of decomposition in the 2-D problem.

If those vectors are expressed as

$$\mathbf{v}_i = \left[{v_i}^1, {v_i}^2, \ldots, {v_i}^P\right]^{\mathrm{T}} \tag{16}$$

$$\mathbf{v}_f = \left[{v_f}^1, {v_f}^2, \ldots, {v_f}^P\right]^{\mathrm{T}} \tag{17}$$

$$\mathbf{v}_{dj} = \left[v_{dj}^1, v_{dj}^2, \ldots, v_{dj}^P\right]^{\mathrm{T}} \tag{18}$$

and if (15) is substituted in (13), the new expression for the modulation law is obtained

$$\begin{bmatrix} 1 \\ {v_r}^1 \\ {v_r}^2 \\ \vdots \\ {v_r}^P \end{bmatrix} = \begin{bmatrix} 0 \\ {v_i}^1 \\ {v_i}^2 \\ \vdots \\ {v_i}^P \end{bmatrix} + \begin{bmatrix} 1 & 1 & \ldots & 1 \\ v_{d1}^1 & v_{d2}^1 & \ldots & v_{dl}^1 \\ v_{d1}^2 & v_{d2}^2 & \ldots & v_{dl}^2 \\ \vdots & \vdots & \ddots & \vdots \\ v_{d1}^P & v_{d2}^P & \ldots & v_{dl}^P \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ \vdots \\ t_l \end{bmatrix}. \tag{19}$$

Finally, if (14) is written as

$$\begin{bmatrix} 1 \\ {v_r}^1 \\ {v_r}^2 \\ \vdots \\ {v_r}^P \end{bmatrix} = \begin{bmatrix} 0 \\ {v_i}^1 \\ {v_i}^2 \\ \vdots \\ {v_i}^P \end{bmatrix} + \begin{bmatrix} 1 \\ {v_f}^1 \\ {v_f}^2 \\ \vdots \\ {v_f}^P \end{bmatrix} \tag{20}$$

and if (19) and (20) are compared, the following relationship between the fractional part of the reference and the displaced switching vectors is obtained:

$$\begin{bmatrix} 1 \\ {v_f}^1 \\ {v_f}^2 \\ \vdots \\ {v_f}^P \end{bmatrix} = \begin{bmatrix} 1 & 1 & \ldots & 1 \\ v_{d1}^1 & v_{d2}^1 & \ldots & v_{dl}^1 \\ v_{d1}^2 & v_{d2}^2 & \ldots & v_{dl}^2 \\ \vdots & \vdots & \ddots & \vdots \\ v_{d1}^P & v_{d2}^P & \ldots & v_{dl}^P \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ \vdots \\ t_l \end{bmatrix}. \tag{21}$$

This new system of linear equations presents the same form as the general modulation law (13). However, in this case, the components of vector $\mathbf{v}_f$ are bounded in the interval $[0, 1)$. Therefore, only the subset of displaced vectors with components zero or one is enough to carry out the reference approximation. Consequently, this new equation represents a two-level modulator where the reference vector is $\mathbf{v}_f$ and the array of switching vectors are the displaced set of switching vectors $\mathbf{v}_{dj}$. Switching times are the same in the multilevel and the two-level modulators. Fig. 1 shows a 2-D example of the decomposition where vector $\mathbf{v}_i$ coincides with a switching vector and the subset $\{[0, 0], [1, 0], [0, 1], [1, 1]\}$ of displaced vectors is enough to synthesize the fractional part of the reference $\mathbf{v}_f$.

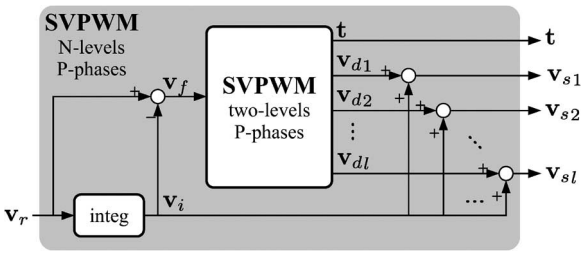


Fig. 2. Block diagram of the multilevel multiphase SVPWM.

In summary, (19) demonstrates that a multilevel multiphase modulator can be realized from a displacement plus a two-level modulator with the same number of phases. Fig. 2 shows a block diagram of the proposed technique.

C. Two-Level Multiphase SVPWM Algorithm

Once the multilevel problem has been decomposed, the two-level modulation law (21) has to be solved. To obtain an exactly determined system of linear equations, the coefficient matrix of that modulation law must be a square matrix. Hence, the length of the switching vector sequence S_l must be

$$l = P + 1 \tag{22}$$

and the particular linear system, which has to be solved, is

$$\begin{bmatrix} 1 \\ {v_f}^1 \\ {v_f}^2 \\ \vdots \\ {v_f}^P \end{bmatrix} = \begin{bmatrix} 1 & 1 & \dots & 1 \\ v_{d1}^1 & v_{d2}^1 & \dots & v_{dP+1}^1 \\ v_{d1}^2 & v_{d2}^2 & \dots & v_{dP+1}^2 \\ \vdots & \vdots & \ddots & \vdots \\ v_{d1}^P & v_{d2}^P & \dots & v_{dP+1}^P \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ \vdots \\ t_{P+1} \end{bmatrix}. \tag{23}$$

The objective of the two-level modulation algorithm is to find a switching vector sequence, that is, the coefficient matrix of the system (23) should be filled with zeros and ones, thus allowing a subsequent system solution. Moreover, the coefficient selection must be carried out taking into account that the switching times must be always positive after the system solution.

There are many different possibilities to fill the coefficient matrix. Nevertheless, the whole power system performance depends on the method employed for calculating the coefficient matrix. In this way, switching losses are minimized if coefficients are selected in such a way that consecutive switching vectors of the switching sequence are adjacent. In other words, only one coefficient is different in two consecutive matrix columns. One possible method for calculating such a matrix is detailed below.

Equation (23) can be written in a shorter form as

$$\begin{bmatrix} 1 \\ \mathbf{v}_f \end{bmatrix} = \mathbf{D}\mathbf{t}. \tag{24}$$

Finding a permutation matrix $\mathbf{P}$ that puts the elements of the reference vector $\mathbf{v}_f$ in descending order

$$\mathbf{P}\begin{bmatrix} 1 \\ \mathbf{v}_f \end{bmatrix} = \begin{bmatrix} 1 \\ \hat{\mathbf{v}}_f \end{bmatrix} \tag{25}$$

where

$$1 > {\hat{v}_f}^1 \geq \dots \geq {\hat{v}_f}^{k-1} \geq {\hat{v}_f}^k \geq \dots \geq {\hat{v}_f}^P \geq 0 \tag{26}$$

and multiplying both sides of (24) by this permutation matrix $\mathbf{P}$, we obtain the following equation:

$$\begin{bmatrix} 1 \\ \hat{\mathbf{v}}_f \end{bmatrix} = \hat{\mathbf{D}}\mathbf{t} \tag{27}$$

where

$$\hat{\mathbf{D}} = \mathbf{P}\mathbf{D}. \tag{28}$$

One coefficient matrix $\hat{\mathbf{D}}$ with adjacent consecutive columns that makes this new system of linear equations exactly determined is the following upper triangular matrix:

$$\hat{\mathbf{D}} = \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ & 1 & 1 & \dots & 1 \\ & & \ddots & \ddots & \vdots \\ & & & \ddots & 1 \\ 0 & & & & 1 \end{bmatrix}. \tag{29}$$

As it will be shown below, the switching times obtained with this coefficient matrix are always positive.

A permutation matrix is an orthogonal matrix so $\mathbf{P}$ is invertible and

$$\mathbf{P}^{-1} = \mathbf{P}^{\mathrm{T}}. \tag{30}$$

Therefore, the coefficient matrix $\mathbf{D}$ of the two-level modulation law can be obtained by solving (28) as

$$\mathbf{D} = \mathbf{P}^{\mathrm{T}}\hat{\mathbf{D}}. \tag{31}$$

The permutation matrix $\mathbf{P}$ applies a set of elementary row-switching transformations to the column vector $\mathbf{v}_f$. In the same manner, the inverse set of elementary row-switching transformations is applied to the matrix $\hat{\mathbf{D}}$ by the matrix $\mathbf{P}^{\mathrm{T}}$ and, consequently, the number of ones and zeros in each column does not change. Hence, the switching number is minimized because consecutive vectors of the sequence are still adjacent after the transformation.

Due to the fact that the solution $\mathbf{t}$ is the same for both linear systems, (24) and (27), it can be calculated by using either of them. The second option seems the best choice because, in this case, the solution is trivial as shown below

$$t_j = \begin{cases} 1 - {\hat{v}_f}^1, & \text{if } j = 1 \\ {\hat{v}_f}^{j-1} - {\hat{v}_f}^j, & \text{if } 2 \leq j \leq P \\ {\hat{v}_f}^P, & \text{if } j = P+1. \end{cases} \tag{32}$$

All intervals calculated by means of the above expression will always be positive numbers because the coordinates of the vector $\hat{v}_f$ obey (26).

In summary, matrix $\mathbf{D}$ permits solving the two-level modulation law getting positive switching times and minimizing switching number. The two-level switching sequence can be directly extracted from the columns of that matrix. Fig. 3

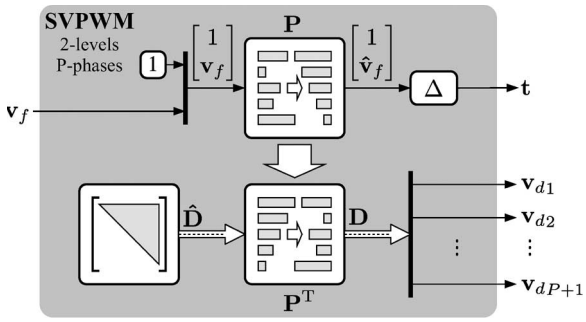


Fig. 3. Block diagram of the two-level multiphase SVPWM.

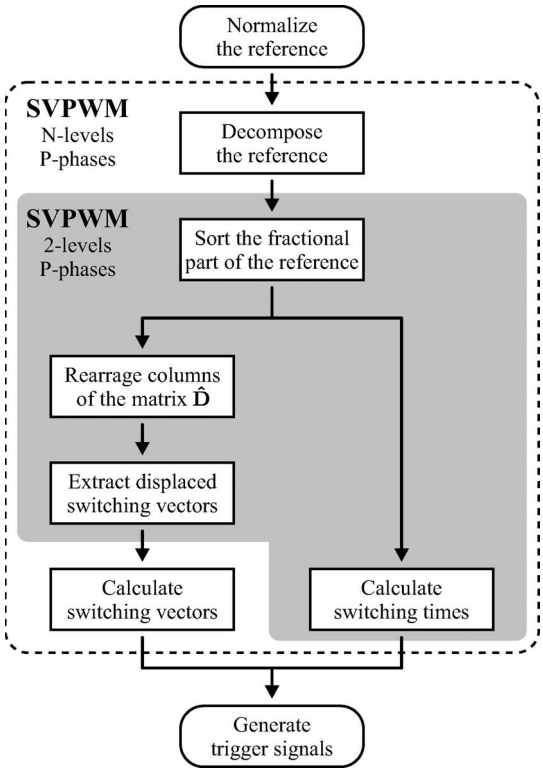


Fig. 4. Algorithm flow chart.

shows the block diagram of the proposed two-level multiphase SVPWM.

D. Multilevel Multiphase SVPWM Algorithm

The proposed multilevel multiphase PWM algorithm is derived from the previous mathematical treatment. The steps of this algorithm are summarized in the flow chart in Fig. 4. First, the normalized reference $\mathbf{v}_r$ must be calculated from the reference voltage vector using the expression (7). Second, the normalized reference has to be decomposed into the sum of its integer part $\mathbf{v}_i$ and its fractional part $\mathbf{v}_f$ by using the expression in (14). After that, the elements of the fractional part of the reference have to be sorted out in descending order to obtain the vector $\mathbf{v}_f$. Information about the tasks done in the sorting process (summarized in the permutation matrix $\mathbf{P}$) will be used to rearrange the rows of the matrix $\hat{\mathbf{D}}$ to obtain the matrix $\mathbf{D}$. The next step is to extract the displaced switching vectors $\mathbf{v}_{dj}$ from the matrix $\mathbf{D}$ by taking into account

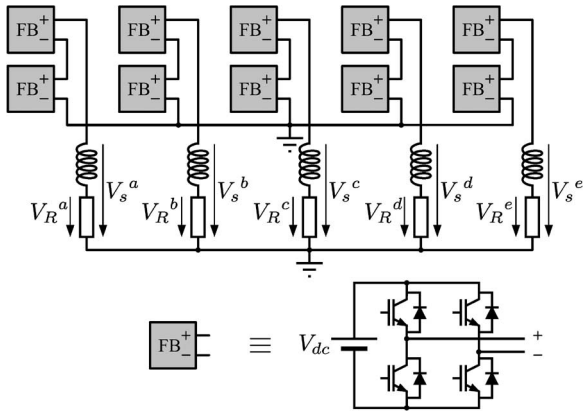


Fig. 5. Five-level five-phase cascaded full-bridge inverter.

the expression (23). The final switching vectors $\mathbf{v}_{sj}$ must be calculated by adding the integer part of the reference $\mathbf{v}_i$ to the displaced switching vectors $\mathbf{v}_{dj}$ according to expression (15). The time corresponding to each switching vector is calculated directly from components of $\hat{\mathbf{v}}_f$ by using (32). Finally, trigger signals have to be generated from the switching vectors and the switching times. The relationship between switching states and the particular trigger signals of transistors depends on the multilevel topology.

The simplicity of the algorithm is here shown by means of an example in which the steps of the previous flow chart are followed. Let us consider a multiphase drive where the voltage reference for each phase k is purely sinusoidal

$$V_r{}^k = A\sin\left(wt + 2\pi\frac{k-1}{P}\right), \qquad k = 1,\ldots,P. \tag{33}$$

If a voltage amplitude $A = 32$ V and a speed $w = 2\pi$ 50 rd/s is considered, the instantaneous reference for a five-phase drive when $t = 3.51$ ms is

$$\mathbf{V}_r = [28.6, 22.6, -14.6, -31.6, -5.0]^{\mathrm{T}}\ \mathrm{V}. \tag{34}$$

If (22) is taken into account, the switching sequence will have six switching vectors: $\mathbf{v}_{s1}$, $\mathbf{v}_{s2}$, $\mathbf{v}_{s3}$, $\mathbf{v}_{s4}$, $\mathbf{v}_{s5}$, and $\mathbf{v}_{s6}$. From (6), if voltage step of the converter is $V_{\mathrm{dc}} = 20$ V, then normalized voltage reference is

$$\mathbf{v}_r = \frac{\mathbf{V}_r}{V_{\mathrm{dc}}} = [1.43, 1.13, -0.73, -1.58, -0.25]^{\mathrm{T}}. \tag{35}$$

By means of (14), this vector is decomposed into an integer and a fractional part

$$\mathbf{v}_i = \mathrm{integ}(\mathbf{v}_r) = [1, 1, -1, -2, -1]^{\mathrm{T}} \tag{36}$$

$$\mathbf{v}_f = \mathbf{v}_r - \mathbf{v}_i = [0.43, 0.13, 0.27, 0.42, 0.75]^{\mathrm{T}}. \tag{37}$$

If the elements of the vector $\mathbf{v}_f$ are sorted out in descending order, the following vector is obtained:

$$\hat{\mathbf{v}}_f = [0.75, 0.43, 0.42, 0.27, 0.13]^{\mathrm{T}}. \tag{38}$$

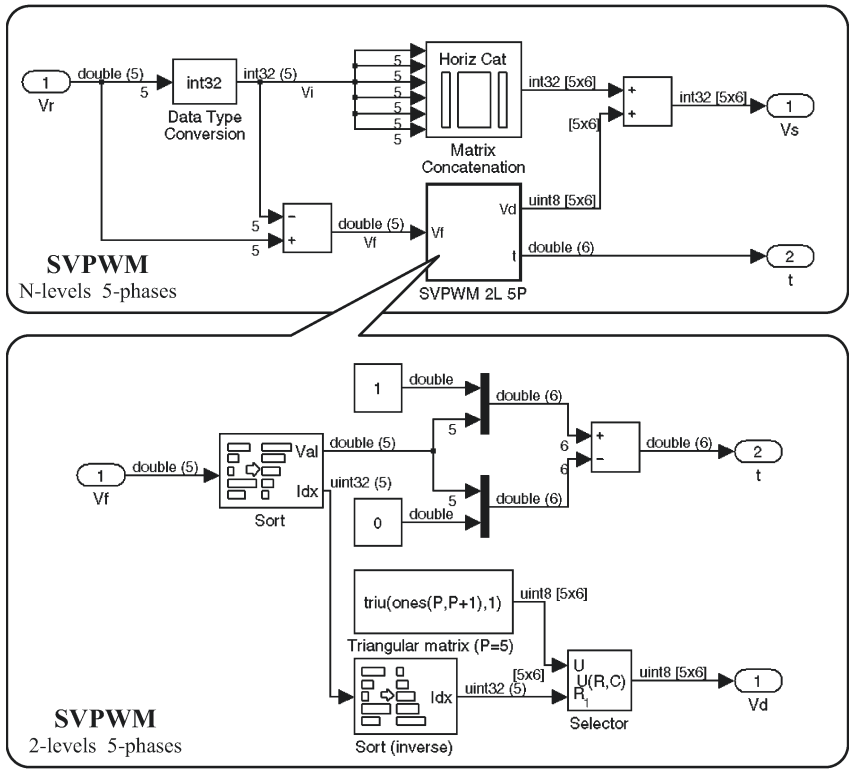


Fig. 6. Simulink model of the hardware implementation of the SVPWM algorithm.

In accordance with (25), the permutation matrix that carries out the above sorting operation is

$$\mathbf{P} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}. \tag{39}$$

The coefficient matrix $\mathbf{D}$ is calculated using the expression in (31) as

$$\mathbf{D} = \mathbf{P}^{\mathrm{T}}\hat{\mathbf{D}} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}. \tag{40}$$

The displaced switching vectors can be extracted from this matrix by means of the expression in (23)

$$\begin{aligned} \mathbf{v}_{d1} &= [0,0,0,0,0]^{\mathrm{T}} \\ \mathbf{v}_{d2} &= [0,0,0,0,1]^{\mathrm{T}} \\ \mathbf{v}_{d3} &= [1,0,0,0,1]^{\mathrm{T}} \\ \mathbf{v}_{d4} &= [1,0,0,1,1]^{\mathrm{T}} \\ \mathbf{v}_{d5} &= [1,0,1,1,1]^{\mathrm{T}} \\ \mathbf{v}_{d6} &= [1,1,1,1,1]^{\mathrm{T}}. \end{aligned} \tag{41}$$

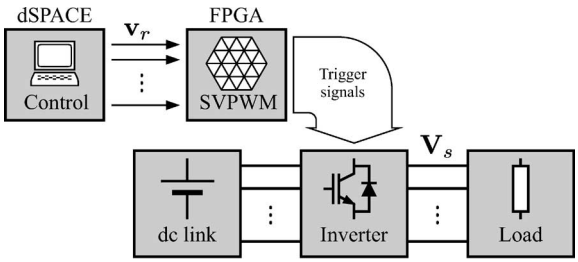
TABLE I
RESOURCES SUMMARY

Target Device	: xc3s200			
Number of Slice Flip Flops:	2,523	out of	3,840	65%
Number of 4 input LUTs:	2,718	out of	3,840	70%
Number of occupied Slices:	1,918	out of	1,920	99%
Total Number 4 input LUTs:	2,762	out of	3,840	71%
Number of bonded IOBs:	99	out of	173	57%
IOB Flip Flops:	75			
Number of Block RAMs:	0	out of	12	0%
Number of MULT18X18s:	0	out of	12	0%
Number of GCLKs:	8	out of	8	100%
Number of Startups:	1	out of	1	100%
Total equivalent gate count for design:	38,765			

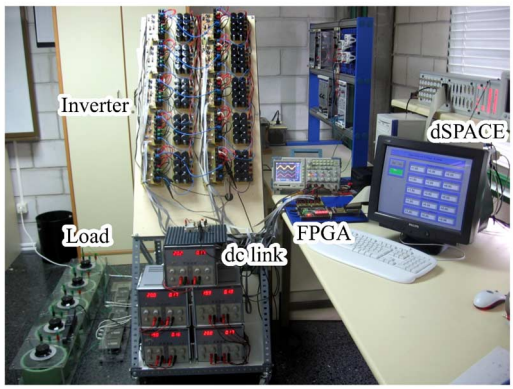
From (15), the final switching sequence can be calculated by adding the shifting vector $\mathbf{v}_i$ to those vectors

$$\begin{aligned} \mathbf{v}_{s1} &= \mathbf{v}_i + \mathbf{v}_{d1} = [1,1,-1,-2,-1]^{\mathrm{T}} \\ \mathbf{v}_{s2} &= \mathbf{v}_i + \mathbf{v}_{d2} = [1,1,-1,-2,0]^{\mathrm{T}} \\ \mathbf{v}_{s3} &= \mathbf{v}_i + \mathbf{v}_{d3} = [2,1,-1,-2,0]^{\mathrm{T}} \\ \mathbf{v}_{s4} &= \mathbf{v}_i + \mathbf{v}_{d4} = [2,1,-1,-1,0]^{\mathrm{T}} \\ \mathbf{v}_{s5} &= \mathbf{v}_i + \mathbf{v}_{d5} = [2,1,0,-1,0]^{\mathrm{T}} \\ \mathbf{v}_{s6} &= \mathbf{v}_i + \mathbf{v}_{d6} = [2,2,0,-1,0]^{\mathrm{T}}. \end{aligned} \tag{42}$$

As expected, consecutive vectors of the sequence are adjacent. Therefore, the number of switchings is minimized.



(a)



(b)

Fig. 7. Experimental test setup. (a) Diagram. (b) Photograph.

Finally, the switching times are calculated from the ordered reference vector $\hat{\mathbf{v}}_f$ by means of the equation in (32)

$$\begin{aligned} t_1 &= 1 - \hat{v}_f{}^a = 0.25 \\ t_2 &= \hat{v}_f{}^a - \hat{v}_f{}^b = 0.32 \\ t_3 &= \hat{v}_f{}^b - \hat{v}_f{}^c = 0.01 \\ t_4 &= \hat{v}_f{}^c - \hat{v}_f{}^d = 0.15 \\ t_5 &= \hat{v}_f{}^d - \hat{v}_f{}^e = 0.14 \\ t_6 &= \hat{v}_f{}^e = 0.13. \end{aligned} \tag{43}$$

E. Algorithm Features

The computational cost of the presented SVPWM algorithm is low and it is independent of the number of levels. However, it grows slightly with the number of phases because the vector $\mathbf{v}_f$ includes more components which must be sorted out. Besides, lookup tables, trigonometric functions or memories to store predefined switching sequences are not needed. Hence, the algorithm is well suited for real-time implementation in low-cost devices.

Several previous two-level multiphase SVPWM algorithms only use a subset of the space vectors [34] for practical reasons because of the high number (2^P) of available space vectors in multiphase systems. Nevertheless, in the proposed modulation technique, even with the higher number (N^P) of available space vectors in multilevel multiphase converters, all space vectors are handled by the algorithm without discarding any of them. In addition, the provided switching vector sequence is so that it minimizes the number of switchings. Hence, no extra effort is needed to achieve this significant goal.

If the modulation index m is defined as the ratio of the peak fundamental of the output voltage to the dc voltage step

$$m = \frac{V_{\text{fund}}}{V_{\text{dc}}} \tag{44}$$

and if harmonic injection is not considered, the modulation index has a range of

$$0 \leq m \leq \frac{N-1}{2}. \tag{45}$$

III. Algorithm Hardware Implementation

The Digilent S3 board was used to implement the new SVPWM algorithm for the five-level five-phase cascaded full bridge inverter in Fig. 5. This board hosts a XC3S200 FPGA from Xilinx which has 4.320 logic cells each constituted by two 16×1 lookup tables and two flip-flops. Before the VHDL description was carried out, the model of the hardware implementation was first tested by simulation using the Simulink model in Fig. 6. The algorithm implementation follows the flow chart in Fig. 4. The integer part of the reference $\mathbf{v}_i$ is calculated by the block `Data Type Conversion`. The fractional part of the reference $\mathbf{v}_f$ feeds the block `SVPWM 2L 5P`. This block is a two-level five-phase modulator that provides the displaced switching vectors $\mathbf{v}_{dj}$ and the switching times $\mathbf{t}$. Switching vectors $\mathbf{v}_{sj}$ that form the final switching sequence are calculated by adding the integer part of the reference to each displaced switching vector. Switching times are simply those ones provided by the two-level modulator block.

Although the matrix approximation of the two-level problem is useful for the algorithm demonstration, it is inefficient in the hardware implementation to calculate the permutation matrix and the matrix operations. Therefore, the $\mathbf{P}$ calculation and the operations made with it were replaced by sorting algorithms that provide the same result. In addition, the first row of matrices $\hat{\mathbf{D}}$ and $\mathbf{D}$, which are also useful in the algorithm demonstration, was not taken into account in the implementation because these rows are always constant and they are not needed for extracting the switching vectors $\mathbf{v}_d$. The implementation of the block `SVPWM 2L 5P` is detailed at the bottom of Fig. 6 where the block `Sort` calculates the ordered vector $\hat{\mathbf{v}}_f$ and the vector of indices `Idx` that summarizes the permutations carried out in the sorting process of $\mathbf{v}_f$. The vector $\hat{\mathbf{v}}_f$ is required to calculate the switching times. The indices `Idx` are used by the block `Sort (inverse)` to select the rows of the matrix $\hat{\mathbf{D}}$ (without the first row) provided by the block `Triangular matrix`. The output of the `Selector` block is the two-level switching vector sequence.

Finally, the algorithm was described in VHDL by following the block diagram of Simulink. An extra block was added to translate the switching vectors into the trigger signals for controlling the five-level cascaded full-bridge inverter. Table I shows the summary of resources used by the implementation. It is important to remark that block RAMs and multipliers available in the FPGA were not used because the algorithm does not need data storage or multiplication operations.

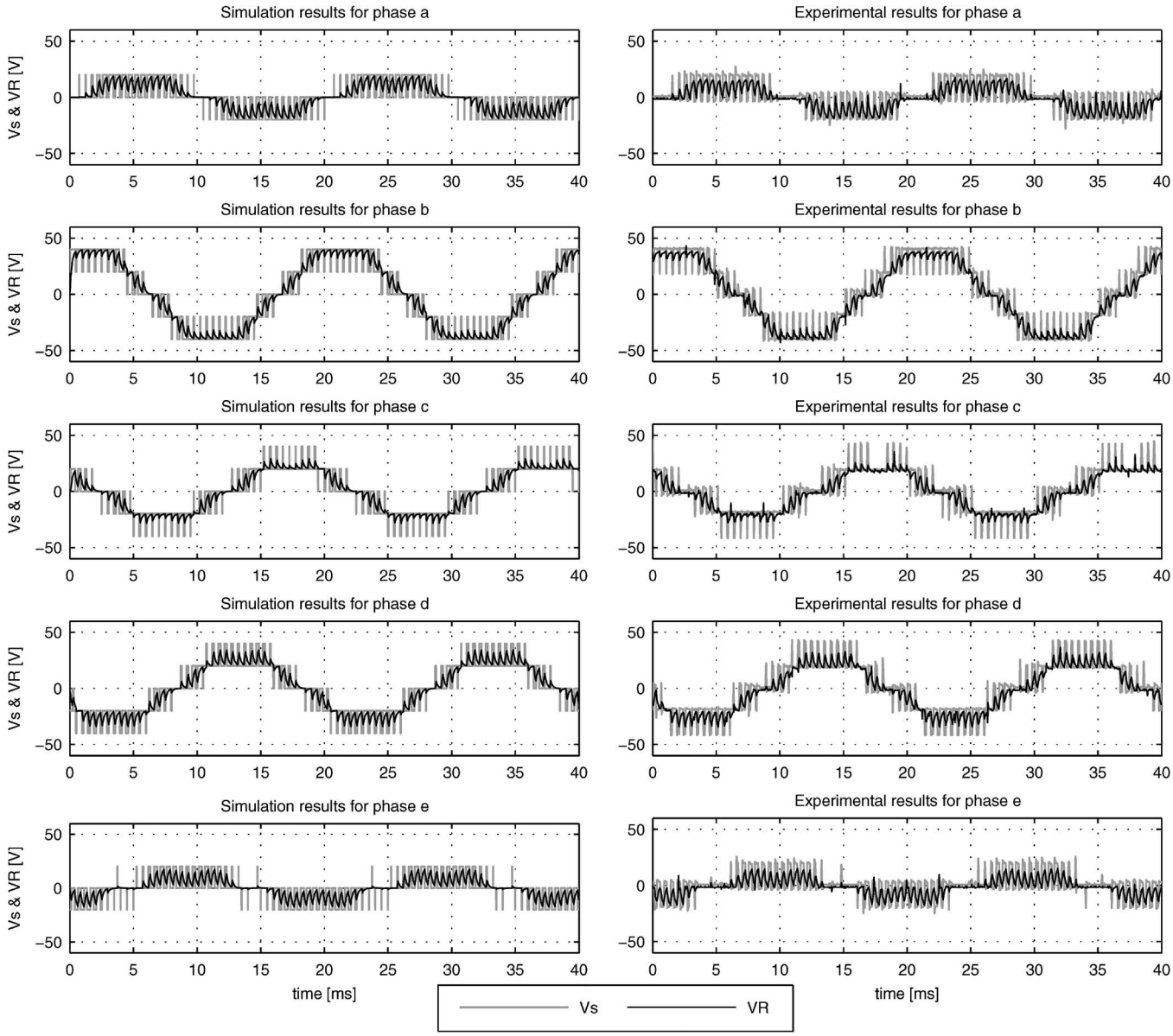


Fig. 8. Comparison of experimental measurements with simulation results.

IV. Experimental Results

The SVPWM algorithm was tested by using a low-power laboratory prototype. Fig. 7 shows the block diagram and a photograph of the experimental setup that includes the FPGA, a dSPACE platform, the inverter and the load. The dSPACE DS1103 PPC Controller Board provides the reference vectors to the FPGA. The trigger signals generated by the FPGA control the transistors of the multilevel inverter. The five-level five-phase cascaded full-bridge inverter shown in Fig. 5, with 3125 different switching states, was used in the experiments. The dc source voltage of all full-bridge cells is 20 V; therefore the inverter voltage step $V_{\rm dc}$ is 20 V as well. A 100 Ω resistive load with a series connected 15 mH inductance was used in tests.

The simulation model of the experimental setup was done in Simulink and it includes the algorithm implementation previously shown in Fig. 6. The inverter and the load were modeled using the SimPowerSystem toolbox. Fig. 8 compares simulation results with experimental measurements. A low switching frequency (2 kHz) was selected to make the comparison easier. To observe the behavior of the modulator with a generic input, a 50 Hz unbalanced reference with a fifth harmonic was considered. Fig. 8 shows a good agreement between the simulation model and the experimental setup. Measurements of voltage across load resistances and inverter output are very similar to simulation results, except for some lost switching pulses due to the dead time included in trigger signals which was not considered in the simulation model. To test the performance of the proposed SVPWM algorithm, the case of sinusoidal output voltage with harmonic injection, typically used in concentrated winding ac machines for torque enhancement, was considered. In all the tests made, the voltage reference had a 50 Hz fundamental frequency and the output switching frequency was 10 kHz. Four cases were considered in tests: two cases with purely sinusoidal output voltage with normalized amplitudes

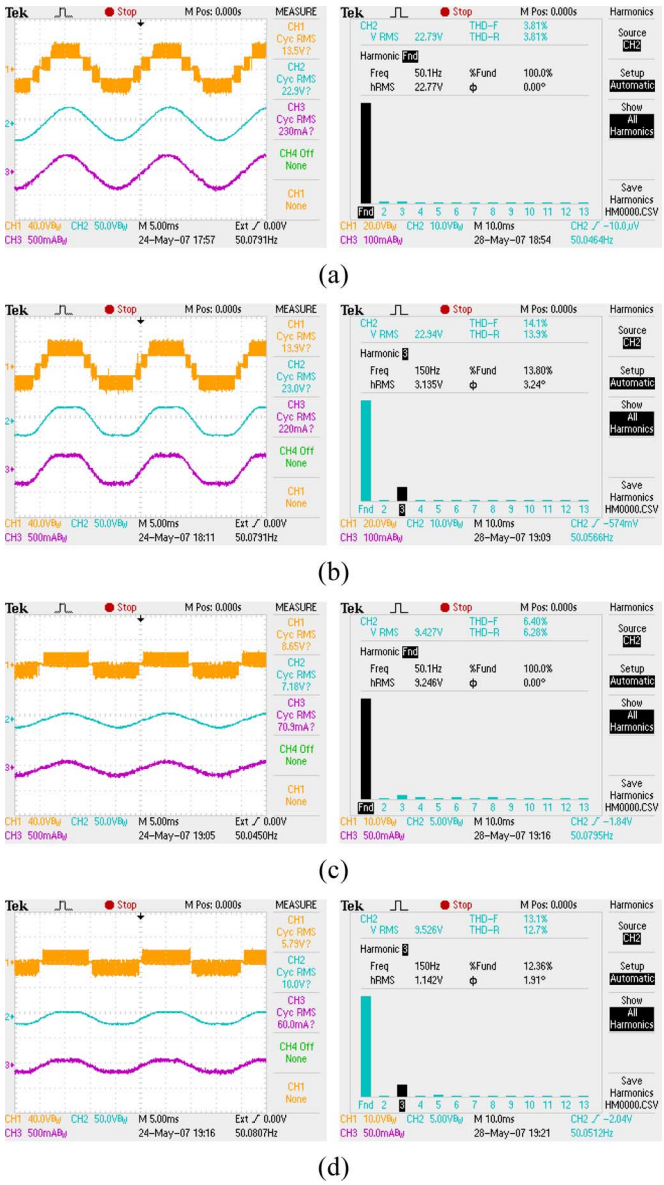


Fig. 9. Phase a experimental results. Ch1: inverter output voltage; Ch2: filtered inverter output voltage; Ch3: phase current. (a) $m_1 = 1.80$, $m_3 = 0.00$. (b) $m_1 = 1.80$, $m_3 = 0.30$. (c) $m_1 = 0.80$, $m_3 = 0.00$. (d) $m_1 = 0.80$, $m_3 = 0.13$.

$m_1 = 1.8$ and $m_1 = 0.8$ and two additional cases where a third harmonic with magnitude $m_3 = m_1/6$ has been injected.

Fig. 9 shows the inverter voltage and phase current waveforms, besides the low-order voltage harmonics of the inverter output. The first channel of the oscilloscope shows the inverter output waveform, the second channel shows the filtered inverter output waveform, and the third one shows the phase current. In Fig. 9(a) and (b), the modulation index is high and the modulation algorithm takes advantage of all five levels of the inverter. Nevertheless, in Fig. 9(c) and (d), the modulation index is low and the output voltage is a three-level waveform. In Fig. 9(a) and (c), with purely sinusoidal output when the modulation index is high, the low-order harmonics are negligible and the total harmonic distortion (THD) is 3.8%. If the modulation index is low, then the low-order harmonics grow because of the three-level output and the THD increases up to 6.4%. In the

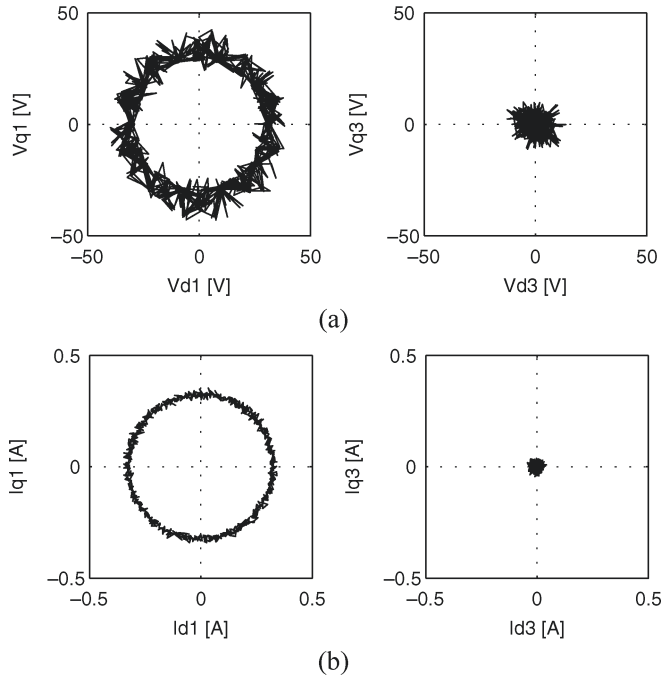


Fig. 10. Trajectories of the voltage and the current vectors in stationary dq axes with $m_1 = 1.8$ and $m_3 = 0$. (a) Inverter output voltage. (b) Output current.

cases of Fig. 9(b) and (d), the amplitude of the third harmonic is nearly the sixth part of the fundamental, and the high THD obtained corresponds to the injected third harmonic.

Fig. 10 shows the trajectories of the inverter output voltage and the load current vectors in stationary dq frames [28] with a balanced sinusoidal reference. Both vectors move, at constant speed, along a circular trajectory in the $dq1$ plane. No third harmonic was injected; hence, as expected, vectors in the $dq3$ plane stay close to the origin.

V. Conclusion

In this paper, a new multilevel multiphase SVPWM algorithm is presented. This algorithm is based on a displacement plus a two-level multiphase SVPWM modulator. It is valid for any number of phases or levels and it can be used with the standard multilevel topologies. The presented modulation technique handles all switching states of the inverter and it provides a sorted switching vector sequence that minimizes the number of switchings. In addition, the proposed SVPWM algorithm proves suitable for real-time implementation due to its low computational complexity. Finally, a five-level five-phase version was implemented in a low-cost FPGA and successfully tested by using a laboratory prototype.

References

[1] G. K. Singh, "Multi-phase induction machine drive research—A survey," *Electr. Power Syst. Res.*, vol. 61, no. 2, pp. 139–147, Mar. 28, 2002.

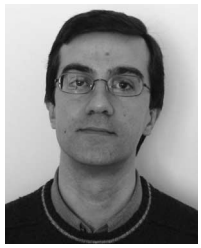
[2] J. Apsley, S. Williamson, A. Smith, and M. Barnes, "Induction motor performance as a function of phase number," *Proc. Inst. Electr. Eng.—Electric Power Applications*, vol. 153, no. 6, pp. 898–904, Nov. 2006.

[3] M. Simoes and J. Petronio Vieira, "A high-torque low-speed multiphase brushless machine—A perspective application for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1154–1164, Oct. 2002.

[4] L. Parsa and H. Toliyat, "Five-phase permanent magnet motor drives for ship propulsion applications," in *Proc. IEEE Elect. Ship Technol. Symp.*, Jul. 25–27, 2005, pp. 371–378.
[5] L. Parsa, H. A. Toliyat, and A. Goodarzi, "Five-phase interior permanent-magnet motors with low torque pulsation," *IEEE Trans. Ind. Appl.*, vol. 43, no. 1, pp. 40–46, Jan./Feb. 2007.
[6] E. Levi, M. Jones, S. N. Vukosavic, A. Iqbal, and H. A. Toliyat, "Modeling, control, and experimental investigation of a five-phase series-connected two-motor drive with single inverter supply," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1504–1516, Jun. 2007.
[7] K. Mohapatra, R. Kanchan, M. Baiju, P. Tekwani, and K. Gopakumar, "Independent field-oriented control of two split-phase induction motors from a single six-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1372–1382, Oct. 2005.
[8] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, S. U. Sulstijo, B. O. Woo, and P. Enjeti, "Multilevel converters—A survey," in *Proc. EPE*, 1999, pp. 408–418.
[9] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[10] P. Correa, M. Pacas, and J. Rodriguez, "Predictive torque control for inverter-fed induction machines," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1073–1079, Apr. 2007.
[11] J. Rodriguez, J. Dixon, J. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.
[12] J. Carrasco, L. Franquelo, J. Bialasiewicz, E. Galvan, R. Portillo Guisado, M. Prats, J. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.
[13] Y. Cheng, C. Qian, M. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.
[14] S. Lu and K. Corzine, "Multilevel multi-phase propulsion drives," in *Proc. IEEE Elect. Ship Technol. Symp.*, Jul. 25–27, 2005, pp. 363–370.
[15] S. R. Bowes and D. Holliday, "Optimal regular-sampled PWM inverter control techniques," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1547–1559, Jun. 2007.
[16] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar. 2001.
[17] M. M. Prats, L. G. Franquelo, J. I. Leon, R. Portillo, E. Galvan, and J. M. Carrasco, "A 3-D space vector modulation generalized algorithm for multilevel converters," *IEEE Power Electron. Lett.*, vol. 1, no. 4, pp. 110–114, Dec. 2003.
[18] L. Franquelo, M. Prats, R. Portillo, J. Galvan, M. Perales, J. Carrasco, E. Diez, and J. Jimenez, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using *abc* coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr. 2006.
[19] J. I. Leon, R. C. Portillo, L. G. Franquelo, S. Vazquez, J. M. Carrasco, and E. Dominguez, "New space vector modulation technique for single-phase multilevel converters," in *Proc. IEEE Int. Symp. Ind. Electron.*, Vigo, Spain, Jun. 4–7, 2007, pp. 617–622.
[20] Q. Song, X. Zhang, F. Yu, and C. Zhang, "Research on space vector PWM of five-phase three-level inverter," in *Proc. 8th ICEMS*, Sep. 27–29, 2005, vol. 2, pp. 1418–1421.
[21] H. Zhang, A. Von Jouanne, S. Dai, A. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.
[22] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector PWM method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.
[23] P. C. Loh and D. Holmes, "Flux modulation for multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1389–1399, Sep./Oct. 2002.
[24] A. Gupta and A. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct. 2006.
[25] A. Cataliotti, F. Genduso, A. Raciti, and G. R. Galluzzo, "Generalized PWMVSI control algorithm based on a universal duty-cycle expression: Theoretical analysis, simulation results, and experimental validations," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1569–1580, Jun. 2007.
[26] P. de Silva, J. Fletcher, and B. Williams, "Development of space vector modulation strategies for five phase voltage source inverters," in *Proc. 2nd Int. Conf. PEMD (Conf. Publ. No. 498)*, Mar. 31–Apr. 2 2004, vol. 2, pp. 650–655.
[27] S. Xue and X. Wen, "Simulation analysis of two novel multi-phase SVPWM strategies," in *Proc. IEEE ICIT*, Dec. 14–17, 2005, pp. 1337–1342.
[28] H.-M. Ryu, J.-H. Kim, and S.-K. Sul, "Analysis of multiphase space vector pulse-width modulation based on multiple $d-q$ spaces concept," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1364–1371, Nov. 2005.
[29] S. Xue, X. Wen, and Z. Feng, "Multiphase permanent magnet motor drive system based on a novel multiphase SVPWM," in *Proc. CES/IEEE 5th IPEMC*, Aug. 2006, vol. 1, pp. 1–5.
[30] G. Grandi, G. Serra, and A. Tani, "Space vector modulation of a seven-phase voltage source inverter," in *Proc. Int. SPEEDAM*, May 23–26, 2006, pp. 1149–1156.
[31] E. Levi, M. Jones, S. Vukosavic, and H. Toliyat, "Operating principles of a novel multiphase multimotor vector-controlled drive," *IEEE Trans. Energy Convers.*, vol. 19, no. 3, pp. 508–517, Sep. 2004.
[32] M. J. Duran and E. Levi, "Multi-dimensional approach to multi-phase space vector pulse width modulation," in *Proc. 33rd Annu. Conf. IEEE IECON*, Paris, France, Nov. 7–10, 2006, pp. 2103–2108.
[33] K. Corzine and S. Lu, "Comparison of hybrid propulsion drive schemes," in *Proc. IEEE Elect. Ship Technol. Symp.*, Jul. 25–27, 2005, pp. 355–362.
[34] A. Iqbal and E. Levi, "Space vector modulation schemes for a five-phase voltage source inverter," in *Proc. Eur. Conf. Power Elect. Appl.*, Sep. 11–14, 2005, p. 12.

Óscar López (M'05) was born in Spain, in 1975. He received the M.Sc. degree from the University of Vigo, Vigo, Spain, in 2001, where he is currently working toward the Ph.D. degree with the Department of Electronic Technology, since 2004.

He is currently an Assistant Professor with the University of Vigo. His research interest is in the areas of power switching converters technology.



Jacobo Álvarez was born in Vigo, Spain, in 1967. He received the Ph.D. degree in electronics from the University of Vigo, Vigo, in 1995.

In 1991, he was an Engineer at the University of Vigo and has been a Full Professor with the University of Vigo since 1997. His main topics of interest are programmable logic devices and field programmable gate arrays architectures and design methods, applied to industrial control problems.

Jesús Doval-Gandoy (M'99) received the M.Sc. degree from Polytechnic University of Madrid, Madrid, Spain, in 1991, and the Ph.D. degree from the University of Vigo, Vigo, Spain, in 1999.

From 1991 to 1994, he worked at industry. He is currently an Associate Professor with the University of Vigo. His research interest is in the area of ac power conversion.

Francisco D. Freijedo (M'07) was born in Spain, in 1978. He received the M.Sc. degree in physics from the University of Santiago de Compostela, Santiago de Compostela, Spain, in 2002. Since 2003, he has been working toward the Ph.D. degree with the Department of Electronic Technology, University of Vigo, Vigo, Spain.

Since 2005, he has been an Assistant Professor at the University of Vigo. His research interests include power quality problems, grid connected switching converters, ac power conversion, and FACTS.