Space-Vector PWM With Common-Mode Voltage Elimination for Multiphase Drives

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***Abstract*—Switching common-mode voltage (CMV) generated by the pulse width modulation (PWM) of the inverter causes common-mode currents, which lead to motor bearing failures and electromagnetic interference problems in multiphase drives. Such switching CMV can be reduced by taking advantage of the switching states of multilevel multiphase inverters that produce zero CMV. Specific space-vector PWM (SVPWM) techniques with CMV elimination, which only use zero CMV states, have been proposed for three-level five-phase drives, and for open-end winding five-, six-, and seven-phase drives, but such methods cannot be extended to a higher number of levels or phases. This paper presents a general (for any number of levels and phases) SVPMW with CMV elimination. The proposed technique can be applied to most multilevel topologies, has low computational complexity and is suitable for low-cost hardware implementations. The new algorithm is implemented in a low-cost field-programmable gate array and it is successfully tested in the laboratory using a five-level five-phase motor drive.**

***Index Terms*—Common-mode voltage elimination, field-programmable gate array (FPGA), multiphase drive, space-vector pulse width modulation (PWM), voltage source inverter (VSI).**

NOMENCLATURE

f_s	Switching frequency.
m	Modulation index.
P	Number of drive phases.
T	Switching period.
T_j	Dwell time of the switching vector $\mathbf{v}_{sj}$.
t_j	Normalized dwell time T_j.
V_{dc}	Voltage step of the multilevel inverter.
$\mathbf{V}_r$	$\in \mathbb{R}^P$. Reference voltage vector.
$\mathbf{v}_r$	$\in \mathbb{R}^P$. Normalized reference voltage vector.
$\check{\mathbf{v}}_r$	$= \mathbf{B}^{-1}\tilde{\mathbf{P}}\mathbf{v}_r \in \mathbb{R}^P$. Transformed reference vector.
$\mathbf{v}_{sj}$	$\in \mathbb{Z}^P$. jth switching vector in the switching sequence.
$\check{\mathbf{v}}_{sj}$	$= \mathbf{B}^{-1}\tilde{\mathbf{P}}\mathbf{v}_{sj} \in \mathbb{Z}^P$. Transformed switching vector.
$\boldsymbol{\omega}_r$	$= \mathbf{R}\mathbf{v}_r \in \mathbb{R}^{P-1}$. Reduced reference vector.
$\boldsymbol{\omega}_{sj}$	$= \mathbf{R}\mathbf{v}_{sj} \in \mathbb{Z}^{P-1}$. jth reduced switching vector.
$\dot{\mathbf{v}}$	$= \dot{\mathbf{P}}\mathbf{v}$. Homopolar component of vector $\mathbf{v}$, i.e., (CMV).
$\tilde{\mathbf{v}}$	$= \mathbf{v} - \dot{\mathbf{v}} = \tilde{\mathbf{P}}\mathbf{v}$. Nonhomopolar component of $\mathbf{v}$.
$\mathbf{v}^T$	Transpose of vector $\mathbf{v}$.

Vectors and matrices are named with bold letters, while scalars, with normal ones. Lowercase is used for normalized variables. Variables related to reduced vector space are written with Greek letters. Superscripts (k) denote the phase, whereas subscripts (j) indicate the position of vectors within sequences.

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I. INTRODUCTION

MULTIPHASE adjustable speed drives have gained increasing attention in last years due to their advantages when compared with three-phase ones [1], [2], namely reduced current rating of inverter switches, fault tolerance [3], [4], and reduced torque pulsations [5].

The CMV is a concern in multiphase drives [6]–[9] because, as in their three-phase counterparts, it is the origin of common-mode currents that lead to premature motor bearing failures, and undesirable electromagnetic interferences [10]–[14]. The main causes that contribute to such currents in drives with VSI and PWM are the capacitive currents, the circulating bearing currents and the rotor ground currents generated by the high dv/dt at the motor terminals, in addition to the electrostatic discharge machining (EDM) currents that arise when the threshold voltage of the bearings is exceeded [13], [14].

Traditional methods to alleviate the adverse effects of CMV rely on passive filters that prevent common-mode currents from flowing [15], [16]. The CMV can also be reduced without additional filtering elements, which increase the cost and decrease the power density, by means of enhanced control or PWM techniques. In two-level multiphase drives, the CMV was reduced by means of predictive control techniques [17], [18] or by means of enhanced space-vector PWM (SVPWM) techniques [6], [7], [19], [20].

Multilevel VSIs are well known to produce a CMV with low dv/dt, which inherently reduces capacitive, circulating bearing, and rotor ground currents [21], [22]. Additionally, they are also able to reduce the EDM currents by taking advantage of the redundant switching states, which produce the same line-to-line voltage but different CMV. Hence, these redundant states allow multilevel VSIs to effectively reduce the common-mode currents if only the states that keep the CMV constant are used [23]. Since such constant voltage is usually taken as the reference voltage, such states are referred to as zero CMV switching states, and the PWM techniques that make use only

and exclusively of such states are named SVPMW with CMV elimination [24], [25]. However, very few attempts have been made to develop PWM methods aiming at CMV elimination for multilevel multiphase drives [26], and most of the them are in the context of open-end winding topologies [24], [27]–[29]. In [26], the common-mode currents are reduced in a single-ended five-phase drive by using only the 53 zero CMV switching states that are available in a three-level neutral-point-clamped VSI. The SVPMW techniques with CMV elimination proposed in [24] and [27] allow to use a single dc source to feed a five-phase open-end winding motor thanks to a significant reduction of the common-mode currents. The works in [24], [26], and [27] in essence propose several three-level five-phase SVPWM algorithms based on the multiple d-q spaces concept [30]. In five-phase systems, there are two d-q planes, one more than in three-phase systems. This fact makes the modulation problem much more challenging because it requires selecting the switching vectors simultaneously in both planes, with the significant inconvenience that a switching vector close to the reference in the first plane can be far away from it in the second one [27], [31]. Consequently, the well-known three-phase SVPWM algorithms with CMV elimination cannot be extended to five-phase VSIs. Likewise, the algorithms in [24], [26], and [27] neither can be extended for VSIs with more than five phases. For six- and seven-phase open-end winding motor drives, two particular SVPWM techniques are proposed in [28] and [29], respectively. Since these two techniques are also based in the d-q spaces concept they can be neither extended for a different number of phases.

Having to look for switching vectors in several planes simultaneously, together with the fact that the number of switching states in each plane increases dramatically with the number of levels and phases [31], [32], make the SVPWM algorithms based on the d-q planes unfeasible even for VSIs with a moderate number of phases or levels. Such limitation has been overcome in [33]–[36] by avoiding the d-q planes and formulating the SVPWM problem in a multidimensional vector space. Even though the techniques in [33]–[36] can be applied to VSIs with any number of levels and phases, they are not able to eliminate the CMV and their adverse effects.

In summary, SVPWM with CMV elimination has not been dealt with for drives with more than seven phases and three levels. The contribution of this paper is to fill such gap with a generic (i.e., any number of levels and phases) SVPWM algorithm with CMV elimination. This objective is achieved by means of a multidimensional formulation of the problem. The new technique can be applied to a wide variety of multilevel topologies, it has a low computational cost that is independent of the number of levels and it is well suited for real-time hardware implementation.

The rest of this paper is organized as follows. Section II presents a rigorous demonstration of the proposed SVPWM algorithm, its required steps and an example. In Section III, the performance of the new modulation technique is assessed in terms of number of switchings, linear range of the modulation index, and CMV elimination. In Section IV, the algorithm is implemented in a field-programmable gate array (FPGA) and is tested by means of a five-level five-phase motor drive prototype. Finally, Section V concludes this study.

II. Algorithm Development

A. Algorithm Formulation

The SVPWM techniques are used in conjunction with VSIs to approximate a voltage reference vector $\mathbf{V}_r$ by means of a sequence of l switching vectors $\{\mathbf{V}_{s1},\ \mathbf{V}_{s2}, \ldots, \mathbf{V}_{sl}\}$, where each switching vector $\mathbf{V}_{sj}$ is applied during an interval T_j in the modulation period T. The reference vector $\mathbf{V}_r = [V_r^1, V_r^2, \ldots, V_r^P]^{\mathrm{T}}$ gathers the voltage references for each phase of the VSI, whereas each switching vector $\mathbf{V}_{sj} = [V_{sj}^1, V_{sj}^2, \ldots, V_{sj}^P]^{\mathrm{T}}$ includes the switching state of each VSI leg. Therefore, the reference and the switching vectors belong to the multidimensional space $\mathbb{R}^P$, where P is the number of phases of the VSI [36]. In the most common multilevel topologies, such as flying capacitor, diode-clamped, cascaded full-bridge or some hybrid VSIs, the output of each phase V_{sj}^k is an integer multiple of a fixed voltage step V_{dc} [37], [38]

$$V_{sj}^k = nV_{dc}, \qquad n \in \mathbb{Z}. \tag{1}$$

If the voltage step and the modulation period are used to normalize all vectors and dwell times, i.e.

$$\mathbf{v}_r = \frac{\mathbf{V}_r}{V_{dc}} = [{v_r}^1, {v_r}^2, \ldots, {v_r}^P]^{\mathrm{T}} \in \mathbb{R}^P \tag{2}$$

$$\mathbf{v}_{sj} = \frac{\mathbf{V}_{sj}}{V_{dc}} = [v_{sj}^1, v_{sj}^2, \ldots, v_{sj}^P]^{\mathrm{T}} \in \mathbb{z}^P \tag{3}$$

$$t_j = \frac{T_j}{T} \in \mathbb{R} \tag{4}$$

then, the normalized switching vectors $\mathbf{v}_{sj}$ become integer vectors and the dwell times become real numbers in the range $[0, 1]$. The relation among the reference vector, the switching vectors and their dwell times can be expressed as a function of the normalized variables as [36]

$$\mathbf{v}_r = \sum_{j=1}^{l} \mathbf{v}_{sj} t_j, \qquad \sum_{j=1}^{l} t_j = 1. \tag{5}$$

Consequently, for a given reference vector $\mathbf{v}_r$, the modulation law in (5) has to be solved in order to find a proper sequence of switching vectors $\{\mathbf{v}_{sj}\}$ with their corresponding dwell times $\{t_j\}$. Additionally, an SVPWM aiming to eliminate the CMV should only use the switching vectors that produce zero CMV. The CMV produced by the switching vector $\mathbf{v}_{sj}$ is

$$V_n = \frac{1}{P} \sum_{k=1}^{P} v_{sj}^k V_{dc} \tag{6}$$

and therefore, the switching vector should obey the following zero-CMV condition to be used:

$$\sum_{k=1}^{P} v_{sj}^k = 0. \tag{7}$$

Every switching vector can be decomposed into the addition of a homopolar component $\dot{\mathbf{v}}_{sj}$ plus a nonhomopolar component

$\tilde{\mathbf{v}}_{sj}$ as

$$\mathbf{v}_{sj} = \dot{\mathbf{v}}_{sj} + \tilde{\mathbf{v}}_{sj} \tag{8}$$

$$\dot{\mathbf{v}}_{sj} = \dot{\mathbf{P}}\mathbf{v}_{sj} \tag{9}$$

$$\tilde{\mathbf{v}}_{sj} = \tilde{\mathbf{P}}\mathbf{v}_{sj} \tag{10}$$

where $\dot{\mathbf{P}}$ and $\tilde{\mathbf{P}}$ are the following $P \times P$ real matrices:

$$\dot{\mathbf{P}} = \frac{1}{P}\begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix} \tag{11}$$

$$\tilde{\mathbf{P}} = \mathbf{I} - \dot{\mathbf{P}} \tag{12}$$

and $\mathbf{I}$ is the identity matrix. The zero-CMV condition in (7) can be expressed either as a function of the homopolar component or as a function of the nonhomopolar component as

$$\dot{\mathbf{v}}_{sj} = \mathbf{0} \qquad \tilde{\mathbf{v}}_{sj} = \mathbf{v}_{sj}. \tag{13}$$

The application of the decomposition defined in (8) to the modulation law in (5) results in

$$\dot{\mathbf{v}}_r + \tilde{\mathbf{v}}_r = \sum_{j=1}^{l} \dot{\mathbf{v}}_{sj} t_j + \sum_{j=1}^{l} \tilde{\mathbf{v}}_{sj} t_j \tag{14}$$

where

$$\dot{\mathbf{v}}_r = \dot{\mathbf{P}}\mathbf{v}_r \in \mathbb{R}^P \tag{15}$$

$$\tilde{\mathbf{v}}_r = \tilde{\mathbf{P}}\mathbf{v}_r \in \mathbb{R}^P. \tag{16}$$

Since $\dot{\mathbf{P}}$ and $\tilde{\mathbf{P}}$ are complementary projections (i.e., $\dot{\mathbf{P}}\dot{\mathbf{P}} = \dot{\mathbf{P}}$ and $\tilde{\mathbf{P}} + \dot{\mathbf{P}} = \mathbf{I}$) [39], it follows that the decomposition in (14) may be split into two independent parts

$$\dot{\mathbf{v}}_r = \sum_{j=1}^{l} \dot{\mathbf{v}}_{sj} t_j \tag{17}$$

$$\tilde{\mathbf{v}}_r = \sum_{j=1}^{l} \tilde{\mathbf{v}}_{sj} t_j. \tag{18}$$

Equation (17) and the zero-CMV condition $\dot{\mathbf{v}}_{sj} = \mathbf{0}$ can only be true at the same time if $\dot{\mathbf{v}}_r = \mathbf{0}$. Thus, an SVPWM technique with CMV elimination can only synthesize the nonhomopolar component of the reference vector $\tilde{\mathbf{v}}_r$. Considering (5), (13), and (18), the following comprehensive modulation law for an SVPWM algorithm with CMV elimination is inferred:

$$\tilde{\mathbf{v}}_r = \sum_{j=1}^{l} \mathbf{v}_{sj} t_j, \qquad \sum_{j=1}^{l} t_j = 1, \qquad \dot{\mathbf{v}}_{sj} = \mathbf{0}. \tag{19}$$

The zero-CMV condition impedes the straightforward application of the method in [36] to (19). Nevertheless, reformulation of (19) in a transformed vector space will allow the basic multilevel multiphase SVPWM algorithm in [36] (hereinafter, B-SVPWM) to be applied to the transformed modulation law in order to obtain a multilevel multiphase SVPWM technique with CMV elimination (hereinafter, CME-SVPWM).

The B-SVPWM is a general modulation technique valid for any number of levels and phases that provides, for a given reference vector, a sorted sequence of switching vectors with the corresponding dwell times. Its computational complexity is low since it basically requires sorting the fractional part of the components of the reference vector and a few arithmetical operations.

B. Modulation Law in a Transformed Vector Space

The switching vectors of a P-phase VSI are P-dimensional vectors that can be expressed as a linear combination of P basis elements

$$\mathbf{v}_{sj} = \sum_{k=1}^{P} \check{v}_{sj}^{\,k} \mathbf{b}_k \tag{20}$$

where $\check{v}_{sj}^{\,k}$ are the coordinates of the vector $\mathbf{v}_{sj}$ with respect to the basis formed by $\{\mathbf{b}_1, \mathbf{b}_2, \ldots, \mathbf{b}_P\}$. The aforementioned equation can be rewritten as

$$\mathbf{v}_{sj} = \mathbf{B}\check{\mathbf{v}}_{sj} \tag{21}$$

where $\mathbf{B} = [\mathbf{b}_1, \mathbf{b}_2, \ldots, \mathbf{b}_{P-1}, \mathbf{b}_P]$ is the $P \times P$ matrix whose columns are the vectors of the basis [39], and $\check{\mathbf{v}}_{sj} = [\check{v}_{sj}^{\,1}, \check{v}_{sj}^{\,2}, \ldots, \check{v}_{sj}^{\,P}]^{\mathrm{T}}$ is the transformed switching vector. An appropriate transformed space vector for solving (19) is the one defined by the following basis:

$$\begin{aligned} \mathbf{b}_1 &= [1, -1, \ 0, \ 0, \ldots, 0, \ 0]^T \\ \mathbf{b}_2 &= [0, \ 1, -1, \ 0, \ldots, 0, \ 0]^T \\ \mathbf{b}_3 &= [0, \ 0, \ 1, -1, \ldots, 0, \ 0]^T \\ &\vdots \qquad\qquad\qquad \vdots \\ \mathbf{b}_{P-1} &= [0, \ 0, \ 0, \ 0, \ldots, 1, -1]^T \\ \mathbf{b}_P &= [1, \ 1, \ 1, \ 1, \ldots, 1, \ 1]^T \end{aligned} \tag{22}$$

in which the basis elements $\{\mathbf{b}_1, \mathbf{b}_2, \ldots, \mathbf{b}_{P-1}\}$ are $P-1$ linearly independent vectors with zero homopolar component ($\dot{\mathbf{P}}\mathbf{b}_k = \mathbf{0}$), and $\mathbf{b}_P$ is a vector that only has homopolar component ($\dot{\mathbf{P}}\mathbf{b}_P = \mathbf{b}_P$).

To express the zero-CMV condition in the transformed vector space, it is necessary to write the homopolar component of the switching vectors as a linear combination of the basis elements. It can be done by taking into account (9), (20), and (22) as follows:

$$\dot{\mathbf{v}}_{sj} = \sum_{k=1}^{P} \check{v}_{sj}^{\,k} \dot{\mathbf{P}}\mathbf{b}_k = \check{v}_{sj}^{\,P} \mathbf{b}_P. \tag{23}$$

Therefore, in the transformed vector space, the zero-CMV condition in (13) can be expressed as $\check{v}_{sj}^{\,P} = 0$ and the comprehensive modulation law in (19) as

$$\check{\mathbf{v}}_r = \sum_{j=1}^{l} \check{\mathbf{v}}_{sj} t_j, \qquad \sum_{j=1}^{l} t_j = 1, \qquad \check{v}_{sj}^{\,P} = 0 \tag{24}$$

where

$$\check{\mathbf{v}}_r = \mathbf{B}^{-1}\tilde{\mathbf{v}}_r \tag{25}$$

$$\check{\mathbf{v}}_{sj} = \mathbf{B}^{-1}\tilde{\mathbf{v}}_{sj} = \mathbf{B}^{-1}\mathbf{v}_{sj} \tag{26}$$

and

$$\mathbf{B} = \begin{bmatrix} 1 & 0 & \dots & 0 & 1 \\ -1 & 1 & \dots & 0 & 1 \\ 0 & -1 & \dots & 0 & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 1 \\ 0 & 0 & \dots & -1 & 1 \end{bmatrix}. \tag{27}$$

Solving (24) requires to find an appropriate sequence of transformed switching vectors $\{\check{\mathbf{v}}_{sj}\}$ together with their corresponding dwell times $\{t_j\}$. The zero-CMV condition, ${\check{v}_{sj}}^{P} = 0$, provides one part of the solution because it sets to zero the value of the last component of every transformed switching vector

$$\check{\mathbf{v}}_{sj} = [\check{v}_{sj}^{1}, \check{v}_{sj}^{2}, \dots, {\check{v}_{sj}}^{P-1}, 0]^T. \tag{28}$$

The rest of the components of the transformed switching vectors can be obtained from a reduced version of the modulation law that excludes the already known Pth component. Such reduced modulation law can be written as

$$\boldsymbol{\omega}_r = \sum_{j=1}^{l} \boldsymbol{\omega}_{sj} t_j, \quad \sum_{j=1}^{l} t_j = 1 \tag{29}$$

where reduced vectors $\boldsymbol{\omega}_r \in \mathbb{R}^{P-1}$ and $\boldsymbol{\omega}_{sj} \in \mathbb{Z}^{P-1}$ are the transformed vectors $\check{\mathbf{v}}_r$ and $\check{\mathbf{v}}_{sj}$ without the last component

$$\boldsymbol{\omega}_r = [{\omega_r}^{1}, \dots, {\omega_r}^{P-1}]^T = [{\check{v}_r}^{1}, \dots, {\check{v}_r}^{P-1}]^T \tag{30}$$

$$\boldsymbol{\omega}_{sj} = [\omega_{sj}^{1}, \dots, {\omega_{sj}}^{P-1}]^T = [\check{v}_{sj}^{1}, \dots, {\check{v}_{sj}}^{P-1}]^T. \tag{31}$$

Bearing in mind (10), (16), (25), and (26), $\boldsymbol{\omega}_r$ and $\boldsymbol{\omega}_{sj}$ can be directly calculated from the reference and the switching vectors as

$$\boldsymbol{\omega}_r = \mathbf{R}\mathbf{v}_r \tag{32}$$

$$\boldsymbol{\omega}_{sj} = \mathbf{R}\mathbf{v}_{sj} \tag{33}$$

where $\mathbf{R}$ is the following $(P-1) \times P$ real matrix that is equal to $\mathbf{B}^{-1}\tilde{\mathbf{P}}$ without the last row

$$\mathbf{R} = \frac{1}{P}\begin{bmatrix} P-1 & -1 & -1 & \dots & -1 \\ P-2 & P-2 & -2 & \dots & -2 \\ P-3 & P-3 & P-3 & \dots & -3 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \dots & 1-P \end{bmatrix}. \tag{34}$$

The reduced modulation law in (29) is identical to the one solved in [36]; thus, the B-SVPWM algorithm can be applied to the reduced reference vector $\boldsymbol{\omega}_r$ in order to obtain a valid sequence of $l = P$ reduced switching vectors $\{\boldsymbol{\omega}_{s1}, \boldsymbol{\omega}_{s2}, \dots, \boldsymbol{\omega}_{sP}\}$ together with their corresponding dwell times $\{t_1, t_2, \dots, t_P\}$. Once the reduced switching vectors $\boldsymbol{\omega}_{sj}$ have been obtained, the transformed switching vectors $\check{\mathbf{v}}_{sj}$ can be easily drawn from (28) and (31) by adding an extra component equal to zero at the end of $\boldsymbol{\omega}_{sj}$

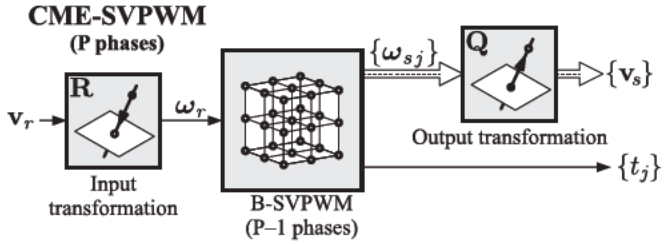

Fig. 1. Block diagram of the new multilevel multiphase SVPWM algorithm with CMV elimination.

$$\check{\mathbf{v}}_{sj} = [\omega_{sj}^{1}, \dots, {\omega_{sj}}^{P-1}, 0]^T. \tag{35}$$

Finally, the zero-CMV switching vectors $\mathbf{v}_{sj}$ can be calculated from $\check{\mathbf{v}}_{sj}$ by means of (21). Alternatively, they may also be obtained in a single step from the reduced switching vectors as

$$\mathbf{v}_{sj} = \mathbf{Q}\boldsymbol{\omega}_{sj} \tag{36}$$

where $\mathbf{Q}$ is the $P \times (P-1)$ integer matrix that is equal to $\mathbf{B}$ without the last column

$$\mathbf{Q} = \begin{bmatrix} 1 & 0 & \dots & 0 \\ -1 & 1 & \dots & 0 \\ 0 & -1 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & -1 \end{bmatrix}. \tag{37}$$

From the columns of this matrix, it follows that the switching vectors $\mathbf{v}_{sj}$ are a linear combination of the $P-1$ first vectors of the basis defined in (22), which are just those elements that have a zero homopolar component. Consequently, the homopolar component of any vector obtained with (36) is always zero, and thus, all the switching vectors of the sequence produce zero CMV. In addition, since the reduced switching vectors obtained with the B-SVPWM are integer vectors and the application of the transformation in (36) only requires a few subtractions, the obtained switching vectors are always integer vectors as well. Hence, they can be synthesized with converters that obey (1), provided that the reference vector is not in the overmodulation region.

C. Steps of the CME-SVPWM Algorithm and Example

Even though the previous demonstration is quite cumbersome, the inferred CME-SVPWM algorithm is, in fact, very simple. Its steps, depicted in Fig. 1, are the following:

1) obtain the normalized reference vector $\mathbf{v}_r$ from the reference voltage $\mathbf{V}_r$ by means of (2);
2) calculate the reduced reference vector $\boldsymbol{\omega}_r$ with (32);
3) apply the B-SVPWM algorithm in [36] to the vector $\boldsymbol{\omega}_r$ in order to get the sequence of reduced switching vectors $\{\boldsymbol{\omega}_{s1}, \boldsymbol{\omega}_{s2}, \dots, \boldsymbol{\omega}_{sP}\}$ with their corresponding dwell times $\{t_1, t_2, \dots, t_P\}$;

4) obtain the sequence of switching vectors with zero CMV $\{\mathbf{v}_{s1}, \mathbf{v}_{s2}, \ldots, \mathbf{v}_{sP}\}$ by means of (36).

Finally, it is also worth mentioning that the relation between switching vectors and the particular trigger signals for the transistors depends on the multilevel VSI topology.

The application of the proposed algorithm is illustrated by means of an example considering a five-phase drive ($P = 5$), where the voltage reference for each phase $k = 1, 2, \ldots, 5$ is purely sinusoidal: $V_r{}^k = mV_{dc}\sin\big(w\,t + 2\pi(k-1)/5\big)$. If a voltage amplitude with $m = 1.9$ and an angular frequency $w = 2\pi 50$ rad/s are considered, the instantaneous normalized reference for the five-phase drive when $t = 2.5$ ms is

$$\mathbf{v}_r = [1.344, 1.693, -0.297, -1.877, -0.863]^T \tag{38}$$

and its corresponding reduced reference vector is the following 4-D vector:

$$\boldsymbol{\omega}_r = \mathbf{R}\mathbf{v}_r = [1.343, 3.036, 2.739, 0.863]^T \tag{39}$$

with $\mathbf{R}$ being

$$\mathbf{R} = \frac{1}{5}\begin{bmatrix} 4 & -1 & -1 & -1 & -1 \\ 3 & 3 & -2 & -2 & -2 \\ 2 & 2 & 2 & -3 & -3 \\ 1 & 1 & 1 & 1 & -4 \end{bmatrix}. \tag{40}$$

The B-SVPWM algorithm applied to $\boldsymbol{\omega}_r$ yields the following sorted sequence of reduced vectors with their dwell times:

$$\begin{aligned} \boldsymbol{\omega}_{s1} &= [1, 3, 2, 0]^T & t_1 &= 0.137 \\ \boldsymbol{\omega}_{s2} &= [1, 3, 2, 1]^T & t_2 &= 0.123 \\ \boldsymbol{\omega}_{s3} &= [1, 3, 3, 1]^T & t_3 &= 0.396 \\ \boldsymbol{\omega}_{s4} &= [2, 3, 3, 1]^T & t_4 &= 0.307 \\ \boldsymbol{\omega}_{s5} &= [2, 4, 3, 1]^T & t_5 &= 0.036. \end{aligned} \tag{41}$$

Finally, the sequence of zero-CMV switching vectors and their dwell times are

$$\begin{aligned} \mathbf{v}_{s1} &= \mathbf{Q}\boldsymbol{\omega}_{s1} = [1, 2, -1, -2, \;\; 0]^T & t_1 &= 0.137 \\ \mathbf{v}_{s2} &= \mathbf{Q}\boldsymbol{\omega}_{s2} = [1, 2, -1, -1, -1]^T & t_2 &= 0.123 \\ \mathbf{v}_{s3} &= \mathbf{Q}\boldsymbol{\omega}_{s3} = [1, 2, \;\; 0, -2, -1]^T & t_3 &= 0.396 \\ \mathbf{v}_{s4} &= \mathbf{Q}\boldsymbol{\omega}_{s4} = [2, 1, \;\; 0, -2, -1]^T & t_4 &= 0.307 \\ \mathbf{v}_{s5} &= \mathbf{Q}\boldsymbol{\omega}_{s5} = [2, 2, -1, -2, -1]^T & t_5 &= 0.036 \end{aligned} \tag{42}$$

with $\mathbf{Q}$ being

$$\mathbf{Q} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix}. \tag{43}$$

Table I shows the simple MATLAB script used to solve the example. As expected, all the obtained switching vectors in (42) produce zero CMV [cp., (6)]. If the dead times are neglected, the switching vectors waveforms corresponding to this example, which are depicted in Fig. 2, show that a rising and a falling edge are forced in the waveforms in every vector transition. For instance, in the transition from $\mathbf{v}_{s2}$ to $\mathbf{v}_{s3}$, there are a rising and a falling edge in phases c and d, respectively. Such pair of simultaneous complementary edges is what ultimately achieves constant $V_n = 0$. Notice that all vector components are in the range $[-2, 2]$; thus, they can be generated by a five-level VSI.

TABLE I
MATLAB SCRIPT FOR THE SVPWM WITH CMV ELIMINATION

```
P=5% Number of phases
%% Ancillary matrices (calculated offline):
Do=triu(ones(P),0);% Needed in the B-SVPWM
Q=[1 0 0 0; -1 1 0 0; 0 -1 1 0; 0 0 -1 1; 0 0 0 -1]
R=[P-1 -1 -1 -1 -1; P-2 P-2 -2 -2 -2;
P-3 P-3 P-3 -3 -3; P-4 P-4 P-4 P-4 -4]/P
%% CME-SVPWM (to be implemented in the FPGA):
vr=[1.343, 1.693, -0.297, -1.877, -0.863]'% Reference vector
wr=R*vr% Reduced reference vector
[vfo,idx] = sort([1; wr-floor(wr)],'descend');
idx2=idx; idx2(idx)=1:P; D=Do(idx2,:);
ws=D(2:P,:)+floor(wr)*ones(1,P)% Reduced switching vectors
t=[1; vfo(2:P)]-[vfo(2:P); 0]% Dwell times
vs=Q*ws% Switching vector sequence
```

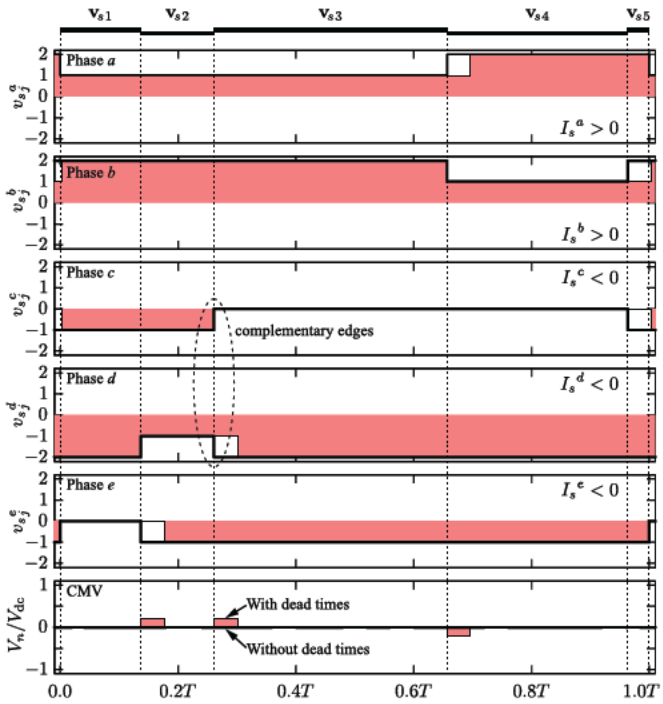

Fig. 2. Switching vector waveforms corresponding to reference vector $\mathbf{v}_r = [1.344, 1.693, -0.297, -1.877, -0.863]^T$ obtained with the CME-SVPWM technique. Thick trace: without dead times. Thin filled trace: with a dead time of $0.04T$.

III. MODULATION TECHNIQUE PERFORMANCE

A. Number of Switchings and Vector Sequence

The proposed P-phase CME-SVPWM algorithm includes an internal $(P-1)$-phase B-SVPWM algorithm in charge of calculating the reduced switching vector sequence; hence, the

performance of the former is directly related to the performance of the latter. The proposed modulation technique inherits from the B-SVPWM algorithm important properties such as the following ones: it is valid for any number of phases and levels; it can be applied to a wide variety of multilevel topologies; it has a low computational cost, which is independent of the number of levels; it does not use trigonometric functions or look-up tables; and it is well suited for real-time hardware implementation [36]. Additionally, as it will be seen shortly, both modulation techniques produce the same number of switchings.

The number of switchings produced by a modulation strategy can be computed by adding the number of switchings required to go through all vectors of the sequence plus the number of switchings required to return from the last to the first vector of the sequence. The P-phase B-SVPWM algorithm provides a sorted sequence of $P+1$ adjacent switching vectors. That is, any two consecutive vectors in the sequence are different in only one phase and the difference is just one unit. The last switching vector of the sequence is not adjacent to the first one, it is $\mathbf{v}_{sP+1} = \mathbf{v}_{s1} + [1, 1, \ldots, 1]^T$. Therefore, this technique produces P switchings in the transitions from $\mathbf{v}_{s1}$ to $\mathbf{v}_{sP+1}$ plus P additional switchings from $\mathbf{v}_{sP+1}$ back to $\mathbf{v}_{s1}$; and consequently, the total number of switchings is $2P$.

With the CME-SVPWM technique, the sequence of reduced vectors is a sorted sequence of P adjacent vectors [cp., (41)]. The fact that two consecutive reduced vectors differ only by one unit in just one phase, together with the fact that the components of the reduced vectors are the components of the switching vectors with respect to the basis $\{\mathbf{b}_1, \mathbf{b}_2, \ldots, \mathbf{b}_{P-1}\}$, implies that the difference between any two consecutive switching vectors is always equal to one of the basis elements. The elements of the basis in (22) have just two components different from zero: one equal to $+1$ and another one equal to -1. As a result, the difference between two consecutive switching vectors differs in just two phases: one that increases the output level by one unit and another one that decreases it by one unit. Since the new algorithm provides a sorted sequence with P switching vectors, it follows that the number of switchings required to go through all the vectors in the sequence is equal to $2(P-1)$. The last reduced vector in the sequence can be calculated from the first one as $\boldsymbol{\omega}_{sP} = \boldsymbol{\omega}_{s1} + [1, 1, \ldots, 1]^T$, and consequently, from (36) the last switching vector is $\mathbf{v}_{sP} = \mathbf{v}_{s1} + [1, 0, \ldots, -1]^T$. Therefore, the new algorithm forces just two more switchings in the transition from the last to the first switching vector of the sequence, and the total number of switchings per modulation period is $2P$. This fact can be verified in Fig. 2, where each phase switches twice in the whole period, which adds up to 10 for the five phases. Notice that the number of switchings required to return from the last to the first vector of the sorted sequence is equal to the number of switchings required to move forward between any two vectors in the sequence; thus, the new modulation technique does not require the typical symmetrical arrangement of the switching vectors in SVPWM techniques. Given that two is the minimum number of switchings that are able to keep the CMV constant, it can be stated that the new algorithm minimizes the number of switchings.

It is important to highlight that the PWM patterns obtained with the proposed modulation technique always switch two pairs of transistors in each leg, like with the B-SVPWM technique, and thus, the switch utilization and the losses are balanced among all VSI legs. Consequently, an optimization process to balance and reduce losses like the one presented in the three-phase carrier-based PWM in [40] is not needed. Besides, an optimization based on joint-phase switching state redundancy (i.e., zero-sequence injection) is not possible.

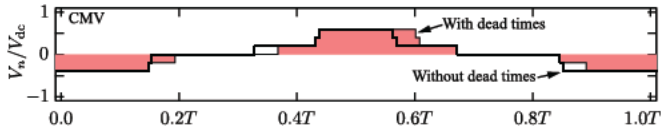

Fig. 3. CMV produced by the B-SVPWM technique for the reference vector $\mathbf{v}_r = [1.344, 1.693, -0.297, -1.877, -0.863]^T$. Thick trace: without dead times. Thin filled trace: with a dead time of $0.04T$.

B. Linear Range of the Modulation Index

The linear range of the modulation index m obtained with the CME-SVPWM algorithm is

$$0 \leq m \leq \begin{cases} (N-1)/2, & \text{if } N \text{ is odd} \\ N/2 - 1, & \text{if } N \text{ is even} \end{cases} \tag{44}$$

where N is the number of levels of the VSI, and m is defined as the ratio of the amplitude of output fundamental component to the dc-voltage step, i.e., $m = V_{\text{fund}}/V_{dc}$. The linear range of the modulation index obtained with the B-SVPWM algorithm is $0 \leq m \leq (N-1)/2$, provided harmonic injection is not considered [36]. Thus, with an odd numbers of levels both techniques make a similar utilization of the dc link, while for an even number of levels the CME-SVPWM algorithm makes a worse utilization. Notice that, according to (44), the proposed algorithm is only valid for VSIs with at least three levels.

C. CMV Elimination

Although all the switching vectors provided by the new algorithm produce a zero CMV, the example in Fig. 2 shows that, when dead times are considered, pulses of amplitude $V_{dc}/5$ arise in V_n in some of the vector transitions. This undesired effect is also reported in [24] and [26]. Even then, the CMV produced by the CME-SVPWM is much less than the one produced by the B-SVPWM, which is depicted in Fig. 3. Evaluation of modulation techniques in terms of the CMV reduction is not straightforward, so in [22], a metric to asses a modulation technique with regard to the risk of a given drive to suffer damage from inverter-induced bearing currents was proposed. The parameters of such metric, as defined in [22], are the following ones:

1) the number of different voltage levels that occur when a certain control scheme is applied, $n_o v_{\text{com}}\_ctrl$;
2) the step size that do occur when a certain control scheme is applied, Δv_{com};
3) the frequencies of occurrence at which the different levels occur, $f\_n_o v_{\text{com},i}$;
4) the frequencies of occurrence at which these different step sizes occur, $f\_\Delta v_{\text{com},i}$.

These parameters are compared in Table II for the CME-SVPWM and the B-SVPWM techniques.

TABLE II
COMPARISON OF CMV METRIC PARAMETERS

Parameter	CME-SVPWM	B-SVPWM
$n_o v_{\text{com}}\_ctrl$	3	$P+1$
Δv_{com}	V_{dc}/P	V_{dc}/P
$f\_n_o v_{\text{com},i}$	$\leq P$	2 or 1
$f\_\Delta v_{\text{com},i}$	$\leq 2P$	$2P$

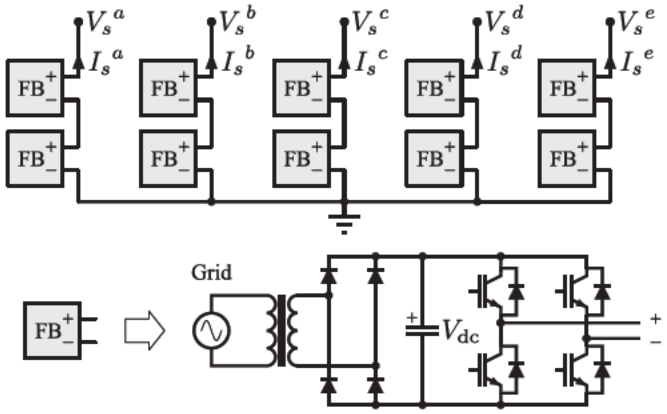

Fig. 4. Five-level five-phase cascaded full-bridge VSI considered in simulation and experiments.

The values for the CME-SVPWM have been obtained considering that during each vector transition, the CMV may take the value $-V_{dc}/P$, 0 or $+V_{dc}/P$, depending on the current directions in the particular phases that are switching. That is, the CMV has a waveform like the one shown in Fig. 2 when dead times are considered. Notice that in such example $n_o v_{\text{com}}\_ctrl = 3$, $\Delta v_{\text{com}} = V_{dc}/5$, $f\_n_o v_{\text{com},i} = 3$ and $f\_\Delta v_{\text{com},i} = 6$.

The values in Table II for the B-SVPWM technique have been obtained taking into account that in this case during a switching period, the CMV waveform is a stepped waveform like the one shown in Fig. 3, which has $P+1$ levels evenly spaced by V_{dc}/P. Particularly, in such waveform $n_o v_{\text{com}}\_ctrl = 6$, $\Delta v_{\text{com}} = V_{dc}/5$, $f\_\Delta v_{\text{com},i} = 10$, and the frequency of occurrence of each level is $f\_n_o v_{\text{com},i} = 2$ for all levels, except for the maximum and minimum CMV levels for which $f\_n_o v_{\text{com},i} = 1$ [22].

Thus, when compared with the B-SVPWM, the CME-SVPWM has a smaller number of CMV levels, the same step size, and equal or lower frequency of occurrence of step sizes. A fair comparison between both SVPWM techniques based on the frequency of occurrence of levels is difficult to perform because the new modulation algorithm has a lower number of different levels, but with a higher number of occurrences.

D. Simulation of B-SVPWM and CME-SVPWM

The performance of the proposed modulation technique is assessed and compared with that of the B-SVPWM by simulating the five-level five-phase VSI in Fig. 4 that has 3125 different switching states [32], but among them just 381 produce zero CMV. The parameters in Table III have been considered, and

TABLE III
SIMULATION AND EXPERIMENTAL SETUP PARAMETERS

Parameter	Simulation	Experiments
Transformer	–	Siemens 4AM4842
Rectifier diodes	–	GBPC2510
Capacitor	dc source	940 mF
V_{dc}	82.4 V	82.4 V
IGBTs	ideal switch	IRGB6B60KD
Switching frequency	9.8 kHz	9.8 kHz
Dead time	4 μs	4 μs
m (*)	1.9	1.9
Fundamental frequency	50 Hz	50 Hz
P	5	5
Load	$R = 10\ \Omega$ $L = 100$ mH	induction motor

(*) Except otherwise specified.

for the sake of simplicity, the transformer, the diode rectifier, and the capacitor were replaced by an ideal dc source. The load is made with five star-connected *RL* branches. Fig. 5(a) shows a quarter of the output voltage waveforms of phase a obtained with the B-SVPWM and the CME-SVPWM plotted in gray and black, respectively, which are very similar, and therefore, they basically present the same switch utilization. Their discrete Fourier transform (DFT), plotted in Fig. 5(b), show minor differences, as well, which are located mainly in the switching frequency sidebands. The output total harmonic distortion (THD) difference is also small, as shows Fig. 6(a), which depicts its variation with the modulation index taking into account the first five switching frequency sidebands. The output voltage waveforms corresponding to the other phases $V_s{}^b$–$V_s{}^e$ are similar to $V_s{}^a$, and thus, the number of switchings are balanced among all the converter legs.

The key difference between the B-SVPWM and the CME-SVPWM is in the CMV. The waveforms of V_n with both modulation techniques, traced in Fig. 5(c), and the DFT of those waveforms, plotted in Fig. 5(d), show a great reduction on the CMV. This fact can be also corroborated in the representation of the variation of the V_n root mean square (RMS) with the modulation index shown in Fig. 6(b). Simulations made with different values for f_s, dead time and number of phases P have rendered similar conclusions.

The value of parameters $f\_n_o v_{\text{com},i}$ and $f\_\Delta v_{\text{com},i}$ averaged over a fundamental period obtained with the CME-SVPWM, are 1.97 and 3.95, respectively, which are in accordance with the theoretical values given in Table II.

IV. EXPERIMENTAL EVALUATION

A Digilent S3 board is used to implement the CME-SVPWM algorithm for the five-level five-phase VSI in Fig. 4. This board hosts a XC3S200 FPGA by Xilinx running at 50 MHz, which has 4320 logic cells, each one constituted by two 16×1 look-up tables (LUTs) and two flip-flops. Since the core of the proposed algorithm is the B-SVPWM, the implementation of CME-SVPWM algorithm is based on the implementation of the former one described in [41]. Just the two blocks shown in Fig. 1 have been added, i.e., the input block $\mathbf{R}$ that reduces the reference vector in accordance with (32), and the output block $\mathbf{Q}$ that

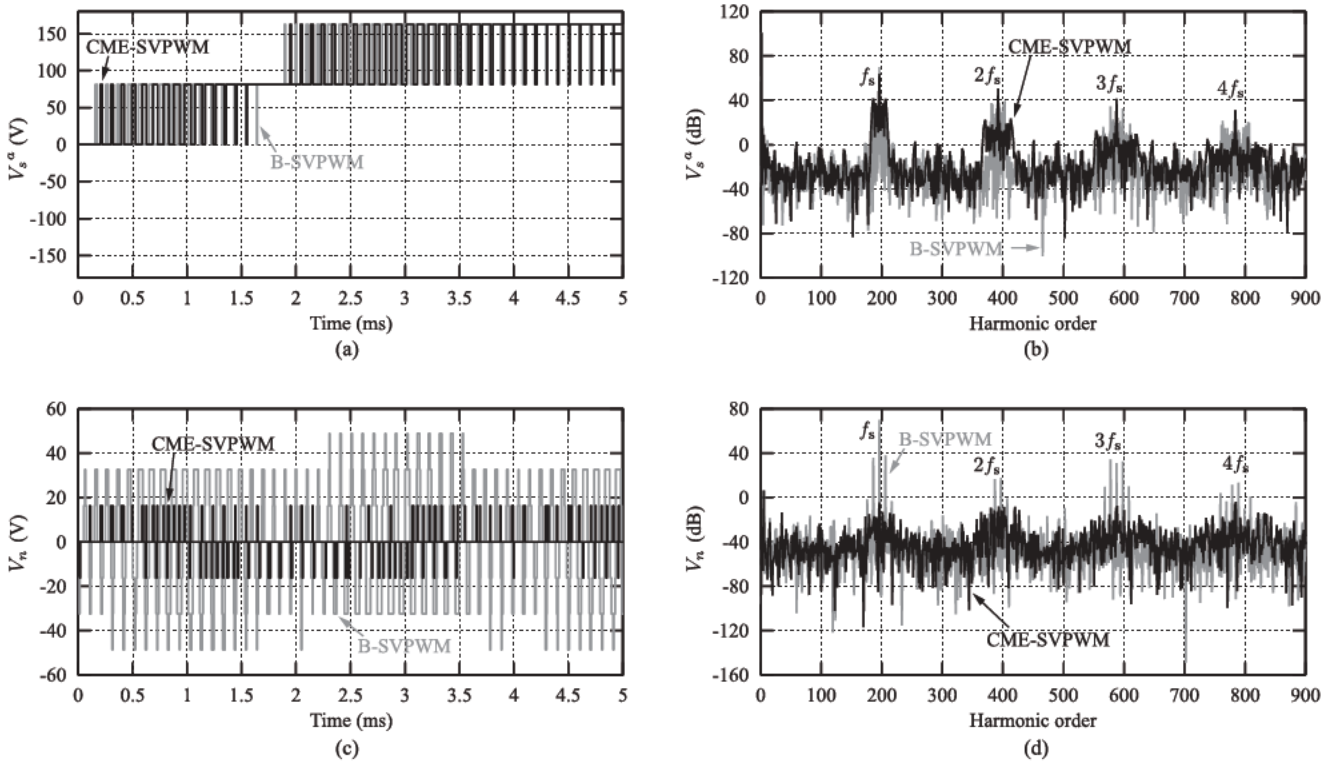

Fig. 5. Output voltage and CMV comparison between the B-SVPWM and the CME-SVPWM, with $f_s = 9.8$ kHz and a dead time of 4 μs. (a) Output voltage V_s^a (b) DFT of the output voltage V_s^a (c) CMV V_n (d) DFT of CMV V_n.

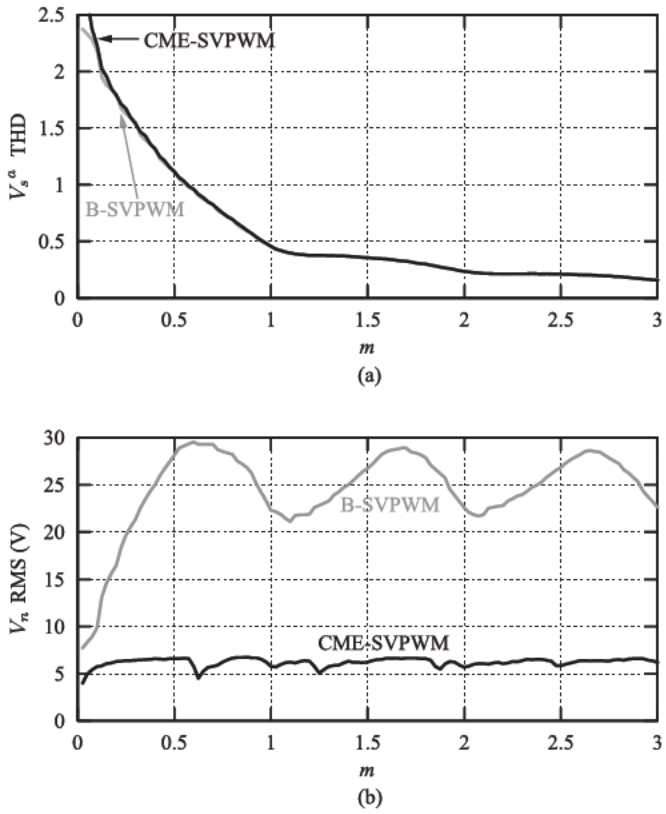

Fig. 6. Performance comparison between the B-SVPWM and the CME-SVPWM, with $f_s = 9.8$ kHz and a dead time of 4 μs. (a) Output THD variation with the modulation index (b) CMV variation with the modulation index.

TABLE IV
RESOURCES SUMMARY

Target Device: xc3s200				
Number of Slice Flip Flops:	899	out of	3,840	23%
Number of 4 input LUTs:	1,881	out of	3,840	48%
Number of occupied Slices:	1,061	out of	1,920	55%
Total Number 4 input LUTs:	1,904	out of	3,840	49%
Number of bonded IOBs:	86	out of	173	49%
IOB Flip Flops:	7			
Number of Block RAMs:	0	out of	12	0%
Number of MULT18X18s:	1	out of	12	8%
Number of BUFGMUXs:	3	out of	8	37%
Number of STARTUPs:	1	out of	1	100%

converts the reduced switching vectors into switching vectors according to (36). These two extra blocks slightly increase the complexity of CME-SVPWM with respect to the B-SVPWM. The implementation resource summary in Table IV shows that approximately half of the slices and LUTs and a quarter of the slice flip-flops in the FPGA are used. It is important to highlight that the available block random-access memories (RAMs) are not employed because the algorithm does not need data storage. Regarding the computation time, the CME-SVPWM takes 1231 clock cycles, i.e., 25 μs. Compared with the B-SVPWM, the CME-SVPWM uses around 20% more logic resources of the FPGA and requires 38% more computation time [41].

The proposed SVPWM algorithm is tested by using the experimental setup shown in Fig. 7, which includes the mentioned S3 board, a dSPACE DS1103 PPC Controller Board, and the VSI feeding a five-phase motor. The dSPACE board provides the reference vectors to the FPGA. The trigger signals generated

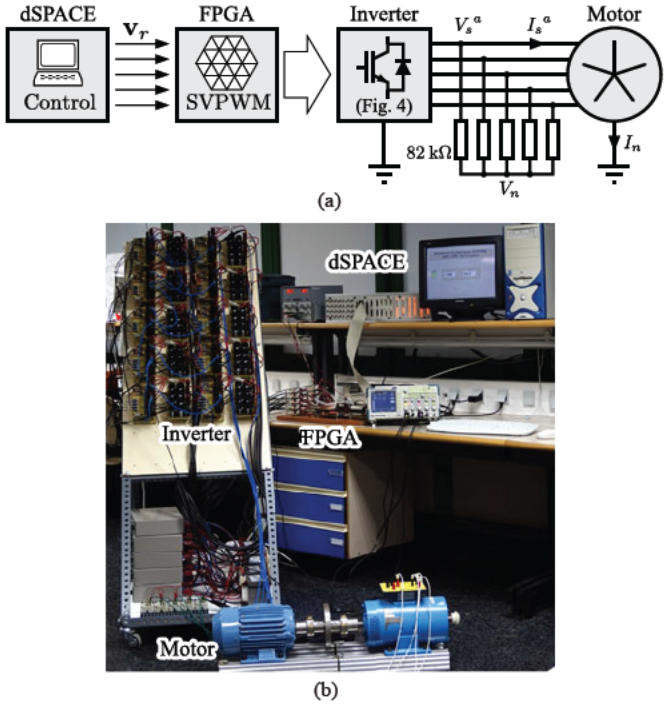

Fig. 7. Five-level five-phase experimental test setup.

by the FPGA control the transistors of the VSI. The parameters of the setup are detailed in Table III. The load is a five-phase squirrel cage motor of four poles built by rewinding the stator phases on the 30 stator slots of a 1.1-kW three-phase motor. In order to test a worst-case scenario, the motor neutral is grounded to allow the free flowing of the common-mode current I_n, as shown in Fig. 7(a). In addition, a virtual neutral made with five star-connected resistors is used to measure the CMV produced by the VSI V_n.

The performances of the CME-SVPWM and the B-SVPWM techniques are compared in Fig. 8. The leg output voltage $V_s{}^a$, the leg output current $I_s{}^a$, the CMV V_n, and the common-mode current I_n are measured without filtering at the points indicated in Fig. 7(a) by means of a TPS2014 Tektronix oscilloscope with the TPS2PWR1 Power Analysis Application. The voltage $V_s{}^a$ is a five-level stepped waveform in both cases. Even though both $V_s{}^a$ waveforms are quite similar, their fast Fourier transform show that the CME-SVPWM produces larger harmonics around the switching frequency sidebands, as it can be observed in Fig. 8. However, the leg output current $I_s{}^a$ obtained with the CME-SVPWM has much less high-frequency ripple, mainly because of the big differences in the CMV and common-mode current. With the B-SVPWM, the peak-to-peak CMV V_n is 104 V, much higher than the 40 V obtained with the CME-SVPWM technique. In addition, the CME-SVPWM produces smaller harmonics around the integer multiples of the switching frequencies. This is the main cause of the significant reduction in the high-frequency ripple in the common-mode current I_n.

Fig. 9 shows the measurement of the low-order harmonic content of the output voltage with the CME-SVPWM technique for $m = 1.90$ and $m = 0.80$. Equivalent measurements made with the B-SVPWM technique rendered very similar results (not shown). These low-order voltage harmonics appear because

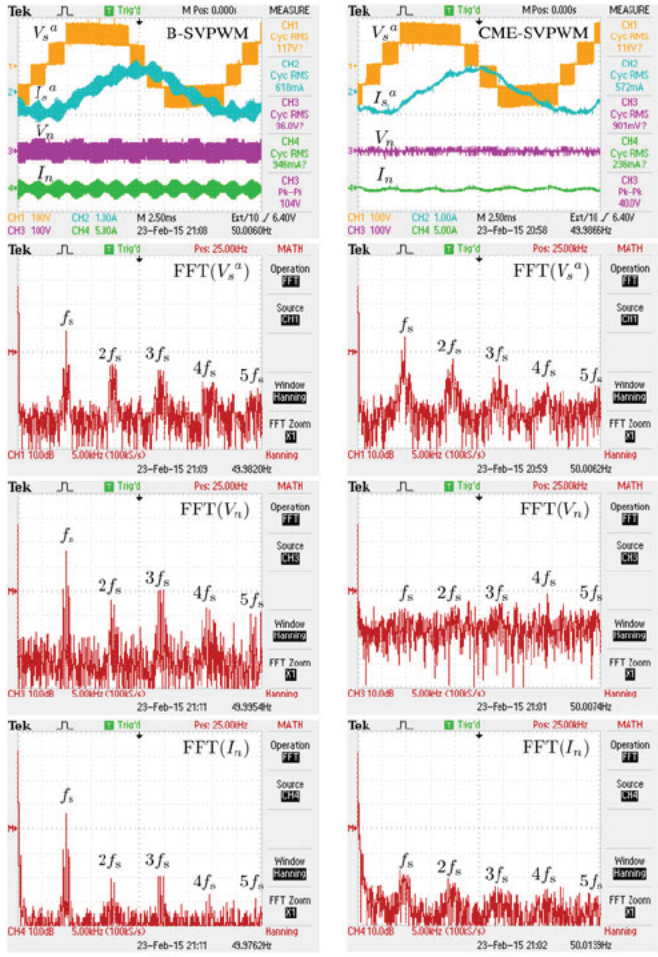

Fig. 8. Performance comparison of (a) B-SVPWM and (b) CME-SVPWM techniques. CH1: output leg voltage $V_s{}^a$; CH2: output leg current $I_s{}^a$; CH3: CMV V_n; CH4: common-mode current I_n.

Fig. 9. Low-order harmonics of the output voltage $V_s{}^a$ with CME-SVPWM. (a) $m = 1.90$ and (b) $m = 0.80$.

of the nonlinear behavior of the VSI, and not because of the PWM algorithm operation; hence, their amplitudes depend on parameters such as the dead time and the voltage drop across the VSI switches [24]. Even though the amplitude of the low-order harmonics in Fig. 9(a) is small, Fig. 8(b) shows that a relatively large low-frequency ripple arises in $I_s{}^a$ and I_n. This is due to the fact that some of the low-order voltage harmonics see a very low impedance as they map into the x–y plane (third, seventh, thirteenth, etc.) or into the homopolar axis (fifth, fifteenth, etc.). The rotor slot harmonics are also an origin of extra ripple in $I_s{}^a$

and I_n, which depends on the nonlinear behavior of the motor and not on the modulation process [24].

V. Conclusion

This paper has presented for the first time a generic multilevel SVPWM technique with CMV elimination for multiphase drives, which only uses switching states that produce zero CMV. The main contribution of the new modulation technique is its validity for VSIs with any number of phases and levels. In addition, it can be applied to a wide variety of multilevel topologies, it has a low computational cost, which is independent of the number of levels, and it does not use trigonometric functions or look-up tables. A five-level five-phase version has been implemented in a low-cost FPGA, and successfully tested with an induction motor drive. Experiments have shown that the common-mode currents are dramatically reduced, although not completely eliminated because of VSI's and motor's nonideal behavior.

References

[1] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[2] E. Levi, "Advances in converter control and innovative exploitation of additional degrees of freedom for multiphase machines," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 433–448, Jun. 2016.

[3] A. Tani, M. Mengoni, L. Zarri, G. Serra, and D. Casadei, "Control of multiphase induction motors with an odd number of phases under open-circuit phase faults," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 565–577, Feb. 2012.

[4] I. Gonzalez, M. J. Duran, H. S. Che, E. Levi, M. Bermudez, and F. Barrero, "Fault-tolerant operation of six-phase energy conversion systems with parallel machine-side converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3068–3079, Apr. 2015.

[5] J. M. Apsley, S. Williamson, A. C. Smith, and M. Barnes, "Induction motor performance as a function of phase number," *Proc. IEE*, vol. 153, no. 6, pp. 898–904, Nov. 2006.

[6] I. S. Freitas, H. A. Toliyat, C. B. Jacobina, and S. B. Ozturk, "A PWM strategy with reduced bearing currents for five-phase motors," in *Proc. IEEE Vehicle Power Propulsion Conf.*, Arlington, TX, Sep. 9–12, 2007, pp. 354–358.

[7] H. A. Hussain and H. A. Toliyat, "Reduction of shaft voltages and bearing currents in five-phase induction motors," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, Sep. 15–20, 2012, pp. 3309–3316.

[8] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 609–619, May 2013.

[9] S. M. Ahmed, H. Abu-Rub, and Z. Salam, "Common-mode voltage elimination in a three-to-five-phase dual matrix converter feeding a five-phase open-end drive using space-vector modulation technique," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6051–6063, Oct. 2015.

[10] A. Romanenko, J. Ahola, A. Muetze, and V. Niskanen, "Study of incipient bearing damage monitoring in variable-speed drive systems," in *Proc. Eur. Conf. Power Electron. Appl.*, Lappeenranta, Finland, Aug. 26–28, 2014.

[11] V. Niskanen, A. Muetze, and J. Ahola, "Study on bearing impedance properties at several hundred kilohertz for different electric machine operating parameters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3438–3447, Sep./Oct. 2014.

[12] A. Muetze, V. Niskanen, and J. Ahola, "On radio-frequency-based detection of high-frequency circulating bearing current flow," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2592–2601, Jul./Aug. 2014.

[13] A. Binder and A. Muetze, "Scaling effects of inverter-induced bearing currents in ac machines," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 769–776, May/Jun. 2008.

[14] A. Muetze and A. Binder, "Don't lose your bearings," *IEEE Ind. Appl. Mag.*, vol. 12, no. 4, pp. 22–31, Jul./Aug. 2006.

[15] P. Stec, J. Guzinski, P. Strankowski, A. Iqbal, A. A. Abduallah, and H. Abu-Rub, "Five-phase induction motor drive with sine-wave filter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Istanbul, Turkey, Jun. 1–4, 2014, pp. 2111–2116.

[16] A. A. Al-Abduallah, A. Iqbal, A. A. Al Hamadi, K. Alawi, and M. Saleh, "Five-phase induction motor drive system with inverter output LC filter," in *Proc. IEEE GCC Conf. Exhib.*, Doha, Qatar, Nov. 17–20, 2013, pp. 153–158.

[17] A. Iqbal, R. Alammari, M. Mosa, and H. Abu-Rub, "Finite set model predictive current control with reduced and constant common mode voltage for a five-phase voltage source inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Istanbul, Turkey, Jun. 1–4, 2014, pp. 479–484.

[18] M. J. Durán, J. Riveros, F. Barrero, H. Guzmán, and J. Prieto, "Reduction of common-mode voltage in five-phase induction motor drives using predictive control techniques," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2059–2067, Nov./Dec. 2012.

[19] M. J. Durán, J. Prieto, F. Barrero, J. Riveros, and H. Guzmán, "Space-vector PWM with reduced common-mode voltage for five-phase induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4159–4168, Oct. 2013.

[20] M. J. Durán, J. Prieto, and F. Barrero, "Space vector PWM with reduced common-mode voltage for five-phase induction motor drives operating in overmodulation zone," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4030–4040, Aug. 2013.

[21] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sep. 2007.

[22] S. Karugaba, A. Muetze, and O. Ojo, "On the common-mode voltage in multilevel multiphase single- and double-ended diode-clamped voltage-source inverter systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2079–2091, Nov./Dec. 2012.

[23] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[24] N. Bodo, M. Jones, and E. Levi, "A space vector PWM with common-mode voltage elimination for open-end winding five-phase drives with a single dc supply," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2197–2207, May 2014.

[25] S. Payami, R. K. Behera, and A. Iqbal, "Common mode voltage elimination for three-level five-phase neutral point clamped inverter," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Vienna, Austria, 10–13 Nov. 2013, pp. 5148–5154.

[26] S. Payami, R. Behera, A. Iqbal, and R. Al-Ammari, "Common mode voltage and vibration mitigation of a five-phase three-level NPC inverter fed induction motor drive system," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 349–361, Jun. 2015.

[27] P. P. Rajeevan, H. Abu-Rub, A. Iqbal, and K. Gopakumar, "Common mode voltage elimination scheme for dual-inverter fed five phase ac drives with open-end stator windings," in *Proc. IEEE Int. Conf. Ind. Technol.*, Cape Town, South Africa, Nov. 20–21, 2013, pp. 1680–1685.

[28] M. B. R. Correa, C. B. Jacobina, C. R. da Silva, A. M. N. Lima, and E. R. C. da Silva, "Six-phase ac drive system with reduced common-mode voltage," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, Madison, WI, USA, Jun. 1–4, 2003, vol. 3, pp. 1852–1858.

[29] N. Bodo, M. Jones, E. Levi, and A. Iqbal, "PWM techniques for an open-end winding seven-phase drive with a single dc source supply," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, Vienna, Austria, Nov. 10–14, 2013, pp. 5209–5214.

[30] H.-M. Ryu, J.-H. Kim, and S.-K. Sul, "Analysis of multiphase space vector pulse-width modulation based on multiple d-q spaces concept," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1364–1371, Nov. 2005.

[31] O. López., J. Alvarez, J. Malvar, A. G. Yepes, A. Vidal, P. Fernández-Comesaña, F. D. Freijedo, and J. D. Gandoy, "Multiphase space vector control modulation technique for voltage source converters," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Montréal, Canada, Oct. 25–28, 2012, pp. 3635–3640.

[32] O. López, E. Levi, F. D. Freijedo, and J. Doval-Gandoy, "Number of switching state vectors and space vectors in multilevel multiphase converters," *Electron. Lett.*, vol. 45, no. 10, pp. 524–525, May 2009.

[33] C. Keng-Yuan and H. Jwu-Sheng, "Multi-level multi-phase VSI control using multi-dimensional feedback quantization," in *Proc. Int. Conf. Intell. Green Building Smart Grid*, Taipei, Taiwan, Apr. 23–25, 2014.

[34] J.-S. Hu, K.-Y. Chen, T.-Y. Shen, and C.-H. Tang, "Analytical solutions of multilevel space-vector PWM for multiphase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1489–1502, May 2011.

[35] O. López, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm with switching state redundancy," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 792–804, Mar. 2009.
[36] O. López, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May 2008.
[37] K. A. Corzine, M. W. Wielebski, F. Z. Peng, and J. Wang, "Control of cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 732–738, May 2004.
[38] S. Lu and K. Corzine, "Multilevel multi-phase propulsion drives," in *Proc. IEEE Elect. Ship Technol. Symp.*, Philadelphia, PA, USA, Jul. 25–27, 2005, pp. 363–370.
[39] C. D. Meyer, *Matrix Analysis and Applied Linear Algebra*. Philadelphia, PA, USA: Soc. Ind. Appl. Math., 2000.
[40] N.-V. Nguyen, T.-K. T. Nguyen, and H.-H. Lee, "A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5425–5438, Oct. 2015.
[41] J. Álvarez, O. López, F. D. Freijedo, and J. Doval-Gandoy, "Digital parameterizable VHDL module for multilevel multiphase space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 3946–3957, Sep. 2011.

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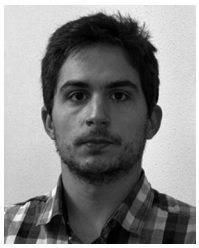

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