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Chip- and System-Level Reliability on SiC-based Power Modules

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Chip- and System-Level Reliability on SiC-based Power Modules

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ABSTRACT

The blocking voltage, switching frequency and temperature tolerance of power devices have been greatly improved due to the revolution of wide bandgap (WBG) materials, such as silicon carbide (SiC) and gallium nitride (GaN). Owing to the development of SiC-based power devices, the power rating, operating voltage, and power density of power modules have been significantly improved. However, the reliability of SiC-based power modules has not been fully explored yet. Thus, this dissertation focuses on the chip- and system-level reliability on SiC-based power modules.

For chip-level reliability, this work focuses on on-chip SiC ESD protection devices for SiC-based integrated circuits (ICs). In order to develop SiC ESD protection devices, SiC-based Ohmic contact and ion implantation have been studied. Nickel/Titanium/Aluminum (Ni/Ti/Al) metal stacks were deposited on SiC substrates to form Ohmic contact. Circular transfer length method (CTLM) structures were fabricated to characterize contact resistivity. Ion implantation was designed and simulated by Sentraurus technology computer aided design (TCAD) software. Secondary-ion mass spectrometry (SIMS) results show a good match with the simulation results. In addition, SiC ESD protection devices, such as N-type metal-oxide-semiconductor (NMOS), laterally diffused metal-oxide-semiconductor (LDMOS), high-voltage silicon controlled rectifier (HV-SCR) and low-voltage silicon controlled rectifier (LV-SCR), have been designed. Transmission line pulse (TLP) and very fast TLP (VF-TLP) measurements were carried out to characterize their ESD performance. The proposed SiC-based HV-SCR shows the highest failure current on TLP measurement and can be used as an area-efficient ESD protection device.

On the other hand, for system-level reliability, this dissertation focuses on the galvanic isolation of high-temperature SiC power modules. Low temperature co-fired ceramics (LTCC)

based high-temperature optocouplers were designed and fabricated as galvanic isolators. The LTCC-based high-temperature optocouplers show promising driving capability and steady response speed from 25 ºC to 250 ºC. In order to verify the performance of the high-temperature optocouplers at the system level, LTCC-based gate drivers that utilize the high-temperature optocouplers as galvanic isolators were designed and integrated into a high-temperature SiC-based power module. Finally, the high-temperature power module with integrated LTCC-based gate drivers was characterized by DPTs from 25 ºC to 200 ºC. The power module shows reliable switching performance at elevated temperatures.

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[1] P. Lai *et al*., "Investigation of ESD Protection in SiC BCD Process," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, pp. 405-409, doi: 10.1109/WiPDA46397.2019.8998959.

[2] P. Lai *et al*., "Area-Efficient Silicon Carbide SCR Device for On-Chip ESD Protection," in *IEEE Transactions on Electron Devices*, vol. 69, no. 6, pp. 3022-3028, June 2022, doi: 10.1109/TED.2022.3166471.

[3] P. Lai *et al.*, "Development of LTCC-packaged Optocouplers as Optical Galvanic Isolation for High-Temperature Applications," *Sci Rep,* vol. 12, 2022, doi: https://doi.org/10.1038/s41598-022-15631-7.

[4] P. Lai *et al*., "High-Temperature SiC Power Module with Integrated LTCC-Based Gate Driver," CS MANTECH, 2022.

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CHAPTER 1

INTRODUCTION

1.1 Background

1.1.1 Wide bandgap (WBG) semiconductor technology

The revolution of first-generation semiconductors, such as silicon (Si) and germanium (Ge), has greatly facilitated industrial technologies. Nowadays, Si-based semiconductor technology is well established and the most commonly used for electrical devices [1]. In the 1950s, the fabrication process of III-V compound gallium arsenide (GaAs), which is one of the presentative of second-generation semiconductors, was developed [2]. With the invention of this technology, second-generation semiconductors, such GaAs and Indium gallium arsenide (InGaAs), have been widely used in high-frequency, high-speed and light emitting electronic devices. Since the 1990s, third-generation semiconductor devices, so-called WBG devices presented by silicon carbide (SiC) and gallium nitride (GaN), have been commercially available [3]. This has boosted the development of power electronics.

Table 1.1 lists the selected material properties of the three generations of semiconductors. The wide bandgap of 4H-SiC (i.e., 3.26 eV) results in orders of magnitude lower intrinsic carrier concentration and leakage current compared to Si and GaAs. The thermal conductivity of 4H-SiC is higher than Si and GaAs. These properties make SiC-based devices promising for high-temperature (HT) applications. Besides, the wide bandgap of 4H-SiC also indicates a high critical field (i.e., 2.2 MV/cm). This allows SiC-based devices to show higher avalanche breakdown voltage than Si- and GaAs-based devices at the same order of doping concentration. Therefore, SiC-based power devices can be fabricated by relatively high-doped and short drift regions, which reduces their turn-on resistance and switching power loss. In general, with the advantage of wide

bandgap and high thermal conductivity, SiC-based devices are capable of operating at high-voltage, high-power, high-frequency and high-temperature conditions.

Table 1.1 Properties of semiconductor materials [1], [3]

	Si	GaAs	4H-SiC
Bandgap (eV)	1.12	1.4	3.26
Intrinsic concentration (cm^{-3})	1.4E10	2.1E6	8.2E-9
Critical field (MV/cm)	0.23	0.4	2.2
Permittivity	11.8	12.9	9.7
Thermal conductivity (W/cm·K)	1.5	0.5	3.8

1.1.2 SiC-based power module

The blocking voltage, switching frequency and temperature tolerance of power devices have been greatly improved due to the revolution of WBG materials. This significantly increases the power rating, operating voltage, and power density of power modules [4]. It has been demonstrated that SiC-based power modules show higher switching frequency and lower loss than silicon (Si) based counterparts [5]. Consequently, a variety of optimized SiC-based power modules have been proposed and developed, which mainly contribute to the increase of power density and the reduction of parasitic elements[6], [7]. One of the promising solutions to increase the power density and reduce the size and weight of the power electronic systems is to enhance the temperature tolerance of power modules and reduce or eliminate the bulky cooling system.

Several HT power modules were studied and developed in recent years. In 2010, J. Scofield et al. [8] investigated the reliability of the packaging materials, such as substrate (i.e., direct bonding copper (DBC)), and encapsulation materials, for HT power modules. Based on these results, J.

Scofield et al. [9] developed two HT power modules. Cree's SiC power MOSFETs were integrated into the power module, and the power modules were characterized up to 200 ºC. Meanwhile, Meanwhile, Z. Chen proposed a 1200-V HT power module [10]. Both SiC power MOSFETs and the power module were characterized and fully analyzed at a temperature of 200 ºC.

On the other hand, the integration of gate driver circuits into power modules reduces the parasitic inductance. This not only lowers the size but also increases the switching frequency of power modules. It should be noted that since the gate driver circuits are tightly integrated with the power devices, their operating temperature is required to be similar to that of the power devices. As a result, researchers proposed HT gate driver circuits for the integration of power modules. In 2010, silicon on insulator (SOI) gate driver integrated circuits (ICs) were integrated into a power module [11]. The power module shows reliable switching behaviors and relatively low power loss. H. A. Mantooth et al, [12] also proposed a solution for the integration of SiC-based gate drivers into power modules.

1.2 Motivation

Although HT and high-density SiC-based power modules have been proposed, their reliability issues have not been fully explored. Therefore, the motivation of this study is the chip- and system-level reliability on SiC-based power modules. Fig. 1.1 shows the schematic of a SiC-based power module system. A control signal controls the turn-on and turn-off of the power module, and a gate driver is needed to drive the gate of the power device. For these components (i.e., control ICs and gate driver ICs), on-chip ESD protection devices are required. Besides, system-level protection, such as galvanic isolation, is needed to protect the low-voltage control ICs from high-voltage power devices. Reviews of on-chip ESD protection and galvanic isolation for SiC-based power modules will be provided in this section to understand the desire and necessity.

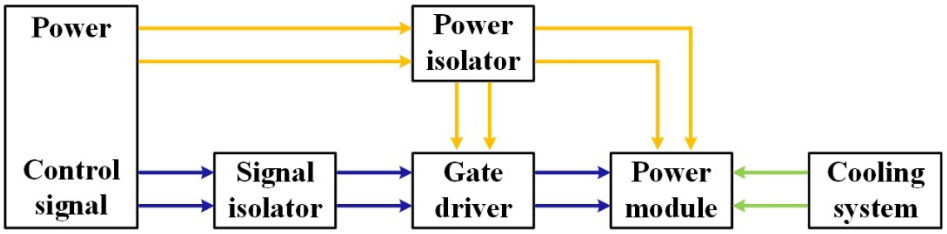


Fig. 1.1 Schematic of SiC-based power module system

1.2.1 On-chip ESD protection for SiC-based integrated circuits

In order to further reduce the power loss and parasitic elements of SiC-based power modules, logic controllers and gate driver circuits are expected to be integrated closely with the power devices, making their operating temperature similar to the power devices. However, the maximum operating temperatures for traditional Si-based ICs are typically below 150 ºC [13]. Therefore, a variety of SiC-based ICs have been demonstrated, such as high-current, high-temperature bipolar SiC ICs [14], SiC digital logic gates functioning at 600 ºC [15], SiC CMOS digital circuits operating at temperatures exceeding 300 ºC [16], high-temperature (i.e., ~400 ºC) analog ICs in SiC bipolar technology [17] and 4H-SiC ultraviolet (UV) photodiodes [18]. Although these SiC ICs show high performance with a wide range of operating temperatures, the reliability has not been sufficiently explored yet. Among the reliability issues, ESD is a great matter of concern that creates overstresses to devices and circuits with a large electric field and high current density, resulting in the dielectric breakdown of the gate oxide or thermal runaway of semiconductor devices [19]. ESD protection devices and circuits have been well studied in traditional Si semiconductor industry [20] to provide effective on-chip and off-chip protections for Si ICs. However, limited studies have been published in the field of SiC-based ESD protection.

Several SiC-based ESD protection devices and circuits have been studied in recent years. A 4H-SiC ESD protection circuit (i.e., gate-body floating NMOS (GBFNMOS)) was proposed and investigated [21]. The transmission line pulse (TLP) measurement results showed that the

proposed GBFNMOS has low on-resistance, low trigger voltage and good high-temperature performance. Kyoung-II Do et al. also proposed SiC-based high-holding floating gate NMOS (HHFGNMOS), low-voltage silicon-controlled rectifier (SCR) and lateral insulated-gate bipolar transistor based SCR (LIGBT-SCR) for ESD protection [22]-[24]. In addition, The behavior of SiC junction barrier Schottky diodes under ESD human body model (HBM) stress was investigated by P. Denis et.al., aiming to address the limitation of SiC devices and processes [25]. T. Phulpin et.al. [26] also studied the operation and failure mechanisms of three types of metal epitaxial-semiconductor FETs (MESFETs) under ESD stress by using TLP and HBM tests. The operation of SiC MOSFETs under ESD stress was investigated and analyzed by photon emission (PE) and spectral photon emission technique (SPE) [27], [28]. Furthermore, D.T. Jarard et al. reported 15V SiC NMOS ESD characteristics in Raytheon high-temperature silicon carbide (HiTSiC) process to explore the ESD robustness and facilitate the ESD protections for SiC ICs [29]. The electrical safe operating areas (SOAs) of low voltage SiC NMOS devices with varying channel width, gate length and gate bias are characterized by the TLP system. Although progress has been made in SiC-based ESD studies in recent years, systematical studies of SiC-based ESD protection for SiC CMOS devices are still desired. For example, the approaches of designing the trigger voltage (V_{t1}), controlling the trigger current (I_{t1}) and increasing the failure current (I_{t2}) of SiC ESD protection devices have not been fully understood. Also, the TLP and VF-TLP measurements on SiC ESD protection devices have not been sufficiently investigated.

1.2.2 Galvanic isolation for SiC-based power module

In gate driver circuitry, galvanic isolation devices and circuits are required to isolate the low-voltage logic controllers from the high-voltage components [29], [30]. Optocouplers, capacitors and transformers are commonly used as galvanic isolators [29]-[32]. Optocouplers provide a small

packaging size, few connection components, low input drive currents, and low power dissipation, making them more desirable than regular isolation transformers [30]. However, the performance degradation of optocouplers at elevated temperatures limits their applications in high-temperature environments [32]. Therefore, the design and fabrication of high-temperature optocouplers for galvanic isolation in gate driver circuitry are highly desired.

In previous work, researchers at the University of Arkansas, Fayetteville have studied emitters and detectors for HT optocouplers. The spontaneous emission quantum efficiency (QE) of different light-emitting diode (LED) materials (i.e., indium-gallium-nitride-based (InGaN-based) multiple quantum wells (MQWs)) over a wide range of temperature was studied using photoluminescence (PL) measurements [33]. The InGaN-based MQW structures exhibit minimum QE drop at temperatures higher than 200˚C. The study was extended to other LED materials as well to investigate the QE at high temperatures. A. Sabbar et al. [34] reported InGaN-based and aluminum-gallium-indium-phosphide-based (AlGaInP-based) MQW structures with different peak wavelength (i.e., 450 nm, 470 nm and 630 nm) for high-temperature optoelectronic applications. Moreover, further optimization into InGaN-based structures was proposed to enhance their behaviors at high temperatures, and relatively high QE at high temperatures (i.e., >200˚C) is observed [35]. The temperature and injected current-dependent internal quantum efficiency (IQE) of InGaN-based MQW LEDs with different peak wavelengths (i.e., 450 nm, 470 nm and 530 nm) were studied using electroluminescence (EL) measurements [36]. Stable peak IQE of these LEDs at high temperatures was reported. These studies [33]-[36] prove that AlGaN-based and AlGaInP-based MQW structures can be utilized to form LED devices in high-temperature optoelectronic applications. In addition, the spectral responsivity (SR) of InGaN-based MQW structures was investigated with the temperature range of -200˚C to 500˚C [37]. The results indicate that the

photodiodes can be used in high-temperature optocouplers. Although systematic studies of the optoelectronic devices for high-temperature applications were carried out, the LEDs and photodiodes were investigated individually. The high-temperature optical coupling behavior of the LEDs and photodiodes is not yet investigated. Therefore, high-temperature optocouplers, which integrate LEDs as emitters and photodiodes as detectors, need further studies.

1.3 Objectives

This dissertation focuses on the on-chip ESD protection and galvanic isolation of SiC-based power module systems, which aims to improve the chip- and system-level reliability of the system. For chip-level reliability, SiC-based ESD protection devices for SiC low-voltage (i.e., <20 V) CMOS devices are investigated. The following works have been accomplished:

a) SiC-based Ohmic contacts have been developed. Circular transfer length method (CTLM) structures were fabricated on SiC substrates to characterize the Ohmic contacts.

b) SiC-based ion implantation profiles have been designed for SiC complementary metal-oxide-semiconductor (CMOS) and ESD protection devices. Technology computer aided design (TCAD) simulation results are provided.

c) SiC-based ESD protection devices have been characterized by transmission-line pulse (TLP) and very fast TLP (VF-TLP) systems. Area-efficient SiC-based silicon controlled rectifier (SCR) structures are proposed.

On the other hand, for system-level reliability, optical-based HT galvanic isolators are developed. The following works have been accomplished:

a) Low temperature co-fired ceramics (LTCC) based HT optocouplers have been designed and fabricated. Their optical coupling efficiency and response speed are characterized and analyzed from 25 ºC to 250 ºC.

b) LTCC-based gate drivers, which utilize the HT optocouplers as galvanic isolators, have been developed.

c) The proposed LTCC-based gate drivers have been integrated into an HT SiC-based power module. Double pulse tests (DPTs) are carried out from 25 ºC to 200 ºC to characterize the SiC-based power module.

1.4 Overview of Dissertation

This dissertation is organized as follows:

Chapter 2 to 5 focus on SiC-based on-chip ESD protection. The design and development of SiC Ohmic contacts and ion implantation profiles for SiC ESD protection devices are discussed in Chapter 2 and 3. Chapter 4, 5 and 6 provide the design, characterization and analysis of SiC-based ESD protection devices. Then HT optical galvanic isolators are discussed in Chapter 7 to 9. Chapter 7 presents the development of the LTCC-based HT optocouplers. The development and characterization of the LTCC-based gate drivers and HT SiC-based power module are presented in Chapter 8 and 9 to verify the performance of the HT optocouplers at the system level. Finally, Chapter 10 gives the conclusion of this dissertation and proposes possible future work for continued research.

1.5 Reference

[1] J. Wu, "The Development and Application of Semiconductor Materials," 2020 7th International Forum on Electrical Engineering and Automation (IFEEA), 2020, pp. 153-156, doi: 10.1109/IFEEA51475.2020.00039.

[2] E. Schubert, Light-Emitting Diodes, Cambridge, U.K.: Cambridge Univ. Press, 2006.

[3] N. Kaminski, "State of the art and the future of wide band-gap devices," *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1-9.

[4] B. Whitaker et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2606-2617, May 2014, doi: 10.1109/TPEL.2013.2279950.

[5] D. Comite and N. Pierdicca, "Decorrelation of the near-specular land scatterinZ. Chen, D. Boroyevich and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," The 2010 International Power Electronics Conference - ECCE ASIA -, 2010, pp. 164-169, doi: 10.1109/IPEC.2010.5543851.

[6] H. Lee, V. Smet and R. Tummala, "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 239-255, March 2020, doi: 10.1109/JESTPE.2019.2951801.

[7] C. Chen, F. Luo and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 3, pp. 170-186, Sept. 2017, doi: 10.24295/CPSSTPEA.2017.00017.

[8] J. D. Scofield, J. N. Merrett, J. Richmond, A. Agarwal and S. Leslie, "Performance and reliability characteristics of 1200 V 100 A 200 °C half-bridge SiC MOSFET-JBS diode power modules", IMAPS Int. Conf. High-Temperature Electronics, 2010-May, doi: https://doi.org/10.4071/HITEC-JScofield-WP22.

[9] J. Scofield, N. Merrett, J. Richmond, A. Agarwal, S. Leslie and C. Scozzie, "Electrical and thermal performance of 1200 V 100 A 200 °C 4H-SiC MOSFET-based power switch modules", Mater. Sci. Forum, vol. 645–648, pp. 1119-1122, 2010, doi: https://doi.org/10.4028/www.scientific.net/MSF.645-648.1119.

[10] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2307-2320, May 2014, doi: 10.1109/TPEL.2013.2283245.

[11] B. Vogler, M. Rossberg, R. Herzer and L. Reusser, "Integration of 1200V SOI gate driver ICs into a medium power IGBT module package," 2010 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2010, pp. 97-100.

[12] H. A. Mantooth, M. D. Glover and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 374-385, Sept. 2014, doi: 10.1109/JESTPE.2014.2313511.

[13] S. Kaplan, T. Griffin, and S. Bayne, “Silicon vs silicon carbide device characterization,” in Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003. 14th IEEE International, vol. 2, 2003, pp. 1217-1220 Vol. 2.

[14] H. Elahipanah, S. Kargarrazi, A. Salemi, M. Östling, C.-M. Zetterling, “500 °C high current 4H-SiC lateral BJTs for high-temperature integrated circuits”, *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1429-1432, Oct. 2017, doi: 10.1109/LED.2017.2737558.

[15] P. G. Neudeck, G. M. Beheim, C. S. Salupo, “600ºC logic gates using silicon carbide JFETs”, *Proc. Government Microcircuit Applications Conf.*, pp. 421-424, 2000.

[16] N. Kuhns, L . Caley, A. Rahman, A. Ahmed, J. Di, H. A. Mantooth, A. M. Francis, and J. Holmes, “Complex High-Temperature CMOS Silicon Carbide Digital Circuit Designs”, *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 105-111, June 2016, doi: 10.1109/TDMR.2016.2530664.

[17] S. Roy, A. U. Rashid, A. Abbasi, R. C. Murphree, M. M.. Hossain, A. Faruque, A. Metreveli, C,-M. Zetterling, J. Fraley, B. Sparkman, and H. A. Mantooth, “Silicon Carbide Bipolar Analog Circuits for Extreme Temperature Signal Conditioning”, *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3764-3770, Sept. 2019, doi: 10.1109/TED.2019.2928484.

[18] L. D. Benedetto, G. D. Licciardo, A. Rubino, “Experimental results on lateral 4H-SiC UV photodiodes”, *Proc. 7th IEEE Int. Workshop Adv. Sensors Interfaces (IWASI)*, pp. 252-254, Jun. 2017, doi: 10.1109/IWASI.2017.7974264.

[19] R. G. Wagner, J. M. Soden, C. F. Hawkins, "Extent and cost of EOS/ESD damage in an IC manufacturing process", *Proc. EOS/ESD Symp.*, vol. EOS-15, pp. 49-55, Sept. 1993.

[20] A. Amerasekera, C. Duvvury, ESD in Silicon Integrated Circuits, New York:Wiley, 1995.

[21] K.-I. Do, B.-S. Lee, Y.-S. Koo, “Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications”, *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 283-286, Feb. 2019, doi: 10.1109/LED.2018.2885846

[22] K. -I. Do, B. Lee, S. G. Kim and Y. -S. Koo, "Design of 4H-SiC-Based Silicon-Controlled Rectifier With High Holding Voltage Using Segment Topology for High-Voltage ESD Protection," in *IEEE Electron Device Letters*, vol. 41, no. 11, pp. 1669-1672, Nov. 2020, doi: 10.1109/LED.2020.3022888.

[23] K. -I. Do, J. -I. Won and Y. -S. Koo, "A 4H-SiC MOSFET-Based ESD Protection With Improved Snapback Characteristics for High-Voltage Applications," in *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 4921-4926, May 2021, doi: 10.1109/TPEL.2020.3032917.

[24] K. -I. Do, S. -H. Jin, B. -S. Lee and Y. -S. Koo, "4H-SiC-Based ESD Protection Design With Optimization of Segmented LIGBT for High-Voltage Applications," in *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 1017-1023, 2021, doi: 10.1109/JEDS.2021.3121212.

[25] P. Denis et al., “Robustness of 4H-SiC 1200V Schottky diodes under high electrostatic discharge like human body model stresses: An in-depth failure analysis”, *Diamond Related Mater.*, vol. 44, pp. 62-70, Apr. 2014.

[26] T. Phulpin et al., “Contribution to Silicon-Carbide-MESFET ESD Robustness Analysis”, *IEEE Transactions on Device and Materials Reliability*, Vol. 18 , pp. 214-223, June 2018).

[27] Niemat Moultif, Eric Joubert, Olivier Latry, “SiC MOSFET robustness to ESD study: Correlation between electrical and spectral photo-emission characterizations”, 2018 19th *IEEE Mediterranean Electrotechnical Conference (MELECON),* 2-7 May 2018.

[28] N. Moultif, E. Joubert, M. Masmoudi, O. Latry, "Characterization of ESD Stress Effects on SiC MOSFETs Using Photon Emission Spectral Signatures", *2017 Reliability and Maintainability Symposium (RAMS),* pp. 1-7, 23-26 January), 2017.
[29] Eric R. Motto, "Hybrid Circuits Simplify IGBT Module Gate Drive", 1999.
[30] J. N. Khan, "Design considerations in using the inverter gate driver optocouplers for variable speed motor drives" in White Paper, Avago Technologies, Mar 2010.
[31] V. Nguyen, L. Kerachev, P. Lefranc and J. Crebier, "Characterization and Analysis of an Innovative Gate Driver and Power Supplies Architecture for HF Power Devices With High dv/dt," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6079-6090, Aug. 2017, doi: 10.1109/TPEL.2016.2619859.
[32] Z. Zhang et al., "SiC MOSFETs Gate Driver With Minimum Propagation Delay Time and Auxiliary Power Supply With Wide Input Voltage Range for High-Temperature Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 417-428, March 2020, doi: 10.1109/JESTPE.2019.2951358.
[33] A Sabbar and S. Madhusoodhanan et al., "Systematic Investigation of Spontaneous Emission Quantum Efficiency Drop up to 800 K for Future Power Electronics Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 845-853, March 2020, doi: 10.1109/JESTPE.2018.2882775.
[34] A Sabbar and S. Madhusoodhanan et al., "High-Temperature Spontaneous Emission Quantum Efficiency Analysis of Different InGaN MQWs for Future Power Electronics Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2995120.
[35] A Sabbar and S. Madhusoodhanan et al. "High Temperature and Power Dependent Photoluminescence Analysis on Commercial Lighting and Display LED Materials for Future Power Electronic Modules," in Scientific Report 9, 16758, Nov. 2019, doi: https://doi.org/10.1038/s41598-019-52126-4.
[36] S. Madhusoodhanan and A Sabbar et al. "High‐Temperature Optical Characterization of GaN‐Based Light‐Emitting Diodes for Future Power Electronic Modules," in Phys. Status Solidi A, 18, Dec. 2019, doi: https://doi.org/10.1002/pssa.201900792.
[37] S. Madhusoodhanan and A Sabbar et al., "High-Temperature Analysis of GaN-based MQW Photodetector for Optical Galvanic Isolations in High-Density Integrated Power Modules," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2974788.

CHAPTER 2

DEVELOPMENT OF SIC-BASED OHMIC CONTACT

2.1 Background

The metal-semiconductor contact resistance is commonly neglected in device modeling. However, in practice, the contact resistance generates undesirable power dissipation, especially under high current conditions (e.g., electrostatic discharge (ESD)). Therefore, the Ohmic contact needs to be well designed and fabricated for not only complementary metal-oxide-semiconductor (CMOS) devices but also for ESD protection devices.

Compared to Si, SiC has lower electron affinity (i.e., 3.6 eV) and wider bandgap (i.e., 3.26 eV). This makes it more difficult for metals to form low contact resistivity with SiC devices. As a result, two strategies are commonly considered to create SiC-based Ohmic contact: first, increasing the doping concentration of the SiC contact regions to increase the field emission (FE); second, implementing metals that react with SiC to reduce the barrier height. For example, Ni is the most commonly used metal for N-type SiC Ohmic contact. It has been demonstrated that Ni generates Ni_2Si with SiC during high-temperature (HT) anneal, which reduces the barrier height and forms a promising contact resistivity [1].

Table 2.1 summarizes the SiC-based Ohmic contact studies. Highly doped SiC surface (i.e., >1E19 cm^{-3}) and high annealing temperature (i.e., >800 ºC) are required to form a promising contact resistivity (i.e., <1E-4 $\Omega \cdot cm^{-2}$). Additionally, while low contact resistivity based on N-type SiC can be achieved by Ni-SiC Ohmic contact, it requires a suitable ratio of Ni/Ti/Al stacks to form promising contact resistivity on P-type SiC. Therefore, this dissertation focuses on the Ohmic contact based on P-type SiC.

Table 2.1 Review of SiC-based ohmic contact

Metal	Type	SiC doping (cm^{-3})	Metal thickness (nm)	Annealing temperature (ºC)	Annealing time (min)	Annealing atmosphere	Contact resistivity ($\Omega \cdot cm^2$)	Ref.
Ni	N	1E19	100	900-1100	3	N_2	5E-4 – 1E-4	[1]
Ni	N	4.2E15		900-1000	1		2.4E-1 – 2.8E-3	[2]
Ni	N	1E16	100	950	1		4.8E-5	[3]
Ni	N	9E18		950	2	Vacuum	5E-6	[4]
Ni	N	2E20	50	1000	2	Ar	6E-6	[5]
Ni	P	2E20	50	1000	2	Ar	7E-3	[5]
Ni	N	3E18	150	700-950	5	Ar+1%H_2	2E-3 – 1E-5	[6]
Ni	P	3E20	100	1000	1	N_2	1E-3	[7]
Ti	N	7E18	100	900-1000	15	Vacuum	1E-4 – 6.7E-5	[8]
Ti	P	1.3E19	150	As-deposit, 700, 750	3	10% H_2/Ar	3.4E-4, 7.4E-4, 7.7E-4	[9]
Al	N	4E20		950	5	Ar	5E-2	[10]
Al	N	1E20		As-deposit			5E-6	[11]
Al	P	4.8E18	160	1000	2	Vacuum	4.5E-4	[12]
Ti/Al	P	1E19	40/60, 60/140, 100/100	900-1200	10	Ar	1E-4 – 2E-3	[13]
Ni/Al	N	1.3E19	50/6	1000	5	Vacuum	1.8E-4	[14]
Ni/Al	P	7.2E18	50/6	1000	5	Vacuum	1.2E-2	[14]

Ni/Al	N	1.3E19	50/2	900	20	Vacuum	5E-4	[15]
Ni/Al	P	7.2E18	50/6	1000	5	Vacuum	1.2E-2	[15]
Ni/Al	N	1E18	900/300	1020	5	N_2:H_2 (99:1)	1.2E-4	[16]
Ni/Al	P	1E19	50/450	1000	2	Ar	5.6E-3	[17]
Ni/Al	P	1E19	50/450	400+1000	1+2	Ar	4.5E-5	[17]
Ni/Ti/Al	N	1E19	25/50/50	800	30	Vacuum	2.5E-3	[18]
Ni/Ti/Al	N	1E19	25/50/70	800	30	Vacuum	2E-3	[18]
Ni/Ti/Al	P	8E18	20/50/50	800	30	Vacuum	2.1E-3	[18]
Ni/Ti/Al	P	8E18	20/50/70	800	30	Vacuum	2.1E-4	[18]
Ni/Ti/Al	N	1E19	80/30/80	950	5	N_2	7.8E-5	[19]
Ni/Ti/Al	N	1E19	80/30/80	1000	5	N_2	1E-4	[19]
Ni/Ti/Al	P	2E19	40/30/80	850	5	N_2	4.2E-5	[19]
Ni/Ti/Al	P	3E18	8/50/300	800	30	Vacuum	2E-4	[20]
Ni/Ti/Al	P	3E18	25/50/300	800	30	Vacuum	8E-5	[20]
Ni/Ti/Al	P	3E18	35/50/300	800	30	Vacuum	1E-4	[20]
Ni/Ti/Al	P	2E19	40/30/80	850	2	N_2	4.2E-5	[21]
Ni/Ti/Al	P	2E19	80/30/80	850	2	N_2	1.3E-4	[21]
Ni/Ti/Al	P	2E19	40/30/80	850	5	N_2	5.5E-5	[21]
Ni/Ti/Al	P	2E19	80/30/80	850	5	N_2	7.6E-5	[21]
Ni/Ti/Al	P	2E19	40/30/80	1000	5	N_2	2E-4	[21]

2.2 Characterization Methods of Ohmic Contact

Circular transfer length method (CTLM) is one of the most commonly used methods to measure Ohmic contact resistivity since it avoids current crowding and does not require isolated layers. Fig. 2.1(a) shows a CTLM structure. The structure is formed by a metallic circular inner region, a semiconductor gap and a metallic outer region. The inner radius of the inner circle and

the gap width are L and d, respectively. When $L >> d$, the resistance between the inner circle and outer region, R_T, can be expressed as [22]

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T) \tag{1}$$

Where R_{sh} is the sheet resistance of the semiconductor, and L_T is transfer length, which can be expressed as

$$L_T = \sqrt{\rho_c / R_{sh}} \tag{2}$$

Where ρ_c is the specific contact resistivity. The transfer length, L_T, is considered as the distance over which most current transfers from metal regions to semiconductor regions or from semiconductor regions to metal regions. Therefore, it can also be expressed as

$$L_T = \frac{\rho_c}{2\pi L R_C} \tag{3}$$

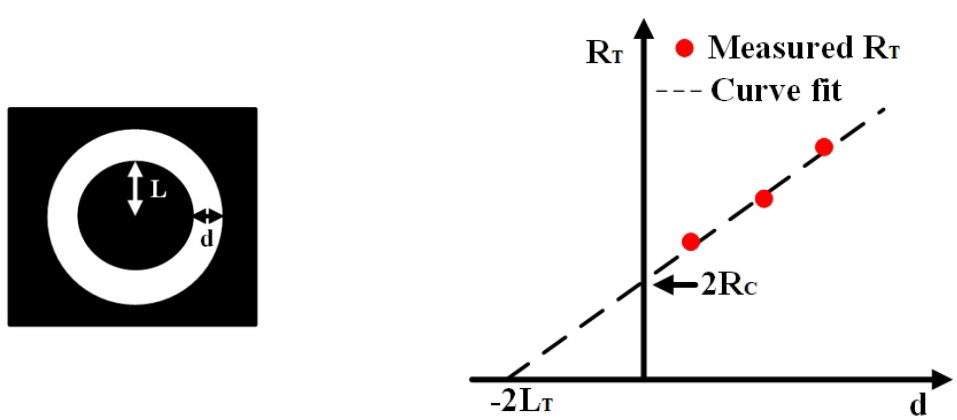
Where R_C is the contact resistance. Combining Eq. (1) to (3), when d=0,

$$R_T = \frac{2L_T R_{sh}}{2\pi L} = 2R_C \tag{4}$$

When R_T=0,

$$d = -2L_T \tag{5}$$

As a result, R_C can be estimated by measuring CTLM structures with varying gap widths, d, as shown in Fig. 2.1(b).



(a) (b)

Fig. 2.1 CTLM (a) structure and (b) R_C extraction method

2.3 Fabrication

The fabrication process of the CTLM structures were shown in Fig. 2.2. 4H-SiC P-type samples with a surface doping concentration of 5E19 cm^{-3} were utilized as substrates. The samples were cleaned by acetone, Isopropyl alcohol (IPA) and water to eliminate contaminations. Then photoresist was applied on the samples by a CEE-100 spin coater. The samples were aligned with the CTLM mask by a Karl SUSS MJB 3 Mask Aligner and exposed to ultraviolet (UV) light for 1 min. The metal deposition was carried out by an Edwards Auto - 306 E- Beam Evaporator. After that, the lift-off process was conducted to remove the metal regions that were covered by the photoresist. Finally, the samples were annealed by an SSI Solaris 150 rapid thermal anneal (RTA) furnace to form Ohmic contacts.

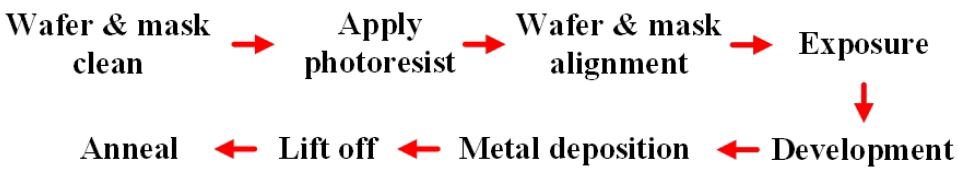


Fig. 2.2 CTLM structure fabrication process

2.4 Experimental Results

According to Table 2.1, Ni/Ti/Al stacks form good Ohmic contacts on P-type SiC samples. Thus, Ni/Ti/Al stacks with varying Ti thickness were deposited to form Ohmic contacts. Table 2.2 lists the metals and RTA conditions of the samples. The fabricated CTLM structures are shown in Fig. 2.3. The resistance of Pad 1 to 5 was extracted by Keithley 2450 source measure unit (SMU) to estimate the contact resistance. The inner radius, L, and gap width, d, of Pad 1 to 5 were listed in Table 2.3.

Table 2.2 Utilized metals and RTA conditions for SiC CTLM structure

Sample	Metal	Metal thickness (nm)	RTA temperature (ºC)	RTA time (min)
1	Ni/Al	80/80	950	4
2	Ni/Ti/Al	80/10/80	950	4
3	Ni/Ti/Al	80/30/80	950	4

Table 2.3 SiC CTLM structure profiles

Pad	1	2	3	4	5
L (μm)	200	200	200	200	200
d (μm)	10	20	30	40	50

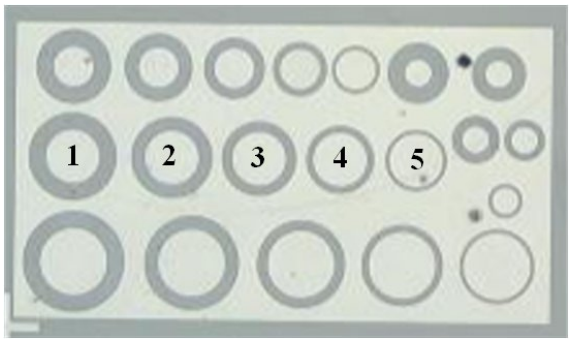


Fig. 2.3 Fabricated SiC CTLM structure

Fig. 2.4 shows the measured resistance versus the gap width, and the extracted R_C, L_T and ρ_c are listed in Table 2.3. Increasing the thickness of Ti decreases the specific contact resistivity. However, the specific contact resistivity is relatively high. CTLM structures with varying RTP conditions will be fabricated and characterized to further improve the SiC-based Ohmic contact.

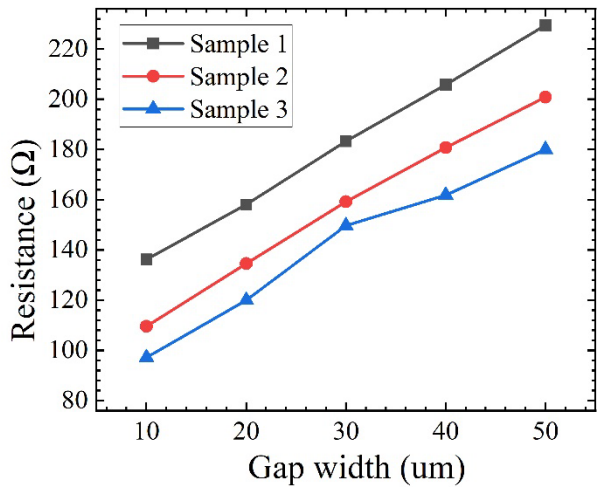


Fig. 2.4 Measured CTLM resistance with varying gap width

Table 2.4 Extracted R_C, L_T and ρ_c from CTLM structures

Sample	R_C (Ω/sq.)	L_T (μm)	ρ_c (Ωcm^2)
1	54.89	22.97	1.6E-2
2	44.23	19.23	1.1E-2
3	39.03	18.59	9.1E-3

2.5 Conclusion

In this chapter, SiC-based Ohmic contact was investigated. CTLM structures were fabricated on 4H-SiC P-type substrates. The fabrication process was presented, and experimental results show that Ni/Ti/Al is capable of forming Ohmic contacts on SiC P-type samples. The specific resistivity is ~1E-2 Ωcm^2, and the specific contact resistivity decreases with the increase of Ti thickness. CTLM structures with varying RTA conditions will be fabricated in future work to further improve the SiC Ohmic contact. A promising metal stack and RTA condition will be proposed for the fabrication of SiC-based ESD protection devices.

2.6 Reference

[1] A. V. Kuchuk et al., “Ni-based ohmic contacts to n -type 4H-SiC: The formation mechanism and thermal stability”, Adv. Condens. Matter Phys., vol. 2016, Feb. 2016.

[2] S. Y. Han et al., “Ohmic contact formation mechanism of Ni on n-type 4H–SiC”, Appl. Phys. Lett. Vol. 79, 1816, 2001.

[3] Roland Madar, Jean Camassel and Elisabeth Blanquet, “Schottky-Ohmic Transition in Nickel Silicide/SiC-4H System: the Effect of Non Uniform Schottky Barrier”, Materials Science Forum, vol. 457–460, pp. 861–864, Jun. 2004.

[4] J. Crofton, P. G. McMullin, J. R. Williams and M. J. Bozack, " High temperature Ohmic contacts to N -type 6H-SiC using nickel ", J. Appl. Phys., vol. 77, no. 3, pp. 1317-1319, Feb. 1995.

[5] S. Yoshida, S. Nishino, H. Harima and T. Kimoto, “Ohmic Contact Structure and Fabrication Process Applicable to Practical SiC Devices”, Materials Science Forum 389–393, April, 2002.

[6] R. Kakanakov, L. Kassamakova-Kolaklieva, N. Hristeva, G. Lepoeva and K. Zekentes, "Thermally stable low resistivity ohmic contacts for high power and high temperature SiC device applications," 2002 23rd International Conference on Microelectronics. Proceedings (Cat. No.02TH8595), 2002, pp. 205-208 vol.1.

[7] M. Vivona et al., "Thermal stability of the current transport mechanisms in Ni-based Ohmic contacts on n- and p-implanted 4H-SiC", Semicond. Sci. Technol., vol. 29, pp. 075018, May 2014.

[8] F. La Via, F. Roccaforte, A. Makhtari, V. Raineri, P. Musumeci and L. Calcagno, "Structural and electrical characterization of titanium and nickel silicide contacts on silicon carbide", Microelectron. Eng., vol. 60, pp. 269-282, 2002.

[9] S. K. Lee, C. M. Zetterling, M. Östling, J. P. Palmquist, H. Högberg, and U. Jansson, "Low resistivity ohmic titanium carbide contacts to n-and p-type 4H-silicon carbide", Solid-State Electron., vol. 44, pp. 1179-1186, 2000.

[10] J. H. Zhao, K. Tone, S. R. Weiner, M. A. Caleca, Honghua Du and S. P. Withrow, "Evaluation of ohmic contacts to p-type 6H-SiC created by C and Al coimplantation," in IEEE Electron Device Letters, vol. 18, no. 8, pp. 375-377, Aug. 1997.

[11] H. Na, H. Kim, K. Adachi, N. Kiritani, S. Tanimoto, H. Okushi, K. Arai, “High-quality schottky and ohmic contacts in planar 4H-SiC metal semiconductor field-effect transistors and device performance”, J. Electron. Mater., vol. 33, pp. 89-93, 2004.

[12] Brian J. Johnson and Michael A. Capano, "The effect of titanium on Al–Ti contacts to p-type 4H-SiC", Solid-State Electronics, vol. 47, no. 6, pp. 1437-1441, Sep. 2003.

[13] T. Abi-Tannous et al., "A Study on the Temperature of Ohmic Contact to p-Type SiC Based on Ti3SiC2 Phase," in IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2462-2468, June 2016.

[14] K. Ito, T. Onishi, H. Takeda et al., “Simultaneous formation of Ni/Al ohmic contacts to both n- and p-type 4H-SiC,” Journal of Electronic Materials, vol. 37, no. 11, pp. 1674–1680, 2008.

[15] I. Kazuhiro, et al., “Effects of Reducing Annealing Temperature on NiAl Ohmic Contacts to n- and p-Type 4H-SiC”, Transactions of JWRI, 2012.

[16] T. Marinova, R. Yakimova, V. Krastev, C. Hallin and E. Janzén, "Interfacial reactions and Ohmic contact formation in the Ni/Al-6H SiC system", J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom., vol. 14, no. 14, pp. 3252-3256, Jul. 1996.

[17] H. Vang, M. Lazar, P. Brosselard, C. Raynaud, P. Cremillieu, J.-L. Leclercq, et al., "Ni–Al ohmic contact to p-type 4H-SiC", Superlattices Microstruct., vol. 40, no. 46, pp. 626-631, Oct.Dec. 2006.

[18] S. Tsukimoto, T. Onishi, K. Ito and M. Murakami, "Simultaneous formation of ohmic contacts for both n- and p-type 4H-SiC using Nial-Based Contact Materials", MRS Online Proceedings Library, vol. 911, 2006.

[19] X. Zhang et al., "Study on simultaneous formation of ohmic contacts on p- and n- type 4H-SiC using Ni/Ti/Al ternary system," 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2014, pp. 1-3.

[20] R. Konishi, R. Yasokuchi, O. Nakatsuka, Y. Koide, M. Moriyama and M. Murakami, "Development of Ni/Al and Ni/Ti/Al ohmic contact materials for p-type 4H-SiC", Mater. Sci. Eng. B, vol. 98, no. 3, pp. 286-293, 2003.

[21] H. Yu, X. et al., “Thermal stability of Ni/Ti/Al ohmic contacts to p-type 4H-SiC”, Journal of Applied Physics, vol. 117 no. 2, 2015.

[22] D. K. Schroder, Semiconductor Material and Device Characterization, New York:Wiley, 1990.

CHAPTER 3

DESIGN OF ION IMPLANTATION FOR SIC DEVICES

3.1 Background

The introduction of dopants and the control of doping concentration and junction depth of semiconductor devices are mainly achieved by ion implantation and diffusion processes. However, for SiC, the diffusion process is not promising due to the low diffusion constants of the dopants in SiC. Therefore, in order to design and fabricate SiC-based ESD protection devices, ion implantation processes need to be designed. In addition, since the ESD protection devices aim to protect SiC complementary metal-oxide-semiconductor (CMOS) devices, their doping profiles and structures need to be compatible with SiC-based CMOS processes. Thus, the design of the ion implantation profiles is based on SiC CMOS processes.

The doping profiles (e.g., peak doping concentration and junction depth) of N-type and P-type regions in SiC CMOS processes, such as N+, P+, N-well and P-well, can be controlled by ion implantation dopant, dose and energy. A variety of studies, which are summarized in Table 3.1, have been conducted to investigate the ion implantation processes based on SiC substrates. According to previous work [1]-[9], the following conclusions can be made:

a) Nitrogen (N) is commonly used as an N-well implantation dopant because it has lower mass and creates lower damage compared to phosphorus (P). However, it also shows low activation rate when doping concentration (or dose) is high (>3E20 cm^{-3}).

b) Phosphorus-based ion implantation normally shows lower resistivity compared to that of nitrogen. Thus, it can be used as an implantation dopant for N+ regions. However, it is not realistic to form N-well by phosphorus implantation due to its high mass.

c) Boron (B) can be used for P-well implantation because it has a lower mass compared to aluminum (Al). However, Boron-based ion implantation also shows passivated issues at high-dose ion implantation and diffusion issues during high-temperature anneal, which makes it difficult to design boron-based ion implantation profiles for SiC.

d) Aluminum-based ion implantation shows lower resistivity and higher activation rate when the annealing temperature is higher than 1700 ºC, which makes it commonly used for P-type ion implantation.

e) It should be noted that although some reports use very high implantation doses to achieve low resistivity, this may create defects and surface roughness that cannot be recovered by the high-temperature anneal. For example, the critical doses for aluminum and boron are 1E15 cm^{-2} and 2E15 cm^{-2}. Implantation doses higher than these values are not preferred, especially for room-temperature ion implantation.

Table 3.1 Summary of SiC-based ion implantation

Dopant	Implantation condition			Anneal		Dopant density (cm-3)	Carrier concentration (cm-3)	Activation rate	Resistivity (Ωcm)	Ref.
	Total Dose (cm^{-2})	Energy (eV)	Temperature (ºC)	Temperature (ºC)	Time (min)					
N	2E13	25k – 280k	600	1700	10	5E17	4.3E17	86%	0.5	[1]
N	-	30k – 600k	500	1700	30	3.8E18	1.5E18	40%	0.03	[2]
N	-	30k – 600k	500	1700	30	7.4E19	1E19	13%	0.015	[2]
N	-	30k – 600k	500	1700	30	3E20	1E18	1%	0.03	[2]
N	4E15	-	500 - 800	1500	30	-	-	-	0.045	[3]
N	-	-	-	1700		3E20	1E20	33%	0.04	[4]

P	2E13	30k – 360k	600	1700	10	5E17	4E17	80%	0.5	[1]
P	-	70k – 750k	500	1700	30	2.6E18	1.5E18	60%	0.05	[2]
P	-	70k – 750k	500	1700	30	5E19	1.5E19	30%	0.015	[2]
P	-	70k – 750k	500	1700	30	2E20	1E20	50%	3E-3	[2]
P	4E15	30k - 195k	600	1600	10	2E20	5E19	25%	6E-3	[5]
P	4E16	30k - 195k	600	1600	10	2E21	-	-	1.8E-2	[5]
P	1E15	10k – 180k	500	1700	30	5E19	4E19	80%	6E-3	[6]
P	1E16	10k – 180k	500	1700	30	2E20	1E20	50%	1.2E-3	[6]
P	6E16	10k – 180k	500	1700	30	3E21	3E20	10%	1E-3	[6]
B	-	-	-	1700	-	3E20	2E20	66%	1	[4]
B	6.8E14	20k – 350k	700	1550 - 1700		1E19	1E18	10%	10	[7]
Al	-	-	-	1700	-	3E20	2E20	66%	0.8	[4]
Al	3.2E14	20k – 2M	500	1600 - 1800		2E18	1E18	50%	1	[7]
Al	1E14 – 1E16	30k – 180k	650	1670	6	3.3E18 – 1E21			0.1 - 5	[8]
Al	4E15	10k – 160k	500	1800	30	1E20	5E19	50%	0.2	[9]
Al	6E16	10k – 160k	500	1800	30	1E21	3E19	3%	0.05	[9]

3.2 Ion Implantation Profile Design

3.2.1 Modeling

In order to design ion implantation profiles for SiC devices, their modeling based on varying dopants needs to be understood. Monte Carlo model is the most accurate model for ion implantation. However, it is too complicated to be an analytical model. As a result, the Gaussian model and behavior models are commonly used for the design and analysis of SiC-based ion implantation. According to the Gaussian model, the relationship between implantation dose, Φ, and doping profile, $N(x)$, can be expressed as [10]

$$\Phi = \int_{-\infty}^{+\infty} N(x)dx \tag{1}$$

Based on Eq. (1), the peak doping concentration, N_m, is

$$N_m = \frac{\Phi}{\sqrt{2\pi}\cdot\Delta R_p} \tag{2}$$

Where ΔR_p is straggle, which can be considered as the width of the peak doping. Therefore, N_m is proportional to Φ.

The implantation depth is mainly determined by the implantation energy, E. According to [11] and [12], the depth of the peak doping concentration, R_m, of SiC-based ion implantation can be expressed as,

$$R_m = k_1 E - k_2[\exp(-rE) - 1] \tag{3}$$

For nitrogen and phosphorus implantation.

$$R_m = k_1(E - k_2)^r \tag{4}$$

For aluminum implantation. Where k_1, k_2, and r are fitting parameters. Their values are listed in Table 3.2.

Table 3.2 Fitting parameters for SiC-based ion implantation modeling [11], [12]

Dopants	k_1	k_2	r
N	0.472 μm/MeV	0.601 μm	1.785 MeV^{-1}
P	0.319 μm/MeV	0.746 μm	0.82 MeV^{-1}
Al	0.93 μm	0.045 MeV	0.64

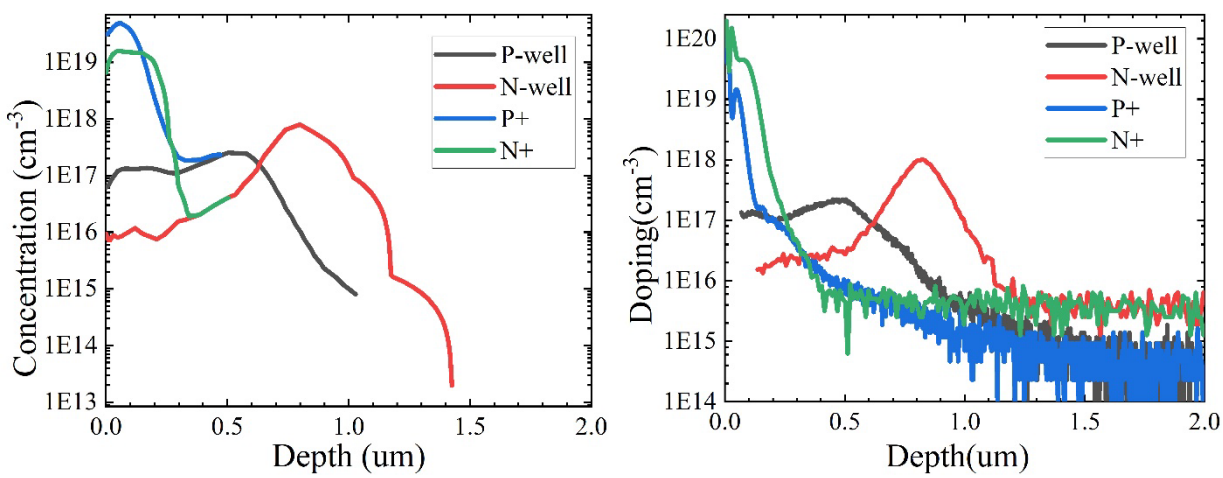
3.2.2 Ion implantation profiles

Since the ESD protection devices aim to protect SiC-based low-voltage (i.e., <20 V) CMOS devices that are commonly used for gate drivers and operational amplifiers, ion implantation profiles for SiC low-voltage CMOS process are designed. Table 3.3 lists the ion implantation profiles for P-well, N-well, P+ and N+ regions. Aluminum is used as the dopant of P-type regions, and nitrogen is utilized as the dopant of N-type regions. Multiple implantations are implemented to achieve uniform doping profiles. To estimate the doping profile, technology computer-aided design (TCAD) simulations were carried out. Monte Carlo model in Sentaurus TCAD software was utilized to achieve a high simulation precision. The simulated doping profiles based on the ion implantation profiles in Table 3.3 are shown in Fig. 3.1(a). The ion implantation processes were carried out on 4H-SiC substrates, and secondary ion mass spectrometry (SIMS) was performed to obtain the doping profiles (Fig. 3.1b). Compared Fig. 3.1(a) with Fig. 3.1(b), the simulated doping profiles highly match the measurement results.

Table 3.3 Designed ion implantation profiles for SiC CMOS process

		P-well	N-well	P+	N+
Dopant		Al	N	Al	N
Step 1	Dose (cm^{-2})	5E12	2E13	2.8E14	4E14

	Energy (keV)	540	810	90	90
Step 2	Dose (cm^{-2})	2E12	2E11	1.8E14	2.3E14
	Energy (keV)	450	380	60	50
Step 3	Dose (cm^{-2})	1.2E12	1.5E11	1.4E14	2E14
	Energy (keV)	320	270	30	25
Step 4	Dose (cm^{-2})	1E12	1E11		
	Energy (keV)	200	180		
Step 5	Dose (cm^{-2})	1E12	5E10		
	Energy (keV)	140	90		
Step 6	Dose (cm^{-2})	7E11	4E10		
	Energy (keV)	75	60		
Step 7	Dose (cm^{-2})	4E11	2E10		
	Energy (keV)	35	30		



(a) (b)

Fig. 3.1 (a) TCAD simulation results and (b) SIMS results of the designed ion implantation profiles for 4H-SiC

Although the simulation results show high math with the SIMS results, seven steps of multiple implantation processes were performed to achieve the N-well and P-well regions. This highly increases the time of the ion implantation process. Therefore, improved ion implantation profiles are designed. The ion implantation profiles are listed in Table 3.4, and the simulation results are shown in Fig. 3.2. The implantation steps of the P-well and N-well are reduced to 2 and 4, respectively.

Table 3.4 Improved ion implantation profiles for SiC CMOS process

		P-well	N-well	P+	N+
Dopant		Al	N	Al	P
Step 1	Dose (cm^{-2})	4.9E12	1.5E11	7.8E14	7.8E14
	Energy (keV)	200	320	36	36
Step 2	Dose (cm^{-2})	1E12	1.5E11	2E14	2E14
	Energy (keV)	36	180	9	9
Step 3	Dose (cm^{-2})		1.5E11	2E13	2E13
	Energy (keV)		90	18	18
Step 4	Dose (cm^{-2})		1E11		
	Energy (keV)		27		

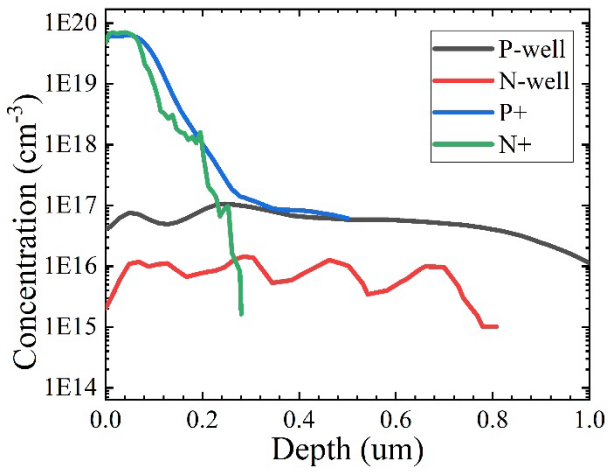


Fig. 3.2 TCAD simulation results of the improved ion implantation profiles for 4H-SiC

3.3 Conclusion

This chapter focuses on the ion implantation profile design for SiC-based ESD protection devices. The modeling of SiC-based ion implantation is presented, and the ion implantation profiles are designed and simulated by Sentaurus TCAD software. SIMS results show a high match with the simulation results. Improved ion implantation profiles are also proposed and simulated to reduce the time of the ion implantation process.

3.4 Reference

[1] M. A. Capano, J. Cooper, M. R. Melloch, A. Saxler and W. C. Mitchel, "Ionization energies and electron mobilities in phosphorus- and nitrogen-implanted 4H-silicon carbide", J. Appl. Phys., vol. 87, no. 12, pp. 8773-8777, Jun. 2000.

[2] M. Laube, F. Schmid, G. Pensl, G. Wagner, M. Linnarsson and M. Maier, "Electrical activation of high concentrations of N+ and P+ ions implanted into 4H–SiC", J. Appl. Phys., vol. 92, no. 1, pp. 549-554, Jul. 2002.

[3] G. Pensl, H. Morkoç, B. Monemar and E. Janzén, “Conductivity Control of SiC by In-Situ Doping and Ion Implantation”, Materials Science Forum, vol. 264–268, Feb. 1998, pp. 675–680.

[4] S. Seshadri, G. W. Eldridge and A. K. Agarwal, "Comparison of the annealing behavior of high-dose nitrogen- aluminium- and boron-implanted 4H-SiC", Appl. Phys. Lett., vol. 72, no. 16, pp. 2026, Apr. 1998.

[5] V. Khemka, "Characterization of phosphorus implantation in 4H-SiC", J. Electron. Mater., vol. 28, no. 3, pp. 167-174, 1999.

[6] Y. Negoro, K. Katsumoto, T. Kimoto and H. Matsunami, "Electronic behaviors of high-dose phosphorus-ion implanted 4H-SiC (0001)", J. Appl. Phys., vol. 96, no. 1, pp. 224-228, Jul. 2004.

[7] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, J. Heindl, et al., "Doping of SiC by implantation of boron and aluminum", Phys. Stat. Sol. (a), vol. 162, no. 1, pp. 277-298, 1997.

[8] J. Bluet et al., "Activation of aluminum implanted at high doses in 4H–SiC", J. Appl. Phys., vol. 88, no. 4, pp. 1971-1977, 2000.

[9] Y. Negoro, T. Kimoto, H. Matsunami, F. Schmid and G. Pensl, "Electrical activation of high-concentration aluminum implanted in 4H-SiC", J. Appl. Phys., vol. 96, no. 9, pp. 4916-4922, Nov. 2004.

[10] K. Suzuki, “Ion Implantation and Activation”, Bentham Science Publisheres Ltd, U.A.E., Sharjah, 2013.

[11] M.V. Rao, J. Tucker, O.W. Holland and N. Papanicolaou, “Donor ion-implantation doping into SiC”, J. Electron. Mater, vol. 28, no. 334, 1999.

[12] E.M. Handy, M.V. Rao, O.W. Holland, P.H. Chi, K.A. Jones, M.A. Derenge, et al., “Al, B, and Ga ion-implantation doping of SiC”, J. Electron. Mater, vol. 29, no. 1340, 2000.s

CHAPTER 4

INVESTIGATION OF ESD PROTECTION IN SIC BCD PROCESS

4.1 Abstract

In order to develop electrostatic discharge (ESD) protection structures in Silicon Carbide (SiC) process, the ESD properties of SiC silicon-controlled rectifier (SCR), lateral-diffused MOS (LDMOS) and NMOS devices are reported in this paper. All devices were fabricated using Fraunhofer 4H-SiC Bipolar-CMOS-DMOS (BCD) process and characterized by transmission line pulse (TLP) system. The scalability of the failure current (I_{t2}) of NMOS with multiple fingers is reported. The critical parameters (i.e. gate length and drift region) of LDMOS are varied to understand the effects on the triggering voltage and other ESD characteristics of the devices. The comparison of the I_{t2} between high voltage SCR (HV-SCR) and LDMOS has been investigated. TLP results show that HV-SCR structures have much higher I_{t2} than LDMOS structures. Cost-effective ESD protection structures can be designed by theses HV-SCR devices. Furthermore, ESD characteristics of SiC HV-SCR and NMOS structures are simulated using Silvaco technology computer-aided design (TCAD) software.

4.2 Introduction

With the development and utilization of wide bandgap devices, the size and weight of the power electronics decrease while the power density increases [1]. Wide bandgap materials, including gallium nitride (GaN) and silicon carbine (SiC), have gained increasing attention due to their excellent performance under extreme environment, such as high-temperature, high-power, high-voltage and strong-radiation conditions [2]. This allows power devices and modules to be used in a variety of applications, such as electric vehicle, aerospace, deep oil drilling and renewable power system [3], [4]. In order to further reduce the power loss and parasitic elements, the gate

driver circuits are expected to be integrated closely with the wide bandgap power devices, making their operating temperature same as the power devices. However, the maximum operating temperature for traditional silicon (Si) based integrated circuits (ICs) are typically below 150ºC [5]. Therefore, high-temperature integrated gate driver and control circuits based on wide bandgap process are demonstrated to cope with the challenges [6]-[8]. Although these gate driver circuits show high performance with wide range of operating temperature, the device and integrated circuit reliability are not sufficiently explored yet. Electrostatic discharge (ESD) is a major reliability issue in integrated circuits [9]. It creates the overstresses to the devices and circuits with large electric field and/or high current density, resulting in dielectric breakdown of the gate oxide or thermal runaway of semiconductor devices. ESD protection devices and circuits have been well studied in traditional Si semiconductor industry [10] to provide effective on-chip and off-chip protections for Si ICs. However, limited studies have been published in the field of SiC ESD protection.

In order to improve the reliability and robustness of SiC devices and ICs, researchers have made efforts to understand the operation of SiC ESD protection devices and designed the ESD protection circuits. Kyoung-Il Do et.al. [11] proposed a 4H-SiC protection circuit (i.e., gate-body floating NMOS (GBFNMOS)), which has low on-resistance, low triggering voltage and good high-temperature performance. The behavior of SiC junction barrier Schottky diodes under ESD human body model (HBM) stress was investigated by P. Denis et.al., aiming to address the limitation of SiC devices and process[12]. T. Phulpin et.al. [13] also studied the operation and failure mechanisms of three types of metal epitaxial-semiconductor FETs (MESFETs) under ESD stress by using transmission line pulse (TLP) and human body model (HBM) tests. The operation of SiC MOSFETs under ESD stress has been investigated and analyzed by photon emission (PE)

and spectral photon emission technique (SPE) [14], [15]. Furthermore, we previously reported 15V SiC NMOS ESD characteristics in Raytheon high-temperature silicon carbide (HiTSiC) process to explore the ESD robustness and facilitate the ESD protections for SiC ICs [16]. The electrical safe operating areas (SOAs) of low voltage SiC NMOS devices with different channel width, gate length and gate bias are characterized by the TLP system. The TLP system can reveal the triggering voltage (V_{t1}), failure voltage (V_{t2}) and failure current (I_{t2}) of semiconductor devices under short pulse condition (i.e., 100ns pulse width). Relatively low I_{t2} (~ 0.2mA/μm) was observed for low voltage SiC NMOS devices. Although progress has been made in SiC ESD studies in these years, the investigation of ESD characteristics and protection scheme in SiC Bipolar-CMOS-DMOS (BCD) process is not yet investigated. BCD process is capable of designing power ICs. It integrates bipolar junction transistors, CMOS and DMOS on the same substrate. The DMOS devices in BCD process can be used to design power or high-voltage circuits. The Bipolar and CMOS devices are used to design the low voltage circuits. In order to improve the reliability of ICs in SiC BCD process, effective ESD protection structures need to be determined. Thus, various structures (i.e., high-voltage silicon-controlled rectifier (HV-SCR), lateral-diffused MOS (LDMOS) and NMOS) fabricated in Fraunhofer 4H-SiC BCD process are characterized by the TLP system. The operations of these structures under ESD stress are also discussed in this paper.

4.3 Layout and Experimental Results

The SiC devices were fabricated using the Fraunhofer 4H-SiC BCD process [17]. The layout of the devices (i.e., HV-SCR, LDMOS and NMOS) can be found in Fig. 4.1. The highlighted regions are NMOS structures, HV-SCR structures and LDMOS structures respectively. The NMOS structures varying from different number of fingers were designed, aiming to investigate the scalability of the MOSFETs. Each finger of the NMOS structures has 1μm gate length and

60μm channel width. In order to investigate the V_{t1}, various HV-SCR and LDMOS structures with different gate length and drift length were designed. The HV-SCR and LDMOS structures channel with same width were also fabricated to observe the ESD robustness of these two devices.

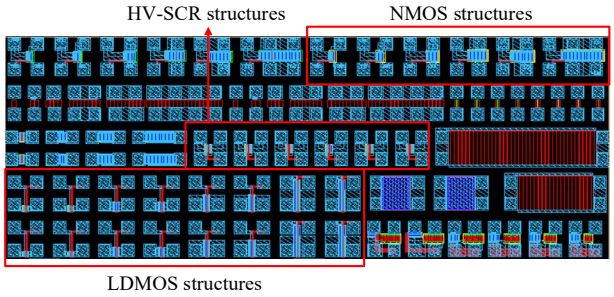


Fig. 4.1 The testchip of the SiC devices

4.3.1 NMOS

The ESD characteristics of the devices were investigated by using TLP system (Model ES62X TLP from ESDEMC) with 10ns rise time and 100ns pulse width, which provides reliable and repeatable waveform for the measurement. In order to explore the scaling of SiC NMOS devices, NMOS devices with different fingers (i.e., 2, 4 and 10) were designed. Each finger has 60μm channel width. The scalability of the I_{t2} of NMOS with different fingers can be found in Fig. 4.2. The gate terminal of the NMOS was tied to ground during the experiment. Under ESD condition, the current path is generated by the parasitic NPN bipolar transistor in the NMOS structure. The collector region of the NPN is formed by the drain of the NMOS, the emitter region is formed by the source, and the base region is formed by the substrate [10]. When the voltage reaches the avalanche breakdown voltage of the drain and substrate junction, the parasitic NPN bipolar transistor turns on to discharge the ESD current. The holding voltage (V_h) and on-resistance (R_{on}) of the device are determined by the current gain of the parasitic NPN bipolar transistor. Higher current gain leads to lower V_h and R_{on}. As shown in Fig. 4.2, the NMOS triggers at 30V. The current gain of the parasitic NPN bipolar transistor in the NMOS is too low to cause the snapback.

The I_{t2} elevates considerably with the increase in the finger. Although the multi-finger NMOS has a higher I_{t2}, the I_{t2} per μm of the 10-finger NMOS (i.e., 0.5mA/μm) is lower than 2-finger NMOS (i.e., 1mA/μm). When the number of the fingers increases to 10, the current distribution is not uniform in the NMOS structures. One or several fingers have higher current density than others, making these fingers damaged beforehand. Therefore, the I_{t2} per μm reduces when the number of finger increases. Furthermore, the I_{t2} per μm of the NMOS structures in the testchip is higher than the I_{t2} per μm (0.2mA/μm) of the 15V SiC NMOS structures we reported previously.

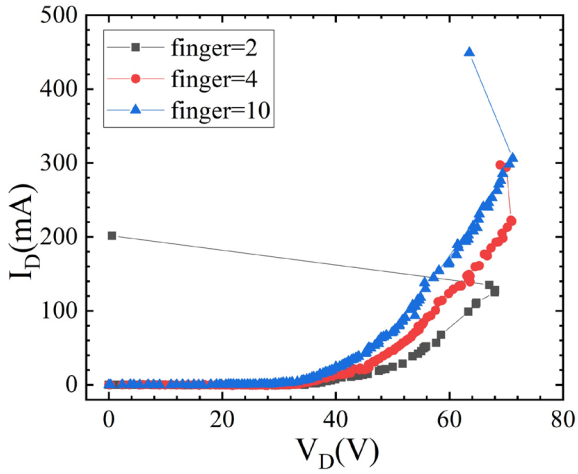


Fig. 4.2 TLP I-V curves of NMOS with different fingers

4.3.2 LDMOS

TLP I-V curves of LDMOS with different gate length (L) are showed in Fig. 4.3. The cross-section of the LDMOS can be found in the insert of Fig. 4.3. The high-voltage N-well, which has low doping concentration, elevates the triggering voltage, making the V_{t1} around 220V. Varying the gate length has minor impacts on the V_{t1}. For example, the V_{t1} increases from 224V to 229V while the gate length varies from 3μm to 5μm. The gate length of LDMOS also indicates the base width of the parasitic NPN. The increase in gate length leads to the decrease of current gain, which increases the triggering voltage. Furthermore, the LDMOS is damaged instantaneously after the triggering. The triggering current (I_{t1}), which is 0.06mA/μm, can be considered as the failure

current (I_{t2}). The I_{t2} per μm of the LDMOS structures (i.e., 0.06mA/μm) is significantly lower than the NMOS structures. The LDMOS structure is not an area-efficient ESD protection device.

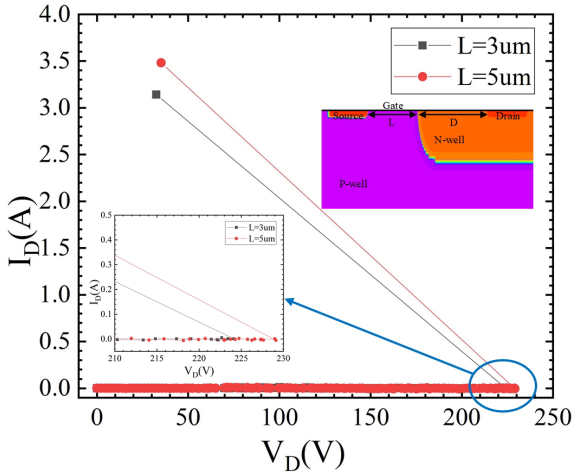


Fig. 4.3 TLP I-V curves of LDMOS with different gate length

Fig. 4.4 shows the TLP I-V characteristic curves of LDMOS with different drift length (D). It can be observed that the triggering voltage of the LDMOS structure has a strong dependence on the drift length. Smaller drift region leads to lower V_{t1}. When the drift length decreases from 6μm to 4μm, the V_{t1} decreases from 224V to 202V. Moreover, the devices do not survive after the triggering. The snapback behavior cannot be observed. The I_{t1}, which is 0.06mA/μm, can be considered as I_{t2}.

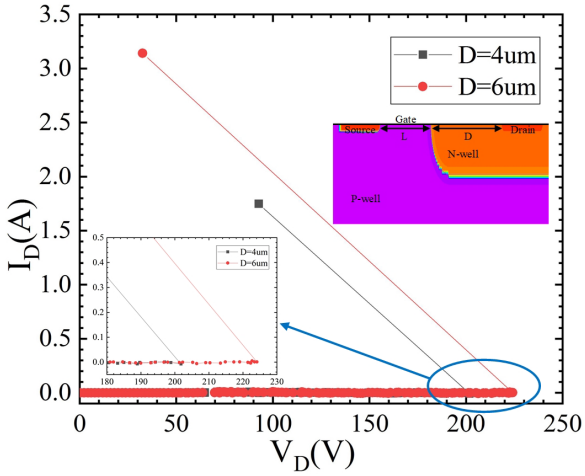


Fig. 4.4 TLP I-V curves of LDMOS with different drift length

4.3.3 Silicon-controlled Rectifier (SCR)

For on-chip ESD protections, various devices (i.e., NMOS, PMOS, NPN, PNP etc) can be implemented as the primary ESD cell. The area of the ESD cell is determined by the I_{t2} of the devices. As the results shown before, SiC NMOS and LDMOS devices have relatively low I_{t2} (i.e., 1mA/μm and 0.06mA/μm). ESD generates high voltage and high current. For example, 2kV HBM ESD stress injects around 1.33A peak ESD current to the ICs or semiconductor devices. Therefore, it will consume large areas by using these types of NMOS and LDMOS devices to design cost-effective SiC on-chip ESD protection cells. Si SCR structures formed by a pair of NPN and PNP bipolar transistors have been demonstrated as an area-efficient ESD protection components due to their high I_{t2}, low on-resistance (R_{on}) and strong snapback behavior [10], [18]. In order to explore an area-efficient SiC ESD protection device, the ESD characteristics of SiC HV-SCR structures were designed, fabricated and characterized by the TLP system.

Fig. 4.5 shows the cross-section of SiC HV-SCR. The N+ and P+ region in the P-well, which are tied together, form the source and body of the LDMOS, respectively. The N+ region in the high-voltage N-well forms the drain of the LDMOS. A P+ region tied to the N+ region is implanted into the N-well to generate the HV-SCR structure. The gate terminal of the HV-SCR is tied to ground during the TLP. The V_{t1} and V_h of the SiC HV-SCR are determined by the current gain of the parasitic NPN and PNP bipolar transistor in HV-SCR. The current gain of the two parasitic bipolar transistors is related to the gate length (L) and drift length (D) in Fig. 4.1. The reduction of L and D can increase the current gain, lowering the V_{t1} and V_h.

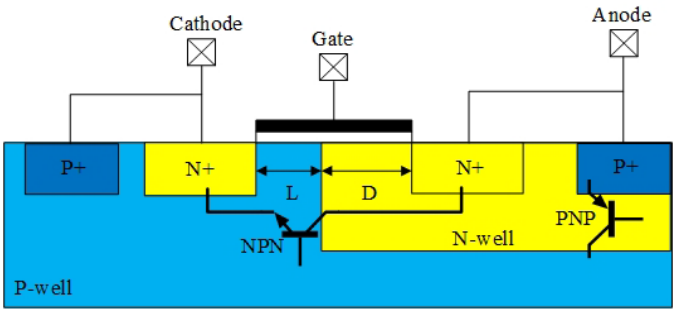


Fig. 4.5 Cross-section of SiC HV-SCR

Fig. 4.6 shows the TLP I-V curves of HV-SCR and LDMOS with the same device width (i.e. 60μm). The gate of the HV-SCR and LDMOS were tied to ground during the measurements. The HV-SCR triggers at around 220V and then shows a strong snapback behavior during TLP measurements. Low holding voltage (i.e., 50V) indicates a high current gain of parasitic PNP and NPN. It can be observed that the exceptionally high I_{t2} of the HV-SCR (i.e., 62mA/μm) can be achieved when compared with that of the LDMOS (i.e., 0.06mA/μm). When the voltage reaches the avalanche breakdown of the P+ and N-well junction, the parasitic PNP bipolar transistor turns on and discharges the ESD current. The high injecting current makes the base-emitter junction of the NPN forward biased and triggers the NPN. The current through NPN bipolar transistor supplies the forward bias of the PNP. The current gain of the device can be defined as the multiplication of the two bipolar transistors' current gain. As a result, the SCR structure has low holding voltage (V_h), on-resistance (R_{on}) and high failure current (I_{t2}). Higher I_{t2} suggests that area-efficient ESD protection structures can be designed using these HV-SCR devices.

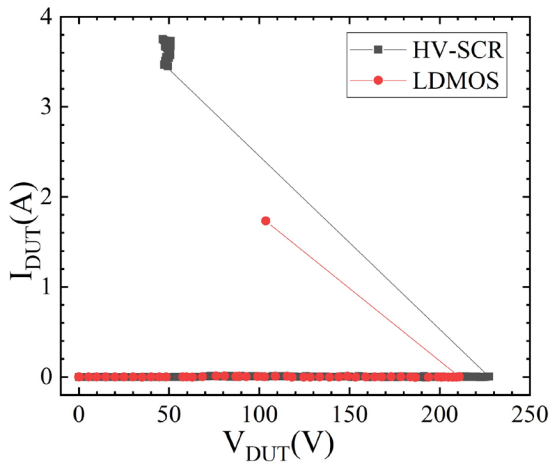


Fig. 4.6 TLP I-V curves of HV-SCR and LDMOS with same width

TLP I-V curves of HV-SCR with different drift length are given in Fig. 4.7. The V_{t1} of the HV-SCR is related with the length of the drift length. When the drift length increases from 7μm to 11μm, V_{t1} increases from 228V to 232V. The drift length determines the base width of the parasitic PNP in HV-SCR, which has a significant impact on current gain. With the drift length increasing, the current gain decreases, elevating the triggering voltage. Furthermore, strong snapback and low R_{on} are observed in HV-SCR I-V curves.

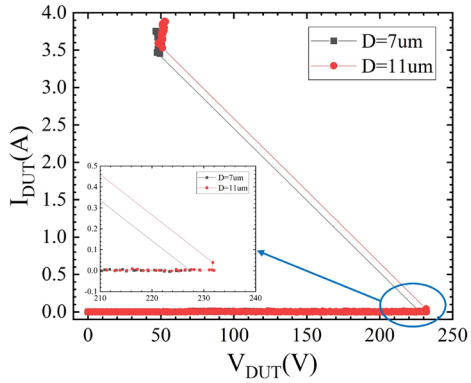


Fig. 4.7 TLP I-V curves of HV-SCR with different drift length

4.4 Simulation results

In order to further understand the operation of the SiC ESD protection devices, the ESD characteristics of HV-SCR structure is simulated with the help of Silvaco technology computer-

aided design (TCAD) tool. The operation of the SiC HV-SCR structure under ESD stress will be discussed based on the current density contribution shown by the TCAD software.

The ESD simulation result of HV-SCR is shown in Fig. 4.8. The HV-SCR has 200V V_{t1} and shows a snapback behavior after triggering. The injected P+ in N-well generates a parasitic PNP bipolar transistor with N-well and P-well. The V_h of the HV-SCR depends on the multiplication of the current gain of the parasitic NPN and PNP bipolar transistors. Fig. 4.9(a) describes the current density distribution of the HV-SCR before triggering. The anode voltage is too low to start the avalanche breakdown and turn on the device. The current density distribution of the HV-SCR after triggering can be found in Fig. 4.9(b). The ESD current flows from anode to cathode after the avalanche breakdown between the N-well and P-well.

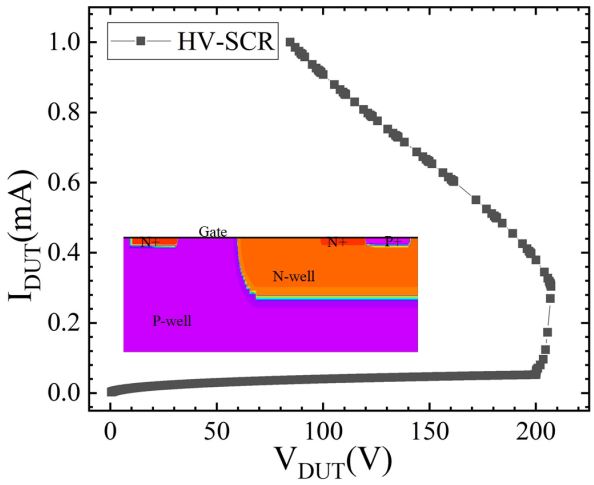
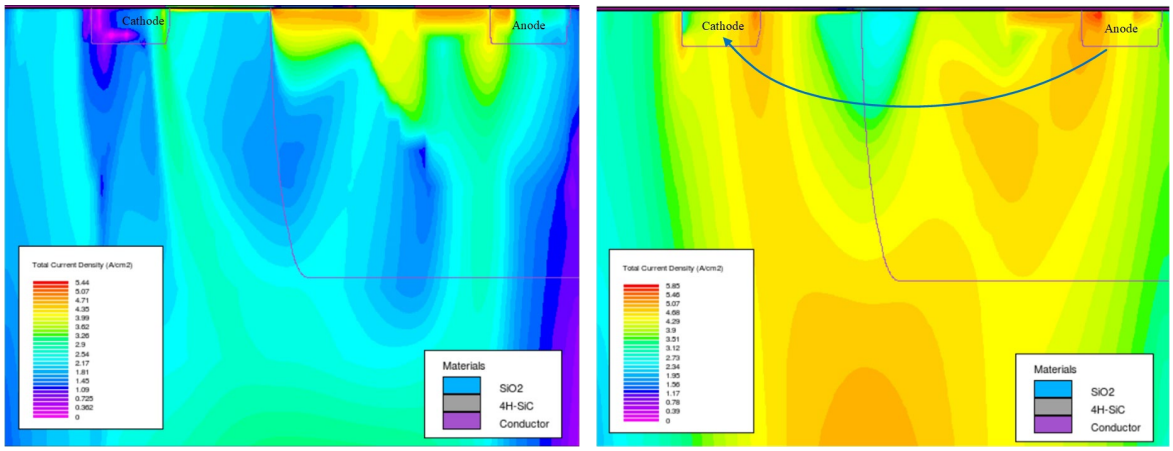


Fig. 4.8 Simulation result of HV-SCR



(a) (b)

Fig. 4.9 Current density distribution of HV-SCR (a) before triggering, (b) after triggering

4.5 Conclusions

To investigate the ESD capability of SiC devices, ESD characteristics of HV-SCR, LDMOS and NMOS fabricated in Fraunhofer 4H-SiC BCD process were obtained by TLP system and discussed based on TCAD simulation results. The TLP results show that the HV-SCR ,which I_{t2} is 62mA/µm, can be used as an area-efficient ESD protection devices. The TLP I-V curves also indicate the drift length can affect the V_{t1} of HV-SCR. The V_{t1} of LDMOS has dependence on the gate length and drift length. The increase in the gate length and drift length elevates the V_{t1}. Furthermore, the scalability of NMOS with different fingers were investigated.

4.6 Acknowledgment

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4.7 Reference

[1] H. A. Mantooth, M. D. Glover, P. Shepherd, “Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems”, Emerging and Selected Topics in Power Electronics IEEE Journal of, vol. 2, pp. 374-385, 2014.

[2] S. Ji, Z. Zhang, F. Wang, “Overview of high voltage SiC power semiconductor devices: development and application”, CES Transactions on Electrical Machines and Systems, vol. 1, no. 3, pp. 254-264, September 2017.

[3] J. Hornberger, A.B. Lostetter, K.J. Olejniczak, T. McNutt, S. Magan Lal, A. Mantooth, "Silicon-Carbide (SiC) Semiconductor Power Electronics for Extreme High-Temperature Environments", 2004 IEEE Aerospace Conference, vol. 4, pp. 2538-2555, 6–13 Mar 2004.

[4] A. Rahman, L. Caley, S. Roy, N. Kuhns, A. Mantooth, J. Di, A. M. Francis, J. Holmes, "High temperature data converters in silicon carbide CMOS", IEEE Trans. Electron Devices, vol. 64, no. 4, pp. 1426-1432, Apr. 2017.

[5] S. Kaplan, T. Griffin, and S. Bayne, “Silicon vs silicon carbide device characterization,” in Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003. 14th IEEE International, vol. 2, 2003, pp. 1217-1220 Vol. 2.

[6] M. Barlow, S. Ahmed, H. A. Mantooth, A. M. Francis, “An integrated SiC CMOS gate driver”, Proc. Conf. IEEE Appl. Power Electron. Conf. Expo. (APEC), pp. 1646-1649, May 2016.

[7] N. Ericson et al., “A 4H Silicon Carbide Gate Buffer for Integrated Power Systems”, IEEE Transacions on Power Electronics, vol. 29, no. 2, pp. 539-542, Feb. 2014.

[8] S. Kargarrazi, L. Lanni, A. Rusu, C.-M. Zetterling, “A monolithic SiC drive circuit for SiC Power BJTs”, 2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD), pp. 285-288, 2015.

[9] R. G. Wagner, J. M. Soden, C. F. Hawkins, "Extent and cost of EOS/ESD damage in an IC manufacturing process", Proc. EOS/ESD Symp., vol. EOS-15, pp. 49-55, Sept. 1993.

[10] A. Amerasekera, C. Duvvury, ESD in Silicon Integrated Circuits, New York:Wiley, 1995.

[11] K.-I. Do, B.-S. Lee, Y.-S. Koo, “Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications”, IEEE Electron Device Lett., vol. 40, no. 2, pp. 283-286, Feb. 2019.

[12] P. Denis et al., “Robustness of 4H-SiC 1200V Schottky diodes under high electrostatic discharge like human body model stresses: An in-depth failure analysis”, Diamond Related Mater., vol. 44, pp. 62-70, Apr. 2014.

[13] T. Phulpin et al., “Contribution to Silicon-Carbide-MESFET ESD Robustness Analysis”, IEEE Transactions on Device and Materials Reliability, Vol. 18 , pp. 214-223, June 2018.

[14] Niemat Moultif, Eric Joubert, Olivier Latry, “SiC MOSFET robustness to ESD study: Correlation between electrical and spectral photo-emission characterizations”, 2018 19th IEEE Mediterranean Electrotechnical Conference (MELECON), 2-7 May 2018.

[15] N. Moultif, E. Joubert, M. Masmoudi, O. Latry, "Characterization of ESD Stress Effects on SiC MOSFETs Using Photon Emission Spectral Signatures", 2017 Reliability and Maintainability Symposium (RAMS), pp. 1-7, 23-26 January), 2017.

[16] D.T. Jarard, S. Ahmed, T. Vrotsos, Z. Chen, “Electrical safe operating area of low-voltage silicon carbide NMOS transistors”, 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 7-9 Nov. 2016.

[17] L. D. Benedetto, G. D. Licciardo, A. Rubino, "Experimental results on lateral 4H-SiC UV photodiodes", Proc. 7th IEEE Int. Workshop Adv. Sensors Interfaces (IWASI), pp. 252-254, Jun. 2017.
[18] M. Kang et. al., “SCR-based ESD protection for high bandwidth DRAMs”, 2007 IEEE Asian Solid-State Circuits Conference, Nov. 2007.

CHAPTER 5

AREA-EFFICIENT SILICON CARBIDE SCR DEVICE FOR ON-CHIP ESD PROTECTION

5.1 Abstract

This paper introduces a SiC-based high-voltage silicon-controlled rectifier (HV-SCR) for on-chip electrostatic discharge (ESD) protection. The SiC HV-SCR is formed by implanting a P+ region into the N-well of SiC laterally-diffused metal-oxide semiconductor (LDMOS) structures. Both LDMOS and HV-SCR structures were characterized using a transmission line pulse (TLP) system to investigate their ESD behaviors. The TLP measurement results show that the trigger voltage (V_{t1}) of the SiC HV-SCR is ~230 V and has minor dependence on the drift length. The V_{t1} of the SiC LDMOS decreases from 224 V to 202 V when its drift length decreases from 6 µm to 4 µm. TLP measurements with 500 Ω impedance were conducted to obtain an accurate holding voltage (V_h) and failure current (I_{t2}) of HV-SCR and LDMOS. Relatively high I_{t2} (i.e., 33 mA/µm) of the HV-SCR structure was observed, which is much stronger than the LDMOS structure (i.e., 0.2 mA/µm). The V_{t1} and V_h of HV-SCR were also investigated with varying gate bias voltage. Moreover, technology computer-aided design (TCAD) simulations of the SiC HV-SCR and LDMOS were carried out to further understand their ESD behaviors.

5.2 Introduction

With the development of power electronics, aerospace and automobile industries, there is a growing expectation to employ wide bandgap (WBG) semiconductor devices [1] and integrated circuits (ICs) [2]-[5] in high temperature environments [6], [7]. The design of silicon (Si) based ICs for high-temperature (e.g., 150 ºC) applications becomes more challenging due to the drastic alteration of the leakage current, threshold voltage and electron mobility [8]. This drives the study

of silicon carbide (SiC) devices and ICs for high temperature applications. A variety of SiC-based ICs have been demonstrated, such as high-current, high-temperature bipolar SiC ICs [9], SiC digital logic gates functioning at 600 ºC [10], SiC CMOS digital circuits operating at temperatures exceeding 300 ºC [11], high-temperature (i.e., ~400 ºC) analog ICs in SiC bipolar technology [2] and 4H-SiC ultraviolet (UV) photodiodes [12]. Although these SiC ICs show high performance with a wide range of operating temperatures, the reliability is not sufficiently explored yet. Among the reliability issues, electrostatic discharge (ESD) is a great matter of concern that causes more than one-third IC failures [13]. Therefore, in order to improve the reliability of SiC ICs, SiC-based on-chip ESD protection devices and circuits are highly desired to be investigated.

Several SiC-based ESD protection devices and circuits have been studied in recent years. A 4H-SiC ESD protection circuit (i.e., gate-body floating NMOS (GBFNMOS)) is proposed and investigated by Kyoung-II Do et al. [14]. The transmission line pulse (TLP) measurement results show that the proposed GBFNMOS has low on-resistance, low trigger voltage and good high-temperature performance. In previous research [15], we reported ESD characteristics of 15 V SiC NMOS in Raytheon high-temperature silicon carbide (HiTSiC) process to explore the ESD robustness and facilitate ESD protections for SiC ICs. The electrical safe operating areas (SOAs) of low voltage SiC NMOS devices with different channel width, gate length and gate bias were characterized by the TLP system. Although the approaches of designing the trigger voltage (V_{t1}) and the trigger current (I_{t1}) have been understood, increasing the failure current (I_{t2}) of the low voltage SiC NMOS devices (~0.2 mA/μm) still needs to be further explored. For on-chip ESD protections, area-efficient structures are always desired to reduce the chip cost. In addition, area-efficient structures introduce less parasitic capacitance and smaller DC leakage current, which is an optimal option for some applications (e.g. high-speed interface ICs). Among the most

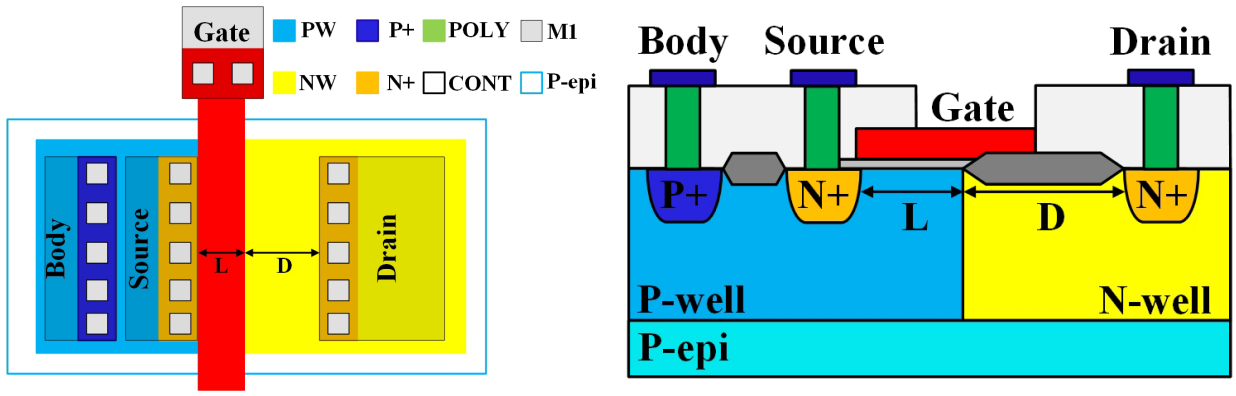
commonly used devices, the silicon-controlled rectifier (SCR) has been widely implemented as one of the area-efficient on-chip ESD protection solutions due to its high I_{t2} and low on-resistance (R_{on}) [16]. The approaches to improve the SCR characteristics, such as increasing I_{t2} and modifying V_{t1} and holding voltage (V_h), have been well studied [17]-[19].

This paper introduces an area-efficient SiC-based high-voltage SCR (HV-SCR) structure that is formed by adding a highly doped P+ region in typical SiC laterally-diffused metal-oxide semiconductor (LDMOS) devices. The SiC LDMOS and HV-SCR structures were fabricated in 4H-SiC Bipolar-CMOS-DMOS (bipolar-CMOS-double diffused MOS, BCD) process by Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie (IISB) in Germany [20]. Both the SiC LDMOS and the HV-SCR structures were characterized using the 50 Ω and 500 Ω load TLP system to investigate their ESD characteristics. The operations of LDMOS and HV-SCR structures under ESD stress are described with insight from technology computer-aided design (TCAD) simulations.

5.3 Experimental results

The SiC SCR devices were designed using the 4H-SiC BCD process in collaboration with Fraunhofer IISB [20]. The minimum linewidth for the SiC BCD process is 1 μm. The process has twin wells and a single metal layer for interconnect routing. Two types of devices (i.e., LDMOS and HV-SCRs) were designed with this SiC BCD process. Figs. 5.1(a) and (b) show the layout and cross-section of the SiC LDMOS. The device is created in a lightly doped (i.e., 1E15 cm^{-3}) P-epitaxial layer. Aluminum (Al) is implanted to form the P-well. The drift region of the SiC LDMOS device is formed by ion-implantation with nitrogen (N). The source and drain of LDMOS were also created by ion-implantation of N+ regions into P-well and N-well, respectively. The

LDMOS devices have various channel widths (i.e., 60 µm and 240 µm), gate lengths (L, i.e., 3 µm and 5 µm) and drift lengths (D, i.e., 4 µm and 6 µm).

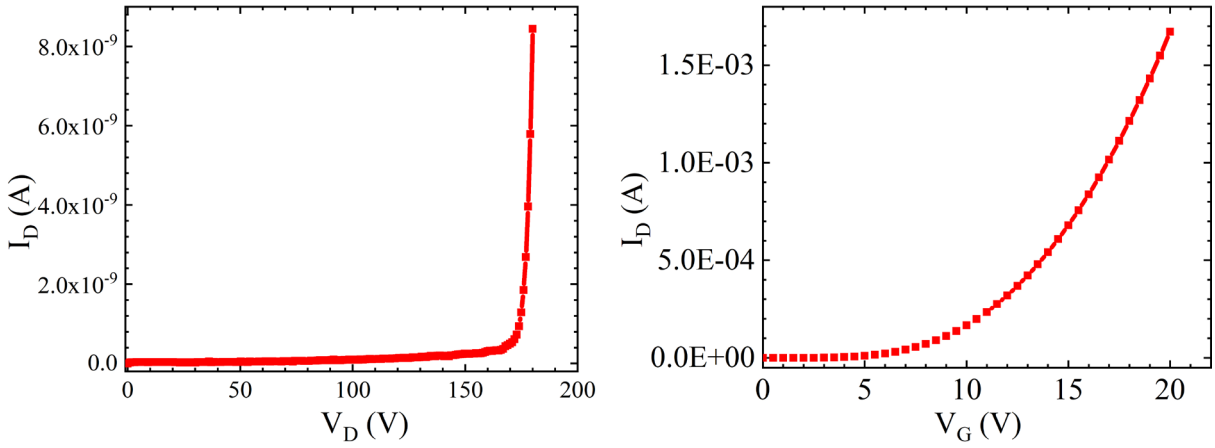


(a) (b)

Fig. 5.1 SiC LDMOS (a) layout, (b) cross-section

5.3.1 LDMOS

The SiC LDMOS drain-source breakdown curve with gate voltage $V_G = 0$ V can be found in Fig. 5.2(a). The device has 240 µm channel width, 5 µm gate length and 6 µm drift length. The leakage current before the breakdown is below ~50 pA. The drain-source DC breakdown voltage is 175 V, at which drain current (I_D) crosses 1 nA. Fig. 5.2(b) shows the DC drain current versus gate voltage (I_D-V_G) characteristics of the LDMOS with gate voltage (V_G) varying from 0 to 20 V with a 40 V drain-source bias (V_{DS}). The threshold voltage (V_{th}) of the LDMOS is ~5 V.



(a) (b)

Fig. 5.2 SiC LDMOS (a) DC breakdown with V_G=0 V, (b) I_D-V_G curve

In order to investigate the ESD behaviors of the SiC LDMOS, the devices were characterized by the TLP system (Model ES62X TLP from ESDEMC) with 10 ns rise time, 100 ns pulse width and 50 Ω load line. The gate terminal was grounded during the measurements. Fig. 5.3 shows the TLP measurement results of SiC LDMOS with 60 μm channel width and different gate lengths and drift lengths. After the trigger (inserts of Fig. 5.3), the LDMOS structure failed instantaneously. When drift length is 6 μm, V_{t1} is ~225 V and has a minor dependence on gate length. The short duration of the TLP pulses reduces the self-heating of the devices, making the V_{t1} higher than the DC breakdown voltage. The holding voltage (V_h) and on-resistance (R_{on}) are related to the current gain of the parasitic lateral NPN bipolar transistor in the LDMOS. The gate length of LDMOS denotes the base width of the parasitic NPN. The increase of gate length leads to the decrease of the current gain, which increases the V_h and R_{on}. However, the trigger current (I_{t1}), which can be considered as the failure current (I_{t2}), is relatively low (i.e., ~10 mA). The LDMOS devices do not survive before they reach the holding voltage. Moreover, it can be observed that varying drift length has impacts on the V_{t1}. The V_{t1} decreases from 224 V to 202 V while the drift length decreases from 6 μm to 4 μm. The V_{t1} of the LDMOS device is mainly determined by the avalanche breakdown voltage between the N-well and P-well. Furthermore, the low-doped drift region of the LDMOS (i.e., N-well) induces significant shunt resistance, causing a part of V_{t1} to drop in this region [21]. Therefore, the V_{t1} is also related to drift length. The longer drift length increases the N-well shunt resistance, creating a higher voltage drop in this area [22]. Thus, a higher voltage is required to turn on the device.

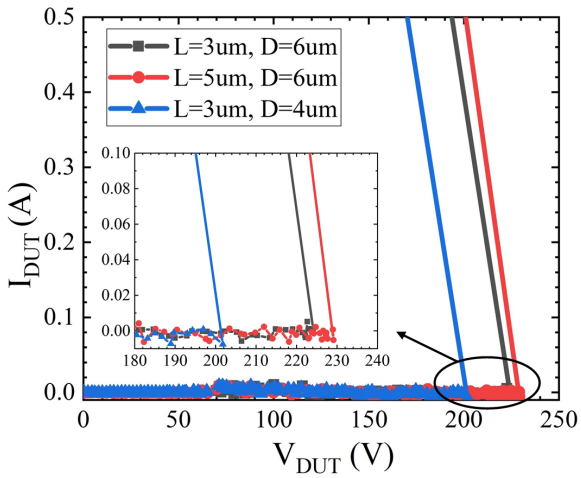
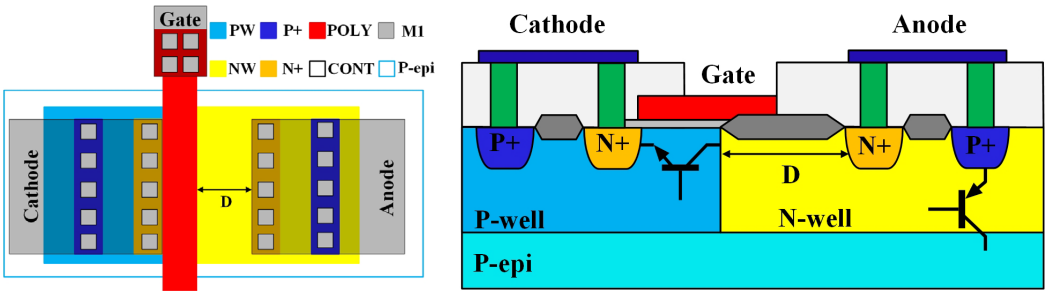


Fig. 5.3 SiC LDMOS TLP measurement results with different gate length (L) and drift length (D).

5.3.2 HV-SCR

The layout and cross-section of the SiC HV-SCR can be found in Figs. 5.4(a) and (b), respectively. A P+ region is implanted into the N-well of SiC LDMOS to form the PNPN structure (i.e., SCR structure). The N+ and P+ region in P-well, which are the body and source of the LDMOS, are tied together to form the cathode of the HV-SCR. The implanted P+ region is connected to the N+ region which then becomes the anode of the HV-SCR. The SiC HV-SCR structures have a gate length of 4 μm and the same channel width (i.e., 60 μm) as the LDMOS. Various drift lengths of the HV-SCR structures (i.e., 7 μm and 11 μm) were fabricated to investigate their ESD behaviors.



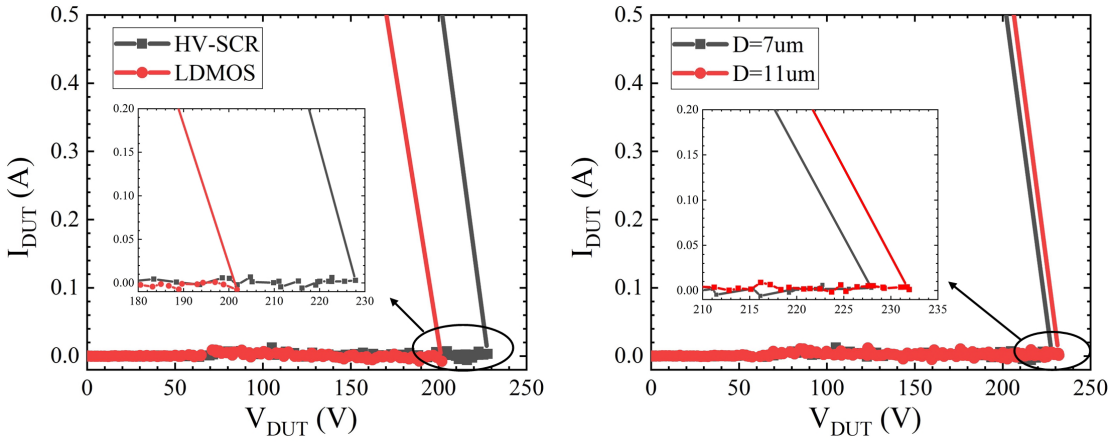
(a) (b)

Fig. 5.4 SiC HV-SCR structure (a) layout, (b) cross-section

The TLP measurement results of the HV-SCR and LDMOS are given in Fig. 5.5(a). The LDMOS has a gate length of 3 μm and a drift length of 4 μm. The HV-SCR has a gate length of 4 μm and a drift length of 7 μm. Both devices have the same channel width (i.e., 60 μm). The gate terminals of the devices were grounded during the measurements. The leakage current (at 5 V DC bias) was measured after each TLP pulse to identify the failure point. As shown in Fig. 5.5(a), the HV-SCR triggers at 228 V and fails after the trigger. Fig. 5.5(b) shows the TLP measurement results of HV-SCR with different drift length. Varying drift length (i.e., from 7 μm to 11 μm) has limited impacts on the V_{t1}. The V_{t1} increases from 228 V to 233 V when the drift length varies from 7 μm to 11 μm. Meanwhile, both devices show failure after the trigger. The V_h, I_h and I_{t2} characterized by the TLP system with a 50 Ω impedance may not be accurate, especially for high-voltage ESD protection devices [23], [24]. After the trigger of the device, the voltage and current obtained by the TLP system are limited by the applied pulse voltage and its impedance [23], which can be expressed as:

$$I_{DUT} = (V_{t1} - V_{DUT})/Z_{TLP} \quad (1)$$

Where V_{DUT} and I_{DUT} are the voltage and current obtained by the TLP system after the trigger of the device, and Z_{TLP} is the impedance of the TLP system. According to (1), the current obtained by the TLP system after the trigger of the LDMOS and HV-SCR is over 4 A, which may be much higher than the I_{t2} of the devices. Thus, the exact V_h, I_h and I_{t2} cannot be observed by the TLP system with 50 Ω impedance.

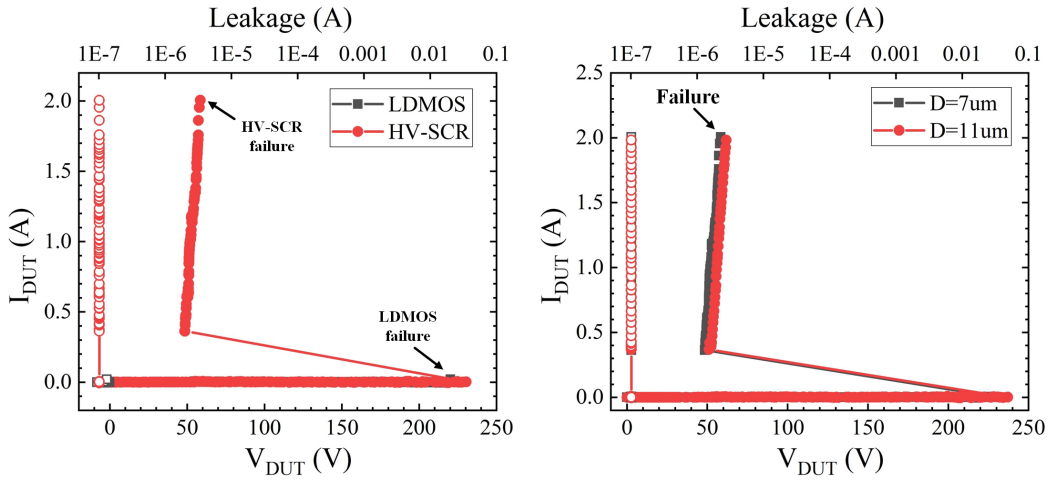


(a) (b)

Fig. 5.5 TLP measurement results of (a) SiC HV-SCR and LDMOS, (b) SiC HV-SCR with different drift length (D).

To obtain the precise I_{t2} and observe the snapback behavior of SiC LDMOS and HV-SCR, TLP measurements with a high impedance (i.e., 500 Ω) were carried out. For 500 Ω impedance TLP system, the slope of the TLP load line is lower than that of the 50 Ω impedance TLP system [23], [24]. Thus, more data points can be obtained during the trigger and snapback process. The 500 Ω impedance TLP measurement results of SiC LDMOS and HV-SCR are shown in Fig. 5.6(a). The leakage current was measured under 5 V DC bias. The channel width of the devices is 60 µm. The SiC LDMOS shows failure after the device trigger. The observed I_{t2} is 12 mA (0.2 mA/µm). The SiC HV-SCR triggers at 230 V and shows a strong snapback behavior. The V_h of the HV-SCR is 48 V, and its I_{t2} is 2 A (33 mA/µm). Compared with SiC LDMOS, the HV-SCR has exceptionally high I_{t2}. Higher I_{t2} suggests that area-efficient ESD protection structures can be designed using these HV-SCR devices. The I_{t2} of SiC HV-SCR (i.e., 33 mA/µm) is at the same level when compared with that of the similar Si-based devices (i.e., 10 mA/µm to 50 mA/µm) [25]-[29]. Fig. 5.6(b) shows the 500 Ω impedance TLP measurement results of the SiC HV-SCR with different drift lengths. The V_{t1}, V_h and I_{t2} show little change when the drift length varies from 7 µm to 11

μm. The V_{t1} increases from 230 V to 237 V. The V_h and I_{t2} of the devices are ~48 V and ~2 A. The V_h of the HV-SCR is determined by the current gain of the parasitic NPN and PNP bipolar transistors. The drift length of the HV-SCR determines the collector width of the NPN. The collector width does not affect the current gain. Therefore, the considerable variation of the V_h cannot be observed.



(a) (b)

Fig. 5.6 500 Ω impedance TLP measurement results of (a) SiC HV-SCR and LDMOS, (b) SiC HV-SCR with different drift length (D)

In order to investigate the turn-on behaviors of the SiC HV-SCR structures, the TLP voltage waveforms with an applied voltage pulse of 245 V and measured current of ~0.4 A were shown in Fig. 5.7. The turn-on time is defined as the time difference between the voltage changing from 10% of the peak value to V_h [30]. As shown in Fig. 5.7, the voltage shows an overshoot. The peak voltage is ~40 V higher than the trigger voltage. Meanwhile, the turn-on times of the HV-SCR with drift length of 7 μm and 11 μm are 33 ns and 42 ns, respectively.

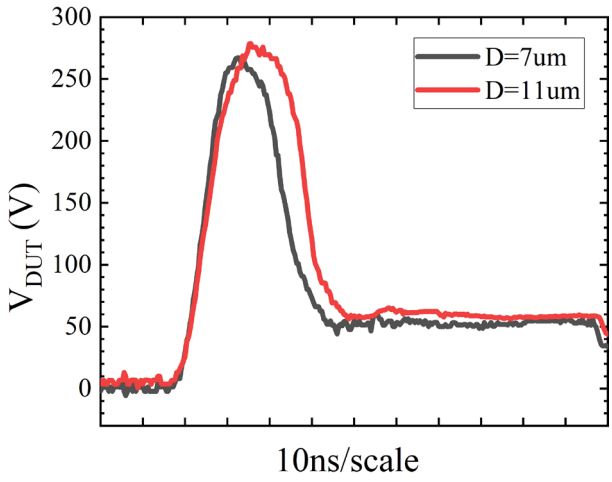


Fig. 5.7 TLP voltage waveforms of SiC HV-SCR with varying drift length (D)

For gate-controlled devices (e.g., NMOS, LDMOS and gate-controlled SCR), the ESD behaviors are related to the gate bias voltage [15], [31], [32]. To further investigate the SiC HV-SCR, 500 Ω TLP measurements with different gate bias (V_g) were carried out. The TLP measurement results of the HV-SCR with 4 µm gate length, 7 µm drift length and varying V_g are shown in Fig. 5.8. V_h shows minor dependence on V_g. V_{t1} shows a slight decrease (i.e., from ~230 V to 220 V) when V_g increases from 0 V to 15 V.

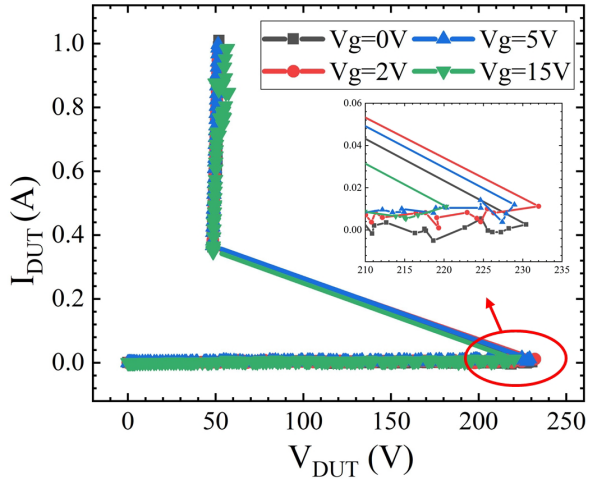


Fig. 5.8 SiC HV-SCR TLP measurement results with varying gate bias (V_g)

5.4 Simulation results and discussion

5.4.1 Operational Mechanism

In order to further understand the operational mechanisms of the SiC devices, the HV-SCR and LDMOS were simulated in Sentaurus TCAD software (from Synopsis). Both SiC LDMOS and HV-SCR were built by Sentaurus SProcess. Monte-Carlo-based ion implantation was performed to form the N-well, P-well, N+ and P+ regions. The ion implantation profiles were extracted from the real process. The gate length and drift length of the simulated SiC HV-SCR are 4 μm and 7 μm, and the gate length and drift length of the simulated SiC LDMOS are 3 μm and 4 μm. Transient-based ESD simulations were performed by Sentaurus SDevice to extract the current density distribution of the SiC devices.

The TCAD-simulated ESD current density distribution of the HV-SCR at the device trigger is shown in Fig. 5.9(a). It can be observed that most of the ESD current flows through the P+ region (i.e., anode), N-well, P-well and N+ region (i.e., cathode). After the anode voltage reaches the avalanche breakdown voltage of the N-well and P-well junction, the ESD current flows into the P-well and N-well, turning on the bipolar transistors (i.e., lateral NPN and vertical PNP). The ESD current density distribution of the SiC HV-SCR after trigger can be found in Fig. 5.9(b). The ESD current is discharged by two paths (i.e., lateral NPN and vertical PNP), which prevents the current from crowding in a certain region. This allows the device to endure higher ESD current. The ESD current density distribution of the SiC LDMOS at trigger is shown in Fig. 5.9(c). Most of the current is at the surface of the N-well. Fig. 5.9(d) shows the ESD current density distribution of the SiC LDMOS after trigger. Compared with the HV-SCR, the current is collecting on the surface of the LDMOS device, especially at the P-well and N-well regions. This leads to the current crowding, making the devices more easily damaged at low ESD current.

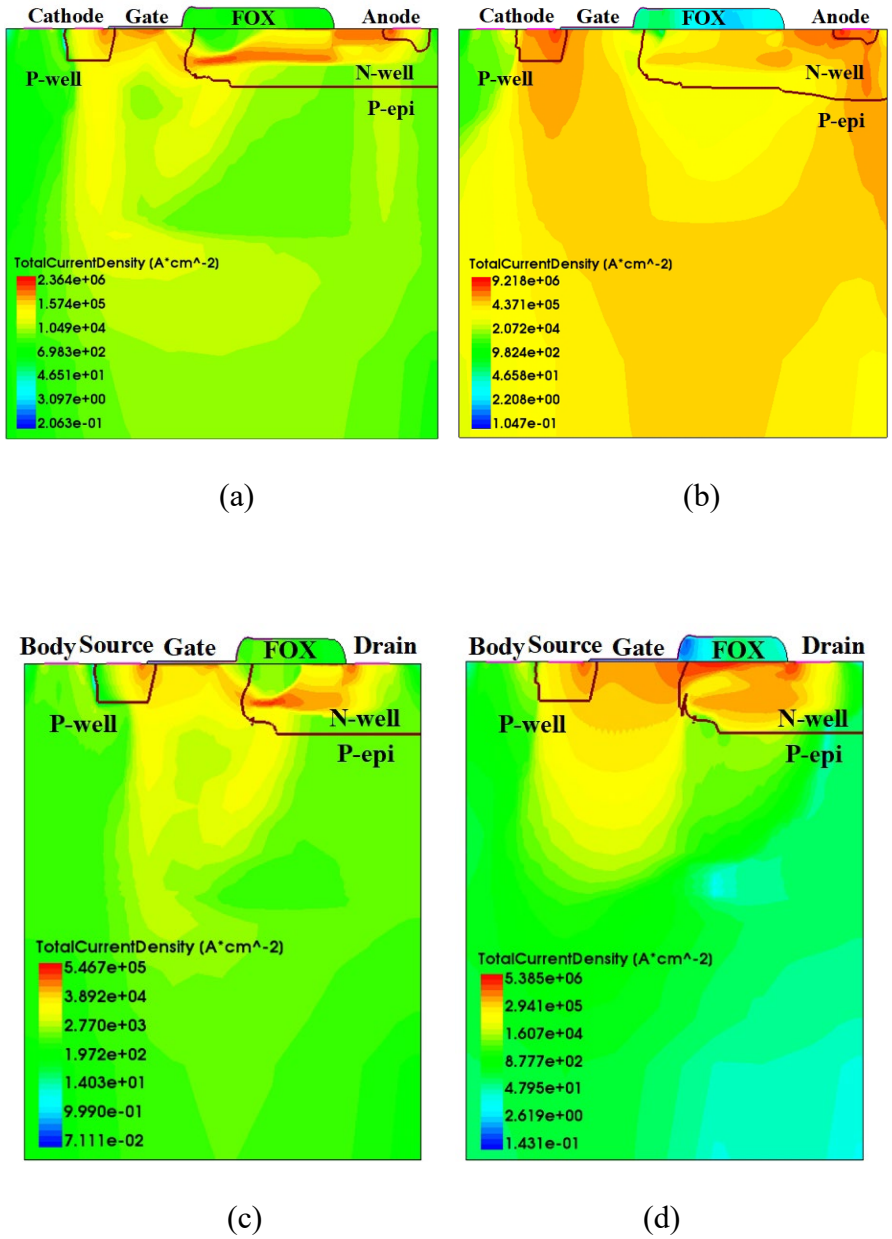


Fig. 5.9 TCAD simulated ESD current density distribution of (a) SiC HV-SCR at trigger, (b) SiC HV-SCR after trigger, (c) SiC LDMOS at trigger and (d) SiC LDMOS after trigger

5.4.2 SiC HV-SCR Holding Voltage

The equivalent circuit of the SiC HV-SCR is shown in Fig. 5.10 to help analyze its V_h. The HV-SCR is formed by the lateral NPN and vertical PNP bipolar transistors. R_{NW}, R_{drift}, R_{epi} and

R_{PW} are the parasitic resistors of the N-well, drift region, P-epitaxial layer and P-well, respectively. The V_h of the HV-SCR can be expressed as [33]:

$$V_h = V_{CEP(sat)} + V_{epi} + V_{BEN} \tag{2}$$

Where $V_{CEP(sat)}$ is PNP emitter-collector voltage drop at saturation region, V_{epi} is the voltage drop at P-epitaxial layer, and V_{BEN} is the NPN base-emitter voltage drop. Assuming the current gains of the NPN and PNP bipolar transistors are much greater than 1, (2) can be written as [34], [35]:

$$V_h = V_{CEP(sat)} + V_{BEN}(1 + R_{epi}/R_{PW}) \tag{3}$$

The V_h of HV-SCR is determined by $V_{CEP(sat)}$, V_{BEN} and the ratio of R_{epi} and R_{PW}. The ratio of R_{epi} and R_{PW} can be expressed as:

$$\frac{R_{epi}}{R_{PW}} = \frac{\rho_{epi}/t_{epi}}{\rho_{PW}/t_{PW}} \tag{4}$$

Where ρ_{epi} and ρ_{PW} are the resistivities of the epitaxy layer and P-well, and t_{epi} and t_{PW} are the thickness of the epitaxy layer and P-well. The resistivity for a P-type semiconductor layer is:

$$\rho = 1/q\mu_p p \tag{5}$$

Where μ_p and p are hole mobility and hole doping concentration. TABLE I lists the values of doping concentration, mobility and thickness. The doping concentration and thickness values were extracted by secondary ion mass spectrometry (SIMS) analysis, while the mobility values were extracted from Ref [36]. Substituting the values into (4) and (5), the ratio of R_{epi} and R_{PW} is 17.94.

The NPN base-emitter voltage drop, V_{BEN}, is the forward bias voltage drop of the P-well and N+ junction, which is approximately the built-in potential of the PN junction and can be expressed as:

$$V_{BEN} = \frac{kT}{q} \ln\left(\frac{N_{PW}N_{N+}}{n_i^2}\right) \tag{6}$$

Where N_{N+} is the doping concentration of the N+ region, and n_i is the intrinsic carrier concentration. According to Ref [36], the intrinsic carrier concentration of 4H-SiC at 25ºC is ~5E-5 cm^{-3}. Thus, V_{BEN} is ~2.7 V. Since $V_{CEP(sat)}$ is in the same order as V_{BEN} during SCR operation [33], it can be neglected in (3). As a result, combining (3) to (6), the value of the holding voltage, V_h, is ~51 V, which is closed to the experimental results. It should be noted that the built-in potential of SiC devices (i.e., ~2.7 V) is ~4 times higher than Si devices (i.e., ~0.7 V). Therefore, the SiC HV-SCR shows higher V_h when compared with Si-based SCR [37].

Table 5.1 Extracted doping concentration, mobility and thickness

Regions	Doping concentration (cm^{-3})	Mobility ($cm^2/V\cdot s$)	Thickness (µm)
N+	3E19		
N-well	1E17	599	
P-well	1E17	105	1
P-epi	1E15	117	5

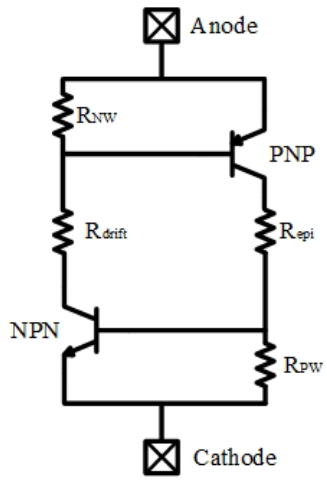
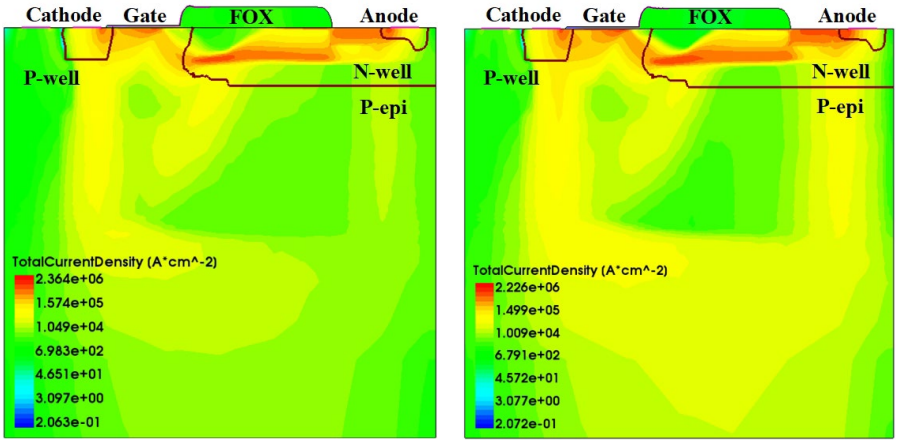


Fig. 5.10 Equivalent circuit of the SiC HV-SCR

5.4.3 SiC HV-SCR with Gate Bias

Typically, V_{t1} of the gate-controlled devices is strongly affected by the gate bias [15]. However, as shown in Fig. 5.7, V_{t1} of the SiC HV-SCR only shows a slight change when V_g increases from 0 V to 15 V. This may be due to the high V_{th} and thick field oxide of the devices [38]. Fig. 5.11(a) to (f) show the current density distribution and electric field distribution of the SiC HV-SCR at trigger point with 0 V, 5 V and 15 V gate bias. The thickness of the field oxide (FOX) is 500 nm, and the thickness of the gate oxide is 50 nm. As the V_{th} of the device is ~5 V, the electron current accumulated on the surface of the device is not sufficient to help the device trigger when V_g is lower than 5 V. When V_g is 0 V, the current does not accumulate below the FOX region (Fig. 5.11a). No apparent difference is observed when V_g increases to 5 V (Fig. 5.11b). When V_g increases from 0 V to 15 V (Fig. 5.11c), the current density below the gate region increases from ~2E6 A/cm^2 to ~4.5E6 A/cm^2. The increase of current helps the turn-on of the lateral NPN transistor and reduces V_{t1}. As shown in Fig. 5.11(d), the maximum electric field locates in the FOX region. For V_g=5 V and 15 V, the location of the maximum electric field does not alter when compared with V_g=0 V (Fig. 5.11e and f). Therefore, the current density only shows a slight increase, and the considerable change of V_{t1} is not observed.



(a) (b)

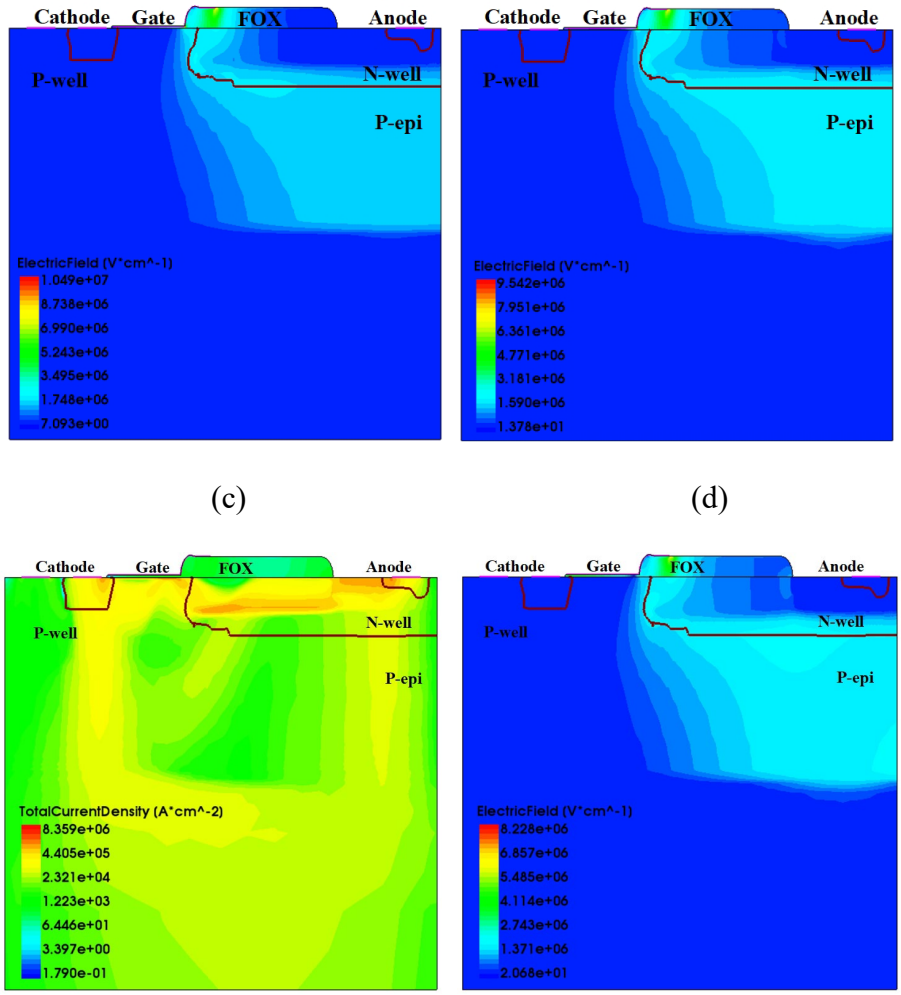


Fig. 5.11 TCAD simulated (a) current density distribution at V_g=0 V, (b) current density distribution at V_g=5 V, (c) current density distribution at V_g=15 V, (d) electric field distribution at V_g=0 V, (e) electric field distribution at V_g=5 V, and (f) electric field distribution at V_g=15 V of the SiC HV-SCR at trigger point

5.4.4 SiC HV-SCR Turn-on Behaviors

The turn-on time of the HV-SCR consists of delay time (t_d) and rise time (t_r) [30], [39]. The delay time (t_d) is the sum of base transit times of the parasitic NPN and PNP. The rise time is the

time that carriers need to charge the NPN base-emitter capacitor, which is mainly determined by the device structure and geometry [30]. Therefore, turn-on time can be expressed as

$$t_{on} = \tau_n + \tau_p + t_r \tag{7}$$

Where τ_n and τ_p are base transit times of the parasitic NPN and PNP, which can be expressed as [30], [39]

$$\tau_n = \frac{W_{BN}^2}{2D_n} \tag{8}$$

$$\tau_p = \frac{W_{BP}^2}{2D_p} \tag{9}$$

Where W_{BN} and W_{BP} are the base width of NPN and PNP, and D_n and D_p are the diffusion coefficients of electrons and holes.

According to the Einstein relationship, the diffusion coefficients can be expressed as:

$$\frac{D_{n\,(p)}}{\mu_{n\,(p)}} = \frac{kT}{q} \tag{10}$$

Where $\mu_{n(p)}$ is the electron (hole) mobility. The electron mobility of the N-well and hole mobility of the P-well are listed in TABLE I. Substituting μ_n and μ_p into (10), D_n and D_p are 15.57 cm^2/s and 2.73 cm^2/s, respectively. Then τ_n and τ_p are 5.13 ns and 1.83 ns, with the W_{BN} and W_{BP} being 4 µm (i.e., gate length) and 1 µm (i.e., P-well thickness). Since the turn-on times of the SiC HV-SCR with D=7 µm and 11 µm are 33 ns and 42 ns, the turn-on time is dominated by the rise time. In addition, comparing the SiC HV-SCR with Si-based SCR [30], [39], [40], although its base transit times are higher due to the low diffusion coefficients of SiC, its longer turn-on time is mainly caused by the geometry.

5.5 Conclusion

This paper presents the ESD behaviors of SiC-based LDMOS and HV-SCR structures. The structures were fabricated in a 4H-SiC BCD process and characterized using a TLP system. The

TLP measurement results show that the drift length slightly affects the V_{t1} of the LDMOS, while it has limited impacts on the V_{t1} of the HV-SCR. In addition, the SiC LDMOS and HV-SCR structures were characterized by the TLP system with 500 Ω impedance to obtain V_h and I_{t2}. Relatively high I_{t2} per µm (i.e., 33 mA/µm) was observed on the HV-SCR structures, which is much higher than that of the SiC LDMOS structure (i.e., 0.2 mA/µm). TCAD simulations show that the majority of the ESD current in the HV-SCR is discharged by the lateral NPN and vertical PNP, which prevents the current from crowding in a certain region. The ESD current in the LDMOS collects on the device surface, making the devices more easily damaged at lower ESD current. Meanwhile, the V_h of the HV-SCR is ~48 V and shows little change when the drift length varies from 7 µm to 11 µm. The V_h of the SiC HV-SCR is mainly determined by the base-emitter voltage drop of the parasitic NPN and the parasitic resistance of the P-well and P-epitaxial layer. The SiC HV-SCR shows higher V_h when compared to Si-based SCR due to its relatively higher built-in potential in the PN junction. The TLP voltage waveforms of the SiC HV-SCR are presented to investigate their turn-on behaviors. The turn-on time of the HV-SCR increases from 33 ns to 42 ns with the drift length varying from 7 µm to 11 µm. The turn-on time is dominated by the rise time of the HV-SCR, which mainly depends on the device structure and geometry. The HV-SCR structures with varying V_g were also characterized by the 500 Ω TLP system. V_{t1} changes from 230 V to 220 V when V_g increases from 0 V to 15 V. The current density distribution and electric field of the HV-SCR with varying V_g were simulated to analyze the TLP results.

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5.7 Reference

[1] S. Ji, Z. Zhang, F. Wang, "Overview of high voltage SiC power semiconductor devices: development and application", *CES Transactions on Electrical Machines and Systems*, vol. 1, no. 3, pp. 254-264, September 2017, doi: 10.23919/TEMS.2017.8086104.

[2] S. Roy, A. U. Rashid, A. Abbasi, R. C. Murphree, M. M.. Hossain, A. Faruque, A. Metreveli, C,-M. Zetterling, J. Fraley, B. Sparkman, and H. A. Mantooth, "Silicon Carbide Bipolar Analog Circuits for Extreme Temperature Signal Conditioning", *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3764-3770, Sept. 2019, doi: 10.1109/TED.2019.2928484.

[3] A. Abbasi, R. Murphree, S. Roy, M. Suggs, J. Fraley, H. A. Mantooth, J. Di, and T. Erlbacher, "High Temperature Memory Design, Implementation, and Characterization in 1μm SiC CMOS Technology", *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2019, No. HiTen, pp. 11-15, July 2019, doi: https://doi.org/10.4071/2380-4491.2019.HiTen.000011.

[4] M. Barlow, S. Ahmed, H. A. Mantooth, A. M. Francis, "An integrated SiC CMOS gate driver", *Proc. Conf. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 1646-1649, May 2016, doi: 10.1109/APEC.2016.7468087, doi: 10.1109/APEC.2016.7468087.

[5] S. Roy, R. C. Murphree, A. Abbasi, A, Rahman, S. Ahmed, J. A. Gattis, A. M. Francis, J. Holmes, and H. A. Mantooth, "A SiC CMOS digitally controlled PWM generator for high-temperature applications", *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8364-8372, Oct. 2017, doi: 10.1109/TIE.2017.2694413.

[6] J. Hornberger, A.B. Lostetter, K.J. Olejniczak, T. McNutt, S. Magan Lal, A. Mantooth, "Silicon-Carbide (SiC) Semiconductor Power Electronics for Extreme High-Temperature Environments", *2004 IEEE Aerospace Conference*, vol. 4, pp. 2538-2555, 6–13 Mar 2004, doi: 10.1109/AERO.2004.1368048.

[7] H. A. Mantooth, M. D. Glover, P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, pp. 374-385, 2014, doi: 10.1109/JESTPE.2014.2313511.

[8] A. Rahman, L. Caley, S. Roy, N. Kuhns, A. Mantooth, J. Di, A. M. Francis, J. Holmes, "High temperature data converters in silicon carbide CMOS", *IEEE Transactions on Electron Devices*, vol. 64, no. 4, pp. 1426-1432, Apr. 2017, doi: 10.1109/TED.2017.2665520.

[9] H. Elahipanah, S. Kargarrazi, A. Salemi, M. Östling, C.-M. Zetterling, "500 °C high current 4H-SiC lateral BJTs for high-temperature integrated circuits", *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1429-1432, Oct. 2017, doi: 10.1109/LED.2017.2737558.

[10] P. G. Neudeck, G. M. Beheim, C. S. Salupo, "600ºC logic gates using silicon carbide JFETs", *Proc. Government Microcircuit Applications Conf.*, pp. 421-424, 2000.

[11] N. Kuhns, L . Caley, A. Rahman, A. Ahmed, J. Di, H. A. Mantooth, A. M. Francis, and J. Holmes, "Complex High-Temperature CMOS Silicon Carbide Digital Circuit Designs", *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 105-111, June 2016, doi: 10.1109/TDMR.2016.2530664.

[12] L. D. Benedetto, G. D. Licciardo, A. Rubino, "Experimental results on lateral 4H-SiC UV photodiodes", *Proc. 7th IEEE Int. Workshop Adv. Sensors Interfaces (IWASI)*, pp. 252-254, Jun. 2017, doi: 10.1109/IWASI.2017.7974264.

[13] R. G. Wagner, J. M. Soden, C. F. Hawkins, "Extent and cost of EOS/ESD damage in an IC manufacturing process", *Proc. EOS/ESD Symp.*, vol. EOS-15, pp. 49-55, Sept. 1993.

[14] K.-I. Do, B.-S. Lee, Y.-S. Koo, "Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications", *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 283-286, Feb. 2019, doi: 10.1109/LED.2018.2885846.

[15] D.T. Jarard, S. Ahmed, T. Vrotsos, Z. Chen, "Electrical safe operating area of low-voltage silicon carbide NMOS transistors", *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 7-9 Nov. 2016, doi: 10.1109/WiPDA.2016.7799945.

[16] A. Amerasekera, C. Duvvury, ESD in Silicon Integrated Circuits, New York:Wiley, 1995, doi: 10.1016/s0026-2714(96)90047-5.

[17] Z. Qi, M. Qiao, L. Liang, F. Zhang, X. Zhou, S. Cheng, S. Zhang, F. Lin, G. Sun, Z. Li, and B. Zhang, "Novel Silicon-Controlled Rectifier With Snapback-Free Performance for High-Voltage and Robust ESD Protection", *IEEE Electron Device Letters*, vol. 40, no. 3, pp. 435-438, Mar. 2019, doi: 10.1109/LED.2019.2894646.

[18] J. Zeng, S. Dong, J. J. Liou, Y. Han, L. Zhong, W. Wang, "Design and analysis of an area-efficient high holding voltage ESD protection device", *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 606-614, Feb. 2015, doi: 10.1109/TED.2014.2381511.

[19] J. Guan, Y. Wang, S. Hao, Y. Zheng, X. Jin, "A novel high holding voltage dual-direction SCR with embedded structure for HV ESD protection", *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1716-1719, Dec. 2017, doi: 10.1109/LED.2017.2766686.

[20] J. Weisse, H. Mitlehner, L. Frey, and T. Erlbacher, "Design of a 4H-SiC RESURF N-LDMOS Transistor for High Voltage Integrated Circuits", Materials Science Forum, vol. 963, pp. 629-32, July 2019, doi: https://doi.org/10.4028/www.scientific.net/MSF.963.629.

[21] M. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis and compact modeling of 40V-LDMOS power devices under ESD stress conditions", *Proc. 21st EOS/ESD Symp.*, pp. 1-10, 1999, doi: 10.1109/EOSESD.1999.818983.

[22] W.-J. Chang, and M.-D. Ker, "The impact of drift implant and layout parameters on ESD robustness for on-chip ESD protection devices in 40-V CMOS technology", *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 2, pp. 324-332, Jun. 2007, doi: 10.1109/TDMR.2007.901185.

[23] E. Grund, "Snapback device studies using multilevel TLP and multi-impedance TLP testers," 2005 Electrical Overstress/Electrostatic Discharge Symposium, Tucson, AZ, 2005, pp. 1-9.

[24] E. Grund and R. Gauthier, "TLP systems with combined 50 and 500-ohm impedance probes and kelvin probes," 2003 Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, NV, 2003, pp. 1-10.

[25] F. Ma B. Zhang, Y. Han, J. Zheng, B. Song, S. Dong, and H. Liang, "High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique", *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1178-1180, Sep. 2013, doi: 10.1109/LED.2013.2272591.

[26] S. Dong, H. Jin, M. Miao, J. Wu, J. J. Liou, "Novel capacitance coupling complementary dual-direction SCR for high-voltage ESD", *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 640-642, May 2012, doi: 10.1109/LED.2012.2188015.

[27] J. Lee, M. Prabhu and M. I. Natarajan, "Engineering ESD Robust LDMOS SCR Devices in FinFET Technology", in IEEE Electron Device Letters, vol. 39, no. 7, pp. 1011-1013, July 2018, doi: 10.1109/LED.2018.2838760.

[28] Jian-Hsing Lee et al., "Novel ESD protection structure with embedded SCR LDMOS for smart power technology", 2002 IEEE International Reliability Physics Symposium.

Proceedings. 40th Annual (Cat. No.02CH37320), Dallas, TX, USA, 2002, pp. 156-161, doi: 10.1109/RELPHY.2002.996629.

[29] Y. Liu, W. Yang, A. Zhou and X. L. Jin, "Design fabrication and test of novel LDMOS-SCR for improving holding voltage", Solid-State Electron., vol. 103, pp. 122-126, Jan. 2015, doi: https://doi.org/10.1016/j.sse.2014.08.007.

[30] J. D. Sarro, K. Chatty, R. Gauthier and E. Rosenbaum, "Study of Design Factors Affecting Turn-on Time of Silicon Controlled Rectifiers (SCRS) in 90 and 65nm Bulk CMOS Technologies", *IEEE International Reliability Physics Symposium Proceedings*, 2006, doi: 10.1109/RELPHY.2006.251210.

[31] Z. Chen, A. Salman, G. Mathur and G. Boselli, "Design and optimization on ESD self-protection schemes for 700V LDMOS in high voltage power IC", 2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Reno, NV, 2015, pp. 1-6, doi: 10.1109/EOSESD.2015.7314735.

[32] A. A. Salman, S. G. Beebe and M. M. Pelella, "Double well field effect diode: Lateral SCR-like device for ESD protection of I/Os in deep sub micron SOI", 2007 29th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Anaheim, CA, 2007, pp. 3A.4-1-3A.4-7, doi: 10.1109/EOSESD.2007.4401750.

[33] O. Semenov, H. Sarbishaei, and M. Sachdev, ESD Protection Device and Circuit Design for Advanced CMOS Technologies (Springer, 2008).

[34] Ming-Dou Ker and Zi-Ping Chen, "SCR device with dynamic holding voltage for on-chip ESD protection in a 0.25-/spl mu/m fully salicided CMOS process," in IEEE Transactions on Electron Devices, vol. 51, no. 10, pp. 1731-1734, Oct. 2004, doi: 10.1109/TED.2004.834904.

[35] Huang Xiaozong, Liu Fan and Liu Zhiwei, "A Holding Voltage Adjustment Technique of SCR for ESD Protection", 3rd International Conference on Intelligent Energy and Power Systems, pp. 72-76, April 2017.

[36] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications, Singapore: Wiley, 2014.

[37] K. -I. Do, J. -I. Won and Y. -S. Koo, "A 4H-SiC MOSFET-Based ESD Protection With Improved Snapback Characteristics for High-Voltage Applications," in IEEE Transactions on Power Electronics, vol. 36, no. 5, pp. 4921-4926, May 2021, doi: 10.1109/TPEL.2020.3032917.

[38] M. P. J. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker and W. Fichtner, "Analysis of lateral DMOS power devices under ESD stress conditions," in IEEE Transactions on Electron Devices, vol. 47, no. 11, pp. 2128-2137, Nov. 2000, doi: 10.1109/16.877175.

[39] J. Liu, Z. Liu, Z. Jia, and J.J. Liu, "A novel DTSCR with a variation lateral base doping structure to improve turn-on speed for ESD protection", *Journal of Semiconductors*, 2014.

[40] C. Russ, M. Mergens, K. Verhaege, J. Armer, P. Jozwiak, G. Kolluri, and L. Avery, "GGSCRs: GGNMOS triggered silicon controlled rectifiers for ESD protection in deep sub-micron CMOS processes," Proc. ESD/ESD Symp., pp. 22-31, Sept. 2001.

CHAPTER 6

VF-TLP CHARACTERIZATION ON SIC-BASED DEVICES

6.1 Introduction

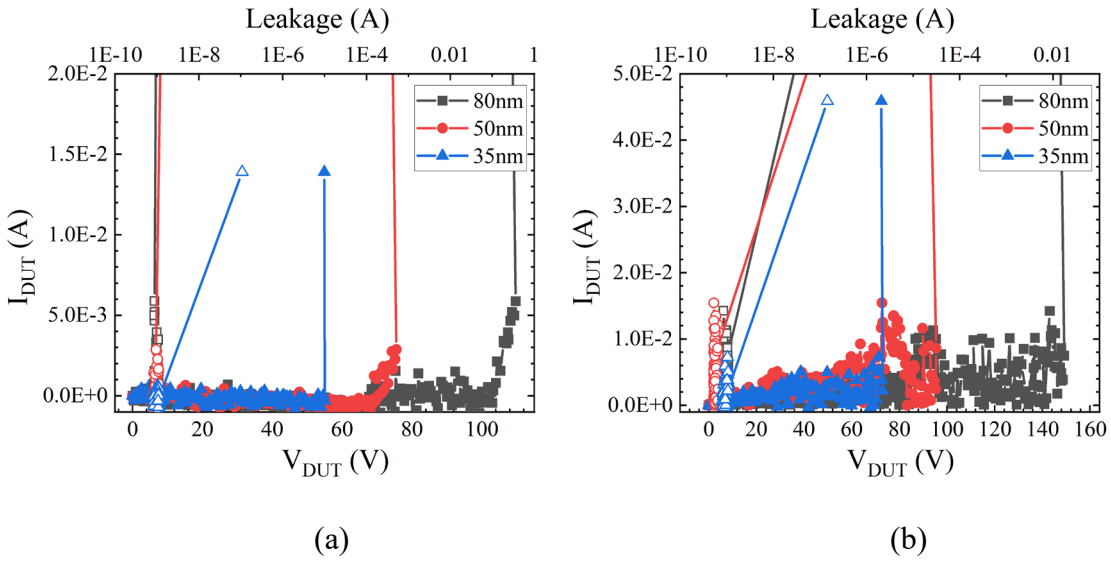
In Chapter 4 and 5, SiC-based ESD protection devices were characterized by a TLP system to investigate their area efficiency under human body model (HBM) ESD tresses. In this chapter, SiC-based devices are characterized by a very fast TLP (VF-TLP) system to investigate their performance under charged device model (CDM) ESD tresses. Additionally, although the SiC HV-SCR structures proposed in Chapter 5 show relatively high I_{t2} per μm, their V_{t1} is too high to protect low-voltage SiC CMOS devices. Therefore, a SiC-based low-voltage SCR (LV-SCR) structure is proposed in this chapter to achieve low V_{t1} of SiC ESD protection devices.

6.2 Experimental Results

6.2.1 VF-TLP measurement on SiC-based gate oxide

Gate oxide of MOS devices, such as CMOS and LDMOS, is very vulnerable to ESD tresses. Thus, the breakdown voltage (BV) of SiC-based gate oxide needs to be investigated for the design of ESD protection devices. Gate oxide breakdown under HBM and CDM ESD stresses can be estimated by TLP measurements with varying pulse widths. Fig. 6.1(a) and (b) show SiC-based NMOS gate oxide breakdown with varying oxide thickness. The pulse widths of TLP and VF-TLP are 100 ns and 10 ns, and the rise time of TLP and VF-TLP pulses are 10 ns and 100 ps. As shown in Fig. 6.1, gate oxide BV increases with the increase of oxide thickness. This is because the gate oxide electric field decreases with the increase of the oxide thickness (i.e., $E_{ox}=V_{ox}/t_{ox}$). Additionally, the gate oxide BV increases with the decrease of the pulse width. When the gate oxide is stressed by ESD, electrons and holes are injected into the oxide region, which generates defects. When the defect density reaches the critical trap density of the oxide, the oxide is bridged

by the defects and shows high leakage current (i.e., breakdown). Since more electrons and holes were injected during longer pulses, the gate oxide stressed by longer pulse widths shows lower BV.



(a) (b)

Fig. 6.1 SiC-based NMOS gate oxide breakdown measured by (a) TLP and (b) VF-TLP

6.2.2 VF-TLP measurement on SiC-based NMOS

Fig. 6.2 shows the TLP and very fast TLP (VF-TLP) measurement results of SiC NMOS devices. The width and gate length of the NMOS is 20 µm and 1 µm, respectively. The rise time and pulse width of the TLP measurement are 10 ns and 100 ns, and the rise time and pulse width of the VF-TLP measurement are 100 ps and 10 ns. The leakage current was measured at 5 V bias to monitor the failure point. As shown in Fig. 6.2, the I_{t2} of the SiC NMOS under VF-TLP (i.e., 74 mA) is much higher than that under TLP measurement (i.e., 31 mA). This is because the short pulses of VF-TLP generate less heat compared to TLP pulses. As a result, I_{t2} measured by the VF-TLP system is higher than that measured by the TLP system.

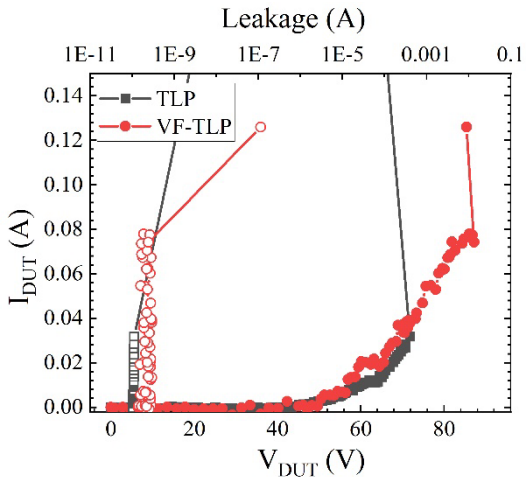


Fig. 6.2 TLP and VF-TLP measurement results of SiC-based NMOS

6.2.3 Characterization of SiC-based low-voltage SCR

The V_{t1} of the SiC HV-SCR proposed in Chapter 5 is ~230 V, which is much higher than the oxide BV (Fig. 6.1a). Therefore, a SiC LV-SCR structure was designed to achieve low V_{t1}. Fig. 6.3 shows the cross-section of the proposed SiC LV-SCR. An N+ region was implanted between the N-well and P-well to reduce the BV. LV-SCR structures with varying *L* and *D* were fabricated in a 4H-SiC CMOS process to control V_h of the devices.

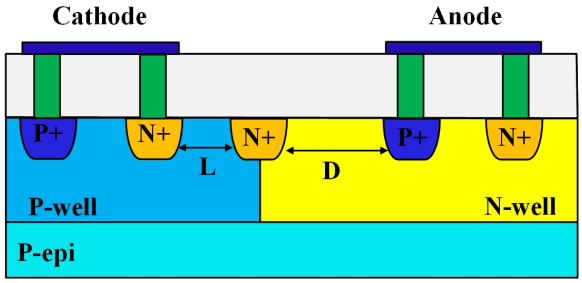
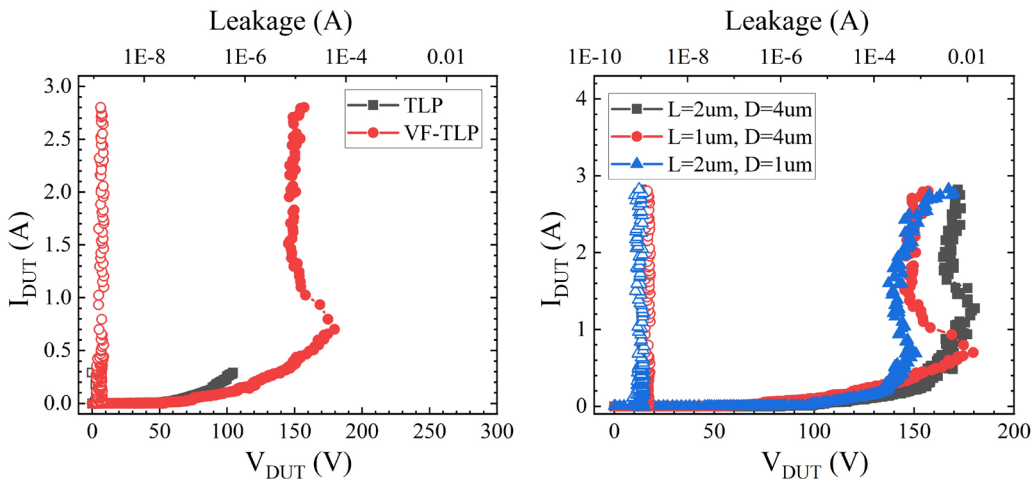


Fig. 6.3 Cross-section of SiC LV-SCR structure

Fig. 6.4(a) shows the TLP and VF-TLP measurement results of the SiC LV- SCR with 60 µm width, 1 µm *L* and 4 µm *D*. For TLP measurement, the SiC LVSCR did not survive before the turn-on of the parasitic PNP and showed early failure (i.e., I_{t2}=300 mA). For VF-TLP measurement, the parasitic PNP turns on at 175 V and forms a PNPN structure with the parasitic NPN. The turn-

on of the bipolar transistors generates a high current gain (i.e., $\beta_{SCR}=\beta_{NPN}\cdot\beta_{PNP}$), and a high failure current (i.e., 2.8 A) is observed. Fig. 6.4(b) shows the VF-TLP measurement results of the SiC LV-SCR with varying L and D. V_h increases with the increases of L and D as the current gain decreases.



(a) (b)

Fig. 6.4 SiC LV-SCR (a) TLP and VF-TLP measurement results and (b) VF-TLP measurement results with varying L and D

6.3 Conclusion

In this chapter, TLP and VF-TLP measurements were carried out on SiC-based gate oxide with varying thickness to characterize the BV under ESD stresses. SiC NMOS was also characterized by VF-TLP and showed higher I_{t2} than the TLP result due to the short pulse width of the VF-TLP measurement. In addition, a SiC LV-SCR structure was proposed to achieve low V_{t1}. Both TLP and VF-TLP measurements were conducted to investigate the ESD behaviors of the SiC LV-SCR. The SiC LV-SCR failed before its turn-on under TLP measurements. For VF-TLP measurements, the LV-SCR triggered at 175 V and failed at 2.8 A. Although the LV-SCR shows lower V_{t1} than

HV-SCR, its V_{t1} is still not promising for ESD protection of low-voltage CMOS devices. New low-voltage ESD protection devices will be designed in future work to achieve suitable V_{t1} and V_h.

CHAPTER 7

DEVELOPMENT OF LTCC-PACKAGED OPTOCOUPLERS AS OPTICAL GALVANIC ISOLATION FOR HIGH-TEMPERATURE APPLICATIONS

7.1 Abstract

This paper reports high-temperature optocouplers for signal galvanic isolation. Low temperature co-fired ceramic (LTCC) technology was used in the design and fabrication of the high-temperature optocoupler package. The optimal coupling behaviors, driving capabilities and response speed of the optocouplers were concentrated and investigated in this paper. Emitters and detectors with different emission and spectral wavelengths were studied to achieve optimal coupling behaviors. Relatively high coupling efficiency is achieved with emitters and detectors of emission and spectral wavelength in the red spectrum (i.e., 620 -750 nm), leading to higher current transfer ratios (CTR). To further enhance the electrical performance, optocouplers with multiple detectors in parallel were designed and fabricated. CTR, leakage current and response speed (i.e., propagation delay, rise time and fall time) of the optocouplers were characterized over a range of temperatures from 25˚C to 250˚C. The CTR degrades at high temperatures, while the leakage current and response speed show little degradation with varying temperatures. Furthermore, the behaviors of the optocouplers with varying temperatures are modeled and analyzed.

7.2 Introduction

The temperature tolerance of semiconductor devices and integrated circuits (ICs) is greatly improved due to the revolution of semiconductor materials (e.g., silicon carbide (SiC) and gallium nitride (GaN)) [1] and technique (e.g., silicon on insulator (SOI)) [2]. This allows power devices, mixed-signal circuits and control systems to be operated in high-temperature environments [3]-[5]. Since these applications involve high voltages, common-mode signals and fluctuating ground

potentials, galvanic isolation devices are required as a protection method [6]. For example, in power systems, galvanic isolation devices and circuits are required for the gate driver circuitry to isolate the low-voltage logic controllers from the high-voltage components [7], [8]. Among galvanic isolators, optocouplers, capacitors and transformers are commonly used [7]-[10]. Optocouplers provide a small packaging size, few connection components, low input drive currents and low power dissipation, making them more desirable than regular isolation transformers [8]. However, the performance degradation of optocouplers at elevated temperatures limits their applications in high-temperature environments [10]. Table 7.1 summarizes recently published optocouplers. Although some of them show high CTR, very few are capable of operating over 150ºC. Therefore, the design and fabrication of high-temperature optocouplers for galvanic isolation are highly desired.

Table 7.1 Recently published optocouplers

Reference	[11]	[12]	[13]	[14]	[15]
CTR	2	0.002	0.02	0.008	1.6
Temperature	25 ºC	25 ºC	25 ºC	25 ºC	125 ºC

A few studies on optoelectronic materials and devices for high-temperature applications were conducted and reported in recent years [16] –[21]. The spontaneous emission quantum efficiency (QE) of different light-emitting diode (LED) materials (i.e., indium-gallium-nitride-based (InGaN-based) multiple quantum wells (MQWs)) over a wide range of temperature was studied using photoluminescence (PL) measurements [17]. The InGaN-based MQW structures exhibit minimum QE drop at temperatures higher than 200˚C. The study was extended to other LED materials as well to investigate the QE at high temperatures. A. Sabbar et al. [18] reported InGaN-based and

aluminum-gallium-indium-phosphide-based (AlGaInP-based) MQW structures with different peak wavelength (i.e., 450 nm, 470 nm and 630 nm) for high-temperature optoelectronic applications. Moreover, further optimization into InGaN-based structures was proposed to enhance their behaviors at high temperatures, and relatively high QE at high temperatures (i.e., >200˚C) is observed [19]. The temperature and injected current-dependent internal quantum efficiency (IQE) of InGaN-based MQW LEDs with different peak wavelengths (i.e., 450 nm, 470 nm and 530 nm) were studied using electroluminescence (EL) measurements [15]. Stable peak IQE of these LEDs at high temperatures was reported. These studies [17]-[20] prove that AlGaN-based and AlGaInP-based MQW structures can be utilized to form LED devices in high-temperature optoelectronic applications. In addition, the spectral responsivity (SR) of InGaN-based MQW structures was investigated with the temperature range of -200˚C to 500˚C [21]. The results indicate that the photodiodes can be used in high-temperature optocouplers. Although systematic studies of the optoelectronic devices for high-temperature applications were carried out, the LEDs and photodiodes were investigated individually. The high-temperature optical coupling behavior of the LEDs and photodiodes is not yet investigated. Therefore, high-temperature optocouplers, which integrate LEDs as emitters and photodiodes as detectors, need further studies.

In this paper, we report high-temperature optocouplers for optical galvanic isolation, which are capable of operating at 250˚C. The design was focused on the investigation and optimization of driving capability and response speed. Commercial high-temperature LEDs, which were studied in previous work[17-21], are used as emitters and detectors in the optocouplers to investigate their optical coupling behaviors. Low temperature co-fired ceramic (LTCC) was utilized for the packaging of the optical isolator. The multilayer fabrication process of the LTCC process allows for easiness to create cavities for light to travel. In addition, LTCC allows for temperature stability

and guarantees functionality to temperatures higher than conventional package technologies. The current transfer ratio (CTR), leakage current, propagation delay, rise time and fall time of the LTCC-based high-temperature optocouplers are measured over a range of temperatures from 25˚C to 250˚C. Device modeling is also provided to illustrate the behaviors of the optocouplers with varying temperatures.

7.3 Device Packaging and Fabrication

Optocouplers are preferred to isolation transformers because they can provide galvanic isolation with a significantly reduced form factor and weight. Optocouplers often use dual in-line package (DIP), surface-mount technology (SMT) and small-outline package (SOP) types of packages [22], [23]. These packages are normally made with epoxy-based materials, which do not endure wide temperature variations [24]. LTCC, on the other hand, is capable of withstanding an electrical operating temperature higher than 400˚C after firing [25], which makes LTCC a promising packaging material for high-temperature applications. Moreover, LTCC technology utilizes a multilayer fabrication process, which allows for creating vias interconnect, cavities, and embedded traces. This makes the LTCC-based devices easy to be integrated with electrical circuits and systems, such as gate driver circuits and power modules. The fabrication for thick film ceramics, such as LTCC, has been successfully mastered in the High-Density Electronic Center (HiDEC) at the University of Arkansas [26]. This has increased the motivation for evaluating LTCC as a substrate or housing material for electronic devices. Table 7.2 shows a material composition comparison for common ceramics that are used for electronic housing, including LTCC. When comparing the different ceramics, temperature functionality, feasibility for tooling, mechanical strength, coefficient of thermal expansion (CTE) and other aspects must be considered. Even though other ceramics such as aluminum oxide (Al_2O_3) and silicon nitride (Si_3N_4) tend to be

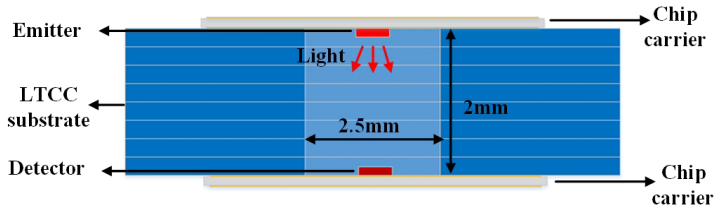
cheaper, extra process to achieve metal plating significantly increases the ceramic prize. In addition, AlN, Al_2O_3 and Si_3N_4 required a laser process to create the channel for the light to travel, which increases the risk of ceramic cracking. From this point of view, LTCC has a much greater advantage since its cavity is formed during ceramic fabrication. Therefore, an LTCC-based package was designed to encapsulate the emitters and detectors.

Table 7.2 Ceramic Material Comparison

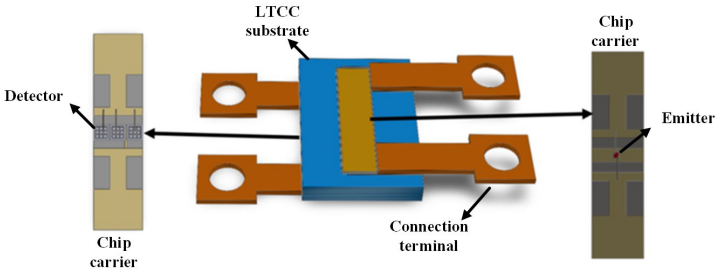
Material	AlN	Al_2O_3	Si_3N_4	LTCC (DuPont™ 951 Green Tape™)
Thermal Conductivity (W/mK)	180	18	30	4.6
CTE (ppm)	4.5	18	3.3	5.8
Elastic Strength (MPa)	330	300	310	230
Dielectric Strength kV/mm	17	14.6	14	7.8
Tooling (Cavity formation)		Laser grooving		Embedded in fabrication

Figure 7.1(a) and (b) show the cross-sectional view and three-dimensional (3D) view of the LTCC-based high-temperature optocoupler. The package of the optocoupler consists of an LTCC-based substrate to support two chip carriers. The chip carriers, which are made by AlN-based gold-plated direct bonded copper (DBC), are utilized to hold the emitters and detectors and attached facing each other to the LTCC-based substrate (Fig. 7.1a). This allows for a free space transmission between the emitters and the detectors. After the emitters and detectors were encapsulated, copper

leads were attached to the LTCC substrate as the connection terminals (Fig 7.1b). It should be noted that the connection terminals are designed only for standalone optocoupler measurements and not to be integrated into application circuits.



(a)

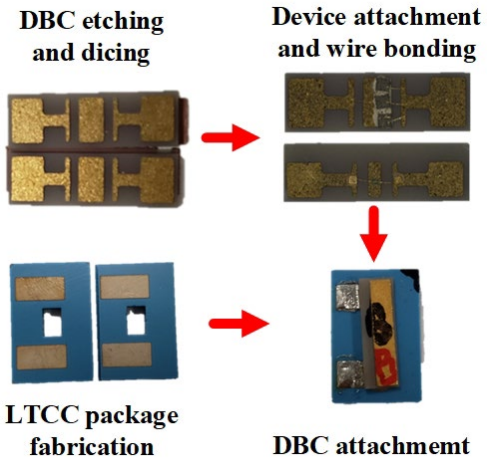


(b)

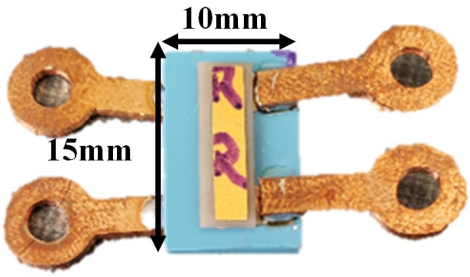
Fig. 7.1 (a) Cross-sectional view and (b) 3D model view of the LTCC-based high-temperature optocoupler

Figure 7.2(a) shows the detailed fabrication flow of the LTCC-based high-temperature optocoupler. The LTCC packages and AlN-based gold-plated DBC were fabricated. The DBC was etched with a chemical solution to form a connection pattern and diced into pieces as chip carriers. The devices were attached to the middle section of the DBC pattern, and wire-bonding was performed to connect the device anode and cathode to DBC pads. After the wire bonding, the chip carriers are attached facing each other in the LTCC-based substrate by using high-temperature conductive epoxy (i.e., CW2400 by Chemtronics). The epoxy, which has a dropping point of 343ºC, provides a close sealing between chip carriers and packages, limiting the light from escaping. In addition, since the CTEs of AlN and LTCC substrate are closed (Table 7.2), the

package has high mechanical stability and better performance at elevated temperatures. Finally, copper leads were attached by high-temperature solder alloy (i.e., SAC305). The fabricated LTCC-based high-temperature optocoupler is shown in Fig. 7.2(b). The device has a length of 15 mm, width of 10 mm and thickness of 2 mm. InGaN-based, AlGaInP-based and aluminum-gallium-arsenide-based (AlGaAs-based) high-temperature commercial LEDs [27], [28] are utilized as the emitter and detector of the optocouplers since they are promising for the high-temperature optoelectronic device fabrications [17]-[21]. Table 7.3 shows the LED materials, peak wavelength, device dimensions and manufacturers of the LEDs that are packaged into the optocouplers. Optocouplers with different combinations of emitters and detectors were fabricated and characterized. The optocoupler samples were named based on emitter-detector combination, i.e., GD-BD stands for optocoupler sample with green for display as the emitter and blue for display as the detector. The fabricated optocouplers are shown in Table 7.4.



(a)



(b)

Fig. 7.2 LTCC-based high-temperature optocoupler (a) fabrication flow and (b) fabricated sample

Table 7.3 Materials, peak wavelength, dimensions and manufacturers of the LEDs that are packaged

Type of LEDs	LED Material	Peak wavelength	Bare die device Dimension	Manufacturer
Blue for light (BL)	Indium gallium nitride (InGaN)	450 nm	1345 µm × 800 µm	HC Semitek
Blue for display (BD)	Indium gallium nitride (InGaN)	470 nm	191 µm × 270 µm	HC Semitek
Green for display (GD)	Indium gallium nitride (InGaN)	530 nm	191 µm × 270 µm	HC Semitek
Red for display (RD)	Aluminum gallium indium phosphide (AlGaInP)	630 nm	300 µm × 300 µm	HC Semitek
OPC-6900-21 (OPC)	Aluminum gallium arsenide (AlGaAs)	700 nm	960 µm × 960 µm	Marktech

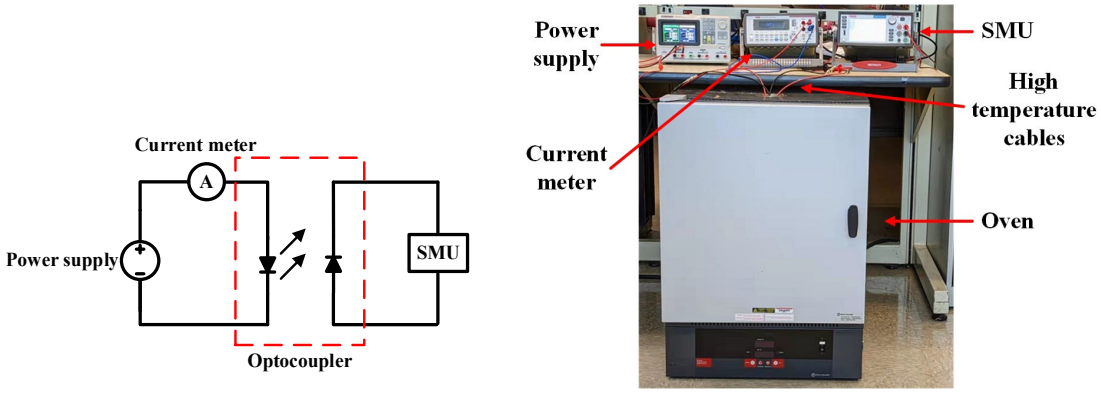
Table 7.4 Fabricated LTCC-based high-temperature optocouplers

Optocoupler	Emitter	Detector
BD-BD	Blue for display	Blue for display
BD-GD	Blue for display	Green for display
GD-GD	Green for display	Green for display
GD-BD	Green for display	Blue for display
GD-BL	Green for display	Blue for light
BL-GD	Blue for light	Green for display
RD-RD	Red for display	Red for display
RD-OPC	Red for display	OPC-6900-21

7.4 Experiments and Results

As a galvanic isolation device, an optocoupler needs to provide sufficient output current to drive the next-stage circuit, such as a transimpedance amplifier (TIA). To understand the output performance of fabricated LTCC-based optocouplers, the output current and the CTR of the optocouplers were characterized with varying temperatures from 25˚C to 250˚C. Fig. 7.3(a) and (b) show the schematic and experimental setup of the DC characterization for the LTCC-based high-temperature optocouplers. Siglent SPD3303X-E power supply is used to drive the emitter, and a current meter is used to measure the input current. Keithley 2450 source measure unit (SMU) is connected with the detector of the high-temperature optocoupler to measure its output current. The input current is controlled by changing the forward-bias voltage of the emitter and limited under the maximum forward current of the emitters (i.e., 30 mA). The optocouplers were characterized in Fisher Scientific 650-126 high-temperature oven to observe their performance

with different temperatures. High-temperature cables are used for the connection between the optocouplers and the measuring instruments.



(a) (b)

Fig. 7.3 (a) Schematic and (b) experimental setup for DC characteristics

In order to determine the optical coupling behaviors and the coupling efficiency of emitters and detectors, optocouplers with various types of emitters and detectors were characterized. Fig 7.4 shows the output current versus the input current of the optocouplers at 25˚C. The highest output current is observed on RD-OPC. The output current is 134 μA when the input current is 30 mA. This is mainly because the OPC has the largest device size (Table 7.2). RD-RD and BL-GD also show good matches. The output currents of RD-RD and BL-GD are 5.5 μA and 5 μA when the input current is 30 mA. Other optocouplers (i.e., BD-BD, BD-GD, GD-GD, GD-BD and GD-BL) show relatively low output current (i.e., lower than 0.5 μA). This indicates that they are not suitable combinations to form optocouplers.

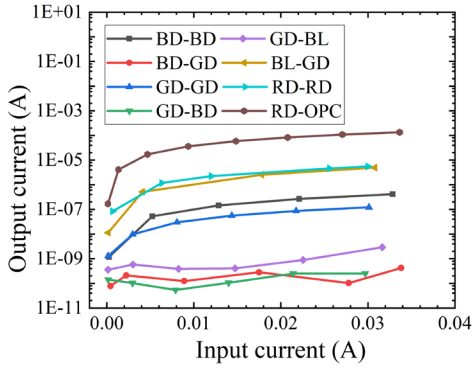


Fig. 7.4 Output current versus input current of optocuplers with various types of emitters and detectors

To further investigate the optical coupling behaviors of the emitters and detectors, the EL emission and SR measurements of the devices were carried out. The normalized EL emission and SR results are plotted together in Fig 7.5. The EL emission of RD is from 600 nm to 650 nm, and the SR of OPC is from 550 nm to 700 nm. Therefore, the optocoupler with RD as the emitter and OPC as the detector shows a good match and relatively high output current (Fig 7.4). As shown in Fig 7.5, RD-RD and BL-GD also have overlap regions on the EL emission and SR, which makes them suitable combinations for optocouplers.

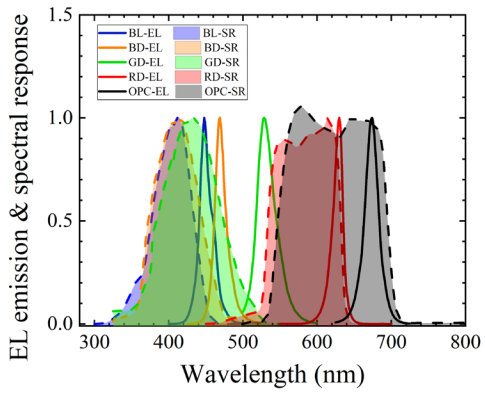


Fig. 7.5 EL emissions and spectral responses for various types of emitters and detectors

RD-OPC and RD-RD samples exhibited better optical coupling behaviors than other optocouplers (e.g., BD-BD, BD-GD and GD-GD). Although RD-OPC has an output current higher

than 100 μA, a higher output current is desired to drive external amplification circuits and achieve a better signal-to-noise ratio (SNR). The output current is strongly related to the total device area of detectors. Therefore, optocouplers with multiple detectors connected in parallel were fabricated to further enhance the output current. Table 7.5 summarizes the details of the fabricated optocoupler samples. The output current versus the input current of optocouplers with different numbers of parallel detectors is shown in Fig 7.6. Increasing the quantity of the detectors enables efficient accommodation of the emitter beam area leading to higher output current. RD-3OPC shows the output current of 337 μA when the input current is 30 mA, which is ~2.6 times higher than RD-OPC (i.e., 134 μA). RD-3RD shows the output current of ~24 μA when the input current is 30 mA.

Table 7.5 Emitter and detector of fabriacted optocoupler samples

Optocoupler	Emitter	Quantity of emitters in parallel	Detector	Quantity of detectors in parallel
RD-RD	RD	1	RD	1
RD-3RD	RD	1	RD	3
RD-OPC	RD	1	OPC	1
RD-3OPC	RD	1	OPC	3

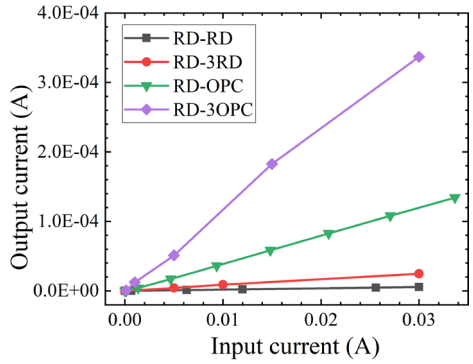


Fig. 7.6 Optocoupler output current versus input current at 25˚C with different quantity of detectors

High-temperature characterization of the optocouplers was conducted in a high-temperature oven (Fig. 3b). As the ambient temperature increases, the output current and the CTR degrades due to the drop in the EL intensity of the emitters [29]. Fig 7.7 shows the measured CTR of the optocouplers with temperatures ranging from 25˚C to 250˚C. A commercial optocoupler (IL300 by Vishay) [22] was also characterized to compare the thermal stability with the fabricated LTCC-based optocouplers. The RD-3OPC and the IL300 have similar CTR values at 25˚C (i.e., ~ 0.01). This indicates that the RD-3OPC has the potential to be operated as a galvanic isolation device. The CTRs of the optocouplers start to degrade when the temperature is over 100˚C.

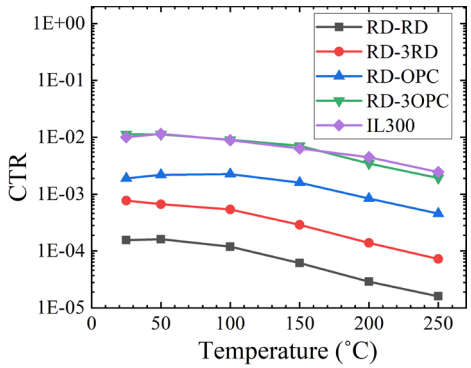


Fig. 7.7 CTR of optocouplers with varying temperatures

In real applications, optocouplers often operate with a small reverse bias voltage. The small reverse-bias voltage (e.g., -1 V) increases the depletion width of the detector, which improves the number of photons absorption and increases the photocurrent. However, the rise in temperature also increases the reverse-bias current (i.e., leakage current) of the detectors, which is attributed to the thermal ionization[21]. The increase in the leakage current elevates the dark current noise power of the detector and limits the SNR of the circuit [30]. Furthermore, the variation of the leakage current with temperature shifts the quiescent point (Q-point) of the next stage circuit, which may

cause mis-triggers. The leakage current of the optocouplers under -1 V bias was measured with varying temperatures and shown in Fig 7.8. It is observed that the commercial optocoupler IL300 shows a rapid increase in leakage current at temperatures above 100˚C. The leakage current of IL300 is ~100 μA at 250˚C, which is in the same magnitude as the photocurrent, indicating low SNR. The leakage current of RD-RD and RD-3RD does not show much variation with the increase of temperature. The leakage current of RD-RD and RD-3RD is ~0.5 nA at 250˚C. The leakage current of RD-3OPC increases from 10 nA at 25˚C to 600 nA at 250˚C. It should be noted that the photocurrent of RD-3OPC is ~50 μA at 250˚C, which is two orders of magnitude higher than the leakage current.

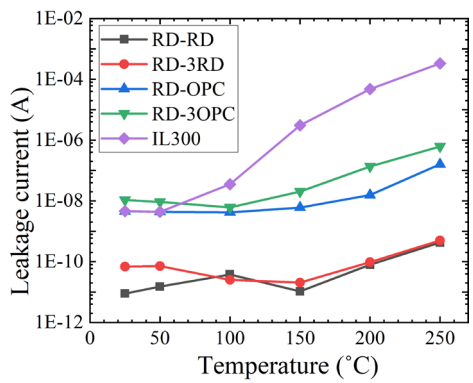


Fig. 7.8 Leakage current of optocouplers with varying temperatures

The response time (i.e., propagation delay, rise time and fall time) of the optocoupler determines its bandwidth. Thus, transient measurements of the optocouplers were conducted to characterize their propagation delay, rise time and fall time. Fig 7.9 shows the test circuit for transient characteristics of the optocouplers. A Rigol DG1022 function generator is used to generate the pulse-width modulation (PWM) signal for the optocouplers. A Tektronix TDS2012B oscilloscope is utilized to capture the output signals of the optocouplers. A 15 kΩ resistor (R_L) is connected to the cathode of the detector. To avoid the over-heating of the emitters at high

temperatures, the input current was limited at 20 mA with an input PWM voltage of 2.5 V. The optocouplers were measured at a reverse-bias voltage (V_b) of -1 V to improve the signal detection.

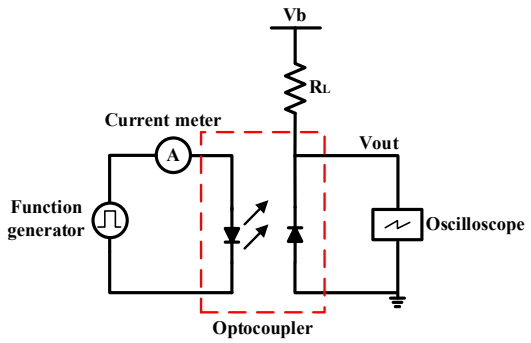
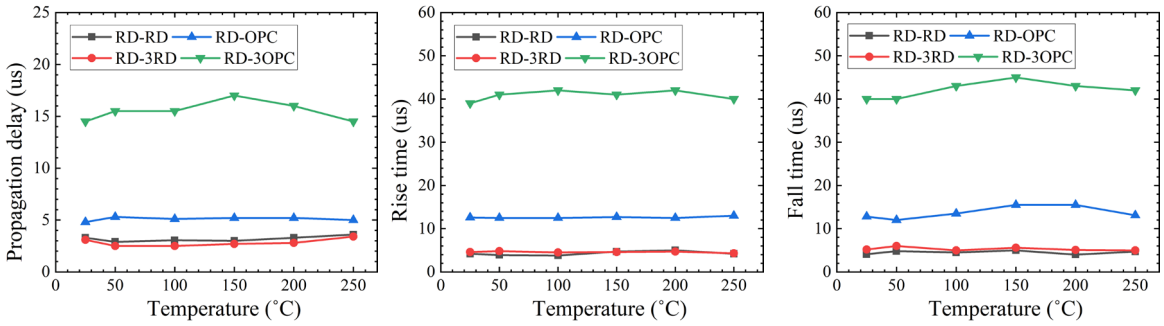


Fig. 7.9 Optocoupler test circuit for transient characteristics

The transient measurement results of four optocouplers with varying temperatures are shown in Fig 7.10. The propagation delay, rise time and fall time show low-temperature sensitivity when the temperature increases from 25˚C to 250˚C. The fall time of the optocouplers shows the same magnitude as the rise time (Fig. 7.10b and c). It is observed that the response time is steady when replacing one RD by three RDs (as the detector). Meanwhile, the response time of RD-3OPC is around three times higher than RD-OPC.



(a) (b) (c)

Fig. 7.10 Transient measurement results of optocouplers with varying temperatures: (a) propagation delay, (b) rise time, and (c) fall time

7.5 Discussion

It is observed that the performance of the LTCC-based optocouplers varies with temperatures. The CTR shows degradation when the temperature is higher than 100˚C. This is because the light output power, P, of the emitters drops at high-temperature conditions. Based on the power-law relationship, the light output power of the emitters is proportional to the integrated EL signal (L_{EL}) [29], [31]. The relationship can be described as:

$$L_{EL}(I_{in}, T) \propto P(I_{in}, T) \tag{1}$$

Where I_{in} is the input current of emitters, and T is the temperature.

For detectors, the relationship between the light input power (i.e., the light output power of the emitters) and the photocurrent (I_{ph}) is [32]:

$$R(\lambda, T) = \frac{I_{ph}}{P} \tag{2}$$

Where R is the responsivity of the detector, and λ is the wavelength of the light. Using (1) and (2), the relationship between the I_{in} and I_{ph} can be expressed as:

$$I_{ph} \propto R(\lambda, T)P(I_{in}, T) \tag{3}$$

The CTR of the optocouplers is defined as:

$$CTR = \frac{I_{out}}{I_{in}} \tag{4}$$

Where I_{out} is the output current of the detectors. As the leakage current of the detectors is three orders of magnitude lower than the photocurrent, the output current can be considered as the photocurrent (I_{out}=I_{ph}). Therefore, the normalized CTR with varying temperatures can be modeled based on (3) and (4).

Table 7.6 shows the normalized integrated EL signal, light wavelength and responsivity of RD-RD and RD-OPC. The results were extracted from previous research, and a detailed experimental setup was discussed [33], [34]. The normalized integrated EL signal was extracted at 300 μA

injected current. The peak wavelength of the samples (λ) increases with the temperature due to the bandgap narrowing effect[34]. The responsivity of the detector was extracted at the corresponding wavelength of the input light. Fig 7.11(a) and (b) show the normalized CTR with varying temperatures of RD-RD and RD-OPC, respectively. The CTR at 25 ˚C is set as the reference value (i.e., 100). The black line represents the modeled CTR based on (3) and (4), and the red line represents the experimental CTR. As shown in Fig. 7.11(a), the modeled CTR increases with temperature from -200˚C to -75˚C due to the increase of the responsivity. When the temperature is higher than 125˚C, the CTR drops rapidly due to the decrease of the integrated EL signal. The modeled CTR drops to 2.51 and 0.97 when the temperature is 325˚C and 425˚C, respectively. The CTR of RD-OPC increases when the temperature varies from -200˚C to 125˚C (Fig. 7.11b). This is contributed to the enhancement of the responsivity with the increase of temperature. When the temperature is higher than 125˚C, the integrated EL signal decreases rapidly, resulting in the drop of the CTR. The modeled CTR drops to 8.6 and 3.96 when the temperature is 325˚C and 425˚C, respectively.

Table 7.6 Normalized integrated EL signal, light wavelength and responsivity of RD-RD and RD-OPC [33], [34]

T (˚C)	Normalized L_{EL} of RD	λ (nm) of RD	R (A/W) of RD	R (A/W) of OPC
-200	149	606	0.17	2.7×10^{-4}
-175	145	607	0.17	5.86×10^{-4}
-75	140	617	0.22	0.0033
25	100	630	0.21	0.043
125	44.9	644	0.22	0.14

225	11.1	658	0.22	0.21
325	2.51	672	0.21	0.25
425	1.07	684	0.19	0.28

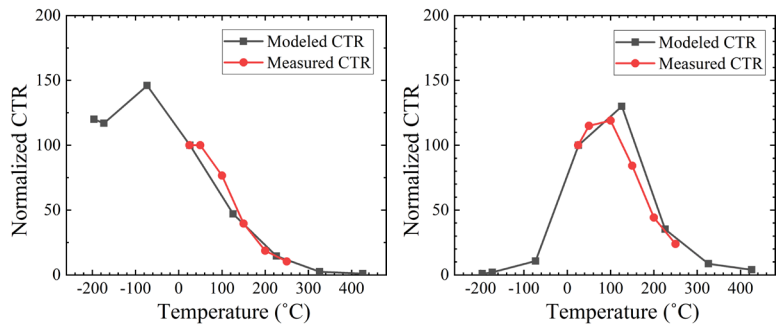


Fig. 7.11 Normalized CTR of (a) RD-RD, and (b) RD-OPC

The photocurrent current and leakage current strongly affect the noise and SNR of the optocouplers. SNR is defined as the ratio of the signal power and noise power, which can be expressed as [30]:

$$SNR = \frac{I_{ph}^2}{B(\sigma_{th}^2+\sigma_{sh}^2+\sigma_{lk}^2)} \tag{5}$$

Where B is the bandwidth of the photodetector, and σ_{th}^2, σ_{sh}^2 and σ_{lk}^2 are thermal noise, shot noise and dark current noise, which can be expressed as:

$$\sigma_{th}^2 = 4kT/R_L \tag{6}$$

$$\sigma_{sh}^2 = 2qI_{ph} \tag{7}$$

$$\sigma_{lk}^2 = 2qI_{lk} \tag{8}$$

Where k is the Boltzmann constant, T is temperature, R_L is the load resistance (i.e., 15 kΩ in fig 7.9), q is the electron charge, and I_{lk} is the leakage current. In terms of (6) to (8), the noise components of the optocouplers at 25ºC and 250 ºC are summarized in Table 7.7. As shown in Table 7.7, for the proposed LTCC-based high-temperature optocouplers, thermal noise and shot

noise are the dominant noise at both 25ºC and 250ºC. On the other hand, for the commercial optocoupler (i.e., IL300), dark current noise becomes the dominant noise at 250ºC due to the increase of the leakage current at elevated temperatures.

Table 7.7 Noise components of the optocouplers at 25ºC and 250ºC

	25ºC			250 ºC		
	σ_{th}^2 (W/Hz)	σ_{sh}^2 (W/Hz)	σ_{lk}^2 (W/Hz)	σ_{th}^2 (W/Hz)	σ_{sh}^2 (W/Hz)	σ_{lk}^2 (W/Hz)
RD-RD	1.1×10^{-24}	1.77×10^{-24}	6.86×10^{-30}	1.84×10^{-24}	2.3×10^{-25}	1.34×10^{-28}
RD-OPC	1.1×10^{-24}	4.29×10^{-23}	1.46×10^{-27}	1.84×10^{-24}	4.36×10^{-24}	5.12×10^{-26}
RD-3RD	1.1×10^{-24}	7.8×10^{-24}	2.2×10^{-29}	1.84×10^{-24}	1.08×10^{-23}	3.6×10^{-28}
RD-3OPC	1.1×10^{-24}	1.08×10^{-22}	3.42×10^{-27}	1.84×10^{-24}	1.92×10^{-23}	1.97×10^{-25}
IL300	1.1×10^{-24}	9.6×10^{-23}	1.48×10^{-27}	1.84×10^{-24}	2.3×10^{-23}	1.06×10^{-22}

The response time of RD-3RD is at the same magnitude as RD-RD, while the response time of RD-3OPC is three times higher than RD-OPC. The response time is considered as propagation delay, rise time and fall time. The propagation delay is the time difference between 50% of the final value of input and output. The rise time and fall time are defined as the time difference between the output signal changing from 10% to 90% of its final value. Ideally, the rise time is equal to the fall time, which is defined as [35], [36]:

$$\tau = \sqrt{(2.2\tau_{RC})^2 + \tau_{drift}{}^2 + \tau_{diff}{}^2} \tag{5}$$

Where τ_{RC} is the RC time constant, τ_{drift} is the drift time of carriers in the depletion region, and τ_{diff} is the diffusion time of the carriers. The RC time constant is defined as:

$$\tau_{RC} = R_L C_j \tag{6}$$

Where R_L is the load resistance, and C_j is the junction capacitance of the detectors. The junction capacitance can be expressed as:

$$C_j = \frac{\varepsilon_r \varepsilon_0 A}{W_d} \tag{7}$$

Where ε_r is the dielectric constant of the device, ε_0 is the permittivity of free space, A is the area of the depletion region, and W_d is the width of the depletion region.

Table 7.8 shows the measured junction capacitance, RC time constant and rise/fall time of the optocouplers while R_L is 15 kΩ (Fig 7.9). The capacitance of 3RD is 52.7 pF, which is around three times higher than the RD (i.e., 18.5 pF). The capacitance of OPC and 3OPC are 387 pF and 1.2 nF, respectively. The junction capacitance of the detectors is proportional to their area. As shown in Table 7.6, the $2.2\tau_{RC}$ of RD-RD and RD-3RD is much lower than their rise/fall time. This indicates that the rise time and fall time of RD-RD and RD-3RD are dominated by the drift time and diffusion time of the carriers. Therefore, RD-RD and RD-3RD have the same magnitude of rise/fall time. In addition, for RD-OPC and RD-3OPC, the rise/fall time is equal to $2.2\tau_{RC}$. This indicates that the rise time and fall time of the RD-OPC and RD-3OPC are dominated by the RC time constant. Thus, the rise/fall time increases three times when an OPC is replaced by three OPCs in parallel, according to (7).

Table 7.8 Junction capacitance, RC time constant and rise/fall time of the optocouplers

	RD-RD	RD-3RD	RD-OPC	RD-3OPC
C_j (pF)	18.5	52.7	387	1200
$2.2\tau_{RC}$ (μs)	0.61	1.73	12.7	39.6
Rise/Fall time (μs)	4	4.6	12.7	40

7.6 Conclusion

High-temperature optocouplers based on LTCC packaging are fabricated and demonstrated as signal galvanic isolation devices for high-temperature applications. The high-temperature optocouplers with various emitters and detectors were fabricated and characterized to identify the coupling efficiency. It is determined that RD-RD and RD-OPC show relatively good optical coupling behaviors. The output current of RD-RD and RD-OPC is 5.5 μA and 134 μA, respectively. Meanwhile, RD-3RD and RD-3OPC are fabricated to improve the output current of the optocouplers. The measurement results show that the RD-3RD and RD-3OPC show output current of 24 μA and 337 μA, respectively. The optocouplers were also characterized over a wide range of temperatures (i.e., 25 ˚C to 250 ˚C). The CTR degrades at high temperatures, while the leakage current shows little degradation with varying temperatures. In addition, the response time of the optocouplers is also characterized with varying temperatures. It is observed that the response time shows low temperature sensitivity. RD-RD and RD-3RD have the same magnitude of response time, while RD-3OPC has a response time that is three times higher than RD-OPC. This is because the response time of RD-RD and RD-3RD is dominated by the drift time and diffusion time of the carriers, and the response time of RD-OPC and RD-3OPC is dominated by the RC time constant.

In conclusion, the LTCC-based high-temperature optocouplers (e.g, RD-3OPC and RD-OPC) are promising to operate as galvanic isolation devices up to 250˚C. Utilizing multiple detectors in parallel improves the CTR. However, it also increases the junction capacitance and decreases the response speed. Moreover, the isolation voltage of the optocouplers is related to the distance between the emitter and the detector. Increasing the distance elevates the isolation voltage. However, it may reduce the CTR. Therefore, the trade-off among CTR, response speed and isolation voltage will be investigated in future experiments.

7.7 References

[1] N. Kaminski: State of the art and the future of wide band-gap devices, 13th European Conference on Power Electronics and Applications, Barcelona (2009).

[2] O. Kononchuk, B.-Y. Nguyen: Silicon-on-Insulator (SOI) Technology: manufacture and Applications, Elsevier (2014).

[3] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, K. Shiozaki: A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices, IEEE Transactions on Power Electronics, (2014), doi: 10.1109/TPEL.2013.2279950.

[4] M.H.Weng , Clark D.T., Wright S.N., Gordon D.L., Duncan M.A., Kirkham S.J., Idris M.I., Chan H.K., Young R.A.R., Ramsay E.P., Wright N.G., Horsfall A.B: Recent advance in high manufacturing readiness level and high temperature CMOS mixed-signal integrated circuits on silicon carbide, semicond. Sci. Technol., 32 (5) (2017), Article 054003.

[5] M. Barlow, S. Ahmed, H. A. Mantooth, A. M. Francis: An integrated SiC CMOS gate driver", Proc. Conf. IEEE Appl. Power Electron. Conf. Expo. (APEC), (2016) 1646-1649, doi: 10.1109/APEC.2016.7468087.

[6] B.R. Mehta, Y.J. Reddy: Industrial Process Automation Systems: Design and Implementation, Butterworth-Heinemann (2014).

[7] J. N. Khan: Design considerations in using the inverter gate driver optocouplers for variable speed motor drives, White Paper, Avago Technologies, (2010).

[8] V. Nguyen, L. Kerachev, P. Lefranc and J. Crebier: Characterization and Analysis of an Innovative Gate Driver and Power Supplies Architecture for HF Power Devices With High dv/dt, IEEE Transactions on Power Electronics, 32 (2017) 6079-6090, doi: 10.1109/TPEL.2016.2619859.

[9] Z. Zhang, K. Yao, G. Ke, K. Zhang, Z. Gao, Y. Wang, X. Ren, Q. Chen: SiC MOSFETs Gate Driver With Minimum Propagation Delay Time and Auxiliary Power Supply With Wide Input Voltage Range for High-Temperature Applications, IEEE Journal of Emerging and Selected Topics in Power Electronics, 8 (1) (2019 Nov 4), pp. 417-428, doi: 10.1109/JESTPE.2019.2951358.

[10] D. M. Products: Dual Current to Current Opto-Isolator, Micropac Industries, Houston (2005).

[11] Z. Jun, Y. X. Fei, L. Meng Lin and S. Hailin: Research on LTCC - based Flat Optocoupler Assembly Technology, 2018 19th International Conference on Electronic Packaging Technology (ICEPT), (2018) 841-849, doi: 10.1109/ICEPT.2018.8480497.

[12] Yu, G., Pakbaz, K. and Heeger, A.J.: Optocoupler made from semiconducting polymers. Electron. Mater. 23, (1994) 925–928.

[13] D. Li, W. Li, L. Duan, G. Zhang, S. Liu and G. Dong: Highly Integrable Organic Optocouplers on a Patterned Double-Side Indium Tin Oxide Substrate With High Isolation Voltage, IEEE Electron Device Letters, 36 (2015) 171-173, doi: 10.1109/LED.2014.2379276.

[14] D. Li, G. Dong, L. Duan, D. Zhang, L. Wang and Y. Qiu: High-Performance Organic Optocouplers Based on an Organic Photodiode With High Blue Light Sensitivity, IEEE Electron Device Letters, 34 (2013) 1295-1297, doi: 10.1109/LED.2013.2274522.

[15] Onsemi: High-Temperature Phototransistor Optocoupler in Half-Pitch Mini-Flat 4-Pin Package, FODM8801 datasheet, (Oct. 2021).

[16] A. Sabbar, S. Madhusoodhanan, S. Al-Kabi, B. Dong, J. Wang, S. Atcitty, R. J. Kaplar, D. Ding, H. A. Mantooth, S.Q. Yu, Z. Chen: Systematic Investigation of Spontaneous Emission Quantum Efficiency Drop up to 800 K for Future Power Electronics Applications, IEEE Journal of Emerging and Selected Topics in Power Electronics, (8) (2020 No. 1), pp. 845-853 doi: 10.1109/JESTPE.2018.2882775.

[17] A. Sabbar, S. Madhusoodhanan, B. Dong, J. Wang, H. A. Mantooth, S.Q. Yu, Z. Chen: High-Temperature Spontaneous Emission Quantum Efficiency Analysis of Different InGaN MQWs for Future Power Electronics Applications, IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2995120.

[18] A. Sabbar, S. Madhusoodhanan, S. Al.Kabi, B. Dong, J. Wang, S. Atcitty, R. Kaplar, D. Ding, A. Mantooth, S.-Q. Yu, Z. Chen: High Temperature and Power Dependent Photoluminescence Analysis on Commercial Lighting and Display LED Materials for Future Power Electronic Modules, Sci. Rep., 9 (2019), p. 16758, doi: https://doi.org/10.1038/s41598-019-52126-4.

[19] A. Sabbar, S. Madhusoodhanan, S. Atcitty, R. Kaplar, D. Ding, A. Mantooth, S.Q. Yu, Z. Chen: High-Temperature Optical Characterization of GaN-Based Light-Emitting Diodes for Future Power Electronic Modules, Phys. Status Solidi A, (18), (Dec. 2019), doi: https://doi.org/10.1002/pssa.201900792.

[20] S. Madhusoodhanan and A Sabbar et al. "High-Temperature Optical Characterization of GaN-Based Light-Emitting Diodes for Future Power Electronic Modules," in Phys. Status Solidi A, 18, Dec. 2019, doi: https://doi.org/10.1002/pssa.201900792.

[21] S. Madhusoodhanan, A. Sabbar, H. Tran, B. Dong, J. Wang, H. A. Mantooth, S.Q. Yu, Z. Chen: High-Temperature Analysis of GaN-based MQW Photodetector for Optical Galvanic Isolations in High-Density Integrated Power Modules, IEEE Journal of Emerging and Selected Topics in Power Electronics, (2020), doi: 10.1109/JESTPE.2020.2974788.

[22] Vishay Semiconductors: Linear Optocoupler, High Gain Stability, Wide Bandwidth, IL300 datasheet, (Mar. 2018).

[23] Vishay Semiconductors: Optocoupler, Phototransistor Output, SOP-4, AC Input, Mini-Flat Package, SFH691AT datasheet, (Apr. 2013).

[24] Ardebili, Haleh, Jiawei Zhang, and Michael G. Pecht. Encapsulation technologies for electronic applications. William Andrew, 2018.

[25] B. Jiang, J. Haber, A. Renken, P. Muralt, L. Kiwi-Minsker, T. Maeder: Fine Structuration of low-temperature co-fired ceramic (LTCC) microreactors, Lab Chip, 15 (2015), pp. 563-574, doi: 10.1039/c4lc01105h.

[26] P. Sun, X. Cui, S. Huang, P. Lai, Z. Zhao and Z. Chen: LTCC Based Current Sensor for Silicon Carbide Power Module Integration, IEEE Transactions on Power Electronics, (Feb. 2022), pp. 1605-1614, doi: 10.1109/TPEL.2021.3104284.

[27] HC Semitek: LED Chip For Display, T12A-WB datasheet, (2018).

[28] Marktech Optoelectronics: LED Chip Visible, OPC6900-21 datasheet.

[29] S. Madhusoodhanan, A. Sabbar, S. Atcitty, R.J. Kaplar, A. Mantooth, S.Q. Yu, Z. Chen: High-Temperature Analysis of GaN-Based Blue-LEDs for Future Power Electronic Applications, IEEE J. Emerg. Sel. Top. Power Electron., 8 (2020), pp. 4186-4190, doi: 10.1109/JESTPE.2019.2945166.

[30] R. Hui: Introduction to Fiber-Optic Communications, London, United Kingdom Academic Press, (2019).

[31] Johnson, Shane R., et al. Excitation dependent photoluminescence measurements of the nonradiative lifetime and quantum efficiency in GaAs, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 25.3 (2007): 1077-1082, doi: https://doi.org/10.1116/1.2720864.

[32] J. Piprek: Handbook of Optoelectronic Device Modeling and Simulation, Boca Raton, FL, USA: CRC Press, (2018).

[33] Sabbar, A., Madhusoodhanan, S., Tran, H. et al. Design and optimization of high temperature optocouplers as galvanic isolation. Sci Rep 12, 2228 (2022). https://doi.org/10.1038/s41598-021-04145-3.

[34] Madhusoodhanan, S., Sabbar, A., Tran, H. et al. High-temperature analysis of optical coupling using AlGaAs/GaAs LEDs for high-density integrated power modules. Sci Rep 12, 3168 (2022). https://doi.org/10.1038/s41598-022-06858-5.

[35] E. F. Schubert: Light-Emitting Diodes, New York, USA, Cambridge University Press, (2006).

[36] A. O. Goushcha and B. Tabbert: On response time of semiconductor photodiodes, Optical Enginering, 59 (2017), doi: https://doi.org/10.1117/1.OE.56.9.097101.

CHAPTER 8

HIGH-TEMPERATURE SIC POWER MODULE WITH INTEGRATED LTCC-BASED GATE DRIVER

8.1 Abstract

This paper proposes a high-temperature SiC power module. High-temperature gate drivers were fabricated on low temperature co-fired ceramic (LTCC) substrates and integrated into the power module. LTCC-based High-temperature optocouplers, which were fabricated in-house, are used as isolation devices for the gate drivers. A detailed fabrication process of the high-temperature SiC power module is presented. High-temperature components and materials are utilized for the packaging. The fabricated high-temperature SiC power module was characterized by a double pulse test at both 25ºC and 100ºC. The turn-on and turn-off times are ~100 ns. The device showed small oscillations during turn-on, while the overshoot during the device turn-off is ~35 V.

8.2 Introduction

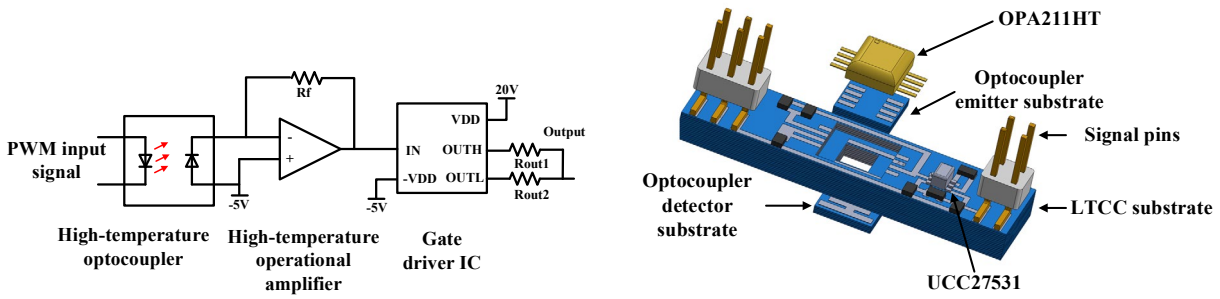
Silicon carbide (SiC) is one of the most commonly used materials in power applications due to its wide energy bandgap, high electric field strength and high thermal conductivity [1]. This significantly increases the power rating, operating voltage, and power density of power modules [2]. Despite the superior temperature tolerance of SiC power devices, the working temperature of power modules is still limited by packaging materials and other passive components. Moreover, to reduce the parasitic elements and improve the switching behaviors, gate driver circuitry is designed to be tightly integrated with the power devices. As a result, the operating temperature of the gate driver is required to be similar to that of the power devices. In order to improve the operating temperature and reduce the size and weight of power systems, a high-temperature SiC half-bridge power module with integrated gate drivers is proposed in this paper. High-temperature

packaging materials are utilized for the encapsulation of the power module. Low temperature co-fired ceramic (LTCC) is used as the substrate of the gate driver circuits. High-temperature optocouplers are used as the galvanic isolation devices of the gate drivers, which achieves a compact size for the gate driving circuits. These approaches allow the gate driver boards to be closely integrated into the SiC power module.

8.3 Design and Simulation

In order to mitigate gate parasitics and increase the power density of the SiC power module, high-temperature gate driver circuits are designed and integrated into the power module for both the high-side and low-side switches. Fig. 8.1(a) shows the schematic of the gate driver. A high-temperature optocoupler is used as the galvanic isolation device, which protects the low-voltage logic controller from the high-power devices. A transimpedance amplifier (TIA) is designed by using a high-temperature operational amplifier (i.e., OPA211HT by Texas Instruments (TI)). It converts the photocurrent from the optocoupler to a voltage signal for a gate driver integrated circuit (IC). The gate driver IC (UCC27531 by TI) is utilized to provide sufficient voltage and current to drive the power devices. The three-dimensional (3D) model of the gate driver is shown in Fig. 8.1(b). LTCC substrates are designed and fabricated for the gate driver circuit. The LTCC substrates have the capacity to withstand high operating temperatures (i.e., 400ºC) [3]. They have also been demonstrated to be easily integrated into power modules [4]. Slots were designed on both the top and bottom sides of the LTCC substrates for the integration of the high-temperature optocoupler. Commercial optocouplers do not promise to operate at high temperatures as the degradation of output current and leakage current affect the operation of the gate driver circuits. Thus, LTCC-based high-temperature optocouplers were developed in house and designed to be compatible with the LTCC substrates. Previous works [5], [6] describe the detailed fabrication

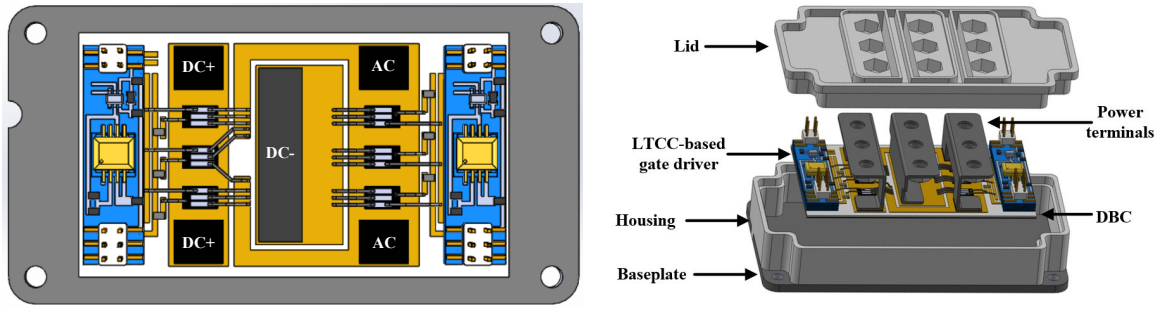
process and characteristics of high-temperature optocouplers. After the fabrication of the LTCC substrates, the optocoupler emitter and detector substrates are integrated into the slots. Then other components (e.g., OPA211HT, UCC27531, resistors and signal pins) are attached to the top layer of the LTCC substrate by high-temperature conductive epoxy (CW2400 by Chemtronics).



(a) (b)

Fig. 8.1 (a) Schematic and (b) 3D model of the proposed LTCC-based gate driver

The layout of the proposed SiC power module is shown in Fig. 8.2(a). 1.2 kV, 149 A SiC MOSFETs (CPM3-1200-0013A from CREE) were integrated into the power module. For this module, each switching position has one device. However, it can be extended to three devices in parallel (Fig. 8.2a). As shown in Fig. 8.2(a), a symmetrical layout was designed to enhance the current balance and improve the thermal distribution. Two LTCC-based gate drivers are attached to the direct bonded copper (DBC). The output pads of the LTCC-based gate driver are on the bottom layer, which allows the gate driver to connect with the power devices by copper traces (on DBC) and bond wires. The short gate loop traces significantly reduce the gate loop parasitic inductance. Fig. 8.2(b) shows the 3D model of the proposed power module. The DC+ and DC- power terminals are placed facing each other to enhance the mutual inductance, which helps to decrease the power loop parasitic inductance. Moreover, the power terminals are designed almost as wide as the DBC (i.e., ~40 mm) to reduce the power loop parasitic inductance.



(a) (b)

Fig. 8.2 (a) Layout and (b) 3D model of the proposed high-temperature SiC power module

The parasitic inductance in the power loop and gate loop affects the switching behaviors of the power module. Thus, both power loop and gate loop parasitic inductances are simulated and extracted by ANSYS Q3D. The source and sink were applied to the output pad (on the bottom layer of the LTCC substrate) of the LTCC-based gate driver and the gate pad of the power device to extract the gate loop inductance, while the DC+ and DC- terminals were set as source and sink during the power loop inductance extraction. The simulation results are shown in Fig. 8.3. Due to the close proximity between the gate driver and power devices, the parasitic inductance of the simulated gate loop is 3 nH at 1 MHz. The power loop inductance simulated from the DC+ terminal to the DC-terminal is 10 nH at 1 MHz.

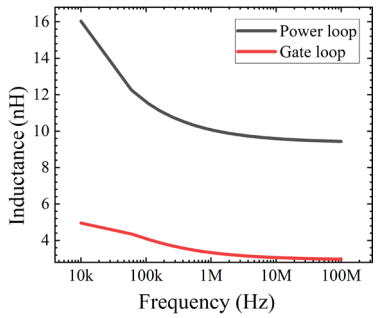


Fig. 8.3 Simulated parasitic inductance versus operating frequency.

A thermal simulation was also carried out to investigate the temperature distribution of the power module. Fig. 8.4 shows the result of the thermal simulation. The power devices were set as

heat flow with a 150 W (power rating) of power dissipation, and the ambient temperature was set at 200ºC. As shown in Fig. 8.4, the maximum temperature is ~256ºC, which is located at the junction of the power devices. The temperature of the LTCC-based gate driver is ~200ºC.

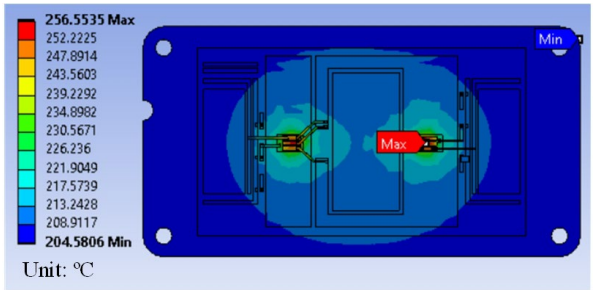
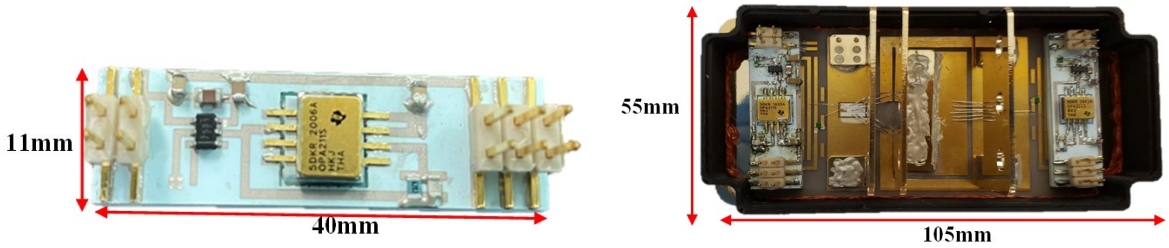


Fig. 8.4 Simulated Thermal distribution

8.4 Experimental Results

The fabricated LTCC-based gate driver and high-temperature SiC power module are shown in Fig. 8.5(a) and (b), respectively. The widths and lengths of the gate driver and power module are shown in the figure, and the heights of the gate driver and power module are ~5 mm and ~18 mm, respectively. The fabrication process of the high-temperature power module is shown in Fig. 8.6. A gold-plated copper base plate was utilized as the heat sink, and an aluminum nitride (AlN) based DBC, which has a similar coefficient of thermal expansion (CTE) to the base plate, was used as the substrate. The power devices were attached to the DBC by silver sintering. A high-thermal-conductive die attach adhesive (H9890-6A from NAMICS), which has a 300ºC melting point, was utilized as the solder paste. After the die attachment, wire bonding was completed to achieve the connection. Then the power terminals and LTCC-based gate drivers were attached. The power terminals were attached with high-thermal-conductive die attach adhesive (H9890-6A), and the LTCC-based gate drivers were attached with high-temperature conductive epoxy (CW2400). Finally, the power module was encapsulated in high-temperature resin and epoxy (EP17HT-LO by Master Bond) to achieve the passivation.



(a) (b)

Fig. 8.5 Fabricated (a) LTCC-based gate driver, and (b) high-temperature SiC power module

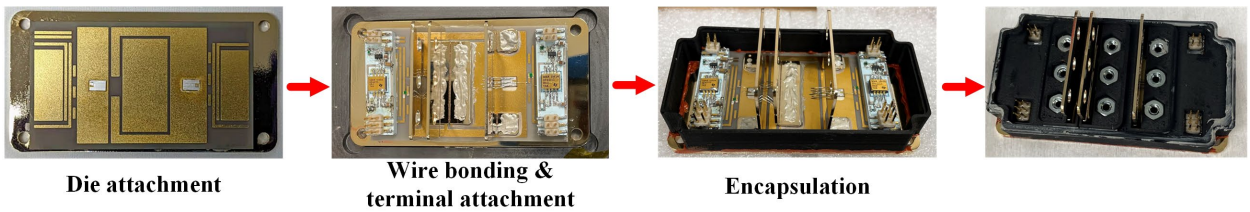
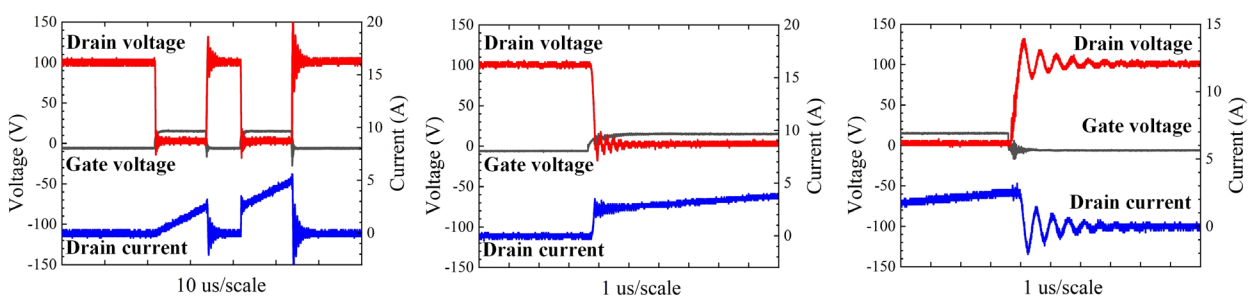


Fig. 8.6 Fabrication process of the high-temperature SiC power module

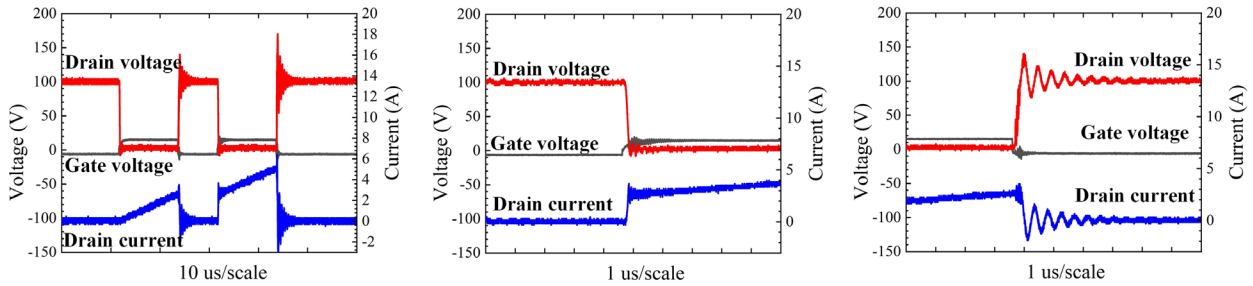
A double pulse test (DPT) was carried out to investigate the switching behaviors of the fabricated high-temperature SiC power module. The DPT results at 25ºC are shown in Fig. 8.7(a) to (c). The gate voltage is -5 V to 15 V, and the drain-source voltage is 100 V. As shown in Fig. 8.7(b) and (c), the turn-on and turn-off time of the power device is ~100 ns. The device shows small oscillations during turn-on, and the overshoot of the turn-off is ~35 V. In addition, the gate signal shows oscillations during the turn-off. This may be caused by the layout of the LTCC-based gate driver as the gate and source traces are narrow on the LTCC substrate.



(a) (b) (c)

Fig. 8.7 Double pulse test results of the high-temperature SiC power module with integrated LTCC-based gate drivers at 25ºC (a) overview, (b) turn-on, and (c) turn-off

The high-temperature SiC power module was heated by a hot plate (PC-600D by Corning) to investigate its high-temperature behaviors. Fig. 8.8 shows the DPT results of the high-temperature SiC power at 100ºC. The result does not show much difference from the one at 25ºC. The overshoot during the device turn-off increases from 35 V to 38 V.



(a) (b) (c)

Fig. 8.8 Double pulse test results of the high-temperature SiC power module with integrated LTCC-based gate drivers at 100ºC (a) overview, (b) turn-on, and (c) turn-off

8.5 Conclusions

In order to improve the high-temperature performance and reduce the size and weight of SiC power modules, a high-temperature SiC power module with integrated gate drivers were designed and fabricated. The gate drivers was fabricated based on LTCC substrates to achieve operations at high temperatures. A detailed fabrication process of the high-temperature SiC power module is presented in this paper. A double pulse test was carried out at both 25ºC and 100ºC to characterize the switching performance of the fabricated power module. The switching performance did not show much degradation from 25ºC to 100ºC.

In general, the proposed high-temperature SiC power module shows reliable switching behaviors at 25ºC and 100ºC. Double pulse tests at higher temperatures (e.g., 200ºC) and drain-

source voltages (e.g., 1000 V) will be performed in future work to further investigate the proposed power module. The layout of the LTCC-based gate driver will also be improved to enhance its driving capability.

8.6 Acknowledgments

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8.7 References

[1] J. A. Powell, "Silicon carbide a high temperature semiconductor", CECON'83 Cleveland Electrical/Electronics Conf. and Expo., pp. 28-32, Oct. 1983., doi: https://ntrs.nasa.gov/citations/19840006864.

[2] B. Whitaker et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2606-2617, May 2014, doi: 10.1109/TPEL.2013.2279950.

[3] B. Jiang, J. Haber, A. Renken, P. Muralt, L. Kiwi-Minsker, T. Maeder: Fine Structuration of low-temperature co-fired ceramic (LTCC) microreactors, Lab Chip, 15 (2015), pp. 563-574, doi: 10.1039/c4lc01105h.

[4] P. Sun, X. Cui, S. Huang, P. Lai, Z. Zhao and Z. Chen, "LTCC Based Current Sensor for Silicon Carbide Power Module Integration," in IEEE Transactions on Power Electronics, vol. 37, no. 2, pp. 1605-1614, Feb. 2022, doi: 10.1109/TPEL.2021.3104284.

[5] P. Lai et al., “Development of LTCC-packaged Optocouplers as Optical Galvanic Isolation for High-Temperature Applications”, submitted to Scientific Reports.

[6] S. Madhusoodhanan et al., “High-Temperature Analysis of Optical Coupling Using AlGaAs/GaAs LEDs for High-Density Integrated Power Modules”, accepted by Scientific Reports in Jan. 2022.

CHAPTER 9

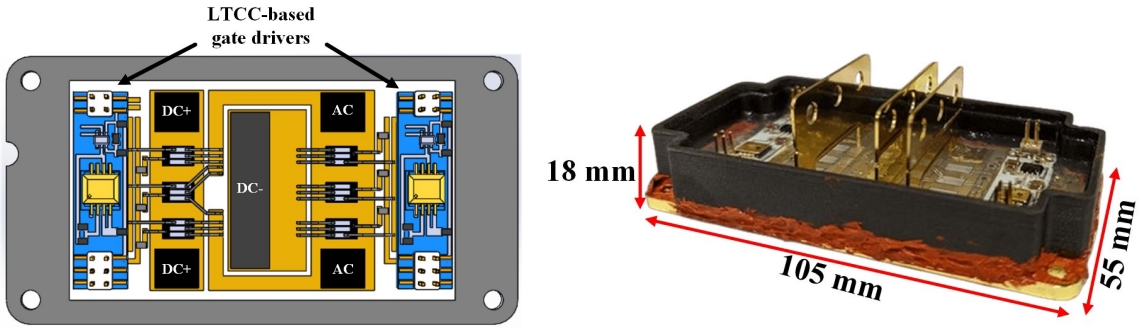
HIGH-TEMPERATURE MEASUREMENTS ON SIC POWER MODULE WITH INTEGRATED LTCC-BASED GATE DRIVER

9.1 Introduction

In Chapter 8, a high-temperature half-bridge power module with integrated LTCC-based gate drivers was proposed. However, each switching position of the power module has only one device, which limits the operating current. In this chapter, a high-temperature half-bridge power module with three power MOSFETs (i.e., CPM3-1200-0013A from CREE) in each switching position has been fabricated. The power module was characterized from 25 ºC to 200 ºC at 600 V drain-source voltage.

9.2 Experimental Results

Fig. 9.1(a) shows the layout of the SiC high-density half-bridge power module. 1.2 kV SiC power MOSFETs from CREE are integrated into the power module. Each position has three devices in parallel. Two LTCC-based gate drivers are attached on the DBC and connected to the power devices with bond wires. The fabrication process and the utilized materials of the power module have been presented in Chapter 8. The fabricated power module is shown in Fig. 9.1(b).



(a) (b)

Fig. 9.1 High-temperature SiC half-bridge power module (a) layout and (b) fabricated sample

Double pulse tests (DPTs) were carried out on the high-density HT power module from 25 ºC to 200 ºC to characterize its switching performance. A function generator (Rigol DG1022) was used to generate a double pulse signal with a 4 µs pulse width, and the power module was heated by a Corning PC-600D hot plate. Fig. 9.2 shows the thermal map of the DPT at 200 ºC.

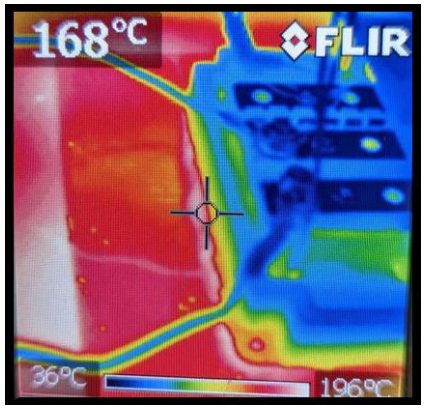
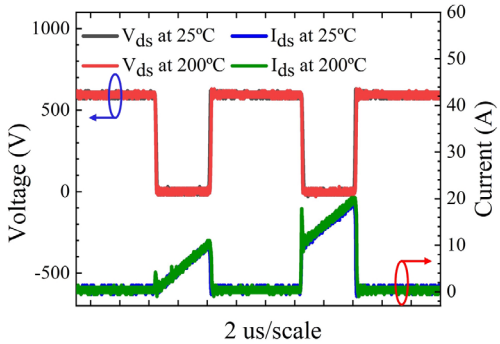


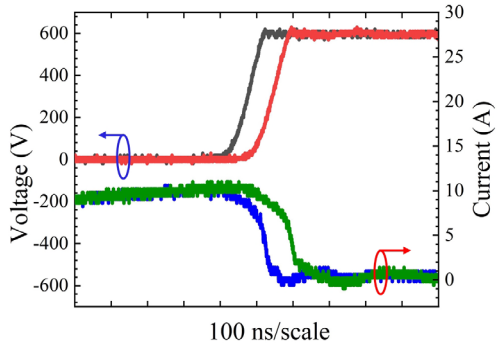
Fig. 9.2 Thermal map of the DPT for the high-density HT power module at 200 ºC

The DPT results at 25 ºC and 200 ºC are shown in Fig. 9.3. The power module was tested at 600 V, 20 A and showed reliable switching performance from 25 ºC to 200 ºC. Very few oscillations were observed at turn-on and turn-off, and the switching behavior shows little degradation with the varying temperatures. As shown in Fig. 9.3(b), for the turn-off period, the sum of the current fall time and voltage rise time, at which the switching loss is generated, increases from ~160 ns to ~170 ns when the temperature varies from 25 ºC to 200 ºC. As shown in Fig. 9.3(c), for the turn-on period, the sum of the current rise time and voltage fall time, at which the switching loss is generated, changes from ~200 ns to ~180 ns when the temperature varies from 25 ºC to 200 ºC. The turn-on pulse width decreases from 4 µs to ~3.9 µs at 200 ºC due to the degradation of the HT optocoupler output current at elevated temperatures. In addition, the reverse

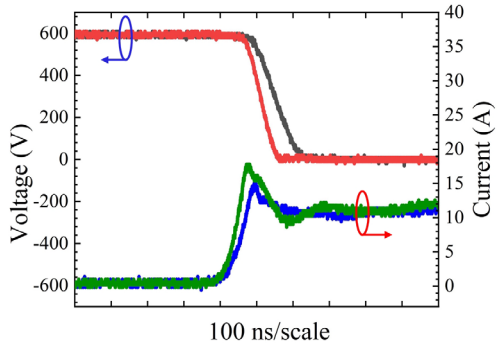
recovery current increases from ~5 A to ~8A with the temperature varying from 25 ºC to 200 ºC. This may be due to the reduction in the body diode forward voltage with temperature.



(a)



(b)



(c)

Fig. 9.3 DPT results of the high-density HT SiC half-bridge power module at 25 ºC and 200 ºC (a) overview, (b) turn-off and (c) turn-on.

9.3 Conclusion

In this chapter, a high-temperature half-bridge power module with three power MOSFETs in each switching position has been fabricated. The power module was characterized from 25 ºC to 200 ºC at 600 V drain-source voltage. The turn-on and turn-off of the power module show little degradation from 25 ºC to 200 ºC, while the turn-on pulse width decreases from 4 µs to ~3.9 µs at 200 ºC due to the degradation of the optocoupler. In general, the power module shows reliable switching performance at elevated temperatures.

CHAPTER 10

CONCLUSION AND FUTURE WORK

10.1 Conclusion

This dissertation studies the on-chip ESD protection and galvanic isolation of SiC-based power module systems, which aims to improve the chip- and system-level reliability of the system.

In order to design and fabricate on-chip ESD protection devices for SiC-based ICs, SiC-based Ohmic contact and ion implantation have been studied. To fabricate SiC-based Ohmic contact, CTLM structures were fabricated on 4H-SiC P-type substrates. Experimental results show that Ni/Ti/Al is capable of forming Ohmic contacts on SiC P-type samples, and the specific contact resistivity decreases with the increase of Ti thickness. For SiC-based ion implantation, the ion implantation profiles are designed and simulated by Sentaurus TCAD software. SIMS results show high match with the simulation results.

SiC-based ESD protection devices, such as NMOS, LDMOS, HV-SCR and LV-SCR, have been fabricated. TLP and VF-TLP were utilized to characterize their ESD performance. Among these devices, HV-SCR shows the highest I_{t2} per µm (i.e., 33 mA/µm) under TLP measurements, which is ~100 times higher than SiC LDMOS. This indicates that the SiC-based HV-SCR can be used as an area-efficient ESD protection device. In addition, a SiC LV-SCR structure was proposed to achieve low V_{t1}. Both TLP and VF-TLP measurements were conducted to investigate the ESD behaviors of the SiC LV-SCR. The SiC LV-SCR failed before its turn-on under TLP measurements. For VF-TLP measurements, the LV-SCR triggered at 175 V and failed at 2.8 A.

On the other hand, for system-level reliability, optical-based high-temperature galvanic isolators (i.e., optocouplers) for SiC-based power modules are developed. LTCC was utilized as the packaging material. The LTCC-based high-temperature optocouplers show promising driving

capability and steady response speed from 25 ºC to 250 ºC. Then LTCC-based gate drivers that utilize the high-temperature optocouplers as galvanic isolators were designed and fabricated. The LTCC-based gate drivers were integrated into a high-temperature SiC-based power module to improve the high-temperature performance and reduce the size and weight of the power system. Finally, DPTs from 25 ºC to 200 ºC were carried out to characterize the power module. The power module shows reliable switching performance at elevated temperatures.

10.2 Future Work

Although SiC-based ESD protection devices and high-temperature galvanic isolators have been designed and fabricated, future work needs to be conducted to further improve their performance. Firstly, SiC Ohmic contact resistivity needs to be improved. Various types of metal stacks with varying annealing temperatures will be carried out. Secondly, the V_{t1} and V_h of the fabricated SiC ESD protection devices are too high to protect low-voltage SiC ICs. New ESD protection structures need to be proposed to achieve suitable V_{t1} and V_h. Thirdly, the response speed of the LTCC-based optocouplers is relatively lower than commercial room-temperature optocouplers, which limits the switching speed of the power module. Therefore, high-temperature optical fibers will be used as the galvanic isolator to improve the switching speed.

APPENDIX: PUBLICATIONS

Journals

[1] **P. Lai** et al., "Area-Efficient Silicon Carbide SCR Device for On-Chip ESD Protection," in IEEE Transactions on Electron Devices, vol. 69, no. 6, pp. 3022-3028, June 2022, doi: 10.1109/TED.2022.3166471.

[2] **P. Lai** et al., "Development of High-Temperature Optocouplers as Galvanic Isolation for Power Electronic Applications," Scientific Reports, vol. 12, 11286, 2022, doi: https://doi.org/10.1038/s41598-022-15631-7.

[3] **P. Lai** et al., "Investigation of parasitic bipolar transistor in rail-based electrostatic discharge (ESD) protection circuits," IEICE Electronics Express, vol. 16, 2019, doi: https://doi.org/10.1587/elex.16.20190306.

[4] D. Gonzalez, **P. Lai**, S. Chinnaiyan *et al*., "Development of High-Temperature Optocouplers for Gate Drivers Integrated in High-Density Power Modules," in *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2022.3229324. (D. Gonzalez and **P. Lai** contributed equally to this work).

[5] H. Wang, **P. Lai** et al., "Area-efficient dual-diode with optimized parasitic bipolar structure for rail-based ESD protections," Microelectronics Reliability, vol. 123, Aug. 2021, doi: https://doi.org/10.1016/j.microrel.2021.114194.

[6] P. Sun, X. Cui, S. Huang, **P. Lai**, Z. Zhao and Z. Chen, "LTCC Based Current Sensor for Silicon Carbide Power Module Integration," in IEEE Transactions on Power Electronics, vol. 37, no. 2, pp. 1605-1614, Feb. 2022, doi: 10.1109/TPEL.2021.3104284.

[7] P. Sun, Y. Guo, T. Wu, Z. Zhao, **P. Lai**, Z. Chen et al., "An online junction temperature monitoring correction method for SiC MOSFETs at different parasitic parameters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2021.3117734.

[8] S. Madhusoodhanan, A. Sabbar, H. Tran, **P. Lai** et al, "High-temperature analysis of optical coupling using AlGaAs/GaAs LEDs for high-density integrated power modules," Scientific Reports, vol. 12, 2022 doi: https://doi.org/10.1038/s41598-022-06858-5.

[9] S. Ahmed, **P. Lai** et al., "Design and Analysis of Integrated LTCC-Based Gate Driver for High-Temperature SiC Power Module", submitted to IEEE Transactions on Power Electronics, under review.

Conferences

[1] **P. Lai** et al., "Investigation of ESD Protection in SiC BCD Process," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2019, pp. 405-409, doi: 10.1109/WiPDA46397.2019.8998959.

[2] **P. Lai** et al., "High-Temperature SiC Power Module with Integrated LTCC-Based Gate Driver," CS MANTECH, 2022.

[3] S. Ahmed, **P. Lai**, S. Chinnaiyan, A. Mantooth, Z. Chen, "High-Temperature (250oC) SiC Module Integrated with LTCC-Based Isolated Gate Driver", accepted by Applied Power Electronics Conference (APEC) 2023.

[4] F. Diao, **P. Lai**, F. Guo, X. Du, P. Sun, Y. Zhao, Z. Chen, "A Medium-Voltage Multilevel Hybrid Converter Using 3.3 kV Silicon Carbide MOSFETs and Silicon IGBT Modules", accepted by Applied Power Electronics Conference (APEC) 2023.

[5] A. Abbasi, S. Roy, R. Murphree, A. Rashid, M. Hossain, **P. Lai** et al., "Characterization of a Silicon Carbide BCD Process for 300°C Circuits," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2019, pp. 231-236, doi: 10.1109/WiPDA46397.2019.8998920.
[6] S. Chinnaiyan, **P. Lai**, S. Ahmed, A. Mantooth, Z. Chen, "Demonstration and Optimization of a 250°C LTCC-based Gate Driver for High Density, High-Temperature Power Modules", accepted by 11th International Conference on Power Electronics – ECCE Asia (ICPE 2023-ECCE Asia).
[7] H. Wang, **P. Lai**, Z. Chen, "Current Injection Effect on ESD Behaviors of the Parasitic Bipolar Transistors inside P+/N-well diode", accepted by IEEE International Reliability Physics Symposium (IRPS).

Patents

[1] Z. Chen, H. A. Mantooth, S.Q. Yu, D. Gonzalez, **P. Lai**, S. Madhusoodhanan, "High-Temperature Integrated Power Module with Optical Galvanic Isolation", United States Patent, Approved, Oct. 2022.